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SAR ADC in 22 nm FDSOI

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Problem Description

The continuous downscaling of CMOS technologies provides new challenges and opportunities for energy efficient SAR ADCs. The main objective of this project is to design an energy efficient SAR ADC in a 22 nm FDSOI CMOS technology for application in medical ultrasound imaging applications. The following work flow is suggested.

- Choose the most promising architecture and develop a behavioural model
- Use the model to derive specifications for the different building blocks
- Implement the ADC on transistor level
- Do the layout of the ADC
- Verify the ADC design based on netlist extracted from layout

The SAR ADC should satisfy the following specifications.

- Resolution: At least 10 bits ENOB
- Sampling rate: 100 MHz
- Power: Minimize
- Power supply: Optimize
- Bulk bias voltage: Optimize
- ADC category: Nyquist

The specifications of the SAR ADC needs to be verified post-layout by simulations on an extracted netlist of the ADC.

Summary

Successive Approximation (SAR) Analog-to-Digital Converters (ADCs) are among the most energy efficient ADCs and has therefore received enormous attention in medical and wireless applications. The great energy efficiency of SAR ADCs are mainly attributed to the downscaling of Complementary Metal-Oxide-Semiconductor (CMOS) circuits, since the SAR architecture benefits greatly by going to smaller and smaller CMOS process nodes. Due to this excellent scaling, the introduction of smaller CMOS nodes opens up for new opportunities and challenges when designing SAR ADCs.

In this thesis, the speed limits of SAR ADCs have been pushed, while high resolution and energy efficiency are maintained. The SAR designed in this thesis is a Nyquist ADC intended for medical ultrasound applications and is designed in a 22 nm Fully Depleted Silicon-On-Insulator (FDSOI) process. The designed SAR ADC is simulated post-layout and the mean Monte Carlo results yields an Effective Number of Bits (ENOB) of 10.2 bits at a sample rate of 100 MS/s. The power consumption is 268 μW and the resulting mean Monte Carlo Walden Figure of Merit (FoM) for the ADC is 2.29 fJ/conv.-step. This is currently better than all state-of-the-art ADCs with similar specifications. The ADC designed is also unique in the sense that no one else has managed similar speed and resolution with the same simple pure SAR ADC architecture.

These results are accomplished by using a popular dynamic latch comparator with capacitive loading, improving on already existing bootstrapped switch topology, improvement on already existing Capacitive Digital-to-Analog Converter (CDAC) architecture to greatly increase linearity and still achieve small unit capacitance, a custom made digital circuitry that has very low propagation delay and clock generation based on CDAC bottom plate.

Sammendrag

Suksessiv Approksimasjon (SAR) Analog-til-Digital Konverter (ADC) er blant den mest energieffektive datakonverter arkitekturen og har derfor mottatt enormt mye oppmerksomhet innen medisinske og trådløse applikasjoner. Energieffektiviteten er hovedsakelig på grunn av nedskaleringen av Komplementær Metall-Oksid-Halvleder (CMOS) kretser, siden SAR arkitekturen skalerer utmerket med mindre og mindre CMOS prosessnoder. På grunn av denne eksepsjonelle skaleringen, vil introduksjon av nye prosessnoder gi nye muligheter og utfordringer ved design av SAR datakonvertere.

I denne masteroppgaven har hastighetsgrensen til SAR datakonvertere blitt presset til nye grenser, mens oppløsningen og energieffektivitet er vedlikeholdt. SAR datakonverteren i denne oppgaven er en Nyquist ADC beregnet for bruk innen medisinsk ultralyd applikasjoner designet i en 22 nm Fullstendig Utarmet Silisium-på-Isolator (FDSOI) prosess. Datakonverteren laget i denne masteroppgaven er simulert etter utlegg og oppnår en gjennomsnittlig Monte Carlo Effektiv Antall Bits (ENOB) på 10.2 bits med en punktprøvefrekvens på 100 MS/s. Effektforbruket til datakonverteren er på 268 μW og resulterende gjennomsnittlig Monte Carlo Walden godhetstall på 2,29 fJ/conv.-step. Dette er per dags dato bedre enn all annen state-of-art datakonvertere med lignede spesifikasjoner. Datakonverteren laget i denne oppgaven er også unik da ingen har tidligere klart å lage en enkel ren SAR ADC med samme hastighet og oppløsning samtidig.

Disse resultatene er oppnådd ved å bruke en populær dynamisk komparator med kapasitiv last, forbedring av allerede eksisterende samplingsbryter topologi, forbedring av en allerede eksisterende Kapasitiv Digital-til-Analog Konverter (CDAC) arkitektur for å øke linearitet og likevel oppnå en liten enhetskapasitans, en tilpasset digital krets med veldig lav forplantningsforsinkelse og klokke generering basert på CDAC bunnplate.

Preface

This master thesis concludes 5 years at Norwegian University of Science and Technology (NTNU) at Department of Electronic Systems (IES). The time frame for this project has been 20 weeks starting from January 15th and includes literature search, behavior modelling, schematic design, layout and post-layout verification of a SAR ADC. The project has been done under supervision of Professor Trond Ytterdal with IES.

I would like to thank Professor Trond Ytterdal for always being available for questions and for excellent guidance during our weekly meetings. It has been great and I look forward continue as your Ph.D. student starting fall 2018.

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Glossary

ADC Analog-to-Digital Converter. ii–iv, 3, 4, 7, 9–15, 17–19, 21–23, 27–29, 36, 38, 39, 41, 43, 45, 49–59, 61–64, 67, 83

BOX Buried Oxide. 7, 8

CDAC Capacitive Digital-to-Analog Converter. ii, iii, 3, 4, 10, 11, 13, 14, 16–19, 21, 22, 28, 29, 36, 38–40, 42, 43, 45, 47, 54, 56, 58, 61–63, 67, 83

CMOS Complementary Metal-Oxide-Semiconductor. ii, iii, 3, 8, 15, 16

DAC Digital-to-Analog Converter. 9, 49, 50, 56

DNL Differential Nonlinearity. 49

DRC Design Rule Check. 23, 47

ENOB Effective Number of Bits. ii, iii, 10, 14, 15, 17–19, 21, 23, 26, 36, 45, 46, 49–58, 61, 62, 64, 67

ESD Electrostatic Discharge. 50

FDSOI Fully Depleted Silicon-On-Insulator. ii, iii, 4, 7, 8, 23, 35, 62, 67

FFT Fast Fourier Transform. 50, 56

FoM Figure of Merit. ii, 23, 28, 50, 51, 53, 57–59, 61, 62, 67

IES Department of Electronic Systems. iv

INL Integral Nonlinearity. 49

ISSCC International Solid-State Circuits Conference. 61

LSB	Least Significant Bit. 12, 28
LSBs	Least Significant Bits. 45
LVT1	Low Treshold Voltage 1. 23–27, 33
LVT2	Low Treshold Voltage 2. 23–27
M1	Metal 1. 36, 43, 44, 47
M2	Metal 2. 43, 44, 47
M3	Metal 3. 43–45
M4	Metal 4. 43–45
M5	Metal 5. 36
MOM	Metal-Oxide-Metal. 36, 43, 62
MOSFET	Metal Oxide Semiconductor Field Effect Transistor. 15, 16, 18, 25, 33
MSB	Most Significant Bit. 12, 13, 17, 28
nMOS	n-channel MOSFET. 8, 23–27, 29–31, 33, 39, 51, 53
NTNU	Norwegian University of Science and Technology. iv, 67
PDK	Process Design Kit. 7, 8, 36, 51, 53, 62
pMOS	p-channel MOSFET. 8, 23–27, 29–31, 33, 39, 47, 51, 53
PVT	Process-Voltage-Temperature. 39, 64
RMS	Root Mean Square. 9, 10, 21, 22, 32
SAR	Successive Approximation. ii–iv, 3, 4, 7, 10–12, 14, 17–19, 21, 23, 28, 29, 36, 38, 39, 45, 49, 50, 58, 61, 62, 64, 67, 83
SINAD	Signal to Noise and Distortion Ratio. 10, 21–23, 49, 50, 52, 56
SPICE	Simulation Program for Integrated Circuits Emphasis. 23
VLSI	Very Large Scale Integration. 7, 61

Chapter 1

Introduction

The continuous downscaling of Complementary Metal-Oxide-Semiconductor (CMOS) technology is mainly motivated by more energy efficient digital circuits. While digital circuits benefit greatly from going to smaller process nodes, analog design in nanoscale CMOS nodes becomes increasingly more difficult. The trend is towards more and more digital chips, but analog circuits are still necessary. One such analog circuit is the Analog-to-Digital Converter (ADC) that provides the interface between the analog and digital domain. Many ADC topologies do exist, but when it comes to energy efficiency, the current trend would indicate that Successive Approximation (SAR) ADCs are among the most energy efficient ADCs [1]. The SAR ADC topology is very simple and consists of just a comparator, a Capacitive Digital-to-Analog Converter (CDAC), a digital control circuit and a sampling switch. The simple architecture makes SAR ADCs very attractive and suitable for smaller process nodes, as many of the blocks scale very well with smaller nodes, especially the digital circuitry.

The SAR topology has proven itself suitable for a wide range of specifications. The SAR handles low speed and high accuracy[1] applications [2], but is also suited for high speed and low accuracy[2] applications [3]. However, applications that may require high speed and high resolution using a pure simple SAR ADC has yet to emerge. If one considers hybrid solutions, then the SAR assisted digital slope ADC [4], interleaved subranging SAR ADC with $\Delta\Sigma$ [5], two-step SAR ADC [6], pipelined SAR ADC [7] are topologies that can satisfy the requirement needed for a high speed and high resolution ADC. However, the ADCs mentioned are not pure SAR ADCs and this increases the design complexity. The SAR ADC presented in [8] is a pure SAR ADC with high resolution and high speed, but uses a dual reference voltage scheme and the ADC needs to be calibrated. This severely increases the power consumption and complexity of the ADC and makes the ADC less attractive. The approaches presented above are interesting, but a simple pure SAR ADC with similar specifications do not exists as of yet.

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[1] speed < 10 MS/s, resolution > 10 bits

[2] speed > 50 MS/s, resolution < 10 bits

1.1 Goal of This Thesis

The goal of this thesis is to design a pure SAR ADC with efficiency comparable to state-of-the-art ADC designs. The ADC should push the limits in terms of speed and still manage high resolution. The ADC should be verified post-layout using a commercially available 22 nm Fully Depleted Silicon-On-Insulator (FDSOI) process. The specifications for the ADC can be found in Table 1.1.

Table 1.1: Specifications for the ADC

Resolution	> 10 bits ENOB
Sampling frequency	100 MS/s
Power	Minimize
Power supply	Optimize
Bulk bias voltage	Optimize
ADC category	Nyquist

1.2 Main Contributions

The main contributions of this thesis are.

- Behaviour modelling, schematic design, layout design and post-layout verification of a high speed, high accuracy SAR ADC in 22 nm FDSOI
- Error budgeting for error distribution and to obtain specifications for the different subcircuits
- Use of a popular comparator topology with capacitive loading at certain nodes to enhance noise performance
- Improvement on already existing bootstrapped switch topology by reducing transistor count and by bulk to gate connection of switching transistor. This saves power and area and the linearity of the switch is increased
- Improvement on already existing CDAC topology. The result is a very linear CDAC and small unit capacitance
- Clock generation based on CDAC bottom plate and with additional feed forwards from the comparator
- Custom made digital logic to achieve very low propagation delay and fast switching speed that is suitable for high speed
- Use of a hybrid switching technique using split-monotonic switching and monotonic switching with a common-mode decrease during switching
- Utilization of bulk biasing of digital circuitry for speed increase

1.3 Thesis Outline

This thesis will be organized as follows.

Chapter 2 - Theory: Background theory needed for this thesis is covered.

Chapter 3 - High Level Design: High level design choices and error budget is presented.

Chapter 4 - Implementation: A detailed description of the different subcircuits implemented.

Chapter 5 - Results: Test bench and post-layout results are presented.

Chapter 6 - Discussion: Comparison to state-of-the-art and discussion of results.

Chapter 7 - Conclusion: Concluding remarks and future works are described.

Chapter 2

Theory

This chapter will cover with some of the background theory needed for this thesis. The subsequent sections will show the transistor architecture used in this thesis and some key parameters of a quantized signal. Thereafter, the SAR ADC will represented as a block diagram and explained briefly. The internal switching operation in a SAR ADC will be explained and analyzed, followed by presentation of two practical switching algorithms. Afterwards, some noise theory will be presented along with sources of distortion in a SAR ADC. Finally, digital buffers driving large capacitive loads will be covered.

2.1 Transistors

This section will present the transistor technology used in this thesis. The general transistor structure will be presented, followed by theory on the flipped-well architecture available in the used Process Design Kit (PDK).

2.1.1 Fully Depleted Silicon On Insulator

As Moore's law is approaching the end, transistor development has to take another path other than just reducing the gate length of the transistor. Not only is there a fundamental limit for the gate length, but leakage current is also a major issue in Very Large Scale Integration (VLSI), where millions (and billions) of transistors are put on a single chip. Facing these problems, it is obvious one has to move away from the conventional bulk process and develop new techniques to enhance transistor performance. One suggested contender to the well established bulk process is the FDSOI transistor structure. In a FDSOI process, a Buried Oxide (BOX) is grown directly on the substrate and then a very thin fully depleted silicon layer is deposited on the BOX as seen in Figure 2.1. The fully depleted silicon act as the transistor's channel and the small thickness of the channel lowers the doping effort needed. In some devices, the channel is even left undoped. The lower doping of the channel reduces the stochastic mismatch since the doping variability is lowered and it also increases the mobility of the transistor due to less impurities in the channel from doping.

The lower amount of impurities in the channel also improves the flicker noise performance of the transistor due to fewer collisions.

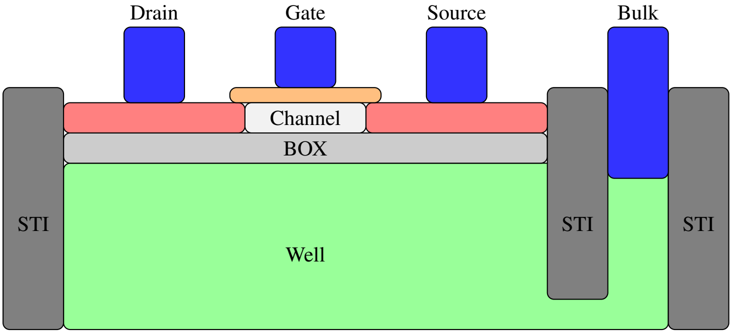

Figure 2.1: General FDSOI transistor structure.

The leakage current is also reduced with this architecture, as the insulating nature of the BOX reduces the bulk leakage current compared to a conventional CMOS bulk process. Since the substrate is now insulated from the source/drain contacts by the BOX, the parasitic PN junctions between the substrate and source/drain are completely eliminated. This makes biasing of the bulk a much more viable option than in a conventional bulk process. Not only due to lack of the PN junctions, but also because the channel is more sensitive to bulk biasing. This allows for optimization of speed and power by just biasing the bulk of the transistor.

2.1.2 Flipped-Well

FDSOI transistor technology offers much more variation when it comes to well placements for transistors. One example of this is the flipped-well architecture available in a FDSOI process. The flipped-well configuration allows n-channel MOSFET (nMOS) transistors to reside in a N-well, while the p-channel MOSFET (pMOS) reside in a P-well as seen in Figure 2.2. This well configuration is in contrast to normal bulk transistor technology where the well placement is opposite.

The main motivation for this well configuration is that it allows for enhancement of speed by biasing the bulks of the transistor at the cost of increased leakage current. For the N-well, a positive voltage between 0 to +2V can be applied to the N-well contact to lower the threshold voltage of the transistor, while the P-well can be biased with voltage between -2V to 0 to lower the threshold voltage. The lowered threshold voltage increases the speed of the devices since the overdrive is increased. For the P-well, a deep N-well has to be utilized to avoid biasing the entire substrate. This is not necessary for the N-well, as the N-well is formed on top of the substrate in "isolated" patches. In the used 22 nm FDSOI PDK, the flip-well configuration is only available to certain low threshold devices. The conventional well configuration is of course also present for devices with higher threshold voltages.

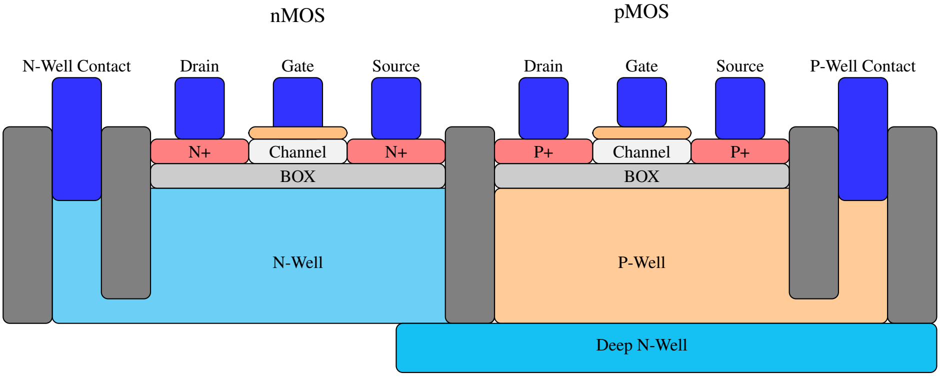
nMOS
pMOS
N-Well Contact
Drain
Gate
Source
Drain
Gate
Source
P-Well Contact
N+
Channel
N+
P+
Channel
P+
BOX
BOX
N-Well
P-Well
Deep N-Well

Figure 2.2: Flip-well architecture for nMOS and pMOS.

2.2 Quantization

Quantization is the process to quantize the amplitude of an analog signal for bit representation. The quantization process inherently introduces noise to the quantized signal due to the finite number of quantization intervals. To analyze certain properties of quantization, assume now that a signal v_{in} is first digitized by an N bit ADC and then converted back to the analog domain by an N bit Digital-to-Analog Converter (DAC) as in Figure 2.3.

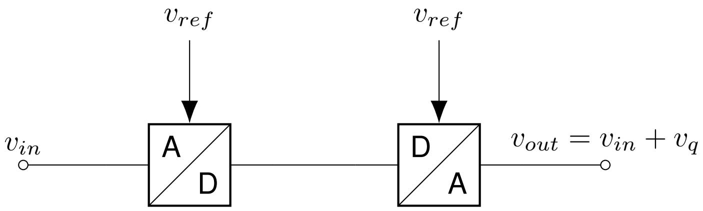
v_{ref}
v_{ref}
v_{in}
A
D
D
A
$v_{out} = v_{in} + v_q$

Figure 2.3: Quantization of v_{in} to obtain v_{out}.

The output signal $v_{out} = v_{in} + v_q$ now contains the input signal v_{in} along with a small error term v_q. The term v_q is not a constant, but is bound as

$$|v_q| \leq v_{ref}/2^{N+1} \tag{2.1}$$

This bound shows that the best resolution we can get is no better than $v_{ref}/2^N$ and this quantity is referred to as V_{LSB}. The term v_q is stochastic and is typically approximated as being white in the frequency domain. This is a good approximation if N is high and if v_{in} varies rapidly. With these assumptions, it can be shown [9] that v_q is a zero mean signal with Root Mean Square (RMS) value of

$$v_{q,RMS} = \frac{v_{ref}}{2^N\sqrt{12}} \tag{2.2}$$

Now that the RMS value of the quantization error has an analytical expression, it is possible to define a Signal to Noise and Distortion Ratio (SINAD) for the quantization process. In order to do this, assume an input sinusoid with input swing from 0 to v_{ref}. Such a sinusoid has a RMS value of $v_{in,RMS} = v_{ref}/(2\sqrt{2})$ and the output SINAD is thus

$$\begin{aligned} \text{SINAD} &= 20\log_{10}\left(\frac{v_{in,RMS}}{v_{q,RMS}}\right) && (2.3)\\ &= 20\log_{10}\left(\sqrt{3/2}\cdot 2^N\right) && (2.4)\\ &= 6.02N + 1.76 \quad [\text{dB}] && (2.5) \end{aligned}$$

Eq. (2.5) shows that the SINAD only depends on the number of bits N. This result is only valid for an ideal ADC. A realistic ADC would have lower SINAD due to noise and distortion in the ADC that reduces SINAD that in turn also lowers the number of bits N. For a practical ADC, it is more common to define a new quantity Effective Number of Bits (ENOB) to reflect actual resolution of the converter. If one define $N = \text{ENOB}$ for such an ADC and rearrange Eq. (2.5), one can obtain ENOB as

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad [\text{bits}] \tag{2.6}$$

Eq. (2.6) gives ENOB in number of bits and the input SINAD is given in decibel.

2.3 Charge Redistribution SAR ADC Topology

A SAR ADC architecture finds the digital output word B_{out} by doing a binary search internally in the ADC. This is typically done by using a CDAC and the operation of finding the output digital word is based on charge redistribution. To get a better understanding of the SAR ADC architecture, the SAR ADC in Figure 2.4 will be briefly be explained. For the differential architecture as seen in Figure 2.4, the following is done for each conversion:

1. The differential input voltage $v_{in} = v_{in}^{+} - v_{in}^{-}$ is initially sampled at the CDAC top plates nodes v_{top}^{+} and v_{top}^{-} through the sampling switches.
2. The SAR Logic will then generate a clock signal to the comparator. The comparator then in turns compares the CDAC top plates voltages v_{top}^{+} and v_{top}^{-} that triggers either output v_{op} or v_{on} from the comparator high.
3. The output signals v_{op} and v_{on} are passed to the SAR Logic that generates control signals that go the CDAC. These control signals causes internal capacitors in the CDAC to have their bottom plates switched to a different potential.
4. This switching changes the differential voltage top plate voltage $v_{top}^{+} - v_{top}^{-}$ by $v_{ref}/2^i$ for $i = 1, 2, 3, ..., (N-1)$, where N is the number of bits and v_{ref} is a reference voltage. The differential change in voltage gets smaller for each bit conversion.
5. After the voltage on the top plate has settled, this procedure is again repeated until all bits have been resolved.

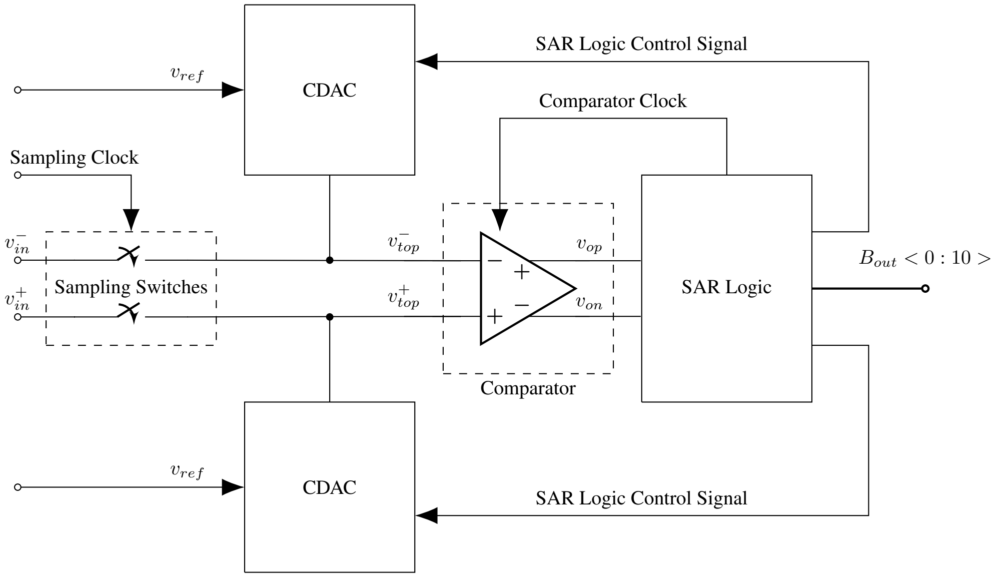
v_{ref}
CDAC
SAR Logic Control Signal
Comparator Clock
Sampling Clock
v_{in}^-
v_{in}^+
Sampling Switches
v_{top}^-
v_{top}^+
v_{op}
v_{on}
Comparator
SAR Logic
$B_{out} < 0:10 >$
v_{ref}
CDAC
SAR Logic Control Signal

Figure 2.4: General differential SAR topology.

The output digital word is then found at $B_{out} < 0 : 10 >$ and the ADC once again samples the differential input voltage for another conversion. It is seen that he conversion to the digital domain is done successively in a binary fashion by changing the top plate voltage by $v_{ref}/2^i$. This is how the SAR architecture gets its name. How the switching of the CDAC is performed is up to the designer as there exist many possibilities with different trade-offs such as complexity, power and common-mode voltage variations.

2.4 CDAC Switching

A charge redistribution SAR ADC does the conversion to the digital domain by switching capacitors. In this section, charge redistribution will be analyzed and two switching algorithms will be reviewed.

2.4.1 Charge Redistribution

A charge redistribution SAR ADC does the conversion from the analog domain to the digital domain by capacitor switching. To understand how this procedure work, the 3 bit CDAC shown in Figure 2.5 is used as an example without loss of generality, as the same principle is applicable for a N bit CDAC. Assume now that the top plate of the capacitors in Figure 2.5 has initially potential v_{top} and the total charge Q accumulated at the top plate is

$$Q = (4C + 2C + C)(v_{top} - v_{ref}) + Cv_{top} \tag{2.7}$$

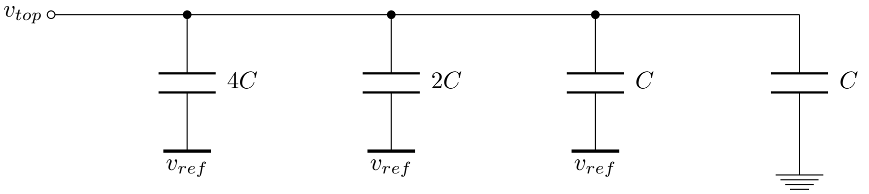

Figure 2.5: 3 bit CDAC with top plate voltage v_{top}.

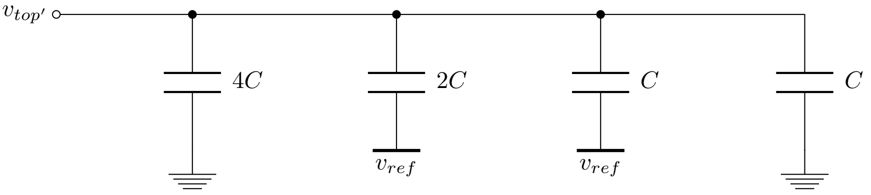

Figure 2.6: 3 bit CDAC with top plate voltage v'_{top}.

If the Most Significant Bit (MSB) capacitor is now switched to v_{ref} as seen in Figure 2.6, the top plate voltage is now changed to a different voltage potential v'_{top} due to charge conservation. The total charge Q on the top plate is in this case the same as in Figure 2.5 and can be written as

$$Q = (2C + C)(v'_{top} - v_{ref}) + (4C + C)v'_{top} \tag{2.8}$$

Due to charge conservation, the following holds true for the total charge Q on the top plate

$$3C(v'_{top} - v_{ref}) + 5C(v'_{top}) = 7C(v_{top} - v_{ref}) + Cv_{top} \tag{2.9}$$

Eq. (2.9) can be solved for v'_{top} to yield

$$v'_{top} = v_{top} - \frac{v_{ref}}{2} \tag{2.10}$$

Eq. (2.10) shows that this switching decreased the top plate voltage v_{top} by $v_{ref}/2$. This exercise is only done for the MSB capacitor, but similar calculation can be done for Least Significant Bits (LSBs) capacitors. The end result is that the top plate voltage decrements by the ratio $\frac{v_{ref}}{2^i}, i = 1, 2, ..., (N-1)$, for each capacitor switched. Lower values of capacitance switched decreases the top plate voltage by a smaller amount for each bit. It is this type of capacitor switching that is done internally in the SAR ADC to perform the binary search. The top plate voltage can also be incremented by $\frac{v_{ref}}{2^i}$. This is done by having all the capacitors' bottom plate initially at ground and then switch each capacitor one by one to v_{ref}.

2.4.2 Monotonic Switching

Monotonic switching [10] is a non-differential charge redistribution switching technique. The algorithm is based on comparing both top plates voltages v^+_{top} and v^-_{top}, but only one of these voltages is changed for each bit conversion by capacitor switching. As an example, consider the MSB conversion, if $v^+_{top} > v^-_{top}$, then v^+_{top} is decremented by $\frac{v_{ref}}{2}$ and $B_0 = 1$. If $v^+_{top} < v^-_{top}$, then then v^-_{top} is decremented by $\frac{v_{ref}}{2}$ and $B_0 = 0$. This process is repeated for all the remaining bits, but the voltage subtracted from the top plate voltage is smaller for each bit. The full algorithmic description is shown in Figure 2.7.

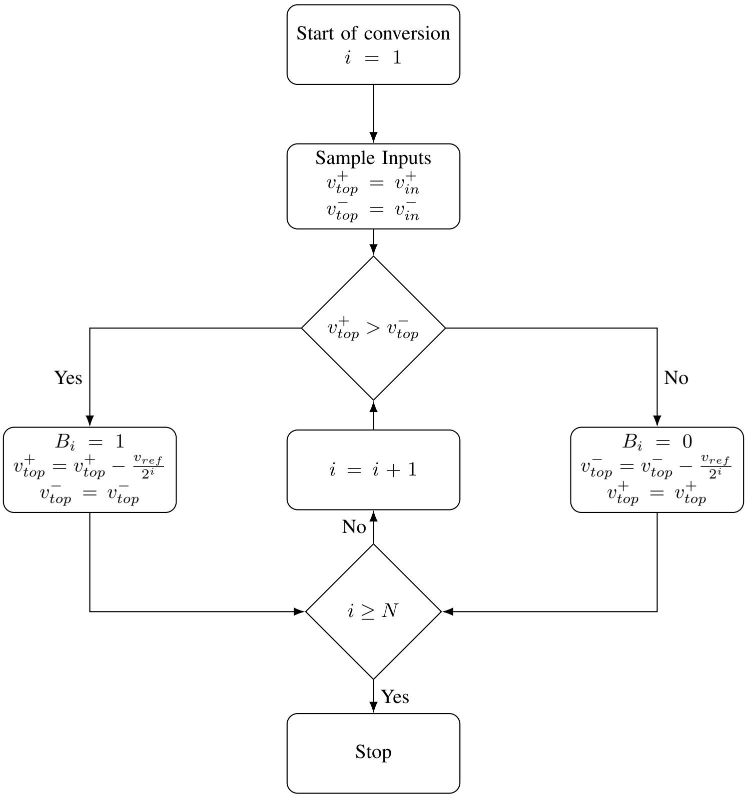
Start of conversion
$i = 1$
Sample Inputs
$v^+_{top} = v^+_{in}$
$v^-_{top} = v^-_{in}$
$v^+_{top} > v^-_{top}$
Yes
No
$B_i = 1$
$v^+_{top} = v^+_{top} - \frac{v_{ref}}{2^i}$
$v^-_{top} = v^-_{top}$
$i = i + 1$
$B_i = 0$
$v^-_{top} = v^-_{top} - \frac{v_{ref}}{2^i}$
$v^+_{top} = v^+_{top}$
No
$i \geq N$
Yes
Stop

Figure 2.7: Flow chart description of monotonic switching.

Since only one side of the input (positive or negative) has its CDAC switched for each bit, it's classified as a non-differential operation. The consequence is that it will affect the common-mode voltage of the differential signal. For the scheme used in Figure 2.7, the result would be a fall in the common-mode voltage during conversion. One of the great advantages of monotonic switching is that it utilize top plate sampling. In short, it means that only a $(N-1)$ bit CDAC is required since a comparison is made before any switching is performed. However, the ADC still requires N comparisons for N bit resolution.

2.4.3 Split-Monotonic Switching

The change in common-mode voltage makes monotonic switching troublesome to use, since it can be difficult for the comparator in the SAR ADC to handle. A large change in common-mode voltage might make the comparator too slow or increase the input referred noise, causing ENOB degradation. To preserve the common-mode voltage, a split-monotonic switching [11] technique can be used. The switching procedure is identical to that of the monotonic-switching, but the switching operation is now done differentially. Since the operation is differential, each top plate of the CDAC is now decremented/incremented by $\frac{v_{ref}}{2^{i+1}}$ instead of $\frac{v_{ref}}{2^i}$[1]. The algorithmic description is seen in Figure 2.8.

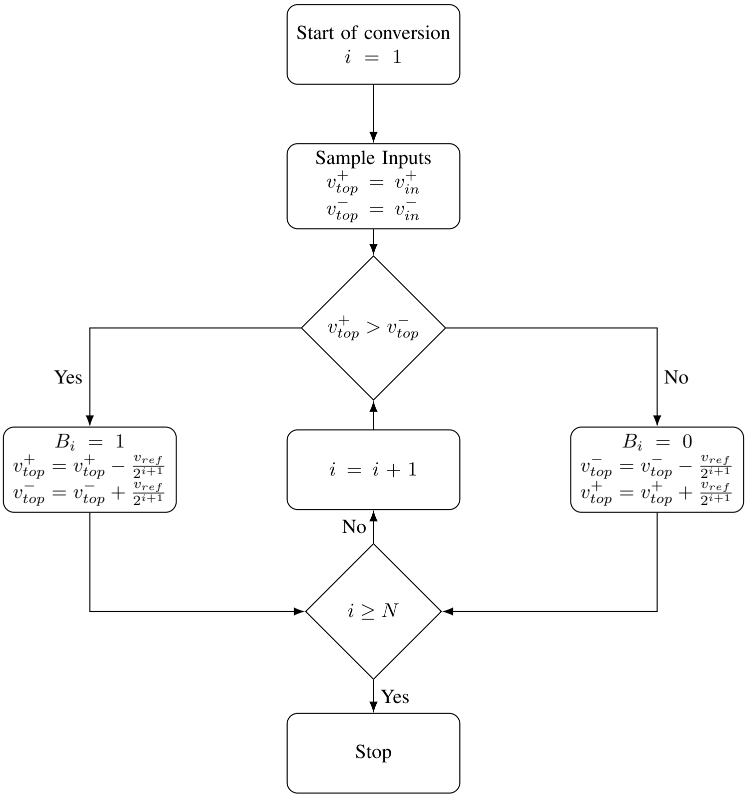
Start of conversion
$i = 1$
Sample Inputs
$v_{top}^+ = v_{in}^+$
$v_{top}^- = v_{in}^-$
$v_{top}^+ > v_{top}^-$
Yes
No
$B_i = 1$
$v_{top}^+ = v_{top}^+ - \frac{v_{ref}}{2^{i+1}}$
$v_{top}^- = v_{top}^- + \frac{v_{ref}}{2^{i+1}}$
$i = i + 1$
$B_i = 0$
$v_{top}^- = v_{top}^- - \frac{v_{ref}}{2^{i+1}}$
$v_{top}^+ = v_{top}^+ + \frac{v_{ref}}{2^{i+1}}$
No
$i \geq N$
Yes
Stop

Figure 2.8: Flow chart description of split-monotonic switching.

In terms of energy efficiency, behaviour simulations [12] show that split-monotonic switching on average require about twice the amount of switching energy compared to monotonic switching. Another disadvantage is that split-monotonic switching require more complicated routing since the number of nets to the CDAC doubles, which corresponds to area and power increase. In a practical ADC, it is common to employ split-monotonic switching for the first few bits and do the rest of the conversion with monotonic switching. This gives a good trade-off between common-mode voltage variations and energy.

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[1] The change in differential voltage is still $\frac{v_{ref}}{2^i}$ for split-monotonic switching

2.5 Noise

All electronic devices are sources of noise which causes degradation in signal integrity in an electronic circuit. For an ADC, noise will cause a degradation in ENOB. These signals are stochastic in nature, so a statistical approach is used to characterize noise. One typically describes noise with parameters of a statistical probability function (like mean or variance) or by using frequency-domain analysis. In CMOS circuits, noise can roughly be divided into thermal noise and flicker noise.

2.5.1 Thermal Noise

Thermal noise is due to the random motions of charge carriers due to their temperature. This kind of noise is proportional to absolute temperature and occurs in all resistors, even in semiconductor devices with resistivity[2]. The spectrum of thermal noise is modelled as being white in the frequency-domain and the time-domain amplitude of thermal noise follows a Gaussian probability density function.

2.5.2 Flicker noise

Flicker noise occurs mainly in active devices and this type of noise is not fully understood. One can attribute some flicker noise due to impurities (doping) in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) channel, but this is not the full picture. Flicker noise is a low frequency phenomena and the power spectrum is inversely proportional to frequency. There exists a simple empirical formula for the flicker noise's spectral density in MOSFET devices given by

$$v_{n,f}(f) = \frac{K}{WLC_{ox}f} \tag{2.11}$$

Where K is a constant dependent on device and process, WL is the gate area of the MOSFET and C_{ox} is the gate oxide capacitance. It is assumed that this noise source $v_{n,f}(f)$ is connected in series with the device's gate as shown in Figure 2.9a.

2.5.3 Noise in Active Devices

A MOSFET in the active region generates white noise due to the resistive channel. This noise can be modelled by a noisy drain current i_n as seen in Figure 2.9b. The spectral density of the current i_n has magnitude

$$i_n(f) = 4kT\gamma g_m \tag{2.12}$$

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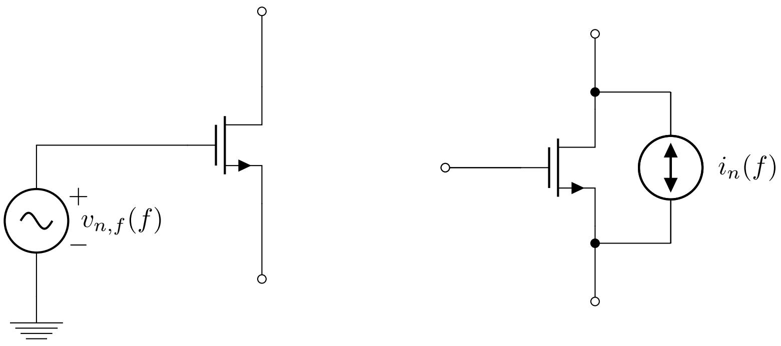
[2] For example in the resistive channel of a MOSFET device.



(a) MOSFET flicker noise model.

(b) MOSFET thermal noise model

Figure 2.9: Noise models for a MOSFET device.

where γ is a white noise parameter and g_m is the transconductance of the device. A long channel device has $\gamma = 2/3$, but γ can be higher for devices with shorter channels. The noisy current i_n can be replaced by a noisy voltage source $v_n(f)$ at the gate. This is done by dividing i_n by the transconductance squared g_m^2 of the transistor.

2.5.4 Resistor Noise

The noise in resistors and in MOSFET devices in the triode region can be modelled as being white in the frequency-domain with spectral density given by

$$v_{n,r}(f) = 4kTR \tag{2.13}$$

Where k is Boltzmann constant, T is the absolute temperature and R is the resistance of the device. This shows that the power spectral density $v_{n,r}(f)$ is proportional to R and is constant for all frequencies f. A practical example would be to connect this resistor to a capacitor C as seen in Figure 2.10. This is realistic, because all nodes in a CMOS circuit have some non-zero capacitance to the substrate. To make the analysis easier, the resistor is considered noiseless and the resistor noise $v_{n,r}(f)$ is put in series with the resistor. The connection in Figure 2.10 effectively forms a RC-filter that filters the noise. It can be shown that the total noise power $\sigma_{n,r}$ at the node $v_{out}(f)$ is now

$$\sigma_{n,r} = kT/c \tag{2.14}$$

The result in Eq. (2.14) is interesting, as the noise power $\sigma_{n,r}$ is not dependent on R, but proportional to the absolute temperature T and inversely proportional to C. The dependency on R is gone, since the pole frequency of the filter decreases inversely with R, but the noise spectral density increases proportionally with R. The net effect is that R is cancelled. kT/c is fundamental formula, because it shows that all nodes in the circuit will produce noise with magnitude kT/c. This noise is important to consider when dimensioning the CDAC, since using too small capacitors might lead to excessive noise.

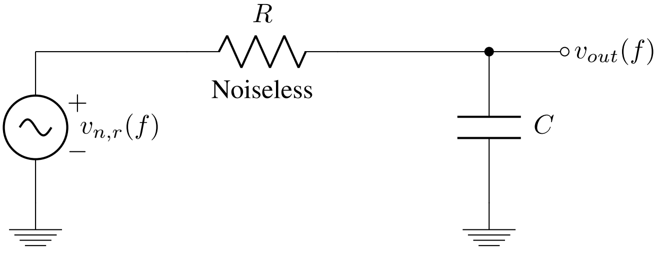


Figure 2.10: Resistor noise model with connection to capacitance for noise power calculation.

2.6 Distortion

There exist several sources of ENOB degradation in the SAR ADC. Some of these sources will be described here mathematically and qualitatively.

2.6.1 Settling Time

The CDAC top plate voltage can not change instantly in time, but its transient response is that of a RC-filter. This is due to the capacitance C from the CDAC and the resistance R from the switches at the bottom plate of the CDAC. When a unit step is applied to the RC-filter, the output response $v(t)$ will be

$$v(t) = 1 - e^{-t/\tau} \tag{2.15}$$

Where $\tau = RC$. It is readily seen from 2.15 that the error from steady state is proportional to the term $e^{-t/\tau}$. For a N bit SAR ADC, it's required that the top plate of the CDAC settles within 1 V_{LSB}. This is equivalent to

$$e^{(-t/\tau)} \leq 2^{-N} \tag{2.16}$$

The amount of time t needed for settling is thus given by

$$t = -\ln(2^{-N})\tau \tag{2.17}$$

It is seen that the required settling time is dependent on the number of bits, the CDAC capacitance C and the switch resistance R. For $N = 11$, the required time is $t = 7.62\tau$. This impose challenges for switching times, especially for SAR ADCs with high sampling frequency and many bits, since the MSB capacitor scales exponentially with N.

2.6.2 Comparator Offset

Comparator offset is a phenomena where the threshold of the comparator has been shifted. The end result is that small differential inputs gives the wrong output due to this offset. This offset is typically caused by mismatch of the input transistors or a mismatch of capacitance in the comparator. This offset can be of systematic nature or of random nature.

The systematic offset occurs when simulating post-layout, as perfect symmetrical layout is not possible. This offset can be corrected post-layout by simulations. The random offset is random in nature, it is not possible to correct this without calibration. However, one can increase the area of the input transistors or use more capacitance to reduce the effects of random offset.

2.6.3 Switch Distortion

The sampling switch in the SAR ADC is not ideal and it can be modelled as a resistor with resistance R_{on}. This resistance and the capacitance C from the CDAC forms a RC-filter as seen in Figure 2.11.

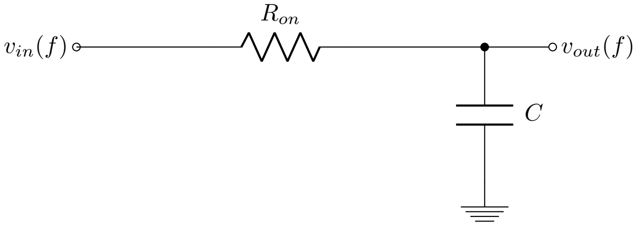


Figure 2.11: Sampling switch model with capacitive CDAC load.

If the switch is implemented by a MOSFET in the triode region, this resistance R_{on} can be approximated by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)} \tag{2.18}$$

Where μ_n is the mobility of the transistor, W/L is the ratio between the gate width and gate length, V_{GS} is the potential difference between the gate and source terminal and V_t is the threshold voltage of the transistor. Eq. (2.18) shows that the switch resistance R_{on} is dependent on the input signal through V_{GS}[3], but also V_t through the body effect. The switch and the CDAC forms a RC-filter with transfer function

$$H(f) = \frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{1 + \frac{j2\pi f}{2\pi R_{on} C}} \tag{2.19}$$

Where f is the input sinusoidal frequency to the switch and $j = \sqrt{-1}$. Since R_{on} now varies with the input signal, it is clear that the transfer function $H(f)$ is also signal dependent which results in signal dependent attenuation and phase shift through the switch. It is this non-constant attenuation and phase shift that causes non-linearity and therefore loss of ENOB.

---

[3] It doesn't matter where the source terminal is located, as both $v_{in}(f)$ and $v_{out}(f)$ will vary with the input signal v_{in}.

2.6.4 CDAC Non-Linearity

The CDAC will also cause reduction of ENOB due to non-linearity in the capacitor array. These non-linearities can be divided into systematic mismatches and random mismatches in the capacitor array. The systematic mismatch of the capacitor array can be lowered by making the boundary conditions as uniform as possible and with careful routing. The random mismatch can only be reduced by making a larger unit capacitance.

2.6.5 Gain Error

Gain errors in a SAR ADC causes saturation of the output decimal signal and leads to reduction of ENOB. Gain errors are caused by increased parasitic capacitance to ground at the CDAC top plate that accumulates extra charge during sampling. This extra capacitance leads slope change in the analog to digital transfer function of the ADC. Gain errors are easily alleviated, since the input signal to the ADC can have its amplitude lowered to avoid saturation, without loss of ENOB.

2.7 Digital Buffers

When driving large capacitive loads with inverters and when switching speed is important, it's not true that a single inverter with high driver strength will minimize the switching speed. The switching time can be minimized by a chain of N inverters and where each inverter is scaled progressively by α. Such a chain of inverters, or a buffer, is seen in Figure 2.12.

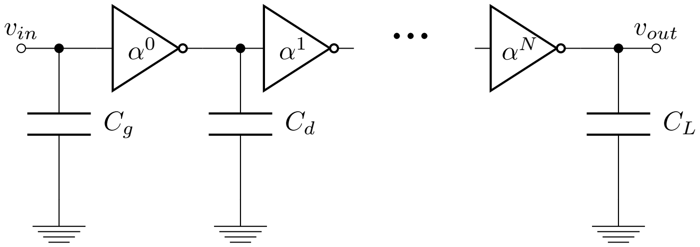


Figure 2.12: Chain of inverters to drive a large capacitive load.

If the first inverter has a input capacitance of C_g and an output capacitance of C_d, then the optimal scaling factor α can be shown to follow [13]

$$\alpha(\ln \alpha - 1) = \frac{C_d}{C_g} \tag{2.20}$$

Eq. (2.20) has to be solved numerically for α. If the inverter chain is terminated in a large load capacitance C_L, then the optimal number of stages N can be calculated as

$$N = \ln\left(\frac{C_L}{C_g}\right) / \ln \alpha - 1 \tag{2.21}$$

These formulas have been derived by minimizing the propagation delay through the chain of inverters.

Chapter 3

High Level Design

This chapter will present some high level design choices for the SAR ADC. The error budget for the SAR ADC will be presented and the devices used in this thesis will be justified from simulations results. Lastly, the switching scheme used in this thesis will be presented.

3.1 Error Budget

An error budget was drafted at the start of this thesis to distribute the error over the different subcircuits, but also to obtain some specifications for each block. It is assumed that all the error sources are uncorrelated so that the sum of errors squared adds up to the total error squared. When dealing with uncorrelated errors like this, it is best to distribute the error as much as possible, since error sources that are large compared to other will be dominating and the total error will still be high even if the other error terms are small.

Since the budget will deal with some assumptions that can not be justified all that well, the budget will be overdesigned by a bit. For example, it is difficult to predict the systematic error caused by the CDAC and it is better to do conservative design. This might seem like a bad decision, but one still has the freedom of adjusting the supply voltage, switching algorithm and bulk biasing after the initial design is done to get to the wanted target ENOB.

In this thesis, the target ENOB is 10 bits and the ADC will therefore be designed to give out 11 bits. An ideal 11 bit ADC will give an output SINAD of 67.98 dB, as given by Eq. (2.5). In this thesis, the required ENOB is at least 10 bits, which corresponds to a SINAD > 61.96 dB. It was assumed initially that the supply voltage was set to 750 mV and the common-mode input voltage was set to half of this. An input sinusoid using the full dynamic range will then have a squared RMS amplitude value of 0.274 V^2, or 0.53 V. With these assumptions and by using Eq. (2.6), one can find the required squared RMS error voltage to be 0.174 μV^2, or 417 μV for 10 bits ENOB. This sets the upper bound

Table 3.1: Quantization parameters needed for error budgeting.

Quantization Parameters	
Number of bits	11 bits
Ideal SINAD	67.98 dB
Target SINAD	61.98 dB
Input Amplitude	750 mV
Reference Voltage	750 mV
V_{LSB}	366 μV
Input RMS amplitude	0.53 V
Maximal RMS Error	417 μV

for the total error in the system. These values are summarized in Table 3.1 for convenience.

The error budget was drafted during initial circuit design of the comparator and design of the sampling switch. The initial plan was to design the comparator so that the input referred RMS noise would be close to $V_{LSB}/2$. Not only will the sampling switch distort the input signal, but some noise will couple to the input signal as well. This means that the sampling switch needs two error source contributions in the budget. The switch topology was also chosen early so that it would fit well in the wanted specifications and the initial goal was to try to keep the sum of squared error of the switch comparable to that of the comparator.

To make the error budget more or less complete, it was assumed that the unit capacitor C_{unit} of the CDAC had a value of 300 aF and that the systematic non-linearities in the CDAC gave a reduction of 1 dB SINAD. The systematic errors are difficult to predict for the CDAC and 1 dB has been chosen mainly because it is an easy number to work with and because it seems reasonable for an ADC that is thermally limited. The unit capacitance of the CDAC was chosen so that it corresponds reasonably well with state-of-the-art CDAC designs [14]. The reasoning for specifying the unit capacitance so early in the design is that allows one to calculate the kT/C noise and therefore complete the budget. The resulting error budget can be seen in Table 3.2. It is assumed that the temperature is 27°.

Table 3.2: Initial error budget for the ADC.

Error Source	Magnitude [μV^2]	Magnitude [μV]	Relative Error [%]
Comparator Noise	0.045	212	36
CDAC distortion	0.025	158	20
Switch Distortion	0.025	158	20
Switch Noise	0.018	134	14.4
kT/C	0.012	110	9.6
Sum	0.125	-	100
$\sqrt{\text{Sum}}$	-	354	-

The sum of errors squared in the budget equals $0.125\ \mu\mathrm{V}^2$ and taking the square root of this result yields $354\ \mu$V, which is less than the upper bound of $417\ \mu$V. The error budget presented should give a theoretical SINAD of 63.33 dB. This corresponds to an ENOB of 10.23 bits.

3.2 Device Choice

The initial plan for this thesis was to design a compiled SAR ADC using ciccreator [15] developed by Carsten Wulff. Ciccreator compiles the layout of a Simulation Program for Integrated Circuits Emphasis (SPICE) netlist once a technology file[1] and a routing file has specified for the compiler. For a compiled design, it is a lot easier to work with standard transistor cells (unit transistors), than having devices with various $\frac{W}{L}$ as the compiled layout needs some regularity to work well. Due to time constraints, the layout of the ADC was done manually, but unit transistors have still been utilized throughout the design.

In this thesis, an analog unit transistor and a digital unit transistor have been defined. The use of unit transistors might seems like a disadvantage when doing analog layout, as there is less freedom to dimensions transistors. This might be true in certain cases, but parallel and series connections can still be utilized for more flexibility.

Another advantage of using unit transistors is that it ensures more regularity when doing layout. For 22 nm FDSOI, the Design Rule Check (DRC) is very strict when it comes to polysilicon rules, especially for minimum gate length. The DRC needs to have 3 dummy polysilicon fingers on both sides of the gate finger for minimum gate length. However, if transistors are stacked, then 3 dummy polysilicon fingers only have to be put at the end of the transistor stack and each transistor only require 1 dummy polysilicon finger on each side of the gate. The 3 dummy polysilicon fingers are referred to as polysilicon termination and the DRC also requires that all polysilicon within a termination are of equal dimensions. This is only possible if all the transistors are identical within a termination. It is clear that the use of unit transistors allows for a huge reduction in dummy polysilicon, which results in reduced overall area.

It was theorized early in the design stage that low threshold devices would give the best Figure of Merit (FoM) due to the high speed requirement. This kit provides various low threshold devices, but only two low threshold devices have been tested for this thesis. These devices will in the following be referred to as Low Treshold Voltage 1 (LVT1) and Low Treshold Voltage 2 (LVT2), where the threshold voltage of LVT2 devices are lower than the threshold voltage of the LVT1 devices. These names are pseudonyms as to not reveal the process house. The following will present some simulation results of LVT1 and LVT2 devices and which devices that have been used for design. Test bench parameters will be given as V_{DS} and V_{GS} for nMOS devices and given as V_{SD} and V_{SG} for pMOS devices. All the devices in the following will have dimensions $W = 1\ \mu$m and $L = 20$ nm.

---

[1] The technology file very loosely said contains design rules and layer definitions.

3.2.1 Noise

The noise in the devices was investigated by probing the drain current. Afterwards, this drain current was then referred to the gate as a voltage to obtain the input referred noise. All the simulations were done in a test bench with $V_{DS} = V_{SD} = 750$ mV and $V_{GS} = V_{SG} = 325$ mV. This is not the ideal setup, since the noise will depend on the biasing condition. This will make the test biased, since the devices have different threshold voltages and the overdrive for the devices will vary. However, the chosen values are early estimations of the final supply voltage and therefore common-mode voltage of the input signal. With this in mind, the results should give reasonable results so that a unit transistor can be picked. To make the results as easy as possible to visualize, only the flicker noise and the thermal noise have been simulated at the frequencies 1 MHz and 10 GHz and the power spectrum density magnitude has been extracted at these frequencies. The results from the noise simulations can be seen in Figure 3.1.

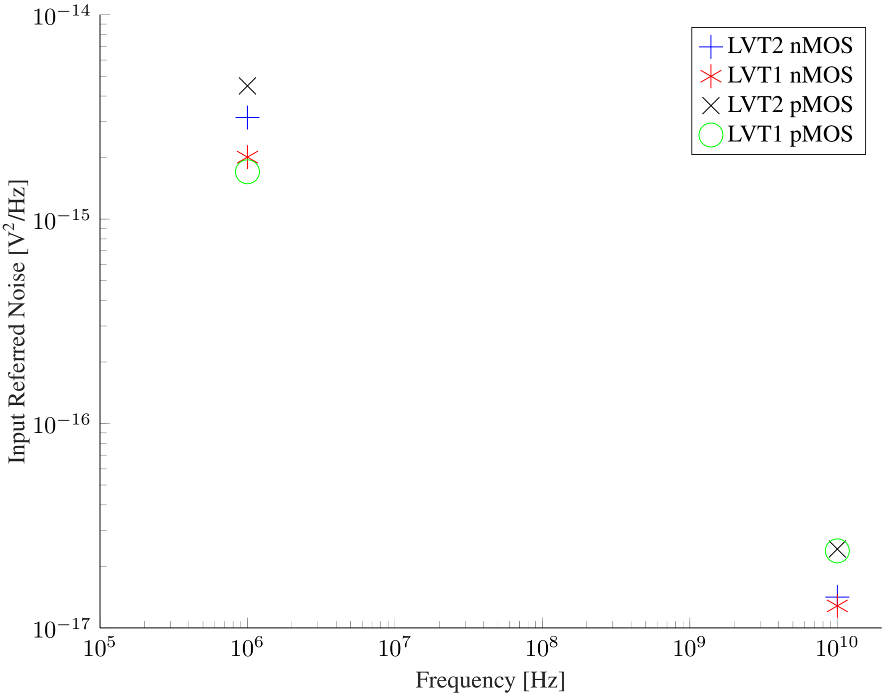


Figure 3.1: Noise performance of various low threshold voltage devices. The spectral density magnitude is extracted for 1 MHz and 10 GHz to study flicker noise and thermal noise separately.

The simulation results shows that the flicker noise for the LVT2 devices are bad compared to the LVT1 devices. This is most likely due to the doped channels of the LVT2 devices, while the LVT1 devices have undoped channels. Doping introduces impurities in the transistor channel and the increase in flicker noise is expected. It's also seen that the LVT1 nMOS devices have slightly worse flicker noise performance than LVT1 pMOS devices.

The LVT1 nMOS devices have about 15% percent higher flicker noise compared to LVT1 pMOS devices, so the difference is modest.

The simulations results also indicate that the nMOS devices have superior thermal noise performance compared to the pMOS devices. The pMOS devices have around 70% higher thermal noise compared to the nMOS devices, which is significant. The difference in thermal noise between the nMOS devices is also seen to be very small.

3.2.2 Transconductance

The transconductance g_m for the simulated devices was obtained by using the definition $g_m = \frac{\partial I_D}{\partial V_{GS}}$. The simulations were performed with constant $V_{DS} = V_{SD} = 750$ mV, while V_{SG} and V_{SG} were swept from 0V to $V_{DD} = 750$ mV. The simulated results for g_m can be seen in Figure 3.2.

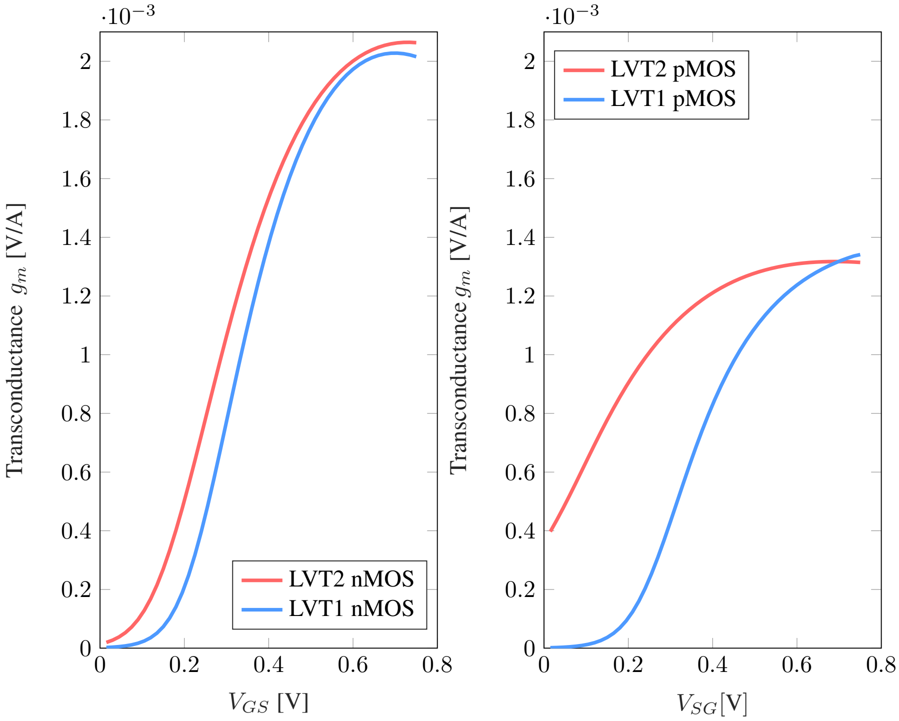


Figure 3.2: Transconductance g_m of the low threshold devices simulated.

It is seen that the nMOS transistors are "stronger" than the pMOS transistors due to the higher g_m, which is normal for MOSFET transistors. The higher g_m of the nMOS devices is beneficial, as the noisy drain current is moved to the gate as a voltage source by dividing by g_m^2. This is especially important when considering other noise sources in a circuit. Another interesting aspect is that LVT2 pMOS devices have high g_m for $V_{SG} = 0$ V. This might suggest that the leakage current for LVT2 pMOS devices is abnormally high.

3.2.3 Transistor Speed and Efficiency

The transistor efficiencies g_m/I_D for the simulated devices can be seen in Figure 3.3. The simulations were performed in parallel with the transconductance simulations, so the test benches are identical. Figure 3.3 reveals that the $|g_m/I_D|$ for the LVT2 devices is smaller than the $|g_m/I_D|$ of the LVT1 devices. This is to be expected, since the lower threshold voltage of LVT2 devices makes these devices faster and therefore more inefficient. The difference in $|g_m/I_D|$ between the nMOS devices is seen to be very modest. An irregularity is seen for the LVT2 pMOS devices, where the $|g_m/I_D|$ is relatively small even for small values of V_{SG}. The difference in $|g_m/I_D|$ between the pMOS devices is also very large.

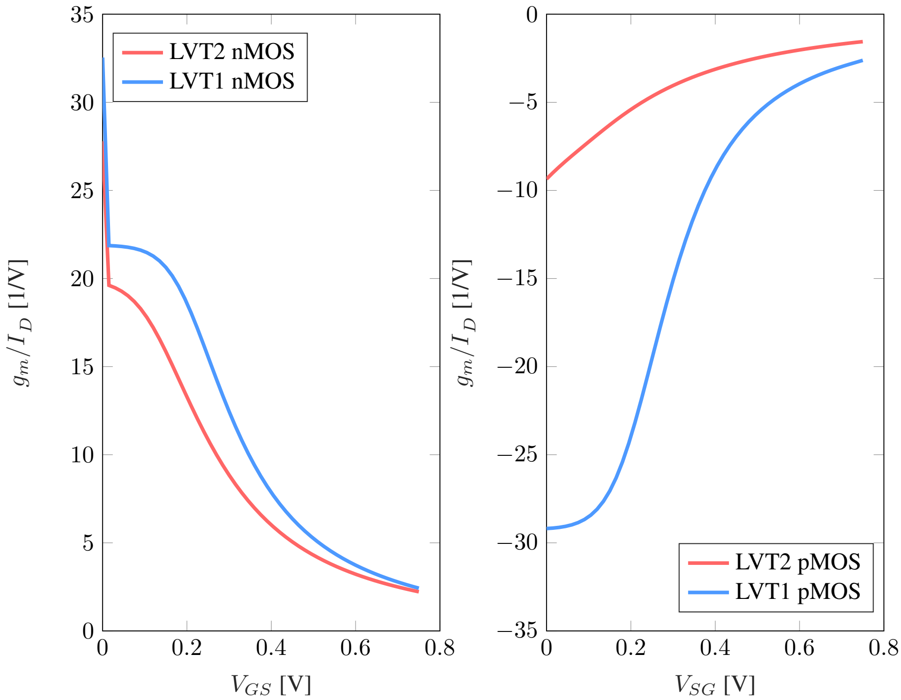


Figure 3.3: Transistor efficiency g_m/I_D of the low threshold devices simulated.

3.2.4 Analog Unit Transistor

Due to the accuracy requirement of ENOB larger than 10 bits and the speed requirement of 100 MS/s, it is probably wise to pick an analog unit transistor that has good noise performance to achieve the target ENOB, but it is also important to consider the $|g_m/I_D|$ due to the speed requirement. It is also probably a good choice to pick a transistor with good thermal noise properties, as flicker noise can be reduced by using a dynamic comparator. This is because a dynamic comparator has a reset phase and a comparison phase. The comparator will act like a highpass-filter[2] due to the reset phase and the effect of low frequency flicker noise will be reduced.

The thermal noise properties of LVT1 nMOS and LVT2 nMOS both stands out when compared to the pMOS transistors, but the LVT1 nMOS has much better flicker noise properties than the LVT2 counterpart. The LVT2 pMOS stands out as the worst noise performer and this transistor will not be used due to this. Comparing the transconductance g_m and transistor efficiency g_m/I_D between the nMOS transistors, it is seen that the difference is modest, so the LVT1 nMOS will be used as the n-channel device due to the superior flicker noise performance. Since the LVT2 pMOS transistor already has been excluded, the choice for p-channel device is the LVT1 pMOS. Another good reason to use the LVT1 devices is the undoped channel. Since the channel is undoped, one should expect a decrease in mismatch because the doping variability is removed.

The dimensions for the analog unit transistor were determined by using an ideal behaviour model of the ADC and a comparator transistor circuit. The dimensions of the input pair of the comparator were increased until a reasonable noise performance was achieved (the value in the budget). The input pair was simulated with a multiplier larger than unity due to matching considerations. The preliminary simulations showed that $W = 1$ μm and $L = 20$ nm would be fitting as an analog unit transistor. The nMOS and pMOS were dimensioned identically and a single finger device was used. The choice of these dimensions is also motivated by layout considerations to avoid abnormally large multipliers that makes layout work tedious.

3.2.5 Digital Unit Transistor

When defining a digital unit transistor there are several aspects that should be considered. Speed is of course important, since the specification of 100 MS/s is so high. Leakage is also important, but speed and leakage tends to be correlated, so a compromise needs to be made. One should also make an effort to balance nMOS and pMOS as much as possible to avoid skewing. It is probably beneficial to either use LVT2 devices or LVT1 devices, i.e, do not mix devices. The LVT2 devices have lower g_m/I_D and the speed is therefore faster. However, the abnormally large leakage current of LVT2 pMOS makes using the LVT2 device little attractive. It is for these reasons that the LVT1 devices will be used in the digital circuitry.

The digital unit transistor has dimensions $W = 350$ nm and $L = 20$ nm. This applies for the both the nMOS and the pMOS transistor. The sizing was determined by post-layout simulations on the entire ADC where the netlist was edited until a reasonable performance was achieved.

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[2] The overall response will be bandpass since the comparator has poles at high frequencies that will limit the bandwidth.

3.3 CDAC Switching

The decision of the switching scheme of the CDAC was based on simulations with a comparator and the sampling switch as a transistor circuits, while the remaining blocks were ideal. This ideal SAR ADC model was composed of ideal components and VerilogA code. This thesis will only model split-monotonic switching and monotonic switching due the simplicity and the good energy efficiency of these algorithms.

A pure monotonic switching scheme where the common-mode voltage was switched up and down was tested, as well as a combination of split-monotonic and monotonic switching was tested. The latter simulations was with 3, 4 and 6 MSBs switched with split-monotonic switching and monotonic switching was performed for the remaining LSBs. The monotonic switching was performed by changing common-mode voltage up and down in this case as well.

Initially, it was found from simulations that 3 MSBs switched as split-monotonic and the remaining LSBs switched as monotonic switching with an increase in common-mode voltage gave the best FoM. However, final simulations with the entire ADC on layout showed that a decrease in common-mode voltage gave the best FoM. This was mainly due to speed limitations in the digital circuitry on layout that resulted in an increase in V_{DD}. With higher supply voltage, the comparator input referred noise increased too much and the extra speed for the comparator was not worth it, so it was decided to switch the common-mode voltage down after all. This means that if the initial common-mode voltage is v_{cm}, then the common-mode voltage v'_{cm} at the end of conversion will be

$$v'_{cm} = v_{cm} \left(1 - \sum_{i=4}^{11} \frac{1}{2^i} \right) \tag{3.1}$$

For a typical supply voltage $V_{DD} = 750$ mV and with initial common-mode voltage of $v_{cm} = V_{DD}/2 = 375$ mV, the final common-mode voltage v'_{cm} is from Eq. (3.1) $v'_{cm} = 328.3$ mV and corresponds to a common-mode voltage decrease of 46.7 mV.

Chapter 4

Implementation

This chapter will present the design solutions chosen for the SAR ADC. The comparator's schematic and design procedure will be explained. Afterwards, the sampling switch topology will be shown. The principle of operation will be described and the transistor circuit will be shown. Thereafter, the digital circuitry involved in the SAR ADC will be presented. The internal architecture of the bit slice designed will be shown, along with needed signal interface and clock generation theory. The different subcircuits of the bit slice will be presented and explained in detail. Subsequently, the CDAC used in this thesis will be shown. The entire metal stack of the CDAC and the purpose of each metal layer will be displayed. In the end, layout for the entire SAR ADC will be shown. This chapter will shown the main schematics of the ADC, but selected additional schematics can also be found in Appendix A as they appear in Cadence Virtuoso.

In the following, it will be assumed that the analog circuitry uses the analog unit transistor and that digital unit transistors are used in the digital circuits. Digital ports present in analog circuits will use the analog unit transistor due to regularity and driving strength considerations. If no multiplier is present on the schematic, it is assumed that a unity multiplier is used. All bulk connections will be to ground (for pMOS and nMOS), unless explicitly stated otherwise[1].

4.1 Comparator

The comparator topology chosen for this thesis is the StrongARM latch [16] and the transistor circuit can be seen in Figure 4.1. This comparator topology has been chosen mainly due to the simple design and also because it is a dynamic comparator, meaning that the comparator only uses current when active. The comparator uses a nMOS input pair due to the superior thermal noise properties of the nMOS devices. The pMOS devices have better flicker noise properties compared to the nMOS devices, but only marginally.

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[1] Normal nMOS and pMOS bulk connection to ground and V_{DD} is not possible due to the parasitic PN junction between the wells. This is due to the flip-well configuration.

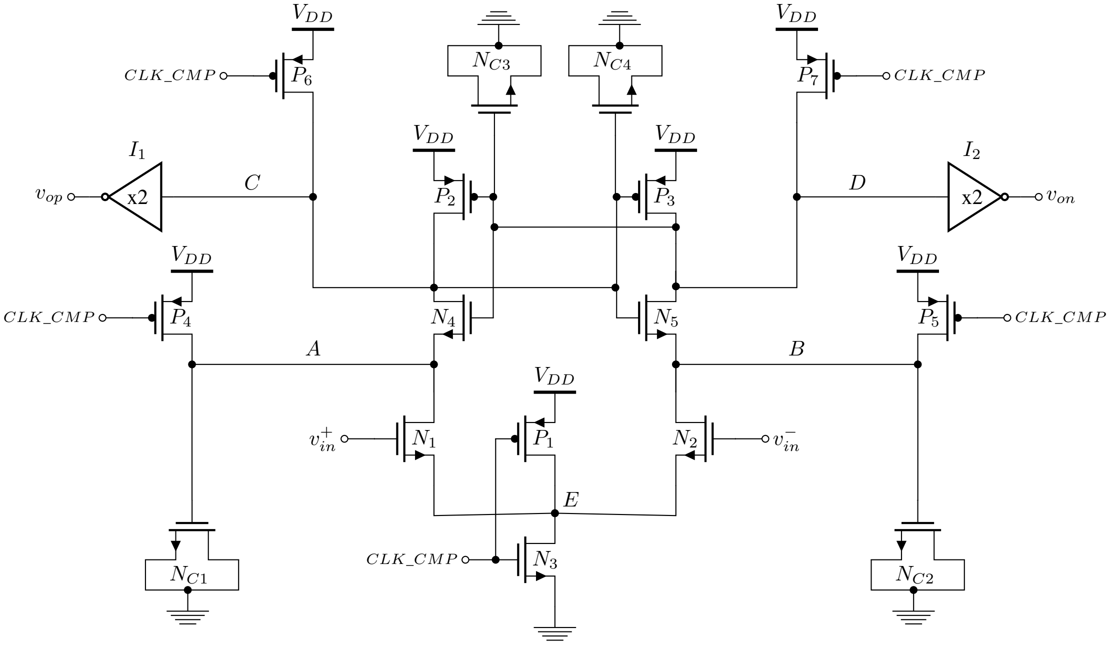


Figure 4.1: StrongARM latch comparator.

The comparator consists of a differential input nMOS transistor pair $N_1 - N_2$, a cross-coupled inverter formed by transistors $N_4 - N_5$ and $P_2 - P_3$, a triode operating transistor N_3 and reset transistors $P_1 - P_7$. Additional capacitance $N_{C1} - N_{C4}$ have been added to the original circuit for better noise performance. The outputs of the strongARM latch at nodes C and D are passed through the inverters $I_1 - I_2$ to generate the signals v_{op} and v_{on}. These inverters are mainly added to generate the wanted signal interface and to satisfy driving strength requirements. The relation between the input differential voltage and the outputs of the comparator are summarized in Table 4.1.

Table 4.1: Relations between input and output during comparison phase of the comparator.

Input Differential	v_{op}	v_{on}
$v_{in}^{+} - v_{in}^{-} > 0$	High	Low
$v_{in}^{+} - v_{in}^{-} < 0$	Low	High

The StrongARM latch is a dynamic comparator and the operation of this circuit is best described by the different phases of the circuit. These phases will be described step-by-step below. In the following, it should be noted that V_{tn} is the threshold voltage of a nMOS transistor used and V_{tp} is the threshold voltage of a pMOS transistor used.

1. The comparator clock CLK_CMP is initially low and the comparator is in reset mode. Reset is handled by the pMOS transistors $P_1 - P_7$ that charges the nodes A, B, C, D and E to V_{DD}. In reset mode, the nMOS transistor N_3 is turned off to prevent the differential input pair $N_1 - N_2$ from discharging the nodes A and B.
2. The comparator clock CLK_CMP goes high and the reset transistors turn off. The nMOS transistor N_3 now turns on and is in triode region. This allows the input differential pair $N_1 - N_2$ to draw a differential current from nodes A and B that is proportional to $v_{in}^{+} - v_{in}^{-}$. This current also discharges the nodes A and B. The discharge rate is determined by the input differential, the capacitance on the nodes A and B as well as the dimensions of nMOS transistor N_3.
3. As the voltage on the node A or B drops below $V_{DD} - V_{tn}$, the nMOS transistor N_4 or N_5 in the cross-coupled pair will eventually turn on, since the source voltage is dropping. When N_4 or N_5 on either sides start to conduct current, the voltage on node C or D will also start to drop.
4. When the voltage on either node C or D goes below $V_{DD} - V_{tp}$, the pMOS transistor P_2 or P_3 turns on and the cross-coupled pair goes into a positive feedback that will put either C or D high, while the other node will be pulled to ground.

The dynamic operation of the StrongARM latch makes it difficult to analyze and therefore dimension the transistors properly. The paper [17] present a noise analysis of the StrongARM latch based on small signal analysis for each phase and by using the noise model presented in the theory part of this thesis. The end result is an analytically formula that gives the input referred noise. This expression has not been used in this thesis for calculation of transistor geometry, due to the complexity of the formula. This is mainly because the derived expression contains several time changing currents, small signal parameters and node capacitances that needs to be found. Even if an approximate effective small signal parameter could be found, it does not guarantee that the circuit is fast enough, which is crucial for high speed operation needed in this thesis. Instead, the guidelines presented for low noise design in the same paper has been used:

- Increase input transistors' W/L
- Make transistor N_3 small
- Decrease the common-mode voltage of the input transistors
- Making N_4 and N_5 bigger than N_3

For initial design, all the pMOS transistors had a multiplier of 1 and the multiplier of N_2 was also set to 1 in accordance to the guidelines above. The dimensioning started by first estimating the comparator clock frequency f_{CMP}. If the sampling clock frequency f_{CLK} has a duty cycle of $D = 25\% = 0.25$, then the comparator clock frequency can be estimated as

$$f_{\text{CMP}} = \frac{N f_{\text{CLK}}}{1 - D} \tag{4.1}$$

Where N is the number of bits of the converter. For $N = 11$ bits, $D = 0.25$ and $f_{\text{CLK}} = 100$ MHz, the comparator clock frequency can be calculated as $f_{\text{CMP}} \approx 1.5$ GHz. The typical design procedure has been to clock the comparator with a frequency of f_{CMP} and then dimension $N_1 - N_2$ and $N_{C1} - N_{C4}$ so that the comparator can make a decision with a small differential input of V_{LSB} within the available time frame. Afterwards, a noise transient simulation was performed. The input referred noise was then estimated by sweeping a small differential input around the threshold of the comparator. For each point in the sweep, the probability of wrong decision was estimated from many comparisons. The final distribution obtained from all the points in the sweep can then be mapped to a Gaussian distribution and the mean and variance can be found. The variance in this case is the input referred noise power and the mean is the mean value of the noise. This procedure is explained more in detail in [18]. This was an iterative procedure and the main goal was to make the comparator fast enough and to make the input referred noise equal to around $V_{LSB}/2$. For every iteration, W/L of the input transistors would be increased along with W/L of transistors $N_{C1} - N_{C4}$. Since the noise sources in the circuit are assumed to be uncorrelated, an effort has been done to scale the input and the capacitors so that the root of sum of squares is kept low. This also avoids very large W/L for the input pair, which is beneficial to avoid too large non-linear capacitance at the input of the comparator. The reset transistors $P_6 - P_7$ have been scaled up from post-layout simulations to avoid hysteresis due to heavy capacitive loading. The final dimensions of the transistors can be found in Table 4.2.

Table 4.2: Transistor multipliers for the strongARM latch. All transistors are unit analog transistors unless specified otherwise.

Transistor Dimensions	
Device(s)	Multiplier
$N_1 - N_2$	6
N_3	1
$N_4 - N_5$	3
P_1	1
$P_2 - P_3$	3
$P_4 - P_5$	1
$P_6 - P_7$	2
$N_{C1} - N_{C2}$[1]	5
$N_{C3} - N_{C4}$[1]	2

[1] Device with $W = 500$ nm and $L = 500$ nm for better area utilization.

These values yielded an input referred RMS noise of around 204 μV with $V_{DD} = 750$ mV and with the common-mode voltage $v_{cm} = V_{DD}/2 = 375$ mV. The noise transient had flicker noise and thermal noise enabled, where the maximal bandwidth of thermal noise was set to 15 GHz. The probability of error for each point in the sweep was estimated by performing 1000 comparisons. A custom-made VerilogA module was written to calculate the probability of wrong decision and the statistical analysis was done in MATLAB.

The choice was made to use LVT1 nMOS transistors to get the right capacitance at nodes A, B, C and D as these devices are thin-oxide devices and therefore provide high capacitance per area. These devices do not use the analog unit transistor, but they are devices with $W = 500$ nm and $L = 500$ nm to avoid very large multipliers and for better use of area. This transistor capacitance is not linear and will be highest when the device is in the strong inversion. The circuit does not need linear capacitance at these nodes, so the non-linearity was not a problem. The choice was made to use nMOS devices rather than pMOS devices, since the nodes A, B, C and D all are high after reset. This ensures that the capacitance at these nodes are at a maximum during comparison. Large gate area of thin-oxide devices can in some cases be significant and has to be checked. In this case, the gate leakage was simulated to be insignificant.

4.2 Sampling Switch

The sampling switch in this thesis will be a MOSFET switch and the theory part of this thesis showed that the on-resistance R_{on} of such a switch has a signal dependent on-resistance. This non-constant resistance is a significant source of distortion due to the signal dependent attenuation and phase shift through the switch. One way to increase the linearity of the switch is by keeping V_{GS} constant, independent on the input signal v_{in}. Keeping the gate-source voltage can be done by bootstrapping the sampling switch. A conceptual figure of this technique is showed in Figure 4.2.

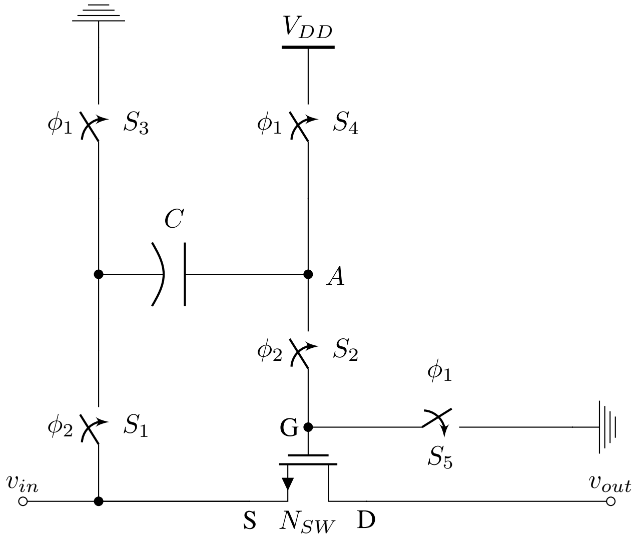
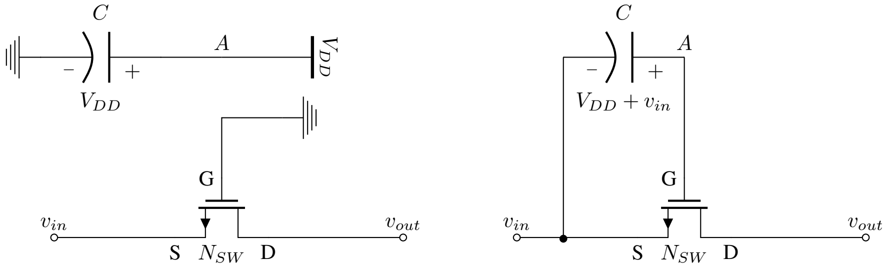


Figure 4.2: Bootstrapped switch conceptual figure.

The bootstrapping in Figure 4.2 consists of a sampling switch N_{SW} and switches $S_1 - S_5$



(a) Bootstrapped switch in phase ϕ_1.

(b) Bootstrapped switch in phase ϕ_2.

Figure 4.3: Phases of a bootstrapped switch.

which are controlled by the signals ϕ_1 and ϕ_2. How the circuit looks in phase ϕ_1 and phase ϕ_2 is shown in Figure 4.3.

During phase ϕ_1, switches $S_3 - S_5$ are closed and switches $S_1 - S_2$ are open. The bottom plate of C is now connected to ground while the top plate of C is connected to V_{DD} as shown in Figure 4.3a. The voltage at node A is therefore V_{DD} and is being stored at the capacitor C for later use during ϕ_2. The gate voltage of the switching transistor N_{SW} is kept at ground potential, so the the switch is not conducting.

Afterwards during ϕ_1, switches $S_1 - S_2$ are opened and switches $S_3 - S_5$ are closed. The bottom plate of C is now connected to v_{in}, while the top plate is connected directly to the gate of N_{SW} as shown in Figure 4.3b. Since no charge has been moved from the top plate, the node A has increased it's potential by v_{in}, so the total voltage at node A is now $V_{DD} + v_{in}$. It is clear now that the bootstrapping will make the gate voltage V_G of N_{SW} in phase ϕ_2 equal to

$$V_G = V_{DD} + v_{in} \tag{4.2}$$

The source-gate voltage V_{GS} of N_{SW} is thus

$$V_{GS} = V_{DD} + v_{in} - v_{in} = V_{DD} \tag{4.3}$$

Eq. (4.3) shows that V_{GS} stays constant regardless of v_{in} and this greatly increases the linearity of the switch. One transistor implementation of such a switch is presented in [19] and the circuit with some minor changes is shown in Figure 4.4. In Figure 4.4, the switches $S_1 - S_5$ are now represented by the transistors N_1, P_3, N_2, P_2 and N_5, respectively. The signal $\textsc{clk}$ is the sampling clock of the system and transistors P_1 and N_3 are controlled by $\textsc{clk}$ directly to generate auxiliary signals to the circuit. During sampling, the maximal voltage at node A can go upwards of $2V_{DD}$ if the entire dynamic range is used for the input signal. This is problematic with these devices, as the maximal overdrive can not exceed 0.9 V[2]. To solve this problem, an additional transistor N_4 is added. The inclusion of this transistor reduces the maximal overdrive in the circuit to $V_{DD} - v_{tn}$ only,

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[2] In this case, the term overdrive is used to describe $|V_{GS}| - V_t$.

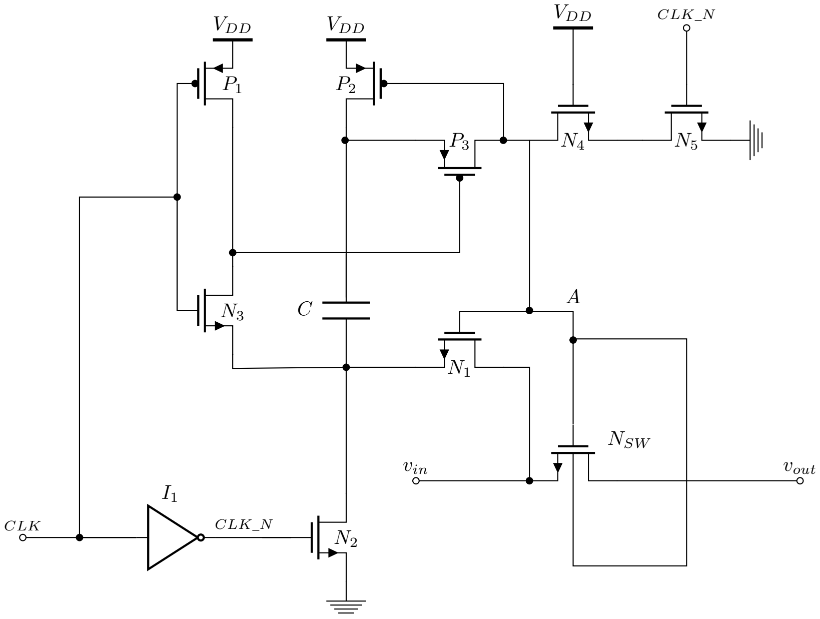

Figure 4.4: Bootstrapped switch transistor circuit.

since N_4 has its gate tied to V_{DD}. During sampling, transistor N_4 will turn off due to the high source voltage and transistor N_5 thus stay isolated from the high voltage at node A. Without transistor N_4, the overdrive of transistor N_5 could reach $2V_{DD} - v_{tn}$ during sampling, which in most cases would violate the maximal overdrive constraint.

While the bootstrapping increases the linearity greatly, it is was simulated to be only sufficient for 8-9 bits linearity. The switch now is mainly limited by the signal dependent body-effect. The body-effect is due to the non-zero source-bulk voltage V_{SB} which causes shift in the threshold voltage V_t of the switching transistor N_{SW}. A constant shift in V_t would be permitted, but this shift can not be signal dependent as this would make R_{on} signal dependent. The body-effect can be cancelled by several connections in Figure 4.4, but this thesis will tie the bulk of N_{SW} to the gate of the same transistor. This will cancel the body-effect, since the potential at node A during sampling is $V_{DD} + v_{in}$. This reduces distortion because v_{in} is found on the gate and the body-effect is thus cancelled, but the extra constant V_{DD} will also lower the threshold voltage V_t of the switching transistor N_{SW}. This reduction in V_t will cause a lower R_{on} and the cutoff-frequency for the switch also increases. This will lead to a lower distortion of the output signal for a given frequency. In a conventional bulk process, this connection of the bulk would be troublesome, due to the parasitic PN junction between the bulk and the source/drain terminals. In that case, one would have to resort to bulk switching as done in [19] to avoid forward bias of this junction diode. However, in an FDSOI process, this action is permitted, because these diodes does not exist. This allows for reduction in number of transistors and better performance compared to the switch in [19].

All the transistors in Figure 4.4 have a multiplier of unity, as this gave a good compromise between leakage of the boosted voltage on node A, speed and noise. While the switching transistor N_{SW} probably could be larger to reduce the on-resistance, it was found that increasing the multiplier of this transistor would decrease ENOB. This might might be caused by coupling of the input to the output of the switch through C_{DS}, due to leakage of the transistor or both. The capacitor is a alternating-polarity Metal-Oxide-Metal (MOM) capacitor included in the PDK with capacitance $C = 132$ fF. A MOM capacitor has been used due to the good linearity. The metal layers used for this MOM capacitor is from Metal 1 (M1) to Metal 5 (M5). Higher metal layers could be used, but the overall area of the switch is so small compared to other blocks, so there is no benefit in using higher metal layers.

4.3 SAR Control Logic

This section of the thesis will deal with the digital circuitry involved in the designed SAR ADC. In this thesis, 11 identical bit slices have been cascaded and constitute the entire digital circuitry. An overview of the bit slice designed will be presented, as well as the entire overview of all 11 bit slices connected together. Each building block in the bit slice will be shown and explained through text and figures.

4.3.1 Overview

The purpose of this subsection is to give an overview of the bit slice signal interface, presentation of a single bit slice's internal architecture and how the bit slices interconnect. A bit slice can be divided into CDAC switches, CDAC control logic, clock generation and enable logic as shown in Figure 4.5. In this thesis report, the CDAC switches and CDAC control logic have been merged into a single subcircuit and the clock generation and enable logic also have been merged into a single subcircuit.

The bit slice in this thesis has four output nets CBP, CBN, CAP and CAN that are connections to the bottom plates of the CDAC. Four output nets are required since a split-monotonic scheme is used. The bit slice that uses monotonic switching uses only two of these outputs, even if four outputs nets are present. This does inherently waste some energy and area, but the regularity of using a single bit slice everywhere makes the layout work less. It also should be mentioned that this configuration allows for rapid change to switch between increase or decrease in common-mode voltage during conversion[3].

Four input auxiliary signals are required for a bit slice. The required signals are v_{op}, v_{on}, $\mathit{CLK\_PULSE}$ and $\mathit{CMP\_RDY}$. All of these signals are derived from the comparator's outputs, directly or generated by the use of simple digital logic gates. Each bit slice has an input signal $\mathit{EN\_IN}$ that triggers the bit slice and an output signal $\mathit{EN\_OUT}$ that triggers the next bit slice in a domino fashion. All the bit slices are connected to a common output net CMP_PULSE that is used to distribute the comparator clock as shown in Figure 4.6.

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[3] The only difference between switching common-mode voltage up or down are the initial conditions of the capacitor bottom plate. In a split-monotonic scheme, both initial conditions are used.

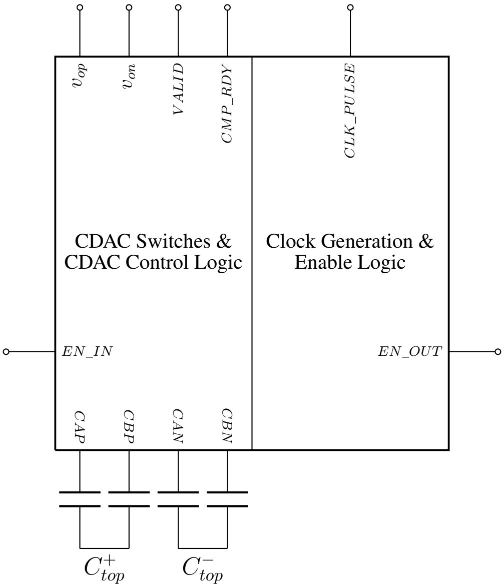
v_{op}
v_{on}
$VALID$
CMP_RDY
CLK_PULSE
CDAC Switches & CDAC Control Logic
Clock Generation & Enable Logic
EN_IN
EN_OUT
CAP
CBP
CAN
CBN
C_{top}^{+}
C_{top}^{-}

Figure 4.5: Single bit slice architecture with input and output signals.

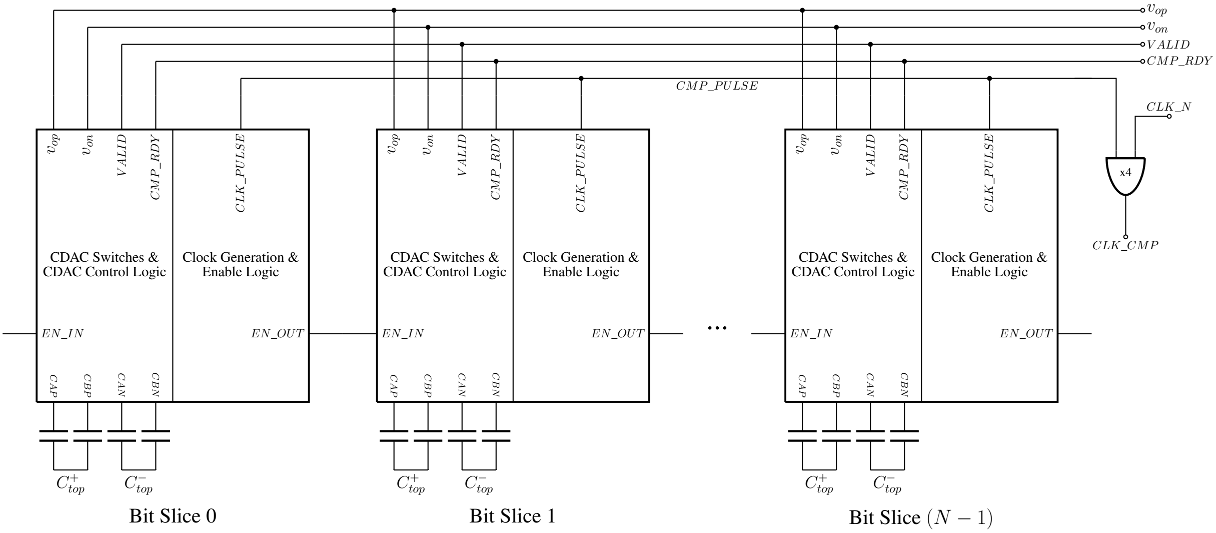
v_{op}
v_{on}
$VALID$
CMP_RDY
CMP_PULSE
CLK_N
x4
CLK_CMP
CLK_PULSE
CDAC Switches & CDAC Control Logic
Clock Generation & Enable Logic
EN_IN
EN_OUT
...
CAP
CBP
CAN
CBN
C_{top}^{+}
C_{top}^{-}
Bit Slice 0
Bit Slice 1
Bit Slice $(N-1)$

Figure 4.6: Total overview of all N bit slices and the signal interface.

Each bit slice when enabled will generate a pulse for the comparator on the net CMP_PULSE. This pulse will force the comparator to make a decision and then pull the comparator back in reset mode once a decision has been made. Each bit slice drives the same common clock net CMP_PULSE and tristate buffers have been used at the output CLK_PULSE for all bit slices to avoid any short circuits. The tristate buffers ensures that each bit slice when not enabled is in a high impedance mode. Different architectures for clock distribution for the comparator have been tested, but most of these solutions suffers from long propagation delay when simulating on layout and is thus not suitable for the high-speed required in this thesis. This tristate buffer solution is superior, since each bit slice now has a direct way to influence the comparator and this greatly decreases the propagation delay.

4.3.2 Comparator Signals

The auxiliary signals v_{op}, v_{on},$VALID$ and CMP_RDY for the bit slices are defined as seen in Figure 4.7. The outputs from the comparator v_{op} and v_{on} are used directly to control the bit slices, but these signals are also passed through the NOR gate I_1 to produce CMP_RDY. CMP_RDY will only be logical high if both of the comparator outputs are low, and logical zero otherwise. This is to ensure enough time for the comparator to settle so that hysteresis is avoided, but it also gives some time extra time for the CDAC to settle. This signal is a delay signal that each bit slice has to wait for before enabling the next bit slice. The signal $VALID$ is derived directly by just inverting CMP_RDY. This signal is important for reduction of metastability at the comparator's outputs, but this signal is mainly needed to keep precharged nodes at the right potential in the CDAC control and CDAC switching circuit as will be explained later.

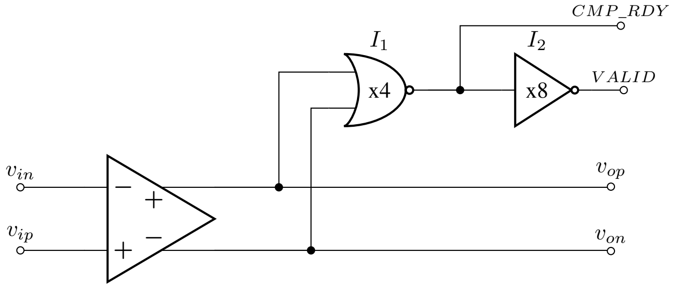

Figure 4.7: Auxiliary signals for the digital circuitry generated directly from the comparator's outputs and by the use of logic gates.

4.3.3 Clock Generation Based on CDAC Bottom Plate

One of the main challenges for high speed, high accuracy SAR ADCs is the clock generation of the comparator clock. It was showed earlier in this thesis that the comparator had to be clocked at 1.5 GHz under the conditions presented. This high frequency imposes major challenges when it comes to settling time of the CDAC, as the settling time needed is more than 7.62 time constants and the challenge is to simulate this needed settling time to avoid distortion. In other SAR ADC designs, this delay is typically generated by making a delay cell. While this work, it is very difficult to replicate the settling time needed for the CDAC over Process-Voltage-Temperature (PVT) variations. In addition, generating delay typically requires use of energy. Such an approach would also probably be troublesome for very high speeds with many bits, where the time-frames for each bit conversion is in the order of tens of picoseconds as in this thesis.

Recently, a new technique for the comparator clock generation has been utilized in [20]. This new technique is based on using the CDAC bottom plate directly for clock generation. The CDAC bottom plate is always switched between ground and v_{ref} and it is thus possible to use the step-response of the CDAC bottom plate directly for clock generation. This works since the voltage levels at the CDAC bottom plate are digital logic levels and simple circuits can be designed to check whether the bottom plate has been switched or not. This technique is very energy efficient, since no delay has to be replicated. Not only that, but this technique is also very robust, since the clock generation is now based on the bottom plate of the CDAC directly and this will make the comparator clock less vulnerable to PVT variations. In this thesis, the same technique will be used for clock generation of the comparator clock.

4.3.4 CDAC Control and Switching Circuit

The CDAC control and switching circuit designed in this thesis can be seen in Figure 4.8. The main functionality of this circuit will be explained first. Afterwards, some of the instances will be explained in more detail and some of the less obvious usage of transistors will be clarified. The pMOS transistors $P_1 - P_2$ will during sampling ($\textsc{clk}$ is high) precharge the nodes A and B to V_{DD}. Since nodes A and B are initially high, it means that pMOS transistors $P_3 - P_4$ are turned off. The precharged voltage at nodes A and B are buffered by the digital buffers $I_1 - I_2$ and then passed through the inverters $I_3 - I_6$. This forces the initial conditions of bottom plate nodes $\textsc{can}$ and $\textsc{cap}$ as logical low and bottom plate nodes $\textsc{cbp}$ and $\textsc{cbn}$ as logical high. Since $\textsc{can}$ and $\textsc{cap}$ are high initially, it means that nMOS transistors $N_6 - N_7$ are off. These transistor will be explained in detail later.

Once the sampling phase is over ($\textsc{clk}$ is low), the pMOS transistors $P_1 - P_2$ are turned off and the voltages at node A and B stay at their precharged potential due to the capacitance at these nodes. The next thing that will happen is that $\textsc{clk\_pulse}$ will go from low to high. This action turns nMOS transistor N_3 on and the potential at node E is consequently zero. The signal $\textsc{clk\_pulse}$ is generated in the clock generation logic and will always be pulled high locally in the bit slice if the bit slice is enabled and a comparator decision has not been made yet. When $\textsc{clk\_pulse}$ goes high, it also means that the comparator will make a decision. A decision will always force the signal $\textsc{valid}$ to go high and the nodes A and B will therefore be connected to node C and D because of this, respectively. When $\textsc{valid}$ is high, it should be clear that the comparator has made a decision. A decision means that either v_{op} or v_{on} will go high and this will force nMOS transistor N_2 or N_4 to turn on. As a result, this implies that either A or B gets pulled down to ground.

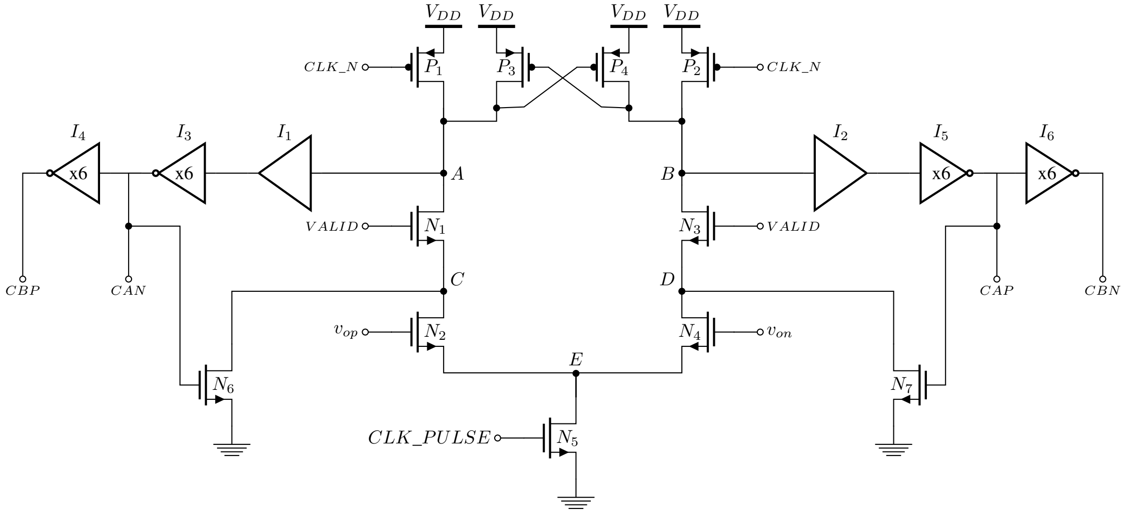
V_{DD}
V_{DD}
V_{DD}
V_{DD}
CLK_N
P_1
P_3
P_4
P_2
CLK_N
I_4
I_3
I_1
I_2
I_5
I_6
x6
x6
x6
x6
A
B
$VALID$
N_1
N_3
$VALID$
C
D
CBP
CAN
CAP
CBN
v_{op}
N_2
N_4
v_{on}
E
N_6
N_7
CLK_PULSE
N_5

Figure 4.8: CDAC Control and CDAC switching circuit.

This action, depending on the comparator's output, will then make the inverters $I_3 - I_4$ or $I_5 - I_6$ switch the CDAC bottom plate and the CDAC top plate voltage will consequently change. The timing diagram of the circuit is shown in Figure 4.9 when the comparator pulls v_{op} high.

The instances $I_1 - I_2$ are a digital buffers and is there to increase the switching speed of the CDAC. These buffers uses only two steps, but the sizing of the steps are close to

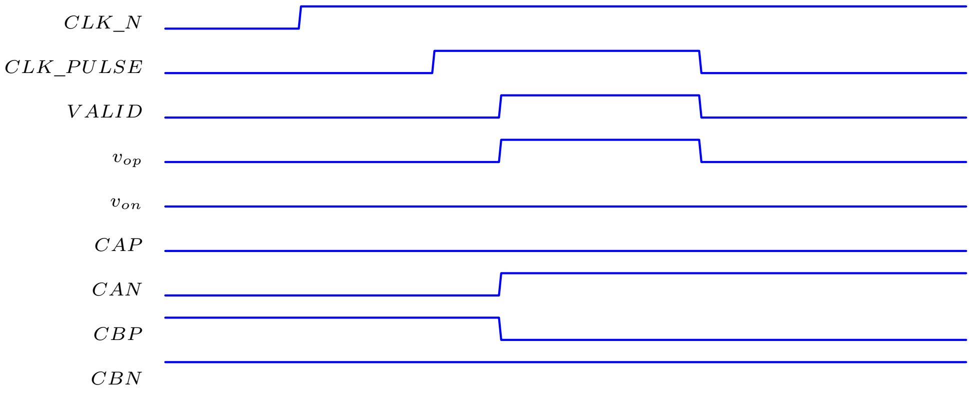

Figure 4.9: Timing diagram for the CDAC control and switching circuit.

optimal by using the scaling factor $\alpha = 3$. None of the buffers uses the optimal number of stages N, mainly since N is dependent on the load capacitance. This means that each bit slice would need a different buffer. Instead, the number of stages for the buffers have been set to 2. This is because two stages was found to be sufficient, but also to save power and area by just using using two stages. The switching inverters should have a multiplier of 9 for the best possible scaling, but this has not been done. Instead, a multiplier of 6 has been used for all the switching inverters. This is again mainly due to geometrical considerations as to not use too much area on top level layout.

It was found during simulations that the precharged nodes A and B would have large voltage transients on them during conversions. Nodes that were supposed to stay at ground level would move up in voltage during conversion and nodes that were supposed to stay high would fall in voltage. In many cases, this would lead to large distortion to the output signal from the ADC, since some capacitors that were already switched would be switched again. Additional transistors $P_3 - P_4$ and $N_6 - N_7$ have been added prevent this from happening. These transistors act on a positive feedback to keep the precharged nodes at their respective levels.

Consider the case where A is pulled down to ground and B stays at V_{DD}. This would mean that P_3 would be turned off and the voltage at node A stays the same. The transistor P_4 would be turned on and this will cause the node B to stay precharged at V_{DD}. Similarly, if A is low, then the node CAN is high and N_6 is turned on. Initially, this might not seem to do anything, since the drain of N_6 is connected to node C. The logical choice seems to connect the drain of N_6 to A, but this would yield a stable state where the node A can not be moved at all, even during sampling. Instead, the drain of N_6 is connected to node C. This connection will enable node A to get pulled downed to ground for every comparison and thus will not have much opportunity to move, since VALID will go high for every comparison, regardless of the comparator's decision.

4.3.5 Enable Logic and Clock Generation

The enable logic and clock generation circuitry designed in this thesis can be seen in Figure 4.10. There are some things worth mentioning before the operation of this circuit is explained. The instance I_2 is a precharged NAND gate and is mainly needed to avoid oscillations at the EN_OUT node. The use of static logic gates would induce oscillations since CMP_RDY will go high and low for each bit during conversion. The use of precharged logic prevents this from happening, because the precharged logic is always charged up to V_{DD} during sampling and then held at that potential until the bit slice needs to trigger the next bit slice. In that case, the precharged logic gate's output is pulled to ground and remains there until the sampling clock pull it back up. The use of precharged logic thus allows for one-shot operations each time the sampling phase is over. The instance I_6 is a tristate buffer that is enabled by the signal EN. This tristate buffer is used to send a pulse to the comparator at the CMP_PULSE net and then go into high impedance mode afterwards to isolate the bit slice from the other bit slices. As explained before, a tristate buffer is needed to avoid short circuiting the CMP_PULSE node. An effort has been made to reduce the number of transistors in the clock generation and enable logic by using inverting gates.

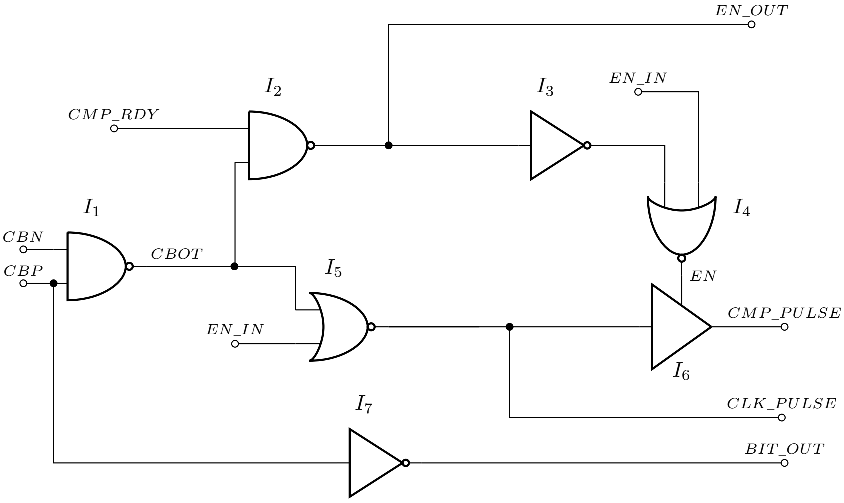

Figure 4.10: Comparator clock generation and enable logic circuit.

As a result, the signal interface contains several signals that are active low. The operation of the circuit will in the following be explained in steps for easier readability:

1. The circuit is first triggered by the enable signal EN_IN going low and the bit slice is then enabled. This forces the enable signal EN to the tristate buffer I_6 to go high and the tristate buffer is activated. At the same time, the signals CLK_CMP and CLK_PULSE will also go high. This action makes the tristate buffer send out a pulse to the comparator and the comparator consequently enters comparison mode. The signal CLK_PULSE is also sent to the CDAC switching circuit and CDAC control logic to enable switching of the CDAC.
2. The comparator will make a decision and cause either of the bottom plates of the CDAC CBP or CBN to go from high to low. This action will change $CBOT$ from low to high, regardless of which bottom plate got switched. The bit output is derived from BIT_OUT. The output bit is dependent on which bottom plate that got switched. The output bit BIT_OUT will be high if the positive CDAC top plate voltage is larger than the negative CDAC top plate voltage.
3. The change in $CBOT$ causes CLK_PULSE and CLK_CMP to go low again and the comparator is put in reset mode.
4. When the comparator has fully settled, CMP_RDY will go high. This action forces EN to go low and the tristate buffer is then deactivated. This also causes the enable out signal EN_OUT to go low and the next bit slice is thus enabled.

The timing diagram for the clock generation and enable logic is shown in Figure 4.11. The timing diagram is given for the case when the comparator pulls v_{op} high.

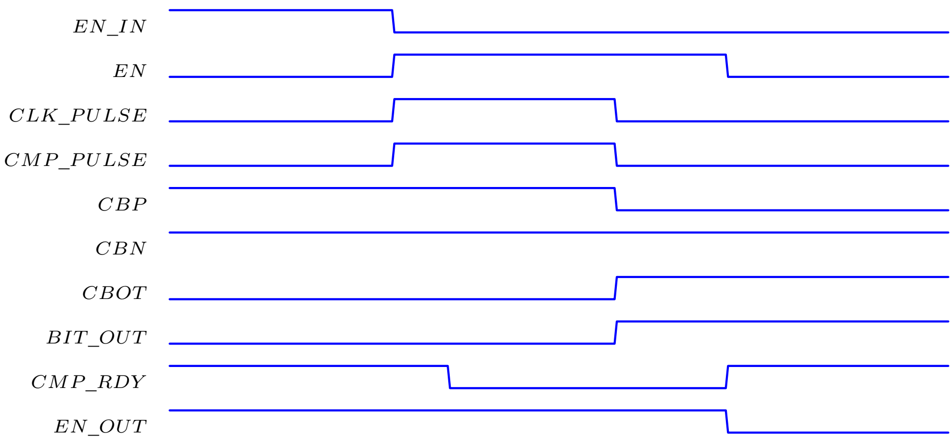

Figure 4.11: Timing diagram for the clock generation logic and enable logic.

4.4 CDAC

This section will show the CDAC used in this thesis. The 10 bit CDAC in this thesis has been built up from a 6 bit capacitor building block that in the following will be referred to as CAP64 when appropriate for easier readability. The following will show the design of CAP64 and how the entire ADC is built up from several blocks of CAP64.

4.4.1 Capacitor Building Block

The 6 bit capacitor used in this is based on the capacitor array topology used in [20]. The capacitor is a metal finger MOM capacitor with the bottom plate in Metal 3 (M3) and Metal 4 (M4), while the top plate is located in M4. The 6 bit capacitor building block will in the following be explained layer for layer and the entire metal stack will be shown in the end.

Figure 4.12a shows M1 layer of CAP64. Each of the vertical lines in M1 seen in Figure 4.12a is one CDAC bottom plate connection. The horizontal lines seen in Figure 4.12a are VIAs that connect up to higher metal layers up to the top plate. Each one of these horizontal lines corresponds to one unit capacitor. By looking at the VIAs in Figure 4.12a, one can see that two of the inputs are connected to one unit capacitor and the other inputs are connected to 2^x unit capacitors for $x = 1, 2, ..., 5$. This shows that the inputs to CAP64 are binary scaled.

The next metal layer Metal 2 (M2) can be seen in Figure 4.12b. Most of the area of M2 are metal fingers that are connected together to ground potential. The connection to ground is done to reduce parasitic capacitance between the bottom plate and the top plate. This is necessary when a small unit capacitance is wanted, since this ground plane will somewhat isolate the bottom plate input in M1 from the top plate in M4. The inclusion of this grounding shield results in smaller unit capacitance C_{unit} and simulations indicate that the inclusion of this grounding plane is beneficial for linearity. Small cuts are made in M2 for the VIAs that go up the to the top plate to not short the bottom plate to the grounding shield.

Metal layer M3 and can be seen in Figure 4.12c. This layer consists of parallel metal fingers that are part of the bottom plate and is coupled to the top plate in the next metal layer. These metal fingers are connected to the previous metal layers and the next metal layers by VIAs.

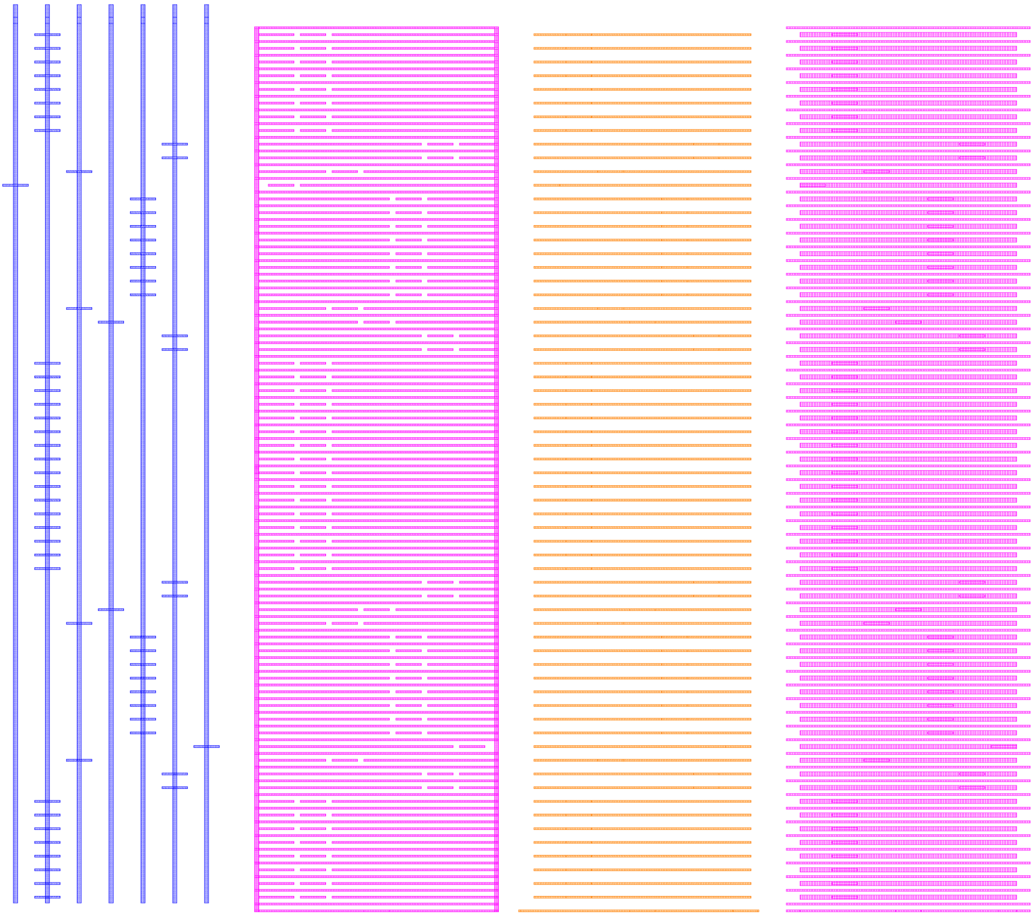
(a) Metal 1 **(b)** Metal 2 **(c)** Metal 3 **(d)** Metal 4

Figure 4.12: Metal stack of CAP64.

The next metal layer M4 consists the top plate and the bottom plate and can be seen in Figure 4.12d. From Figure 4.12d, one can see thin and thick parallel metal fingers. The thin metal fingers seen are part of the top plate and the thick metal fingers are part of the bottom plates. The top plate is capacitively coupled to the thick metal fingers in M4, but also coupled to some of the metal in M3 as explained before. From Figure 4.12d, one can see that the top plate is not complete, as the thin metal fingers are not connected together. It was found that completing the top plate by having a frame around the entire structure as done in [20] would give significant systematic errors for the unit capacitors close to this frame. By not completing the top plate for the capacitor building block, an increase of around 0.51-0.6 bits were achieved in ENOB since the systematic mismatch decreased. However, the top plate has to be completed on top level for the entire CDAC. This is done by stacking several blocks of CAP64 next to each other and complete the top plate by routing metal around the entire structure to connect the top plate together. Another small change done compared to [20] is that the bottom plate fingers are thicker than the top plate fingers. This was mainly done to decrease systematic mismatch a bit at the cost of higher unit capacitance C_{unit}. CAP64 with the entire metal stack can be found in Appendix B in Figure B.6. The total area of CAP64 is 23×3.1 μm^2.

4.4.2 Entire CDAC

The entire CDAC was made out of 16 CAP64 that was stacked next to each other and the top plate was completed by routing additional metal in M4 around the entire structure. Least Significant Bits (LSBs) capacitors have been put in the middle of the array and larger capacitors have been distributed outwards in an alternating fashion to improve matching. The unit capacitance was simulated to be $C_{unit} = 350$ aF and the total area was measured to be 48.4×25.7 μm^2. The CDAC layout can be found in Appendix B in Figure B.7.

4.5 Layout

The top-level layout of the SAR ADC is shown in Figure 4.13 with letter annotations. The total area of the ADC is 59×73 μm$^2 = 0.0043$ mm^2. Layout for selected other building blocks can be found in Appendix B. An enlarged version of the entire top-level layout without letter annotations is also included in Appendix B.

An effort has been made for symmetrical routing for critical nodes, especially the top plate of the CDAC. The main reasoning for symmetric routing is that many layout effects will appear as a common-mode error, thus it will be cancelled by the differential operation. This was seen with the layout of the bootstrapped switch, as the post-layout simulations of a single switch showed a modest reduction in ENOB, but simulations on the entire SAR ADC showed little to no reduction in performance simulating post-layout due to the switch.

The routing of the CDAC top plate is routed from the sampling switch at the bottom of the layout, around the CDAC and then up to the comparator. Shorter routes exists to connect the top plate to the input of the comparator, but the routing used was found to be more

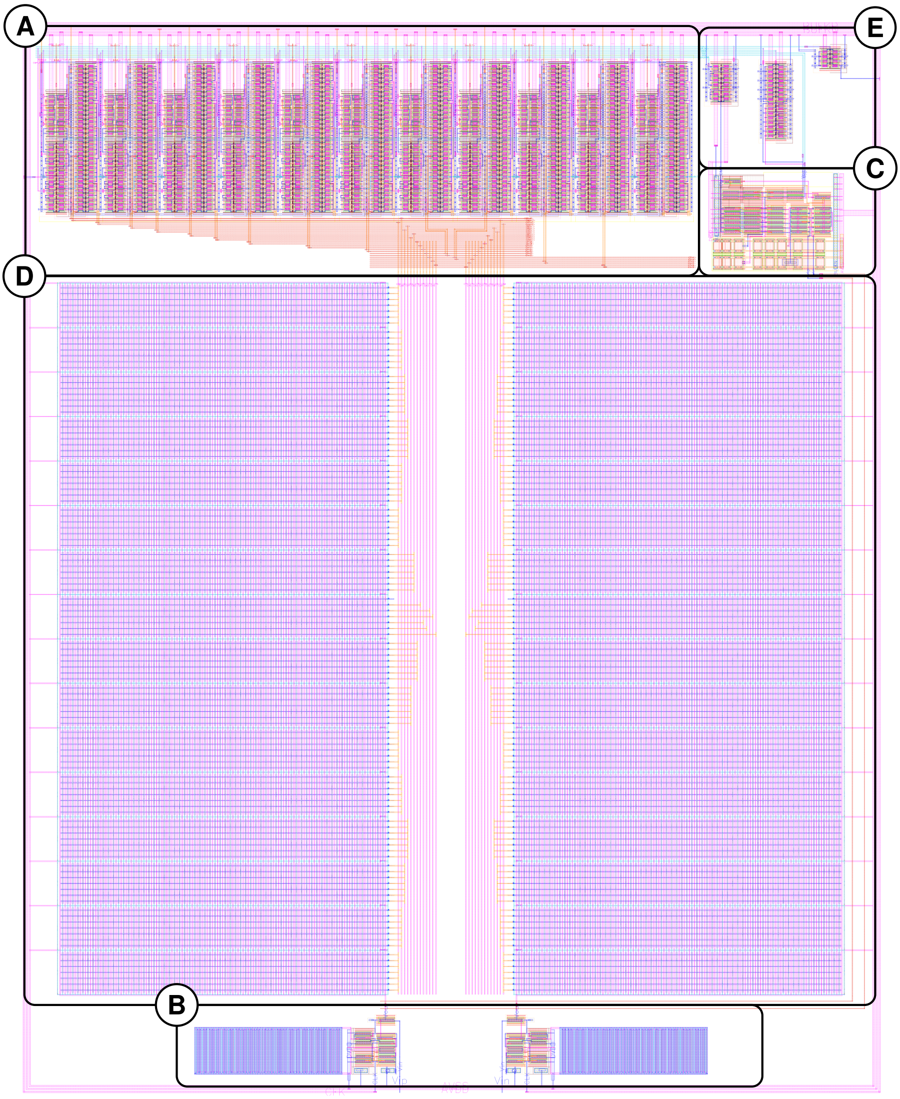

Figure 4.13: Top-level layout of SAR ADC – Digital Circuitry (A), Sampling Switches (B), Comparator (C), CDAC (D), Digital ports at comparator outputs and inverter for inverting sampling clock (E).

"quiet" and consequently gave the best ENOB.

The digital part consists of 11 bit slices that have been cascaded and put as close as possible to the comparator, as these subcircuits exchange a lot of high frequency signals and it is wanted to minimize the parasitic routing capacitance for these nets. The comparator's input transistors are matched by laying out these transistors in a common-centroid configuration and the routing has been done with care internally in the comparator to reduce the systematic offset. The inherent systematic offset from layout was cancelled post-layout by routing some extra metal in M1 at the positive input transistor's drain terminal for a slight increase in capacitance at this node.

The CDAC has been symmetrically put in the middle of everything and the ground plane in M2 of the CDAC has several connections to ground for resistance reduction. The CDAC connections to the digital circuitry has been done by a grid in several metal layers and then connected using VIAs for best use of area. The bootstrapped switch is placed at the bottom of the layout to utilize area to best extent.

The power supply taps go around the entire structure, but taps for biasing the bulks has only been placed at the top of the layout. This is because biasing other circuitry other than the digital part gave worse performance. Analog transistors don't have individual bulks exposed, but the well contact is generally placed on the periphery of the group of transistors. All the digital transistors have their bulk contact exposed on just one side of the transistor. This is mainly done to easy of bulk biasing and to improve regularity when doing layout. The clock signal is routed around the entire structure as hollowed rectangle, but a small slit is cut at the inputs of the sampling switches. This is to avoid any clock coupling to the analog input. This coupling might appear as an common-mode error, but no risks have been taken in routing. Jumpers have been used at certain parts in the digital circuit to avoid antenna rules where large metal to polysilicon connectivity exists and the layout is compliant with the DRC (with the exception of density rules).

The pMOS transistors in the digital circuitry, including top-level digital ports at the comparator's output, has been put in a deep N-well for bulk biasing purposes. This was only done for the digital circuitry, as the analog circuitry will have no benefit of reduced threshold voltage. This will for example affect boosted voltage stored on the capacitor in the sampling switch due to increased leakage or increase overdrive of the transistors in the comparator leading to worse noise performance. The bulks that are not biased will have bulk connections to ground potential.

Chapter 5

Results

This chapter will present the simulation results for the SAR ADC designed in this thesis. All the simulations results in this thesis are obtained from Virtuoso Spectre Circuit Simulator. The test setup schematic and the parameters used for simulations will be covered first. Afterwards, a sweep of the input amplitude is conducted and then simulations results over corners will be presented. This is followed by random mismatch simulations on a typical process corner. Afterwards, the ADC will be characterized over a wide range of input frequencies and sample rates. Lastly, a breakdown of the power consumption of the SAR ADC will be shown for a nominal process corner.

5.1 Test bench Setup

An ADC can be characterized in many different ways, but this thesis will use spectral estimations to obtain the wanted parameters of the ADC. The general idea behind such an approach is to sample a high frequency sinusoid by the ADC and then convert these samples back to decimal form by an ideal DAC for spectral analysis. The spectral analysis allows for estimations of SINAD, which in turn can be used for ENOB estimations. This procedure will be explained more in detail later. In most cases, the input frequency will be set close to the Nyquist rate. This type of testing characterizes the dynamic performance of the ADC, since the input frequencies are of high frequency.

An ADC can also be characterized at DC (or low frequencies) for static characterization. In such a scenario, parameters such as Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) are of importance. However, estimating these parameters requires a lot of samples to establish a good certainty in the results. The typical test method is to obtain a histogram of the output signal and then relate this histogram to the statistical properties of the input signal. The statistical properties can only be estimated well if the sample size is large enough. This means that each of digital words needs to be sampled many times for good statistical estimation. This is problematic for high accuracy ADCs, like the ADC in this thesis, since the number of digital words are many and increase exponentially with the number of bits. Due to the excessive simulation times associated with this type of characterization, it will not be used in this thesis. It is only the dynamic performance that will be investigated.

The test bench schematic used for final verification of the SAR ADC can be found in Figure A.1 in Appendix A. In the test bench, the input sinusoid is supplied as a single-ended signal and an ideal balun is used to convert to differential-signaling. The balun also adds the common-mode voltage to the differential signal. To make the test bench as realistic as possible, some non-ideal effects are also modelled. The sampling clock source, common-mode voltage source and the input sinusoid source all have connections to a series 50 Ω resistor to model the source impedance. Preliminary modelling of the bonding wire and signalpad are done for non-DC signals, such as the sampling clock and the differential signal. In this thesis, the bonding wire inductance has been modelled as an inductor with inductance 2 nH and the pad is modelled as a capacitor with capacitance 100 fF. A resistor with 0 Ω is used to model the signalpad resistance. The pad is assumed to have infinite conductivity in this thesis, but the resistor has been added in case more Electrostatic Discharge (ESD) protection is wanted.

The output bitstream out of the SAR ADC is converted back to decimal form by an ideal DAC. This DAC consists of an ideal sample-and-hold module and an ideal DAC written in VerilogA. To extract the output ENOB, a Fast Fourier Transform (FFT) is performed on the output decimal signal and the SINAD is then estimated from the spectrum. Once the SINAD is known, the ENOB is then calculated by use of Eq. (2.6).

As described above, the input frequency will in most cases be chosen close to the Nyquist rate and the exact frequency is chosen to satisfy coherent sampling to avoid spectral leakage. Due to the coherent sampling, only a rectangular window will be applied to the signal prior to the FFT to avoid spectral smearing. The input frequency is generated from a MATLAB script that computes the input frequency so that a prime number of cycles is always processed by the FFT. The FFT length used in this thesis for all subsequent simulation results are 1024 samples. No change in ENOB was simulated by increasing the number of samples to 2048 or 4096.

To characterize the ADC on a general basis, the popular Walden ADC FoM will be used in the subsequent sections. When the Walden FoM is used, a lower FoM indicate better energy efficiency than higher FoMs. This FoM is given by

$$\text{FoM} = \frac{P}{2^{\text{ENOB}} \times 2f_{in}} \quad \text{[J/conv.-step]} \tag{5.1}$$

Where f_{in} is the input sinusoidal frequency and P is the power consumption of the ADC. The power P of the SAR ADC is calculated by solving the following integral

$$P = \frac{V_{DD}}{T} \int_0^T i(t)dt \tag{5.2}$$

Where T is the simulation time and $i(t)$ is the current going into the ADC. In practice, this is done in Spectre by probing the current going into the V_{DD} pin of the ADC and then taking the average of this current. The power is then calculated by multiplying this current with V_{DD}.

The simulations are performed by doing a noise transient simulation with thermal and flicker noise enabled. The maximum thermal noise bandwidth is set to 10 GHz and no change has been discovered by increasing this parameter. The simulations themselves are performed on a nominal C extracted netlist. Simulations on a RC extracted netlist has not yet been performed, mainly due to a faulty setup that generates parasitic resistances in the kΩ-MΩ range, even when the PDK guidelines have been followed closely.

The integration method, simulation temperature, the accuracy settings, the sampling clock's duty cycle and previously discussed parameters are summarized briefly in Table 5.1. The remaining parameters in Spectre has not been touched and should be at the default values. The tolerance values in Table 5.1 can be increased a bit for a tiny increase in ENOB, but this has not been done to avoid unnecessary long simulation times. The simulation temperature is this thesis is set to the standard temperature of 27°C that corresponds reasonably well with room temperature. The ADC designed in this thesis will only be characterized at this temperature, since no specifications have been set on temperature range for the ADC.

In the following, the parameter V_{BULK} will be represented for bulk biasing. When V_{BULK} is given, it should be understood that the pMOS transistors are biased with a bulk voltage of $-V_{BULK}$ and nMOS transistors are biased with a voltage $+V_{BULK}$. The sampling clock in this thesis is set to 100 MHz and the duty cycle of the sampling clock will in all subsequent simulations be set to 15%. In this thesis, the reference voltage v_{ref} is set to V_{DD}. Unless explicitly stated otherwise, all simulations will be performed with $V_{DD} = 750$ mV, $V_{BULK} = 500$ mV and with input common-mode voltage set to $V_{DD}/2$. These values have been optimized to give best FoM on a nominal process corner.

Table 5.1: Test bench Settings.

Parameter	Value/ Setting
FFT length	1024 Samples
Netlist	Nominal C Extracted Netlist
Integration Method	gear2
Relative Tolerance	10^{-4}
Current Absolute Tolerance	10^{-13}
Voltage Absolute Tolerance	10^{-7}
Simulation Temperature	27°C
Sampling Clock Duty Cycle	15%
Noise Transient Max Frequency	10 GHz

5.2 Input Amplitude Sweep

The ENOB of a converter is strongly related to the input signal of the converter. This is because ENOB is derived from SINAD and SINAD again is directly proportional to the signal strength of the input. Consequently, small input signals will thus lead to low values of ENOB due to the lower signal strength. However, a very large input signal will lead to saturation of the output signal due to gain errors in the ADC. This means that there exist an optimal input signal swing that optimizes ENOB of the converter. To find the optimal input signal swing, a sweep of the input amplitude has been conducted. The results are shown in Figure 5.1 and the input amplitude v_{in} is normalized to V_{DD} and plotted versus ENOB. Each dot in Figure 5.1 corresponds to one transient simulation.

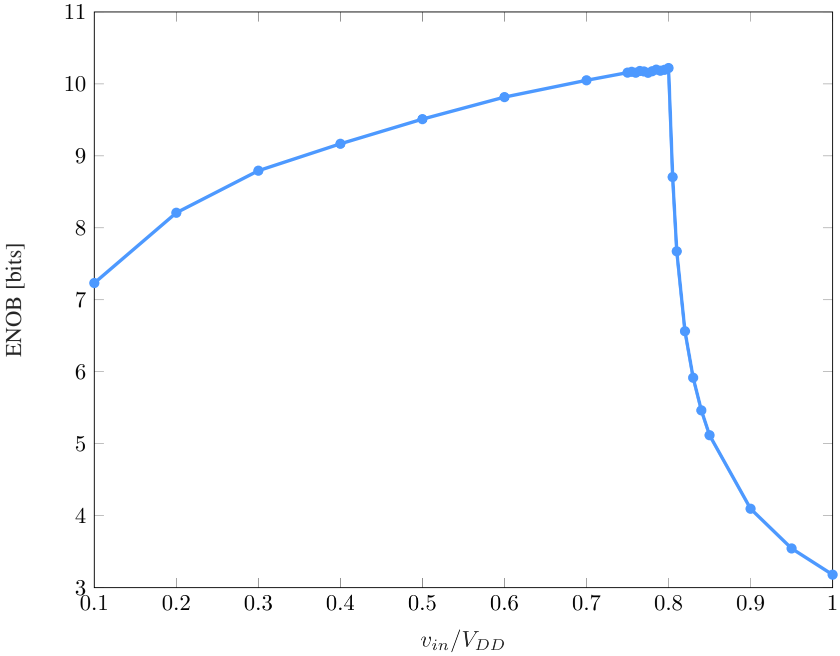

Figure 5.1: ENOB for different values of v_{in}/V_{DD}.

The simulation results show that peak ENOB is 10.22 bits and occurs when $v_{in}/V_{DD} = 0.8$. This value is not very suitable to use, since there is very little margin for gain errors. Any input signal that is larger than this quickly reduces the ENOB of the converter. This is important to consider when random mismatch simulations are conducted, since a small increase in input capacitance of the ADC can yield disastrous results. Instead, the input amplitude has been chosen to be $v_{in}/V_{DD} = 0.785$ and this value give an ENOB of 10.2 bits. The value $v_{in}/V_{DD} = 0.785$ corresponds to $v_{in}/v_{ref} = 0.99$, which has to be considered good performance, since almost the entire dynamic range is used. In terms of absolute values, this means that the output signal has a reduced swing of about 8 mV from the maximal value of v_{ref}. The value $v_{in}/V_{DD} = 0.785$ thus gives a good trade-off between ENOB and margin for random mismatch. This value will be used in all subsequent simulations.

5.3 Corner Simulations

To account for the variability in parameters when a chip is manufactured, process corners simulations have been performed. The corner setup used in this thesis are post-layout corners available from the PDK, no custom changes has been made to the corner setup. The nomenclature used in this thesis is that FF means fast nMOS and fast pMOS, while SF means slow nMOS and fast pMOS. The input frequency for all the corner simulations are $f_{in} = 49.71$ MHz to satisfy coherent sampling and the simulations results over corners of the ADC can be found in Table 5.2. A few comments are in place before the results over corners are discussed. No adjustments have been done to V_{DD} and V_{BULK} if the ADC was fast enough with nominal settings, even if some optimization could be done to for example lower V_{DD}. For SF, the bulk bias voltage V_{BULK} was increased to 700 mV due to speed issues. For the slowest corner SS, the supply voltage V_{DD} has been increased to 800 mV and the bulk voltage V_{BULK} has been set to 1400 mV to make the ADC fast enough.

Table 5.2: Simulation results over corners.

	Typical	FF	SS	SF	FS
V_{DD} [mV]	750	750	800	750	750
V_{BULK} [mV]	500	500	1400	700	500
f_{in} [MHz]	49.71	49.71	49.71	49.71	49.71
Power [μW]	268	329	332	269	283
ENOB [bits]	10.20	10.21	10.29	10.27	10.24
FoM [fJ/conv.-step]	2.28	2.79	2.65	2.18	2.35

The nominal ENOB is simulated to be 10.2 bits and it is seen that the ADC satisfy the specification of at least 10 bits ENOB over all corners with good margin since the ENOB $\geq$ 10.2 bits for all corners. It should also be noted that there is little variation over corners even if some supplies have been adjusted manually. There is some variation of power at FF and SS. In both of these cases, the high power consumption can be explained by extra leakage due to lower threshold voltage. The nominal FoM is 2.28 fJ/conv.-step. This result will be further discussed in the next chapter.

The output spectrum for typical process corner with and without noise is shown in Figure 5.2 as a reference. A simulation without noise enabled yields an ENOB of 10.87 bits due to systematic mismatch and distortion in the ADC. The reduction in ENOB due to systematic errors are thus only 0.13 bits, while the decrease in ENOB from noise is 0.67 bits. It is seen that noise is the dominating factor for ENOB reduction. This should come as no surprise, since high accuracy ADCs are typically limited by thermal noise in the circuit.

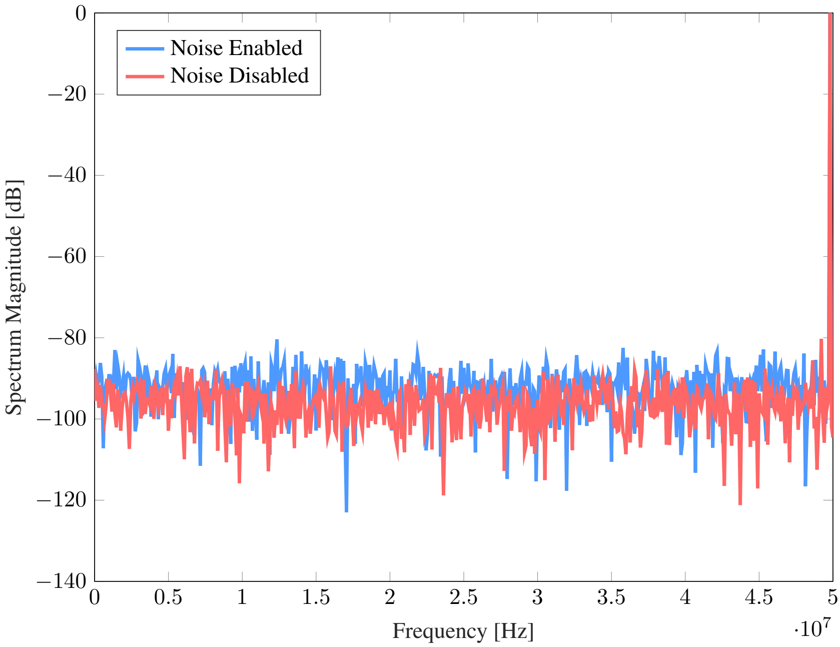

Figure 5.2: 1024 point FFT for nominal corner with and without noise with input sinusoidal frequency $f_{in} = 49.71$ MHz.

It is interesting to compare the error budget to the simulation results. The error budget predicted an ENOB of around 10.23 bits and the nominal simulations results show an ENOB of 10.2 bits. This is very close to the value in the budget. Some discrepancies are tolerated, since the budget was drafted pre-layout and also because some assumptions have been made early on. Nonetheless, the budget has been vital in the design as a general guideline to distribute the error in a reasonable way.

5.4 Mismatch Simulations

To check the random mismatch performance of the ADC, Monte Carlo simulations have been performed. The simulations are performed on a nominal process corner with only mismatch variation enabled. One thing to note is that the CDAC used in this thesis is custom made, meaning no random mismatch model exists for this block. This lower the validity of some of these results, since the random mismatch of the CDAC is likely to cause ENOB degradation. Everything else do have mismatch models and the mismatch models have been utilized during the Monte Carlo simulations.

The mismatch performance was verified by running 30 simulations using a low discrepancy sequence for sampling and the main results are briefly summarized in Table 5.3. The mean value of the mismatch simulations corresponds very well with that of a nominal pro-

Table 5.3: Mismatch results obtained from 30 Monte Carlo simulations.

	Mean	Standard Deviation	Min	Max
Power [μW]	268.50	0.34	267.99	269.45
ENOB [bits]	10.2	0.039	10.04	10.25
FoM [fJ/conv.-step]	2.29	0.064	2.21	2.56

cess simulation and the standard deviation for the parameters are seen to be really small. For the ENOB, it was calculated that the mean value $\mu = 10.2$ bits and the standard deviation $\sigma = 0.039$ bits. To get a more intuitive understanding of how good these results are, the standard deviation σ of ENOB is normalized by the mean μ to obtain $\sigma/\mu = 0.4\%$. This has to be classified as good performance, since the deviation around the mean is very small.

The ENOB obtained from the mismatch simulations are plotted as a histogram in Figure 5.3. The histogram shows that most sample points bundle around the mean of 10.2 bits ENOB and that the variance is very small. Another way to interpret the results is to approximate the resulting ENOB histogram to be Gaussian. This gives $5\sigma \approx 0.195$ bits and this means that 1 in approximately 1744278 of the sample points will not satisfy ENOB $\geq$ 10 bits. This reveals that the ADC has very good mismatch tolerance.

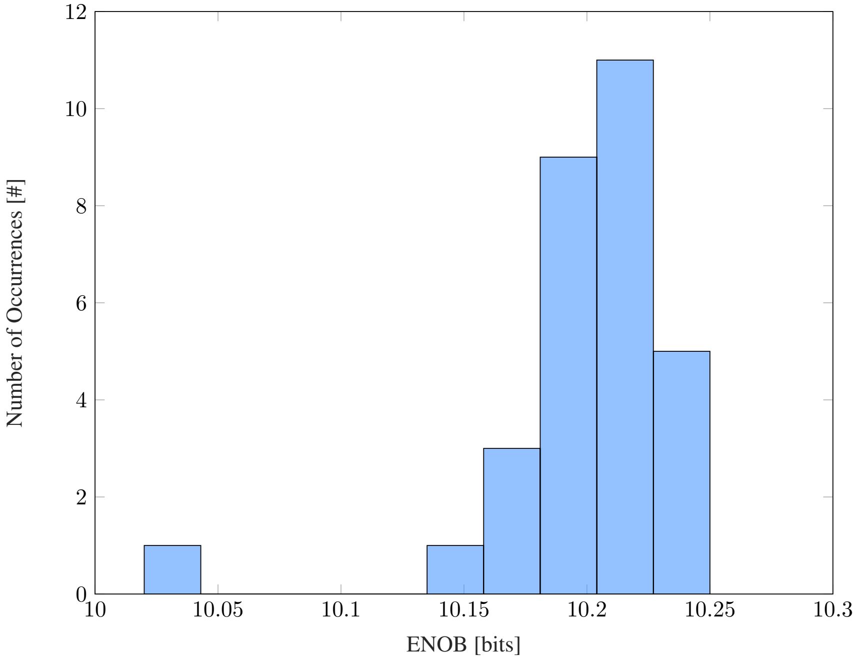

Figure 5.3: ENOB obtained from 30 Monte Carlo mismatch simulations.

However, there is one discrepancy found around 10.04 bits. It was verified from simulations that the decimal output from the DAC would start clipping at this sample point and the ENOB is thus quite lower than the other simulations points. The clipping of the output signal would indicate that the problem is related to gain errors in the ADC. This is caused by an increase in parasitic capacitance to ground at the CDAC top plate and is most likely due to the input pairs of the comparator getting larger. This is really insignificant, as gain errors can be avoided by reducing the input signal swing and this will not affect the SINAD. Ideally, the simulations should be rerun with a bit lower input swing, but this has not been done, mainly due to the time consuming process of running Monte Carlo simulations, but also because the results are satisfying despite the gain errors.

5.5 Input Frequency Sweep

All the preceding simulation results characterized the ADC with an input frequency close to the Nyquist rate. To show that the ADC performs well at other frequencies as well, a sweep of the input frequency has been conducted. The lowest input frequency simulated in this thesis is 1 MHz. Lower frequencies than this has not been simulated, mainly due to difficulty in obtaining coherent sampling with very low frequencies with the used FFT length.

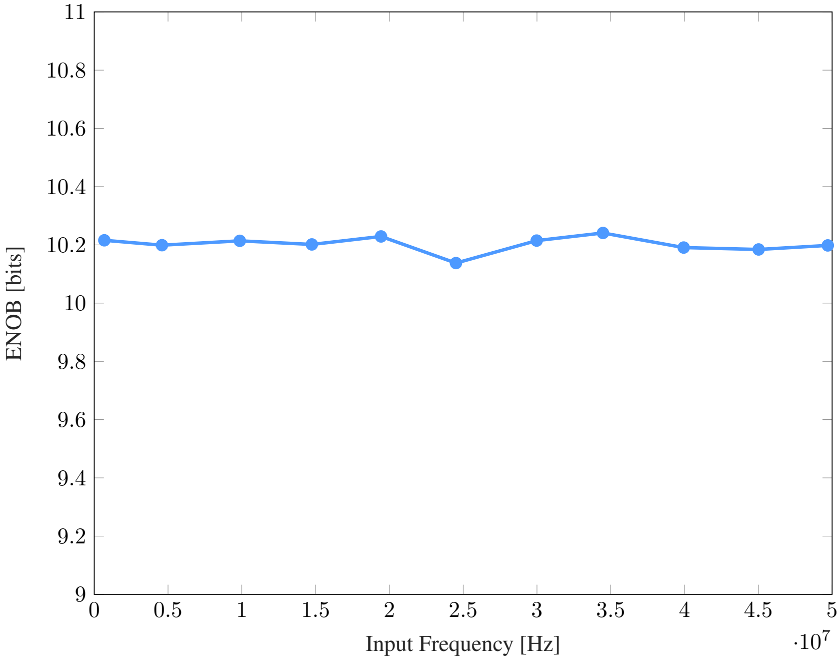

Figure 5.4: ENOB versus input frequency.

The remaining input frequencies are chosen from 5 MHz as a starting point and picked with 5 MHz increments up to 50 MHz. The exact frequencies are chosen for coherent sampling as before and the simulations are performed on a nominal process corner. The resulting ENOB versus frequency is shown in Figure 5.4. The ENOB is for most practical purposes constant over the entire bandwidth with an mean value of around 10.2 bits. This show overall good quality of design for an ADC. Some inconsistencies are seen, but these could be due to the finite number of samples obtained from a noise transient. No degradation in ENOB is seen for higher frequencies. This suggest that the sampling switch in this thesis is well designed, as this switch acts like a lowpass-filter and will attenuate higher input frequencies. No other blocks in the ADC have frequency dependent effects for a given sample rate.

5.6 Sampling Rate Sweep

The specification for this ADC is a sample rate of 100 MS/s, but it is still interesting to test the designed ADC with different sample rates to check performance in general. Two sweeps have been performed with the sample rate. One sweep is performed with $V_{DD} = 700$ mV and $V_{BULK} = 500$ mV for all the sweep points, while the other sweep has optimized supply voltages for each sample rate. In each of these sweeps, the sample rate starts at 20 MHz and is incremented in 20 MHz steps up to 100 MHz. All the input frequencies are picked to satisfy coherent sampling and be close to the Nyquist rate. Table 5.4 briefly summarizes the results when $V_{DD} = 750$ mV and $V_{BULK} = 500$ mV for all the sample rates.

Table 5.4: Simulation results for different sample rates f_s with constant $V_{DD} = 700$ mV and $V_{BULK} = 500$ mV.

	$f_s = 20$ MS/s	$f_s = 40$ MS/s	$f_s = 60$ MS/s	$f_s = 80$ MS/s
V_{DD} [mV]	700	700	700	700
V_{BULK} [mV]	500	500	500	500
f_{in} [MHz]	9.94	19.88	29.82	39.77
Power [μW]	52.76	96.89	140.80	184.70
ENOB [bits]	10.12	10.12	10.16	10.10
FoM [fJ/conv.-step]	2.38	2.19	2.06	2.12

It is seen that the ENOB stays practically constant for a given sample rate and with constant supplies. This should make sense, since signal strength depends on voltage supplies and noise of active devices depends on biasing conditions[1]. The power also increases in an almost linear fashion as expected. The main reason for deviation from linearity is probably the constant leakage current that is common for all the points in the sweep. The best FoM from the sweep is 2.06 fJ/conv.-step and this is obtained when the sample rate is 60 MS/s. This is a local minima for the FoM and is better than the FoM achieved for the intended sample rate of 100 MS/s.

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[1] If thermal noise is assumed to be the dominating noise factor

The previous sweep has constant voltage supplies for the entire sweep. It is also interesting to see what happens if the supplies can also be adjusted to each sample rate as seen in Table 5.5. The supplies are not optimized for ENOB, but the voltage supplies have been turned down until the ADC is "fast" enough for conversion of all bits. This is done to save time, since ENOB optimization takes up a lot of time. Looking at the results, one thing that is really noticeable is the huge reduction in power when the supplies also goes down. This can be attributed to the square dependency between active power and V_{DD}.

Table 5.5: Simulation results for various sample rates f_s with different V_{DD} and V_{BULK}.

	f_s = 20 MS/s	f_s = 40 MS/s	f_s = 60 MS/s	f_s = 80 MS/s
V_{DD} [mV]	475	525	600	660
V_{BULK} [mV]	250	500	500	500
f_{in} [MHz]	9.94	19.88	29.82	39.77
Power [μW]	20.80	51.30	99.70	162.00
ENOB [bits]	9.51	9.7	9.98	10.09
FoM [fJ/conv.-step]	1.44	1.55	1.66	1.87

Table 5.5 also shows that ENOB goes down with the supply voltage. It is speculated that this is because of smaller quantization steps due to lower supply voltages while noise reduction is not linear with supply. This should make sense, since the lower voltage supply decreases the available signal power. In addition, noise sources like kT/c of the CDAC and flicker noise do not have dependencies on supplies. The reduction of V_{DD} voltage will thus not have any effect on these noise sources. The noise from the comparator and the bootstrapped switch will be reduced with lower supply voltages, as this changes the biasing conditions of these blocks, but this reduction is probably not linear. It is also interesting to see that the FoM for all points in the sweep is better compared to when the sample rate is 100 MS/s. The minimum FoM is 1.44 fJ/conv.-step for lowest sample rate at 20 MS/s and that the FoM increases with higher sampling rates.

5.7 Power Consumption Breakdown

This section will give a detailed breakdown of the power consumption in the SAR ADC. The power estimation will be given in terms of currents where the dynamic current and leakage current is merged into a single number. Due to difficulty in extracting currents at top-level layout, the values presented here will give the power consumption when the top-level is simulated on schematic, but all the blocks are simulated on layout. The total power will thus be a bit off, but the relative power consumption of the blocks should be quite accurate nonetheless. The values will be given for a nominal process corner and can be seen in Table 5.6.

It seen is seen that the distribution of power is very evenly distributed, since most blocks consume around 25% of the total power. The even power distribution is a good sign overall, meaning no block consumes excessive power. If one block consumed a large portion

Table 5.6: Power consumption breakdown for a nominal process.

Block	Current [μA]	Relative Power Consumption [%]
Comparator	96.1	27.9
CDAC	90.2	26.1
Digital Circuitry	82.4	24.0
Top-level Digital Ports	72.4	21.1
Sampling Switch	2.9	0.8
Total	344	100

of the power, then the overall power distribution would be dominated by that block and it would be very difficult to to reduce overall power without doing design changes to the dominating block. When the power is well distributed like this, then any of the blocks can be optimized for power and the overall power reduction will still be significant.

The leakage current is estimated to be around 8 μA and majority of this leakage comes from the digital circuitry. This should come as no surprise, since the digital transistors are many and the bulks of these transistors are bulk biased for lower threshold voltage. Although the leakage is large, the lower threshold voltage allows for lower values of V_{DD} and leads to better FoM.

One thing that comes to mind is the power consumption of digital ports at top level. These are the digital ports that uses the comparator's outputs to generate signals to the digital circuitry, but also the clock driver of the comparator clock. These consume 21$\%$ of the total power, which is very much, considering they just provide control signals to the digital circuitry. It does makes sense that the power consumption is so high, since they are clocked by the comparator clock and the ports also drive large capacitive loads.

Another interesting aspect is the power consumption of the sampling switch, which is very low compared to the other blocks. This was seen early in the design and the sampling switch has thus seen the least optimization for performance due to this. This is due to the low capacitive loading of the switch and because this circuit is clocked by the relatively slow sampling clock. This clock is much slower than the comparator clock found internally in the ADC.

Chapter 6

Discussion

This chapter will discuss the simulation results of the ADC designed in this thesis. First, the designed ADC will be compared to state-of-the-art ADC designs with similar specifications. Different parameters will be brought up, but it is mainly the Walden FoM that will be used for comparisons. Afterwards, areas of future improvements and issues regarding the designed ADC will be covered.

6.1 Comparison to State-of-the-art

The following section will present how the designed ADC fare with state-of-the-art ADCs. The ADC survey [1] by Boris Murmann has been used as a source of ADC designs, mainly due to ease of comparison. This survey contains ADC data from International Solid-State Circuits Conference (ISSCC) and VLSI conferences and should give a good indication of state-of-the-art ADC designs in the academic world. The main focus has been to find designs with samples rate with tens of MS/s for fair comparison, but one ADC with outstanding FoM with kS/s sample rate is also presented to give a better overview of achievable FoM for lower frequencies and fewer bits. This comparison will only include Nyquist ADCs to limit the scope of comparison, but also to make the comparison more direct. A table with state-of-the-art comparisons are shown in Table 6.1.

When the ADC designed is compared to state-of-the-art ADCs, it is seen that the energy efficiency is superior by comparing the FoMs of the presented ADCs with similar specifications. However, the ADC with best FoM is around 5 times more energy efficient than the ADC designed in this thesis. This comparison is unfair, mainly due to the low sampling rate and fewer bits ENOB for that ADC. Out of all the ADCs presented, it also seen that the area of the designed ADC is the smallest. This can probably be attributed to the small CDAC used in this thesis. For SAR ADCs with many bits, it is not uncommon that the CDAC takes up most of the top-level layout area.

Table 6.1: State-of-the-art ADC comparison.

Paper	[4]	[21]	[22]	[23]	This Thesis
Architecture	SAR Assisted Digital Slope	SAR ADC with Semi-Resting DAC	SAR with VCO and TDC	SAR Assisted Pipeline	Pure SAR
Technology	28 nm	90 nm	45 nm	45 nm	22 nm FDSOI
Sampling Rate	100 MS/s	600 kS/s	200 MS/s	80 MS/s	100 MS/s
Area	0.0047 mm^2	0.035 mm^2	0.08 mm^2	0.14 mm^2	0.0043 mm^2
Power	350 μW	187 nW	3.4 mW	1.5 mW	268 μW
ENOB	10.41 bits	9.46 bits	11.00 bits	10.67 bits	10.2 bits
FoM [fJ/conv.-step]	2.58	0.44	6.90	11.51	2.28

The ADC designed in [4] is similar to the ADC designed in this thesis when it comes to both FoM and area. This ADC currently holds the record for most energy efficient SAR ADC with ENOB around 10 bits and sampling rate at 100 MS/s in Murmann's ADC survey, but the ADC designed in this thesis is marginally better. The comparison is of course a bit unfair, since the latter ADC was measured in the lab, while the ADC in this thesis is just simulated in software. Physical verification might show other results, depending on what has been modelled and what has not been modelled in the PDK.

It should also be noted that this thesis uses a smaller process node than the other ADCs presented. It is a well known fact that the SAR ADC scale very well with smaller transistors. This might partially explain the exceptional FoM. The ADC designed in this thesis unique nonetheless, since no other pure SAR ADC has managed the same resolution and speed to the author's knowledge. The usual approach for similar specifications is by doing more complex architectures, such as pipelining or by using SAR assisted architectures. Another approach is to use calibration as done in [8]. The benefit of using a simple SAR ADC, such as in this thesis, is that the complexity is reduced significantly leading to shorter development times.

6.2 CDAC Mismatch

Although the results in this thesis are promising, there are some concerns of things that are not modelled. In this thesis, the CDAC is custom made, so no stochastic mismatch model exist for this block. This further means that the random mismatch in the CDAC is not included in the mismatch simulation results and that the corner simulations are simulated with nominal capacitance values for the CDAC. Since no tape-outs have been done in 22 nm FDSOI yet at the author's location, it is difficult to say something about the random mismatch of the CDAC. It is clear that the inclusion of random mismatch would most likely reduce the ENOB. The CDAC used is a MOM capacitor and it would be possible to use the PDKs model for MOM capacitors to obtain some sensible results. This has not been done, mainly due to time constraints, but it is an approach that is interesting. On the other hand, systematic mismatch has been modelled through parasitic extractions. Only nominal extractions have been performed. Again, this is mainly due to the limited timeframe for this thesis.

The CDAC designed in this thesis does not use minimum metal rules. The geometry is simply derived from the original CDAC used in [20]. It would be interesting to further work on the CDAC so that minimum metal (or close to) rules are followed. This will definitely affect the random and systematic mismatch of the CDAC and the kT/c noise will clearly be increased as a result. However, it is an interesting area to research, as downscaling the CDAC would benefit area, power and speed. If the CDAC geometry is altered, then a random mismatch model should be implemented for the CDAC. Aiming for a smaller unit capacitance without considering the increase in random mismatch is not a feasible approach.

6.3 Sampling Clock

The sampling clock in this thesis had a duty cycle of 15% and such a duty cycle might be difficult to realize in the lab for physical verification. This of course depends on equipment, since very expensive equipment has capability to vary the duty cycle over a wide range with good resolution.

In less refined testing setups, the sampling clock has to be provided sine-generator. In that case, one have to resort to sine-to-square-generators, use frequency dividers and digital ports to obtain the wanted duty cycle. Of course there is limitations in such a setup. For example, consider a wanted duty cycle of D and a wanted clock frequency of f. This means that the output frequency out of the generator has to be Df. This clock frequency then needs to be reduced down to f by dividing the frequency by D. The original clock and the divided-down clock can then be used to generate a duty cycle of D by use of digital ports. This means that not all duty cycles of interest can be generated, since $D \in \mathrm{N}$. This again means that a duty cycle of 15% is difficult to realize. A duty cycle of for example 12.5% is very easy to generate by division of $2^3 = 8$ since $1/8 = 0.125$.

A duty cycle of 12.5% was simulated and was found to be troublesome due to the limited sampling time. If this is related to the sampling switch or due to the speed of the digital circuit is uncertain. If the sampling switch is too slow, then the multiplier of the switching transistor could be increased to increase the strength of this transistor. If the problem lies in the digital circuitry, then the digital unit transistors' dimensions have to be increased. Some local optimization could also be performed in each bit slice for nodes that are very slow to allow for faster operation. It is also possible that a smaller CDAC would allow for a duty cycle of 12.5% due to less capacitance.

Another solution is to increase the duty cycle to something higher than 15%. Increasing the duty cycle is problematic, since it would be difficult to make the ADC fast enough over corners with such a duty cycle without some design changes. The main problem is that the digital circuit is too slow over corners which needs to be resolved, either by redesign or increase of W/L of the digital unit transistor used in this thesis.

6.4 Digital Circuit

It is clear that the main speed bottleneck in this thesis is the digital circuitry. The digital circuitry performs excellent on schematic, but the extra routing capacitance on layout makes the digital circuitry a bit slow. This was compensated over corners by mainly increasing V_{BULK}, but V_{DD} was also increased a bit for SS process corner. While this works, it is not really a robust solution as it requires manual adjustments. In the end, some redesign should be done to the digital circuitry to avoid excessive adjustments of parameters for right functionality. The architecture may require some changes, but easiest solution is to increase W/L of the digital unit transistor for faster operation.

To avoid manual adjustments of V_{BULK}, it is possible to measure PVT variations and then make a compensation circuit that works on negative-feedback to adjust V_{BULK} to counteract these variations. One such solution is presented in the master thesis in [24]. The result presented in that thesis shows excellent compensation over PVT variations and the power consumption of such a compensation circuit is very modest. One also need to keep in mind that such a circuit is not meant for a single-circuit, but can work over the entire chip to make the entire chip less vulnerable to variations. Such compensation could be part of future improvements to increase robustness.

The proposed ADC also uses a single bit slice for both split-monotonic switching and monotonic switching. The bit slice is designed to support both split-monotonic switching and monotonic switching, but a similar bit slice that only works for monotonic switching could be designed to avoid wasting energy on unused circuitry. The approach used in this thesis was very attractive for initial design, since the development time was shortened by using a single bit slice for the entire digital circuitry. Another advantage is the flexibility to switch the common-mode up or down for monotonic switching. Initial simulations showed that switching the common-mode up to be the best design choice, but the finalized design switches the common-mode down. For a finalized design, this flexibility is not needed, and the ADC could be more energy efficient by using one bit slice for split-monotonic switching and one bit slice for monotonic switching.

6.5 Digital Ports

It was shown that the digital ports at top-level consumed almost a quarter of the power. This is very much, considering these ports only provide auxiliary signals for the digital circuitry. If the power consumption of the digital circuitry is combined with the power consumption of the digital ports, then this almost constitutes half of the total power of the entire ADC. This is very much power for a ADC that should thermally limited. For a SAR ADC that is thermally limited, it makes most sense that the comparator should be dominating power source, since the kT/c noise suppression is very energy demanding. This is because a thermally limited ADC requires a fourfold increase in power is needed to increase ENOB by one bit. It is possible that these auxiliary signals could be generated locally in each bit slice for better power efficiency. This would eliminate power consumption of large capacitive nets to the digital circuitry. An alternate solution for the digital circuitry could also be developed, removing the need of these signals. The latter option is the most feasible solution, but doing so would require modest changes to the digital circuitry.

Chapter 7

Conclusion

This thesis showed the design of an energy efficient SAR ADC in 22 nm FDSOI intended for medical ultrasound applications. The ADC designed has pushed the limits in speed and accuracy possible for a simple pure SAR ADCs. Post-layout simulations on a nominal process corner yields 10.2 bits ENOB with a sampling frequency of 100 MS/s. The power consumed by the ADC is 268 μW and the resulting mean Monte Carlo Walden FoM is 2.29 fJ/conv.-step. These results shows that the designed ADC perform better than state-of-the-art ADCs with similar specifications.

7.1 Future Works

The author of this thesis will have more opportunities to work on this ADC as a Ph.D. student at Norwegian University of Science and Technology (NTNU) starting fall 2018. It would be interesting to tape-out the ADC designed in this thesis for physical verification. Some changes probably has to be done prior to tape-out, as the duty cycle used for the sampling clock in this thesis is troublesome to achieve with the current measurement setup. The duty cycle most likely needs to be increased a bit for physical verification, which means the ADC needs to be faster. The digital portion of the ADC definitely needs some rework to increase the speed to handle a longer duty cycle. The easiest way to increase the speed is to increase the driving strength of the digital unit transistor and use the current architecture. It is also possible that the digital circuitry architecture can be improved slightly. More specifically, it is seen that top-level digital ports consume a significant portion of the power and it would be advantageous to get rid of these ports to improve energy efficiency. Another area to research is to change the current geometry of the CDAC to use minimum metal rules for lower power consumption and higher speed, but at the cost of higher kT/c noise and more mismatch in the capacitor array of the CDAC. A random mismatch model should in that case be implemented to include the increase in random mismatch.

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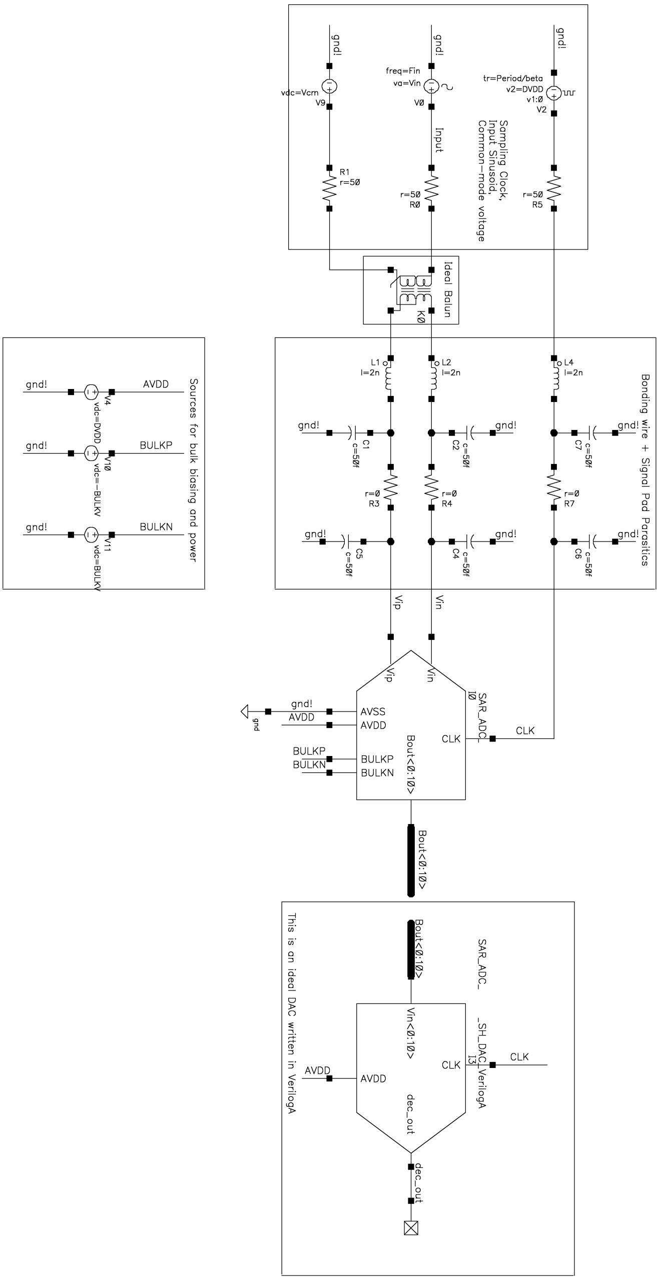
Appendix A

Schematics

This appendix will show some of the schematics as they appear in Cadence Virtuoso. Some processing have been performed to adjust the contrast of the pictures for better readability. Names of instances have been partially blurred out to not reveal the process house used.

Standard digital ports and the unit transistors will not be shown here. This is mainly done to not overflow the Appendix with simple standardized circuits. Digital ports of more specific use will be shown, such as the precharged NAND gate or the tristate buffer.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V0
tr=Period/beta
v2=DVDD
v1:0
V2
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r=50
r=50
R0
r=50
R5
Input
Sampling Clock,
Input Sinusoid,
Common-mode voltage
Ideal Balun
K0
Sources for bulk biasing and power
AVDD
V4
vdc=DVDD
BULKP
V10
vdc=-BULKV
BULKN
V11
vdc=BULKV
L1
l=2n
L2
l=2n
L4
l=2n
C1
c=50f
C2
c=50f
C7
c=50f
r=0
R3
r=0
R4
r=0
R7
C5
c=50f
C4
c=50f
C6
c=50f
Bonding wire + Signal Pad Parasitics
Vip
Vin
SAR_ADC_
I0
AVSS
AVDD
CLK
BULKP
BULKN
Bout<0:10>
gnd
CLK
Bout<0:10>
This is an ideal DAC written in VerilogA
SAR_ADC_
_SH_DAC_VerilogA
I3
Vin<0:10>
CLK
AVDD
dec_out
dec_out

Figure A.1: Schematic of test bench used for final verification.

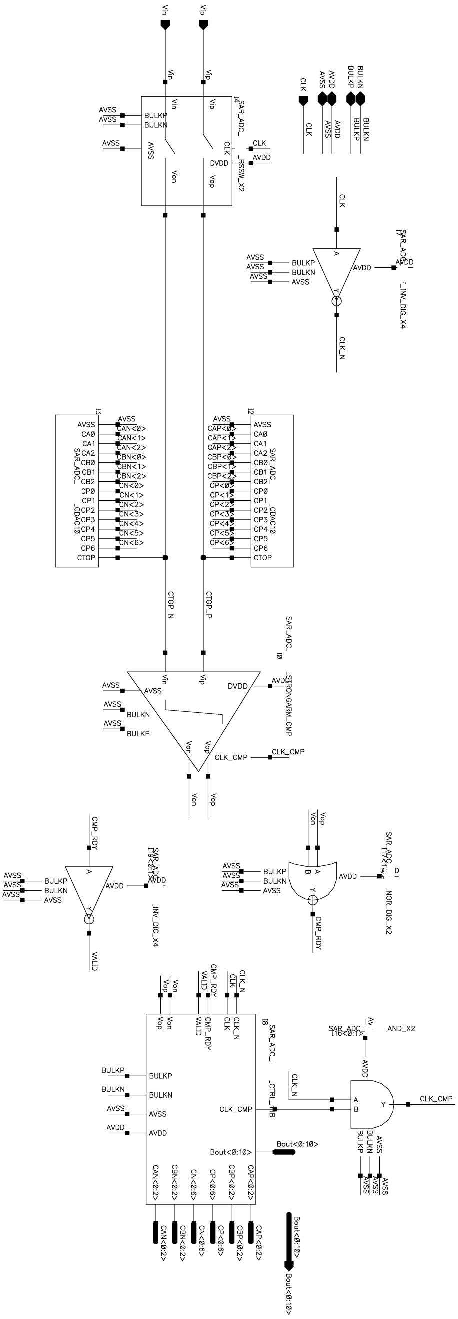
Vin
Vip
SAR_ADC_BSSW_X2
CLK
AVDD
AVSS
BULKP
BULKN
DVDD
Von
Vop
SAR_ADC_INV_DIG_X4
CLK_N
SAR_ADC_CDAC10
CTOP
CTOP_N
CTOP_P
CAN<0:2>
CBN<0:2>
CN<0:6>
CP<0:6>
CBP<0:2>
CAP<0:2>
SAR_ADC_STRONGARM_CMP
CLK_CMP
CMP_RDY
SAR_ADC_NOR_DIG_X2
VALID
SAR_ADC_CTRL_11B
Bout<0:10>
AND_X2

Figure A.2: Schematic of top level SAR ADC.

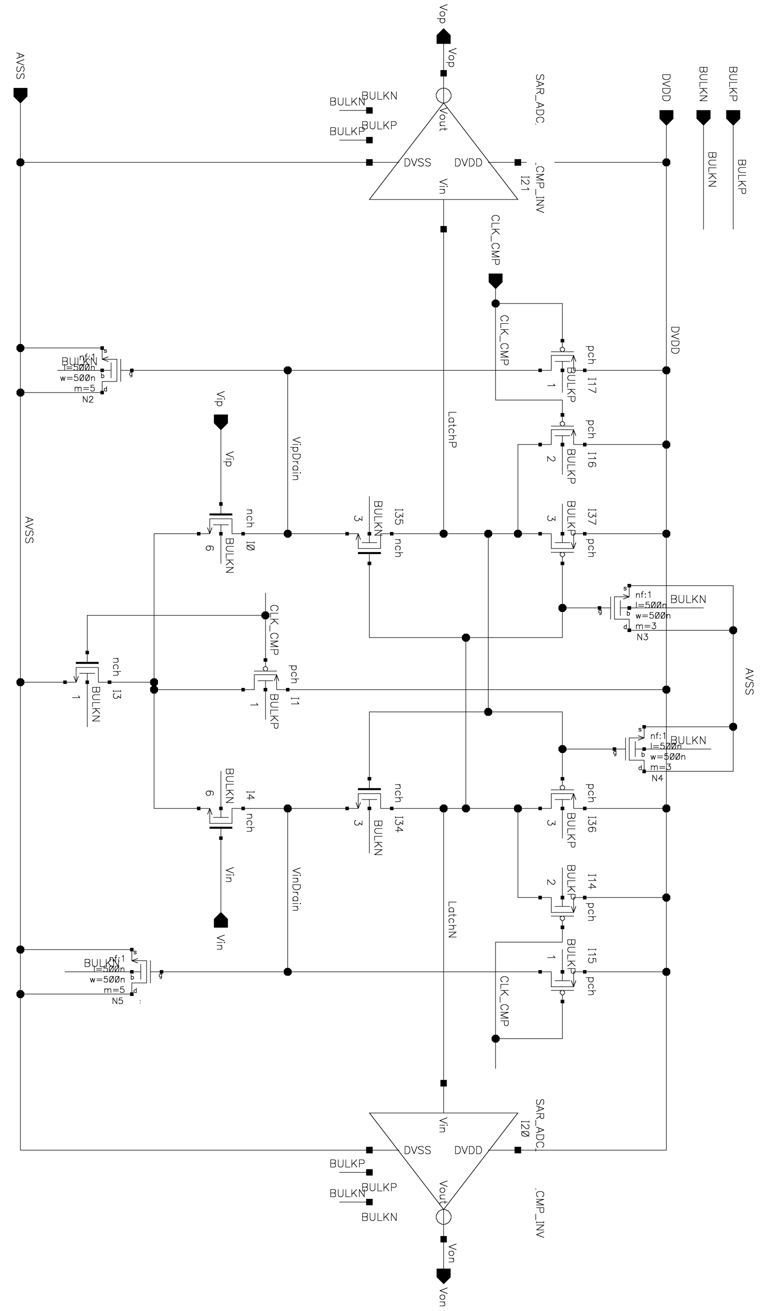
Vop
AVSS
DVDD
BULKN
BULKP
SAR_ADC_CMP_INV
I21
Vout
DVSS
DVDD
Vin
CLK_CMP
pch
I17
I16
I37
I36
I14
I15
nch
I35
I34
I0
I4
I3
I1
BULKN
BULKP
nf:1
l=500n
w=500n
m=5
m=3
N2
N3
N4
N5
Vip
VipDrain
VinDrain
LatchP
LatchN
Vin
I20
Von

Figure A.3: Schematic of comparator.

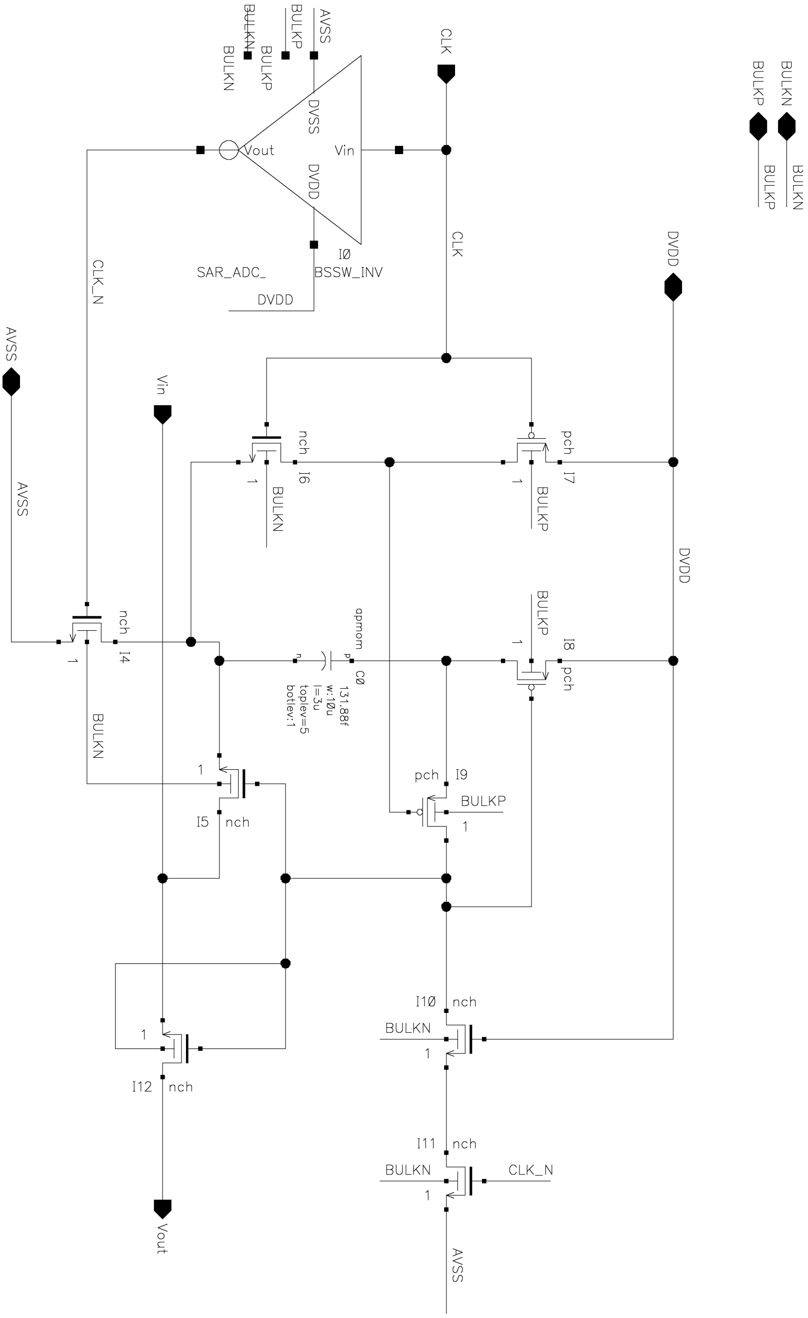
AVSS
BULKP
BULKN
BULKP
BULKN
CLK
BULKN
BULKP
BULKN
BULKP
DVSS
Vin
Vout
DVDD
I0
SAR_ADC_
BSSW_INV
DVDD
CLK
CLK_N
DVDD
AVSS
Vin
nch
I6
1
BULKN
pch
I7
1
BULKP
AVSS
DVDD
nch
I4
1
BULKN
apmom
C0
131.88f
w:10u
l=3u
toplev=5
botlev:1
BULKP
I8
pch
1
pch
I9
BULKP
1
1
I5
nch
I10
nch
BULKN
1
1
I12
nch
I11
nch
BULKN
CLK_N
1
Vout
AVSS

Figure A.4: Schematic of bootstrapped switch.

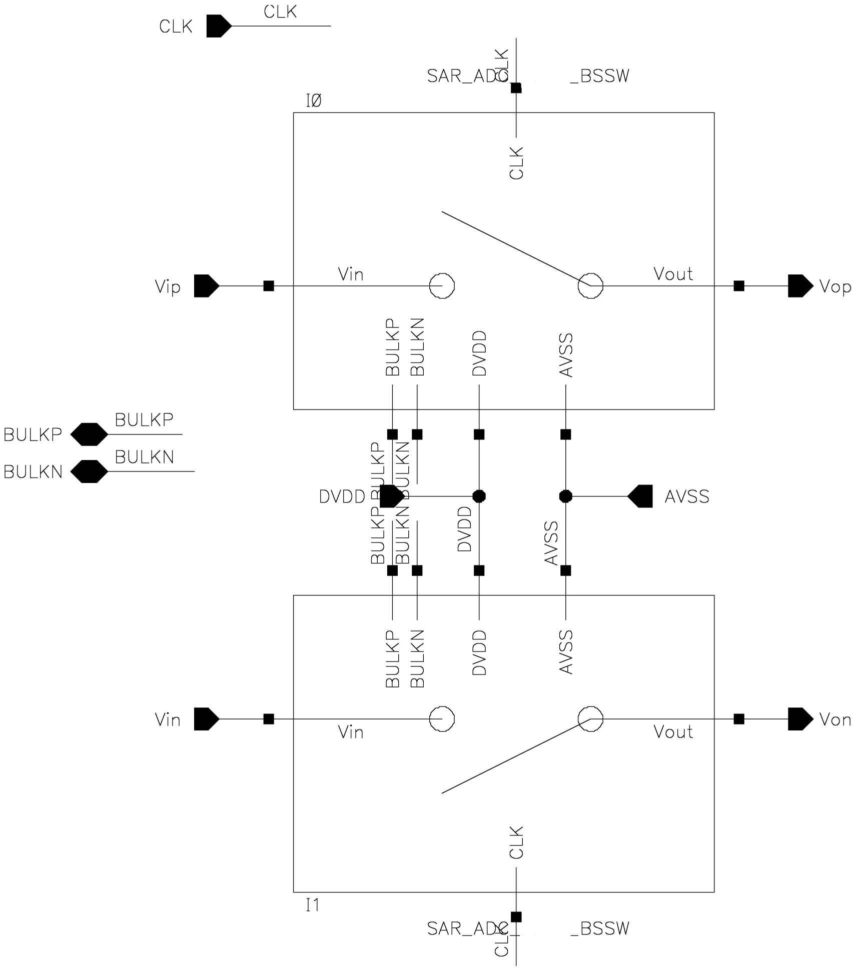
CLK
CLK
CLK
SAR_ADC_BSSW
I0
CLK
Vip
Vin
Vout
Vop
BULKP
BULKN
DVDD
AVSS
BULKP
BULKP
BULKN
BULKN
DVDD
AVSS
Vin
Vin
Vout
Von
CLK
I1
SAR_ADC_BSSW
CLK

Figure A.5: Schematic of bootstrapped switch for both inputs.

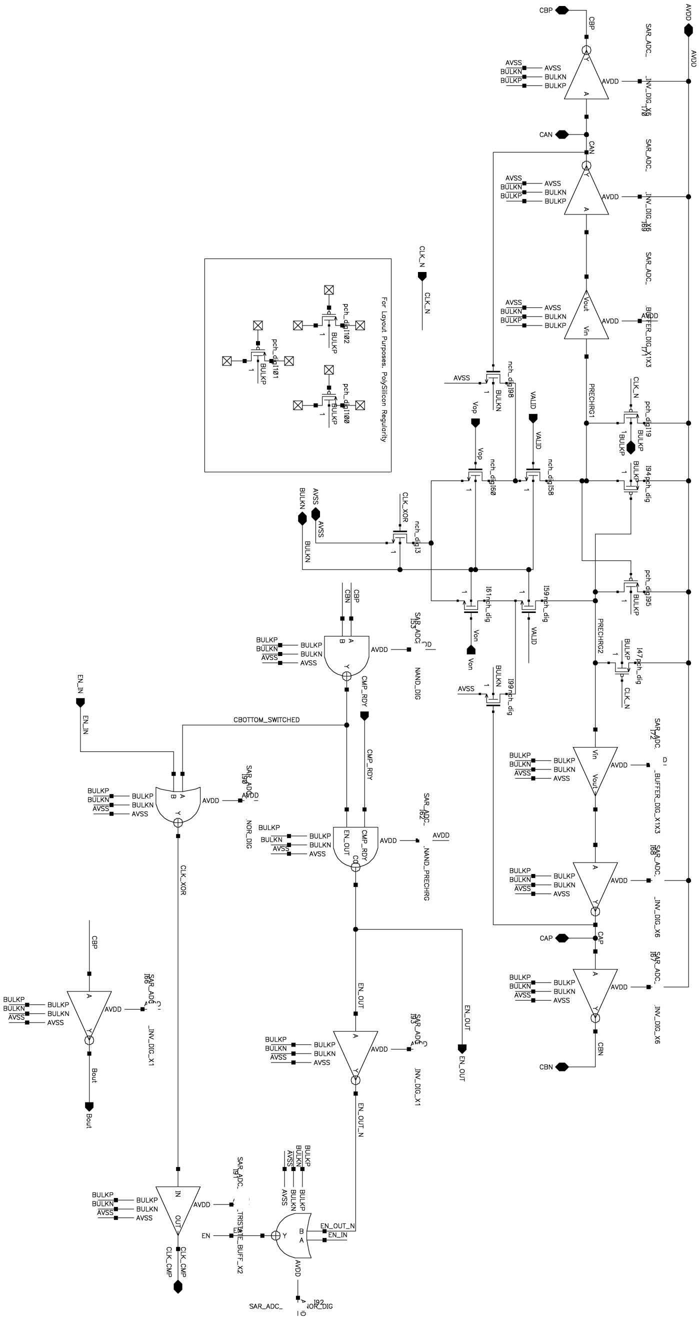
CBP
CAN
CAP
CBN
AVDD
AVSS
BULKN
BULKP
SAR_ADC_
_INV_DIG_X6
_BUFFER_DIG_X1X3
CLK_N
VALID
Vop
Von
PRECHRG1
PRECHRG2
CLK_XOR
NAND_DIG
CMP_RDY
CBOTTOM_SWITCHED
EN_IN
NOR_DIG
_NAND_PRECHRG
EN_OUT
EN_OUT_N
_INV_DIG_X1
Bout
CLK_CMP
_TRISTATE_BUFF_X2
EN
For Layout Purposes: PolySilicon Regularity

Figure A.6: Schematic of a single bitslice.

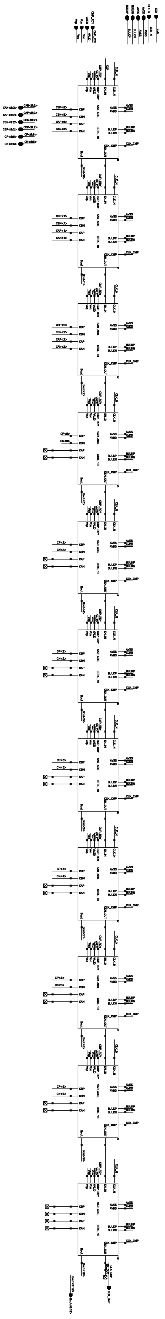

Figure A.7: Schematic of all the bitslices.

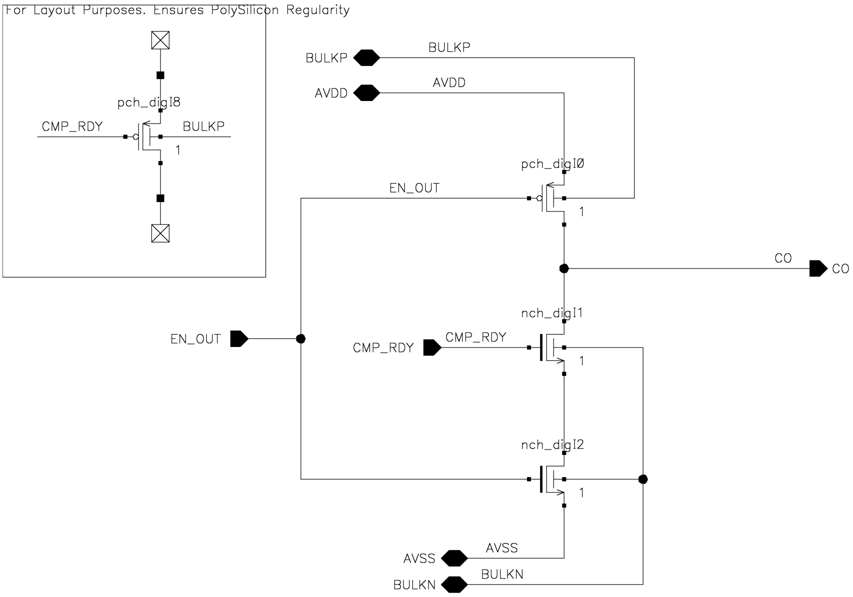
For Layout Purposes. Ensures PolySilicon Regularity
pch_digI8
CMP_RDY
BULKP
1
BULKP
AVDD
pch_digI0
EN_OUT
CO
nch_digI1
EN_OUT
CMP_RDY
nch_digI2
AVSS
BULKN

Figure A.8: Schematic of precharged NAND gate.

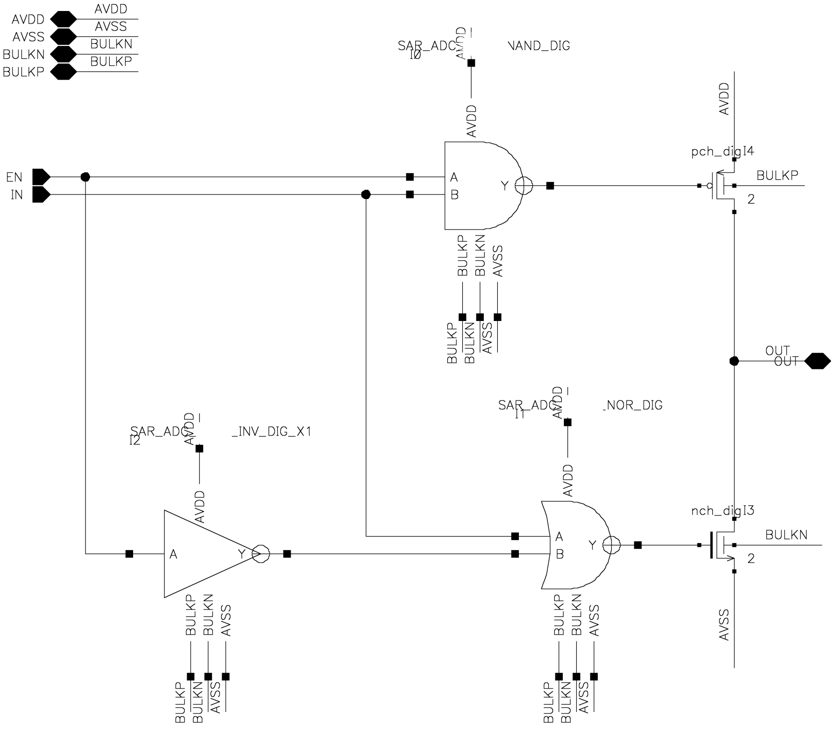
AVDD
AVSS
BULKN
BULKP
SAR_ADC_NAND_DIG
I0
EN
IN
A
B
Y
pch_digI4
BULKP
2
OUT
SAR_ADC_NOR_DIG
I1
SAR_ADC_INV_DIG_X1
I2
nch_digI3
BULKN
AVSS

Figure A.9: Schematic of tristate Buffer.

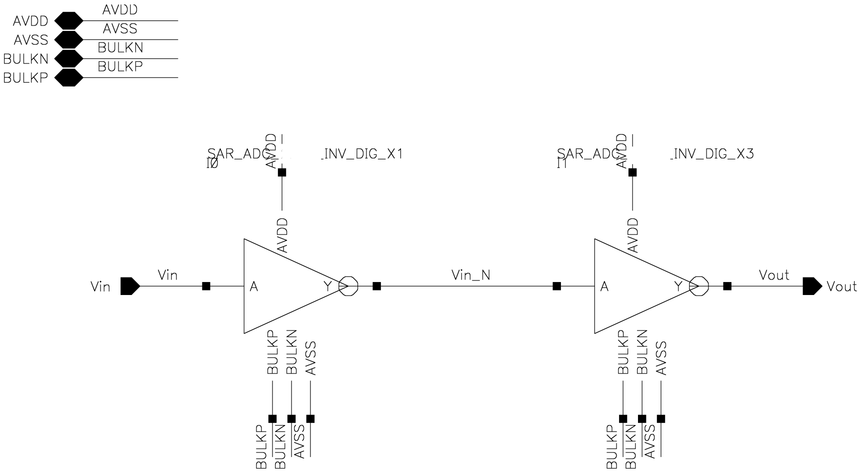
AVDD
AVSS
BULKN
BULKP
AVDD
AVSS
BULKN
BULKP
SAR_ADC
I0
AVDD
_INV_DIG_X1
SAR_ADC
I1
AVDD
_INV_DIG_X3
AVDD
AVDD
Vin
Vin
A
Y
Vin_N
A
Y
Vout
Vout
BULKP
BULKN
AVSS
BULKP
BULKN
AVSS
BULKP
BULKN
AVSS
BULKP
BULKN
AVSS

Figure A.10: Schematic of digital buffer.

Appendix B

Layout

This appendix will show selected layouts part of the SAR ADC. Only the main subblocks designed will be shown. Smaller standardized circuits (such as digital ports or unit transistors layouts) will not be shown. The entire layout of the SAR ADC without letter annotations will be presented, as well as layout of the comparator, the bootstrapped switch, the CDAC, a single bit slice and all the bit slices connected.

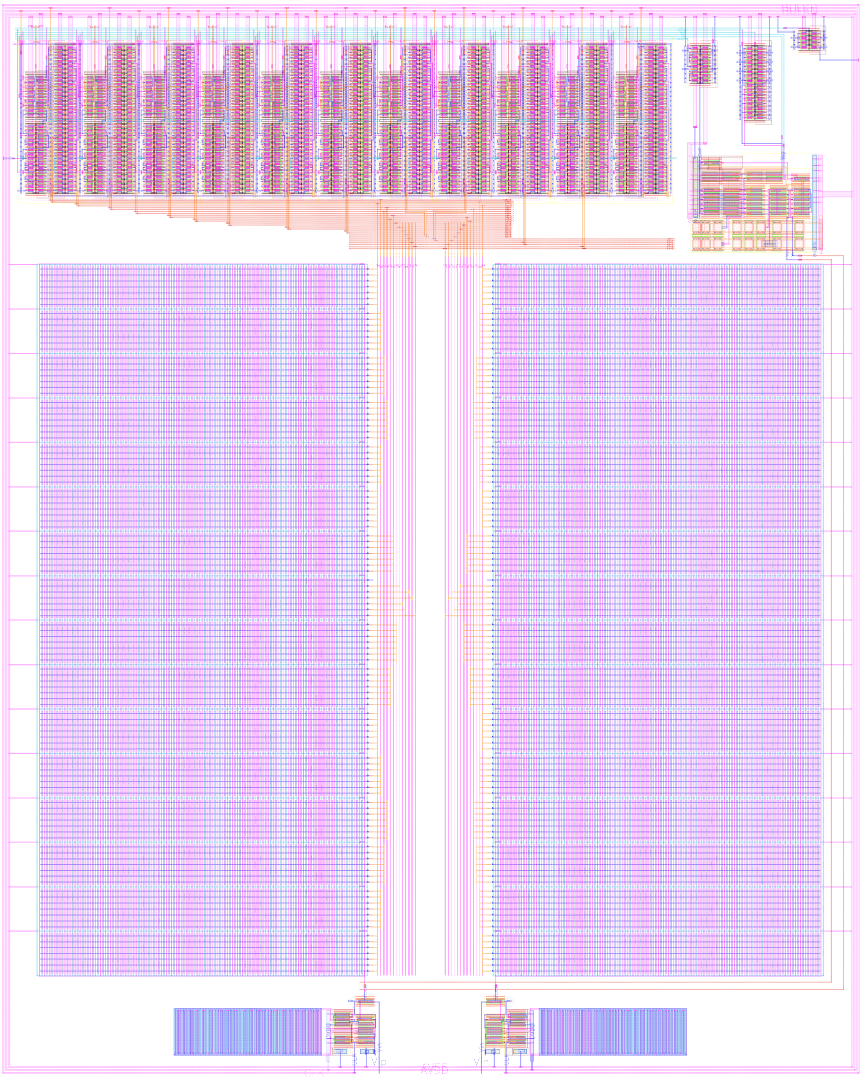
BUFKD
CLK
Vip
AVDD
Vin

Figure B.1: Top-level layout of SAR ADC.

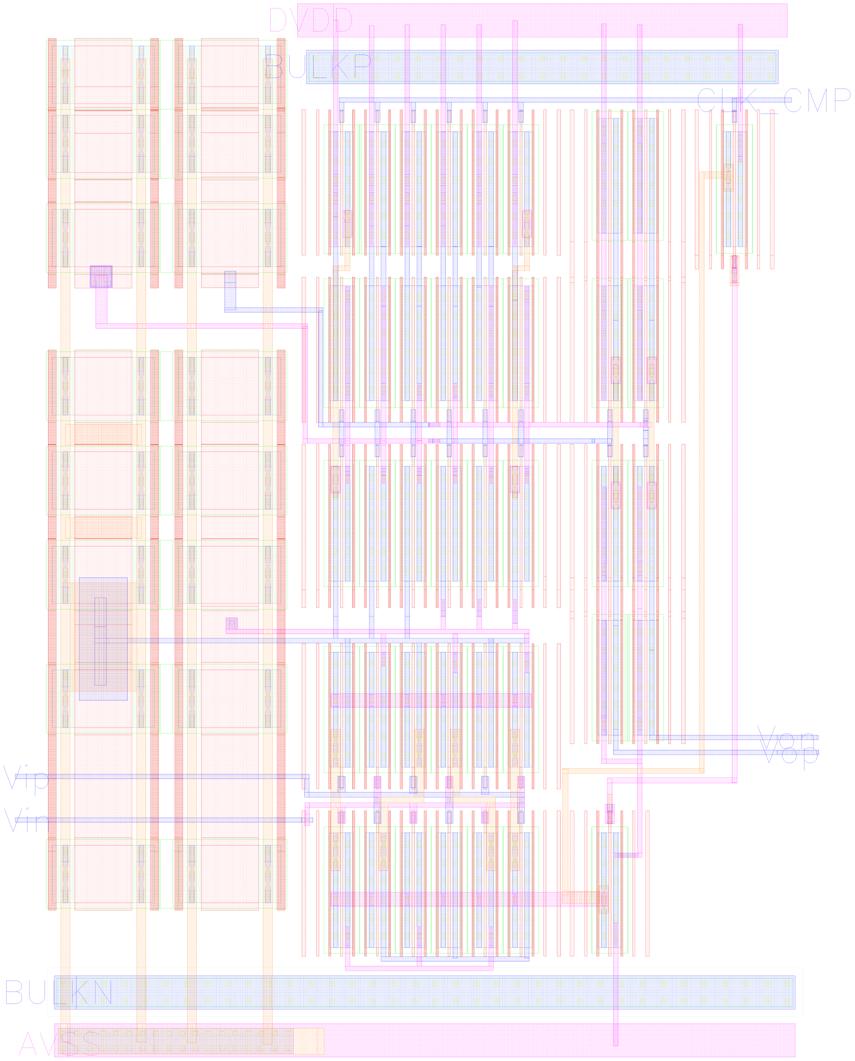
DVDD
BULKP
CLK_CMP
Von
Vop
Vip
Vin
BULKN
AVSS

Figure B.2: Layout of comparator.

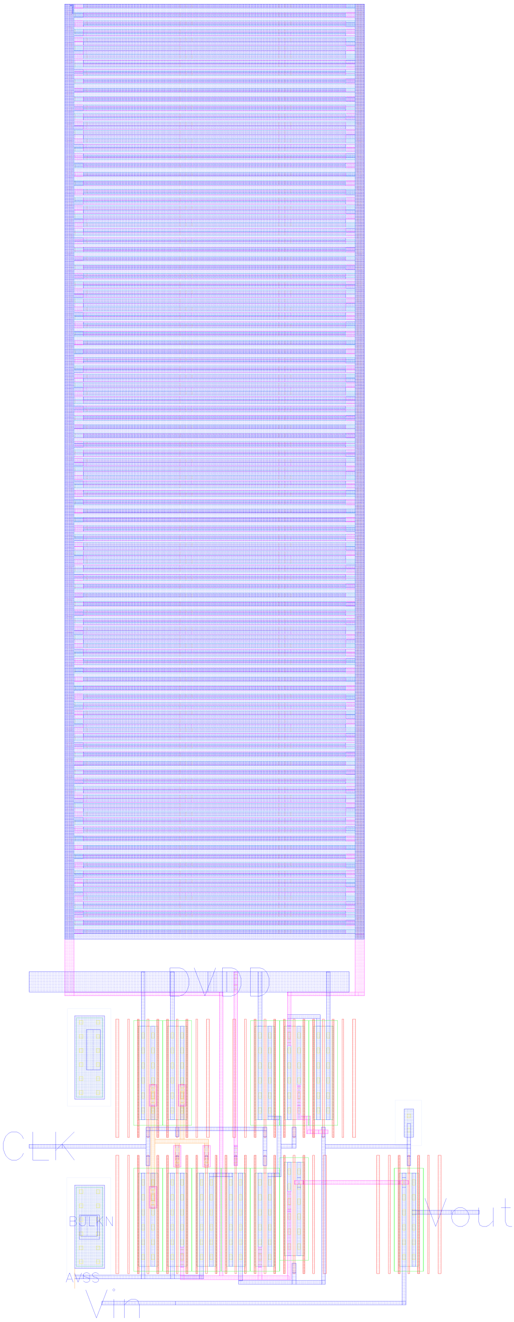
DVDD
CLK
BULKN
AVSS
Vin
Vout

Figure B.3: Layout of bootstrapped Switch.

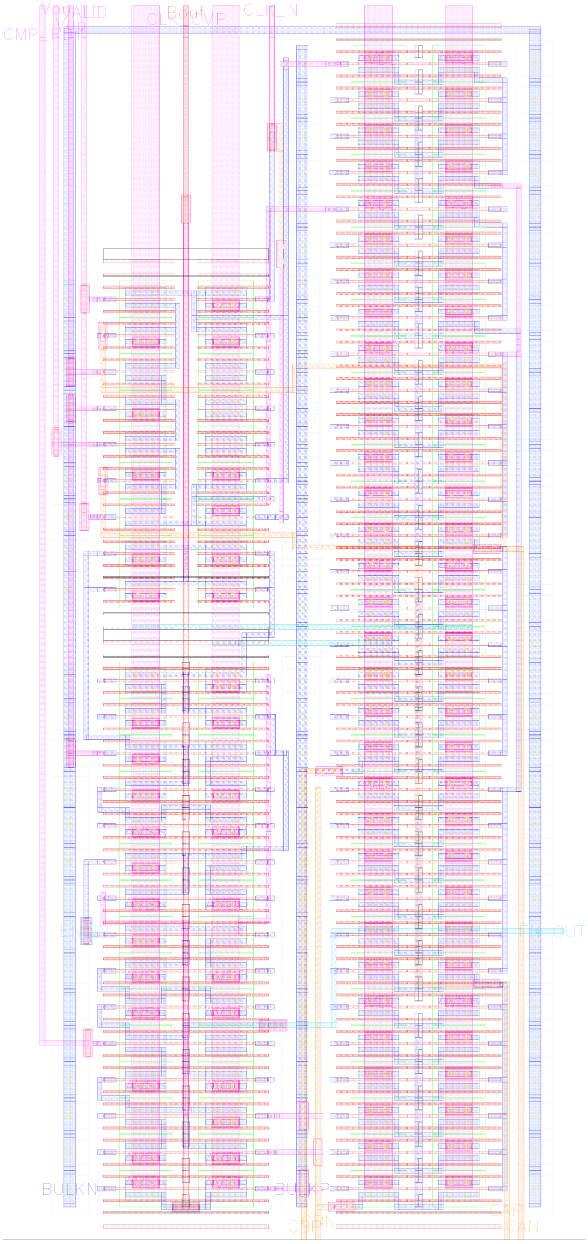
Von
VALID
Vop
CMP_RDY
CLK_CMP
Bout
CLK_N
AVDD
AVSS
EN_IN
EN_OUT
BULKN
BULKP
CBP
CBN
CAP
CAN

Figure B.4: Layout single bit slice.

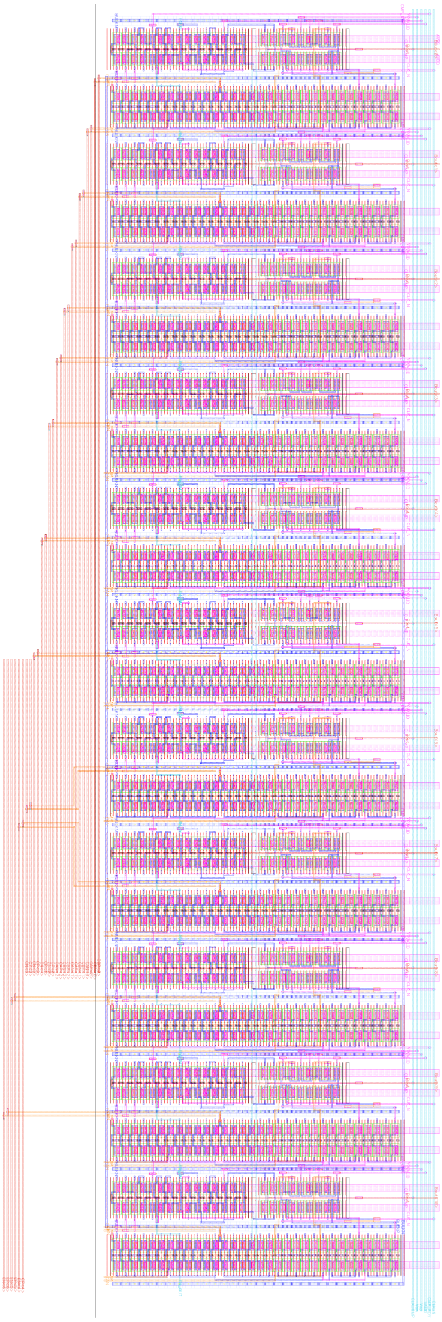

Figure B.5: Layout of all bit slices.

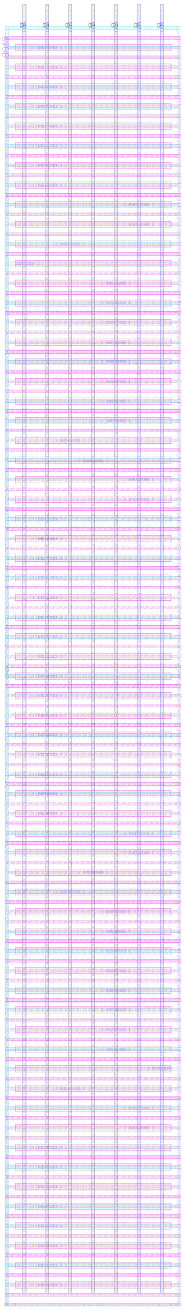

Figure B.6: Layout of CAP64.

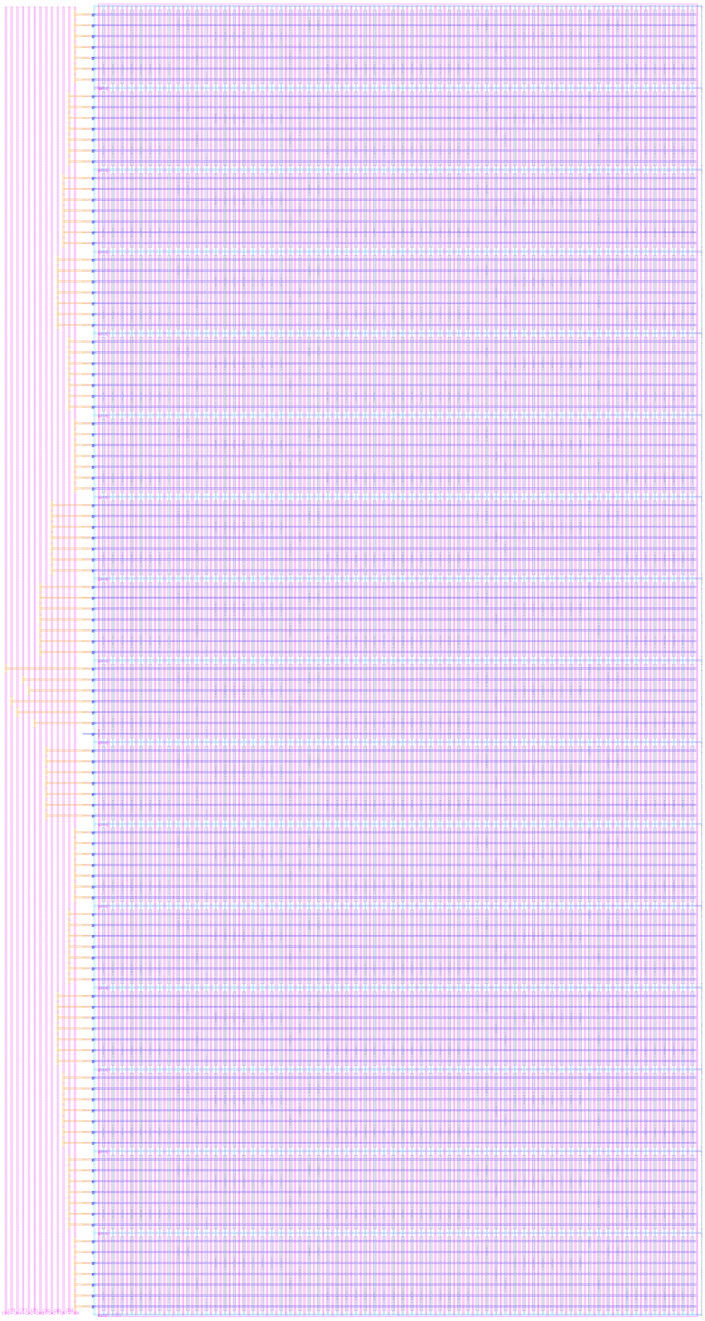

Figure B.7: Layout of CDAC.