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Battery energy storage integration via DC/AC converter in grid connected wind turbines

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Problem Description

Considering the continuously increasing power ratings of wind turbines and the introduction of more demanding grid codes for wind farm interconnection to utility, the natural intermittent of the wind resource may influence the stability of the traditional power system. Potential unbalances between the power generation and consumption can be efficiently compensated by introducing energy storage systems interconnected to the grid. In order to integrate energy storage systems into the grid, a proper power electronics interface, having an inherent bidirectional power flow capability, is required.

The scope of this project is to study the integration of battery energy storage into a 10 MW wind energy system. More specifically, the main task of the project is to investigate the performance of a selected power electronics converter both under regular operation and under various fault scenarios.

The M.Sc. thesis during spring 2018 will have a specific focus on:

- Detailed modeling of a DC/AC power electronics converter suitable to interface the energy storage to the AC grid using Matlab/Simulink. Proper control strategies will also be studied and modeled.
- Electrical performance investigation of the system under various fault scenarios and various fault locations.
- Based in the results, identify some fault handling strategies and the most critical fault

The project will be conducted in collaboration with Equinor ASA.

Preface

This master thesis is the final work of my master's degree at the Department of Electric Power Engineering at the Norwegian University of Science and Technology (NTNU). It has been written over one semester and was delivered the 4th of June 2018. The master thesis is worth 30 credits in the European Credit Transfer System (ECTS). My specialization is within electrical energy conversion and my interest within renewable generation has grown during the final years of my degree. Equinor ASA proposed the topic of both this thesis and a specialization project that was carried out during the fall 2017. The specialization project served as background knowledge when choosing battery and converter technologies to investigate in the master thesis and is a literature review of a battery energy storage system connected to the AC grid in a wind energy conversion system.

Trondheim, June 2018

Kristin Rekdal

Acknowledgment

The topic of this master thesis was proposed by Equinor ASA, hence I would like to thank my co-supervisor Dr. Eng. Kamran Sharifabadi in Equinor for proposing an interesting and relevant topic. I would also thank him for taking time to read through my thesis and always answering questions straight away. I am very grateful for the support and feedback which has been a great motivation to put down the necessary amount of work. I would also thank Antonios Antonopoulos for always welcoming me into his office. I would not have been able to understand and implement the control without him and his pedagogical abilities has been indispensable. I will also thank PhD. candidate Andreas Giannakis and Post. Doc. Gilbert Bergna Diaz for always taking the time to help me troubleshoot in Simulink and for giving me a better understanding of the simulation and control.

Most of all, I would like to thank my supervisor at NTNU, Assoc. Prof. Dimosthenis Peftitsis for constructive feedback, always being available and providing great assistance with guiding the direction of the thesis.

K.R.

Abstract

The growing need of battery energy storage to support the increase in renewable production in the electricity mix has brought the attention to the modular multilevel converter (MMC) for medium voltage applications. Modular multilevel converters have been verified as most promising battery interface as it has very high efficiency, excellent AC waveforms, scalable and modular structure and it allows for the use of low rating semiconductors. In addition it provides redundancy due to the ability of distributing the batteries into each submodule. A drawback with the MMC, is that when half-bridge submodules are used, the converter cannot handle DC faults, hence it is necessary to understand the dynamics of the converter during various fault scenarios.

In this thesis, a MMC interfacing a 1 MW battery to the grid is built in *Matwork's Matlab/Simulink*. Both the converter and control system are evaluated and designed to evaluate post-fault currents and voltages. The converter was designed with a DC voltage of 15 kV and five submodules in each arm. The degree of complexity chosen for this model is the submodule level switched model type, including IGBT, reverse diodes and SM capacitors. A high carrier frequency and phase-shifted pulse-width modulation eliminate the need of submodule energy balancing. Five short circuit fault locations have been investigated, two inside the submodule, over one arm, on the DC link and between two phases on the AC side of the converter. No fault handling strategies, AC or DC breakers are implemented in the model.

The simulation of short circuit faults inside the submodules reviled that five submodules are not enough to ensure redundancy. The importance of developing fast responding DC breakers was demonstrated as the upper converter arm on phase a was short-circuited. As this fault only includes one phase, the first post fault zero-crossing appears too late to prevent damage on the converter. DC breakers are also necessary to prevent the extremely high discharge current from the battery to the fault during the short circuit fault on the DC link. During the short circuit fault between two phases, all semiconductors will be damaged by the large current if no fault handling is applied, but on the other hand the zero-crossing appears fast enough to isolate the converter from the grid before the damage is done.

The most critical faults are the short circuit faults across one arm and across the DC link because they both requires DC circuit breakers, which is not yet commercialized.

Sammendrag

Det økende behovet for batteribasert energilagring som støtte for den økende mengden fornybar produksjon i elektrisitetsmiksen, har rettet oppmerksomhet på Modular Multilevel Converter (MMC) for medium spenningsnivå. MMC er den mest lovende omformerteknologien for batterier knyttet til AC-nettet fordi den har høy effektivitet, lav harmonisk forvrengning, er skalerbar og modulær, samt tillater bruk av halvledere med lav dimensjonering. Den modulære strukturen gjør at batteriene kan fordeles utover i omformerstrukturen. En ulempe med denne omformeren er at hvis submodulene er half-bridge, så tolerer ikke omformeren feil på DC-terminalene. Det er derfor viktig å undersøke hvordan omformeren oppfører seg under ulike feil.

Denne hovedoppgaven tar for seg en MMC som bindeledd mellom et 1 MW batteri og AC-nettet i nett-tilkoblede vindturbiner. Både omformer og reguleringssystemer er evaluert og designet med tanke på å analysere feilstrømmer og feilspenninger. Omformeren er designet med en DC-spenning på 15 kV og har fem submoduler i hver arm. En detaljert modell med IGBT, dioder og kondensatorer er implementert. Høy omkoblingsfrekvens samt faseforskjøvet pulse-width modulation gjør at algoritmer for balansering av submodulenergi er overflødig. Kortslutning på fem ulike steder er analyser. Av disse stedene er to inne i en submodul, en over én arm, en på DC-terminalene og en mellom to faser på AC-terminalen.

Fra simuleringene ble det klart at den designede MMC-en ikke har overflødige submoduler ettersom at hvis en submodul kortsluttes, kan det være skadelig for omformeren å fortsette operasjonen. Viktigheten av å utvikle DC-brytere ble også demonstrert da kortslutning over én arm førte til høye feilstrømmer før en eventuell AC-bryter fikk mulighet til å bryte strømmene. Også for feil på DC-terminalene oppsto det et behov for DC-brytere for å beskytte batteriet mot høye utladningsstrømmer. For en kortslutning mellom to faser på AC-terminalene, er AC-brytere tilstrekkelig for å forhindre at de potensielt høye feilstrømmene gjør skade i omformeren.

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Acronyms

AC Alternating Current

BESS Battery Energy Storage System

BMS Battery Management System

CCSC Circulating Current Suppression Control

DC Direct Current

DoD Depth of Discharge

EMI Electromagnetic Interference

FRT Fault-ride through

HB Half-bridge

HV High Voltage

IGBT Insulated Gate Bipolar Transistor

IGCT Integrated Gate-commutated Thyristor

MMC Modular Multilevel Converter

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MV Medium Voltage

PCC Point of Common Coupling

PD Phase-disposition

PLL Phase-Locked Loop

PMW Pulse Width Modulation

SLS Submodule-level Switched

SM Submodule

SOC State of Charge

THD Total Harmonic Distortion

VSC/I Voltage Source Converter/Inverter

VRS Variable Renewable Sources

VRT Voltage Ride Through

WECS Wind Energy Conversion System

Nomenclature

ω_0	Grid angular frequency
ω_s	Fundamental frequency
ϕ	Phase shift between the output voltage and the output current
ϕ_h	Phase shift angle of the hth harmonic
θ	dq-transformation angle
C_{sm}	SM capacitance
$f_{carrier}$	Carrier frequency
h	Harmonic component
i_c	Circulating current
i_s	Output AC current
I_{arm}	Arm current
$i_{c,dc}$	DC component of the circulating current
$i_{u,l}$	Current through the upper and lower arm
K_i	Integer gain of PI-controllers
K_p	Proportional gain of PI-controllers
L_s	System inductance
L_{arm}	Arm inductance

m_a Modulation index

N Number of SMs

n Modulation index

R_s System resistance

R_{arm} Arm resistance

R_{fault} Fault resistance

T_i Time constant of the PI-controller

T_{delay} PWM time delay

T_{sys} Time constant of the MCC converter

v_c Voltage across the passive components in each arm

v_g Voltage on the grid side of the filter

v_s Voltage at the converter output terminals

V_{block} Blocking voltage of the chosen IGBT

V_{dc} Common DC link voltage

$v_{u,l}$ Upper and lower arm voltages

$W^{\Sigma}_{cu,l}$ Stored energy in the upper and lower arms

C_{arm} Arm capacitance

E_{Cmax} The maximum energy stored in the capacitors

M Number of phases

$v^i_{cu,l}$ Capacitors voltage of each SM

Chapter 1

Background and motivation

This chapter will introduce the global context of this master's thesis. The topics introduced are meant to give an insight in the motivation and background of this work. A specialization project was carried out during fall 2017 to provide background knowledge and understanding of the subject investigated. The specialization project included a comprehensive literature review on the following topics:

- The state-of-the-art power electronics interfaces employed in wind turbine systems, with particular focus on emerging medium voltage (MV) solutions
- The battery storage technologies used for wind turbine applications
- Challenges and operating principles and performance of power electronic converters used to interface energy storage systems to an AC grid
- Potential fault locations in the system and identify the most critical fault

In the specialization project, a system for further investigation was proposed. This system will be described in chapter 2.

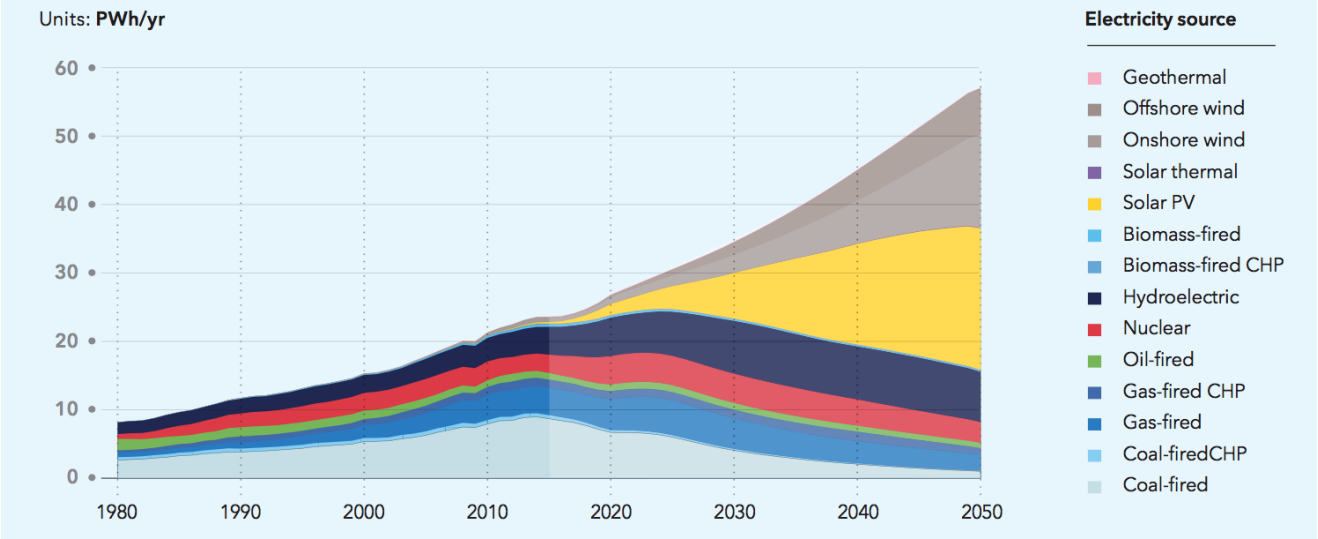


Figure 1.1: World electricity generation by power station type [7]

1.1 Integration of renewable energy

The share of renewable power generation must increase in order to reach the goal of having a low carbon society achievable. As a result of decreasing costs and political incentives, the power system is experiencing a rapid growth of renewable power generation [1–3]. Renewable sources as wind, solar, waves and geothermal energy are emitting less greenhouse gasses and toxic components, as well as not being scarce resources [4–6]. Among the mentioned renewable sources, wind has proven to be one of the most economical ways of producing electric power [4, 5]. As seen in Figure 1.1, wind generation is expected to grow to approximately 20 PWh/year by 2050, according to DNV GL's recent report on the energy transition [7]. In 2016, onshore wind energy generation could compete with conventional energy generation on costs [1].

The technologies used in wind power applications are changing as the wind turbines and parks are getting bigger. The industry has moved from fixed speed wind turbine systems to the increasingly popular fully-rated converter-based wind turbine systems with permanent magnets [8]. The latter provides full speed control, as well as decoupling between the generator and grid frequencies, which means that both the generator and grid are protected against faults from the opposite side of the converter. These advantages come at a cost of higher losses and complexity [9, Chap.6]. Trends indicate higher levels of digitization and control to increase the total efficiency. The average size of turbines was 7.7 MW in the second part of 2016, while offshore grid connected 8 MW turbines were installed by the end of 2016 [1]. By 2020 the wind turbines will reach 15-20 MW and

have diameters up to 200 m and be 250 m tall [8]. The costs of offshore wind will also experience a continued dramatic cost reduction [7].

1.1.1 Challenges

The amount of produced wind energy is dependent on wind speed [1], hence it is intermittent by nature. High shares of wind generation in weak grids leads to an increase in disturbances and unbalance [10]. Conventional power plants can support the grid stability by providing inertia response, active- and reactive power control, oscillation damping, short circuit capability and voltage back-up during faults [11], which until now have been impossible to achieve with variable renewable sources (VRS). As the installations of grid connected wind turbines have increased rapidly during the recent years, so has the penetration of wind energy in the electrical energy mix [8, 11], rising challenges concerning stability and power quality.

1.1.2 Grid code requirements

Due to the stability problems caused by the increasing amount of wind power generation, grid codes are constantly being updated by transmission system operators (TSO) [11]. Today, wind turbines must be able to control frequency and voltage range, active- and reactive power and power quality during normal operation [12]. The mentioned requirements can be achieved using power electronic converters.

Wind turbines are also required to stay connected through fault currents for a certain time [13]. This ability is called fault-ride through (FRT) and is an important concern for power electronic manufacturers. The wind turbine must be able to operate during abnormal grid conditions [14, Chap.13].

1.2 Energy storage

As mentioned, wind turbines haven't had the ability to ensure reliable supply and obtain an acceptable power quality and efficiency [6, 15, 16], hence plants driven by fossil fuels have tradition-

Name	Description	Technology	Energy (MW x h)	Location
Battery Energy Storage System (BESS)	Improve reliability if GVEA Services	Nickel cadmium (NiCd)	27x0.25 or 46x0.08	Alaska, USA
Rokkasho Village Wind Farm	Load leveling and spinning reserve	Sodium sulfur (NaS)	34x7 6	Aomori, Japan
National Wind and Solar Energy Storage and transm. Demonstration project (1-5)	Electric power interactive management	1-3) Lithium Iron Phosphate, 4) Lithium-ion, 5) Vanadium Redox Flow	1) 6x6, 2) 4x4, 3) 1x2, 4) 3x3, 5) 2x4	Hebei, China
Notrees Wind Energy Storage Project	Energy Delivery optimization	Advanced Lead Acid	36x0.67	Texas, USA
EKZ Zurich 1 MW BESS	Frequency Control, peak shaving	Lithium-ion	1x0.5	Zurich, Switcherland
Younicos and Vattenfall Project	Fluctuation balancing	Lithium-ion, Sodium sulfur (NaS)	1.2x06.2	Berlin, Germany
Orkney Storage Park Project	Renewable power stabilization	Lithium-ion	2x0.25	Kirkwall Orkney, UK
Auwahi Wind Farm	Wind ramp management	Lithium-ion	11x0.4	Hawai, USA

Table 1.1: Worldwide Battery Energy Storage System Installations [21]

ally been used for ancillary services [15]. The U.S. Department of Energy (DoE) claims that 17 MW of spinning reserves must be added to the grid, to support one gigawatt of wind capacity [17]. As available energy is crucial to obtain the grid code requirements, energy storage systems are recognized as an important solution for integration of high amounts of VRS into the power system [16, 18, 19].

Batteries can be implemented in wind farms to increase the value of the wind power output, i.e. reduce the total generation costs [16, 19]. If battery energy storage is located near the wind production site, the production can be smoothed before fed into the grid. If the battery energy capacity is sufficiently large, production can be saved for later periods [15]. To enable high penetrations of renewable energy, batteries can contribute to obtain system flexibility. The storage unit can provide ancillary service, maintain power quality, improve efficiency, make more efficient use of the power network and reduce the risk of power blackouts [20]. According to the Energy Storage Association, battery energy storage systems (BESS) can provide a 10x faster and more accurate response than power turbine generators, and can therefore operate on the competitive ancillary service market [19]. Some worldwide large energy storage projects are listed in Table 1.1.

Chapter 2

Case Description

The main objective of this thesis is to investigate the power electronic solution connecting a wind turbine and an energy storage unit. A system was proposed in the specialization project based on a literature survey of wind energy conversion systems, battery technologies, converter technologies and faults. The system proposed will be presented in this chapter along with the objective and structure of this thesis.

2.1 System description

The system investigated consists of a 10 MW wind turbine with an attached 1 MW energy storage unit. The focus will be on the power electronic interfacing the battery to an AC grid at the point of common coupling (PCC). As it is increasingly popular, the fully rated converter based topology is chosen for the wind energy conversion system (WECS). The converter is a back-to-back voltage-source converter (VSC), and in order to simplify the model of the WECS, a two-level full-bridge converter is chosen because the WECS is not the main topic of investigation. The converter is MV rated, which is defined as 1-33 kV AC [8]. The wind turbine is connected to a 33 kV grid through a filter and a line frequency transformer. The system data presented in Figure 2.1 is summarized in Table 2.1.

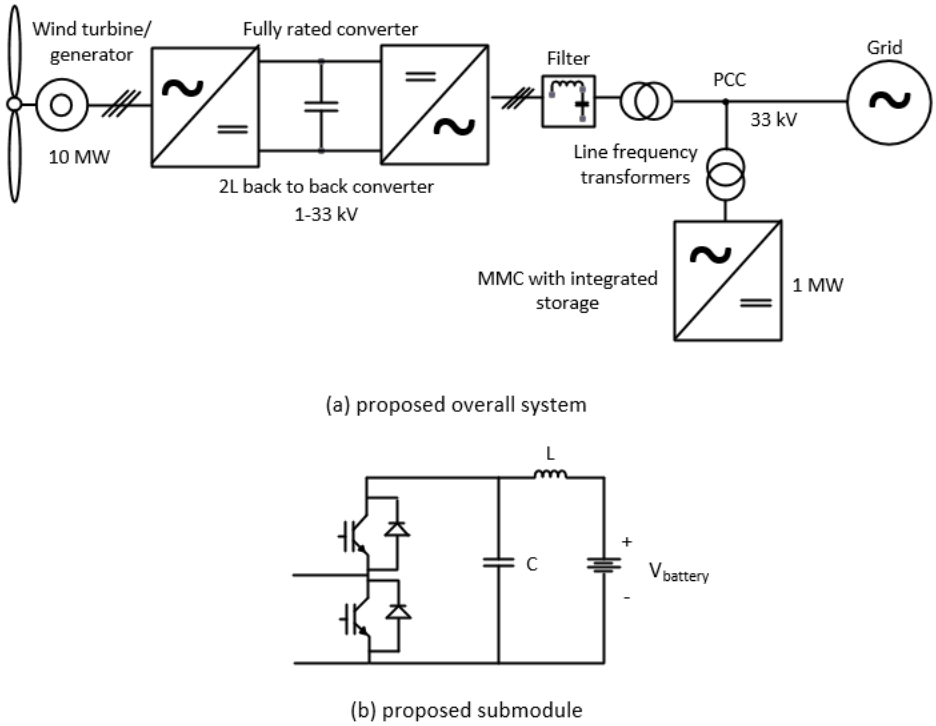


Figure 2.1: System investigated during this master's thesis

Parameter	**Abbreviation**	**Value**
Battery power rating	P_n	1 MW
Grid voltage (phase, peak)	V_g	33 kV
Number of phases	M	3

Table 2.1: Initial System Parameters

2.1.1 Lithium-ion battery

Battery energy storage technologies have been verified as the best choice for dealing with the intermittent nature of renewable sources. In the specialization project, several battery types were reviewed in therms of power capability, energy storage capacity, response time, calendar and cycle life, depth of discharge (DoD), efficiency, self-discharge, energy density and costs. Among the electrochemical batteries compared, lithium-ion, sodium (NaS) and lead-acid batteries were the strongest candidates for wind power applications. Lead-acid batteries are cheaper than NaS and lithum-ion, but also have a smaller range of application, lower cycle life and lower energy efficiency [16]. NaS is cheaper than lithium-ion, however the lithium-ion have the best properties, which is why it was chosen as the technology for this thesis. In Table 1.1, worldwide battery energy storage system examples were listed, and it can be noted that several wind connected energy storage projects include lithium-ion batteries.

2.1.2 Modular multilevel converter with integrated energy storage

As the modular multilevel converter has been verified the most promising converter for BESS [22], it was suggested as the battery power electronic interface. The MMC has several advantages over the two- and three-level converters, as high efficiency, excellent AC waveform, modular and scalable structure, low electromagnetic interference (EMI) and use of semiconductors with low voltage rating [23–26]. In order to achieve redundancy for the storage unit, the battery is split in to several units and placed inside each of the MMC's submodules (SM). A disadvantage related to the MMC, is a large amount of switches, which is considered the most expensive component in power electronics.

2.1.3 The choice of submodule

As demonstrated in Figure 2.1, the SM proposed for this MMC is a half-bridge topology because of the low losses, high reliability and simple control. Each submodule must include filters to protect the battery against AC current components, as they will reduce the lifetime of the battery [27]. The filter can be replaced by a DC-DC converter, as discussed in the specialization project. The

battery-SM interconnection will be discussed later on in the thesis. The main drawback with the MMC with half bridge SMs, is that it cannot handle DC-faults, hence the MMC must be isolated from the AC grid until the fault is cleared to protect the converter valves. On the other hand, it is the simplest of the SM topologies investigated in the specialization project, which simplifies the modulation and control, and increase the efficiency of the converter.

2.2 Objectives

The previous sections have provided insight in problems related to the increased amount of renewable, intermittent sources and a description of the proposed solution. This section will present the objectives of this master thesis. As faults can cause damage on converter components and result in long down-times, fault scenarios should be investigated for a MMC designed for this specific application. The main objectives are listed below.

- A detailed model of the proposed DC/AC MMC suitable to interface the energy storage to the AC grid will be build using Matlab/Simulink. Proper control strategies will also be studied and modeled
- The electrical performance will be investigated under various fault scenarios and locations
- Based on the results, several fault handling strategies will be suggested

Thus, a detailed model of a 1 MW MMC with battery energy storage will be implemented in order to apply several faults and investigate the electrical performance. The redundancy and DC-fault capability is especially interesting for the proposed MMC. Critical components will be identified and fault handling strategies suggested in terms of limiting the damage of the converter and battery units.

2.3 Structure of the Report

The remaining part of the master thesis will be separated into six different chapters. First, Chapter 3 will introduce the theory of the MMC including topology, operation, design considerations and

faults. The theory will be further explained in Chapter 4 where several relevant control systems will be reviewed. Only those that are considered in this thesis will be included. In both Chapter 3 and 4, a general MMC without BESS is considered.

The MMC investigated will be designed in Chapter 5, which also includes the tuning and implementation of the controllers, grid and filters. In the end, all parameters used in the simulation, are summarized in a table. All assumptions and simplification made in order to build a simulation model is also given in this chapter. Chapter 6 includes the results from the simulations of a reference case and five different faults. These results are discussed in Chapter 7 with a focus on critical components and fault handling strategies. Conclusion and summary can be found on Chapter 8.

2.4 Implementation and limitations

A detailed MMC model has been implemented in *Matwork's Matlab/Simulink*. Simulink is not able to model the component failure resulting from high over-currents or over-voltages, thus this must be analyzed and identified manually. Several simplifications must be done to satisfy the time constraint of this thesis, resulting in a detailed model of the converter and SMs and a less detailed model of the energy storage units and wind energy conversion system.

Chapter 3

Modular Multilevel Converter

The modular multilevel converter has rapidly been established as the dominant choice of topology for high voltage DC (HVDC) applications [28]. The main reason for its increasing popularity, is that conventional semiconductors with low ratings can be used within each submodule to achieve high blocking voltage suitable for HV applications [28, 29]. It also provides scalability in terms of voltage and excellent harmonic performance. Other advantages over the more conventional multilevel converters are redundancy, reliability, better state of charge (SOC) control of the battery, simple and robust structure, non or small filter requirements, low electromagnetic interference (EMI) due to smaller current loops, transformerless operation and reduced manufacturing costs due to the modular structure [23–26]. The MMC topology is very promising for large-scale BESS and it supports both centralized batteries on the common DC link and distributed batteries in each submodule [22, 30].

3.1 Topology and basic operation

A MMC consists of six converter arms (two on each phase) where each arm consists of series connected, identical submodules with an individual DC capacitor [31]. The upper and lower arm are denoted u and l respectively, while the number of submodules is denoted N. Figure 3.1 demonstrates one converter leg and the generated output AC signal. The topology differs from the cascaded multilevel converter because it includes a common DC link, hence it can be interconnected

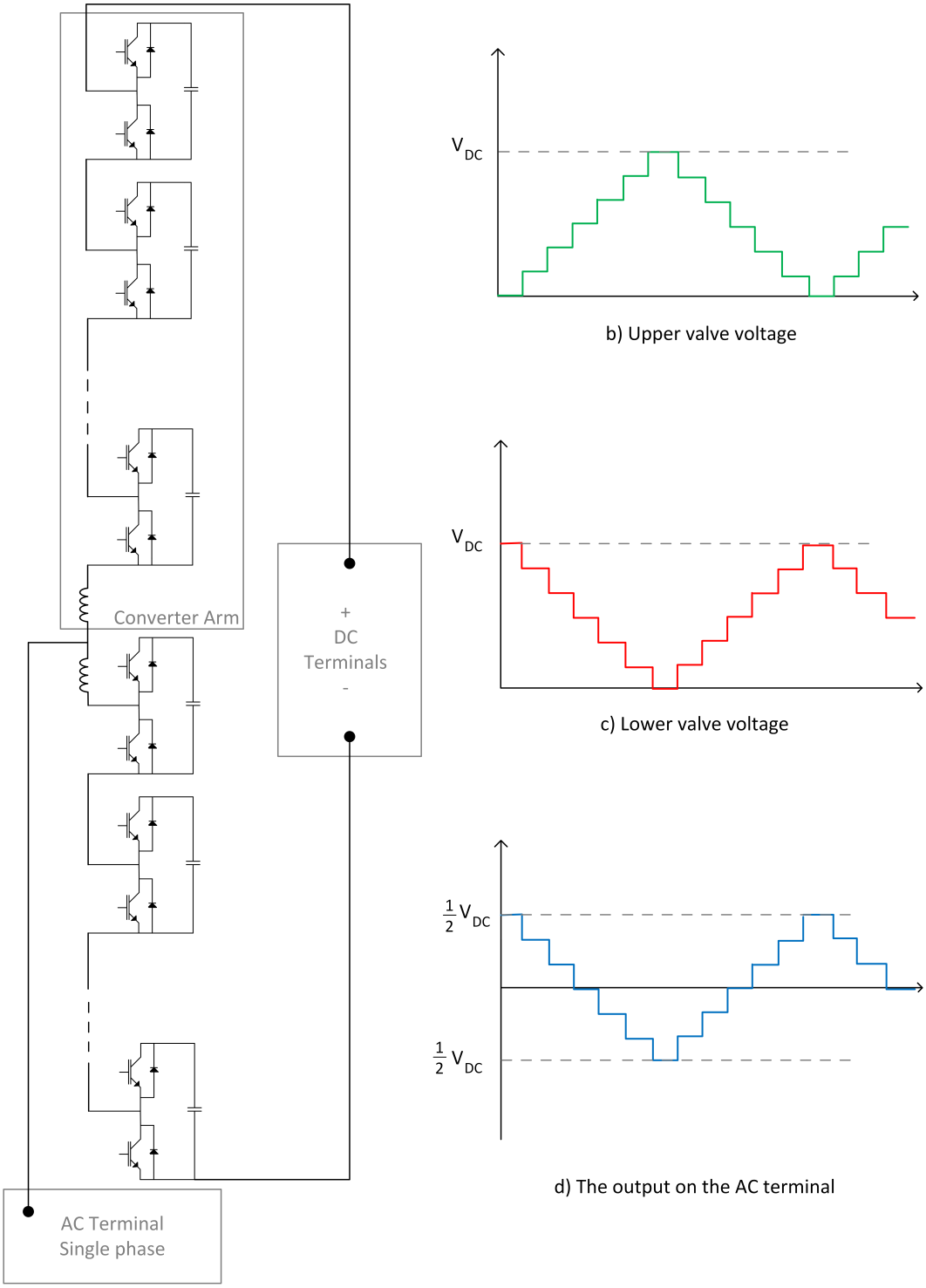


Figure 3.1: Schematic diagram of the MMC topology and output voltage of one converter leg

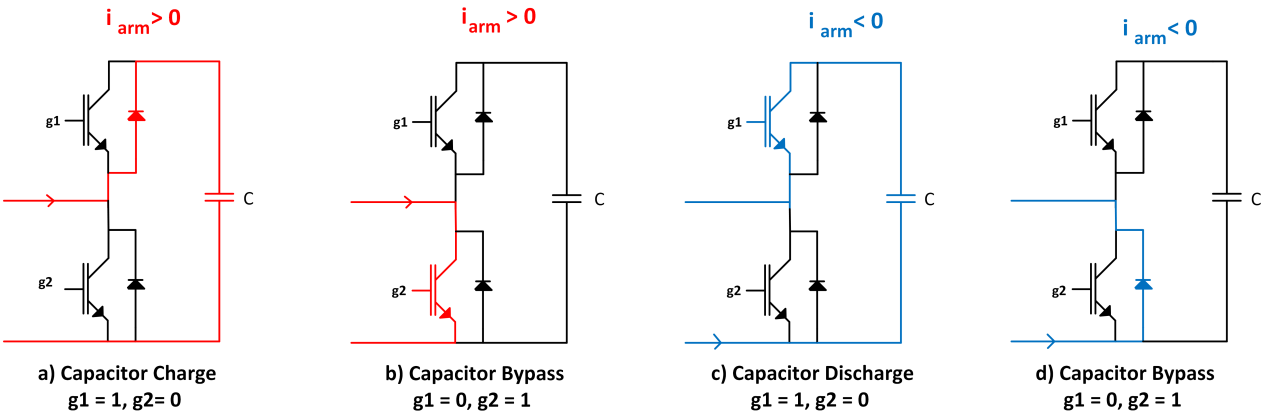


Figure 3.2: Operating states and arm current direction in a half-bridge submodule

with a DC grid [32]. Each arm also includes an inductor to prevent the potentially high transient currents that could occur between phase legs because of uneven DC and AC current distribution, circulating current control, limiting of the di/dt and protection of semiconductors in case of DC-faults [33, Chap.1]. It will also allow for the parallel connection between the DC bus and the AC side of the converter.

The most discussed submodule in the literature is the half-bridge submodule, which also is the submodule investigated in this thesis. The half-bridge submodules have two operating states: the series state and the bypass state. In the series state, the capacitor is either charged or discharged, dependent on the direction of the arm current. In bypass state the capacitor is bypassed, so that no contribution is done to capacitor state of charge [25, 26]. The two semiconductors in each submodule determine which of the two operating states the submodule will operate in. Figure 3.2 shows the four possible combinations of current directions and operating states. If the two transistors are turned off at the same time, the SM is in blocked state, hence no current will flow through the transistors.

The resulting AC output of each converter leg is the difference between the lower and upper arm voltage. The more SMs per arm, the better AC waveforms at the output [34]. The voltage of each arm is the sum of the voltages over all the submodules in that particular arm, which is dependent on the state of each submodule. The output AC voltage can potentially be set to any value between the DC rails [33, Chap.1]. As a result, the converter acts like a controllable voltage source seen from both the AC and DC side, which is a feature the two-level and conventional multilevel converters discussed in the specialization project lacks. The result is that with any number of submodules,

both the DC and AC voltage can be very precisely controlled [33, Chap.1].

3.1.1 Circulating currents

It is important to consider the circulating currents in the MMC as it contributes to a strong 2nd order harmonic ripple which increases the rms-value of the arm currents, resulting in higher losses and component ratings. The circulating currents will try to oppose the unbalances within the converter, as sum-capacitor voltages different to the DC-link voltage and unbalance between the two arms in the same phase leg [35]. The circulating current in the converter arms contains a DC component together with even-order harmonics [36], as described by

$$i_c = I_{c,dc} + \sum_{h=1}^{\infty} I_{c,h} sin(h\omega t - \phi_h) \tag{3.1}$$

where $I_{c,dc} = I_{dc}/3$ is the DC component, $I_{c,h}$ the the amplitudes of the harmonic components and ϕ_h is the phase shift angle of the h^{th} harmonic. Not that $I_{c,h} = 0$ when h = 2n-1. It is desired that the circulating current should be kept small and a pure DC component [33, Chap.3]. If the circulating current is zero, there can be no active power transfer to and from the input and output sides of the converter [35]. If a 2nd order component is injected to the arm voltages, the strong 2nd order harmonic in the circulating current can be reduced, as suggested in [34]. Replacing the arm inductance with an LCL-filter tuned at the 2nd order harmonic has also been mentioned as a possible solution. The downside of this is an increase in converter size and cost.

3.2 Design considerations

Several design choices for the main circuit of the MMC must be considered. Power semiconductor ratings, submodule capacitance (C_{sm}), arm inductors (L_{arm}), number of submodules (N), submodule design, redundant submodules, auxiliary power supplies and start-up procedures [33, Chap.2]. This thesis is considering a 1 MW rated converter with half-bridge SMs connected to a 33 kV AC grid, hence the power and output voltage is for this converter is known. When the semiconductors are chosen and the blocking voltage, V_{block} is known, the number of SM can be

calculated using

$$N = \frac{V_{dc}}{(2/3)V_{block}} \tag{3.2}$$

where 2/3 is the safety margin of the power semiconductor and V_{dc} is the DC voltage that the submodules must withstand.

The SM capacitance, C_{sm}, must be chosen very carefully. As the capacitors are bulky and costly, high values of the capacitance should be avoided. On the other hand, voltage ripples occur if the capacitor is too small [33, Chap.3]. The maximum energy stored in the capacitors is E_{Cmax} is determined by summarizing the total energy stored in all the SMs in all the converter arms,

$$E_{C,max} = 2MN\frac{1}{2}C_{sm}\left(\frac{V_{dc}}{N}\right)^2 \tag{3.3}$$

where M = 3 is the number of phases of the converter. Since energy is defined as power over time, the time constant can be defined as

$$t = \frac{E}{P} = \frac{E_{C,max}}{S_n} \tag{3.4}$$

and should typically be around 10 ms to 50 ms [36]. Further, the expression for energy that can be stored in the capacitors of a three phase converter with 6 arms is used to derive that C_{sm} can be calculated using

$$C_{sm} = \frac{tS_n}{MNV_{dc}^2} \tag{3.5}$$

The inductance of each arm, L_{arm}, is necessary to avoid direct parallel connection of the voltage sources implemented by the SM strings [33, Chap.1]. Their role is to avoid the high frequency of the arm currents caused by differences in the upper and lower arm voltages [36]. When the number of SMs is high, the control of the voltage over the arms can be very precise, hence the inductance generally do not need to be large. The circulating current can be suppressed using a proper selection of L_{arm} due to the avoidance of the resonance that occurs for a given C_{arm} . When

C_{sm} is know, the resonance arm inductance can be calculated using [36]

$$L_{arm,r}|_{C_{arm,r}=C_{arm}} = \frac{1}{C_{arm}\omega_s^2}\frac{2(h^2-1)+m_a^2h^2}{8h^2(h^2-1)} \tag{3.6}$$

where h is the harmonic orders and ω_s / 2π the fundamental frequency.

3.3 Modeling and dynamic equations

This section will present a mathematical representation of the MMC, which is used for the purpose of dynamic control. The equations are based on derivations in [33, Chap.3] and [35]. When referring to the AC quantities, the subscripts describing phase *a, b* and *c* are replaced by the subscript *s*. In order to simplify the analysis, some assumptions must be made. At first it can be assumed that the output voltage and current is single-frequency quantities and that the direct voltage source is constant. The voltage of the upper or lower arm can be varied between zero and the sum of all capacitor voltages in the given arm, as seen below,

$$0 \leq v_{u,l} \leq v_{cu,1}^{\Sigma} \tag{3.7}$$

This is done by bypassing and inserting a certain number of submodules. The fraction of inserted submodules is denoted n and is calculated by the number of cells inserted divided by the total number of cells in one arm, N.

$$n = \frac{inserted\ cells}{inserted\ cells} = \frac{inserted\ cells}{N} \tag{3.8}$$

which is equivalent to the duty cycle and from this point will be referred to as the modulation index. If a stable and balanced operation is assumed, it can be seen from Figure 3.3 that the voltage contribution to the upper and lower arm is

$$v_{cu}^* = V_{dc}/2 - v_s^* - v_c^* \tag{3.9a}$$

$$v_{cl}^{*} = V_{dc}/2 + v_{s}^{*} - v_{c}^{*} \tag{3.9b}$$

where v_{c}^{*} is the voltage across the passive components in each arm, L_{arm} and R_{arm}. The output and circulating current can be described as

$$i_s = i_u - i_l \tag{3.10a}$$

$$i_c = \frac{i_u + i_l}{2} \tag{3.10b}$$

In order to keep the DC-voltage constant, the DC current has to be the sum of the mean value of all the currents in the upper and lower arm in all three phases,

$$\sum_{k=1}^{3} \overline{i_{u,l}^{k}} = i_{dc} \tag{3.11}$$

This means that unless the DC-current is zero, there will be a DC component in the arm currents. Further, the string of series-connected SMs of each arm can be replaced by controllable voltage sources, hence the sum of the voltage stored in each string is given by

$$v_{cu,l}^{\Sigma} = \sum_{i=1}^{N} v_{cu,l}^{i} \tag{3.12}$$

where $v_{cu,l}^{i}$ is the individual voltage of the capacitors of each SM. Using the insertion index $n_{u,l}$, one can define the voltage across the SMs in each arm as

$$v_{cu,l} = n_{u,l} v_{cu,l}^{\Sigma} \tag{3.13}$$

Further, the equations listed above can be used to derive the dynamic equations of the MMC. The first step is to apply Kirchhoff's voltage law (KVL) on the two circuits including the upper and lower arm, in Figure 3.3. For the upper arm circuit, applying KVL gives

$$\frac{V_{dc}}{2} = v_s + n_u v_{cu}^{\Sigma} + R_{arm} i_u + L_{arm} \frac{di_u}{dt} \tag{3.14}$$

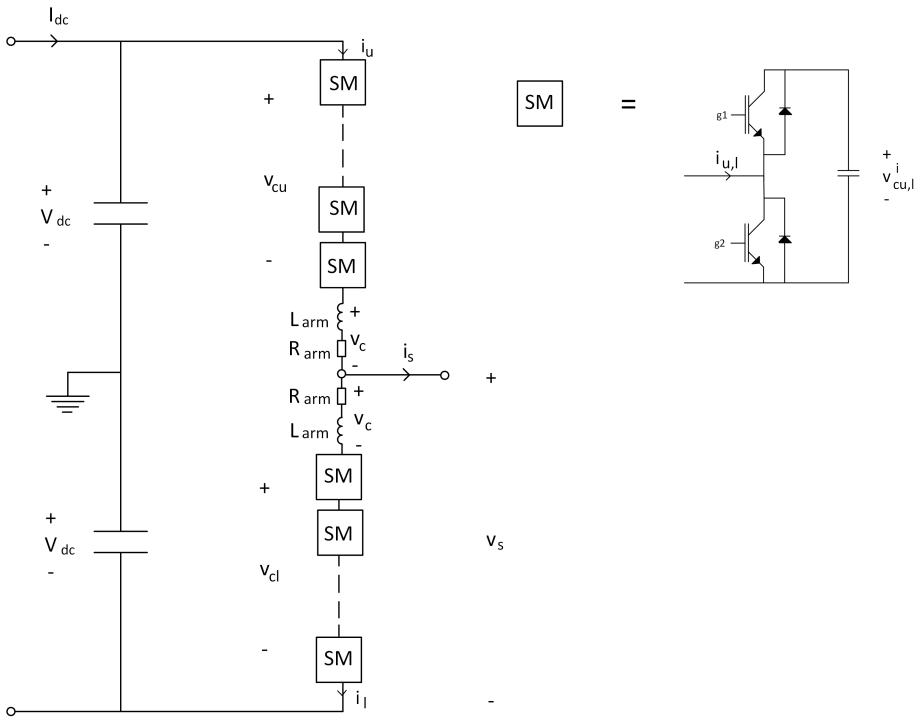


Figure 3.3: Circuit diagram and submodule of an MMC

Note that (3.13) is applied so that $n_u v_{cu}^{\Sigma}$ is included in the equation. Applying KVL and (3.13) on the lower arm circuit gives

$$\frac{V_{dc}}{2} = -v_s + n_l v_{cl}^{\Sigma} + R_{arm} i_l + L_{arm} \frac{di_l}{dt} \tag{3.15}$$

Modifying (3.14) and (3.15), the dynamic equations for the circulating current i_c and the output current i_s is obtained. The circulating current can be described by

$$L_{arm} \frac{di_c}{dt} + R_{arm} i_c = \frac{V_{dc}}{2} - \frac{1}{2}(n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}) \tag{3.16}$$

In the same way as for the circulating current, the dynamic expression of the output current is derived as

$$L_s \frac{di_s}{dt} + R_s i_s = n_l v_{cl}^{\Sigma} - n_u v_{cu}^{\Sigma} - 2V_s \tag{3.17}$$

where L_s is defined as $L_{line} + L_{arm}/2$. During an ideal situation, where the converter is able to create ideal voltage contribution for all arms, (3.16) and (3.17) can be simplified into

$$L_{arm}\frac{di_c}{dt} + R_{arm}i_c = v_c^* \tag{3.18a}$$

$$L_s\frac{di_s}{dt} + R_s i_s = v_s^* - v_s \tag{3.18b}$$

which reveal which control variables that are used to control the circulating and output current. It should also be noted that the sum of the capacitor voltages $v_{cu,l}^{\Sigma}$ is not constant, but a varying quantity. The current flowing through the arm is governing the voltage, as explained by

$$\frac{C_{sm}}{N}\frac{dv_{cu,l}^{\Sigma}}{dt} = n_{u,l}i_{u,l} \tag{3.19}$$

where C_{sm} is the capacitance inside each of the SMs. (3.19) is the upper and lower arm aggregated voltage dynamics, while (3.18a) and (3.18b) are the circulating and grid current dynamics.

3.4 MMC with integrated energy storage

Integrating the battery into the SMs means that each SM must include one storage module, which again consists of a number of storage elements [37]. The MMC topology allows batteries to be connected directly into the SMs. As the energy storage units will be injected with high AC components when connected directly to the switching module [27], one of the main aspects of integrating storage units to the SMs is the SM-battery interface solution. In the ABB Energy Storage Modules data sheet [38], it is specified that their 1 MW lithium ion battery has a 10 % AC tolerance, hence the interface must be designed accordingly. The simplest interface is a filter module, but a double stage solution including a DC/DC converter can also be implemented. This requires additional control, which increases the complexity of the system. On the other hand, the power can then be controlled independently from the MMC control system. The filter module can prevent unnecessary high losses and reduce the harmonic components of the battery current [27]. The harmonic components in the battery current should be minimized as the battery will permanently loose a

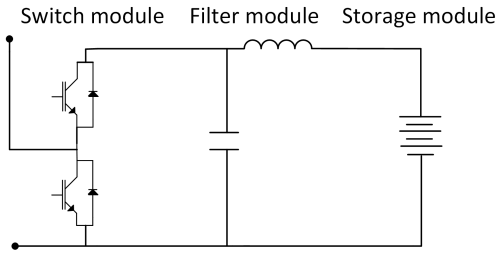


Figure 3.4: Schematic diagram of a simple submodule structure for the MMC converter with integrated storage

small amount of the active material every time the battery is charged and discharged [39], hence the battery life will decrease. A simple filter module consists of a capacitor and an inductor, as demonstrated in Figure 3.4. The converter will still have a common DC-link, hence the properties of the MMC are kept [21].

Several balancing and control methods must be applied to a MMC with integrated storage. It is very important to balance the battery units and all the units requires its own battery management system (BMS) to monitor and control state of charge (SOC) for all battery units [27]. Phase power control, branch power control and SOC balancing on all SMs are among the control strategies that must be applied [21]. The SOC control is crucial to avoid internal damage of the battery such as under- or overcharging [40]. The BMS must be implemented through the MMC's control system [27].

3.5 Faults

Faults on high power (above 1 MW) equipment have big impacts on the total system costs because the potential damage in equipment is significant, hence analyzing faults on the MMC is of great importance. Two aspect will be discussed in this section. The first is how reliable the converter is and what happens to the converter when faults occur. The second is fault locations and impact.

3.5.1 Reliability

Reliability is defined as 'probability that an item will perform a required function without failure under the stated conditions for a stated period of time' [14, Chap.1]. In wind turbines the converter

is one of the most critical assemblies in terms of lifetime and maintains cost [14, Chap.1]. Both transistors and capacitors are considered critical elements, and for MMCs with a high number of submodules, the critical element's component count is high. In the MMC it is important that the capacitors in the SMs are extremely reliable because they are used to achieve the desired arm voltage [33, Chap.2]. Higher reliability can be achieved by increasing the rating of the capacitors [41], but due to high number of capacitors required, the capacitor is a major contributor to the total cost.

To achieve higher reliability for the MMC, redundancy is introduced through a high number of SMs. In order to operate the MMC during faults in the submodules, the fault must be detected and bypassed, which can be challenging for converters with a high number of identical SMs [42], but on the other hand, bypassing a SM will then hardly have any effect the arm or leg voltage and they can both continue operation after component failure [14, Chap.12].

3.5.2 Fault locations

Generally, the fault of a MMC can be classified into AC network fault at the PCC, AC fault inside the converter station, DC faults (pole-pole or pole-ground) and converter internal faults as submodule faults and modulation and control faults. Grid unbalances are likely to affect any MMC connected to a three-phase grid. The MMC is generally robust against unbalanced AC networks and are able to fulfill the low voltage ride through requirements in the grid codes [33, Chap.9]. If a Δ - Y transformer is included in the grid connection, the zero-sequence current can be blocked, hence only the positive- and negative-sequence currents must be controlled. This is possible for a MMC with distributed capacitor energy storage because they are able to control each phase independently. Such control scheme is demonstrated in [34]. If the circulating currents are controlled properly, the MMC can also eliminate the common-mode second-order DC-link component, which is not possible using conventional three-phase converters [21].

Just like the conventional 2L- and 3L-VSCs, the MMC with half-bridge submodule topology will loose control of its currents as DC-faults occur [33, Chap.9]. If a short circuit fault occurs on the DC bus, the voltage at the DC link becomes zero, and the AC/DC submodule will act as rectifier and feed currents to the fault through the free-wheeling diodes [28, 37]. This is due to the diodes constituting an uncontrollable rectifier, hence contribute to increasing the DC side current [28].

The stored energy in the system will be released, resulting in extremely high currents [43]. This is why the DC fault is the most critical fault to the converter and battery.

There are several fault handling strategies for the HB MMC [28]. The first is to control the current supplied from the AC-side into the DC-side. One way of doing this is to change the topology of the SMs to a fault tolerant topology as full-bridge SMs. The second fault handling strategy is to use AC circuit breakers which is the most cost effective method, but one must then isolate the whole converter and there is a time delay until the AC current reaches the zero-crossing, thus the response time might be too long to prevent damage [44]. The third method often mentioned is to apply fast DC circuit breakers, which still are being developed [28, 44]. DC breakers are able to clear the fault faster, but the response time is varying in a range of microseconds to tens of milliseconds [45, 46]. The first DC circuit breaker suggested was a mechanical switch with active resonance. This DC breaker has a response time of 50-60 ms, which is equivalent with 3 fundamental periods and is considered long [47]. A faster option is a pure semiconductor switch which breaks the current in terms of μs, but which consists of several series connected semiconductors, thus have high conduction losses [45]. Several DC breaker topologies are investigated and compared in [45, 46]. The most promising DC breaker is the hybrid DC circuit breaker suggested by ABB [48].

Chapter 4

Control of the Modular Multilevel Converter

This chapter will present a review of the applied control for the MMC modeled in *Mathwork's Matlab/Simulink*. Compared to conventional power converters, the MMC is relatively complicated to control because of the complex dynamics [33, Chap.3]. Several control methods can be applied, but this chapter will only review those that are considered for this specific MMC. In this chapter it is assumed that the energy storage unit is placed at the centralized DC link.

4.1 Principle

The control system applied to the MMC can be divided into four sections, as demonstrated in Figure 4.1. The first control stage is the higher-level control which includes the phase locked-loop (PLL) used for grid synchronization, active and reactive control and DC bus voltage control [33, Chap.3]. The heart of the control system is the output current controller which has the highest bandwidth of the nested control loops. The resulting signal of the output current controller is the output voltage reference, which for 2L-VSC can be forwarded directly into the pulse-width modulator (PWM) to generate the modulation index, but since the MMC has more complex dynamics, an additional stage must be included. This stage is the arm-balancing control which includes the circulating current control and the control of the sum capacitor voltages, and produces the insertion indices which is the input of the modulation and submodule balancing stage.

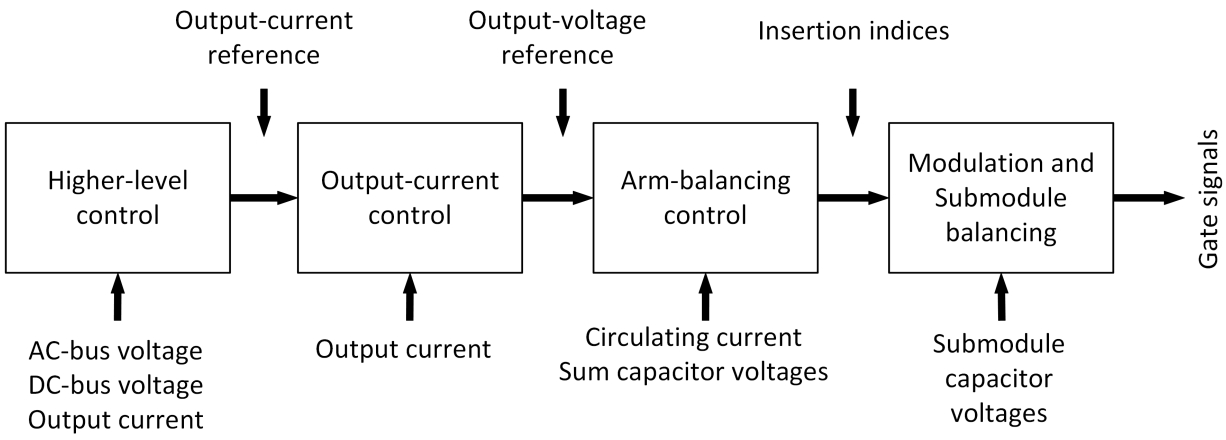


Figure 4.1: Overview of a typical MMC control system [33, Chap.3]

4.2 Modulation and submodule energy balancing

When designing the control system it is natural to start with the innermost controller, as the control system then can be tested while the outer stages are added. The modulation and submodule energy balance stage is determining the number of submodules inserted and which SMs that should be inserted in order to balance the energy of each submodule capacitor. As the number of levels improves the harmonics, the switching frequency can be lower than with the conventional converters.

4.2.1 Pulse-width Modulation

The objective of a pulse-width modulation (PWM) is to choose the instances for switching between the levels in order to produce an output AC voltage that coincides with the reference signal [33, Chap.5]. In order to describe the PWM, the amplitude-modulation index must be defined as

$$m_a = \frac{2\hat{v}_s}{V_{dc}} \tag{4.1}$$

where $\hat{v}_s$ is the amplitude of the output voltage. The modulation index is generally a value between zero and one if over-modulation is avoided. Hence, it should be noted that the amplitude of the sinusoidal voltage is restricted by the DC bus voltage, so that the maximum amplitude of the output AC voltage is half of the DC voltage. The method of modulation chosen for for this project

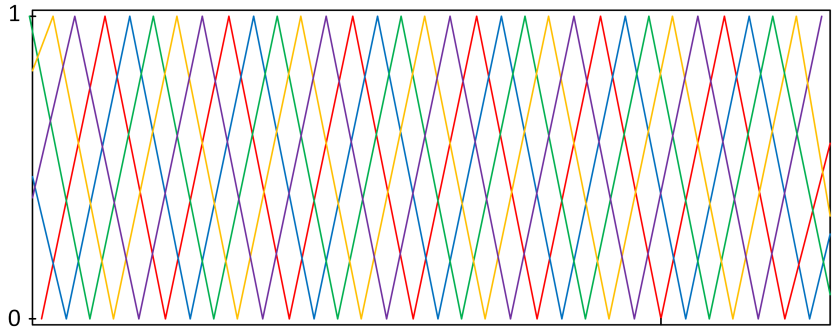


Figure 4.2: Phase-shifted carrier multilevel modulation. N = 5

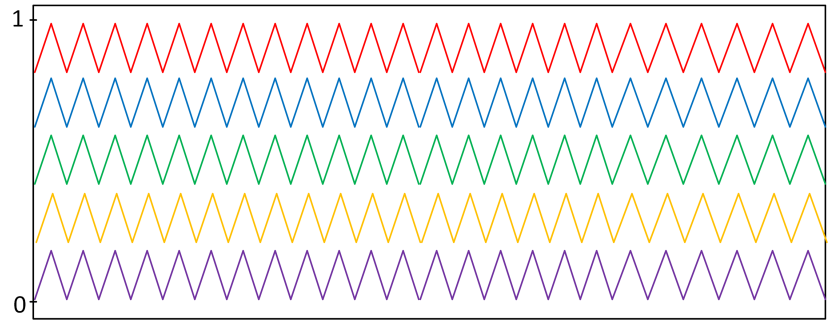


Figure 4.3: Level-shifted carrier multilevel modulation with phase disposition. N = 5

is the carrier-based method, as it can easily be adopted to multilevel converters [33, Chap.5]. The carrier-based method consists of a fundamental frequency reference signal being compared to high frequency carrier signals. It is common to use only one set of triangular carrier signals for all the three phases and compare them to three 120 degree phase shifted reference signals. The carrier signals for the upper and lower arm can be equal as well.

There are several ways of adapting the carrier signals to multilevel converters. In this section, only two methods will be reviewed. The first is the phase-shifted carriers where N identical triangular carrier signals are phase-shifted by 360/2N degrees as seen in Figure 4.2 for N=5 [42]. The insertion indices, $n_{u,l}$ are also varying between zero and one, hence the modulation will work the same way as for the 2L-VSC for each SM. At a sufficiently high switching frequency, no energy balance between the submodule capacitors is required, as the switching of the submodules are evenly distributed [42] [33, Chap.5] [49].

The level-shifted carriers with phase disposition (PD) seen in Figure 4.3, have an amplitude of 1/N, differ in offset and no phase-shift between them. The main disadvantage of using this method, is that the SM that has been assigned the lowest carrier will be turned on for a long time,

while the SM that has been assigned the upper carrier signal will only be turned on for a short period of time, hence there is an uneven distribution of both the energy stored and losses in each SM. This problem can be solved using SM energy balancing [42]. The carrier frequency should also be N times higher than with the phase-shifted carriers in order to achieve the same average frequency as with the phase-shifted carriers [33, Chap.5].

4.2.2 Submodule balance using the sorting algorithm

The energy stored in each individual SM is varying during the operation of the MMC [33, Chap.5]. The objective of the sorting algorithm is to decide which SM that should be charged and discharged in order to obtain capacitor voltages balanced at their nominal values [49]. Instead of assigning one carrier signal to each SM, the balancing method takes in the number of submodules inserted at any instant,

$$N_{u,l}^{\Sigma} = \sum_{i=1}^{N} n_{u,l}^{i}, \tag{4.2}$$

the direction of the arm current and the measured voltage of the capacitors in each SM. As the gate signals, $n_{u,l}^{i}$, are either zero or one, $N_{u,l}^{\Sigma}$ will be a staircase signal of integers between zero and N. When the arm current is positive, the inserted SMs are charging, hence the SMs with the lowest measured capacitor voltages should be inserted. In case of negative arm current, the SMs with the highest capacitor voltages should be inserted, i.e. discharged. The sorting algorithm is illustrated in Figure 4.4 [49] [33, Chap.5]. The sorting algorithm can be implemented into the modulation stage [50].

4.2.3 Direct modulation

A natural start when simulating a MMC, is to apply direct modulation to calculate the insertion indices [35]. The insertion indices can be defined as

$$n_{u,l} = \frac{1 \mp m_a cos(\omega_s t)}{2} = \frac{1 \mp 2\frac{v_s^*}{V_{dc}}}{2} \tag{4.3}$$

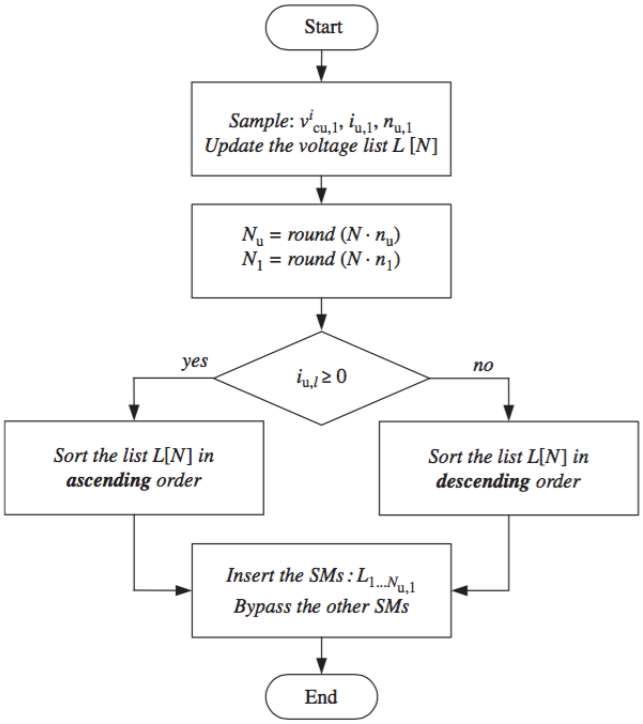


Figure 4.4: Flowchart of the conventional sorting algorithm [33, Chap.5]

With no feedback or measurements, this is a simple, robust and time efficient way of providing control of the converter, as it works without the need for measured values from the converter [31]. On the other hand, direct modulation can give rise to high circulating currents which increases the losses and required ratings of the converter [36, 42]. These circulating currents have a high 2nd-order harmonic component in steady state [35], due to the fact that this open-loop control assumes the use of the sorting algorithm in order to balance the capacitor voltages [31].

4.3 Arm-balancing control

The next step is to apply more advanced control in order to prevent unbalance between the two arms in the same phase legs, which causes a circulating current component with the fundamental frequency. The method chosen for this thesis, is a open-loop voltage control with ripple estimation based on [35, 51]. This method avoids complex systems of measurements and control, hence reduce the total system delay [51]. The alternative is a closed-loop control system which has some issues with data exchange between the controller and the modulator if the number of SMs are

high. Comparison between different arm-balancing methods have found that the open-loop control provides the fastest voltage response [31]

As already explained, the insertion indices, $n_{u,l}$, are the number submodules should be inserted. In this case, the insertion indices are defined as

$$n_{u,l} = \frac{v^*_{cu,l}}{v^{\Sigma *}_{cu,l}} \tag{4.4}$$

where $v^{\Sigma *}_{cu,l}$ is an estimate of the total capacitor voltages available and will be calculated without any need for measurements. Further [51] provides an explanation of how to generate this estimate, while [35] is providing simple step by step outline of the assumptions taken and the calculation.

The first assumption made is that the circulating current is a pure DC component, hence v^*_c can be calculated as $v^*_c = R_{arm} i^*_c$. The DC component of the circulating current is given by

$$i_{c,dc} = \frac{\hat{V}_s \hat{I}_s cos\phi}{2V_{dc}}. \tag{4.5}$$

The dynamics of the voltage stored in the capacitors of each SM can be written

$$\frac{dv^{\Sigma *}_{cu,l}}{dt} = \frac{N}{C_{sm}}\left(i^*_c \pm \frac{i_s}{2}\right)\frac{\frac{V_d}{2} \mp v^*_s - v^*_c}{v^{\Sigma *}_{cu,l}}, \tag{4.6}$$

hence the expression for the total stored energy can be calculated in an open-loop fashion,

$$\frac{dW^{\Sigma *}_{cu,l}}{dt} = \left(i^*_c \pm \frac{i_s}{2}\right)\left(\frac{V_d}{2} \mp v^*_s - v^*_c\right). \tag{4.7}$$

Assuming that the mean energy in both arms are equal, $W^{\Sigma}_{cu0} = W^{\Sigma}_{cl0}$, the expression for the estimated total energy that can be stored in the converter arms is

$$W_{cu,l}^{\Sigma *} = W_{cu,l0}^{\Sigma} \mp \frac{\hat{V}_s i_{c,dc} sin\omega_s t}{\omega_s} \pm \frac{\left(\frac{V_d}{2} - R i_{c,dc}\right)\hat{I}_s sin(\omega_s t - \phi)}{2\omega_s} - \frac{\hat{V}_s \hat{I}_s sin(2\omega_s t - \phi)}{8\omega_s} \tag{4.8}$$

.

Finally, the total capacitor voltage estimate must be calculated based on the estimate of the total stored capacitor energy,

$$v_{cu,l}^{\Sigma *} = \sqrt{\frac{2NW_{cu,l}^{\Sigma *}}{C_{sm}}}. \tag{4.9}$$

An overview of the method is presented in Figure 4.5. The open-loop energy balancing may reduce the need of additional circulating current control, as it reduces the oscillating components.

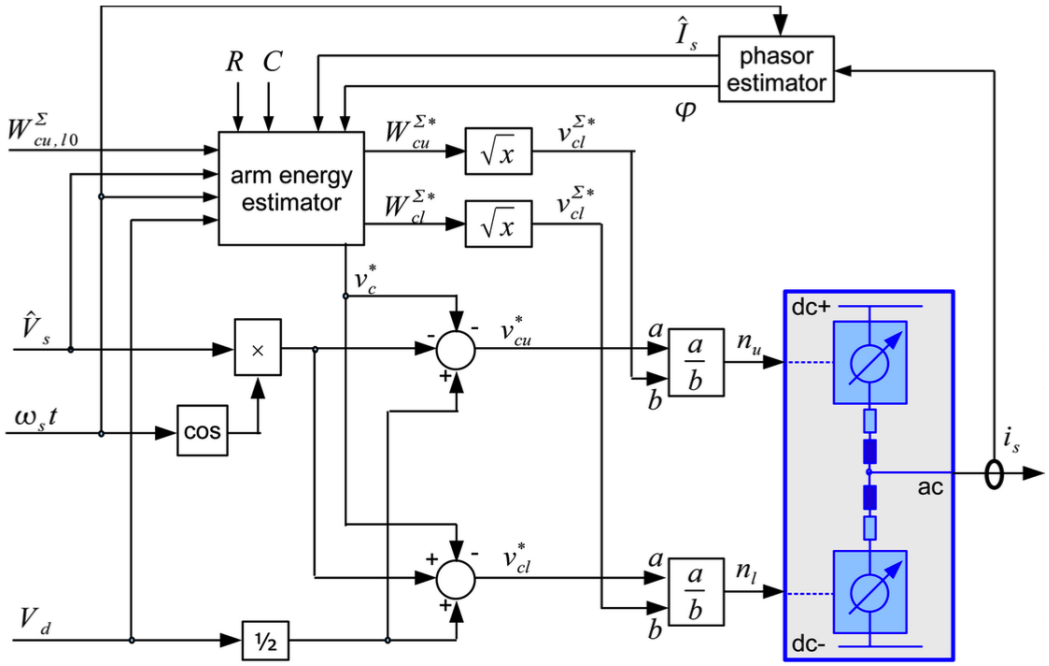


Figure 4.5: Block diagram of the open-loop controller [35]

4.4 Current control

As seen in (3.18a) and (3.18b), a big advantage with the MMC is that the control of the circulating current and output current is decoupled [52]. This is due to the decoupling of circulating current driving voltage, v_c, and the output voltage v_s, which depends on the the sum and difference of the upper and lower arm voltage, respectively. This is what makes the circulating current an additional degree of freedom.

4.4.1 Output current control

Controlling the grid currents of the MMC follows the same principles as for the 2L-VSC. The simplest way is through the *dq*-coordinates using Park-transformation [53]. The transformation matrix is given by

$$T_{abc/dq} = \frac{2}{3}\begin{bmatrix} cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \end{bmatrix}, \tag{4.10}$$

where $\theta = \omega_0 t$ is the grid voltage angle measured in the PLL. When the *dq* frame is aligned with the output voltage, the *d* and *q* components of the output current are proportional to the active- and reactive power [33, Chap.3]. Reactive power, Q, is regulated by acting on to the *d*-component of i_s, while active power, P, is regulated by acting on to the *q*-component. The MMC current model in *dq*-coordinates can be expressed

$$v_s^d(s) = \left(k_p + \frac{k_i}{s}\right)(i_s^{d*} - i_s^d) + v_g^d + \omega_s \frac{L}{2} i_s^q \tag{4.11a}$$

$$v_s^q(s) = \left(k_p + \frac{k_i}{s}\right)(i_s^{q*} - i_s^q) + v_g^q - \omega_s \frac{L}{2} i_s^d \tag{4.11b}$$

where $v_g^{d,q} \mp \omega_0 \frac{L}{2} i_s^{q,d}$ are the feed forward decoupling terms. These terms can be excluded if not needed, but will generally improve the dynamic response of the controller. When doing the Park-transformation, it is important to take defined positive current direction and the orientation of the *dq*-reference frame into account. The control system flow diagram is shown in Figure 4.6

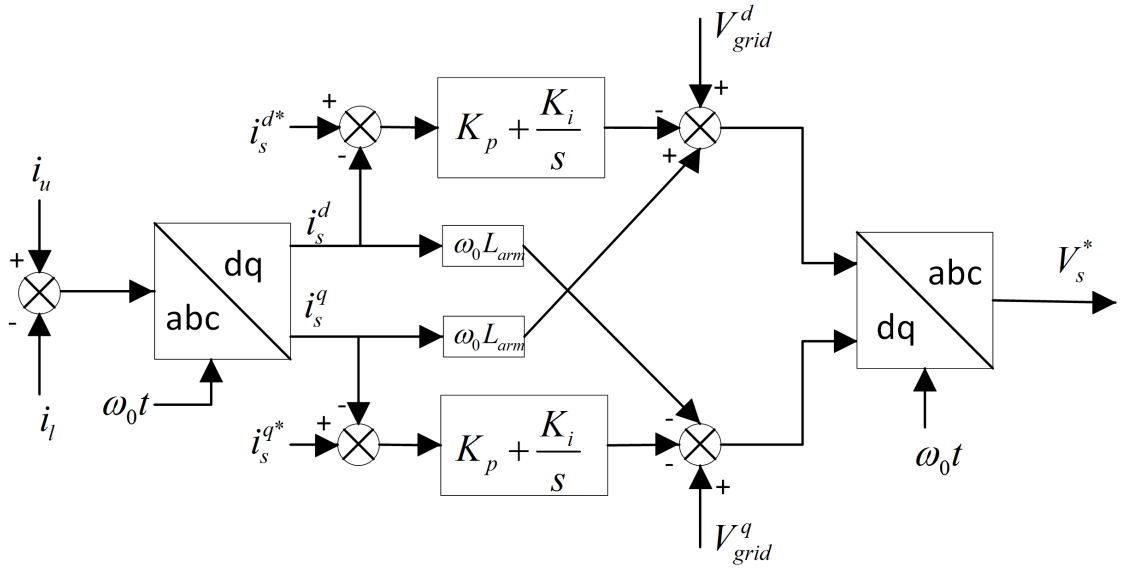


Figure 4.6: The output current control scheme

which is based on (4.11a) and (4.11b) .

4.4.2 Circulating current suppressing controller

In a MMC, each leg current is composed of three terms; AC, DC and a term dominated by the circulating current [34]. As it contributes to losses and increased component ratings, the circulating currents were previously considered a big drawback related to the MMC [52]. Now better dynamics can be achieved by controlling the circulating current, hence it is considered an additional degree of freedom. The circulating current suppressing control (CCSC) has been proposed to suppress the 2nd harmonic component of the circulating current [54]. The goal is to minimize the ripples so that the circulating current becomes a pure DC component. This is possible because the harmonic components don't contribute to the active power flow between the AC and DC terminals. This method also improves the AC output voltage of the converter.

The CCSC is based on converting the three-phase circulating currents into a double line frequency, negative sequence *dq*-reference frame [52]. That includes a Park-transformation at $2\omega_0$, which composes the 2nd harmonic into two DC components which both are controlled using PI-controllers. This is the same transformation described in (4.10) using $\theta = 2\omega_0 t$. In order to minimize the 2nd harmonic component, the *dq*-component reference signals for the currents are zero. The control scheme is demonstrated in Figure 4.7. The main drawback with this control method,

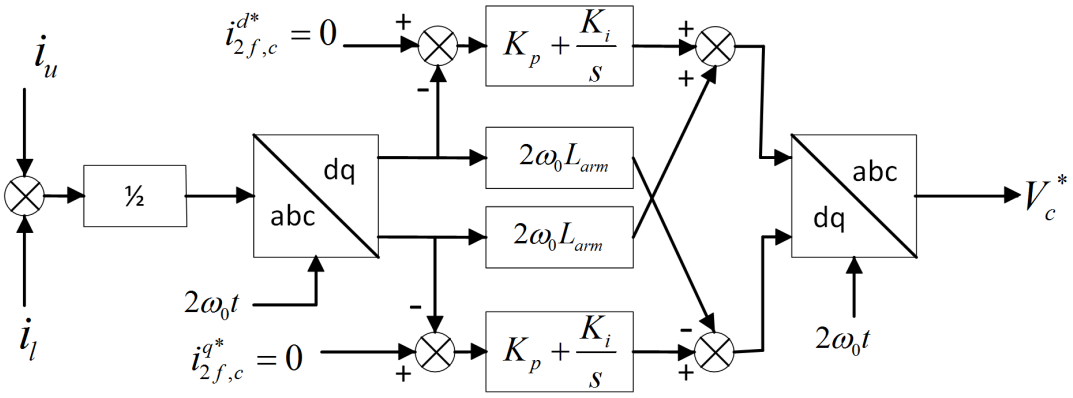


Figure 4.7: Circulating current suppression control scheme based on [54]

is the robustness under AC-grid imbalances and faults [42] .

A second method has been proposed where the unwanted 2nd order components of the circulating current can be compensated by injecting 2nd order harmonics terms to the deal modulating signals, hence obtain the desired output voltage [34]. Based on conversations with the industry it was concluded that the CCSC makes the control system less complicated, hence it was implemented in the MMC model.

4.5 Higher-level control

The high-level control often consists of four control loops, including the PLL, active and reactive power control, DC bus voltage control and power-synchronization control [33, Chap.3]. The bandwidth of these control loops must me lower than that of the current controller. In this model the PLL is used to measure the transformation angle θ used in the dq-transformation of the current controllers. The transformation angle is measured at the PCC.

In addition to the PLL, active and reactive power control will be investigated in this section. The dq-transformation for the output current control decouples the active and reactive power control, where the d- and q-axis will control reactive and active power respectively, as seen in Figure A.1. The reference for the power control is the required power while the output is the d and q components of the current reference which will be entering the output current control system. Figure A.1 demonstrates the whole control system and is found in the Appendix.

Chapter 5

Designing the MMC

This chapter will give an insight in the design and model strategies of the MMC investigated. The design of a MMC includes sizing of the capacitor and inductor, as well as finding the suited number of SMs [42]. In this chapter the design of the filter interconnecting the grid to the converter is also included.

The program used for the simulation is Matworks's Matlab/Simulink, which is a circuit simulator. When creating a Simulink model, the degree of detail must be chosen in terms of the main objective of the thesis. In this case the current and voltage stress on individual main-circuit components during faults will be investigated, hence a detailed model including switches, reverse diodes and SM capacitors is created. This model is able to demonstrate the balancing control of the capacitor voltages on SM level [33, Chap.5]. The degree of complexity is referred to as submodule-level switched (SLS) model type. The typical time step for simulations of power electronics considering internal fault studies is 10-100 μs. The time step chosen used in this simulation is 10 μs. When choosing a solver one must consider the speed om computation, robustness of the solver, the dynamics of the system and the stability of the solution [55]. The chosen solver is the *ode8*-solver, which is the most accurate of the fixed-step continuous explicit solvers provided in Simulink .

5.1 Converter arm current

In order to choose the correct semiconductor devices, the arm currents should be known. Thus, the arm currents are calculated using

$$I_{arm} = \frac{I_{dc}}{3} + \frac{i_{s,rms}}{2} + I_{marg} \tag{5.1}$$

where I_{marg} is the current margin which is assumed to be around 10-15 % of the $i_{s,rms}$ at full load and should account for the circulating current in the arms [56]. As the nominal DC-current is 66.7 A and the nominal rms AC-current is 67.3 A, I_{arm} = 66 A.

5.2 Power semiconductor devices

When using the SLS model type, ideal switches and diodes can be used to build the SMs [33, Chap.5]. IGBTs are often used with the MMC because it has low on-state resistance, hence low on-state losses, which is well suited for converters with low switching frequency [31]. The operation of a IGBT is designed to be midway between that of a BJT and a MOSFET. It is faster than a BJT and slower than a MOSFET, but still has losses that are comparable to those of a BJT. The IGBT is also capable of both series and parallel connection of the switches. IGCT was also considered as it offers higher efficiency and higher possible converter rating, which is important for HVDC-VSCs [57]. On the other hand, in applications where power fluctuations are strong, as in wind power applications, the IGBT have proved to achieve higher efficiency. The IGBT technology is mature and the most commonly used semiconductor for multilevel converters [58, Chap.25]. The IGBT chosen for this MMC is ABB's StakPak IGBT Module [59] with a blocking voltage of 4.5 kV. The maximum DC collector/forward current of 3000 A and a peak collector/forward current of maximum 6000 A for 1 ms. According to the data sheet, the maximum forward current that can be blocked by the IGBTs is 6000 A, also called turn-off safe operating area.

ABB is also supplying a fast recovery diode with a blocking voltage of 4.5 kV [60]. The average on-state current is 2620 A, while the peak non-repetitive surge current is 56 kA for maximum 10 ms. As the diodes cannot be controlled or blocked, they must tolerate higher surge currents than

Table 5.1: Power Semiconductor Parameters [59, 60]

Parameter	**IGBT**	**Diode**	**Unit**
Blocking voltage, V_{block}	4500	4500	V
Forward voltage, V_f	3	3	V
On-state resistance, R_on	1/1400	0.47e-3	Ω
Snubber resistance, R_s	5e6	5e6	Ω
Snubber capacitance, C_s	5e-9	5e-9	F

the transistors. The parameters used in the simulation model are taken from the ABB data sheets and are listed in Table 5.1.

5.3 Battery

The battery is modeled as an ideal DC voltage source to reduce the complexity of the model and the control system. Because of the time constraint, one ideal voltage source is placed at the common DC link instead of distributed into each SM. The ideal voltage source on the DC link will have the same voltage as the DC link. If the project is continued, the batteries can be moved to inside the SMs. The batteries will then be modeled as constant voltage sources with a voltage equal to the SM capacitor voltage. It is common practice to include a safety margin on the operating voltage of the semiconductor devices of 67% of the rated blocking voltage, hence the SM capacitor voltage should be equal to the SM voltage,

$$V_{bat} = V_{SM} = \frac{2}{3} V_{block} = 3kV \tag{5.2}$$

5.4 Number of submodules

The number of SMs can be calculated from the chosen semiconductor ratings and the desired DC bus voltage, as seen in (3.2). A DC voltage of 15 kV is chosen for this converter and since the IGBT has a blocking voltage of 4.5 kV, the number of SMs per arm is

$$N = \frac{15kV}{(2/3)4.5kV} = 5 \tag{5.3}$$

Since the MMC is a three-phase converter it has 6 arms, the total number of SMs is 30.

5.5 Converter parameters

In order to design a MMC to investigate fault currents, several parameters must be selected. The first decision made for this specific converter is the carrier frequency, $f_{carrier}$, of 1068.5 Hz. This specific value was obtained by testing in Simulink. Since the carrier frequency divided by 50 is not an integer, the switching pattern of each transistor will not be equal in each fundamental period. The carrier frequency is relatively high which gives rise to high switching losses, on the other hand losses are not investigated in this thesis and high switching frequency allows phase-shifted carrier signals with no submodule balancing, which simplifies the control system.

5.5.1 Submodule capacitance

The total energy stored in the SM capacitors is calculated to be

$$E^{tot} = 6x5\frac{1}{2}C_{sm}\left(\frac{15kV}{5}\right)^2 = 135C_{sm} \quad kV^2 \tag{5.4}$$

using (3.3). As the power rating of the converter is 1 MW and by demanding the time constant to be 40 ms, using (3.4), the calculation can be continued with

$$t = \frac{135C_{sm}}{1000}\frac{kV^2}{kVA} = \frac{135C_{sm}}{1000}\frac{kV}{A} = 0.135C_{sm}\frac{kV}{A} = 40ms \tag{5.5}$$

Hence, from (3.5) the minimum value of C_{sm} is calculated as

$$C_{sm} = \frac{40}{0.135}\frac{msA}{kV} = 0.296mF \tag{5.6}$$

To avoid ripples in the capacitor voltage, a higher C_{sm} should be chosen. After testing different values, it was concluded that C_{sm} should be 20 mF in order to reduce the capacitor voltage ripple. It was also mentioned in Section 3.5.1 that the reliability of the SM capacitors were extremely important to the operation of the converter.

5.5.2 Arm inductance

As the 2nd harmonic is considered the most dominant harmonic of the circulating current, h=2 is chosen when calculating the arm inductance using (3.6), resulting in an arm inductance, L_{arm} = 0.7mH. When implemented into the model, it became clear that this value is too low. Based on conversations with the industry, a method based on calculating Z_{base} using the converter nominal values and then choose L_s as 15 % of Z_{base}. As $V_{s,rms}$=8.6 kV and $I_{s,rms}$=67.3 A, Z_{base}=75.5 Ω.

$$0.15 Z_{base} = \omega_s L_s = 11\Omega \Rightarrow L_s = 35mH \tag{5.7}$$

As no filter is chosen at this point, L_s is $L_{arm}/2$. Hence, L_{arm} is 70 mH until the filter is chosen.

5.6 Grid

The three-phase grid is modeled as three controllable AC sources producing balanced sine wave currents with an amplitude of 7 kV. The maximum output current amplitude can't exceed $V_{dc}/2$, hence a lower grid voltage will reduce the chances of over-modulation. In order to reduce transients in the beginning of the simulation, the source is controlled to increase the amplitude from 0 to 7000 V during the first 0.2 s. A line transformer can be added to increase the voltage to 33 kV, but is excluded from the simulation to reduce the complexity of the model. The transformer should be a Δ - Y transformer, with the Δ on the converter side, in order to prevent the zero-sequence components caused by the unsymmetrical faults [61].

5.6.1 LCL Filter

Even though the MMC has very good output voltage and currents qualities, the current can have some harmonics around the switching frequency, an LCL filter has been proposed [62, 63]. For applications above several kWs the values of reactors and capacitors become rather high [62]. The LCL filter can be designed so that the inductance and capacitance are assigned optimal values, thus the filter cost and losses are decreased.

A step-by-step method for calculating the inductance and capacitance have been demonstrated in [63] and was used in the design of this LCL filter. The first step is to determine the converter side inductance, $L_{f,conv}$,

$$L_{f,conv} \geq \frac{V_{dc}}{8 i_{rip,max} f_{PWM}} = 0.0987H \tag{5.8}$$

when the peak nominal current is assumed to be 95.2 A. Hence since the total value of the inductance should limit the current ripple to 15-25 %, $I_{rip,max}$ is set to 19 A. Further, to avoid large AC voltage drop and poor ability of current tracking, $L_{f,conv}$ should be limited to

$$L_{f,conv} \leq \frac{\sqrt{V_{dc}^2/3 - V_{s,peak}^2}}{\omega_s I_{s,peak}} = 0.170H \tag{5.9}$$

After some testing in Simulink, $L_{f,conv}$ = 0.01 H was implemented. The capacitance, C_{filter}, can be designed as followed,

$$C_{filter} \leq 5\% x \frac{P_n}{3x2\pi f_s V_{rated}^2} = 0.1083mF \tag{5.10}$$

where V_{rated} is the RMS value of the converter output phase voltage. C_{filter} = 0.1 mF is implemented. By selecting the desired current ripple, σ, to be 10 %, the converter side inductance, $L_{f,grid}$, can be calculated using

$$\sigma = \frac{1}{| L_{f,grid} C_{filter} \omega_{PWM}^2 - 1 |} = 10\% \tag{5.11}$$

The resulting $L_{f,grid}$ is 2.78 mH, while $L_{f,grid}$ = 3 mH is implemented in the model. This filter gives an excellent current output, but also makes the calculations of L_s and further the tuning of the output current PI-controllers rather complex, thus the LCL filter is removed from the model.

5.6.2 Applied filter

The applied filter is an inductor in each phase. As discussed when calculating L_{arm}, the total inductance L_s should be 35 mH. A line inductance, L_{line}, is chosen as 20 mH, hence the arm inductance must be 30 mH. This filter gives a sufficient current output and is not as big and bulky as the LCL-filter.

5.7 Faults

The short circuit faults will be modeled as ideal switch which will be turned on by changing the gate signal from 0 to 1. The internal resistance is R_{fault} = 0.00001 Ω. All faults will occurs at t = 1 s.

5.8 Modulation and control systems

In order to avoid the balancing algorithm, the PWM method with phase-shifted carriers is implemented. In addition, the carrier signals for the lower legs are phase shifted by 180 degrees in order to reduce the period where each leg do not have 5 SMs in total switched on. This reduces the high frequency ripples in the circulating current.

Four control loops were described in chapter four, and have been created in order to control the MMC and achieve a sufficient operation. When the CCSC was implemented, it was noted that it had little effect on the circulating current because the circulating current didn't contain high 2nd order ripples. To avoid unnecessary calculations and measurements, hence reduce the simulation time, the CCSC-loop was removed from the implementation. It was mentioned that the 2nd order harmonic component of the circulating current was reduced when the arm balancing was introduced, hence the CCSC appears to be redundant.

5.8.1 Tuning and implementation of the inner PI controller

When simulating the PI controller for the output current it was noted that it wasn't bidirectional, as it was only able to follow the reference for either positive or negative requested power depending on the signs of the feed-forward terms. As the signs of the feed-forward terms are dependent on the direction of the measured current, these terms were removed from the controller, thus bidirectional operation was enabled. As it is a first order system, modulus optimum can be applied to tune the output current controller. The control in the *dq*-reference frame is described in (4.11a) and (4.11b). When tuning the controller, the feed-forward terms can be neglected [64]. The transfer function is given as

$$H(s) = \frac{K_p(1+sT_i)}{sT_i} \frac{1}{(1+sT_{delay})} \frac{1}{R_s(1+sT_{sys})} \tag{5.12}$$

where the three terms are the PI-controller, PWM delay (T_{delay}) and system transfer function respectively. T_{delay} is set to half the switching period [65]. Modulus optimum can be applied because one time constant is dominant compared to the others [64]. In this case it is the system time constant, T_{sys}. Setting the closed loop gain to 1, the following equations can be derived,

$$T_i = T_{sys} \tag{5.13a}$$

$$K_p = \frac{T_s R_s}{2T_{delay}} \tag{5.13b}$$

The resulting parameters are K_p = 37.40 and T_i = 0.035, thus K_i = 1068.5. The parameters were tested in Simulink and adjusted to achieve satisfying results. It should be noted that the modulus optimum method does not take the simulation time step, T_s, into account. T_s is affecting the integrator of the PI controller in discrete simulations, thus the calculated parameters are expected to need modification. After testing and adjusting in Simulink, the resulting parameters implemented into the model is K_p = 0.0374 and K_i = 427.4.

5.8.2 Tuning and implementation of the outer PI controller

The outer PI controller should be one decade slower than the inner PI controller [64]. The transfer function of the outer loop is given below.

$$H(s) = \frac{K_p(1+sT_i)}{sT_i} \frac{1}{(1+sT_{delay})} \left(\pm \frac{3}{2} V_{dc}\right) \tag{5.14}$$

The PI-controller tuning method is symmetrical optimum, and the equations for the parameter calculations are

$$T_i = a^2 T_{eq} \tag{5.15a}$$

$$K_p = \frac{2}{3V_{dc}} \tag{5.15b}$$

where a is the symmetrical distance between $1/T_i$ and cross-over frequency which is often set to a value between two and four. In this calculation a=2 is used. T_{eq} is representing the delay of the inner current controller. The calculation resulted in K_p = 0.000044 and and K_i = 0.00022. Adjustments in Simulink resulted in the final values of K_p= 4.4e-6 and and K_i = 0.0022.

5.9 Summary of model parameters

The parameters calculated in this chapter is implemented into the MMC model in Simulink and can be summarized in Table 5.2. The model implemented in Simulink is given in Figure 5.1.

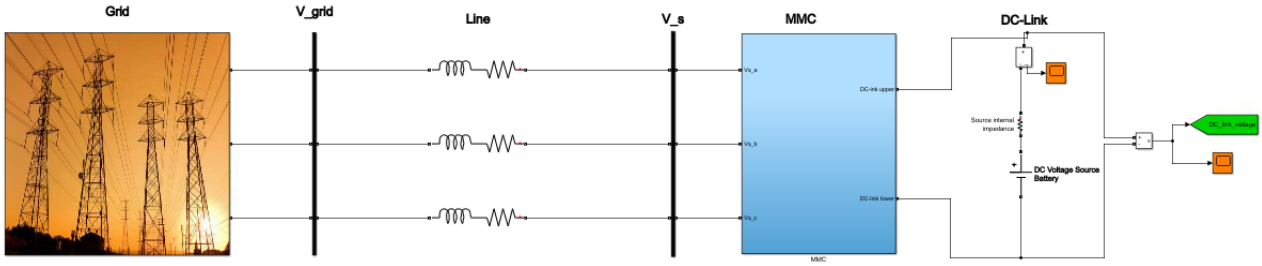


Figure 5.1: The model implemented in Simulink

Table 5.2: Circuit parameters for the MMC model

Item	**Abbreviation**	**Value**
Nominal power	P_n	1 MW
DC-link voltage	V_{dc}	15 kV
Grid voltage before transformer (phase, peak)	V_{grid}	7 kV
Grid frequency	ω_0	50 Hz
Sampling period	T_s	10μs
Number of SMs per arm	N	5
Carrier frequency	$f_{carrier}$	1068.5 Hz
Line inductance	L_{line}	20 mH
Line resistance	R_{line}	0.01 Ω
Arm inductance	L_{arm}	30 mH
SM capacitance	C_{SM}	20 mF
Proportional gain inner loop	$K_{p,inner}$	0.0374
Integral gain inner loop	$K_{i,inner}$	427.4
Proportional gain outer loop	$K_{p,outer}$	4.4e-6
Integral gain outer loop	$K_{i,outer}$	0.0022
Fault resistance	R_{fault}	0.00001 Ω

Chapter 6

Simulation and Results

In this chapter several fault scenarios will be investigated and compared to the reference case where no faults are applied. The different fault scenarios are listed below.

- Fault 1: Short-circuit fault on the capacitor side of a SM
- Fault 2: Short-circuit fault between a SM's terminals
- Fault 3: Short-circuit fault over one arm
- Fault 4: External short circuit fault on common DC-link
- Fault 5: External short circuit fault between phase b and c

If the control system is able to regain control, the DC link voltage and current, currents and voltages across the capacitor and semiconductors inside the SMs and the output voltage and currents will be investigated for all of the fault scenarios listed above. Graphs that are not included in the report, can be found in Appendix A.

6.1 Reference case

The model is run to observe the dynamics of the converter with the applied control and modulation. The reference for the active power will be changed during the simulation in order to see how

the system responds to step changes in power. It should be noted that the current is measured in such way that a positive power means that the converter is delivering power to the grid, thus acting as an inverter. When the power reference is negative, the grid supplies power to the converter, hence the converter is acting as a rectifier.

When the simulation is started, the converter is supplied by 1 MW power from the grid, hence the reference is -1 MW. The model uses approximately 0.5 s to reach steady state, thus this part of the simulation is excluded from the results, as it is not of interest in this thesis. The first step change in active power is at t = 0.8 s where the active power is changed from -1 MW to -0.5 MW. The next change is from -0.5 MW to 1 MW at t = 1 s, and the last is from 1 MW to -1 MW at t = 1.4 s. The reference of the reactive power is remaining 0 VAr.

6.1.1 Active power control

Figure 6.1 shows how the outer controller is able to follow the described step changes in active power. It takes the control system 230 ms to follow the power reference change from 1 MW out of the MMC to 1 MW into the MMC. As the active power is changed, the reactive power is experiencing some short-term deviations from the reference of around 20 kVAr. Some relatively large ripples can be seen in the DC current in Figure A.16, but they seem to decrease in magnitude with time. These ripples have a frequency of 6.5 Hz, which will be explained in the discussion.

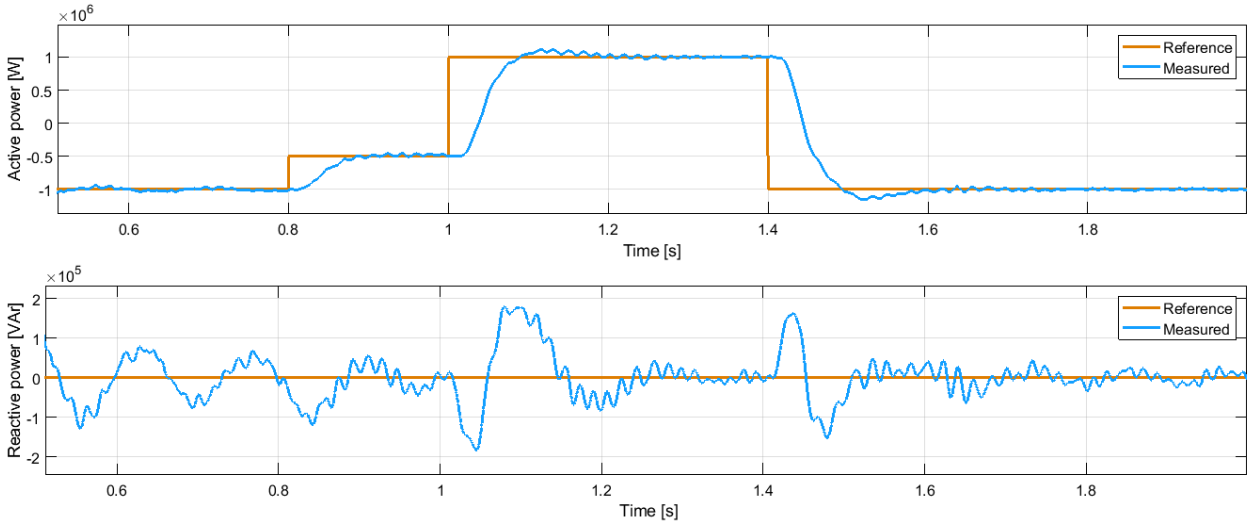


Figure 6.1: Dynamics of the outer controller during the reference case

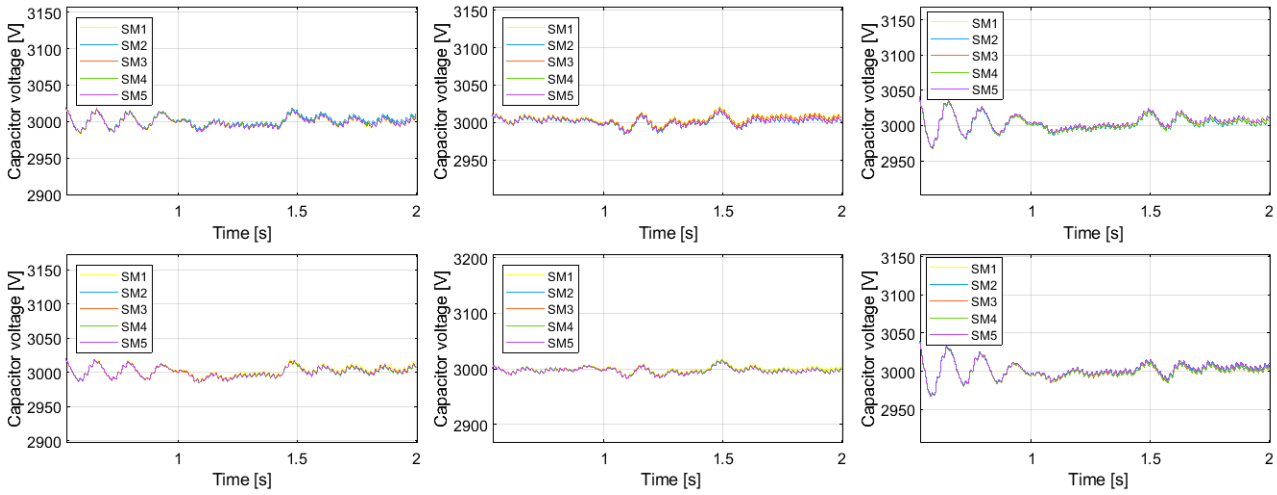


Figure 6.2: Capacitor voltages during the reference case

6.1.2 Capacitor voltage balancing

As the sorting algorithm to balance the SM capacitor voltages is excluded from the model, the SM voltages should be investigated to validate if PWM with phase-shifted carriers is sufficient, as assumed earlier through this thesis. In Figure 6.2 it can be that all five SMs of each arm are very well balanced and have insignificant deviations in the capacitor voltage which doesn't increase. The ripples are at around 1 % and within the acceptable limit.

The circulating current oscillations are decreased as the SM voltage is balanced and because the arm balancing is implemented. This can be seen from Figure 6.3. Some low frequency oscillations can be observed in all three phases and the DC component at nominal power is approximately ± 25 A as the power reference changes between ± 1 MW.

6.1.3 Current controller

As the q-component controls the active power and d-component controls reactive power, the output of the outer PI-controllers are used as reference for the dq-control system. In Figure 6.4 it can be seen how the measured current is following the reference form the outer controller. The current controller is delayed by approximately 20 ms from the reference. Figure 6.5 shows how the three phase voltage on the output terminals of the MMC, V_s, voltage at the grid side of the filter, V_{grid}, and current i_s. V_s has a total harmonic distortion (THD) of 10.73 % and can only be improved with

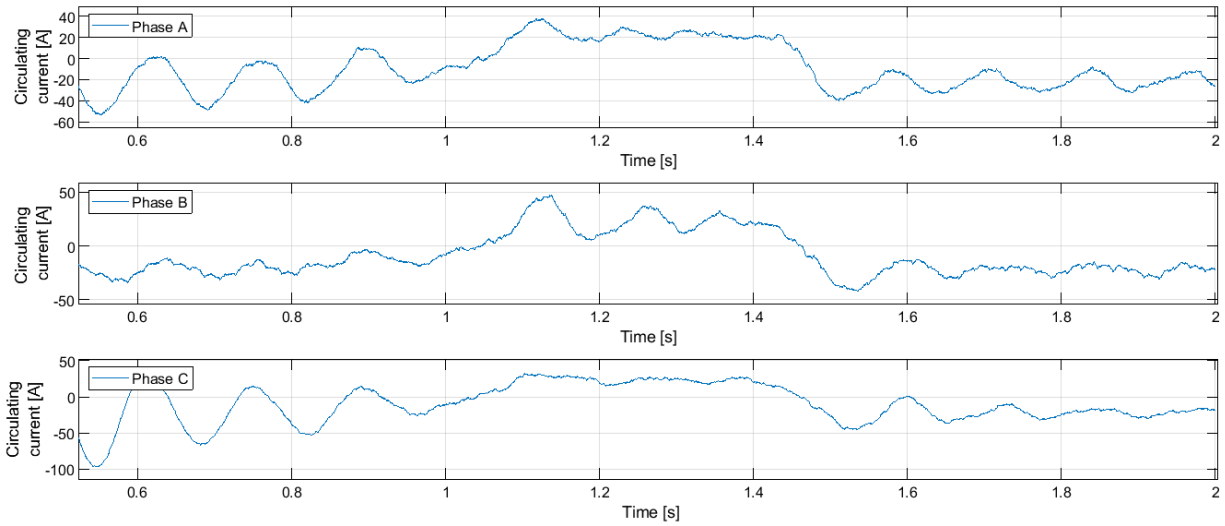


Figure 6.3: Circulating current during the reference case

an increased amount of SMs. When the current/power is negative, the three-phase current has a 180 degree phase-shift compared to the grid voltage. The output current THD in steady state is 1.78 %.

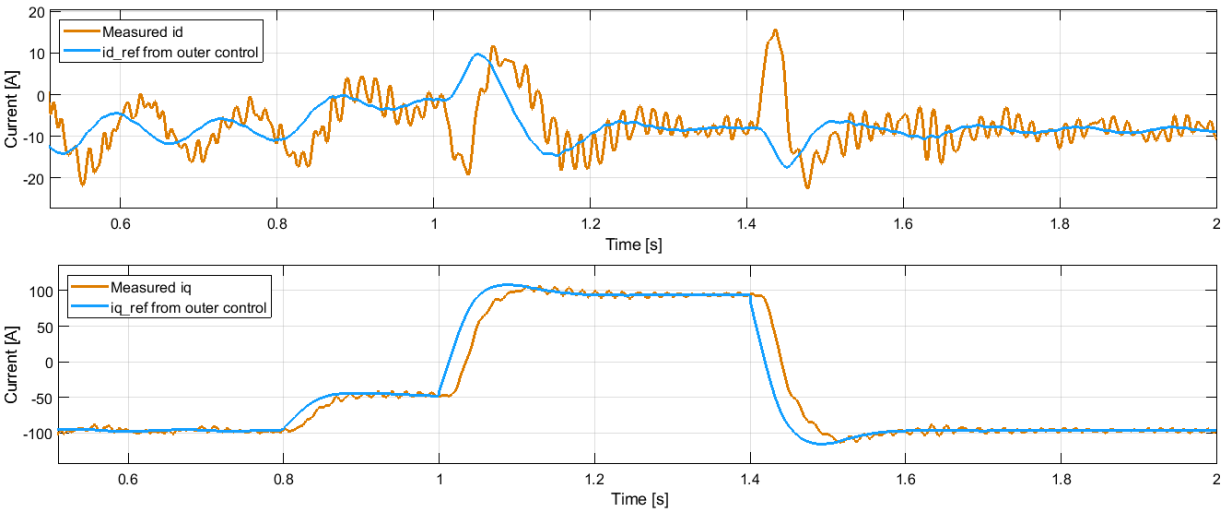


Figure 6.4: Dynamics of the inner controller during the reference case in the *dq*-frame

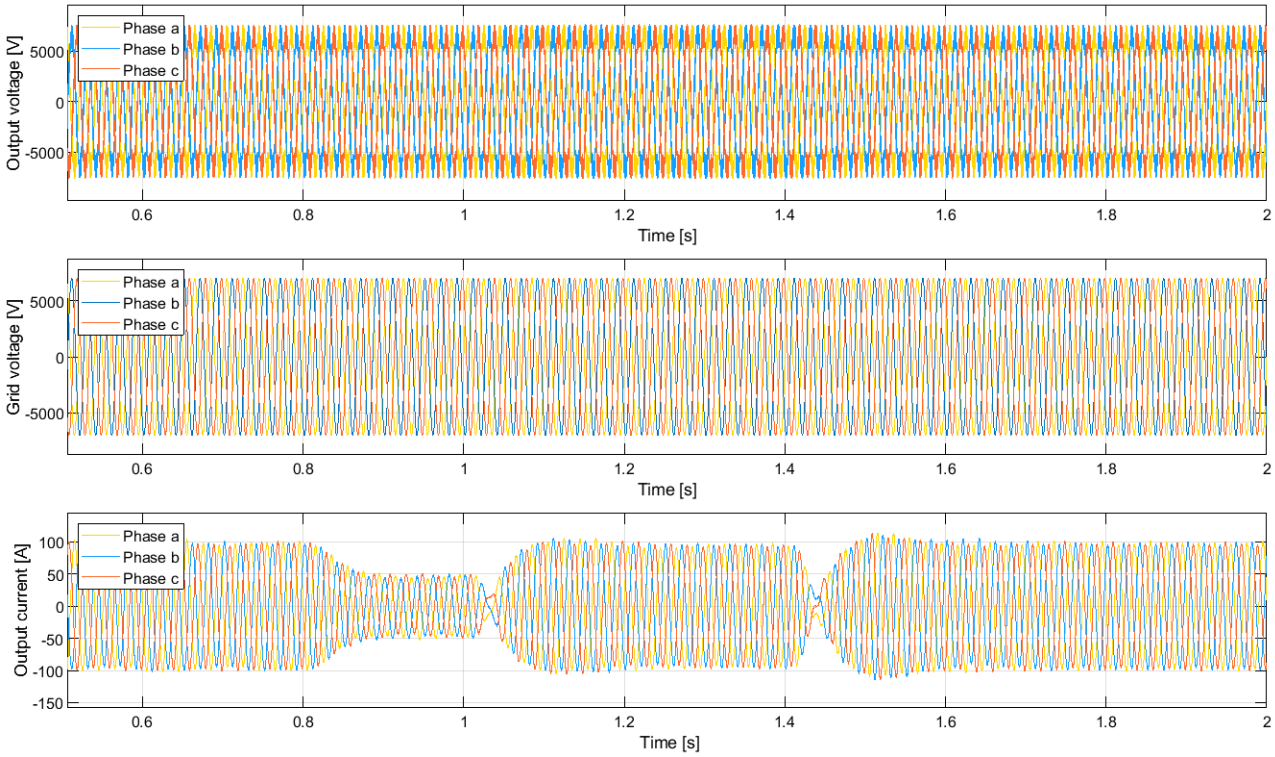


Figure 6.5: 3-phase output voltage, grid voltage and output current during the reference case

6.2 Fault 1: Short-circuit fault on capacitor side of SM

The first scenario to be investigated is when a short-circuit fault appears at the SM capacitor in the uppermost SM in the upper arm of phase *a*, as seen in Figure 6.6. In Figure 6.7, the phase *a* peak output current reaches 400 A at its maximum value, while the phase *b* and *c* peaks at approximately 250 A. The first post fault zero-crossing for all phases happens after 110 ms. At t = 1.2 s, the currents have stabilized, but all phases has a very low frequency oscillation, hence there is an offset between the phases. The current THD is 15.27 % after the fault where the largest harmonic component is 7 Hz, which creates the observed offset between the phases. The voltage doesn't experience any significant change as the fault appears and the THD is 11.95 %.

The capacitor voltage of the faulty SM is instantaneously decreased to zero as the fault occurs, as seen in Figure 6.8. This has an impact on the other SM voltages. First it can be seen that in the same arm as the fault, the SM capacitor voltages increases to a DC value of 3.6 kV with a ripple of 300 V, hence the peak value that appears right after the fault, is 3.9 kV. At the lower arm in phase *a*,

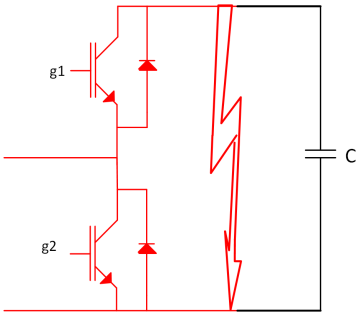


Figure 6.6: Schematic diagram illustrating Fault 1

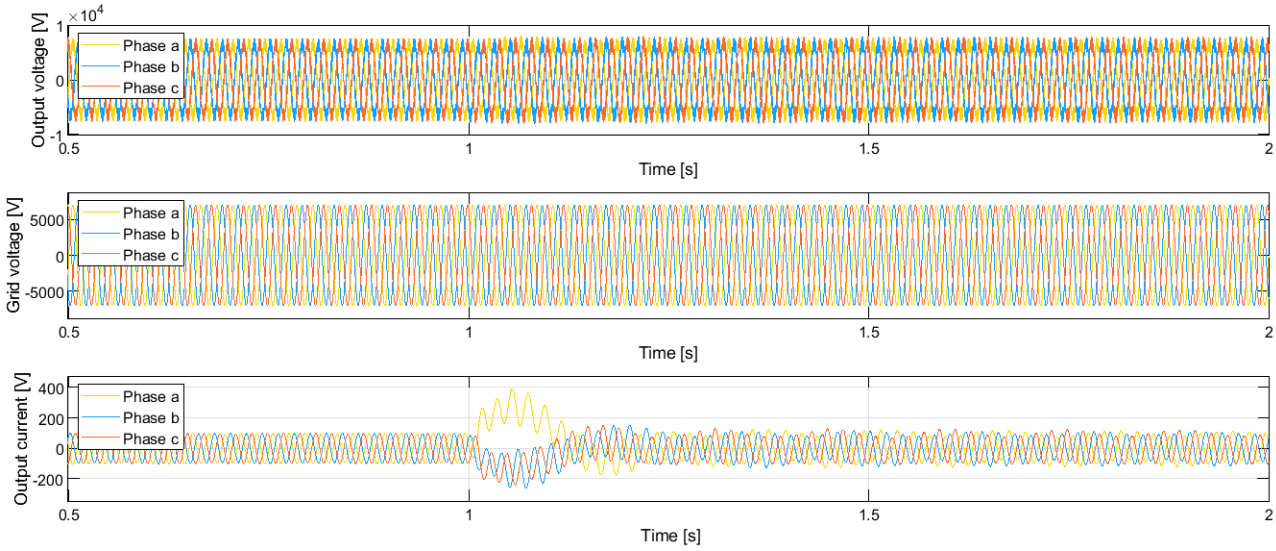


Figure 6.7: 3-phase output voltage, grid voltage and output current during Fault 1

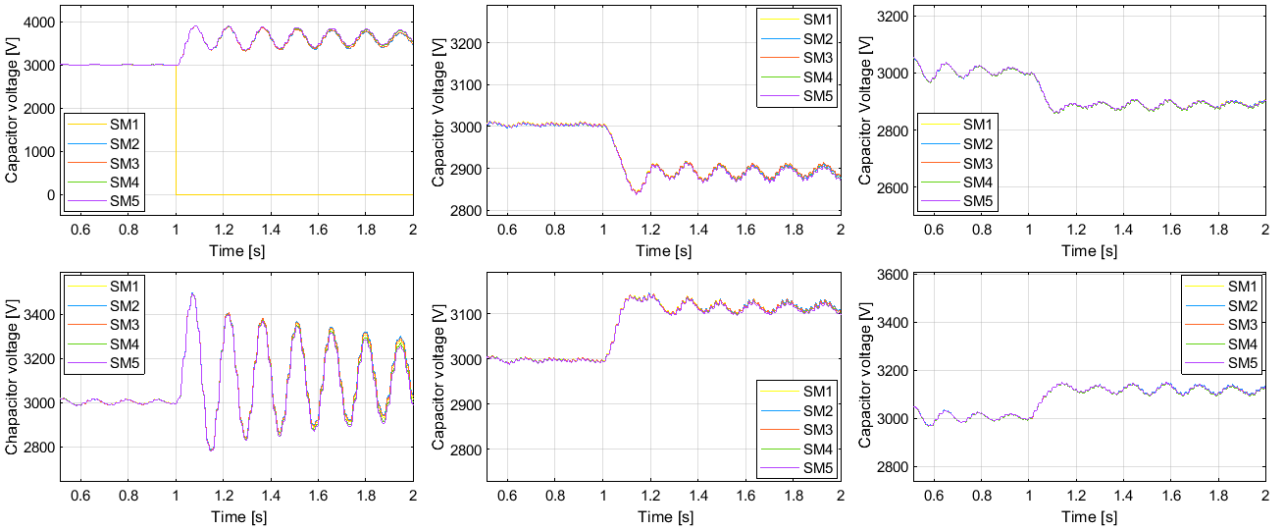


Figure 6.8: The SM capacitor voltages in all arms during Fault 1

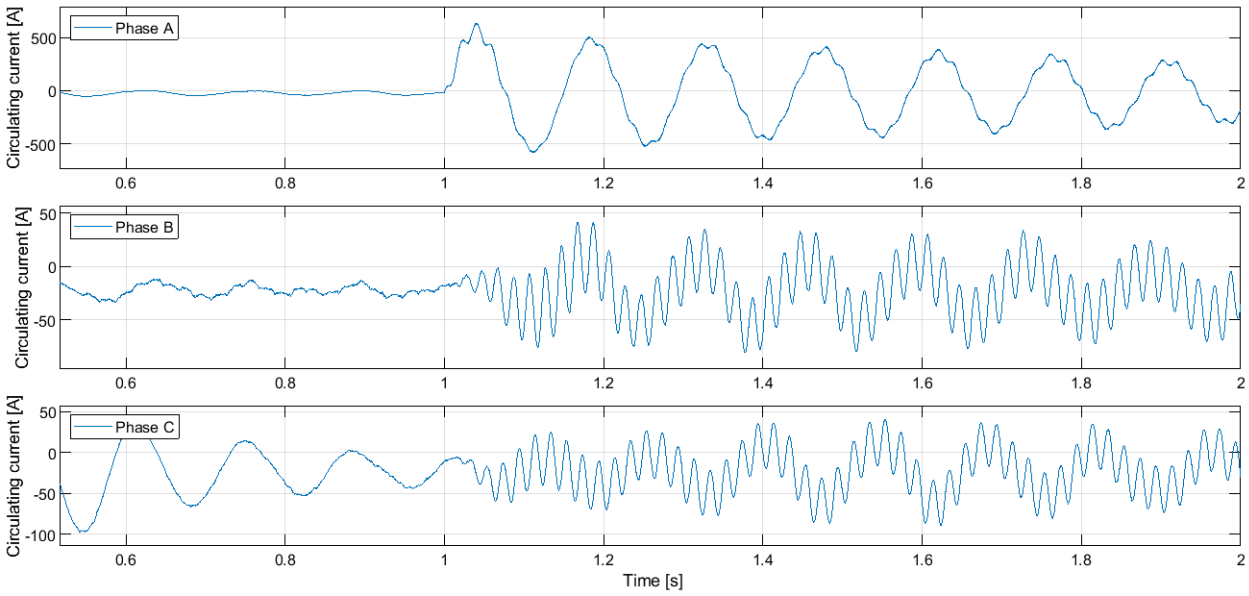


Figure 6.9: The circulating current of each phase during Fault 1

the DC components of the voltages are increased by 100 V and a ripple of the same magnitude as in the upper arms can be observed. For the capacitor voltages in phase *b* and *c*, a decrease by 100 V can be seen in the upper arms, while an increase by 100 V can be seen in the lower arms.

It is also interesting to look at the currents through the semiconductors in each individual SM. For the faulty SM the peak current through the semiconductors is reaching 800 A at the maximum value. The same maximum current magnitude is seen through the semiconductor devices in the other SM of the upper and lower arm of phase *a*. The post-fault arm current has a frequency of 6.5 Hz, which is the same as the circulating current through phase *a*. The circulating current through phase *a* has an amplitude of 500 A at zero offset. Different results are observed in phase *b* and *c*, as can be expected when looking at the circulating currents in these phases. The circulating current has a 50 Hz ripple of 25 A, and also a small 6.5 Hz harmonic. Looking at the currents though the semiconductors in phase *b*, it can be seen that the maximum current is 150 A with a characteristic in terms of frequency similar to the circulating current.

As the DC current flows through the battery in this model, it must be investigated to see if the battery can handle such currents. The battery will experience an oscillating current with a frequency of 6.5 Hz and amplitude of 600 A with no DC offset.

6.3 Fault 2: Short-circuit fault on the SM terminal

The second fault that will be investigated is a short-circuit fault at the terminals of the uppermost SM on the upper arm of phase *a*. This is relatively similar to Fault 1, but one difference should be noted. No current is flowing through the diodes and switches in the faulty SM after the fault occurs. A very high transient current appears at the same time as the fault. This transient current flows through the upper switch for 70 μs and has a magnitude of 2.7 MA. The currents through the other SM semiconductors in phase *a* are increased after the fault and the maximum peak current is 800 A. As in Fault 1, the arm currents though phase *a* have a frequency of 6.5 Hz. The current through the semiconductors in the healthy phases are similar to the ones of fault 1. The maximum peak current is 160 A and the frequency of the current is 50 Hz. There is no significant change in the magnitude of the semiconductor currents. The circulating current has the same characteristics as in Fault 1 which is shown in Figure 6.9.

As expected the capacitor voltage of the faulty SM goes to zero as the fault happens. As seen in Figure 6.11, the resulting capacitor voltages of the other SMs have no significant deviations from the results for Fault 1. The output current is shown in Figure 6.12, and it can be seen that the phase *a* current is subjected to a positive offset and reaches a maximum peak value of 400 A, while the phase *b* and *c* currents are subjected to a negative offset, hence there is an unbalance between the phases. After 150 ms, the offsets disappear and the currents seem to be under control. The 6.5 Hz component in the circulating current is creating an offset between the phases in the output current. The THD of the output current and voltage after the fault is 16.09 % and 11.96 % respectively.

The active and reactive power are subjected to a higher amount of high frequency ripples, but are able to follow the reference value. The DC current has the same 6.5 Hz frequency oscillation with an initial amplitude of 600 A.

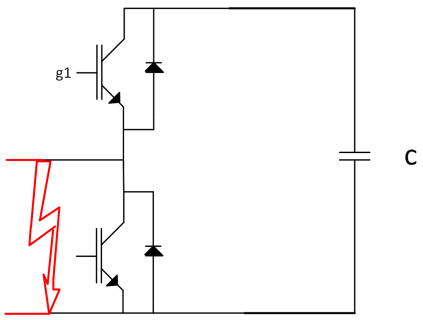


Figure 6.10: Schematic diagram illustrating Fault 2

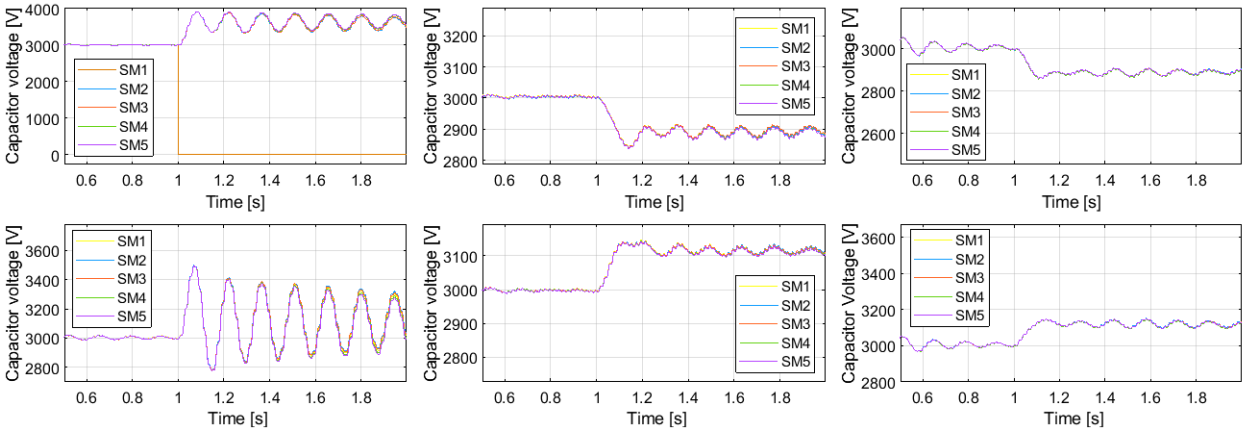


Figure 6.11: The SM capacitor voltages in all arms during Fault 2

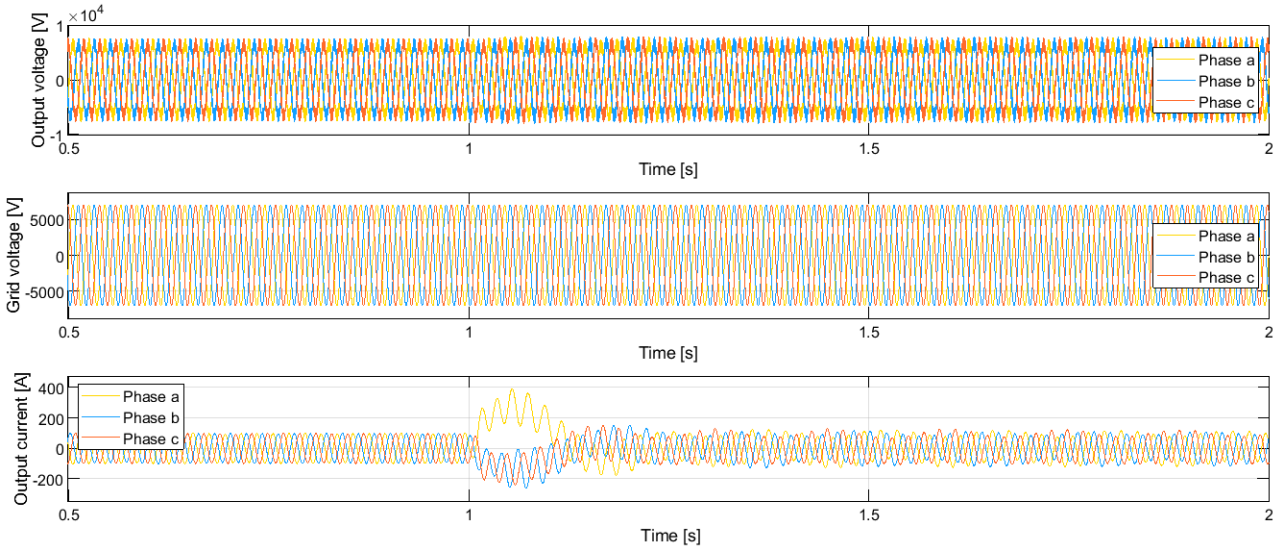


Figure 6.12: 3-phase output voltage, grid voltage and output current during Fault 2

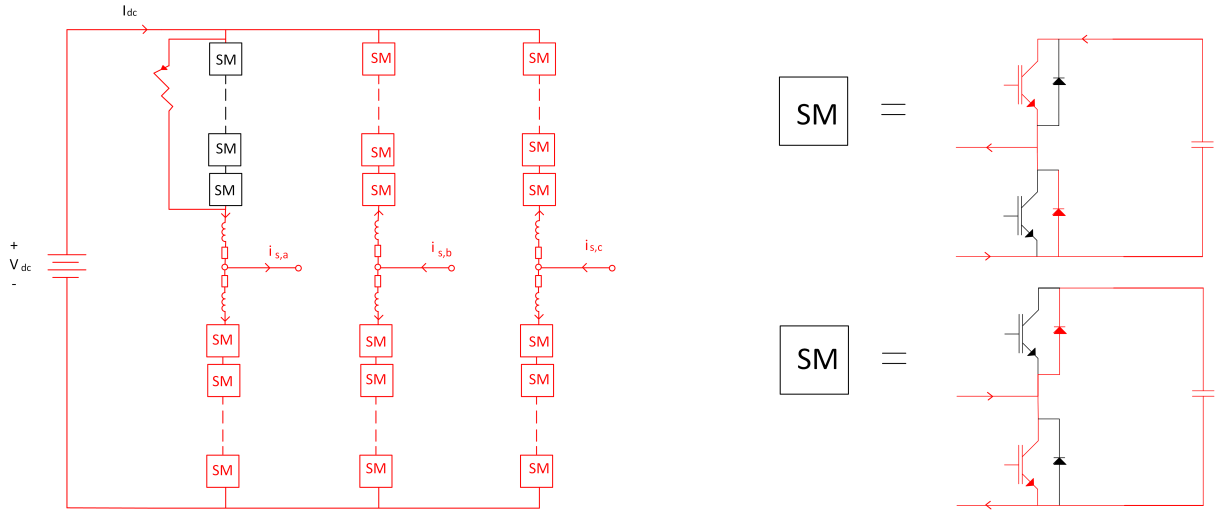


Figure 6.13: Line diagram describing the post fault currents of Fault 3 for the first 0.1 s after the fault occurs.

6.4 Fault 3: Short-circuit fault over one arm

As a short-circuit fault occurs over the upper arm of phase *a*, the voltage across the SMs in this arm immediately becomes zero. In Figure 6.14 it can be seen that the voltages across the SMs of the upper arms in phase *b* and *c* decrease to zero in 0.2 s. As a consequence, the voltages at the lower arm SMs increases to 6 kV. In phase *a* this change is happening very fast, thus the there is an overshoot in the voltage which has a peak value of 8.3 kV. The other phases the voltage increases slower, hence there is no significant overshoot. This compensation can also be seen in Figure 6.15, where all the upper arm voltages becomes zero and the lower arm SM voltages increase to 6 kV.

The output current experiences high transients after the fault. The phase *a* current reaches a magnitude of 5000 A, while phase *b* and *c* currents reach 3000 A at the maximum. The system stabilizes at around t = 1.2 s as seen in Figure 6.16 and the first zero-crossing takes place 1.9 ms after the fault occurs. After this the magnitude of the current is 1500 A and the output voltage magnitude is 3 kV. The THD of the output current and voltage from t = 1.8 s to t = 2 s, is 1.26 % and 20.66 % respectively. The current lags the grid voltage by approximately 90 degrees, hence it is an inductive current. The mean value of the transferred active power is 2 MW into the converter and with more high frequency ripples close to the switching frequency. The reactive power transfer increases to 5 MVAr out of the converter. The reactive power has both high frequency ripples, as in

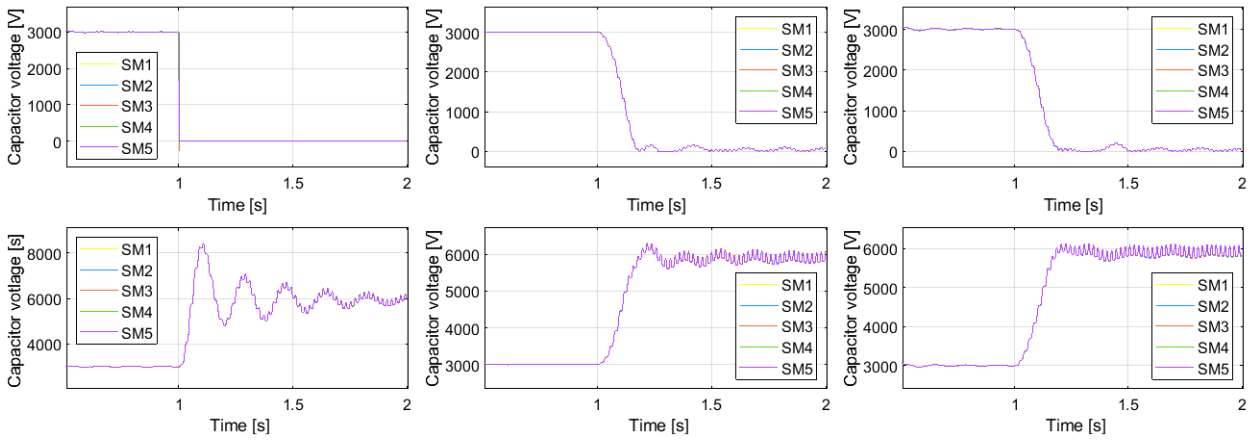


Figure 6.14: The SM capacitor voltages in all arms during Fault 3

the active power, and a dominant harmonic component of 300 Hz. The DC-current drops to -5000 amperes immediately after the fault and the drop lasts for 130 ms. After the drop, the DC current stabilizes around it's original value, but with 6.5 Hz oscillations with an amplitude of 1000 A and approximately 10 % ripple with a frequency of 150 Hz. The circulating currents also have ripples with an amplitude of 1000 A with the fundamental frequency.

When investigating the currents through the semiconductor devices, very high transients are observed in the SMs of upper arm of phase *a*. This transient occurs at t = 1 s, and only lasts for an instant before the currents becomes zero. The magnitude of the transient through the upper switches and lower diodes is 1.8 MA, which is unrealistically high, while through the lower switches and upper diodes it is 56 000 A. This can be seen in Figure A.27 in Appendix A. The transients in the SMs of the upper arms of phase *b* and *c* last longer and have magnitudes of up to 1650 A for the upper switch and lower diode, and 450 A for the lower switches and upper diodes. The current decreases after 0.2 s, but does not become zero. For the SMs on lower arm in phase *a* the upper switches and lower diodes experience currents of up to 4000 A and the lower switches and upper diodes experience currents of up to 2530 A. In phase *b* and *c* same currents are 2000 A and 1800 A respectively. In the lower SMs the current doesn't become zero and the transients are small.

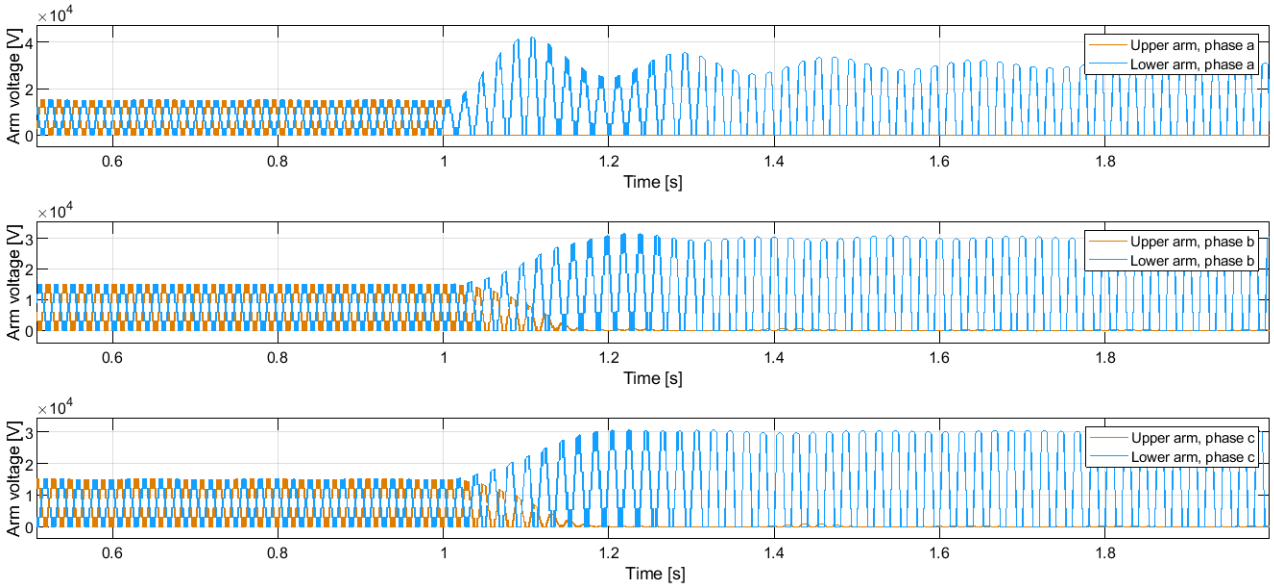


Figure 6.15: The arm voltages during Fault 3

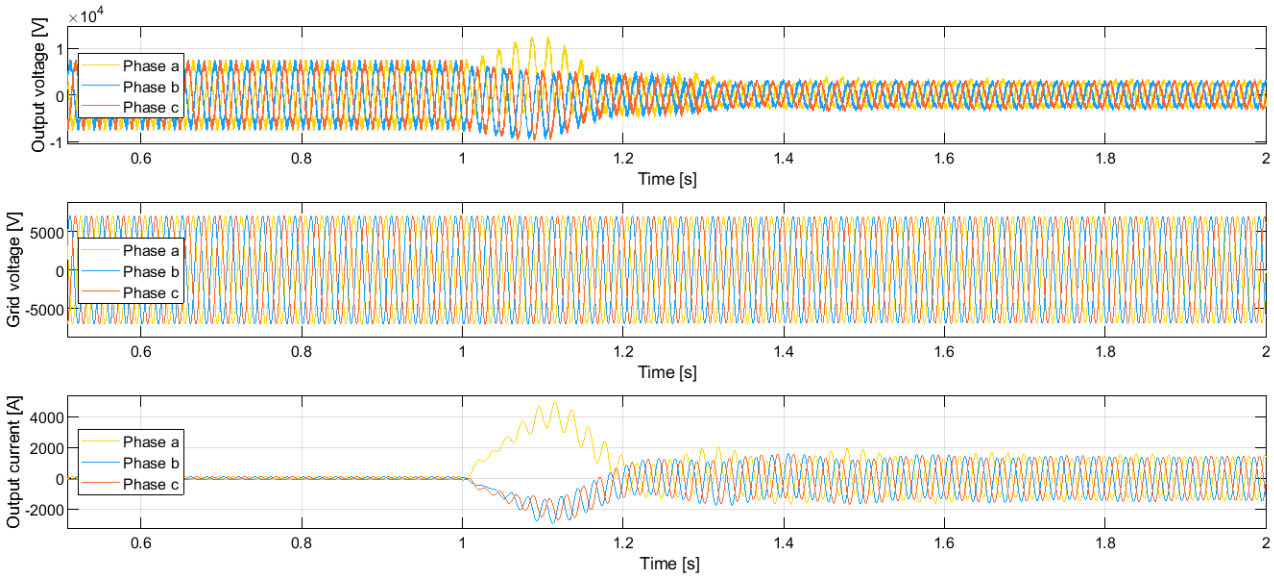
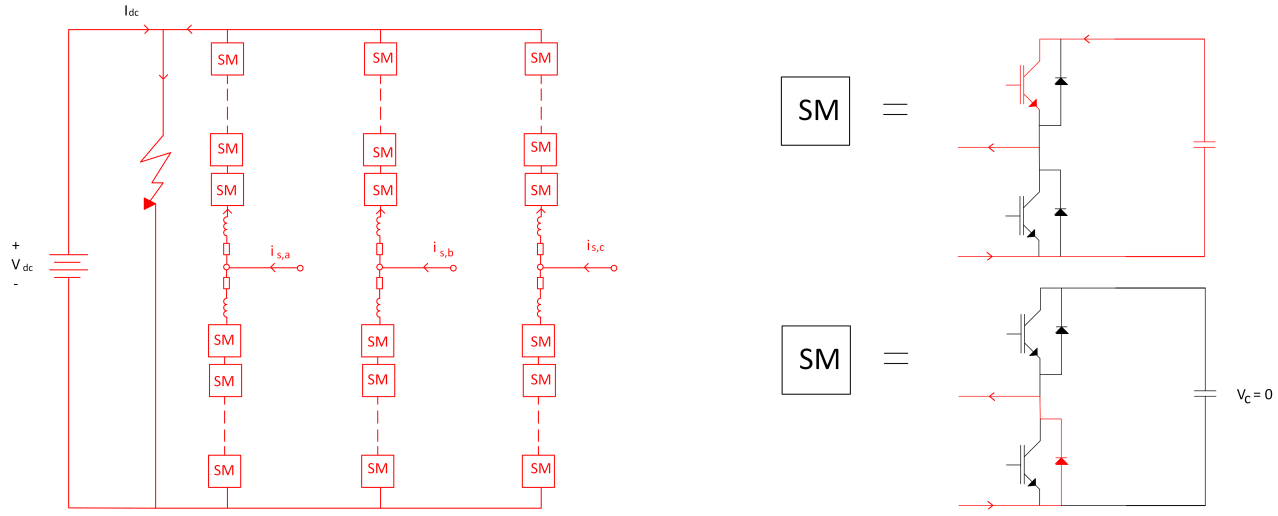


Figure 6.16: 3-phase output voltage, grid voltage and output current during Fault 3



a) The full MMC topology

b) The SM topology before and after the capacitor has discharged

Figure 6.17: Schematic diagram describing the post fault currents of Fault 4

6.5 Fault 4: Short-circuit at the DC bus

Figure 6.17 shows the current under a line-to-ground DC-link fault. The voltage of the DC bus goes to zero, hence the dynamics of the converter is changed. As a result of the low fault resistance, the DC current becomes extremely high. In this case it has a magnitude of 15 MA discharging the battery into the fault. The biggest contribution to the fault current comes from the battery, as the current from the MMC into the fault is 15 kA. This affects the active and reactive power transferred between the converter and the grid. The active power out of the converter goes from 1 MW to zero, while the reactive power goes from zero to 2.8 MVAr into the converter, feeding the fault. The active power going to zero is a consequence of the DC voltage being zero, hence no active power is delivered to the DC side. In addition to this, the circulating current DC-component is increased from -20 A to approximately -4000 A in 20 ms, and then slowly decreasing to -5000 A. Changes can also be observed in the output current and voltage, as seen in Figure 6.18. The first post fault zero-crossing for the current is 22 ms after the fault occurs. The system retains stability, but with a different voltage and current amplitude than what is requested from the control system. The magnitude of the output voltage after the fault is 3 kV and the magnitude of the current after the fault is 620 A and phase shifted by 90 degrees, thus it is an inductive current.

As the fault occurs, the voltage of the SMs are all decreased to zero as seen in Figure 6.19, thus all the capacitors are discharged relatively fast. This gives rise to the high transient AC current seen

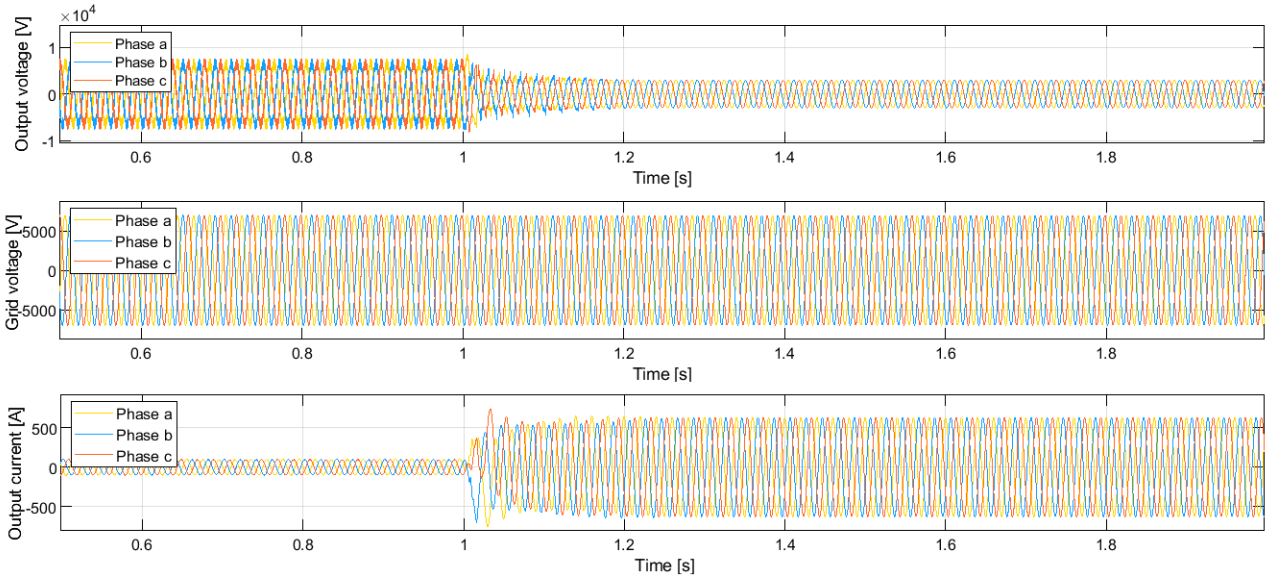


Figure 6.18: 3-phase output voltage, grid voltage and output current during Fault 4

in Figure 6.18. Further the currents through the upper diode and lower switch of each SM become zero after the fault occurs. The upper switches experiences some high currents of up to 5000 A the first 100 ms after the fault, then it goes to zero. The current through the lower diodes has some transients at the same time as the upper switches, but then it stabilizes as a DC fault current of 5000 A and less than 10 % ripple.

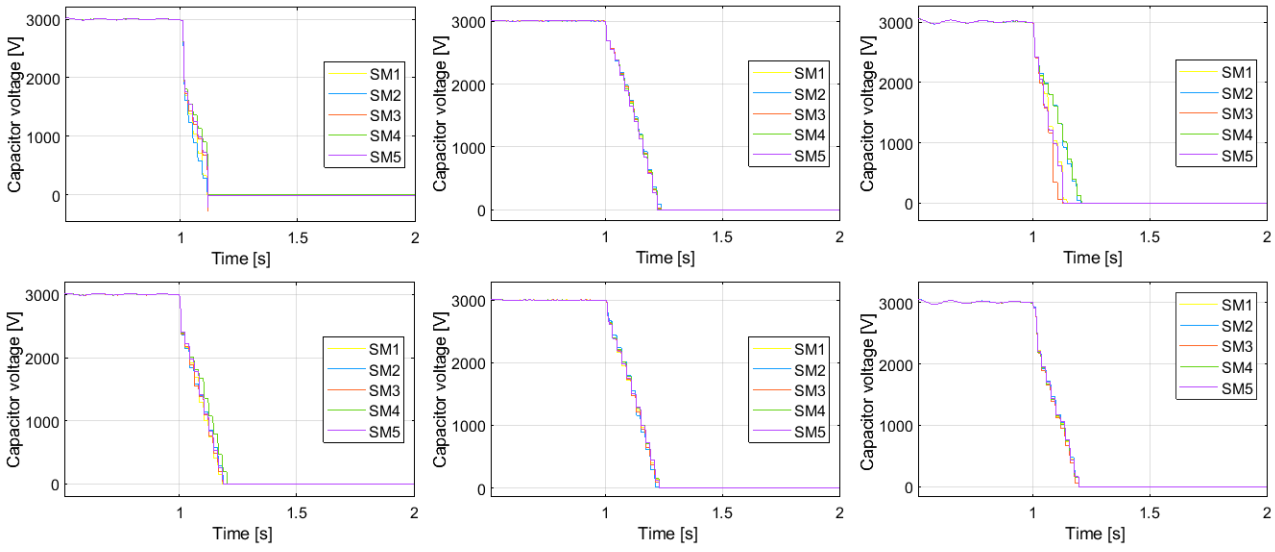


Figure 6.19: The SM capacitor voltages in all arms during Fault 4

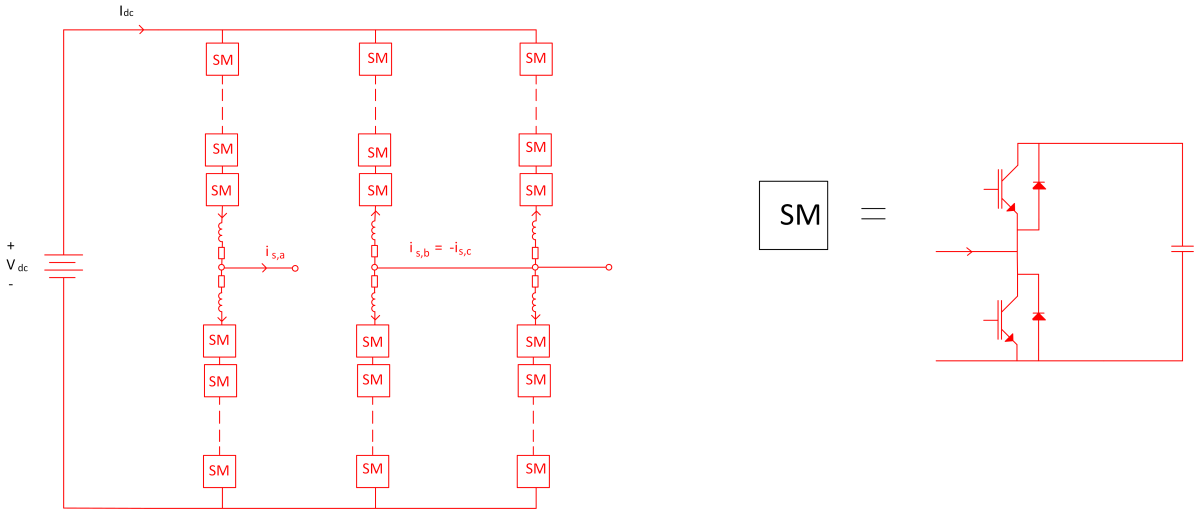


Figure 6.20: Schematic diagram describing the post fault currents of Fault 5

6.6 Fault 5: Short-circuit fault between phase b and c

The last fault to be investigated is a short-circuit fault between phase *b* and *c* at the output of the MMC as seen in Figure 6.20. This fault produces the highest disturbance at the output voltage because the voltage of phase *b* and *c* are equal, thus a balanced three-phase voltage cannot be regained, as seen in Figure 6.21. The output current suffers from extremely high peak values in the range of 5 to 12 kA. The first post fault zero-crossing for the output current is 10.7 ms after the fault occurs. The current through the short-circuited lines is approximately the same, but with opposite polarities. Both active and reactive power have high magnitude oscillations, meaning that a lot of power is going in and out of the converter.

In Figure 6.22 it can be seen that the line-to-line fault causes large oscillations in the capacitor voltage as the fault occurs. Note that the variations are smaller in phase *a*, where the ripple reaches a peak value of 4 kV, while in phase *b* and *c* the amplitude of the ripple is higher, so that the capacitor voltage exceeds 6 kV for all arms. The upper arm of phase *c* even exceeds 10 kV. The frequency of the capacitor voltage ripples is approximately 6.5 Hz. Similar results are seen when the currents through the SM semiconductors are investigated. In phase *a* the currents through the upper switch and lower diode do not exceed 1400 A and the current through the lower switch and upper diode does not exceed 1600 A. While in phase *b* and *c*, the currents through semiconductors reach 4800 A.

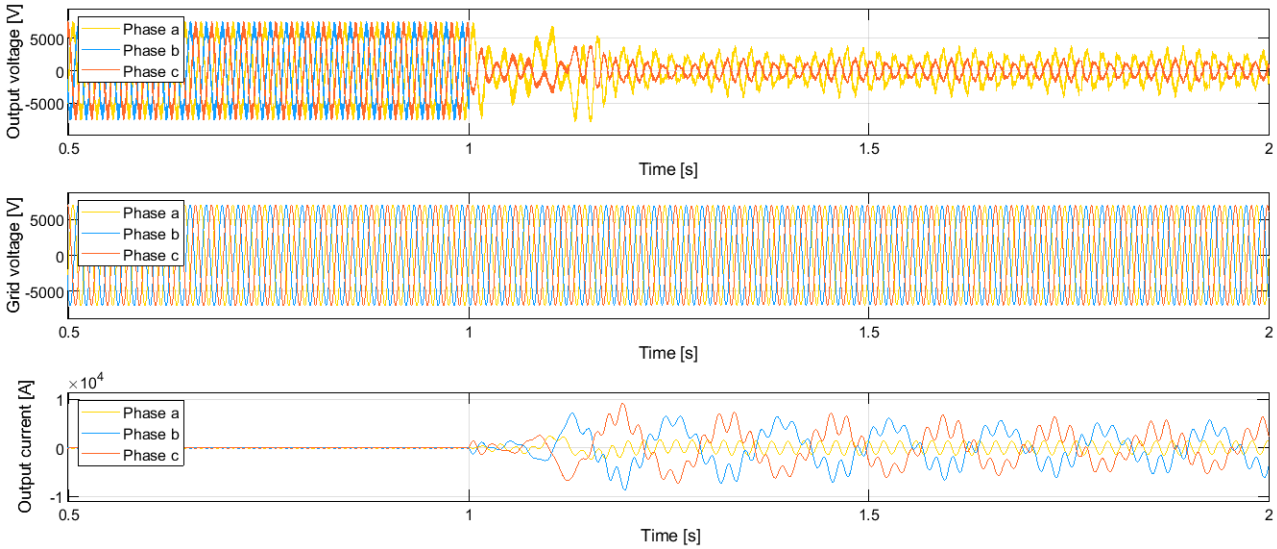


Figure 6.21: 3-phase output voltage, grid voltage and output current during Fault 5

It should also be noted that the DC current is oscillating with an amplitude of almost 5000 A and that the circulating currents also have oscillations that are around 500 A in amplitude in phase *a* and over 2000 A in phase *b* and *c*. Both have oscillations of 6.5 Hz frequency.

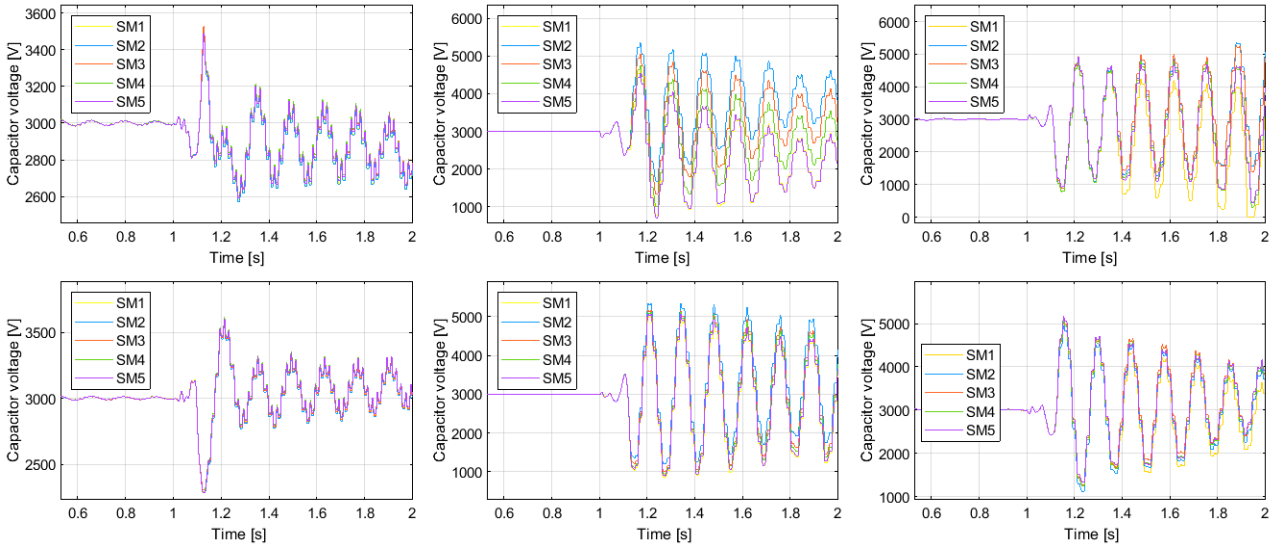


Figure 6.22: The SM capacitor voltages in all arms during Fault 5

Chapter 7

Discussion

The main goal of this thesis is to investigate the consequences of different faults on the suggested MMC with 1 MW BESS. A detailed model has been implemented in Simulink with IGBTs, diodes and capacitors, thus current and voltage stress can be investigated in order to identify the most critical components for each fault. The results presented in Chapter 6 are the current and voltages that appear for the different faults when no control or fault handling is present.

7.1 Comments on the results

The control system contains three controllers that regulate the active- and reactive power, output current and arm-energy balance. It was assumed that both CCSC and submodule energy balancing are not necessary, thus they were not included in the model. The modulation implemented is the carrier-based PWM. As the output current controller wasn't able to control the current in both directions when the feed forward decoupling terms were included, these terms were removed. The grid is modeled as three controllable ideal sources of 7 kV and is connected to the MMC through a filter consisting of an inductor.

7.1.1 Reference case

The reference case was run to investigate whether the assumptions, design and control chosen for this system are sufficient. Starting with the design, it can be seen that the SM capacitors are sufficiently high as the ripple of the capacitor voltage is approximately 1 %. As there is no significant high frequency ripple in the arm currents, the arm inductance is also sufficient. This was expected, as both C_{sm} and L_{arm} were increased from the calculated minimum values. The current THD is low, hence the filter has a sufficiently large inductance as well. The problem with this solution is that the size of capacitors might be larger than necessary, increasing the size and costs of the converter, hence an optimization of the capacitance should have been done.

To exclude the CCSC from the control system sufficient approximation for this MMC as there is no clear 2nd order harmonic or fundamental component in the circulating current. The phase-shifted PWM together with the relatively high switching frequency balance the energy between the SMs, while the arm-energy balance control balances the energy between the arms of each phase. This was seen both from the small ripples in the capacitor voltages in Figure 6.2 and the small oscillations in the circulating current in Figure 6.3. The oscillation on the DC current should be avoided as it was mentioned that a typical lithium ion battery has a AC tolerance of 10 %. A battery filter should have been implemented.

The dynamics of the system can be reviewed as the power reference is changes from 1 MW to -1 MW. This is a step change in power of twice the nominal power, thus the 230 ms before the controller has stabilized the system is sufficiently fast. This is an indicator of that the feed forward decoupling terms can be neglected from the inner controller.

7.1.2 Fault 1: Short-circuit fault on capacitor side of SM

The short circuit of the SM capacitor on the uppermost SM causes some relatively large transient AC currents before after 110 ms, it is controlled to it's original magnitude of 100 A. In this case, the capacitor discharges into the fault. In the theory it was stated that as the number of SMs is high, the bypassing of one SM will not affect the operation significantly. As the THD increases from 1.78 % in steady state prior to the fault, to 15.23 % in steady state post fault, it can be concluded that the number of SMs isn't high enough to ensure redundancy. If the number of SMs is higher, the

increase in capacitor voltage in the remaining SMs is smaller, thus the fault will have less impact on the converter operation.

As it was seen in the results, the healthy SMs of the upper arm will increase the capacitor voltage in order to compensate for the voltage being zero in the faulty SM. This increase means that the remaining capacitors and transistors in the faulty arm must operate at a higher voltage for a longer time if the operation of the converter is continued. When transistors are operated at a higher voltage than ideal, failures are more frequent, hence the operation shouldn't continue too long before the fault is cleared. The currents through the faulty SM components are reaching 800 A, thus is not exceeding the limit of operation of nether IGBTs or diodes.

The increase in magnitude of the circulating current will result in higher losses in the converter. These losses will also increase the operating temperature, which also indicates that the operation of the converter shouldn't continue too long. The converter can be isolated from the grid using AC breakers, but as the zero-crossing doesn't take place before 110 ms after the fault occurs, it will not be able to prevent the 400 A transient in the AC current. On the other hand, the transients can be reduced if the IGBTs are blocked. The third reason to end the operation, is that the DC current has large oscillation, thus the battery is charged and discharged at currents up to 600 A, which as mentioned in the theory, will reduce the cycle life of the battery.

The low frequency oscillating current seen in the DC current, circulating current and capacitor ripple comes from the design of L_{arm} and C_{sm}. As $1/(2\pi\sqrt{C_{sm}L_{arm}}) = 6.5$ Hz, this frequency is the resonance frequency of the MMC.

7.1.3 Fault 2: Short-circuit fault on the SM terminal

The only difference from Fault 1, is that no currents are going through the semiconductors after the fault occurs, except from an unrealistically high surge current of 2.7 MA through the upper switch. This current comes from discharging the capacitor through the IGBT, and not through the fault as in Fault 1. When calculating the discharge current from a 3 kV capacitor through the upper IGBT with an on-state resistance of $1/1400\ \Omega$ and a forward voltage of 3 V, it is seen that this is the correct capacitor discharge current magnitude. On the other hand, in a real case there will not be such high currents because of the over-current protection circuits integrated with the gate driver.

If the large transient is not blocked, the upper IGBT of the faulty SM will be damaged.

7.1.4 Fault 3: Short-circuit fault over one arm

As expected, the transient current of phase *a* would be bigger than for Fault 1 and 2 as five SMs are short-circuited on the upper arm. As a result, the upper arms of the two healthy phases are discharged too, this is due to all arms being connected at the positive DC terminal, thus having the same voltage . A total of 15 SMs are discharged, thus causing the 5000 A transient in the AC current. Since the fault only appears at one arm, there is a deviation between the phases in the output current which is the reason why the first post fault zero-crossing takes place 190 ms after the fault occurs. This is enough time for a large current to flow through all the converter valves, hence AC breakers might be insufficient. The decrease in voltage between the grid and converter terminals is due to the large current through the line impedance. As the upper arm voltages go to zero, the arm balancing control is not working and the control system is not able to control the active and reactive power, currents or voltages. A 1500 A inductive current enters the MMC from the grid, and is reflected in the large circulating currents.

During the first 100 ms, which is before the AC breakers are able to break the current, the battery will feed the fault with surge current of up to 5000 A. After that, the DC current has oscillations of up to 1000 A both charging and discharging the battery. As mentioned in the discussion of Fault 1, this decreases the cycle lifetime of the battery. This, in addition to the AC breakers time delay, proves the importance of the development of DC breakers with short response time.

The unrealistically high current through the transistors in the upper arm SMs would not appear in a real case, as the transistors would be blocked before the currents reach such magnitudes. As high currents through the transistors are detected, the transistors will be blocked by the over-current protection function in the drive circuit. The maximum current that can be blocked by the chosen IGBTs, is 6000 A. The lower diodes can't be blocked while experiencing a 56 kA surge current, thus they are at risk of being damaged as 56 kA is the maximum surge current of the diodes from ABB chosen in this thesis.

As the upper arms have discharged all capacitors to zero voltage, it was seen that the remaining SMs tried to compensate for the upper arms by increasing their voltage to 6 kV, hence exceeding

the maximum blocking voltage of the transistors and diodes in all SMs at the lower arms. This demonstrates the importance of blocking the transistors in the lower arms as the fault occurs. The blocking of the transistors can be realized using a over-voltage protection function in the drive circuit that detects high voltages over the transistor.

7.1.5 Fault 4: Short-circuit at the DC bus

It was previously discussed that just like the conventional 2L- and 3L-VSCs, the MMC with HB SMs will loose control of its currents as a DC fault occurs. This is because the SMs will act as rectifiers and feed currents to the fault. The released energy from discharging all the capacitors at the same time will result in extremely high transient currents. This has been proven in the results of Fault 4.

One important aspect of the DC link fault, is that when the DC voltage is zero, the arm energy balancing control is not able to estimate the arm energies, thus the control system will loose control over the currents. As for Fault 3, an inductive, large, uncontrollable current is entering the converter. Thus AC breakers should be implemented to isolate the MMC from the grid. The active power transfer after the fault is zero, which is consistent with theory, as the DC voltage is zero.

As the DC link is short-circuited, a large DC current of 15 MA from the battery to the fault occurs. This is a result of the battery being modeled as an ideal DC source. Since it is an ideal source, there is no limitations on how much current the battery can supply and for how long. This is a drawback with the chosen implementation in Simulink. The real case current will be smaller and limited by the SOC and power rating, but this demonstrates how important it is to include battery protection control in the BMS, especially to protect the battery from undercharging. DC circuit breakers are particularly important to protect the battery in case of DC faults. If the battery is left unprotected, which would not be the case in a real system, the anticipated current will be 15 MA.

As in Fault 3, fault handling strategies should be implemented to prevent damage in the converter valves. The currents through the upper switches and lower diodes are reaching values just over 5000 A which is close to the peak collector current limit of the IGBTs. The continuous current through the lower diode is almost twice the maximum average on-state current, hence the lower diodes of all SMs will be damaged. Blocking of the SM transistors is necessary, as the large current can cause over-heating. The blocking doesn't prevent the current through the lower diode, hence

AC breakers must be applied. The AC breakers will not be able to turn off the current before 22 ms after the Fault, nevertheless this is relatively fast compared to Fault 3, thus the fault current has not yet reached the highest magnitudes. 22 ms is also fast enough to break the current before the diodes experience the 5000 A on-state current, hence they can be spared. The zero-crossing comes faster than for Fault 3 because all phases are involved in the fault.

The capacitors have not fully discharged 22 ms after the fault, hence it is possible to turn off the AC breakers at a given time after they are activated to see if the fault has cleared. If the fault is cleared, the operation can continue. It is important to deactivate the control system while the AC breakers are on, so that the errors in the PI-controllers are not able to accumulate as this would prevent the control system in regaining balance.

7.1.6 Fault 5: Short-circuit fault between phase b and c

The highest AC currents appear during the short-circuit fault between phase *b* and *c*, which is expected as the current from the grid flows directly into the fault. The AC voltage at the converter terminals is not balanced as the voltages of the two faulty phases are equal after the fault. The DC current increases with time and becomes very large, on the other hand it doesn't become large before 100 ms after the fault.

The oscillations in capacitor voltages in phase lag *b* and *c* exceed the SM blocking voltage, hence all semiconductors in these phases will be damaged. Both blocking of the transistors and AC breakers must be activated to limit the damage from the fault. A zero-crossing that appears 10.5 ms after the fault is very sufficient as it is only half a fundamental period, and the fault currents have not yet obtained the highest magnitudes. If the AC breakers are turned on 10.5 ms after the fault occurs, the large fault current through the semiconductors will be prevented, thus little damage is done to the components. AC breakers seam to be sufficient to handle a line-to-line short circuit fault, but IGBT blocking should also be implemented to prevent damage and reduce the transient currents from discharging the capacitors.

7.1.7 Comparison and most critical components

As expected, the least critical faults are those that appears inside the SM, as the control system is able to continue the operation. On the other hand, there are too few SMs in each arm to operate the converter for long without increasing the risk of component failure due to high transistor voltages and large circulating currents. The DC current is also oscillating so that the battery is charged and discharged, hence the cycle life of the battery is decreased. The converter should be designed with more SMs to achieve proper redundancy.

For the short-circuit of one converter arm, DC link and phase-to-phase AC terminals, the control system is not able to control the AC current, hence the converter must be isolated from the grid to prevent damage on the converter valves. This can be achieved using AC breakers, hence appearance of the first post fault zero-crossing for the AC current is crucial. For Fault 3, this is after 190 ms, thus fast-acting DC breakers must be in place to prevent damage. These are not yet commercially available, hence Fault 3 can be recognized as the most critical fault. As the voltage in the line-to-line fault is unbalanced, this fault might effect the voltage on the PPC for the wind turbine, hence this fault is also critical, but on the other hand the AC breakers will be turned on before the fault currents gets too big.

7.2 Limitations

Some simplifications are done in order to build the Simulink model with a sufficiently good control system within the time limit of this master thesis. The main limitations of this thesis are

- Simulink is not modeling the component failure and DC and AC breakers are not implemented, thus the operation of the converter after fault will continue as if no components has failed.
- Batteries are modeled as ideal voltage sources, hence the available power (SOC) and physical limitations are neglected
- Only the MMC and battery are studied, hence WECS problems and fluctuations are neglected

- Ideal grid model was used, hence effects from disturbances in the grid are neglected. Unbalanced output voltages will not affect the grid voltage in this model.
- The Δ-Y transformer is excluded, thus it's effect on the zero-sequence current is not studied
- Only half-bridge submodule configuration is considered
- No control systems for unbalanced systems was studied
- The results from the simulation are not verified by hardware implementation and testing

Chapter 8

Summary and Recommendations for Further Work

This thesis has focused on a detailed model of a MMC with proper control strategies suitable to interface energy storage to a AC grid using Matlab/Simulink simulations. The main objective was to investigate the system under various fault scenarios and locations. Several assumptions and simplifications have been made in order to meet the deadline of the thesis, hence the system dynamic response was investigated to ensure a sufficient operation.

8.1 Summary and Conclusions

As battery energy storage has been identified as the key enabling technology to integrate higher shares of renewable, intermittent power generation to the grid, the converter interfacing the battery to the grid has gained more attention. The MMC has been suggested as a well suited converter topology as it enables distributed energy storage and conventional low ratings semiconductors can be utilized. The simulation model is of a grid connected 1 MW MMC with battery storage on the common DC link. The grid is 33 kV and half-bridge SMs are implemented to achieve high efficiency and simpler control. No fault handling strategies is implemented to the model.

A MMC was designed and modeled in order to test for five different short circuit fault locations. The THD of the output AC current is 1.78 % when no faults are implemented. A step change in

power from 1 p.u. to -1 p.u. was applied to ensure that the design and simplifications made, was appropriate. As the response time was 230 ms it was concluded that the implementation of the MMC was sufficient.

To investigate if the MMC with five SMs is redundant, both the capacitor and then the terminals of one SM were short-circuited one by one. The two faults have similar behavior, except from the currents through the semiconductors in the faulty SM. When the short circuit fault happens at the capacitor side of the SM, the capacitor discharges through the fault, while the fault current goes through the diode and IGBTs without exceeding the current ratings. When the fault happens on the terminals, the capacitor discharges through the upper IGBT, thus it must be blocked immediately after the fault to prevent being damaged. The control system is able to control the AC currents, but the THD increases to 15.27 %. The capacitor voltage of each SM in the faulty arm increases to compensate for the faulty SM, hence the semiconductors must operate with higher voltages, leading to more frequent component failures. It is concluded that the MMC designed with five SMs is not redundant.

The importance of developing DC breakers with short response time was demonstrated as the upper converter arm on phase *a* was short-circuited. As this fault only includes one phase, the first post fault zero-crossing took place 190 ms after the fault occurred. As the AC breakers would not be able to break the current before that, large fault currents will damage the battery and converter valves. As all capacitor voltages of the upper arms become zero, the lower arm capacitors try to compensate for the upper arms by increasing the voltage to 6 kV, hence exceeding the blocking voltage of the transistors.

As the MMC with half-bridge SMs looses the control of it's currents as a DC fault occurs, the DC link terminals were short-circuited. A DC link short circuit fault results in a rapid discharge of all the capacitors, hence very high transients appear in the AC current. As the battery is modeled as an ideal voltage source, it will feed a 15 MA current to the fault demonstrating the importance of battery protection in the BMS. The arm-balancing control is not able to estimate the arm energies as the DC voltage is zero, hence the control system is not able to control the AC currents and the free-wheeling diodes act as rectifiers feeding large currents from the grid to the fault. As all three phases are included in the fault, the zero-crossing will happen faster than for Fault 3, thus the AC breakers can be turned after 22 ms, which is equivalent to one fundamental cycle. Thus, the AC breakers are able to isolate the MMC before the large fault current damages any components.

The most critical fault in terms of AC voltage is the line-to-lone fault, where the phase *b* and *c* voltage become equal, hence there is no longer a balanced three phase signal. As a result the control based on the *dq*-reference frame is not working and no control over the currents is obtained. Large fault currents and capacitor voltages will damage all the semiconductors in the converter, if the converter is not isolated from the grid. This fault has the fastest occurrence of the zero-crossing of the AC current, hence AC breakers are sufficient to prevent damage from the fault currents.

Since DC circuit breakers are not yet available, the short circuit faults across one converter arm and over the DC link are identified as the most critical faults, thus the importance of developing fast-acting DC circuit breakers are stressed.

8.2 Further work

This study should be continued with a more detailed battery model that includes SOC control and battery protection algorithms. The batteries should be placed inside the SMs in order to see how it would effect the fault currents. The results from the battery at the DC link and inside the SMs should be compared to verify that distributed energy storage is the best choice for this application. IGBT blocking capability and AC breakers can be implemented to achieve more realistic results, as the converter should not be able to operate with high currents feeding the faults, as in the results of this thesis.

The 7 kV AC grid model should be connected to the PPC through a Δ-Y transformer to investigate the effect on the zero sequence currents during asymmetrical faults. The positive and negative sequence currents can then be controlled by two separate control systems, as was mentioned earlier in the thesis.

The complete system included the WECS and grid should be built in order to see how the energy storage and MMC will co-operate during regular operation and under fault conditions. How the battery is able to compensate for the intermittent nature of the wind power generation should be investigated, hence it will be known if the design system is sufficiently designed for the given application.

Full-bridge SM configuration can be applied to compare to the results from this thesis. The

improvements in operations should then be weighed up against the increased costs. In addition, the new hybrid MMC with a combination of half-bridge and full-bridge SMs suggested in [10] could be investigated, as it claims to provide DC fault ride through capabilities with no additional costs.

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Appendix A

Additional figures

A.1 Control System

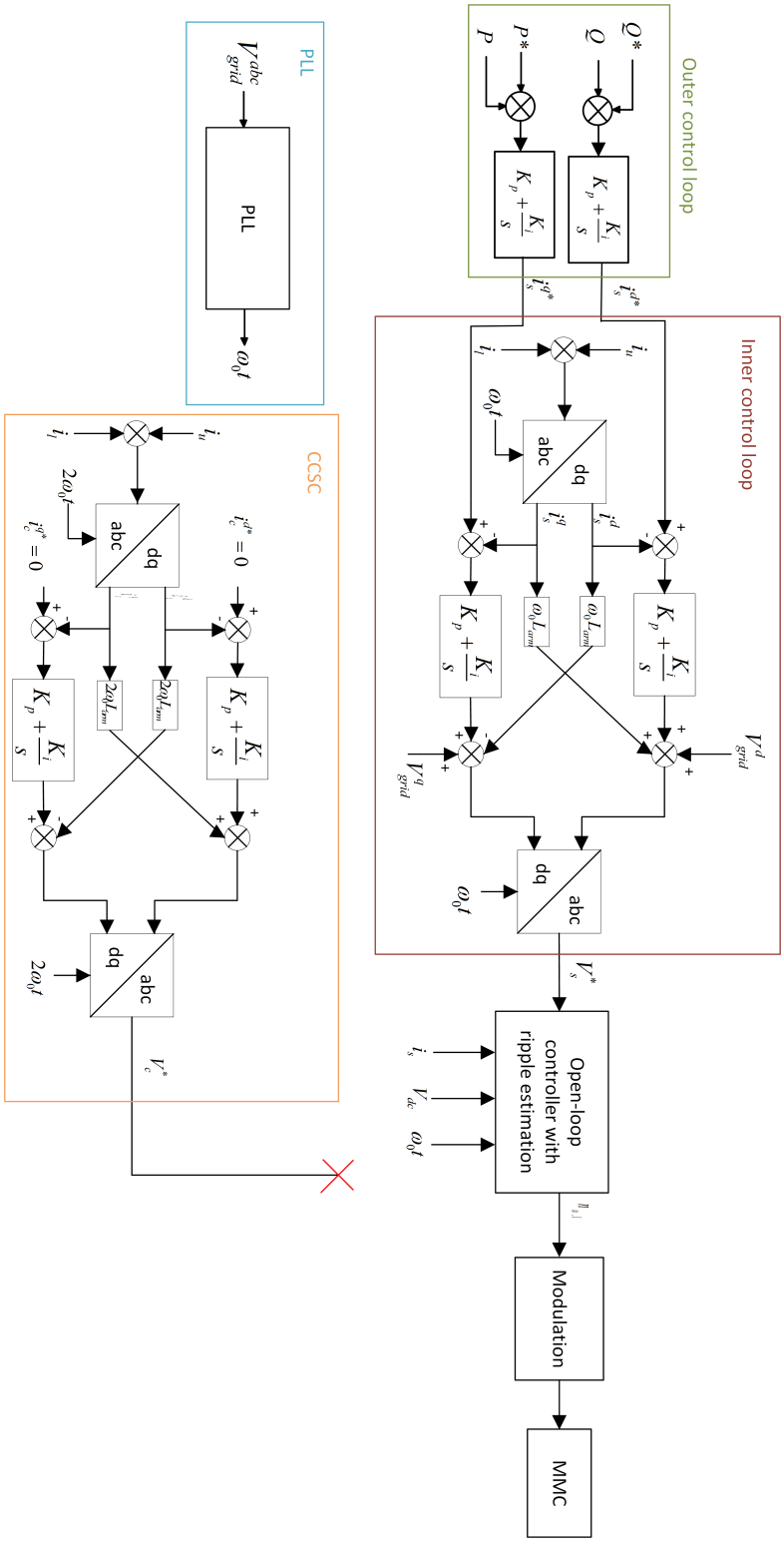

Figure A.1: Block diagram of the full control system designed for the MMC investigated

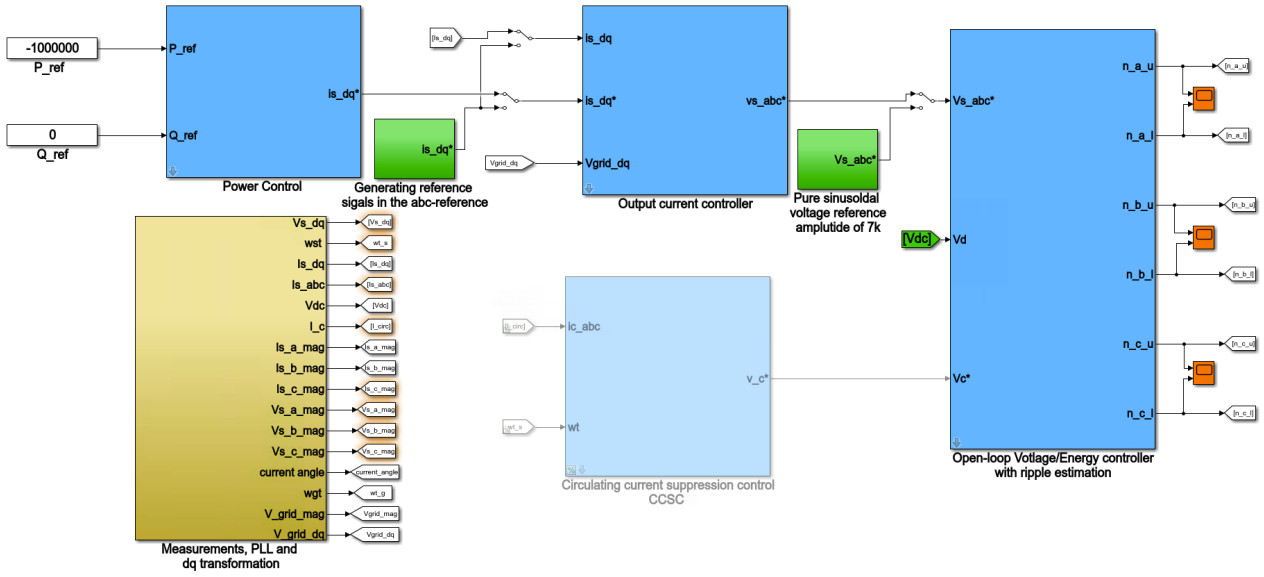

Figure A.2: The full control system implemented in Simulink

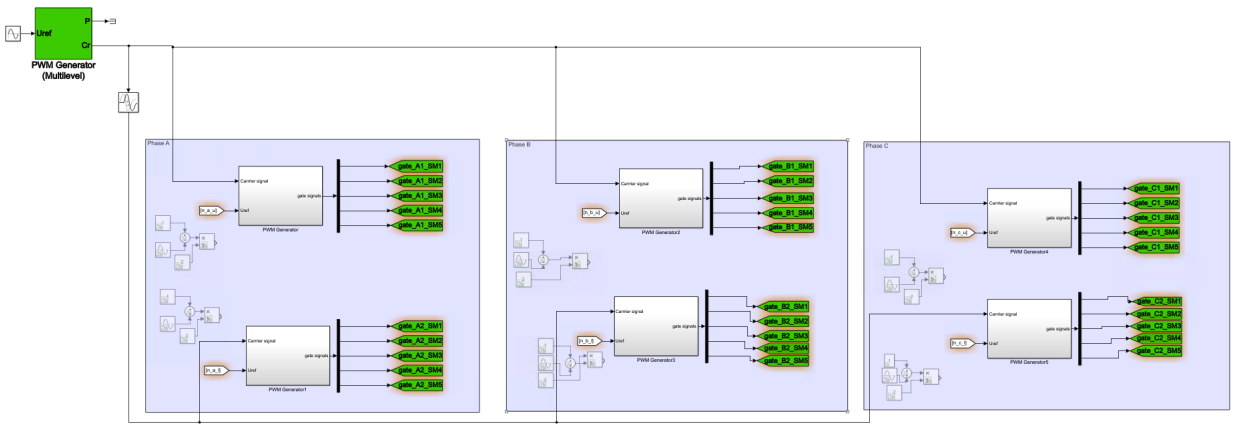

Figure A.3: The PWM for each leg in all three phases implemented in Simulink

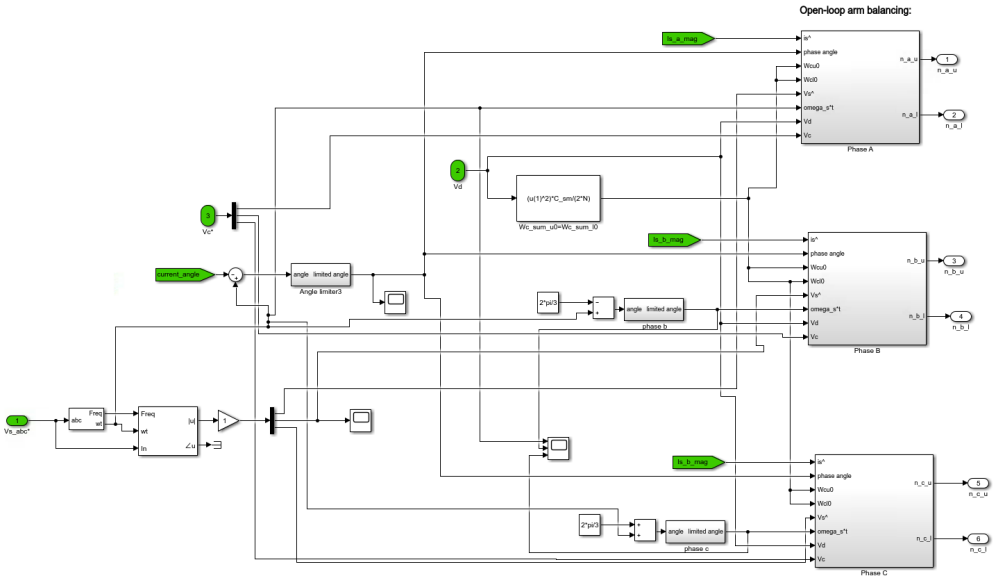

Figure A.4: Parameter deviation for the open-loop voltage/energy controller with ripple estimation

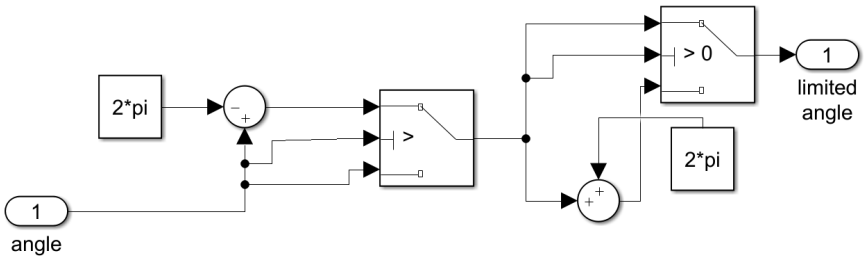

Figure A.5: Angle limiter block

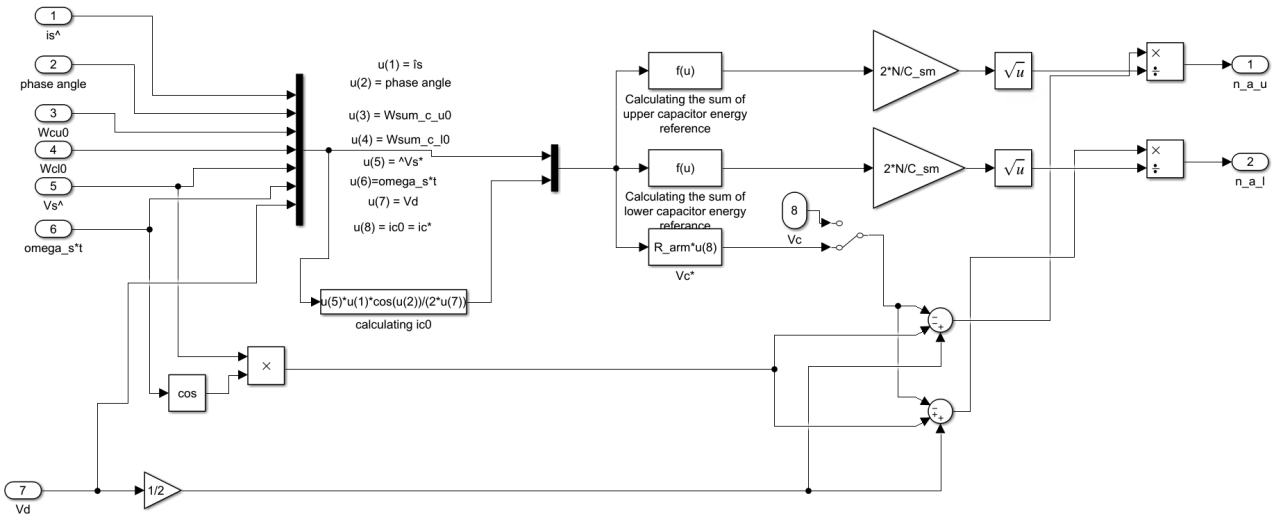

Figure A.6: The arm energy balancing control with arm energy estimation for each phase

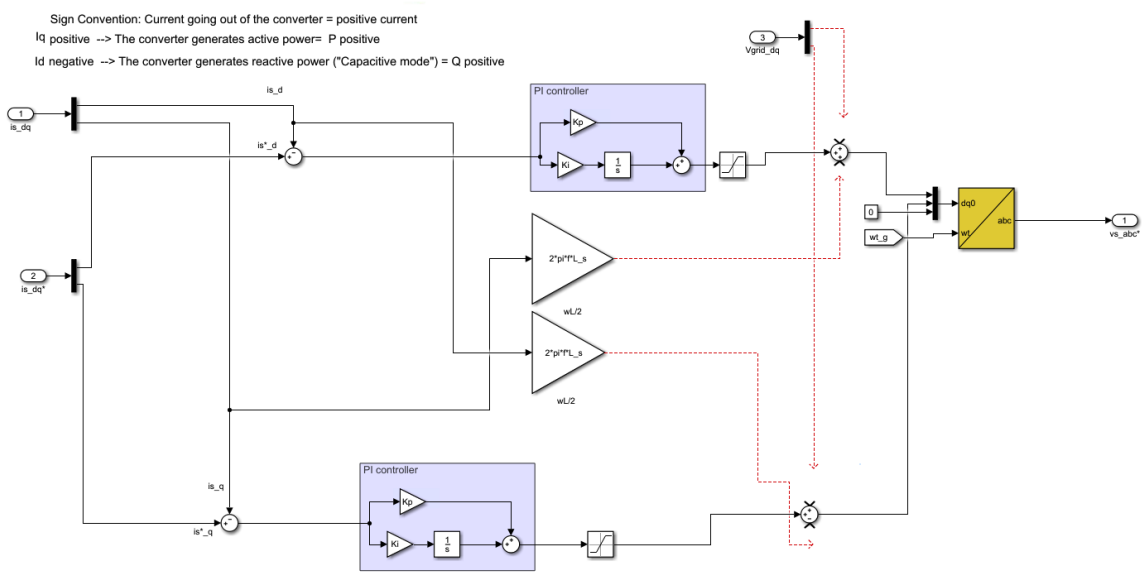

Figure A.7: The PI current controller in the *dq*-reference frame implemented in Simulink

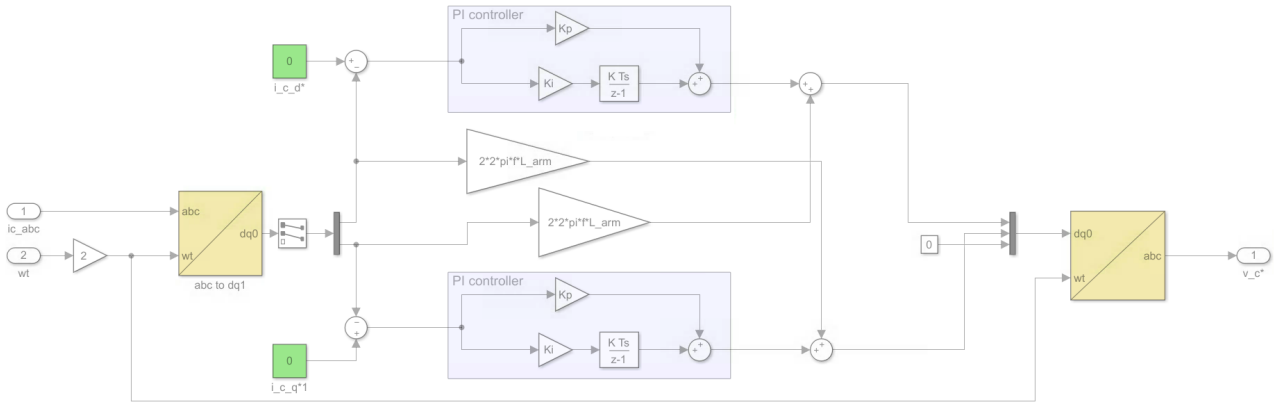

Figure A.8: The PI-CCSC in the *dq*-reference frame implemented in Simulink

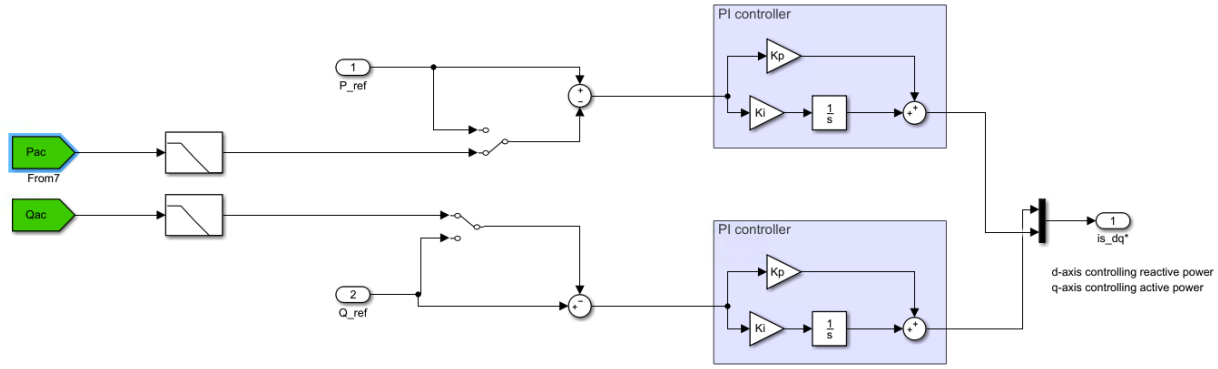

Figure A.9: The PI power controller implemented in Simulink

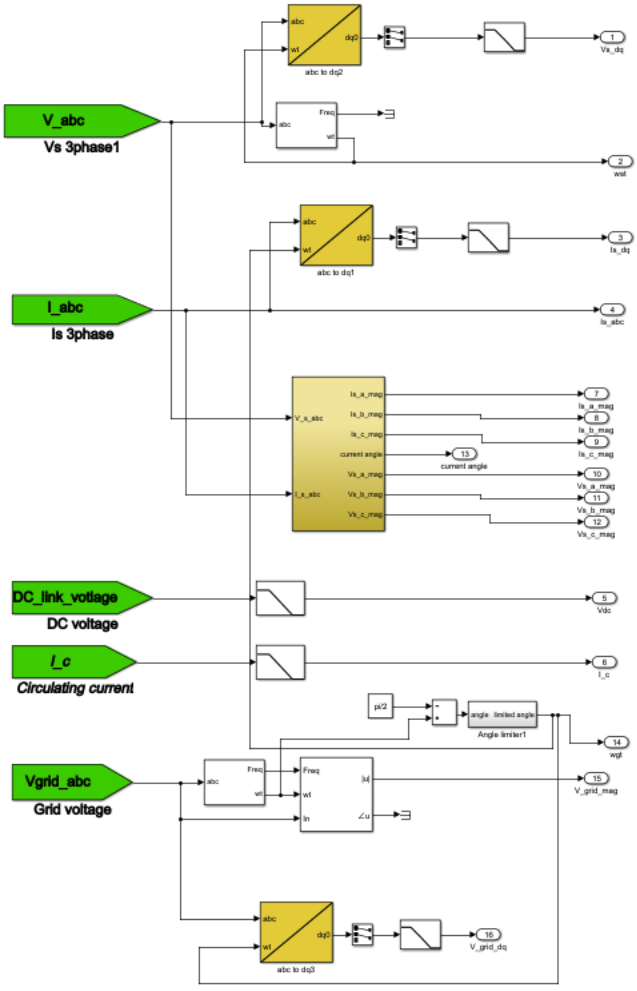

Figure A.10: Measurement, PLL and *dq*-transformation block

A.2 Electrical system in Simulink

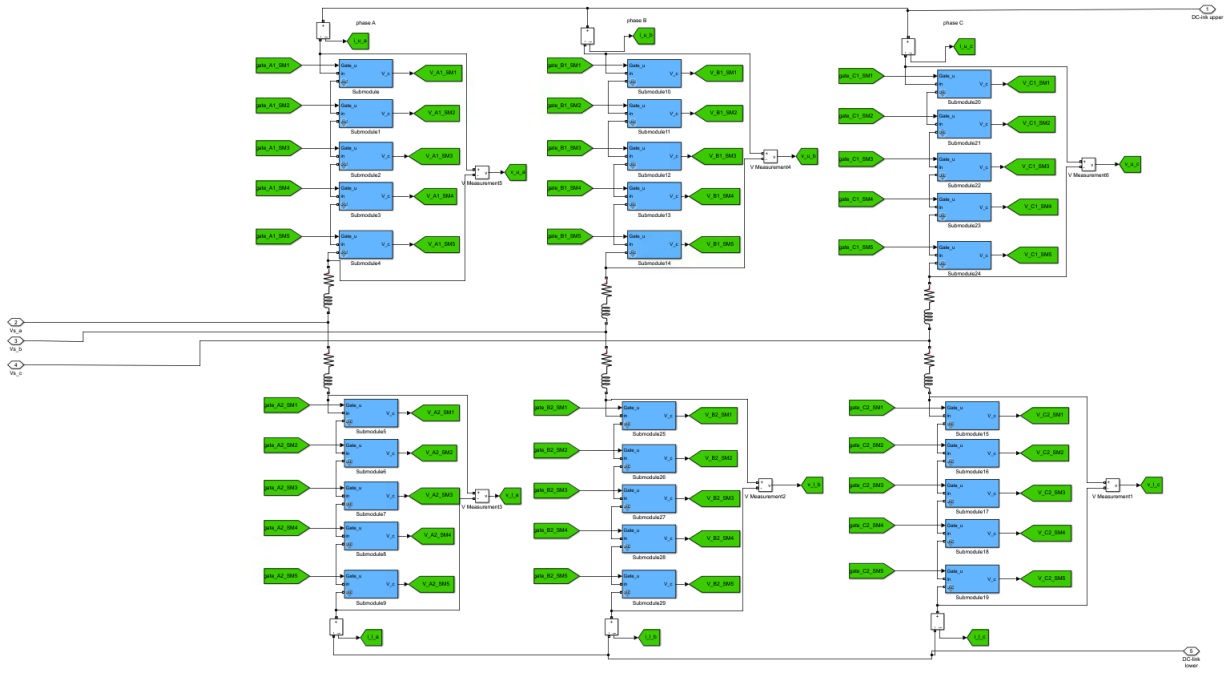

Figure A.11: The MMC model built in Simulink with 5 SMs

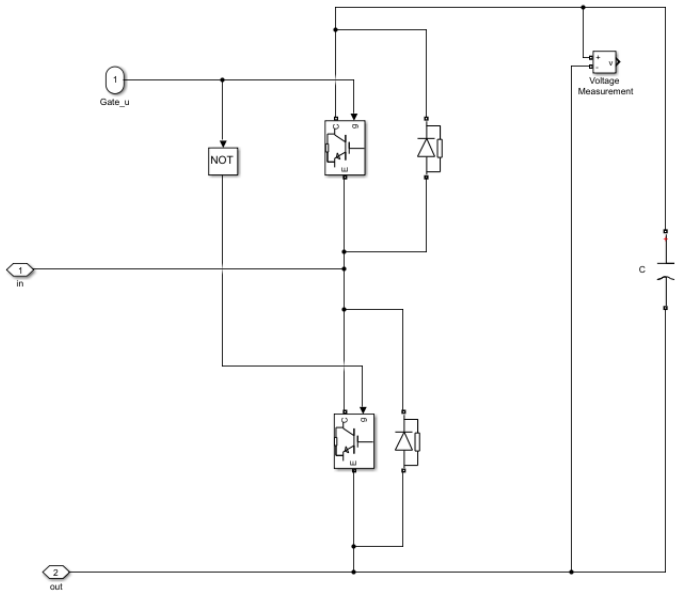

Figure A.12: The submodule model built in Simulink with IGBT and free-wheeling diode

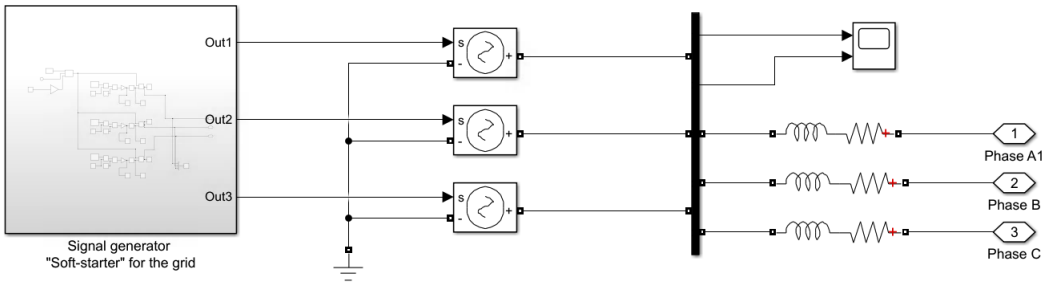

Figure A.13: The grid modeled as three controllable voltage sources and a soft-starter

A.3 Results reference case

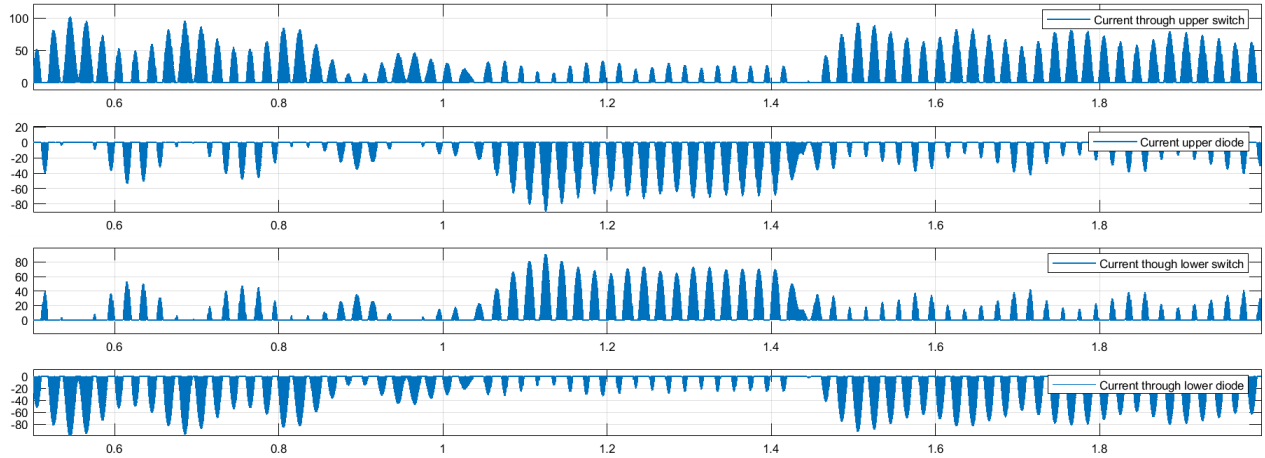

Figure A.14: Currents though the devices in a SM during the reference case

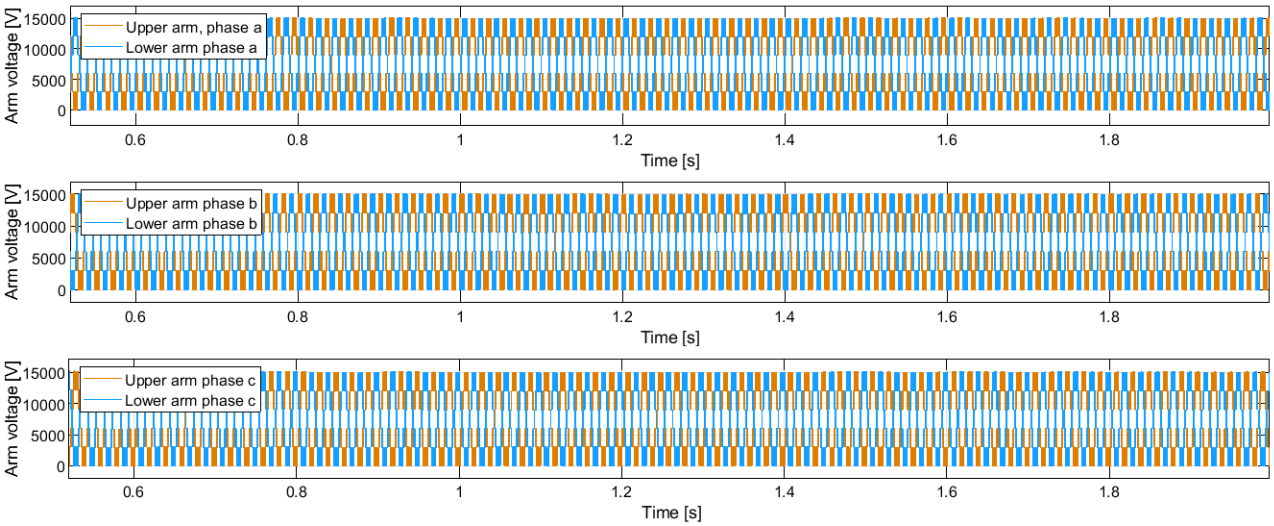

Figure A.15: Arm voltages during the reference case

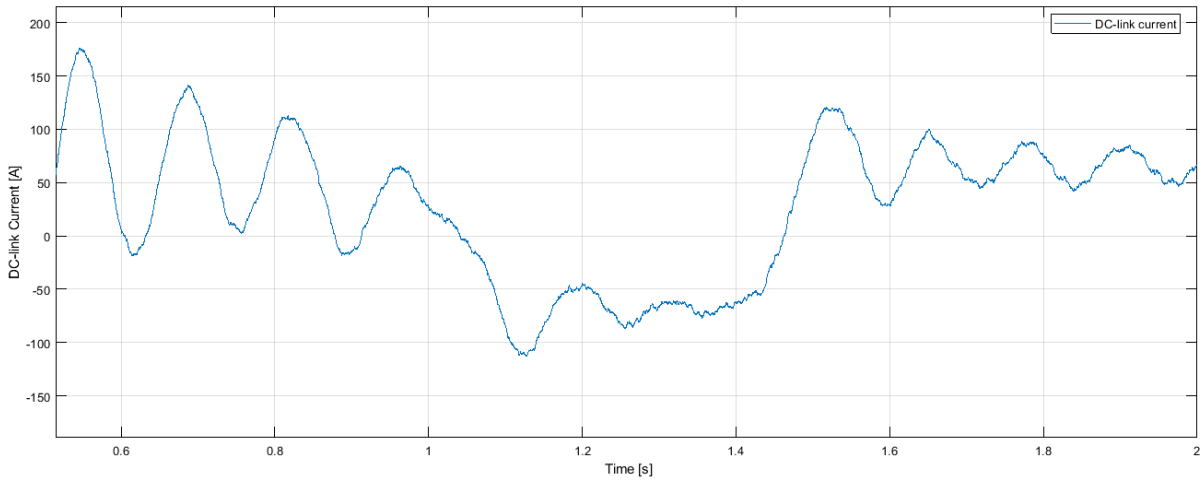

Figure A.16: The DC current during the reference case

A.4 Results fault 1 and 2

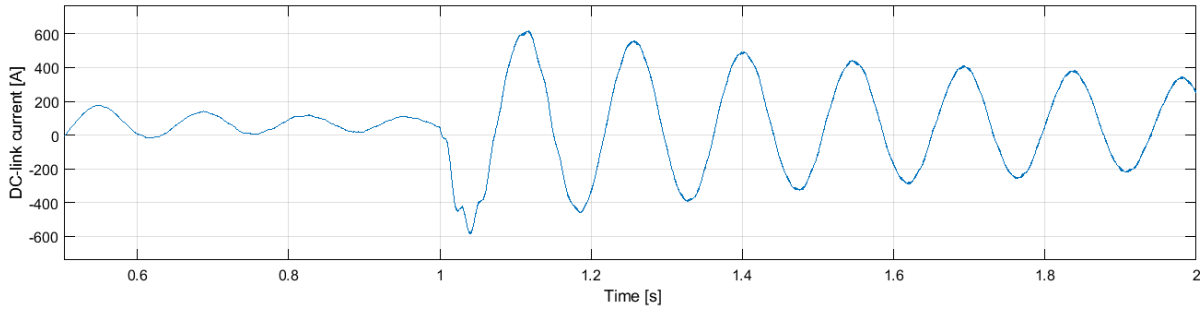

Figure A.17: The DC current during fault 1 and 2

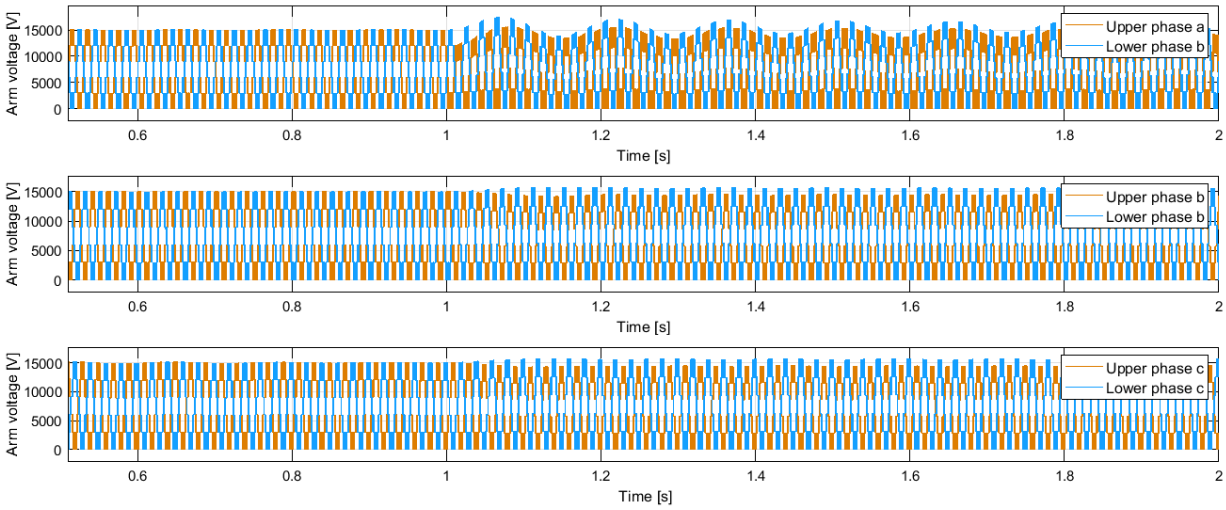

Figure A.18: The arm voltages during fault 1 and 2

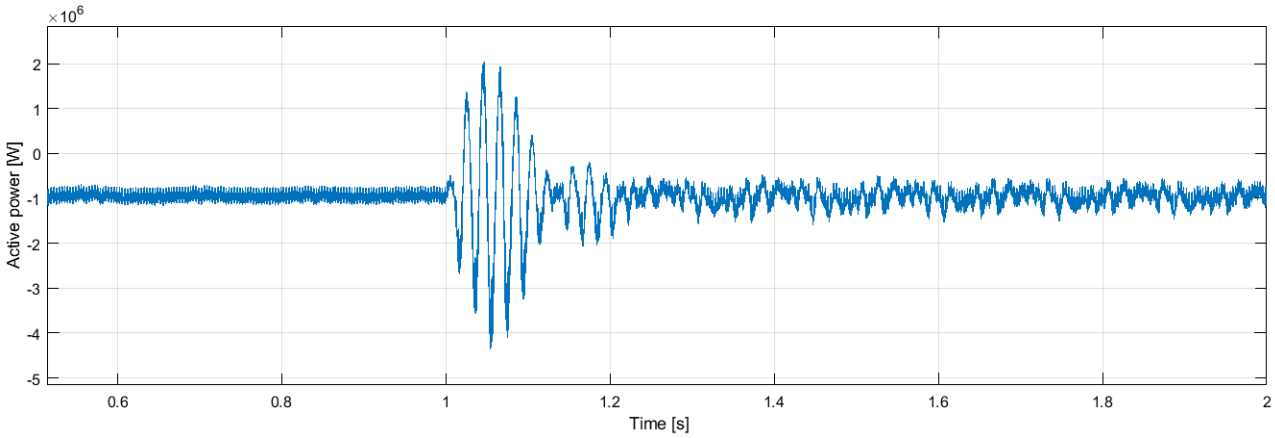

Figure A.19: The active power during fault 1 and 2

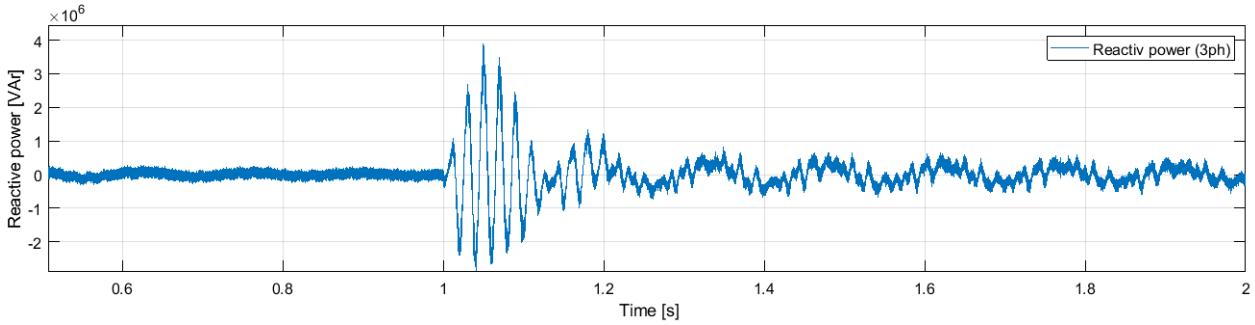

Figure A.20: The reactive power during fault 1 and 2

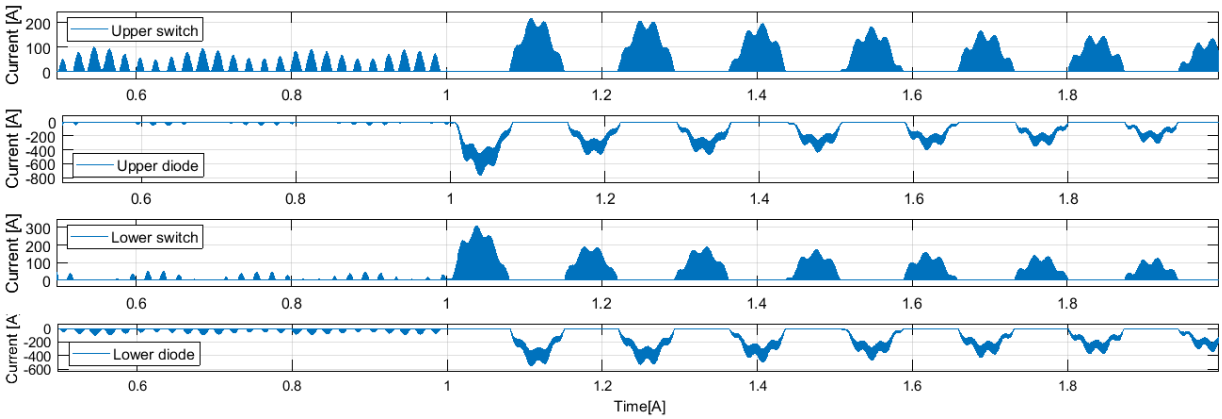

Figure A.21: Currents though the devices in the faulty SM during fault 1

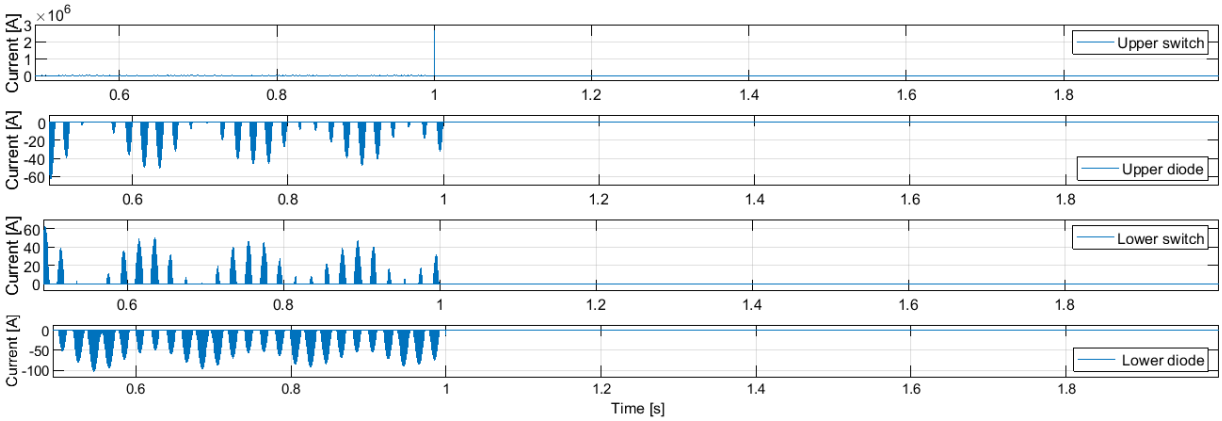

Figure A.22: Currents though the devices in the faulty SM during fault 2

A.5 Results fault 3

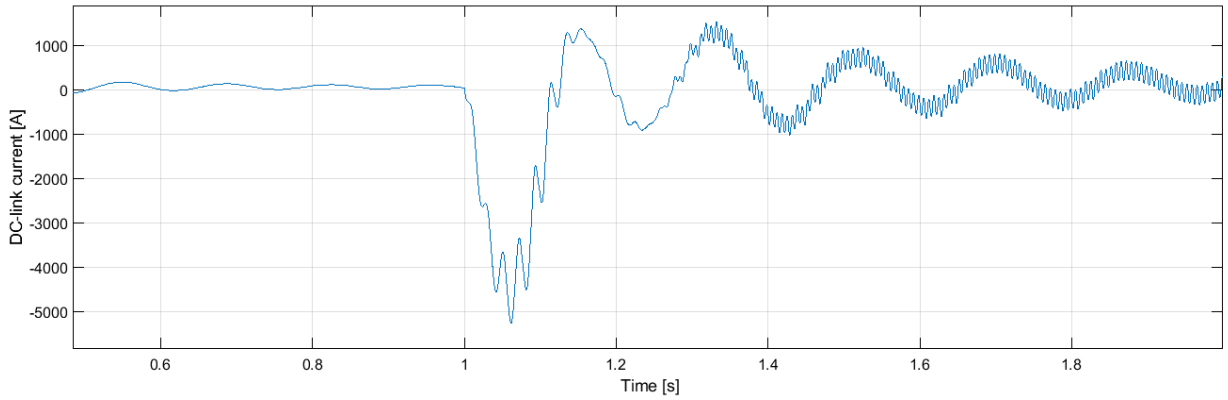

Figure A.23: The DC current during fault 3

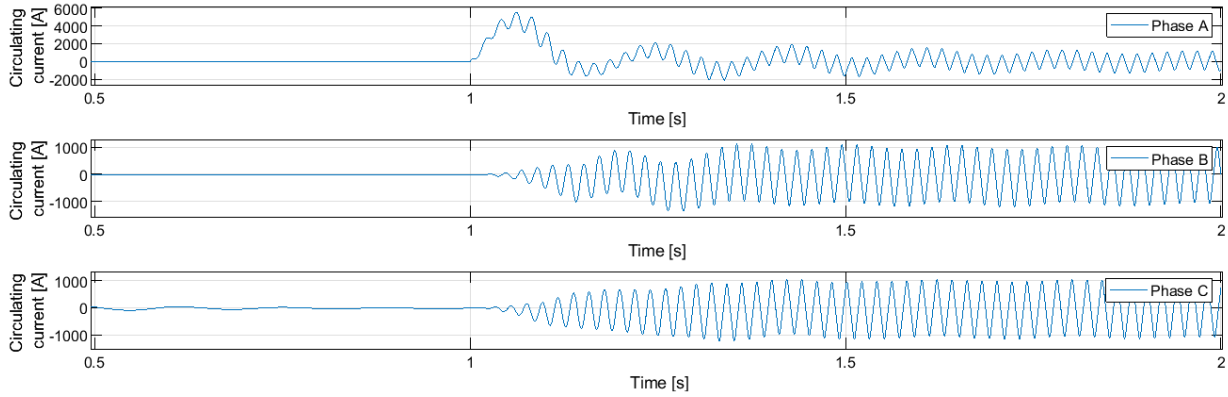

Figure A.24: The circulating current during fault 3

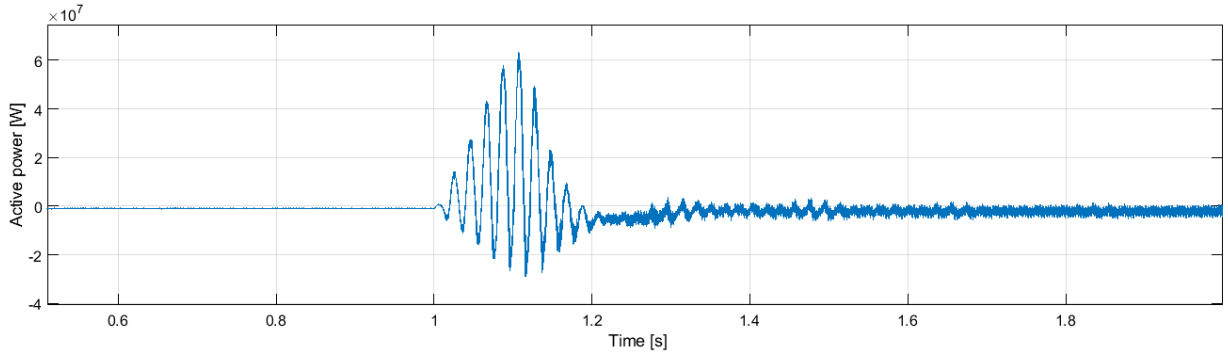

Figure A.25: The active power during fault 3

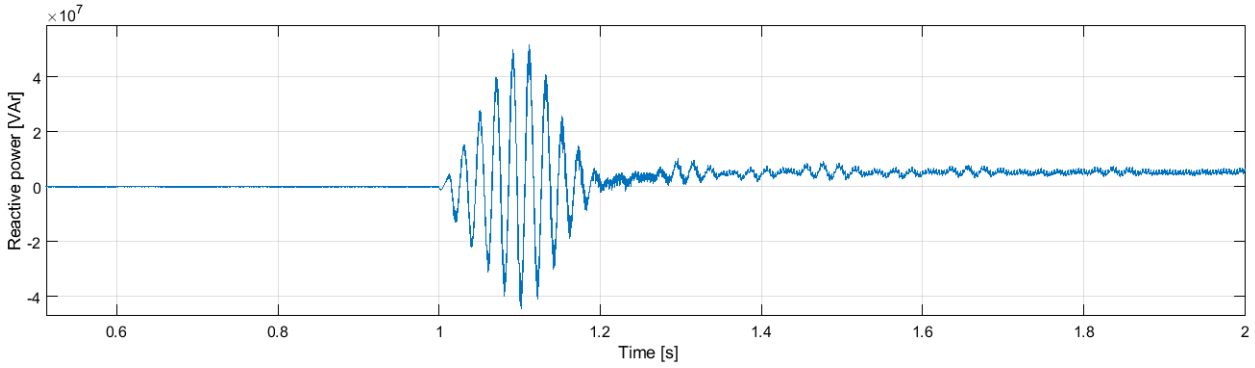

Figure A.26: The reactive power during fault 3

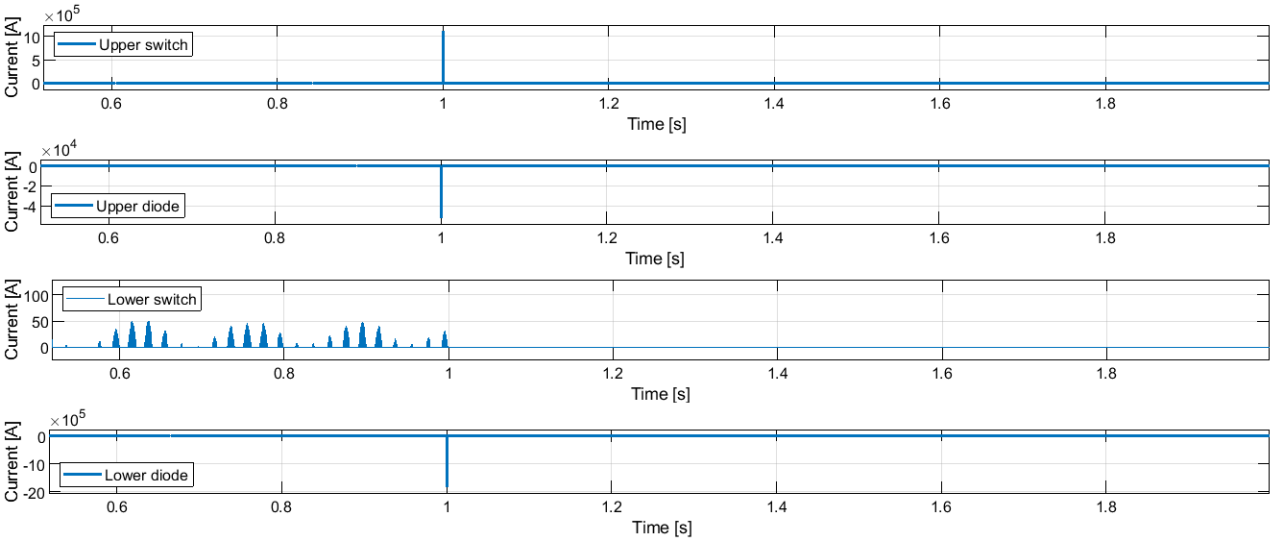

Figure A.27: Currents though the devices in a SM at the faulty arm during fault 3

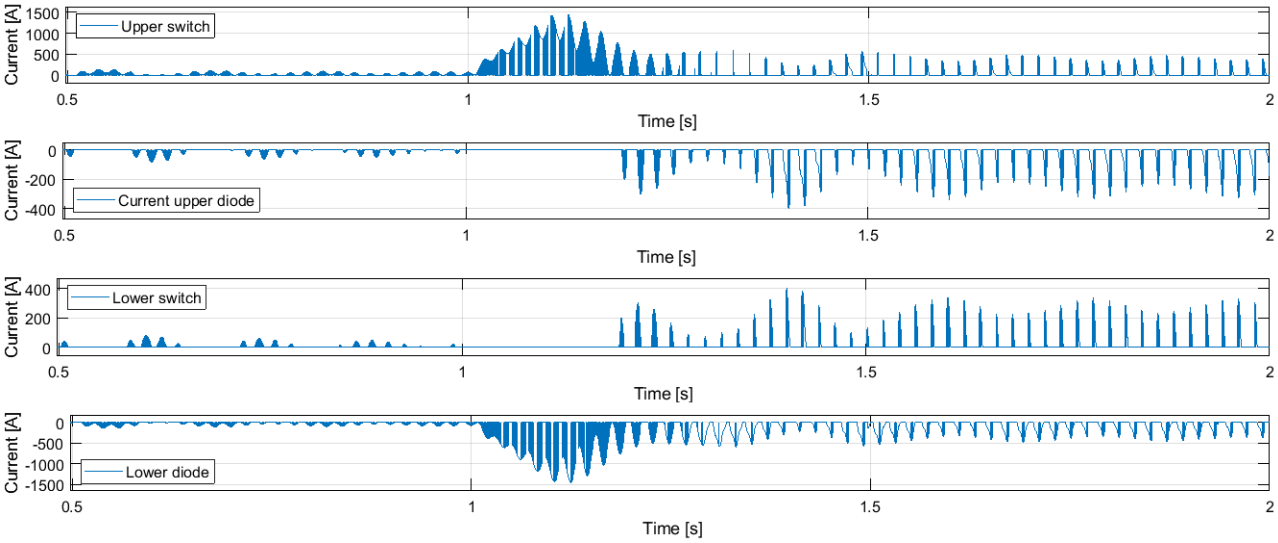

Figure A.28: Currents though the devices in a SM at the upper arm of phase b and c during fault 3

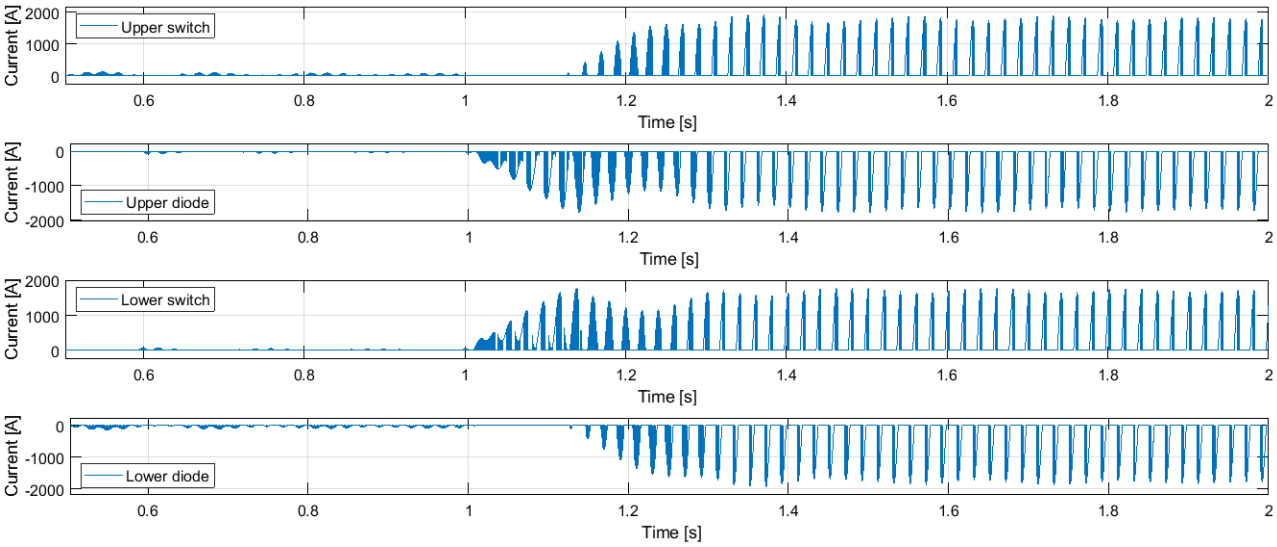

Figure A.29: Currents though the devices in a SM at the lower arms during fault 3

A.6 Results fault 4

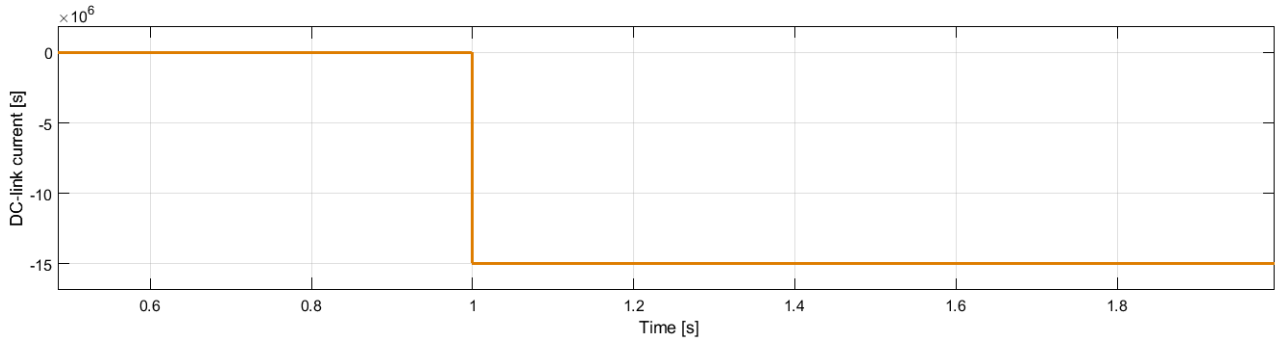

Figure A.30: The DC current during fault 4

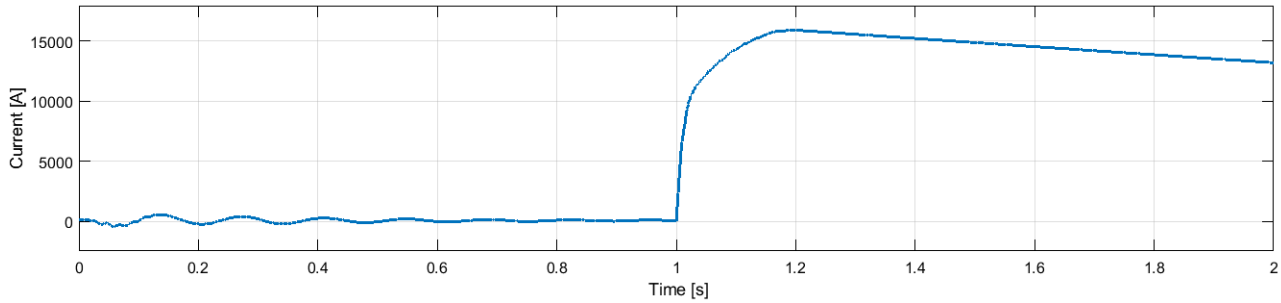

Figure A.31: The current out of the MMC into the fault during fault 4

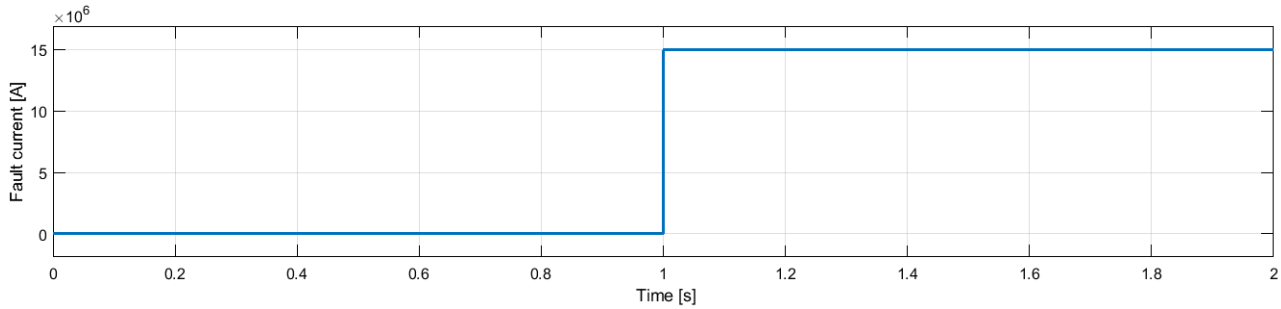

Figure A.32: The fault current during fault 4

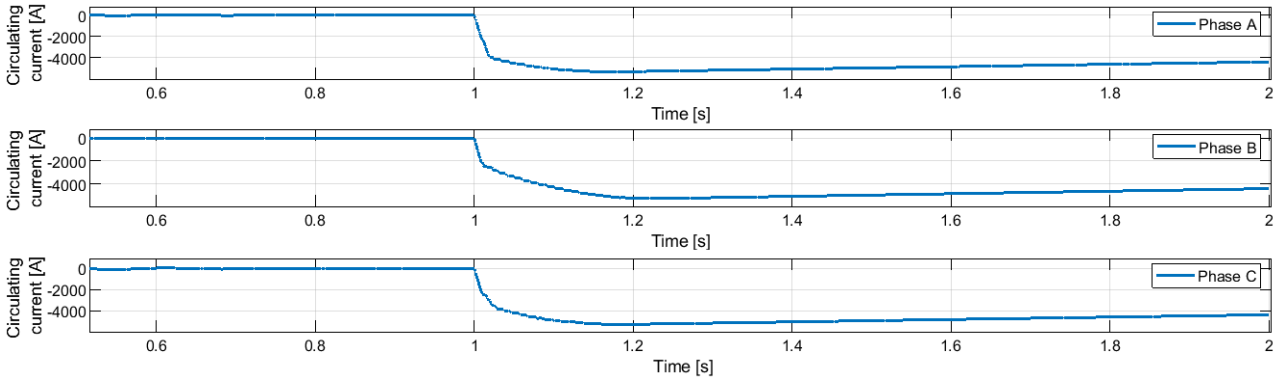

Figure A.33: The circulating current during fault 4

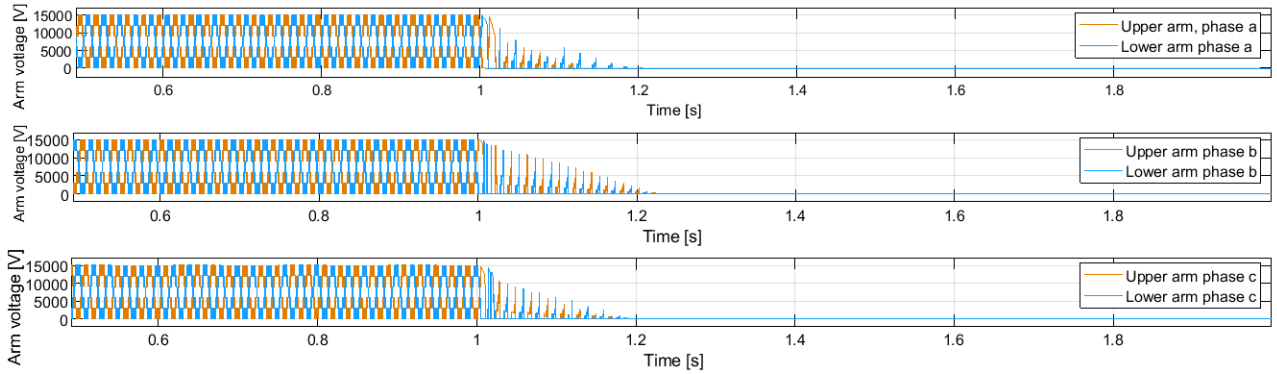

Figure A.34: The arm voltages during fault 4

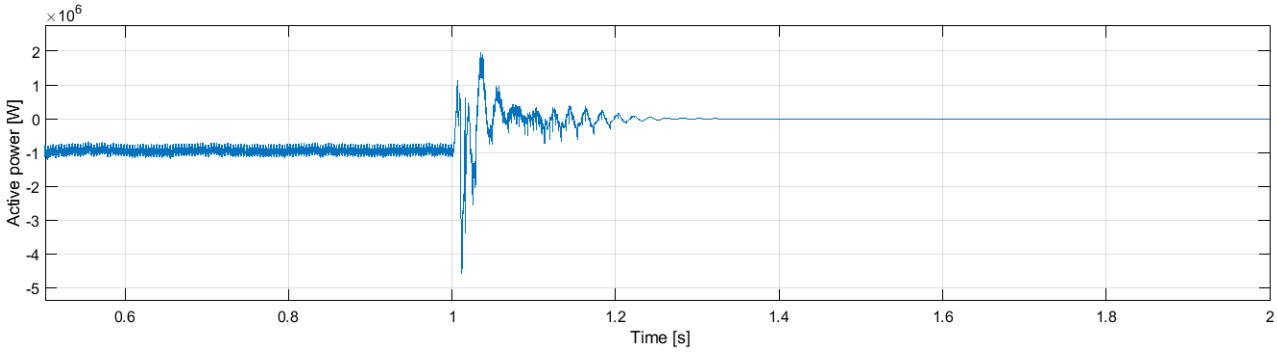

Figure A.35: The active power during fault 4

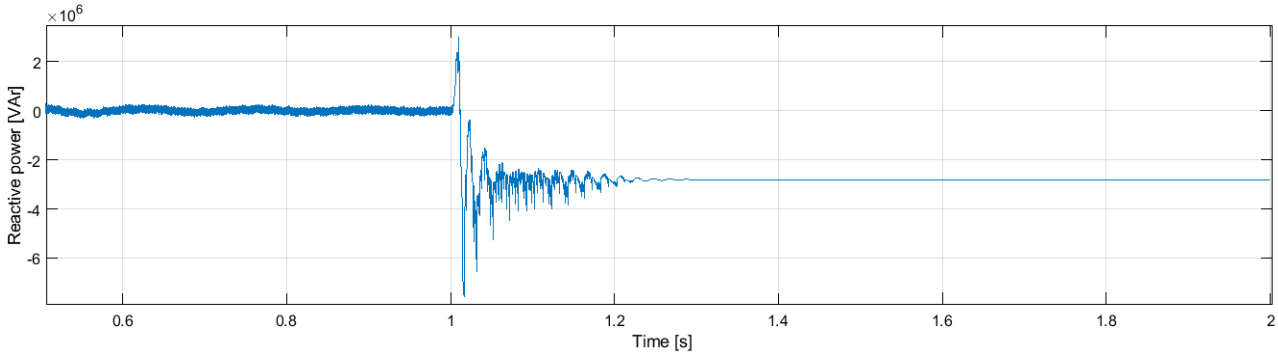

Figure A.36: The reactive power during fault 4

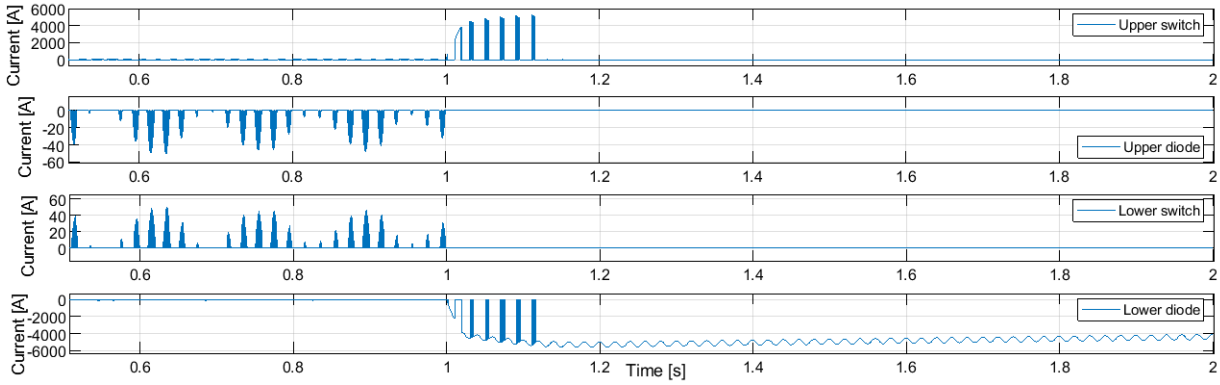

Figure A.37: Currents though the devices in the SMs during fault 4

A.7 Results fault 5

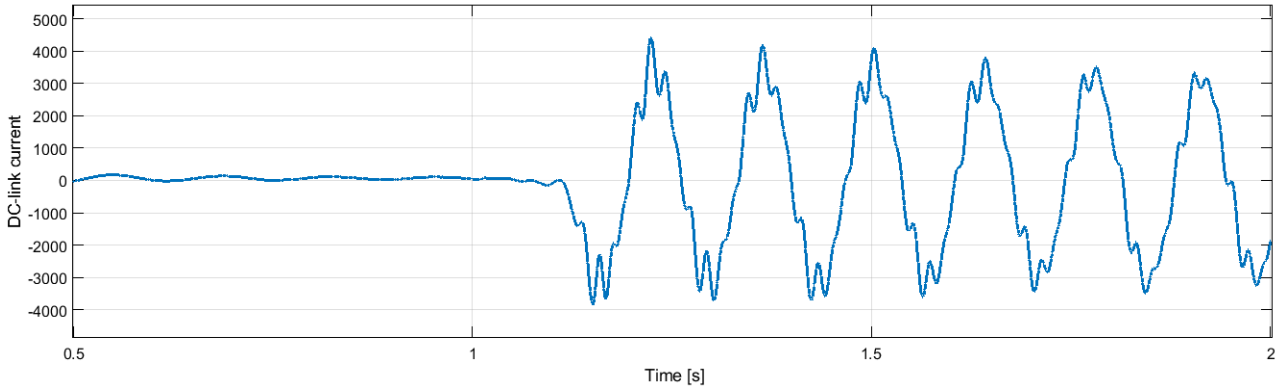

Figure A.38: The DC current during fault 5

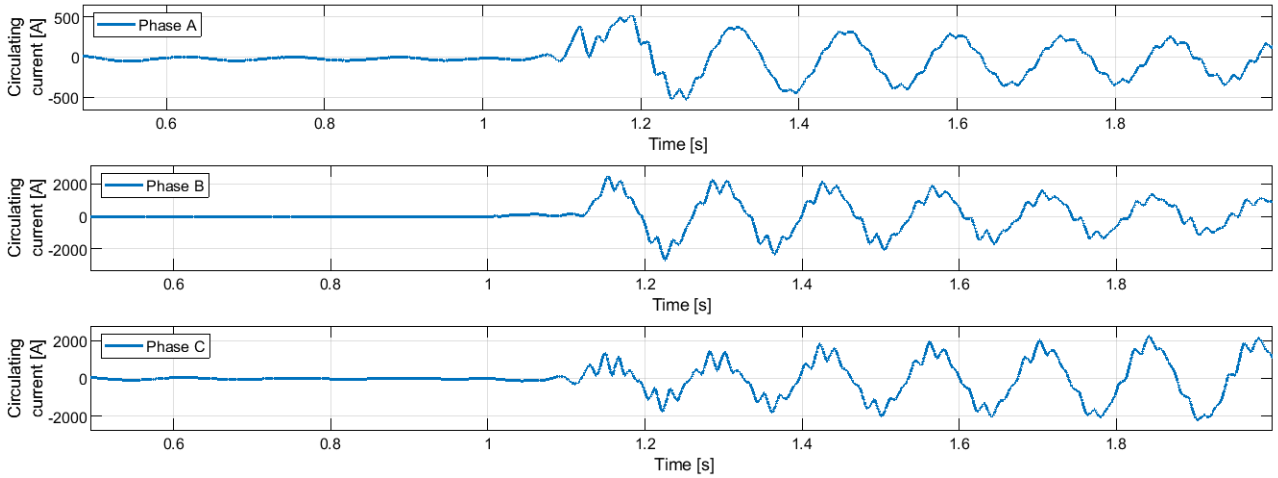

Figure A.39: The circulating current during fault 5

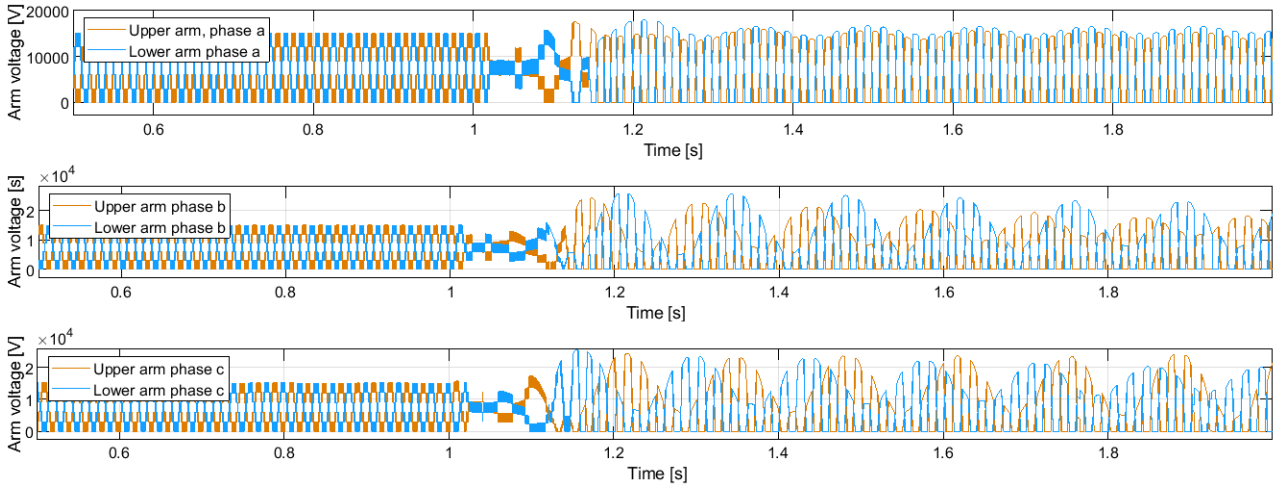

Figure A.40: The arm voltages during fault 5

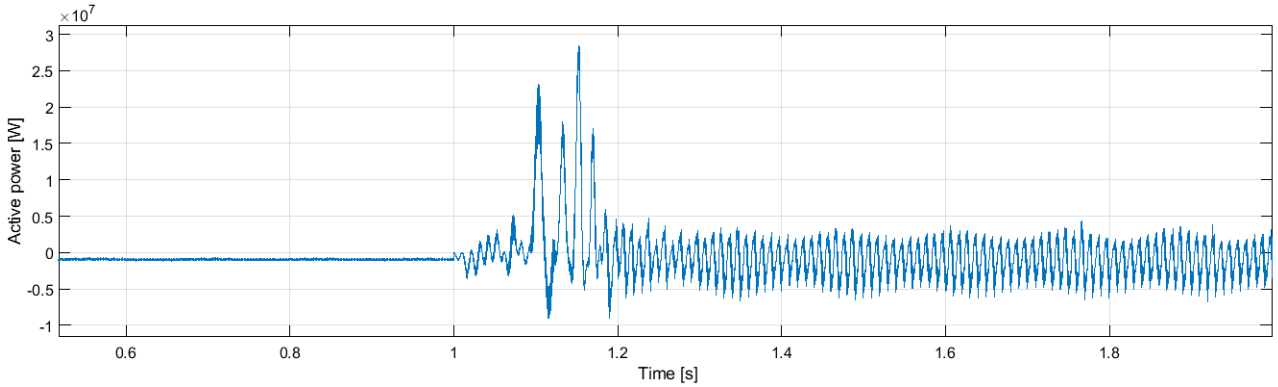

Figure A.41: The active power during fault 5

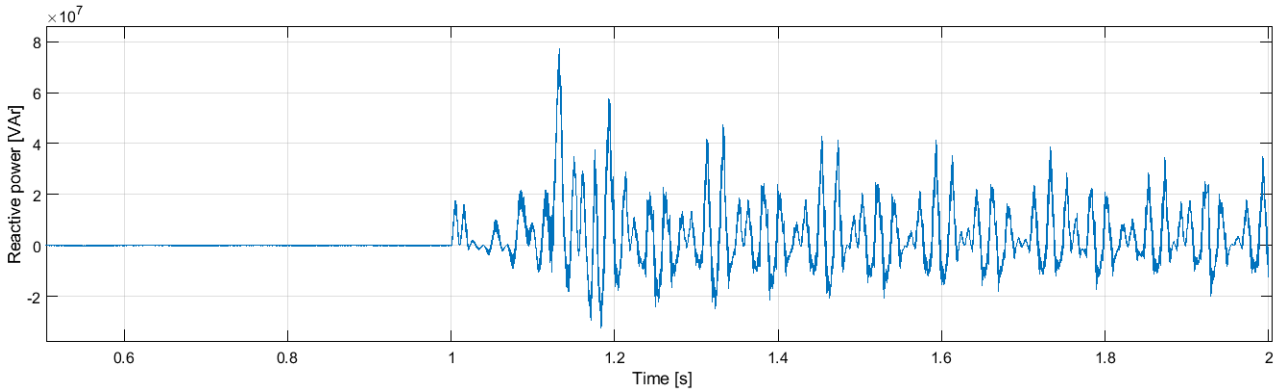

Figure A.42: The reactive power during fault 5

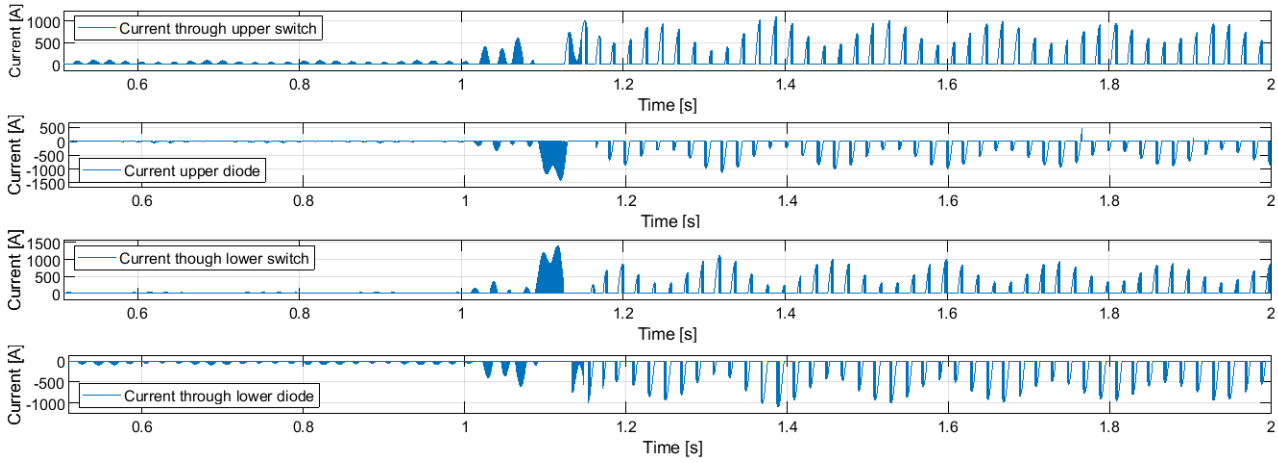

Figure A.43: Currents though the devices in the phase *a* SMs during fault 5

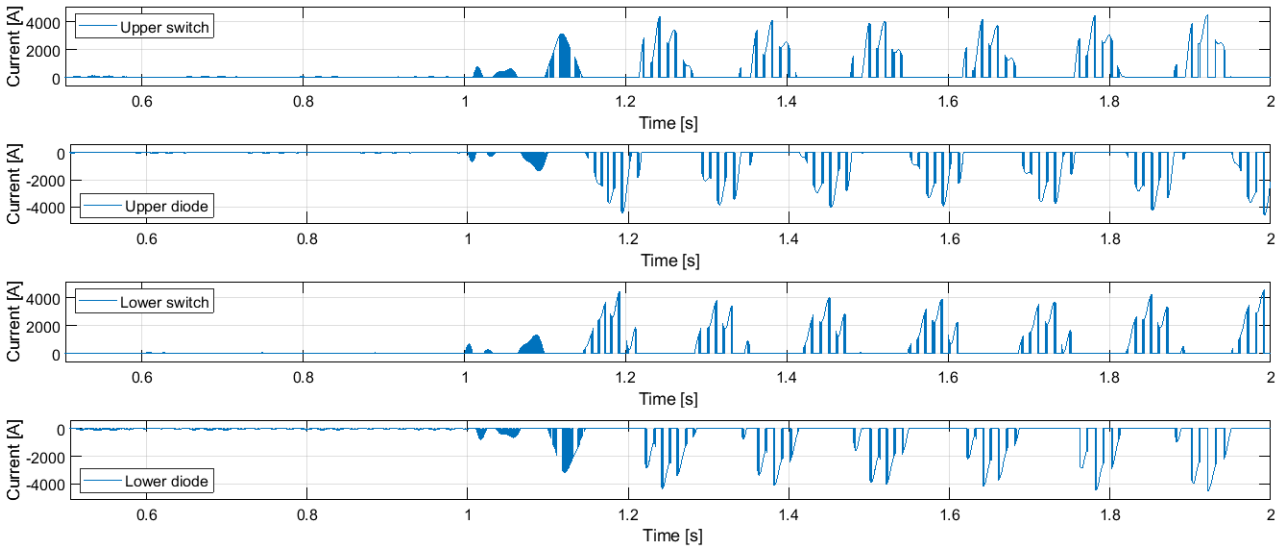

Figure A.44: Currents though the devices in the phase *b* and *c* SMs during fault 5

Appendix B

Additional information

B.1 Matlab script for model initialization

```
%Initializatoin file for MMC model
clc;
clear;

%Ratings
f = 50; %Hz
N=5;
P_n = 1000000; % W
V_s_n = 7000; %V
V_dc=15000;
f_carrier=1068.5;
V_bat = 15000/N;
T_s=10e-6; %Sampling time

%% MMC Parameters
L_arm=30e-3;
R_arm = 0;
C_sm=20e-3;

```

```
L_line=2e-2;
R_line=1;

L_s=L_line+(L_arm/2);
R_s=R_line+(R_arm/2);

%% Power Semiconductor parameters
%IGBT
IGBT_r_on = 1/1400; % ohms
IGBT_l_ind = 0; % H
IGBT_V_f = 3; % V
IGBT_R_s = 5e6; % snubber resistance (ohm)
IGBT_C_s = 5e-9; %snubber capacitance (F)

%diode
diode_r_on = 0.47e-3; %ohm
diode_l_ind = 0; % H
diode_V_f = 3; % V
diode_R_s = 5e6; % snubber resistance (ohm)
diode_C_s = 5e-9; %snubber capacitance (F)

%% PI output current controller
% calculated using modulus optimum
T_d=0.5/f_carrier;
T_pi_is=L_s/R_s;
Kp_is=T_pi_is/(2*T_d);
Ki_is=Kp_is/T_pi_is;

%% PI power controller
% calculated using symmetrical optimum
Kp_power=2/(3*V_dc);
Teq=50e-3; %time delay of current controller (++)
Ti_power=2^2*Teq;
Ki_power=Kp_power/Ti_power;
```