Practical Thermal and Electrical Parameter Extraction Methods for Modelling HBT's, and their Applications in Power Amplifiers

by

Morten Olavsbråten

A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor Ingeniør

2002

Report no.: 420302
Department of Telecommunications
Norwegian University of Science and Technology
N-7491 Trondheim, Norway

URN:NBN:no-3376

Norwegian University of Science and Technology
Department of Telecommunications
N-7491 Trondheim, Norway

Doktor ingeniøravhandling 2003:20
Report no.: 420302

ISBN 82-471-5568-0
ISSN 0809-103X

URN:NBN:no-3376

Abstract

In Chapter 3, a new practical technique for estimating the junction temperature and the thermal resistance of an HBT was developed. This technique has been published by the author in 2002 [5], and can be found in Appendix A.1. The new technique estimates an interval for the junction temperature. The main assumption in the new technique is that the junction temperature can be calculated from three separate phenomena:

- Thermal conduction of the substrate.
- Thermal conduction of the metal connecting the emitter to the via holes.
- The effects of the via holes on the substrate temperature.

The main features of the new technique are:

- The junction temperature and the thermal resistance are calculated from a few physical properties and the layout of the transistors.
- The only required software tool is a mathematical program like MATLAB.
- The calculation time is very short compared to a full 3D thermal simulation.
- The technique is easy to use for the circuit designer.
- The technique has good accuracy.

The new technique shows good accuracy, when applied to several InGaP/GaAs HBT's from Caswell Technology, and compared to the results from other methods in [3, 4]. All the results presented in [3, 4] fall well within the estimated junction temperature intervals from the new technique, except for the 4x40C transistor evaluated at 85 °C, where the result is just outside the estimated interval. As an

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example of results from the new technique, the estimated junction temperature increase - relative to the ambient temperature - for the P4x40C is calculated to be T_j = [62.9, 81.3] °C. In [3, 4] the junction temperature increase is found using two different techniques which give T_j = 71.8 °C and T_j = 80.3 °C. These results are all found for a dissipated power of 0.4 W at an ambient temperature of 25 °C.

A simple method for estimating the thermal capacitance was also developed. This method was applied to the 1x40C transistor giving an $C_{TH} = 1.4 \cdot 10^{-9}$ J/K. Using the thermal resistance R_{TH} = 380 K/W from Table 3.6, the thermal time constant becomes τ_{TH} = 0.53 µs. Caswell Technology reports the thermal time constant to be somewhat smaller than 1 µs. From this the method can be assumed to have good accuracy.

In Chapter 4, an overview of the modelling concepts is given. Based on several requirements the VBIC model was chosen for all the practical modelling. An overview of all the parameters associated with VBIC model is given together with an explanation on how to find values for these parameters. From this, a practical parameter extraction method for the VBIC model was developed. This method is the first published practical parameter extraction technique for the VBIC model used on an InGaP/GaAs HBT, as far as the author knows. The method was published by the author in 2000 [6], and can be found in Appendix A.2.

The main features of the extraction method are:

- Only a few common measurements are needed (forward Gummel, reverse Gummel, IV, cold capacitor s-parameter, active s-parameter measurements).
- Easy and practical to use for the circuit designer.
- Good accuracy with only a few iterations.
- No expensive and specialized parameter extraction software is required. The only software needed is a circuit simulator (and MATLAB to get a good set of start values).

The method includes the extraction of the bias dependent forward transit time. The parameter extraction and an evaluation of the transit time implementation in the VBIC model were published by the author in 2001 [7], and can be found in Appendix A.3.

The extraction method was evaluated on a single finger, 1x40, InGaP/GaAs HBT from Caswell Technology. Only four iterations were required to fit the measurements very well. There is less than 1 % error in both the I_C-V_{CE} and V_{BE}-V_{CE} plots in Figure 4.12 and 4.13. At I_c = 20 mA and V_{ce} = [2, 3, 5] V, S_{21} and S_{12} have the largest error. The maximum magnitude and phase error in the whole frequency range up to 40 GHz are less than 1.5 dB and 15 degrees.

This chapter also includes measurements and modelling of SiGe HBT's. Models for a single finger and a 8-finger transistor were extracted. All the dc characteristics of the modelled transistors have less than 3.5 % error. Some amplitude and phase errors are observed in the s-parameters, especially for the single finger. The errors are

caused by uncertainties in the calibration due to a worn calibration substrate, high temperature drift during the measurements, and uncertainties in the physical dimensions/properties caused by lack of information from the foundry. Overall, the extracted models fit the measurements quite well.

In Chapter 5 a very linear class A power amplifier has been designed using the InGaP/GaAs HBT's from Caswell technology. The thermal junction estimation technique developed in Chapter 3 has been used to make a very good thermal layout of the power amplifier. The estimated average junction temperature is 98.6 °C above the ambient temperature, calculated with a total dissipated power of 6.4 W at an ambient temperature of 45 °C. The maximum junction temperature difference between the transistor fingers is less than 11 °C.

The estimated thermal resistance of each finger was used in the VBIC model extracted in Chapter 4.

The PA was constructed with a 'bus bar' power combinder at both input and output, and optimized for maximum gain with a 10 % bandwidth. The PA had a small signal transducer power gain of 15.3 dB and a maximum output power of 34.8 dBm. The 1 dB compression point was simulated to be 34.5 dBm, and the third order intercept point was 49.9 dBm. At 33 dBm output power the PAE was 27.2 %, the gain compression was 0.285 dB and the phase error -0.728 degrees. The PA was unconditionally stable for all frequencies above 100 MHz.

The bias circuits must be included for a complete stability analysis at low frequencies. In a complete stability analysis of a PA, the 'bus bar' should be analysed in a 2.5D simulator. This has not been performed here.

URN:NBN:no-3376

Acknowledgement

This thesis is submitted in partial fulfilment of the requirements for the degree *Doctor Ingeniør* (Dr.Ing) at the Norwegian University of Science and Technology (NTNU). The research have been carried out at the Department of Telecommunications. It has been financed partly by the Norwegian Research Council (NFR) under the program 'Telecom 2005', the Department of Telecommunications and WIWIC[1].

I would like to thank my supervisor Associated Professor Kjell Aamo for his guidance, support and encouragement throughout this work. He inspired and motivated me in the beginning, and his comments and advice on the final stages helped me to complete this thesis.

An important part of this work has been based on measurements of the InGaP/GaAs HBT's, provided by Caswell Technology. I am very grateful to Dr. Steve Marsh and Dr. Mike Brookbanks at Caswell Technology for valuable discussions on their HBT process, and for inviting me to visit the foundry at Caswell. I would also like to thank Professor Thomas J. Brazil at the University College Dublin (UCD) for inviting me to visit UCD under the TMR[2] network, and for letting me stay at UCD to measure some SiGe HBT's.

I would like to thank Professor Petter Bakken, who through WIWIC has financed parts of this work.

1. WIWIC - Radio design principles for low-cost terminals and base stations of wideband wireless communications.
2. TMR - Training and Mobility of Researchers, EU Fifth Frame Program.

URN:NBN:no-3376

I would also like to thank my colleagues at the Department of Telecommunications for their support and help during these years. In particular, I would like to thank Kari B. Øien for all her excellent help on the non-technical parts of being a Dr. Ing. student. I would also like to thank all my colleagues at SINTEF for their support during this work.

Several other people have supported me during these years. I would like to thank my parents for their continues support, and all my friends for their patience. I can not mention all of them, but Edvard Ringen, Torbjørn Bakke, Per Morten Berg, Halgeir Ludvigsen and the members of Trondheim Bowling Klubb deserves a special note.

My special thanks goes to my fiancee, Heidi Snapa, for her love, help and patience during these years.

Trondheim, December 2002.

Morten Olavsbråten

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Chapter 1 Introduction

Since the first transistors were developed in the late 1940's, the progress in the electronic industry has been tremendous. New applications are introduced continuously, demanding higher and higher performance. Advanced technologies are used to develop new devices and circuits to meet the demands. The electronic industry today requires a short "time to market" for new products, and at a low cost. To accomplish this, the need for accurate computer simulations are apparent.

This work started by looking at the increasing demands on MMIC power amplifiers in signal transmission systems, where properties like high power, high efficiency, high linearity and compact small size are critical. A promising InGaP/GaAs HBT process [1, 2] developed at GEC Marconi Materials Technology Ltd. (GMMT) was chosen, for the purpose of analyzing power amplifiers at circuit level, and to find where the key problems are.

In the analysis of a power amplifier at circuit level, the accuracy of the models for the components used, are of vital importance. The development of semiconductor processes in the electronic industry is changing so fast, that the development of models almost can not keep up the pace. This is also the case for the development of practical parameter extraction procedures, which produces good models, that can be easily used by the circuit designer. This was one of the key problem encountered by analyzing a power amplifier in the HBT process from GMMT. Parts of this thesis will focus on the development of a practical procedure for parameter extraction for the chosen transistor model.

Another key problem in the development of a compact MMIC power amplifier is the thermal behaviour. High dissipated power inside the devices, does not only influence the behaviour of the transistors, and models, but also the behaviour of the circuit designer. The circuit designer can not only design a power amplifier from an

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electrical point of view. The design, and especially the layout of the design, must reflect the thermal behaviour of the circuit. A good thermal design, increases the electrical performance such as gain, output power and linearity, reduces the possibility of thermal instability, and increases the life expectancy of the power amplifier. Parts of this thesis will focus on the development of a practical procedure for calculating the thermal parameters needed in the transistor model, and aiding the thermal design of power amplifiers.

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1.1 Outline of the Thesis

The thesis consists of three main parts.

- The first part (Chapter 3) describes practical estimation techniques for estimating the thermal properties of an HBT.
- The second part (Chapter 4) describes a practical estimation technique for parameter extraction for the VBIC model.
- The third part (Chapter 5) describes the design of a power amplifier, with the aid of the techniques developed in Chapter 3 and Chapter 4.

In detail:

- **Chapter 2**: This chapter includes a brief description of the principal of operation for an HBT, and includes properties for different transistor types and a list of reported “state of the art” HBT performance. The HBT process from GMMT is presented. A short overview of a SiGe HBT process, made available through the TMR network, is also included.
- **Chapter 3**: In this chapter, a new practical technique for finding an estimate of the thermal resistance is presented. A method for estimating the thermal capacitance is also included. The new technique is evaluated on some of the InGaP/GaAs transistors from GMMT, by comparing the results to results given in [3, 4] for the same transistors. The new technique is also applied to three of the SiGe transistors.
- **Chapter 4**: In this chapter, an overview of different modelling concepts are given. The background for the model choice, explanation of the associated parameters, and how to find the values of these, are presented. A practical parameter extraction method for the VBIC model, used on an InGaP/GaAs HBT, is developed. The method is based on only a few common measurements. The measurements needed are: forward Gummel, reverse Gummel, IV, cold capacitor (passive) s-parameter, and active s-parameter measurements. The parameter extraction method is evaluated on an InGaP/GaAs HBT. This chapter also includes the measurements and modelling of the SiGe HBT.
- **Chapter 5**: In this chapter, a brief overview of power amplifiers and linearization techniques are given. The thermal junction estimation technique and the results of the parameter extraction method developed in Chapter 3 and Chapter 4, are used to design a power amplifier with an output of minimum 33 dBm. A ‘bus bar’ power combinder is used at the in- and output of the amplifier.

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1.2 Contributions of this Thesis

The main contributions of this thesis are:

- **The practical thermal resistance estimation technique**
  In Chapter 3, a technique for estimation of the thermal resistance of an HBT, is developed. This technique has been published by the author in 2002 [5], and can be found in Appendix A.1.
- **The practical parameter extraction method for the VBIC model**
  In Chapter 4, a practical method for extraction of the parameters for the VBIC model, is developed. As far as the author knows, this method is the first published parameter extraction technique for the VBIC model used on an InGaP/GaAs HBT. The method was published by the author in 2000 [6], and can be found in Appendix A.2.
- **Evaluation of the VBIC model implementation of forward transit time, T_f**
  In Chapter 4, as a part of the parameter extraction method used on an InGaP/GaAs HBT, an evaluation and extraction of the parameters in the VBIC model associated with forward transit time is performed. This evaluation and suggested parameter extraction has been published by the author in 2001 [7], and can be found in Appendix A.3.

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Chapter 2 Technology

__Technology__ - the application of scientific knowledge to the practical aims of human life or, as it is sometimes phrased, to the change and manipulation of the human environment.
- Encyclopedia Britannica

Just before Christmas, on December 23rd, 1947, the first point contact transistor where invented by J. Bardeen, W. Brattain and W. Shockley at Bell Labs. In June 1948 Shockley filed a patent on the BJT (Bipolar Junction Transistor). In this patent Shockley even describes a wide band gap emitter structure, which later become known as the HBT (Hetero-junction Bipolar Transistor). Independently of this, H. Kroemer invented an HBT, and he was also the first to explain the advantages of the HBT. [8-11] describes in detail the historical events that lead to the development of the bipolar transistor.

From this day in December 1947, the semiconductor industry has developed tremendously in the area of electronics. Today, the number of transistors produced per year is in the order of 10^{17} [12].

In this chapter some of the properties and principle of operation of the HBT are briefly explained. The InGaP/GaAs HBT process from Caswell Technology, and the SiGe chip made available through the TMR-network, are briefly described.

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2.1 Background

Technology - A word that is commonly used on the *results* of technology. As stated on page 5, technology is the application of scientific knowledge. “We have developed a new: GaAs technology, Si technology, HBT technology, HEMT technology, InGaP technology” are all examples of commonly wrong use of the word technology.

2.1.1 Properties and principal of operation of an HBT

The HBT is used in a circuit in the same way as a BJT. The main difference compared to the BJT, is the improved gain and frequency properties. In an HBT, the emitter is composed of a different material than the base. This material has a higher energy band gap than the base. The band gap in a material is the energy required to move an electron from the valence band to the conduction band. Figure 2.1 shows a principal structure of the energy bands of an HBT. The increase in band gap ΔE_g in the emitter is equal to $\Delta E_c + \Delta E_v$.

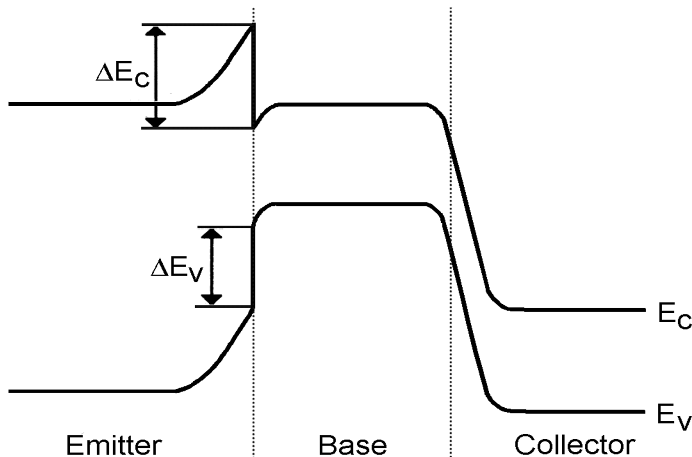

Figure 2.1. Band structure of an HBT.

In operation, the electrons coming from the emitter have a very high potential energy when they enter the base region, due to the increased band gap in the emitter. This causes the current gain to increase significantly. The main limitation of the current gain is the re-combinations in the base. The width of the base is therefore important. The gain can be increased even more by making the base more narrow, but this reduces the operating frequency due to increased resistance in the narrow base. Therefore, in an HBT, the base is highly doped to reduce the resistance and consequently increase the operating frequency. Increased doping in the base reduces the gain, and the base is made narrow to maintain the increased gain from the high band gap in the emitter. A more detailed analysis is given in [10, 13-16].

There are two main HBT types. The single HBT, usually just called HBT, has a wide band gap material in the emitter only. This type of HBT has a high gain, but also

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a high collector/emitter offset voltage causing difficulties in low voltage designs. An example of this type of HBT is the InGaP/GaAs/GaAs (emitter/base/collector) transistor from Caswell Technology. The other type is the double HBT, called DHBT. The DHBT has a wide band gap material in the emitter and in the collector. This reduces the gain compared to the single HBT, but the collector/emitter offset voltage is reduced, making it more attractive for use in low voltage designs. An example of this type of HBT is the Si/SiGe/Si (emitter/base/collector) transistor available through the TMR network.

In [17-20] different transistor types are compared. Table 2.1, shows a summary of key properties for different types of transistors.

Table 2.1. "Figure of merit" of different transistor types.

	MESFET	HEMT	BJT	HBT	DHBT
f_T [GHz]	Low	Medium	Low	High	High
F_{MAX} [GHz]	Medium	High	Low	Medium	Medium
Gain	Medium	High	Low	High	High
Noise Figure	Medium	Low	Medium	High	High
Phase Noise	Medium	High	Medium	Low	Low
Power Density	Medium	Medium	Medium	High	High
Low voltage	Good	Good	Poor	Medium	Good
Breakdown	Medium	Medium	Medium	High	High/Low
Single supply	No	No	Yes	Yes	Yes

Table 2.1 clearly shows the superior performance of the HBT over the BJT. From all the transistor types in Table 2.1, the HBT is the preferred transistor in power amplifiers and oscillators due to the high power density and the low phase noise. But, the choice of transistor type depends not only on performance, but also on the application and production cost.

2.1.2 Different materials used in HBT's - "State of the art"

An HBT can be made of many types of materials. Four of the most common materials are listed below.

The SiGe HBT is a rather new Si transistor where the base is composed of a SiGe alloy. The amount of Ge introduced in the base vary from process to process, but is usually in the interval from 8 to 15 % [21]. The base is usually graded to avoid a large lattice mismatch, which can cause faults in the lattice and traps.

The AlGaAs/GaAs HBT and the InGaP/GaAs HBT are fairly equal when it comes to performance. The base/emitter may be graded, but this is not as common as for the SiGe HBT. The main difference may be the reliability of the transistors. [22, 23] reports that InGaP/GaAs HBT has enhanced reliability over the AlGaAs/GaAs HBT.

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The InGaAs/InP HBT has higher thermal conductivity than GaAs and superior frequency response. On the negative side, the InGaAs/InP transistors are expensive in production.

[1, 2, 17, 18, 21, 22, 24-29] reports some "state of the art" performance of these four transistor types. A summary is listed in Table 2.2.

Table 2.2. "State of the art" performance of different transistor types.

	Si/Ge	**AlGaAs/ GaAs**	**InGaP/ GaAs**	**InP/ InGaAs**
f_T [GHz]	130	171	160	300
F_{MAX} [GHz]	160	192	300	1000
Breakdown [V]	5.5	17	23	20
Maximum current gain β	113	200	400	150
Thermal cond. [W/m/K]	170	46	46	77
Bulk band gap E_g [eV]	1.12	1.42	1.42	1.34

2.2 InGaP/GaAs HBT from Caswell Technology

The InGaP/GaAs HBT's were originally developed by GEC Marconi Materials Technology Ltd. (GMMT). The GMMT foundry located at Caswell, England, changed their name to Caswell Technology. Just before and during this transition, Dr. Steve Marsh at Caswell provided many measurements on the InGaP/GaAs HBT's. These measurements are described in Chapter 4.

[1, 2] describes the InGaP/GaAs HBT process. Some of the key properties of the InGaP/GaAs HBT from [1, 2] and Dr. Steve Marsh are listed in Table 2.3.

Table 2.3. Properties of the InGaP/GaAs HBT.

Property	Value
Emitter length [μm]	5.0-40
Emitter width [μm]	2.0
Collector height [μm]	1.3
Substrate thickness [μm]	100
f_T [GHz]	>50
f_{MAX} [GHz]	>100
Breakdown Voltage [V]	>23
Current gain β	>150
Max. recommended collector current [mA/μm]	1.0
Substrate thickness [μm]	100
Thickness metal M1, gold alloy [μm]	0.5
Thickness metal M2, gold [μm]	0.5
Thickness metal M3, gold [μm]	3.0
Thickness Silicon Nitride dielectric [μm]	0.13
Thickness Polyimide dielectric [μm]	1.4
Spiral inductance approx. [nH]	0.3-13
Polyimide Capacitor approx. [pF]	0.027-2.6
Silicon Nitride Capacitor approx. [pF]	0.52-58
Nichrome thin film resistors [Ω/square]	20, 200

As a part of the cooperation with Caswell Technology, they offered to process test circuits based on my new models extracted from their measurements. Unfortunately, shortly after this agreement, political decisions were made at Caswell, with the consequence that their funding for further development of the HBT process was stopped. Caswell Technology was then bought by Bookham Technology, a company in the optical market. Their primary interest was Caswell Technology's HEMT process. The HBT process is not terminated, but halted for an indefinite time.

2.3 SiGe transistors available through TMR network

The SiGe transistors discussed in Section 4.5, were available through the Training and Mobility of Researchers (TMR) network. The TMR network was an international post-graduate and researcher exchange program under the European Union's fifth frame program. Professor Thomas J. Brazil at the University College Dublin (UCD) was a part of this TMR network. He offered the possibility of visiting UCD, and do some measurement work for the TMR network on a SiGe chip.

Figure 2.2 shows a photo of the SiGe chip and the probe tips. All the images of the SiGe chip were taken through the microscope with an ordinary digital camera.

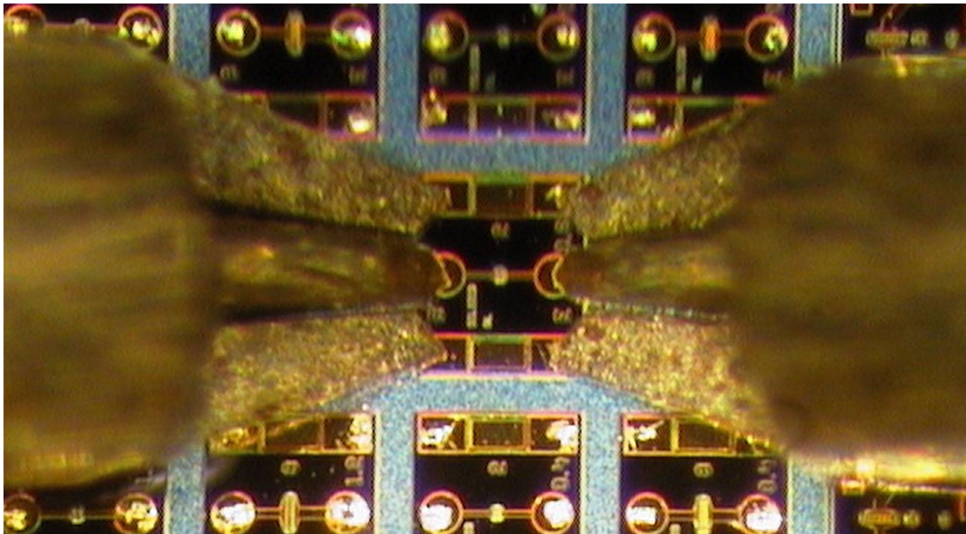

Figure 2.2. SiGe chip and probe tips.

The only information provided on the SiGe chip were: the transistors were connected as an emitter follower with the collector connected to the ground, the width of the emitter fingers were printed on the chip and the thickness of the chip was almost certainly 100μm.

The physical dimensions of the transistors and the lines connecting the transistor to the probe pads had to be estimated for the thermal and electrical modelling in the next chapters. The only means of measuring the dimensions of the chip was by using the probe tips. The edge of the ground contacts on the probe tip were very sharp, making it ideal for a measurement reference point. The probes were lifted slightly above the chip and moved over the chip. The scale of the probe adjustment knobs was read. Some of the dimensions, like the line widths, had to be estimated from zooming in on the photo, and geometrically estimate the width/length ratio. The length of the lines were measured using the probe tips. Table 2.4. shows the estimated dimensions of the SiGe chip.

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Table 2.4. SiGe chip dimensions.

	Dimension	
Base/Emitter line length [mil]	1.5	measured
Emitter length [mil]	0.4	measured
Base line width 1-finger [mil]	0.25	calculated
Emitter line width 1-finger [mil]	0.25	calculated
Base line width 2-finger [mil]	0.25	calculated
Emitter line width 2-finger [mil]	0.25	calculated
Base line width 8-finger [mil]	0.50	calculated
Emitter line width 8-finger [mil]	0.75	calculated

The width of the emitter was printed on the chip.

The energy band gap of the SiGe base was estimated to be 1.05 eV. [30] reports the reduction of band gap compared to Si, to be approximately 7.5 meV per percent of Ge added to the base. The percentage of Ge in the base was assumed to be 10 %.

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Chapter 3 Thermal Properties

The main key for success in active circuit design are reliable models for the components. For large signal transistor amplifiers the thermal behaviour must be accurately described. The thermal properties of the transistors, are therefore of great importance, together with the DC and the frequency dependent parameters.

Usually a first order model is used as an approximation of the complex thermal behaviour of a transistor. The first order model is composed of an equivalent thermal resistance and an equivalent thermal capacitance.

The objective in this chapter is to develop a simple technique capable of producing acceptable values for the junction temperature, the thermal resistance and the thermal capacitance from a few physical data and the layout of the transistor. The main focus will be on the junction temperature and the thermal resistance.

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3.1 Thermal Material Properties

The main thermal properties of the materials used in InGaP/GaAs HBT's and SiGe/Si HBT's are discussed in the next subsections. Only properties needed for the estimation methods in Section 3.2 and Section 3.3 are discussed.

3.1.1 Thermal Properties of Bulk GaAs and Si

Thermal Conductivity:

The thermal conductivity of both GaAs and Si bulk material are highly dependent on the temperature. Figure 3.1 shows an example of this for GaAs taken from [31].

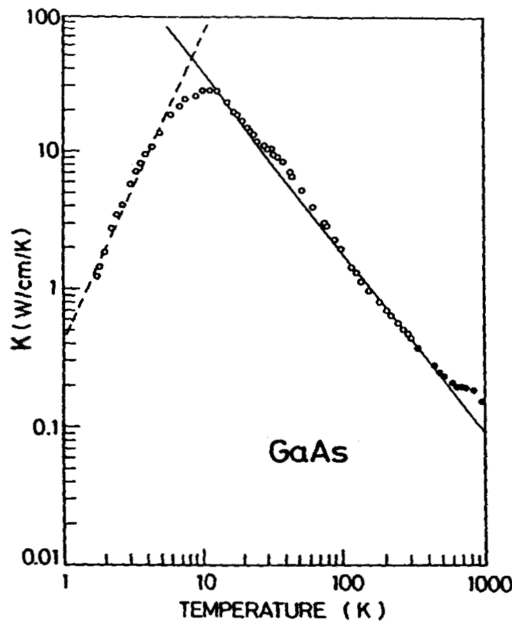

Figure 3.1. Thermal conductivity of GaAs from [31]

Several equations that describes the relationship between thermal conductivity, k_{GaAs}, and temperature, have been proposed [13, 31]. (3.1) shows the commonly accepted relationship recommend by [31] and [32].

$$k(T) = \mathrm{A} \cdot T^{\mathrm{n}} \tag{3.1}$$

The temperature is given in kelvin.

[31] reports that $\mathrm{A} = 745$ and $\mathrm{n} = -1.30$ for GaAs. [32] uses the same equation for the temperature dependence of the thermal conductivity for Si, and reports that $\mathrm{A} = 5000$ and $\mathrm{n} = -1.40$.

Specific Heat:

The specific heat $C_{P,\ GaAs}(T)$ of GaAs is given by (3.2). (3.2) is taken from [31]. The specific heat for GaAs does not vary greatly around room temperature, as shown in Figure 3.2.

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$$C_{p,\,GaAs}(T) = 0.343 + 4.7 \cdot 10^{-5} T - 3.2 \cdot 10^{3} T^{-2} \tag{3.2}$$

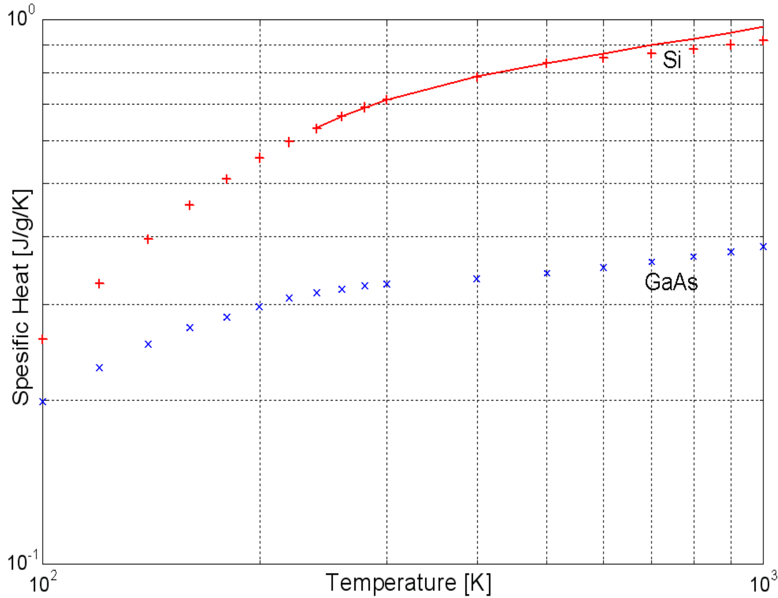

Figure 3.2. Specific heat versus temperature for GaAs and Si.

The data points, marked with crosses, plotted in Figure 3.2 is taken from data given in [31, 33, 34].

The specific heat for Si can be described by the same type of equation. By fitting the data in Figure 3.2 for Si, from 260K to 500K, the equation for $C_{P,\,Si}(T)$ is given in (3.3). (3.3) is plotted in Figure 3.2 for evaluation.

$$C_{p,\,Si}(T) = 0.768 + 5.14 \cdot 10^{-4} T - 1.07 \cdot 10^{4} T^{-2} \tag{3.3}$$

Thermal expansion:

The density and thermal linear expansion coefficient for GaAs and Si are listed in Table 3.1. The data is taken from [10].

Table 3.1. Density and Linear Expansion Coefficient of GaAs and Si.

Material	Density, ρ	Thermal linear expansion coefficient, α
GaAs	5.318 g/cm^3 at 300K	6.86 µm/m/K at 300K
Si	2.329 g/cm^3 at 298K	2.60 µm/m/K at 298K

3.1.2 Thermal Properties of Gold and Aluminium

The metal used in GaAs processes is usually gold. In Si processes aluminium is usually used. The density, thermal conductivity and specific heat for both materials are shown in Table 3.2. The data in Table 3.2 are taken from "MatWeb" [35].

Table 3.2. Density, Thermal Conductivity and Specific Heat of Au and Al.

Material	Density, ρ	Thermal Conductivity	Specific Heat	Thermal linear expansion coefficient, α
Gold	19.32 g/cm^3	301 W/m/K	0.1323 J/g/K	14.4 μm/m/K at 293K
Aluminium	2.699 g/cm^3	210 W/m/K	0.9 J/g/K	24.0 μm/m/K at 293K

3.1.3 Thermal Properties of Polyimide and Silicon Nitride

The polyimide and the silicon nitride layers are used in GaAs to build different capacitors. Both layers are separating the metal 3 from metal 2. Table 3.3 shows the thermal conductivity and thickness of the polyimide and the silicon nitride layers. The thermal conductivities are taken from [35]. The thickness are specified by Caswell Technology.

Table 3.3. Thermal conductivity and thickness of polyimide and silicon nitride.

	Thermal Conductivity	Thickness
Polyimide	0.25 W/m/K	1.4μm
Silicon Nitride	15-35 W/m/K	0.13μm

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3.2 Thermal Resistance

There are several ways to find the thermal resistance. All having their advantages and disadvantages.

- *A full 3D thermal simulation*: Software that is capable of doing 3D thermal simulations will give results with high accuracy, but this kind of software is usually expensive and inaccessible for the common circuit designer. The simulations are time consuming and depend on a high level of physical details. The level of details needed for an accurate simulation, is usually not available from the manufacturer.
- *DC measurements at different temperatures*: Methods based on DC measurements at different temperatures usually produce results with good accuracy. There are three common methods of calculating the thermal resistance. The first method is given in [36], and is based on measuring the base-emitter voltage V_{be} at different temperatures. The method in [37] is based on measuring the current gain β at different temperatures. The main drawback of the methods in [36, 37] is that they linearize the measured V_{be} and β with the respect to the temperature. This generates inaccuracies as pointed out by [3]. The method in [36] is also only valid at low power dissipations, where the thermal resistance is constant. The newest method is given by [4]. This method is based on measuring the collector current with constant base current at different temperatures. It overcomes the drawbacks of the other methods, and can be used to find the thermal resistance under high power dissipation. A comparison of these methods can be found in [38]. The main disadvantage of these three methods is that they require equipment for temperature regulation on the probe station, when doing DC measurements.
- *New technique for estimating the junction temperature*: A new technique for estimating junction temperature is proposed by the author and presented in [5]. The new technique will be developed in the following subsections. The technique is based on a few physical data and the layout of the transistor. No measurements and specialized software are needed, only a mathematical tool like MATLAB is required. The limitations of this estimation technique are in the validity of the assumptions in Section 3.2.1.

All the junction temperature results presented in the next sub-sections are relative temperature changes from the ambient temperature.

3.2.1 Assumptions

The main assumptions for the new junction temperature estimation technique are:

- First assumption: The contributions to the junction temperature are dependent only on three separate phenomena - the thermal conduction in the substrate, the thermal conduction of the metal connecting the emitter to the via holes, and the

effects of the via holes on the substrate temperature. These three effects can be calculated separately. Figure 3.3 illustrates these three effects.
Validation: In a power transistor, the metal connected to the emitter is usually the top level metal, which is also the thickest. The top level metal is usually separated from the substrate by a polyimide layer, and connected to a via hole through the substrate to the backside. The separation of thermal conduction in the substrate and the thermal conduction of the top level metal is valid, because the separating layer has a low thermal conductivity. The thermal conductivity of the top level metal, which in the case of GaAs is gold, is a factor of 1200 times higher than that of the separating polyimide. A rule of thumb, is that this method is valid as long as the length of the metal lines, connecting the emitter to the via-holes, is less than 1200 times the thickness of the polyimide layer.

- *Second assumption*: The dissipated power flows only in the top level metal and in the substrate as indicated in Figure 3.3.
  Validation: Parts of the dissipated power is going down into the substrate. The rest of the dissipated power are conducted through the top level metal connected to the emitter. Of course, a very small part of the dissipated power will be spread out into other parts, like the metal connected to the base and collector. This power is then either flowing into the substrate or it is going into the air by convection. This small part is disregarded, and therefore the heat flow is assumed to be as illustrated in Figure 3.3.

- *Third assumption*: The power dissipation in the transistor is assumed coming from a flat rectangular plate with size equal to the emitter dimensions, and with an uniform distribution of the dissipated power.
  Validation: The power dissipation in a real transistor is not coming from a flat rectangular plate, but the power is dissipated non-uniformly throughout the volume of the transistor. Since the height of the transistor is small and the material to the side of the transistor will mainly be polyimide, the heat flow to the sides will be very small. Also, the height of the transistor is small compared to the length of the transistor. Seen from below, the transistor will approximately look like a rectangle. The junction temperature calculated in the next sections will therefore be an average temperature inside the transistor. This is a commonly accepted assumption [13, 39, 40].

- *Fourth assumption*: The effect of the via holes on the heat transfers in the substrate can be approximated with a negative (or sometime positive) point source instead of the via hole.
  Validation: This assumption will be explained in Section 3.2.3.

- *Fifth assumption*: The top of the gold filled via holes will have a uniform temperature given by the dissipated power flowing from the top level metal to the via hole multiplied by the thermal resistance of the via hole. The temperature will be equal to the backside of the substrate at a low heat flow.

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Validation: The thermal resistance of a via hole is low, because the via hole structure is massive. Since the thermal conductivity of gold is high and the via hole is filled, the assumption of a uniform temperature over the top of the via hole is valid. The thermal resistance of a via hole from top surface to the back side, is approximately 106 K/W. This was calculated from the geometry of the via hole, where the diameter of the top side hole is 50 µm, diameter of the back side hole is 80 µm and the height is 100 µm. At low heat transfers, the temperature at the top side of the via hole can therefore be set equal to the temperature of the substrate back side.

- *Sixth assumption*: The backside of the substrate is connected to an ideal heat sink.
  Validation: If the chip is mounted in a package and the dissipated power is high, this assumption is not valid. In this case, the thermal resistance from the back side of the substrate to the heat sink must be taken into account. In this work it is assumed that the back side is connected to a massive chuck in a probe station. This is close to an ideal heat sink.

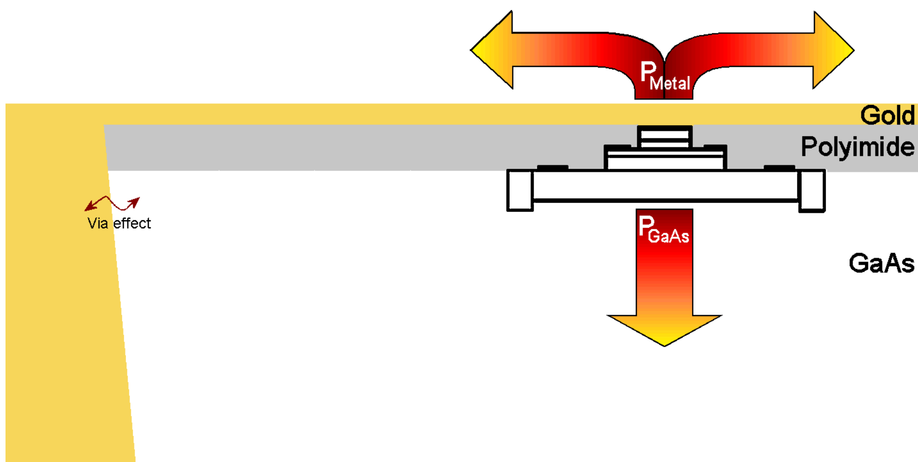

Figure 3.3. The three effects contributing to the junction temperature. (Figure is not to scale)

3.2.2 Heat Transfers in the Substrate

The heat transfer in the substrate, as it is stated in [13], is described by the heat flow equation given in (3.4):

$$\vec{\nabla} \cdot k(T)\vec{\nabla} T(x, y, z) = -P(x, y, z) \tag{3.4}$$

P is the dissipated power density, T is the temperature, and k is the temperature dependent thermal conductivity.

Equation (3.4) can be reduced to the Laplace's equation (3.5), when assuming that the thermal conductivity is independent of the temperature. It will be shown in Section 3.2.5 that this assumption is valid.

$$\nabla^2 T(x, y, z) = -\frac{P(x, y, z)}{k} \tag{3.5}$$

One solution to the Laplace equation, that fits this problem, is stated in [13] and shown in (3.6).

$$T_{point}(x, z, x'_0, z'_0) = \frac{P_{Sub}}{2\pi \cdot k_{Sub}\sqrt{(x - x'_0)^2 + (z - z'_0)^2}} \tag{3.6}$$

(3.6) is a solution to the Laplace equation when the observation point and the point source are located at the substrate surface ($y = 0$, $y'_0 = 0$), and assuming a semi-infinite substrate. The temperature T_{point} at an arbitrary point (x, z) on the substrate surface is calculated from the point source located at (x'_0, z'_0), where P_{Sub} is the power dissipated from point source into the substrate in watts and k_{Sub} is the thermal conductivity in W/m/K at a constant temperature.

All the transistors in a MMIC are located at the substrate surface. In the analysis performed in this chapter, it is therefore only necessary to calculate the temperature at the substrate surface.

A transistor is assumed to be a flat rectangular plate heat source of length L and width W, equal to the size of the emitter. Figure 3.4 shows the rectangular plate placed in a coordinate system centred at (x_0, z_0).

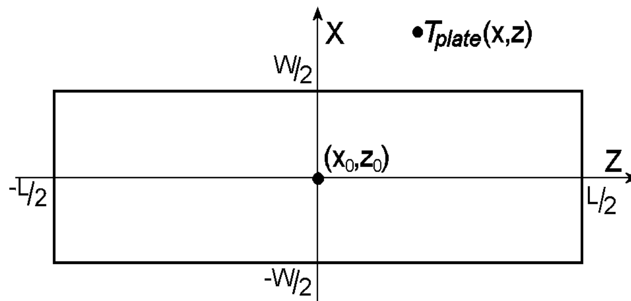

Figure 3.4. Rectangular plate in a coordinate system.

The temperature T_{plate} at an arbitrary point (x, z) on the substrate surface, caused by the rectangular heat source, is found by integrating (3.6) over the rectangular plate, as shown in (3.7).

$$T_{plate}(x, z) = \frac{1}{LW}\iint_{LW} T_{point}(x, z, x'_0, z'_0)\,dx'_0\,dz'_0 \tag{3.7}$$

The solution to the heat flow equation given in (3.6) assumes that the substrate has an infinite thickness. In a real device the substrate has a finite thickens, and the backside of the substrate is connected to an ideal heat-sink as shown in Figure 3.5. As a first approximation, the effect of the ideal heat sink is included by removing the heat sink, and replacing it by an additional heat source. This new heat source is a negative image of the real heat source, placed below the backside of the substrate, at a distance equal to the substrate thickness. This is the first step in a mirror technique given in [13]. Several images may be added to achieve higher accuracy. The first mirrored heat source is shown in Figure 3.5.

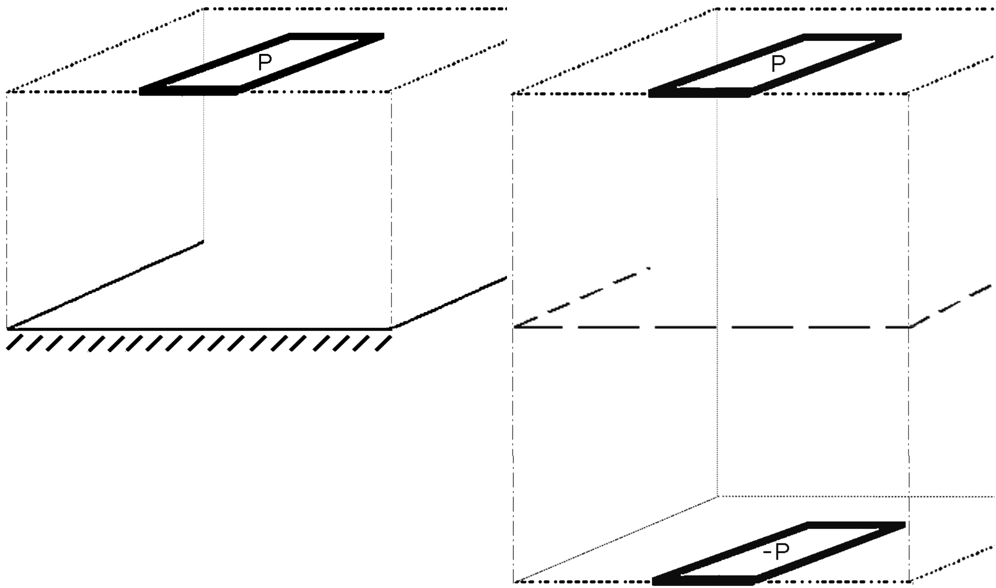

Figure 3.5. The heat source with heat sink and with the first image source.

The overall temperature function $T_{top}(x, z)$ at the substrate surface is a sum of the contribution from the heat source at the substrate surface, T_{plate}, and the image sources evaluated at the substrate surface $T_{n,\,im}$, as shown in (3.8).

$$T_{top}(x, z) = T_{plate}(x, z) + \sum_{N} T_{n,\,im}(x, z) \tag{3.8}$$

N is the number of image sources that is taken into account.

The average junction temperature $T_{j,Sub}$ from the heat conduction in the substrate is found by calculating the average temperature across the rectangular heat source, by the use of (3.9).

$$T_{j,\,Sub} = \frac{1}{LW} \iint_{LW} T_{top}(x, z)\,dx\,dz \tag{3.9}$$

All this calculations can easily be done in MATLAB by numerical integration. To increase the speed of the calculations in MATLAB, the first part of the double integral in (3.9) (the double integral over T_{plate}, consequently the quadruple integral over T_{point}) can be found analytically after many pages of tedious manipulations. The result is shown in (3.10).

$$T_{j,plate} = \frac{P}{2\pi kLW} \cdot \Bigg\{ A_2\left[\sinh^{-1}\left(\frac{B_2}{|A_2|}\right) - \sinh^{-1}\left(\frac{B_1}{|A_2|}\right)\right] - A_1\left[\sinh^{-1}\left(\frac{B_2}{|A_1|}\right) - \sinh^{-1}\left(\frac{B_1}{|A_1|}\right)\right] + B_2\left[\sinh^{-1}\left(\frac{A_2}{|B_2|}\right) - \sinh^{-1}\left(\frac{A_1}{|B_2|}\right)\right] - B_1\left[\sinh^{-1}\left(\frac{A_2}{|B_1|}\right) - \sinh^{-1}\left(\frac{A_1}{|B_1|}\right)\right]\Bigg\} \quad (3.10)$$

$$, where\ A_2 = x - x_0 + \frac{W}{2},\ A_1 = x - x_0 - \frac{W}{2},\ B_2 = z - z_0 + \frac{L}{2},\ B_1 = z - z_0 - \frac{L}{2}$$

The second part of the double integral in (3.9) is producing an extremely large analytical expression, because the image sources are positioned below the substrate surface and therefore includes the height ($y_0 \neq 0$). Therefore, this part is evaluated in MATLAB as numerical integration.

In the multi finger case, the thermal coupling between fingers must be taken into account. This is achieved by using (3.8) to find the temperature rise from one finger on the other fingers. The temperature rise from all the other fingers is then integrated over the finger in question and added to the junction temperature calculated for this finger, as if it was alone. This is then done for all fingers.

3.2.3 The Effect of the Via-Holes on the Heat Transfers in the Substrate

The analysis in Section 3.2.2, assumes that the substrate is homogeneous and infinite in x and z directions. In a real device, vertical via holes through the substrate are often used. The vertical via holes generate areas on the substrate surface where the temperature is practically equal to the temperature in the metal at the top of the via hole, due to the power flowing from the top level metal through the via hole. To emulate the effect of a via hole and remove it, the via hole is, as a first order estimate, replaced by a point source located at the substrate surface. The power and position of the point source are selected in such a way that this source together with the transistor, give a temperature increase along the edge of the via hole equal to the temperature increase due to the power flowing from the top level metal through the via hole. Since this only is a first order estimate, only one point source is used. The via hole itself is removed.

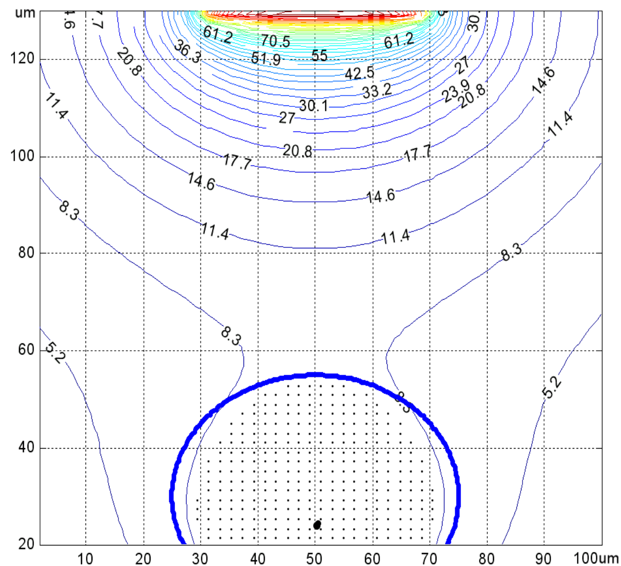

Figure 3.6. Illustration of the negative point source inside the via hole.

The illustration in Figure 3.6 shows one half of an isotherm contour plot for a single finger transistor. The indicated temperatures are the temperature increase above the ambient temperature. The large black dot indicates a possible placement of the negative point source, inside the area where the via hole was placed. The thick blue line indicates the edge of the physical via hole.

When calculating the temperature in i.e. MATLAB, the temperature can become extremely high either positive or negative inside the shaded area close to the point source. This is non physical (and a non interesting area when calculating the temperature at the substrate surface, see Section 3.2.1), and the temperature here is set to the temperature calculated at the top of the via hole from the power flowing in the metal.

The shaded area indicates where the temperature increase is equal to the temperature increase at the top of the via hole, due to the heat flow from the top level metal through the via hole.

The method of replacing the via hole with a point source may result in errors in the area behind the via hole. This area is of no interest when estimating the temperature inside and close to the transistor. Therefore, this area is disregarded. If power dissipating devices of interest are placed behind the via hole, these devices must be included in the thermal simulation, in order to give a new and correct power and position for the point source.

Before calculating the effect of the point source inside the via hole, onto the rectangular plate, the method of imaging is employed on the point source. The contribution $T_{j,Via}$ to the total junction temperature T_j, is found by averaging the

temperature contribution from the point source, and its images, across the rectangular plate. The total junction temperature is given in (3.11).

$$T_j = T_{j,\,Sub} + T_{j,\,Via} \tag{3.11}$$

This method is just a simplified estimate of the effect from the via holes on the temperature inside the substrate. The temperature around the rectangular heat source drops off rather quickly, and there are some distance between the active device and the via hole. Therefore, the effect of the via hole is rather small, but not neglectable. The first order estimate is therefore a good enough estimate of the effect from the via hole, resulting in good accuracy.

3.2.4 Heat Transfers in the Top Level Metal through the Via Holes

The emitter of the transistors is connected to the top level metal. The top level metal is connected to the via holes. The temperature rise in the metal at the emitter, is a result of the heat transfer in the top-level metal, and can easily be calculated from (3.12).

$$T_{j,\,M} = P_M \cdot R_{t,\,M} \tag{3.12}$$

$T_{j,M}$ is the temperature increase at the emitter, P_M is the power flowing in the metal from the emitter to the via holes in watts, and $R_{t,M}$ is the total thermal resistance of the metal from the emitter to the backside of the substrate in K/W.

The thermal resistivity of a rectangular metal line is given by (3.13).

$$R_{line,\,M} = \frac{L_m}{k_m\, W_m\, h_m} \tag{3.13}$$

where k_m is the thermal conductivity of the metal in W/m/K, and L_m, W_m and h_m is the length, width and height of the metal line in meter.

3.2.5 Junction Temperature Estimation Technique

The total power dissipated in the transistor is flowing partly in the metal and partly in the substrate, as indicated in Section 3.2.1 and in Figure 3.3. The total dissipated power is divided in such a way that the temperature in the metal at the emitter is equal to the temperature in the substrate at the emitter, including the effect of the via hole. (3.14) describes this relation:

$$\left.\begin{array}{l} P_{Sub} = nP_{tot} \\ P_M = (1-n)P_{tot} \end{array}\right\} \Rightarrow T_{j,\,M} = T_j \tag{3.14}$$

The value of n is the part of the dissipated power that flows into the substrate.

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The calculation of the temperature in the substrate in Section 3.2.2 is based on a constant value of the thermal conductivity k_{Sub} in the substrate. However, the thermal conductivity in the substrate is dependent on the temperature, and the temperature changes with the distance from the transistor. The dependence of the thermal conductivity on temperature of GaAs is shown in (3.1). The estimation technique to find the actual junction temperature T_j of a device, is therefore divided in two parts (*Part A* and *Part B*), each solving the equations for different selected values of k_{Sub}. This makes the assumption of constant k_{Sub} valid.

Part A:

1. Choose a value for *n* in (3.14).

2. Calculate $T_{j,Sub}$, $T_{j,Via}$ and $T_{j,M}$ from Section 3.2.2 to Section 3.2.4 using k_{Sub} at ambient temperature.

3. Repeat *Step 1* and *Step 2* until the a value of *n* is found that fulfil (3.14).

The result from *Part A* is the junction temperature $T_{j,PartA}$ evaluated for k_{Sub} at ambient temperature. The ambient temperature is the lowest temperature in the device.

In *Part B* the highest temperature in the device is used to find the k_{Sub}.

Part B:

1. Choose a new value for *n* in (3.14).

2. Calculate $T_{j,Sub}$, $T_{j,Via}$ and $T_{j,M}$ from Section 3.2.2 to Section 3.2.4 using k_{Sub} at the highest temperature in the device, with $T_{j,PartA}$ as a starting value.

3. Repeat *Step 1* and *Step 2* until the a value of *n* is found that fulfil (3.14).

The result from *Part B* is the junction temperature $T_{j,PartB}$ evaluated for k_{Sub} at the highest temperature in the device.

The junction temperatures calculated in *Part A* and *Part B* are the lower and upper limits of the junction temperature estimate. The actual value of the junction temperature will be between these limits as shown in (3.15).

$$T_{j,\,actual} \in [T_{j,\,PartA}, T_{j,\,PartB}] \tag{3.15}$$

The junction temperature estimation technique described above, was published [5] by the author in 2002, and can be found in Appendix A.1.

3.2.6 The Thermal Resistance

The thermal resistance of the transistor can be found by dividing the junction temperature found in (3.15) by the total dissipated power P_{tot}, as shown in (3.16).

$$R_{TH} = \frac{T_{j,\,actual}}{P_{tot}} \tag{3.16}$$

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3.3 Thermal Capacitance

The thermal capacitance can be found by different methods, as for the thermal resistance. There are very little in the published papers describing how to find the thermal capacitance, except by measurement. From pulsed DC-measurements [41], the thermal time constant can be found. If the thermal resistance is already found, by some other technique, the thermal capacitance can easily be calculated. The thermal capacitance could also be found by a full 3D simulation. This is, as for the thermal resistance, expensive software and requires a high physical detail.

For this work, none of these methods were possible to use. An estimate of the thermal capacitance had to be calculated from simple physical properties.

$$C_{TH}(T) = C_p(T) \cdot \rho \cdot V \tag{3.17}$$

(3.17) gives the thermal capacitance of a material as a function of the specific heat, density and volume. In a practical device the main difficulty will be to find a good approximation of the effective volume for the thermal capacitance.

The volume for the thermal capacitance, may include different materials i.e. the GaAs in the transistor and parts of the gold connected to the emitter. The total thermal capacitance will then be a sum of the separate thermal capacitance of each of the materials involved.

The density of a material change with the temperature, but the changes are very small for the materials considered here. The thermal linear expansion coefficient of GaAs, Si, gold and aluminium are rather small, and therefore the volume change will be rather small. By changing the temperature from 300K to 400K the volume of GaAs, Si, gold and aluminium will only increase with approximately 0.21%, 0.078%, 0.43% and 0.725% respectively. The densities will decrease with the same small factors. The change in the density is neglectable compared to the uncertainty in the volume estimation, and the density can therefore safely be set to a constant value.

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3.4 Results for the InGaP/GaAs HBT

The estimation technique in Section 3.2.5 was evaluated by comparing the results with measurements of the junction temperature for different GaAs HBT's. The measurement results were taken from [3, 4]. All the results in [3, 4] were found by using the techniques presented in [4, 36, 37], except for the single finger transistor, which has been evaluated in [4] by a full 3D thermal simulation.

The single finger transistor is made in two versions. One version, has the emitter connected to a wide metal line, connecting the emitter to the back side of the substrate through two via holes, thermally shunting the device. The use of this transistor, 1x40C, is in circuits with grounded emitter. The other version has no thermal shunt to ground. This transistor, 1x40, can be used in circuits where the emitter should necessarily not be connected to the ground. In [4] only the 1x40C transistor is evaluated.

There are four 4-finger transistors evaluated in [3, 4]. Two of them have a narrow finger spacing of 6 μm. The 4x40 transistor has no thermal shunt to the ground, while the 4x40C transistor has a thermal shunt to the ground. The other two have a wide finger spacing of 50 μm. The P4x40 transistor has some thermal shunt (see Section 3.4.5), while the P4x40C transistor has a full thermal shunt.

A MATLAB program was made, that uses the new technique presented in Section 3.2.5, to calculate the temperature function on the substrate surface and the junction temperature interval, including the heat flowing in the top level metal and the effect of the via holes.

All the junction temperature results presented in the next sub-sections are relative temperature changes from the ambient temperature.

3.4.1 Single Finger 1x40C Transistor, Thermally Shunted

The single finger 1x40C transistor, has the top level metal (metal 3) running across the transistor from one via hole to the other via hole. The collector is connected to metal 2 (dark blue) and connected to metal 3 outside the transistor. The layout of this transistor is shown in Figure 3.7.

Thermal Resistance:

In the junction temperature estimation technique, the image method [40] include an infinite number of images, in theory. In a practical application only a limited number of images can be used. To decide how many images that are needed to produce a satisfactory result, a test with different number of images was done. The simulations for this transistor was evaluated at a power dissipation of 0.265W with 22°C ambient temperature. In the first 5 columns in Table 3.4 the results with different numbers of images are shown. Here the via holes are disregarded. After the first two images have been included there are only minor changes in the results, and well within the accuracy of this method. It was therefore decided to include three images. The last column in Table 3.4 shows the results for three images including the effect of the via holes. The effect from the via holes for this transistor was very small due to the relatively large distance from the transistor.

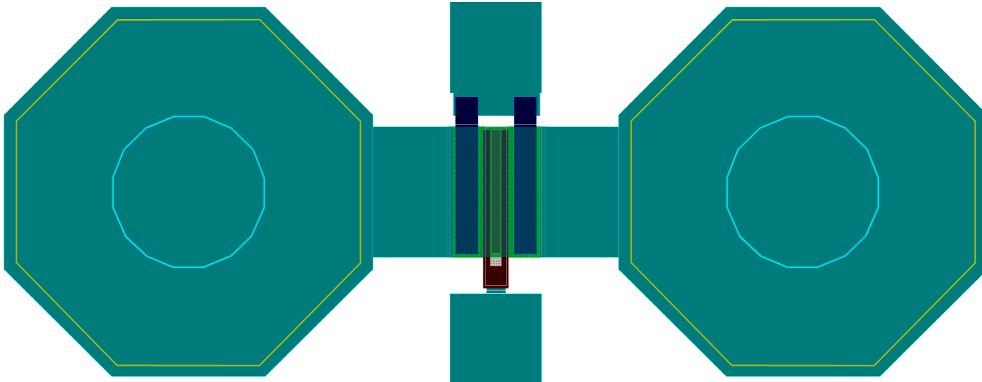

Figure 3.7. Layout of the 1x40C transistor.

Table 3.4. Results with different numbers of images.

	1x40C no image no via	1x40C 1 image no via	1x40C 2 image no via	1x40C 3 image no via	1x40C 4 image no via	1x40C 3 image via
$T_{j,PartA}$	99.8°C	96.7°C	98.3°C	97.2°C	98.2°C	97.5°C
$T_{j,PartB}$	133.6°C	129.2°C	131.5°C	130.0°C	131.4°C	130.3°C

The MATLAB program will be used with three images and the effect of the via holes included for all the transistors in the following sub-sections.

In [4], the single finger transistor is not measured, it is only simulated in a 3D thermal simulation with a dissipated power of 0.4W. This is done in [4], just for comparing results. In a practical situation, the transistor would be damaged by this power level. The maximum recommended average power dissipation is about 0.1W for this transistor.

Table 3.5 shows the results from the thermal simulation of the transistor for two values of power dissipation, at an ambient temperature of 25°C.

The simulation time was approximately 10 seconds for *Part A*, and includes the time to find the part n of the power flowing in the substrate, to calculate the junction temperature, and the temperature function on the surface. The simulation time for *Part B* was approximately 20 seconds, and includes the time to find n, to calculate new values for k_{Sub} for each iteration based on the T_j found in previous iteration, to calculate the junction temperature, and the temperature function on the surface.

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Table 3.5. Results for the single finger 1x40C transistor.

	Part A	*Part B*	*Part A*	*Part B*
Total dissipated power P_{tot} [W]	0.4	0.4	0.265	0.265
Power flowing in the metal [%]	42.5	57.3	42.5	52.2
Temp. at top of via hole $T_{M,via}$ [K]	9.0	12.1	6.0	7.3
Thermal conduction k_{GaAs} [W/m/K]	45.2	21.4	45.2	28.2
Junction temperature increase T_j [K]	**148.5**	**232.3**	**98.4**	**131.3**
Thermal Resistance R_{TH} [K/W]	371.2	580.8	371.2	495.3

A relatively large part of the dissipated power is flowing in the top level metal in this transistor as shown in Table 3.5. The temperature at the top of the via hole will be between 6.0°C and 7.3°C for a power dissipation of 0.265W. This is the reason for the very low impact the via holes have on the temperature in the substrate. The temperature in the substrate have, due to distance from the via hole to the transistor, dropped off to a value just below the temperature of the via hole. The via holes are in fact warming the substrate slightly, due to the high power flowing in the metal. This is accomplished by a positive heat source placed in the via hole.

The main results in Table 3.5 are the junction temperature interval. [4] calculates the junction temperature increase to be T_j = 163°C for the dissipated power of 0.4W, and T_j = 105°C for the dissipated power of 0.265W. Both results fall well within the upper and lower limits calculated from the present technique.

The large interval found at the highest power level with present technique is due to the destructive power level in this transistor. At normal power levels, the estimated interval will be considerably smaller.

An isothermal plot of the 1x40C transistor is shown in Figure 3.8. The blue circles indicates the edge of the via holes.

In this case, the temperature calculated at the substrate surface, at the edge of the via hole, was lower than the temperature, $T_{M,via}$, at the top of the via hole calculated from the heat transfer in the metal. The shaded area inside the via holes indicates where the temperature was lower than $T_{M,via}$, and where it now is higher due to the point source indicated with the black dot inside the via hole. The temperature inside the via hole is, due to the point source, higher than $T_{M,via}$. This is non physical, and the temperature inside the shaded area is therefore set equal to $T_{M,via}$.

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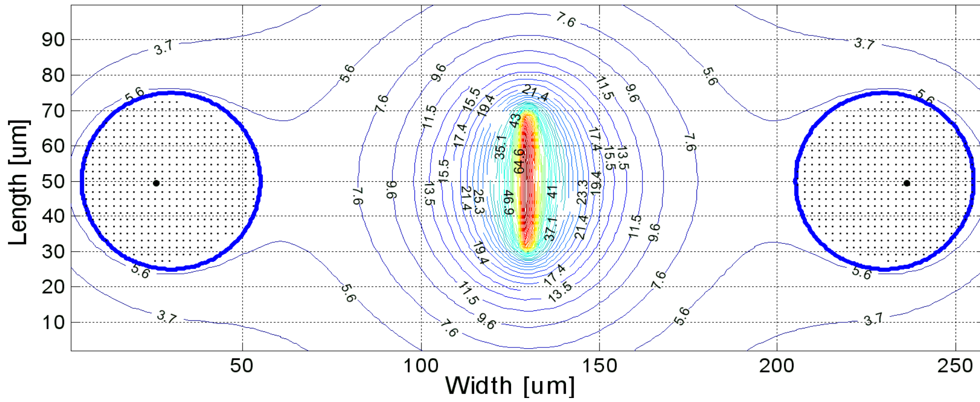

Figure 3.8. Isothermal plot of the 1x40C at P_{tot}=0.265 W and k_{GaAs}=45.2 K/W.

In Figure 3.9 a 3D thermal plot is shown.

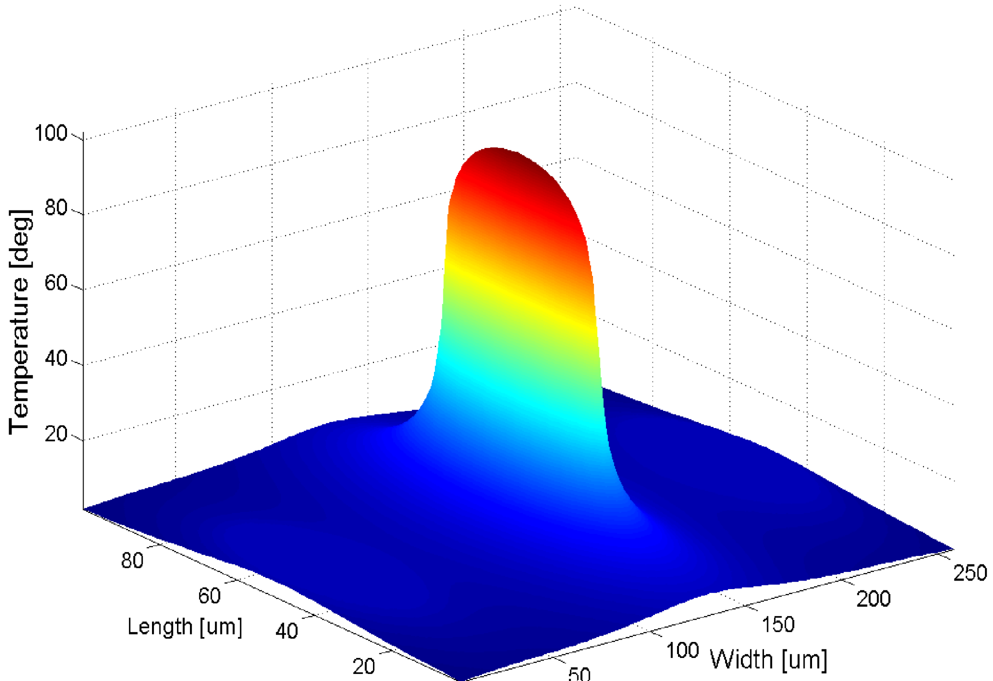

Figure 3.9. 3D thermal plot of the 1x40C at P_{tot}=0.265 W and k_{GaAs}=45.2 K/W.

In device modelling, the thermal resistance and the thermal capacitance, R_{TH} and C_{TH}, are the most interesting parameters. The thermal resistance will change with different power dissipation and with the changing of the ambient temperature. Thermal resistance at an ambient temperature of 25°C, for different power dissipations is shown in Table 3.6.

Table 3.6. R_{TH} at T_{amb} = 25 °C for different power dissipations.

	P_{tot} = 0.05W	P_{tot} = 0.1W	P_{tot} = 0.265W	P_{tot} = 0.4W
Estimated R_{TH} interval [K/W]	371 - 391	371 - 413	371 - 495	371 - 581
R_{TH} from [4] [K/W]	-	-	380	413

Thermal resistance at constant power dissipation of 0.4W, for different ambient temperatures is shown in Table 3.7.

Table 3.7. R_{TH} at P_{tot} = 0.4 W for different ambient temperatures.

	T_{amb} = 0.0°C	T_{amb} = 25°C	T_{amb} = 50°C	T_{amb} = 100°C
Estimated R_{TH} interval [K/W]	345 - 550	371 - 581	396 - 611	445 - 668
R_{TH} from [4] [K/W]	394	413	432	469

Table 3.7 shows that the results from [4] is well within the results[1] from the new estimation technique.

<u>Thermal Capacitance</u>:

The thermal capacitance is estimated from an equivalent volume approximating the transistors heated area. Figure 3.10 shows the cross-section of a single finger transistor.

The drawing in Figure 3.10 is not to scale. The width of the collector and the gold are just an approximation, since Caswell Technology did not provide exact numbers for these dimensions. The other dimensions are exact numbers from Caswell Technology.

One possible approximation to the equivalent volume, is to let the volume include the collector/emitter area and the part of the gold shown in Figure 3.10. The length of the transistor is 40 μm. Using (3.17), the thermal capacitance for this transistor is given in (3.18), assuming that the temperature dependence of the specific heat of gold is small compared to the uncertainty in the volume estimate.

$$C_{TH}(T) = C_{p,GaAs}(T)\,\rho_{GaAs}\,V_{GaAs} + C_{p,gold}\,\rho_{gold}\,V_{gold} \tag{3.18}$$

1. The results presented here are slightly different from the results presented in the published paper [5]. This is due to a small error in the paper, where the edge of the via hole is set to the edge of the octagonal metal plate on top of the via hole. See Figure 3.7.

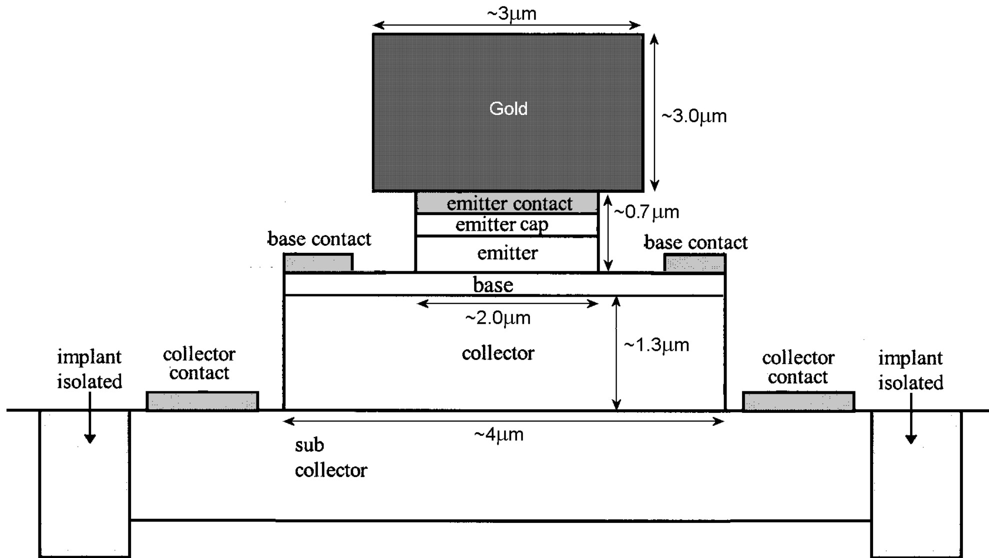

Figure 3.10. Cross section of the single finger transistor.

The volume, V_{GaAs}, of collector/emitter is calculated to be $2.6 \cdot 10^{-10}$ cm^3 and the volume, V_{gold}, of the gold is calculated to be $3.6 \cdot 10^{-10}$ cm^3, giving a thermal capacity of $C_{TH} = 1.4 \cdot 10^{-9}$ J/K at ambient temperature of 25 °C.

The thermal capacitance will change slightly with the temperature. In normal use the volume used in the estimation of the thermal capacitance, has a temperature close to the junction temperature. The thermal capacitance should be found using the temperature equal to the junction temperature. The thermal capacitance at different junction temperatures is shown in Table 3.8.

Table 3.8. C_{TH} at different junction temperatures.

	$T_j = 25$°C	$T_j = 100$°C	$T_j = 200$°C
Estimated C_{TH} [J/K]	$1.37 \cdot 10^{-9}$	$1.39 \cdot 10^{-9}$	$1.41 \cdot 10^{-9}$

Table 3.8 shows that the change in thermal capacity over the temperature is minimal. The use of the thermal capacity at an ambient temperature of 25 °C is well within the uncertainty of the volume estimation.

The thermal time constant is given by $\tau_{TH} = R_{TH} \cdot C_{TH}$. Using $R_{TH} = 380$ K/W from Table 3.6, the thermal time constant becomes $\tau_{TH} = 0.53$ μs. The thermal time constant for this device is reported from Caswell Technology to be somewhat smaller than 1 μs. The estimate of the thermal capacitance is somewhat smaller than the reported value, but more precise values were not available during this work. This type of estimate of the thermal capacitance, will be used for the transistors presented in the next sub-sections.

3.4.2 Single Finger 1x40 Transistor

In the single finger 1x40 transistor, the top level metal (metal 3) is connected at the short edge of the transistor. Metal 3 is then directly connected to a 8 µm wide metal 2 line. This line is then connected to the via holes in metal 2. The layout of this transistor is shown in Figure 3.11.

Thermal Resistance:

The thermal resistivity of metal 2 is about a factor of 6 higher than the thermal resistivity of metal 3, due to the difference in thickness. Compared to the 1x40C transistor, the metal lines is also much smaller in this transistor. This leads to a very high thermal resistance in the metal. The second assumption in Section 3.2.1 may not be completely valid for this transistor, because the metal 2 is not separated from the substrate by a polyimide layer. But since the thermal resistance in the metal for this transistor is large, this is ignored.

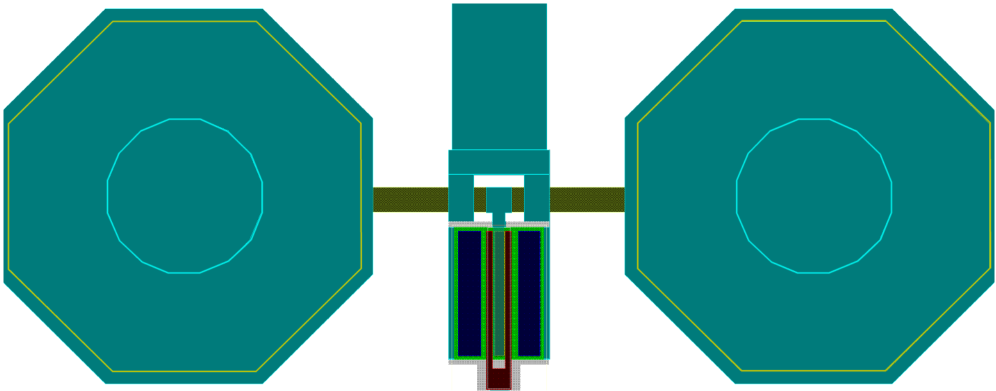

Figure 3.11. Layout of the 1x40 transistor.

Table 3.9 shows the results from the thermal simulation of the transistor for two different power dissipations, at an ambient temperature of 25 °C.

The simulation time was approximately the same for this transistor as for the 1x40C.

Table 3.9. Results for the single finger 1x40 transistor.

	Part A	*Part B*	*Part A*	*Part B*
Total dissipated power P_{tot} [W]	0.05	0.05	0.1	0.1
Power flowing in the metal [%]	4.2	4.8	4.2	5.6
Temp. at top of via hole $T_{M,via}$ [K]	0.1	0.1	0.2	0.3
Thermal conduction k_{GaAs} [W/m/K]	45.2	39.1	45.2	32.9
Junction temperature increase T_j [K]	**30.7**	**35.2**	**61.3**	**82.9**
Thermal Resistance R_{TH} [K/W]	613	704	613	829.2

This transistor is the one that will be electrically modelled in Chapter 4. The model for this transistor can be used as a basic unit for building other transistor configurations, by changing the value for R_{TH} and adding parasitic components. In the electrical IV measurements of this transistor the average power dissipation is about 0.05 W at an ambient temperature of 25 °C. An appropriate choice for the thermal resistance is R_{TH} = 650 K/W.

Table 3.10. R_{TH} at P_{tot} = 0.05 W for different ambient temperatures.

	T_{amb} = 0.0°C	T_{amb} = 25°C	T_{amb} = 50°C	T_{amb} = 100°C
Estimated R_{TH} interval [K/W]	549 - 630	613 - 704	676 - 780	808 - 933

If the transistor is to be used in an environment where the ambient temperature is different, or in close proximity to a heat source, the value for R_{TH} should be chosen according to Table 3.10.

It was not possible to compare these results to any measurements during this work, so there will be no further discussion on R_{TH} for this transistor.

Thermal Capacitance:
The geometry of this transistor is the same as the 1x40C transistor. They both have metal 3 connected to the emitter. So with respect to the thermal capacitance, this transistor is approximately equal to the 1x40C transistor, i.e. $C_{TH} = 1.4 \cdot 10^{-9}$ J/K.

3.4.3 4-Finger 4x40 Transistor

As shown in Figure 3.12 the 4-finger 4x40 transistor has a metal connections layout equivalent to that of the 1x40 transistor. The same assumptions as for the 1x40 transistor can be used for this transistor.

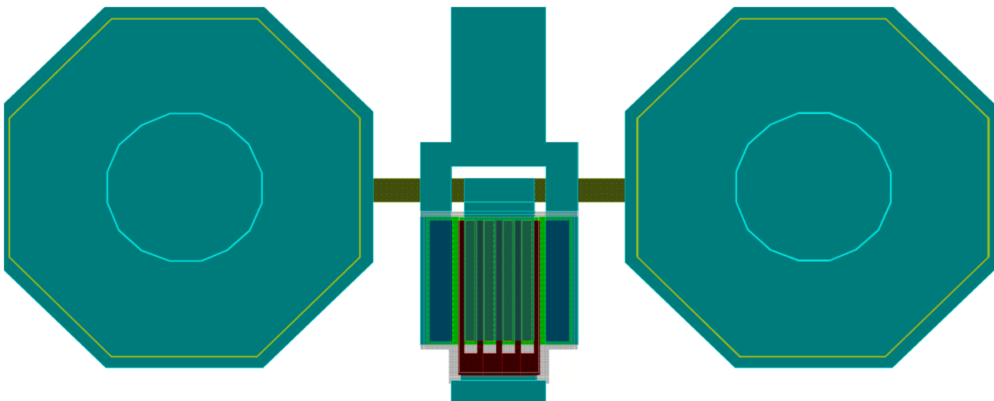

Figure 3.12. Layout of the 4x40 transistor.

Thermal Resistance:

Table 3.11 shows the results from *Part A* of the thermal simulation of the transistor at an ambient temperature of 25°C.

The simulation time was approximately 60 seconds for *Part A* and approximately 130 seconds for *Part B*. Both simulation times include the same type of calculations as the calculations for the 1x40C.

Table 3.11. Results for the 4-finger 4x40 transistor, *Part A*.

	Part A				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	-8.9	12.4	12.4	-8.9	3.5
Temp. at top of via hole $T_{M,via}$ [K]		0.4		0.4	0.4
Thermal conduction k_{GaAs} [W/m/K]		45.2		45.2	45.2
Junction temperature increase T_j [K]	**130.9**	**135.8**	**135.8**	**130.9**	**133.4**
Thermal Resistance R_{TH} [K/W]	1309	1358	1358	1309	333.4

Table 3.12 shows the results from *Part B* of the thermal simulation of the transistor at an ambient temperature of 25°C.

Table 3.12. Results for the 4-finger 4x40 transistor, *Part B*.

	Part B				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	-8.0	14.6	14.6	-8.0	6.6
Temp. at top of via hole $T_{M,via}$ [K]	0.7		0.7		0.7
Thermal conduction k_{GaAs} [W/m/K]	23.2		23.2		23.2
Junction temperature increase T_j [K]	**251.5**	**259.6**	**259.6**	**251.5**	**255.6**
Thermal Resistance R_{TH} [K/W]	2515	2596	2596	2515	638.9

In this transistor, only a very small part of the dissipated power is flowing into the via holes. The four closely spaced transistors have a common metal plate connecting the emitters together thermally. Due to this, the outside fingers actually receive dissipated power from the middle fingers. This is seen in Table 3.12 from the negative power flowing in the metal of finger 1 and 4.

The main results in Table 3.11 and Table 3.12 are the junction temperature interval. [3] measures/calculates the junction temperature increase to be T_j = 187 °C for the dissipated power of 0.4 W at an ambient temperature of 25 °C. This result fall well within the upper and lower limits calculated from the present estimation technique.

[3] also measures/calculates the junction temperature increase to be T_j = 215 °C for the dissipated power of 0.4 W at an ambient temperature of 85 °C. The present technique produces T_j = [166.4, 361.9] °C. This result also fall well within the upper and lower limits calculated from the present technique.

An isothermal plot of the 4x40 transistor is shown in Figure 3.13. The blue circles indicate the edge of the via holes.

In this case, the temperature calculated at the substrate surface was higher than the temperature, $T_{M,via}$, at the top of the via hole calculated from the heat transfer in the metal. The shaded area inside the via holes indicates where the temperature was higher than $T_{M,via}$, and where it now is lower due to the point source indicated with the black dot inside the via hole. In this case the point source is a negative one. The temperature inside the via hole is, due to the point source, lower than $T_{M,via}$. This is non physical, and the temperature inside the shaded area is therefore set equal to $T_{M,via}$.

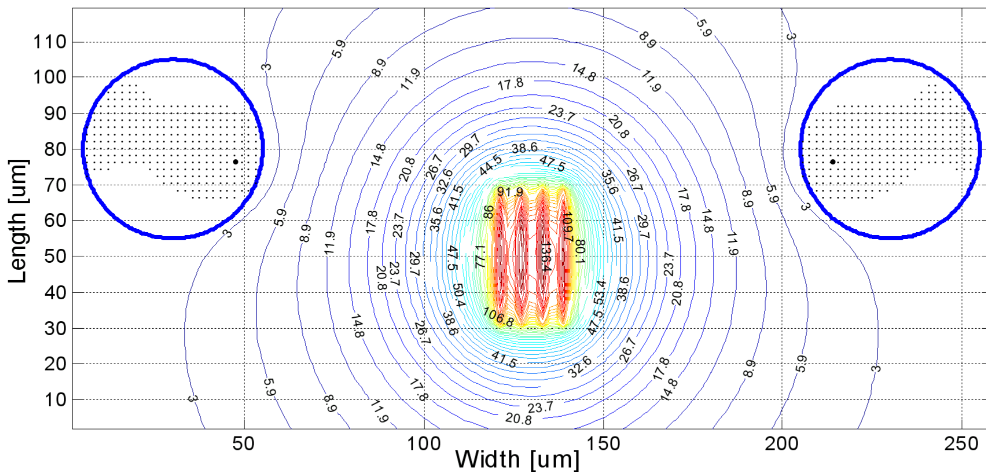

Figure 3.13. Isothermal plot of the 4x40 at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

In Figure 3.14 a 3D thermal plot is shown.

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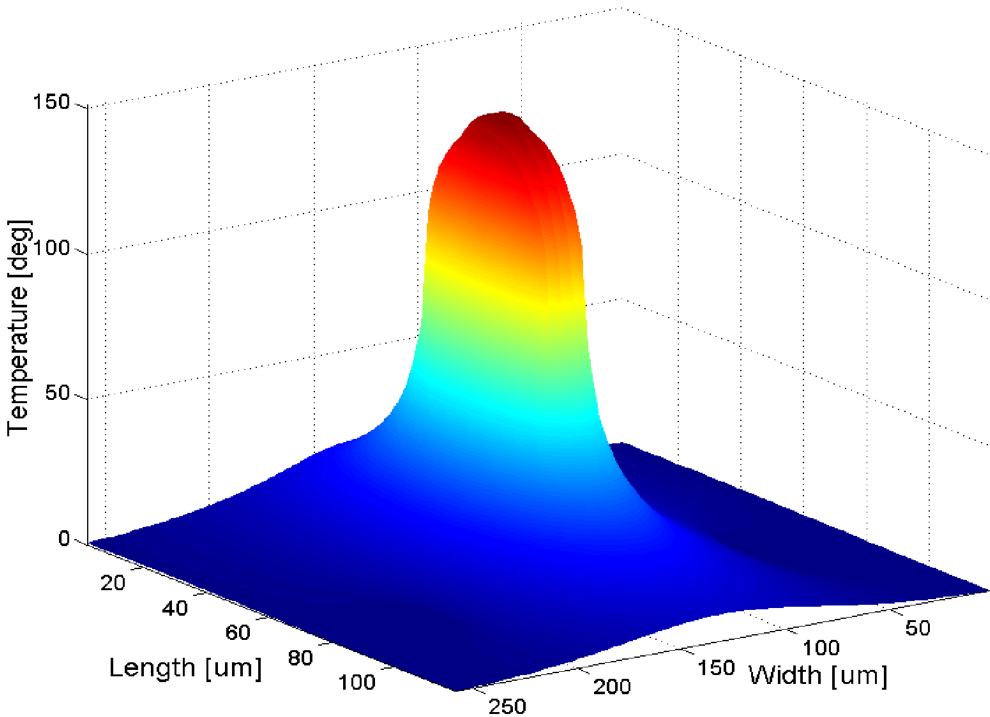

Figure 3.14. 3D thermal plot of the 4x40 at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

Thermal Capacitance:
Figure 3.15 shows the cross-section of a single finger transistor.

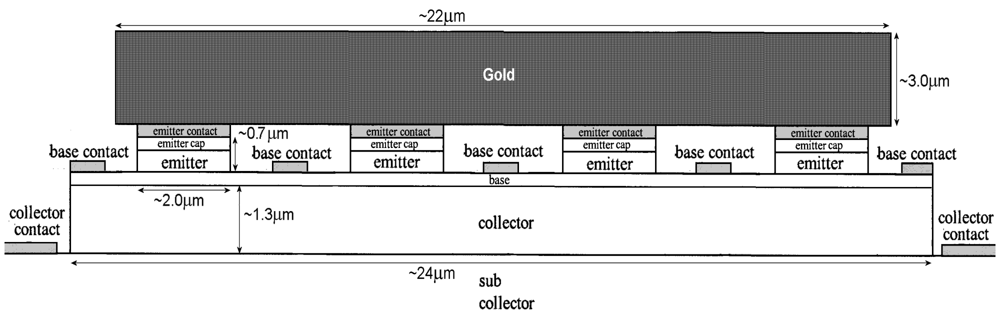

Figure 3.15. Cross section of the four finger transistor.

The drawing in Figure 3.15 is not to scale.

The equivalent volume for the thermal capacitance is chosen for this transistor to be the whole collector, the four emitter areas, and the part of the gold shown in Figure 3.15. The length of the transistor fingers is 40 µm. The volume of collector and emitter is $1.5 \cdot 10^{-9}$ cm^3 and the volume of the gold is $2.6 \cdot 10^{-9}$ cm^3, giving a thermal capacity of $C_{TH} = 9.3 \cdot 10^{-9}$ J/K.

3.4.4 4-Finger 4x40C Transistor, Thermally Shunted

The 4-finger 4x40C transistor, has a metal layout equivalent to that of the single finger 1x40C transistor. The layout of the 4x40C transistor is shown in Figure 3.16.

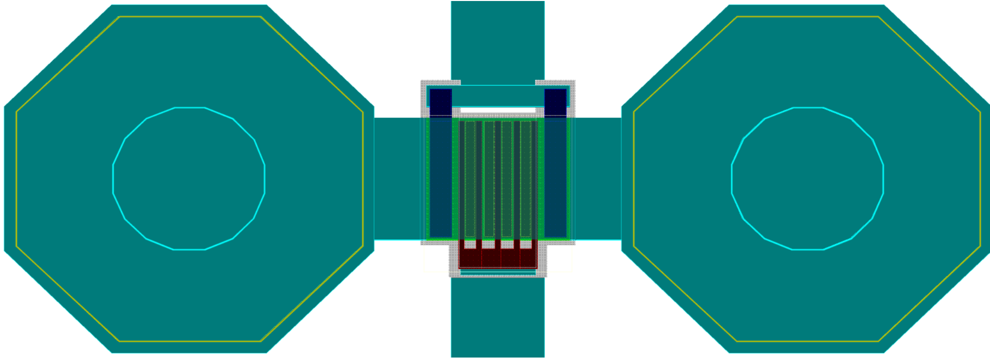

Figure 3.16. Layout of the 4x40C transistor.

Thermal Resistance:

Table 3.13 shows the results from *Part A* of the thermal simulation of the transistor at an ambient temperature of 25°C. The simulation time was approximately the same for this transistor as for the 4x40.

Table 3.13. Results for the 4-finger 4x40C transistor, *Part A*.

	Part A				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	18.3	23.4	23.4	18.3	22.6
Temp. at top of via hole $T_{M,via}$ [K]	4.8		4.8		4.8
Thermal conduction k_{GaAs} [W/m/K]	45.2		45.2		45.2
Junction temperature increase T_j [K]	**103.4**	**112.9**	**112.9**	**103.4**	**108.2**
Thermal Resistance R_{TH} [K/W]	1034.3	1129.1	1129.1	1034.3	270.4

Table 3.14 shows the results from *Part B* of the thermal simulation of the transistor at an ambient temperature of 25°C.

Table 3.14. Results for the 4-finger 4x40C transistor, *Part B*.

	Part B				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	28.3	35.7	35.7	28.3	32.0
Temp. at top of via hole $T_{M,via}$ [K]	6.8		6.8		6.8

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Table 3.14. Results for the 4-finger 4x40C transistor, *Part B*.

	Part B				
Finger no.	**1**	**2**	**3**	**4**	**All**
Thermal conduction k_{GaAs} [W/m/K]	24.8		24.8		24.8
Junction temperature increase T_j [K]	**163.4**	**175.9**	**175.9**	**163.4**	**169.7**
Thermal Resistance R_{TH} [K/W]	1634	1759	1759	1634	424.1

In this transistor a much higher part of the dissipated power is flowing into the via holes than for the 4x40 transistor, due to the thermal shunt to ground.

The main results in Table 3.13 and Table 3.14 are the junction temperature interval. In [3, 4], different methods are used to find the junction temperature from measurements. The junction temperature increase is found to be T_j = [153, 157]°C for the dissipated power of 0.4W at an ambient temperature of 25°C. This result fall well within the upper and lower limits calculated from the present estimation technique.

[3] also measures/calculates the junction temperature increase to be T_j = 197°C for the dissipated power of 0.4W at an ambient temperature of 85°C. The present technique produces T_j = [130.2, 196.5]°C. This result fall just outside the upper limit calculated from the present technique.

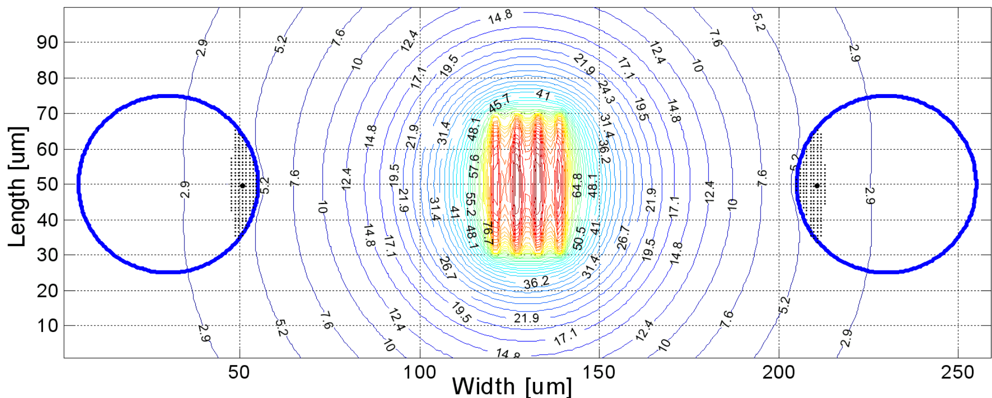

Figure 3.17. Isothermal plot of the 4x40C at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

An isothermal plot of the 4x40C transistor is shown in Figure 3.17. The blue circles indicates the edge of the via hole.

In Figure 3.18 a 3D thermal plot is shown.

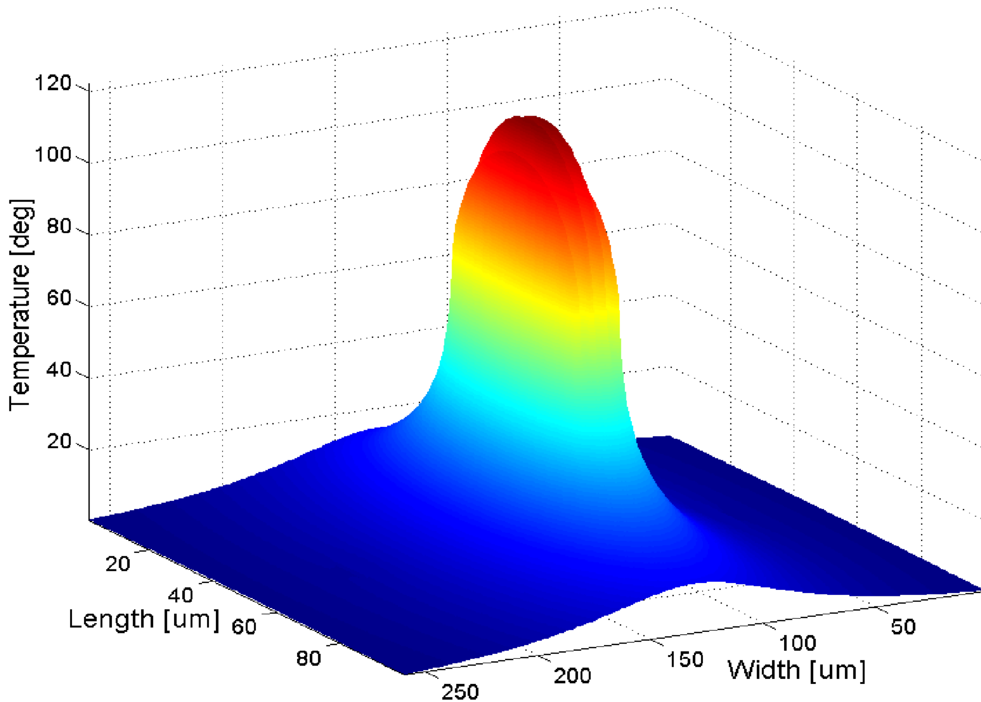

Figure 3.18. 3D thermal plot of the 4x40C at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

Thermal Capacitance:

The geometry of this transistor is the same as the 4x40 transistor. They both have metal 3 connected to the emitter. So in respect to the thermal capacitance, this transistor is approximately equal to the 1x40C transistor, i.e. $C_{TH} = 9.3 \cdot 10^{-9}$ J/K.

3.4.5 4-Finger P4x40 Transistor

The 4-finger P4x40 transistor, has a finger spacing of 50 µm. The emitters are connected to the via hole by metal 3, at the short edge of the emitter. The layout of this transistor is shown in Figure 3.19.

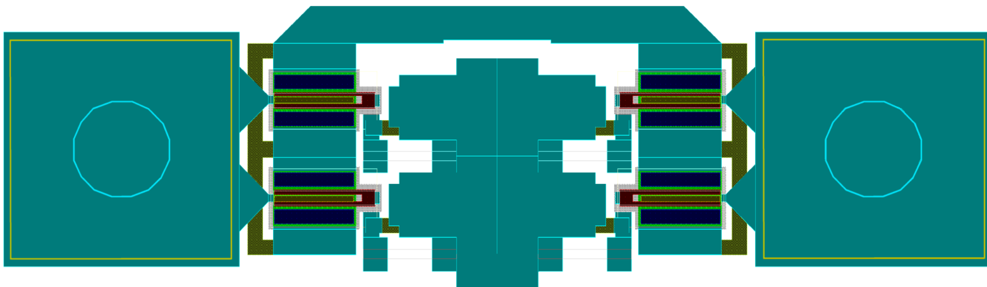

Figure 3.19. Layout of the P4x40 transistor.

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Thermal Resistance:

Table 3.15 shows the results from *Part A* of the thermal simulation of the transistor at an ambient temperature of 25°C. The simulation time was approximately 40 seconds for *Part A* and approximately 80 seconds for *Part B*. Both simulation times include the same type of calculations as the calculations for the 1x40C. Thermally, the transistor is symmetrical in both directions, giving the same results for all the fingers.

Table 3.15. Results for the 4-finger P4x40 transistor, *Part A*.

	Part A				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	7.9	7.9	7.9	7.9	
Temp. at top of via hole $T_{M,via}$ [K]	1.7		1.7		1.7
Thermal conduction k_{GaAs} [W/m/K]	45.2		45.2		45.2
Junction temperature increase T_j [K]	**68.7**	**68.7**	**68.7**	**68.7**	**68.7**
Thermal Resistance R_{TH} [K/W]	687.4	687.4	687.4	687.4	171.9

Table 3.16 shows the results from *Part B* of the thermal simulation of the transistor at an ambient temperature of 25°C.

Table 3.16. Results for the 4-finger P4x40 transistor, *Part B*.

	Part B				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	10.9	10.9	10.9	10.9	10.9
Temp. at top of via hole $T_{M,via}$ [K]	2.3		2.3		2.3
Thermal conduction k_{GaAs} [W/m/K]	31.5		31.5		31.5
Junction temperature increase T_j [K]	**95.3**	**95.3**	**95.3**	**95.3**	**95.3**
Thermal Resistance R_{TH} [K/W]	953.1	953.1	953.1	953.1	238.3

In this transistor only between 7.9% and 10.9% of the dissipated power is flowing into the via holes, due to the metal 3 being connected to the short edge of the fingers.

The main results in Table 3.15 and Table 3.16 are the junction temperature interval. In [3], different methods are used to find the junction temperature from measurements. The junction temperature increase is found to be T_j = 89 °C for the dissipated power of 0.4 W at an ambient temperature of 25 °C. This result fall well within the upper and lower limits calculated from the present junction estimation technique.

[3] also measures/calculates the junction temperature increase to be T_j = 102 °C for the dissipated power of 0.4W and ambient temperature of 85 °C. The present technique produces T_j = [85.4, 118.0] °C. This result fall well within the upper and lower limit calculated from the present technique.

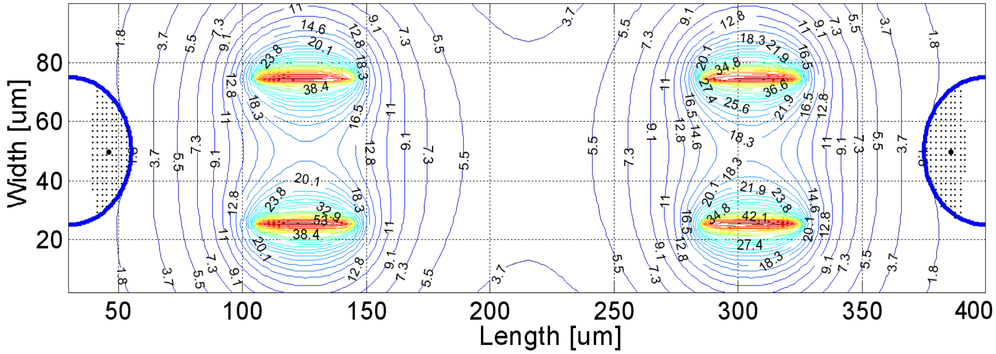

Figure 3.20. Isothermal plot of the P4x40 at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

An isothermal plot of the P4x40 transistor is shown in Figure 3.20.
In Figure 3.21 a 3D thermal plot is shown.

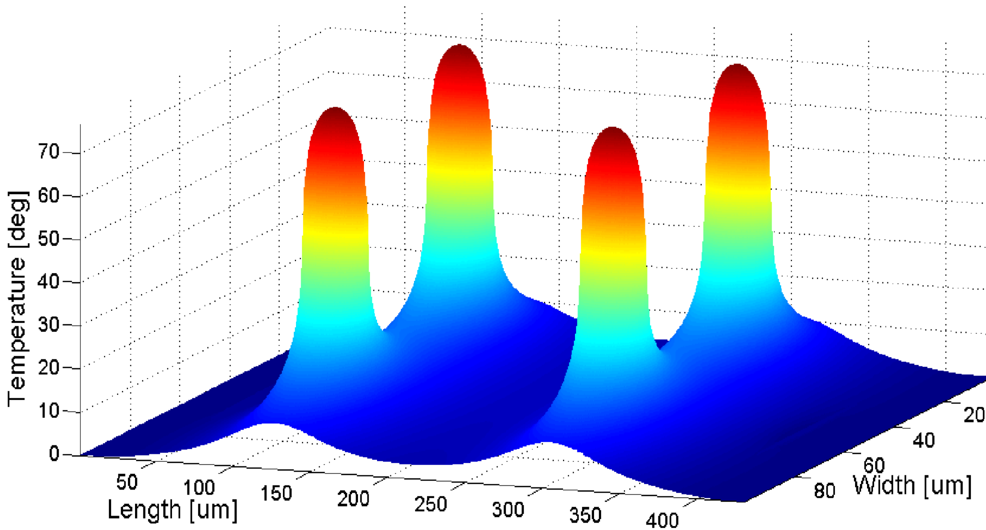

Figure 3.21. 3D thermal plot of the P4x40 at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

Thermal Capacitance:
This transistor is built using four single finger transistors. It is therefore fair to assume that the thermal capacity of this transistor will be approximately the sum of the thermal capacity of each finger. The thermal capacity is estimated to be C_{TH} = $5.6 \cdot 10^{-9}$ J/K.

3.4.6 4-Finger P4x40C Transistor, Thermally Shunted

The 4-finger P4x40C transistor, has a finger spacing of 50 µm. Metal 3 from each of the via holes is directly covering the entire finger structure, making a good thermal shunt to the ground. The layout of this transistor is shown in Figure 3.22.

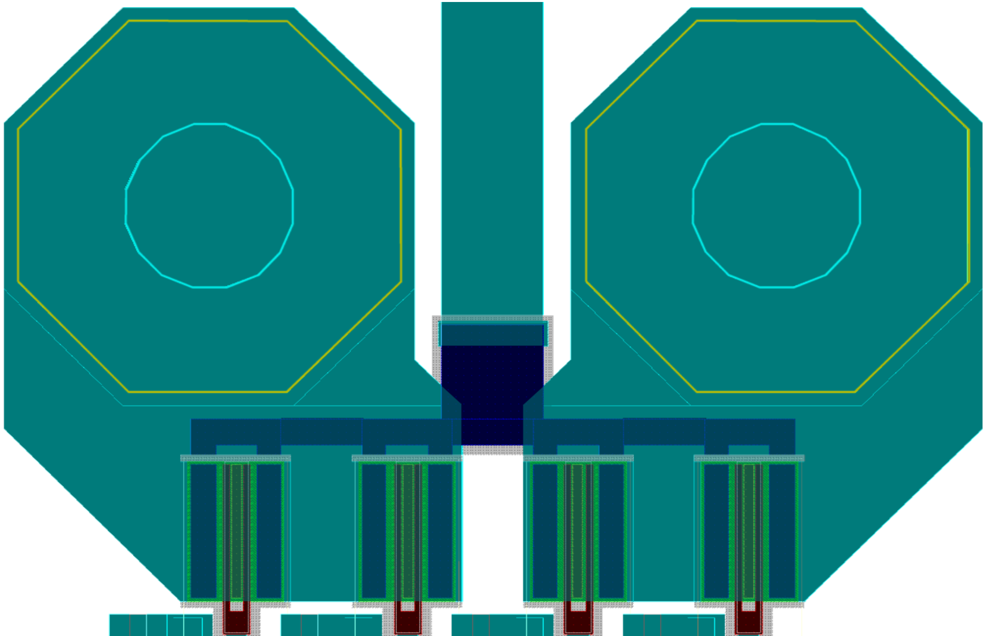

Figure 3.22. Layout of the P4x40C transistor.

Thermal Resistance:

Table 3.17 shows the results from *Part A* of the thermal simulation of the transistor at an ambient temperature of 25 °C.

The simulation time was approximately the same for this transistor as for the P4x40.

Table 3.17. Results for the 4-finger P4x40C transistor, *Part A*.

	Part A				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	20.3	18.5	18.5	20.3	19.4
Temp. at top of via hole $T_{M,via}$ [K]	4.1		4.1		4.1
Thermal conduction k_{GaAs} [W/m/K]	45.2		45.2		45.2
Junction temperature increase T_j [K]	**60.7**	**65.1**	**65.1**	**60.7**	**62.9**
Thermal Resistance R_{TH} [K/W]	607.2	651.0	651.0	607.2	157.3

Table 3.18 shows the results from *Part B* of the thermal simulation of the transistor at an ambient temperature of 25°C.

Table 3.18. Results for the four finger P4x40C transistor, *Part B*.

	Part B				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]	0.1	0.1	0.1	0.1	0.4
Power flowing in the metal [%]	25.6	23.7	23.7	25.6	24.7
Temp. at top of via hole $T_{M,via}$ [K]	5.2		5.2		5.2
Thermal conduction k_{GaAs} [W/m/K]	32.7		32.7		32.7
Junction temperature increase T_j [K]	**78.3**	**84.2**	**84.2**	**78.3**	**81.3**
Thermal Resistance R_{TH} [K/W]	783.3	842.1	842.1	783.3	203.2

In this transistor a much higher part (between 19.4% and 24.7%) of the dissipated power is flowing into the via holes than for the P4x40 transistor.

The main results in Table 3.17 and Table 3.18 are the junction temperature interval. In [3, 4] the junction temperature is found to be T_j = [71.8, 80.3]°C for the dissipated power of 0.4W and ambient temperature of 25°C. This result fall well within the upper and lower limits calculated from the present estimation technique.

[3] also measures/calculates the junction temperature increase to be T_j = 98 °C for the dissipated power of 0.4 W and ambient temperature of 85 °C. The present technique produces T_j = [76.5, 98.1] °C.

An isothermal plot of the P4x40C transistor is shown in Figure 3.23.

In Figure 3.24 a 3D thermal plot is shown.

Thermal Capacitance:

This transistor is also built using four single finger transistors. The thermal capacity is therefore assumed to be approximately the same as for the P4x40 transistor, i.e. $C_{TH} = 5.6 \cdot 10^{-9}$ J/K.

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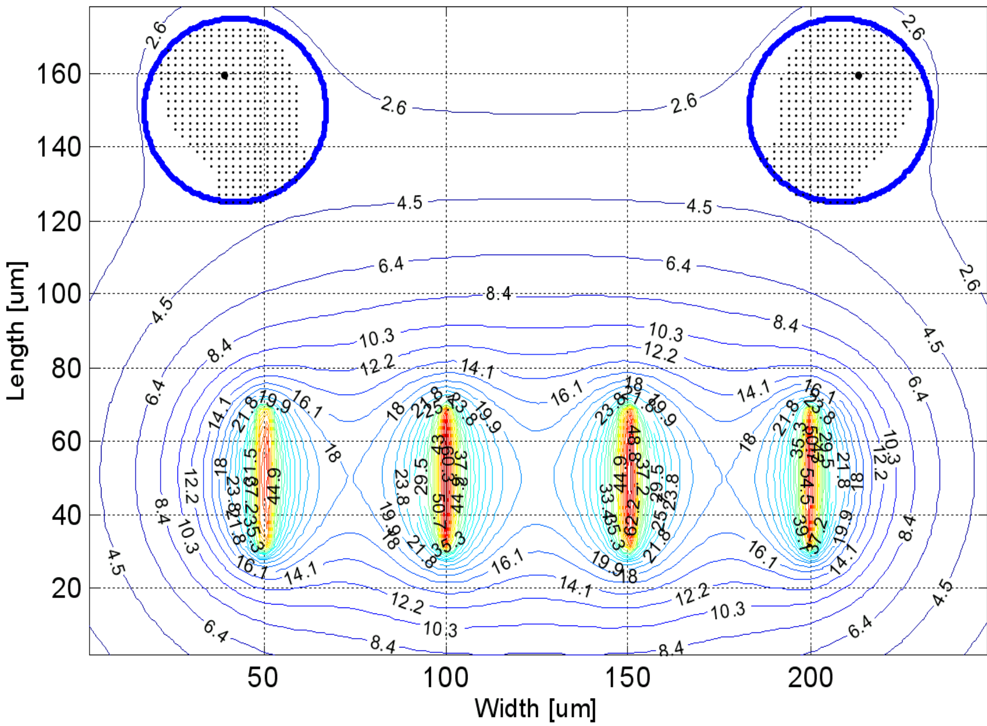

Figure 3.23. Isothermal plot of the P4x40C at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

Figure 3.24. 3D thermal plot of the P4x40C at P_{tot} = 0.4 W and k_{GaAs} = 45.2 K/W.

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3.5 Results for the SiGe HBT

The layout of three of the SiGe transistors is shown in Figure 3.25. Almost no information were given about the transistors as stated in Chapter 2. Due to the lack of information about the thickness of the metal, the thermal conductivity in the metal had to be disregarded. The analysis of the transistors will therefore only include the thermal conduction of the substrate. The exclusion of the thermal conduction in the metal does not generate large errors in the estimated thermal resistance. There are several reasons for this. From the layout in Figure 3.25, there seems to be no via holes making a thermal shunt to the backside of the substrate. This combined with the fact that the thermal conductivity of aluminium is lower than that of gold, will result in just a small part of the dissipating power flowing in the metal. Since the thermal conductivity of Si is 3-4 times that of GaAs, the junction temperature will be lower for the same dissipated power. This also reduces the part of the power flowing in the metal.

The transistor will have some small part of the dissipated power flowing in the metal. Since this is disregarded in the thermal simulations, the results from these simulations will be slightly higher than the real values.

Only the three transistors shown in Figure 3.25 will be analysed in the next sections.

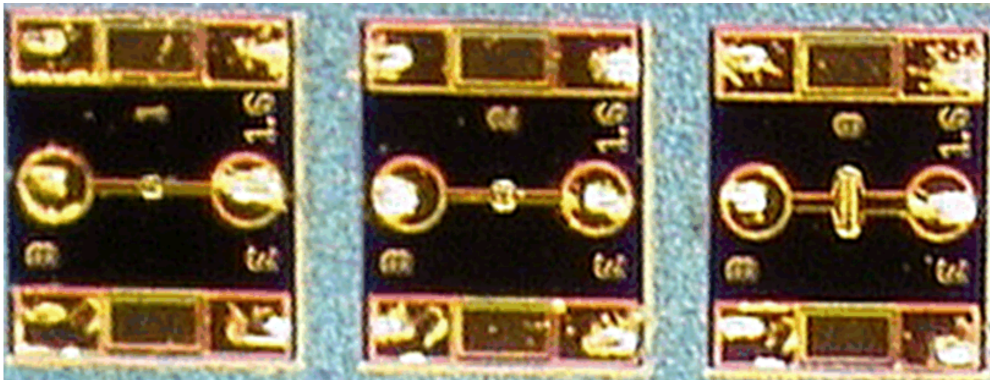

Figure 3.25. Layout of three SiGe transistors.

3.5.1 Single Finger Transistor

The single finger transistor is the transistor shown to the left in Figure 3.25. The emitter is 1.6 µm wide and 10 µm long. Table 3.19 shows the simulation results for the junction temperature and the thermal resistance for different dissipated powers at an ambient temperature of 26 °C.

Table 3.19. Thermal resistance R_{TH} of the single finger SiGe transistor.

	Part A	*Part B*	*Part A*	*Part B*	*Part A*	*Part B*
Total dissipated power P_{tot} [mW]	10	10	25	25	50	50
Thermal conduction k_{SiGe} [W/m/K]	170.9	166.3	170.9	159.5	170.9	147.8
Junction temperature increase T_j [K]	5.7	5.8	14.1	15.1	28.2	32.6
Thermal Resistance R_{TH} [K/W]	**564**	**582**	**564**	**605**	**564**	**652**

Table 3.20 shows the simulation results for the thermal resistance for different ambient temperatures at a dissipated power of 25 mW.

Table 3.20. R_{TH} at P_{tot} = 0.025W for different ambient temperatures.

	T_{amb} = **0.0**°C	T_{amb} = **26**°C	T_{amb} = **50**°C	T_{amb} = **100**°C
Estimated R_{TH} interval [K/W]	497 - 532	564 - 605	628 - 675	767 - 828

It was not possible to estimate the thermal capacitance of the single finger transistor, due to the lack of information.

3.5.2 2-Finger Transistor

The 2-finger transistor is the transistor shown in the centre of Figure 3.25. The emitter dimensions are equal to that of the single finger transistor. Table 3.21 shows the simulation results for the junction temperature and the thermal resistance for a dissipated powers of 50 mW, at an ambient temperature of 26 °C.

Table 3.21. Thermal resistance R_{TH} of the 2-finger SiGe transistor.

	Part A			**Part B**		
Finger no.	**1**	**2**	**All**	**1**	**2**	**All**
Total dissipated power P_{tot} [mW]	25	25	50	25	25	50
Thermal conduction k_{SiGe} [W/m/K]			170.9			156.9
Junction temperature increase T_j [K]	17.3	17.3	17.3	18.8	18.8	18.8
Thermal Resistance R_{TH} [K/W]	691	691	**346**	752	752	**376**

It was not possible to estimate the thermal capacitance of the 2-finger transistor, due to the lack of information.

3.5.3 8-Finger Transistor

The 8-finger transistor is the transistor shown to the right in Figure 3.25. Each emitter dimensions are equal to that of the single finger transistor. Table 3.22 shows the thermal simulation results for the junction temperature and the thermal resistance from *Part A*, for a dissipated power of 120 mW at an ambient temperature of 28 °C. From symmetry considerations, only four of the fingers are shown.

Table 3.22. Thermal resistance R_{TH} of the 8-finger transistor, *Part A*.

	Part A				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]					0.12
Thermal conduction k_{SiGe} [W/m/K]					170.9
Junction temperature increase T_j [K]	13.3	15.0	15.7	16.0	15.0
Thermal Resistance R_{TH} [K/W]	890	1001	1047	1066	**125.1**

Table 3.23 shows the simulation results for the junction temperature and the thermal resistance from *Part B*, for a dissipated power of 120 mW at an ambient temperature of 28 °C. From symmetry considerations, only four of the fingers are shown.

Table 3.23. Thermal resistance R_{TH} of the 8-finger transistor, *Part B*.

	Part A				
Finger no.	**1**	**2**	**3**	**4**	**All**
Total dissipated power P_{tot} [W]					0.12
Thermal conduction k_{SiGe} [W/m/K]					157.9
Junction temperature increase T_j [K]	14.5	16.2	17.0	17.3	16.2
Thermal Resistance R_{TH} [K/W]	963	1082	1133	1153	**135.3**

Figure 3.26 shows an isothermal plot of the 8-finger SiGe transistor at a dissipated power of 0.12 W. Figure 3.27 shows a 3D thermal plot of the 8-finger SiGe transistor at a dissipated power of 0.12 W.

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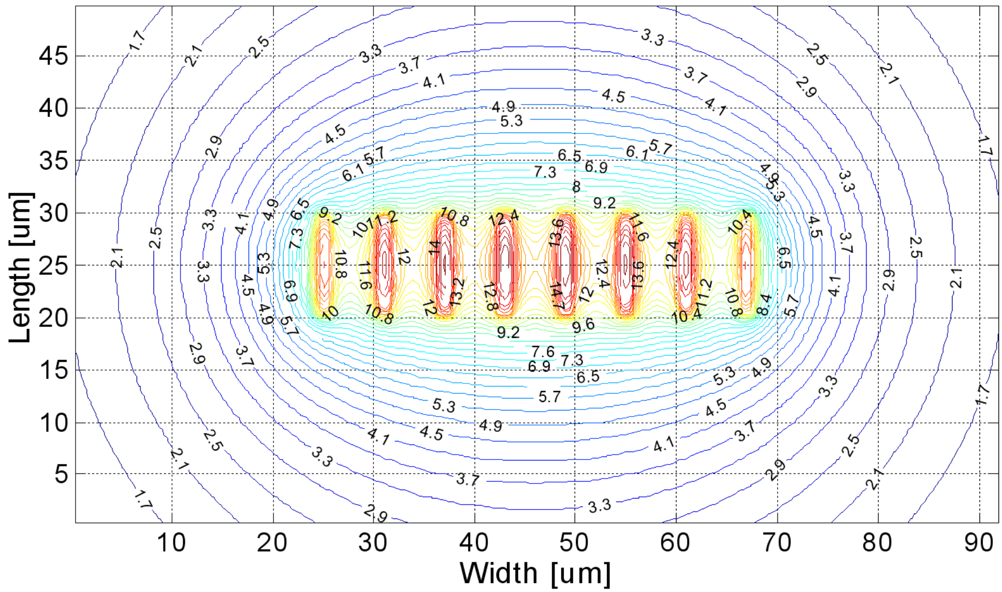

Figure 3.26. Isothermal plot of the 8-finger transistor (P_{tot}=0.12W, k_{SiGe}=170.9K/W).

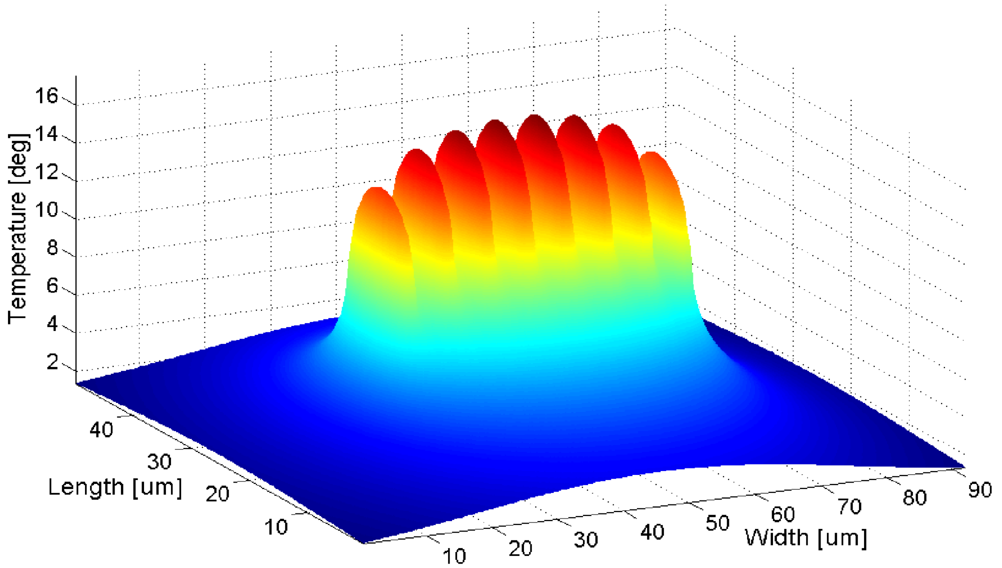

Figure 3.27. 3D thermal plot of the 8-finger transistor (P_{tot}=0.12W, k_{SiGe}=170.9K/W).

3.6 Conclusion

In this chapter, a new practical technique for estimating the junction temperature and the thermal resistance of an HBT was developed. This technique has been published by the author in 2002 [5], and can be found in Appendix A.1. The new technique estimates an interval for the junction temperature. The main assumption in the new technique is that the junction temperature can be calculated from three separate phenomena:

- Thermal conduction of the substrate.
- Thermal conduction of the metal connecting the emitter to the via holes.
- The effects of the via holes on the substrate temperature.

The main features of the new technique are:

- The junction temperature and the thermal resistance are calculated from a few physical properties and the layout of the transistors.
- The only required software tool is a mathematical program like MATLAB.
- The calculation time is very short compared to a full 3D thermal simulation.
- The technique is easy to use for the circuit designer.

The new technique shows good accuracy, when applied to several InGaP/GaAs HBT's from Caswell Technology, and compared to the results from other methods in [3, 4]. All the results presented in [3, 4] fall well within the estimated junction temperature intervals from the new technique, except for the 4x40C transistor evaluated at 85 °C, where the result is just outside the estimated interval. As an example of the results from new technique, the estimated junction temperature increase - relative to the ambient temperature - for the P4x40C is calculated to be T_j = [62.9, 81.3] °C. In [3, 4] the junction temperature increase is found using two different techniques which give T_j = 71.8 °C and T_j = 80.3 °C. These results are all found for a dissipated power of 0.4 W at an ambient temperature of 25 °C.

A simple method for estimating the thermal capacitance was also developed. This method was applied to the 1x40C transistor giving an $C_{TH} = 1.4 \cdot 10^{-9}$ J/K. Using the thermal resistance R_{TH} = 380 K/W from Table 3.6, the thermal time constant becomes τ_{TH} = 0.53 μs. Caswell Technology reports the thermal time constant to be somewhat smaller than 1 μs. From this the method can be assumed to have good accuracy.

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Chapter 4 HBT Modelling

Modern electronic systems are using active semiconductor devices in many applications. These devices work in different operating regions when the applied AC signal amplitude is high. A linear small-signal device model, which is a good approximation around a particular operating point, is no longer valid. Therefore the nonlinear behaviour of the device must be considered. For some cases, the device nonlinearity is the key function used to achieve rectification, mixing, signal-doubling etc. On the other hand, the nonlinearity of the device may be harmful to the system performance, such as nonlinear distortion in the linear power amplifier. Therefore, good nonlinear device models are extremely important to the circuit designer. The ability to achieve "first time" design success depends strongly on the quality and accuracy of the nonlinear device models.

The objective in this chapter is to develop a practical parameter extraction method for the VBIC[1] model, used on an InGaP/GaAs HBT. A background on modelling concepts and the reasons for choosing the VBIC model are also given.
The parameter extraction method is evaluated on an InGaP/GaAs HBT from Caswell Technology, and on a SiGe/Si chip with HBT's.

1. VBIC - Vertical Bipolar Inter-Company model.

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4.1 Modelling Concepts

Todays active microwave devices requires advanced nonlinear models. It is difficult, if not impossible, to make a perfect nonlinear model for such devices. Some of the reasons for this are:

- Many currently-used microwave devices, such as the MESFET, BJT, HEMT etc., often present complex internal nonlinear behaviour [42-44]. Some of their nonlinear behaviour is still difficult to model and to simulate using available techniques.
- Thermal effects, like self-heating, changes the behaviour of the device significantly, and become more and more important when the devices have to handle higher powers and at the same time the chips get smaller in size.
- Parasitic effects strongly influence device characteristics, at high frequencies. In both the frequency- and time- domain the microwave devices often present very complex characteristics.
- At high signal frequencies, the device may no longer be considered as a device with lumped elements, and therefore distributed effects (linear and nonlinear) must be taken into account. It may be difficult to solve in a compact way the partial differential and/or integral equations which often are associated with distributed effects.

For linear device models there exist different general-purpose procedure for making models. There is no standardised general-purpose procedure to create a nonlinear model. Techniques for creating a nonlinear model are not yet mature.

At zero frequency, the model degenerates to the DC model (static). At a fixed bias point with a low signal amplitude, the model degenerates to a small-signal AC model. A small-signal AC model can usually cover the frequency band from DC to infinity. When a large signal amplitude is applied to a standard nonlinear model, it is usually not valid for the whole frequency spectrum, and it is usually only valid in some operating regions with limited accuracy.

In microwave device modelling there are three terms that are widely used: Static, quasi-static and non quasi-static models. An example of a static model is as stated before, a DC model of a transistor. There have been stated several definitions of the term quasi-static in the literature. One widely accepted definition [45] of quasi-static is: In cases where a nonlinear device model can be constructed entirely by a combination of static or DC measurement results plus small-signal AC measurements around an appropriate set of static bias points, then the model may be termed a ‘quasi-static’ model. At very high frequencies, the quasi-static assumption may not be valid if the carrier diffusion time and transit time (distributed effects) become comparable to the period of the signal. The quasi-static assumption may also not be valid at very low frequencies where the device may suffer from hysteresis effects i.e. self-heating,

etc. Since self-heating is a low frequency effect, the quasi-static model may still be used at high frequencies.

A non quasi-static model covers the area in modelling that is not covered by a static or a quasi-static model. A fully physical model is a non quasi-static model.

4.1.1 Physical Models

Physical models are the most accurate models. They are based on exact knowledge of the devices dimensions, doping profiles etc. The model itself is built up by solving drift-diffusion equations, Schrodinger equation, and thermal diffusions equations together in three dimensions. Still there are unknowns like errors in the crystal lattice causing traps etc. An example of an physical model is given in [46].

The main advantages with this kind of models are:

- High accuracy. The model describes the physical behaviour almost exact (Traps etc. may cause some uncertainty).

The main disadvantages with this kind of models are:

- Simulation time. Typical simulation time for one single device, biased at one operating point with a small RF signal applied, can be several hours. In a circuit with just a few components, the simulation time become impractical even with the fastest computers today. Simulations with large RF signals and optimizations are not an option.
- Physical details. The circuit designer does not usually have the necessary details of a particular process to use physical models. Usually foundries and manufactures do not want to give out such detailed information of their processes.

4.1.2 Physics Based Analytical Models

Physics based analytical models are at the present the most important commonly used approach in todays modelling. Most of these models are quasi-static, or quasi-static with some additions, i.e. self-heating. The basic approach for this kind of modelling is to first study the physical properties of the device. Second, analytically solving the device equations. Third, simplify the solutions in such way that the final equations are easily solved on a computer (removing discontinuities in the analytical functions and its derivatives, etc.). And fourth, creating a circuit model which describes the analytical solutions.

Usually, for a bipolar transistor, a one-dimensional representation can be a good approximation to the intrinsic behaviour of a real device. Using several assumptions, these equations can be simplified resulting in ordinary differential equations and solutions obtained using the boundary conditions. Using this approach, a circuit model can be found by combining several nonlinear resistors, capacitors (diodes) and controlled current sources. Two good examples of this are the Ebers-Moll model [47] and the Gummel-Poon model [48].

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Many modern device models have been invented using the four steps explained above, for example, HICUM (High Current Model) [49-51], Philips MEXTRAM [52], VBIC-95 (Vertical Bipolar Intercompany) model [53] and many others [44, 54-70]. The VBIC-95 (called VBIC in the following) model will be used for parameter extraction in Section 4.2 and the following chapters.

The main advantages with this kind of models are:

- Simulation time. The analytical equations are easily solved on computers. Complete circuits with many active and passive components can be simulated within minutes. Optimizations and simulations with large RF signals are easily done.
- Easy to understand. It is easy to understand the behaviour of models which are built up this way. There usually exist a rather simple equivalent circuit diagram of the model.
- Good accuracy. This kind of models usually have good accuracy in the operating area where the model is valid.

The main disadvantages with this kind of models are:

- Validity. The validity of the model depends on the validity of the physical analysis of the device and the validity of all the approximations made during the process to derive the final circuit model. Examples of this are limited bandwidth of the model, and limited area of the active region which the model can be used.

4.1.3 ‘Black Box' Analytical Model

The ‘black box’ model is based on experimental results which are carefully observed. By analyzing the relationships between the input responses and the output responses, the relationships may be described by a set of mathematical equations. [71] shows a typical ‘black box’ model.

The main advantages with this kind of models are:

- Simulation time. The mathematical equations are easily solved on computers.
- Unknown devices. The ‘black box’ model is very useful when the device physics and operating principles are unknown.
- Fair/Good accuracy. The accuracy depends on how many responses that have been used as a basis for the mathematical equations.

The main disadvantages with this kind of models are:

- No physical relations. The model can not give direct physical explanations of device properties.

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- Validity. The validity of the model depends on how many responses that make up the basis for the mathematical equations. Theoretically, one should use infinite number of responses to ensure a valid model for all possible kinds of excitations.

4.1.4 Models Based on Look Up Tables

The look up table models uses tabular data instead of analytical equations. The tabular data are usually obtained by measurements. The model uses a data table to store the complete measurement data sets. The model uses splines to perform the necessary interpolations. [72, 73] show examples of this model type.

The main advantages with this kind of models are:

- Simulation time. The simulations can be very fast, due to the use of look up tables.
- Process independent. The model is process independent. Almost any device can be modelled with this model, as long as all the necessary measurements can be made.
- Fair/Good accuracy. The accuracy depends on how detailed the measurements are, and how well-behaved the device is.

The main disadvantages with this kind of models are:

- No physical relations. The model can not give direct physical explanations of device properties.
- Validity. The model uses interpolation, and therefore the use of the model must be well within the area covered by the measurements. The measurements must cover a wide range of DC biases, frequencies and powers.
- Complexity of measurements. The measurements may get very complex, i.e. it may be difficult (require specialized measurement equipment) to find the output impedance of a high power device. A more physical based model can use only a few measurements and then accurately extrapolate the response outside the measurements.

4.2 Model Choice and Parameter Description

In the resent years many papers have been published describing new models for the HBT [44, 49-73]. The models all have their advantages/disadvantages.

Choosing a model is a difficult task. The model choice depends on which device that is to be modelled, the accuracy needed etc. In this work the criteria for choosing model have been:

- The model should be able to model second order effects like self heating etc.
- The model should have good accuracy.
- The model should be implemented in commercial simulators like Agilent (HP) ADS.
- The model should, if possible, have some resemblance to earlier well established models.

From the criteria above the model should be chosen from the quasi-static model group. The most promising models for the HBT are the HICUM, MEXTRAM and VBIC models. They all model second order effects. The MEXTRAM and VBIC models are both implemented in Agilent ADS. All models have good accuracy.

The choice fell on the VBIC model due to the fact that this model is almost (with a certain set of parameters) backwards compatible with the well-known Gummel-Poon model [48].

4.2.1 The VBIC Model

The VBIC model [53] was developed by some of the large companies in the silicon industry like Motorola, Texas Instruments, Analog Devices, Hewlett-Packard, IBM etc.

The main purpose of making this model, was to look at all published models at that time, and select the best feature from them all. The result was the VBIC model. The model is an open source model, with all information public available. Figure 4.1 show the schematic of the VBIC model.

The main advantages and improvements of the VBIC model over the Gummel-Poon model are:

- Self heating.
- Excess phase.
- Improved depletion capacitance model.
- C_∞ continuous modelling (no discontinuities in the derivatives).
- Quasi-saturation.
- Avalanche modelling in base-collector.
- Parasitic substrate transistor.

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- Improved Early effect modelling.
- Distributed base.

The VBIC model is discussed in detail by [74, 75]. The VBIC model was originally made for silicon BJT's, but it will be shown that it has all the necessary features needed for modelling an InGaP/GaAs HBT.

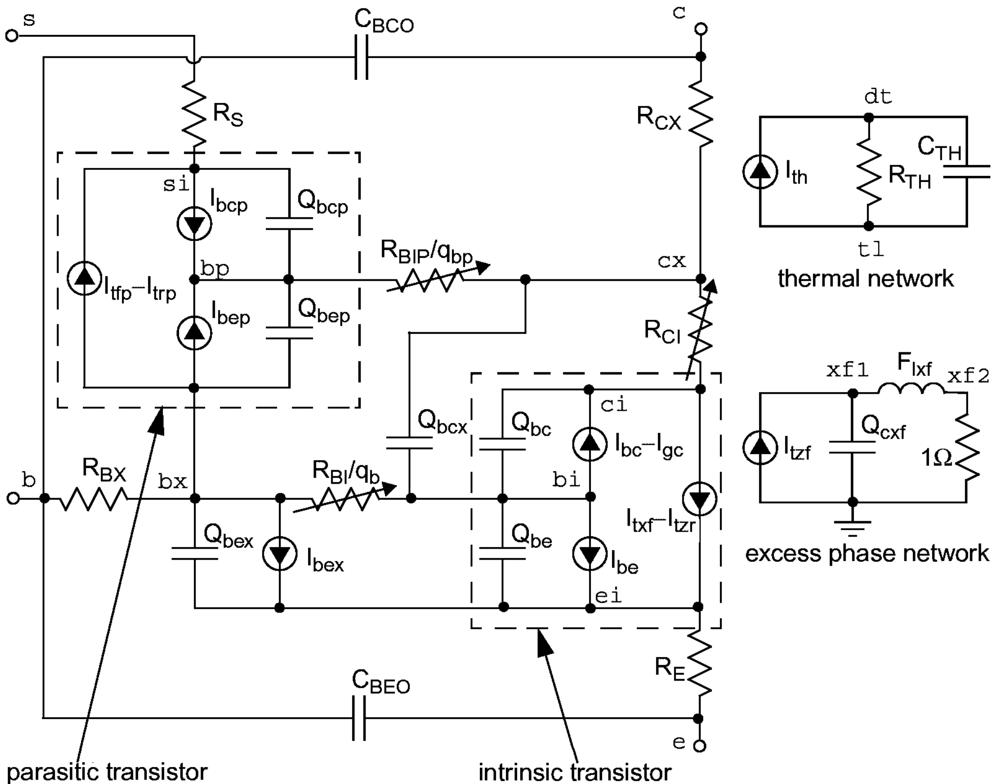

Figure 4.1. The VBIC model.

Many papers have been published on parameter extraction [76-85] for different models of bipolar transistors. As far as the author knows, at the time when [6] was published, only one paper [86] demonstrated a method of parameter extraction for a silicon BJT with the VBIC model. In the following sections, a practical parameter extraction algorithm will be developed for the VBIC model used on a InGaP/GaAs HBT. This algorithm will also be used on a SiGe HBT, at the end of this chapter.

The symbols used for the model parameters in the next sections are all taken from the VBIC model implementation in Agilent ADS.

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4.2.2 DC Parameters of the Junctions

The DC parameters that are associated with the junctions are the saturation currents and the emission coefficients. In the VBIC model the transistor are divided in two regions: the base-emitter region and base-collector region. In the base-emitter region, (4.1) describes the intrinsic base-emitter current, I_{be}, as a function of the intrinsic base-emitter voltage, V_{bei}. This equation include a non-ideal effect given by the second part of the equation. (4.2) describes the intrinsic forward transport current, I_{tzf}, as a function of the intrinsic base-emitter voltage, V_{bei}.

$$I_{be} = \mathrm{I_{BEI}}\left(e^{\frac{qV_{bei}}{\mathrm{N_{EI}}kT}} - 1\right) + \mathrm{I_{BEN}}\left(e^{\frac{qV_{bei}}{\mathrm{N_{EN}}kT}} - 1\right) \tag{4.1}$$

$$I_{tzf} = \mathrm{I_S}\left(e^{\frac{qV_{bei}}{\mathrm{N_F}kT}} - 1\right) \tag{4.2}$$

In the base-collector region, (4.3) describes the intrinsic base-collector current, I_{bc}, as a function of the intrinsic base-collector voltage, V_{bci}. This equation also include a non-ideal effect given by the second part of the equation. (4.4) describes the intrinsic reverse transport current, I_{tzr}, as a function of the intrinsic base-collector voltage, V_{bci}.

$$I_{bc} = \mathrm{I_{BCI}}\left(e^{\frac{qV_{bci}}{\mathrm{N_{CI}}kT}} - 1\right) + \mathrm{I_{BCN}}\left(e^{\frac{qV_{bci}}{\mathrm{N_{CN}}kT}} - 1\right) \tag{4.3}$$

$$I_{tzr} = \mathrm{I_S}\left(e^{\frac{qV_{bci}}{\mathrm{N_R}kT}} - 1\right) \tag{4.4}$$

The parameters that have to be specified in the VBIC model are: the saturation currents $\mathrm{I_{BEI}}$, $\mathrm{I_{BEN}}$, $\mathrm{I_S}$, $\mathrm{I_{BCI}}$, $\mathrm{I_{BCN}}$ and the emission coefficient (ideality factors) $\mathrm{N_{EI}}$, $\mathrm{N_{EN}}$, $\mathrm{N_F}$, $\mathrm{N_R}$, $\mathrm{N_{CI}}$, $\mathrm{N_{CN}}$. These parameters can easily be calculated from the measured low current part of the forward and reverse Gummel plots. In these measurements the total base and collector currents and voltages are measured. The equations (4.1)-(4.4) describes the intrinsic values of the same currents and voltages. Approximate values for the saturation currents and the emission coefficients can be found by assuming that the measured currents and voltages are equal to the intrinsic values.

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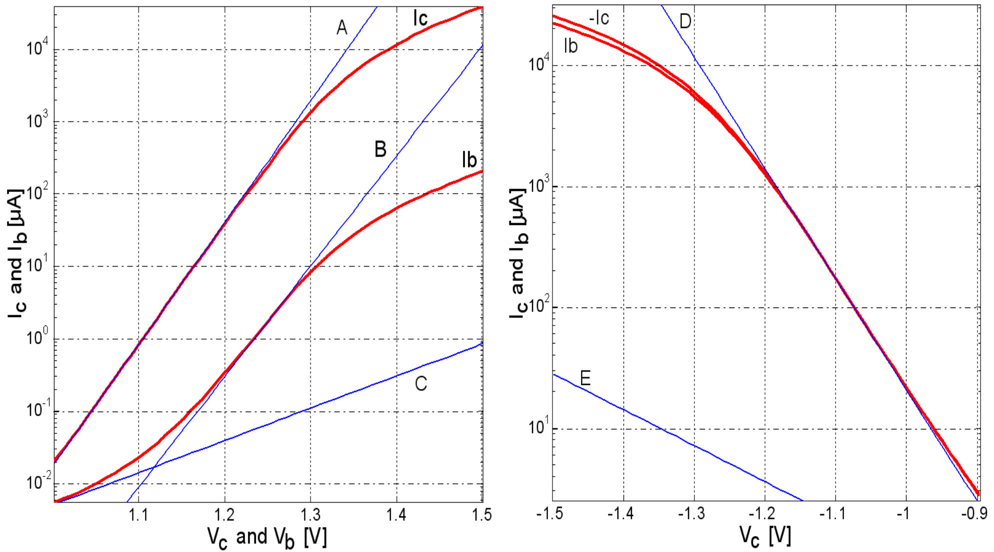

Figure 4.2. Forward Gummel plot and Reverse Gummel plot.

In Figure 4.2 a forward and a reverse Gummel plot is shown in red. Blue asymptotic lines are drawn in the figure. The asymptotic line A describes the lower part of the collector current. The asymptotic line B and C describes the lower part of the base current. From the asymptotic lines, the saturation currents and the emission coefficients can be found. The transport saturation current I_S is found where the asymptotic line A crosses the y-axes ($V_b = 0$) in the forward Gummel plot. The slope of line A is used to find the forward emission coefficient N_F. This is given by (4.5).

$$N_F = \frac{q}{\ln(10) \cdot kT \cdot \text{SlopeA}} \tag{4.5}$$

The same method as above is used with asymptotic lines B and C, to find the ideal and non-ideal saturation currents, I_{BEI}, I_{BEN}, and the corresponding emission coefficient, N_{EI}, N_{EN}, of the base-emitter.

Line D and line E in the reverse Gummel plot are used to find the parameters associated with base-collector region the same way as above. In the documentation on the VBIC model it is recommended that N_R is set equal to N_F. This is done to ensure convergence (the equations in the model may, with the wrong parameter values, generate more power than applied). In some cases, i.e. GaAs HBT technology, it is safe to apply different values to N_R and N_F.

The parameter values found by using the asymptotic lines are in most cases quite good, but if higher accuracy is needed the values can be used as a starting point for an optimization in Agilent ADS.

4.2.3 Extrinsic Components

In the VBIC model there are five extrinsic components (excluding the components associated with the parasitic transistor). There are three resistors, R_E, R_{CX}, R_{BX}, and two capacitors C_{BEO}, C_{BCO}.

Emitter resistance, R_E:

The importance of the emitter resistance, R_E, must not be underestimated, even if R_E appears to be a simple contact resistance (which is not always the case) and its value normally is only around a few ohms. There are several techniques that can be used to extract R_E for an HBT. One common method is the open-collector method [87], another method is to use the forward Gummel plot.

The open-collector method uses an open-collector measurement. This measurement is obtained by sweeping the base-emitter current I_b, and measure the open collector voltage, V_{ce}. The collector works as a voltage probe, that observes the base-emitter voltage variations without influence from the base resistance. Figure 4.3 illustrate what an open-collector measurement may look like. The emitter resistance R_E is then given by the slope of the asymptotic blue line in Figure 4.3.

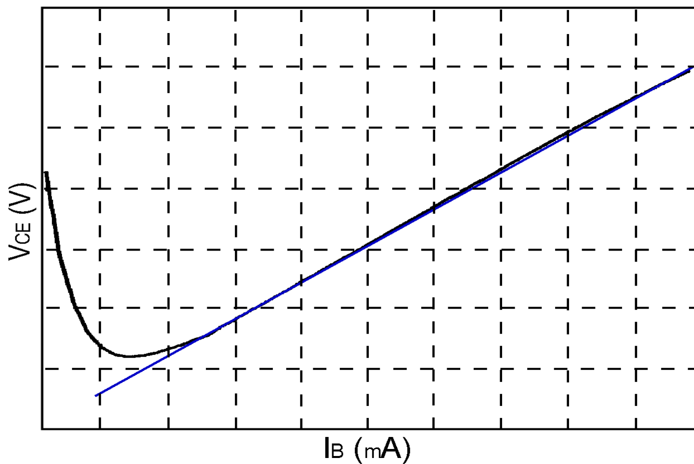

Figure 4.3. Open Collector Measurement.

Another method is to use the forward Gummel plot. In the high current region of the forward Gummel plot, Figure 4.2, the main reason for the deviation from the asymptotic lines is the emitter resistance. The emitter resistance is not the only parameter that affect this region, but it is the dominant one. An estimate of the emitter resistance can be found by calculating R_E using the deviation from the asymptotic line for the collector current. A much more accurate value is found by optimization of R_E to fit the forward Gummel data. This method may be the preferred one, because it does not require any additional measurements. The accuracy of the two methods are similar.

Collector Resistance R_{CX}:

The collector resistance R_{CX} is mainly a combination of bulk and contact resistances. Figure 4.4 shows a typical set of I-V curves from an HBT. The asymptotic line F indicates the maximum slope in the triode region of the I-V-curves. The collector resistance R_{CX} can be found directly from I-V measurements using the slope of line F. The slope of line F is given by (4.6).

$$\text{Slope F} = (R_{CX} + R_E)^{-1} \qquad (4.6)$$

The emitter resistance R_E was found in the high current region of the forward Gummel plots.

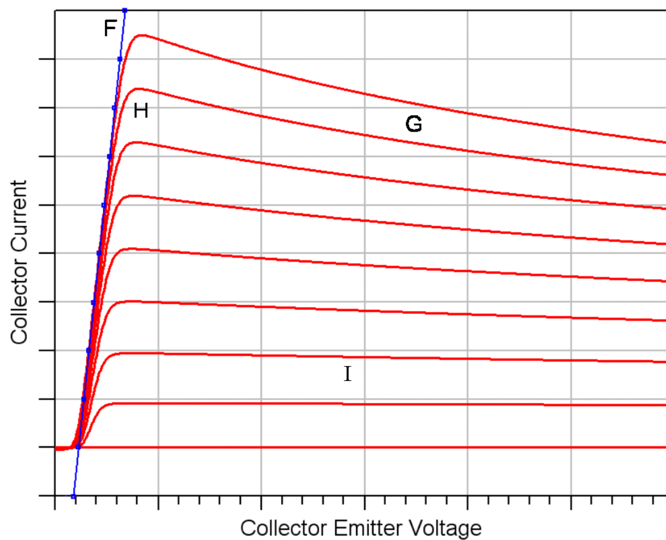

Figure 4.4. IV curves of a typical HBT.

Base Resistance R_B:

In the VBIC model the base resistance may have a distributed effect. The base resistance is then divided in two parts, the extrinsic contact resistance R_{BX} and the intrinsic nonlinear resistance R_{BI}/q_b, where q_b is the normalized transport charge at the base. The intrinsic nonlinear resistance depend on the base current. There is no clear method to separate R_{BX} and R_{BI} by DC measurements only. An active s-parameter optimization is require. This will be discussed in Section 4.2.7. For an InGaP/GaAs HBT the distributed effect in the base is usually very small, and can usually be omitted. In any case, the total base resistance will be found in the following. If the distributed effect is omitted, the total resistance equals the extrinsic resistance R_{BX}.

The extrinsic resistance R_{BX} can be found from the high current region of the reverse Gummel plot, Figure 4.2. Many parameters have influence on the behaviour in this region, but the most dominant parameters here are the resistances in the base-

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collector junction, R_{BX} and R_{CX}. The collector resistance, R_{CX}, is already found. The best way to find the value of R_{BX} is to do an optimization of R_{BX} so the model match the measurements. A start value of the total resistance in the base-collector junction can be found by calculating R_{BX} + R_{CX} using the deviation from the asymptotic line for the collector current.

Base-emitter capacitor C_{BEO} *and base-collector capacitor* C_{BCO}:
The bias independent base-emitter capacitor, C_{BEO}, and base-collector capacitor, C_{BCO}, are best found by optimization. A passive s-parameter measurement is needed to find these parameters. This measurement is also used to find the zero bias junction capacitance described in Section 4.2.4.

4.2.4 Junction Capacitances Parameters

The VBIC model has two different equations implemented, that describes the depletion capacitances in each junction. One is compatible with the Gummel-Poon model. Unfortunately, it is not continuous in all the derivatives. The other is continuous (smooth) single piece function, that is continuous in all the derivatives. This second function is preferred, because it does not create any problems in a circuit simulator. The base-emitter junction capacitance is described by the following parameters: the zero bias junction capacitance C_{JE}, the built-in potential P_E, the grading coefficient M_E, the capacitance smoothing factor A_{JE} and the capacitance threshold FC. The base-collector junction capacitance is described by the parameters C_{JC}, P_C, M_C, A_{JC} and FC. Note that the parameter FC are the same for both junctions.
Equation (4.7)-(4.9) describes the normalized depletion charge in the junction. (4.10) gives the normalized depletion capacitance. An example of this function is given in Figure 4.5.

$$q_j = \frac{-\mathrm{P}\left(1-\frac{V_1}{\mathrm{P}}\right)^{1-\mathrm{M}}}{1-\mathrm{M}} + (1-\mathrm{FC})^{-\mathrm{M}}(V - V_1 + V_{10}) - \frac{-\mathrm{P}\left(1-\frac{V_{10}}{\mathrm{P}}\right)^{1-\mathrm{M}}}{1-\mathrm{M}} \tag{4.7}$$

$$V_1 = 0.5 \cdot \left((V - \mathrm{P}\cdot\mathrm{FC}) - \sqrt{(V - \mathrm{P}\cdot\mathrm{FC})^2 + A}\right) + \mathrm{P}\cdot\mathrm{FC} \tag{4.8}$$

$$V_{10} = 0.5 \cdot \left((-\mathrm{P}\cdot\mathrm{FC}) - \sqrt{(-\mathrm{P}\cdot\mathrm{FC})^2 + A}\right) + \mathrm{P}\cdot\mathrm{FC} \tag{4.9}$$

$$\bar{C_j} = \frac{\partial}{\partial V} q_j(V, \mathrm{P,M,FC,A}) \tag{4.10}$$

The parameters in the equations above are substituted with their corresponding parameters for the junction in question.
The best way of finding the parameters for the junctions are to use Cold-Capacitor measurements. In a Cold-Capacitor measurement, the collector and emitter voltage are both set to zero. The base voltage V_b, is stepped from a negative value (i.e. -2.5V)

to a positive value (i.e. 1.1V). For each step in base voltage a complete set of s-parameters are measured.

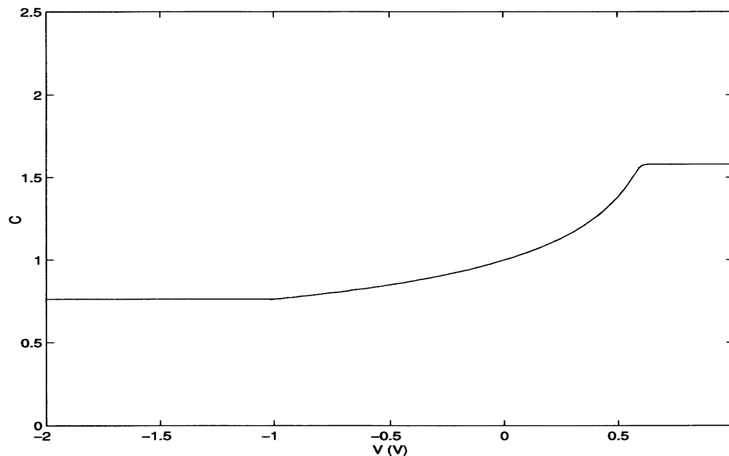

Figure 4.5. Example of the normalized junction capacitance.

The technique for finding the parameters is (the whole frequency range measured should be used):

- At zero bias (V_b = 0) the bias independent parameters C_{JE} and C_{JC} are found (together with C_{BEO} and C_{BCO} from Section 4.2.3) by optimization of the model to the s-parameter measurement.
- The bias dependent parameters can be found by finding the equivalent total junction capacitances for different base voltages. This is done in Agilent ADS by setting the built-in potentials P_E and P_C very large, and the grading coefficient M_E and M_C very small. This makes the junction capacitances constant. C_{JE} and C_{JC} are then optimized to match the measured s-parameter set. This is done for each bias point, giving a set of C_{JE} and C_{JC} versus V_b. (4.7) to (4.10) are then used in a mathematical tools, like MathWorks MATLAB, to estimate the best fit of the parameters P_E, P_C, M_E, M_C, A_{JE}, A_{JC} and FC to the set of capacitances.

If higher accuracy is needed, or the calculation in the second point above is not done, the parameters for the junction capacitances can be found by an iterative optimization process:

- At negative bias (i.e. V_b = -2.5V), optimize the base-emitter/base-collector junction exponents M_E and M_C.
- At moderate positive bias (i.e. V_b = 0.5V), optimize the base-emitter/base-collector grading coefficient P_E and P_C.

- At positive bias (i.e. V_b = 0.9V or higher), optimize the forward bias junction capacitance threshold FC.

If necessary, repeat these three steps for the best results. If possible, all parameters can be fine-tuned by a global simulation, using all base voltages in the same simulation.

4.2.5 Temperature Parameters

The VBIC model has several temperature parameters.

Self-Heating:
The self heating parameters R_{TH} and C_{TH} are found in Chapter 3.

Saturation currents and emission coefficients:
The three most important parameters are: the temperature exponent X_{IS} of the forward saturation currents I_S, the temperature exponent X_{II} of the saturation currents I_{BEI}, I_{BCI}, I_{BEIP}, I_{BCIP} and the temperature coefficient T_{NF} of N_F. These parameters are found by optimization of the area G of the I-V curves in Figure 4.4, measured at two or more temperatures. Increased accuracy can be obtained by including measurements of the V_{be} versus V_{ce} curves. If no temperature measurements are available, the best results are obtained by optimizing X_{II} and leave X_{IS} and T_{NF} at their default value.

The temperature exponent X_{IN} of the non-ideal saturation currents I_{BEN}, I_{BCN}, I_{BENP} and I_{BCNP} is set to simulator default values. The effect of this parameter is very small.

If some of these parameters are used, the earlier extracted DC parameters may need some adjustments.

Resistances:
The temperature exponents for the base, collector and emitter resistances X_{RB}, X_{RC} and X_{RE} can be found by calculating the resistances described in Section 4.2.3 at different temperatures. The effect of these parameters in a normal operating range around ambient temperature is small. If no temperature measurements are available these parameters can be set to zero.

Other parameters:
If temperature measurements are available, the temperature coefficient T_{AVC} of the base-collector weak avalanche parameters A_{VC1} and A_{VC2}, and the temperature exponent X_{VO} of the epi drift saturation voltage V_O, can be found. At normal temperature ranges the effect of these parameters are very small, and they can therefore both be set to simulator default values.

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4.2.6 Transit Time Parameters

The forward transit time T_f is given by the parameter T_F. The bias dependence of T_f is described by additional four parameters: the coefficient for the intrinsic base-collector voltage dependence V_{TF}, the coefficient for the ideal forward transport current I_{TF}, the coefficient of voltage and current dependence X_{TF} and the coefficient for the base width modulation Q_{TF}. (4.11) shows the bias dependence of T_f.

$$T_f = T_F \cdot (1 + Q_{TF} \cdot Q_1) \cdot \left(1 + X_{TF}\left(\frac{I_{txf}}{I_{txf} + I_{TF}}\right)^2 \cdot e^{\frac{V_{BCi}}{1.44 \cdot V_{TF}}}\right) \tag{4.11}$$

Where, I_{txf} is the ideal forward transport current, V_{BCi} is the intrinsic base-collector voltage, and Q_1 is the change of base charge due to base width modulation.

Extraction of the parameters for the forward transit time are best done with s-parameter measurements for at least five different active I-V bias points. The bias points should be chosen to cover the part of the I-V-diagram for which the model is to be used. This may be the four corners and the centre in the chosen area of the I-V-diagram.

The first step is to find good starting values for the forward transit time, by using (4.11) to calculate the parameters. It is quite difficult to calculate the base width modulation parameter Q_1 by hand, so as an approximation Q_1 is omitted. If forward and reverse Early voltages (V_{EF} and V_{ER}) are large (which is usually the case in GaAs HBT), this is a very good approximation. A second approximation is to set the intrinsic base-collector voltage and the ideal forward transport current equal to the measured base-collector voltage and collector current. The technique now is to find a set of equivalent values for T_f from the s-parameter measurements at different bias points. In Agilent ADS this is done by setting $X_{TF} = Q_{TF} = 0$, i.e. no bias dependence of T_f. Then simulate to find the equivalent optimized value of T_f for each bias point. (4.11) is then used in MathWorks MATLAB or similar software to calculate the values of T_F, V_{TF}, I_{TF} and X_{TF} that best fits the equivalent optimized values of T_f.

The second step is to use the calculated values of T_F, V_{TF}, I_{TF} and X_{TF} in Agilent ADS and compare the simulation to the measured data. If the results are acceptable, no further simulations are needed. If this is not the case, or the base width modulation can not be omitted, an optimization of the parameters are needed. This requires a global optimization with multiple biases and automatic selection of different measured s-parameter files for each bias, all at the same time. By setting up this optimization in Agilent ADS, it is possible to optimize all five parameters simultaneously.

The method described above was published [7] by the author in 2001, and can be found in Appendix A.3.

The effect of the reverse transit time T_r, for a device used in the normal operating range, is usually neglected. Therefore, T_R can be set to zero.

4.2.7 Other Parameters

Parasitic substrate transistor:

The VBIC model also includes a parasitic substrate transistor. All transistors considered here have the collector down structure with the collector connected to two collector contacts, one on each side of the transistor. This effectively removes the need for modelling the parasitic substrate transistor.

In GaAs technology low substrate losses and high isolation also removes the need for the parasitic substrate transistor. This parasitic substrate transistor will not be discussed any further. The parasitic substrate transistor parameters R_S, R_{BP}, I_{SP}, I_{BEIP}, I_{BENP}, I_{BCIP}, I_{BCNP}, I_{KP}, X_{RS}, C_{JEP}, C_{JCP}, W_{SP}, N_{FP}, N_{CIP}, N_{CNP}, P_S, M_S and A_{JS} are set to the default values in ADS. This effectively removes the parasitic transistor from the simulations.

Early voltage:

The forward and reverse Early voltage are usually very high in a GaAs HBT. This is due to the heavy doping in the base region which makes the base width modelling, due to the bias, very small. Usually, the modelling parameters V_{EF} and V_{ER} can be set to infinite for a GaAs HBT.

In a SiGe HBT the forward and reverse Early voltage usually are higher than that of a silicon BJT, but not high enough to be ignored. V_{EF} can be found by optimizing the active region of the I-V curves. If the device suffer from self-heating, the self-heating effect may mask the Early effect. Therefore, the lower part (area I in Figure 4.4) of the I-V curves should be used for optimization, even if the Early effect here is smaller. Usually, V_{ER} can be set equal to V_{EF}.

Knee currents:

In an HBT the forward and reverse knee current are usually very high and can often be set to infinity. However, if the knee currents are needed, the forward knee current I_{KF} can be optimized in the active region of the I-V curves to ensure the best fit. The reverse knee current I_{KR} can be found either from a reverse active I-V measurement or from the high current region of the reverse Gummel measurement. Reverse active I-V measurements are usually not performed. If these parameters are used, the earlier extracted DC parameters may need to be adjusted.

Quasi saturation in collector epi layer:

The VBIC model include quasi saturation [53] (modified Kull model) in collector epi layer. In a GaAs HBT, the quasi saturation is usually negligible, but in a SiGe it may be necessary to include. The quasi saturation occurs in the region H in Figure 4.4. It is described by four parameters: the intrinsic collector resistance R_{CI}, the epi drift saturation voltage V_O, the epi doping parameter G_{AMM} and the high current RC factor H_{RCF}. These parameters can be found by optimizing the I-V curves in region H in Figure 4.4. If these parameters are used, the earlier extracted DC parameters may need some adjustments.

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Distributed base:

The distribution effect in the base are composed of the base resistance and the base current.

The intrinsic nonlinear resistance R_{BI}/q_b may be difficult to separate from the extrinsic resistance R_{BX}. If the distributed base effects are present, the parameter R_{BI} can be found by optimizing the active s-parameters at different base currents (fixed collector-emitter voltage). If this parameter is used, the earlier extracted DC parameters may need some adjustments.

The parameter W_{BE} directs a portion of the intrinsic base current I_{be} to the extrinsic base current I_{bex}. The extrinsic base current flows outside of the base-emitter on the side walls of the transistor. This effect is very small and is therefore neglected.

Weak avalanche:

The weak avalanche multiplication effect in the base-collector region, occurs at high collector-emitter voltages. This effect generates the avalanche current I_{gc} in Figure 4.1.

$$I_{gc} \sim A_{VC1} \cdot (P_C - V_{bci}) \cdot e^{\left(-A_{VC2} \cdot (P_C - V_{bci})^{(M_C - 1)}\right)} \tag{4.12}$$

V_{bci} is the intrinsic base-collector voltage, P_C and M_C are explained in Section 4.2.4. The weak avalanche parameters A_{VC1} and A_{VC2} may be found using the high collector-emitter voltage region of the I-V curve. These parameters can only be found after P_C and M_C are found from the cold capacitor measurements. If these parameters are used, the earlier extracted DC parameters may need some adjustments.

Noise:

Noise parameters are not considered, due to the lack of measurement data.

Excess phase:

The excess phase is modelled as a sub circuit in the VBIC model (Figure 4.1). The physical reason for the excess phase is not well documented in the literature. The excess phase parameter T_D can be found (if needed) by an optimization of an active s-parameter measurement.

Activation energy:

The activation energy parameters in the VBIC model are E_A, E_{AIE}, E_{AIC}, E_{AIS}, E_{ANE}, E_{ANC} and E_{ANS}. These parameters are given directly from the physical properties. The activation energy are for: GaAs 1.42eV, InGaP 1.87eV, Si 1.12eV, Ge 0.664eV and $Si_{90}Ge_{10}$ about 1.05eV. Values are taken from [10, 21, 33, 34, 88]. The practical values of the activation energy can be optimized for even higher accuracy. This has not been necessary here.

4.3 Practical Extraction Method

Today, devices and models have become more and more complex. This makes several phenomena influence the same characteristics. This makes pure analytical parameter extraction methods inadequate.

The common circuit designer needs models that can predict the behaviour of the circuits accurately for "first time" design success. Many circuit designers want to measure and model the devices they use themselves to ensure design success. The need for a practical parameter extraction method that uses just a few common measurements is desired.

Parts of the practical parameter extraction developed below was published [6, 7] by the author in 2000 and 2001, and can be found in Appendix A.2 and Appendix A.3.

4.3.1 Measurements Types

In the algorithm in Section 4.3.2, there are only five different measurements needed for extracting good parameter values. The measurements needed are three DC-measurements and two s-parameter measurements. The measurements are:

- Forward Gummel measurement: This is performed by measuring the collector and base currents while sweeping the base/collector voltage. The base and collector are connected together, while the emitter is grounded.
- Reverse Gummel measurement: This is performed by measuring the collector and base currents while sweeping the collector voltage. The base and emitter are both grounded.
- I-V measurement: This is performed by measuring the collector current and the base voltage while sweeping the base current I_b and collector voltage. For each step in base current, the collector-emitter voltage is swept. The sweeps should cover the hole area of interest.
- Cold Capacitor s-parameter measurement: This is performed by measuring s-parameters, while the base voltage is stepped from negative to slightly positive values. The collector and emitter are grounded. The frequency range should be as wide as possible. The measurement must include a passive measurement.
- Active s-parameter measurement: This is performed by measuring s-parameters, at selected bias points that cover the part of the active region (IV-curves) of interest. The frequency range should be as wide as possible.

If the device is going to operate in a wide temperature range, the DC-measurement should be done at different temperatures, so the temperature parameter can be extracted.

Temperature measurement were not available during this work, so the parameters will not be extracted.

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4.3.2 The Algorithm

The algorithm was developed by testing out many different sequences of parameter extractions. The goal was to find a sequence that required only a few iterations in order to find a good set of parameters. The algorithm is graphically shown in Figure 4.6, with all the steps described below.

1. From Chapter 3, the self-heating parameters R_{TH} and C_{TH} are calculated.
2. From Section 4.2.2, I_{BEI}, N_{EI}, I_{BEN}, N_{EN}, I_S and N_F are extracted from the low current region of the forward Gummel measurement.
3. From Section 4.2.2, I_{BCI}, N_{CI}, I_{BCN}, N_{CN} and N_R are extracted from the low current region of the reverse Gummel measurement.
4. From Section 4.2.3, the emitter resistance R_E is extracted from the high current region of the forward Gummel plot, or from an open collector measurement.
5. From Section 4.2.3, the collector resistance R_{CX} is extracted from line F in the IV-measurement.
6. From Section 4.2.3, the base resistance R_{BX} (and from Section 4.2.7 I_{KR} if necessary), is extracted from the high current region of the reverse Gummel plot.
7. From Section 4.2.5, the temperature dependent parameter X_{II} is found from part G of the IV-measurement. If IV-measurements at different temperatures are available, X_{IS} and T_{NF} (and if necessary X_{RB}, X_{RC}, X_{RE}, T_{AVC}, X_{VO}) are extracted.
8. If necessary: From Section 4.2.7, the Early parameters V_{EF} and V_{ER}, the forward I_{KF}, and the quasi saturation R_{CI}, V_O, G_{AMM} and H_{RCF} can be found from the respective areas of the IV-measurement.
9. From Section 4.2.3 and Section 4.2.4, the bias independent junction capacitances C_{JE} and C_{JC}, and the extrinsic capacitances C_{BEO} and C_{BCO} are extracted from the passive (V_b=0) cold-capacitor measurements. If other parameters like extrinsic inductances (L_B, L_C, L_E) are included, they all are found from this measurement.
10. From Section 4.2.4, the bias dependent junction capacitance parameters M_E, M_C, P_E, P_C, A_{JE}, A_{JC} and FC are extracted from of the cold-capacitor measurements.
11. From Section 4.2.6, transit time parameters T_F, I_{TF}, V_{TF}, X_{TF}, Q_{TF} and T_R are extracted from the active s-parameter measurements. If needed, the excess phase T_D in Section 4.2.7 is found from the same measurements.
12. If necessary: From Section 4.2.7, the intrinsic base resistance R_{BI} of the distributed base, can be found from active s-parameter measurements. The weak avalanche parameters A_{VC1} and A_{VC2} can be found from the IV-measurement.

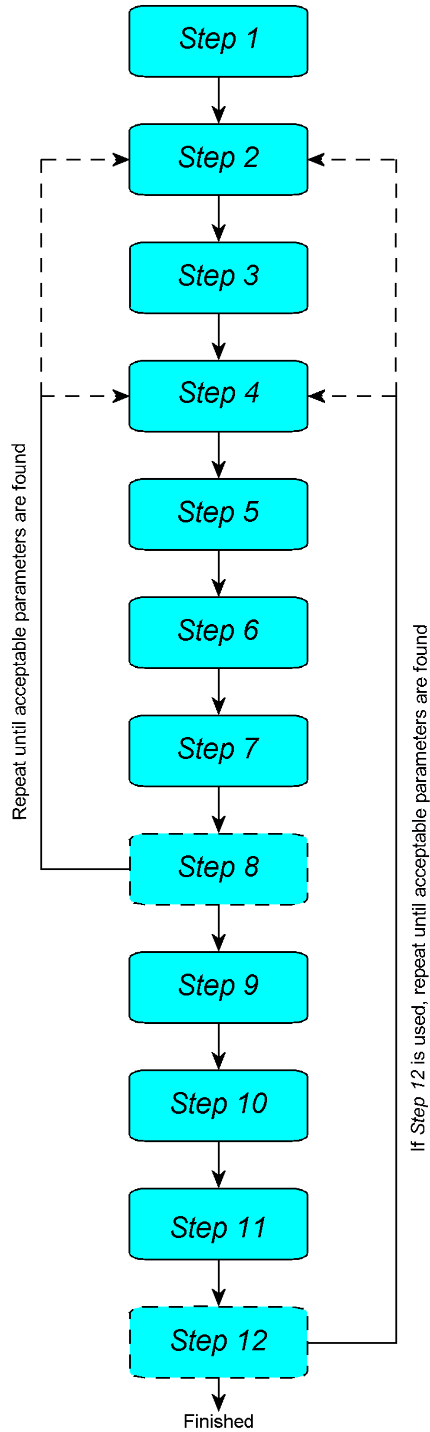

Figure 4.6. The parameter extraction algorithm.

After *Step 8*, it is necessary to repeat the steps covering the DC parameters by going back to *Step 2*. It usually requires only be a few iterations. If only small changes were made in the last iteration, it is only necessary to go to *Step 4*.

If *Step 12* is used, it is necessary to repeat the whole procedure from *Step 2* or *Step 4* depending on the results from the last iteration.

Each step in the algorithm is based on results from the previous steps.

4.3.3 Limitations

There are some limitations in using this algorithm. The algorithm does not address the extraction of noise parameters. This is due to the fact that noise measurements were not available for this work. The algorithm does not include the extraction of the parasitic substrate transistor, as explained in Section 4.2.7.

The algorithm does not necessarily result in the theoretically best model parameters, but it will result in very good model parameters. It depends on how many iteration one is willing to perform.

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4.4 Results for the InGaP/GaAs HBT

4.4.1 Devices and Measurements from Caswell Technology

Caswell Technology provided measurements for several of their devices. The available measurements are listed in Table 4.24. Figure 4.7 shows the layout of the test structures for several of the HBT's.

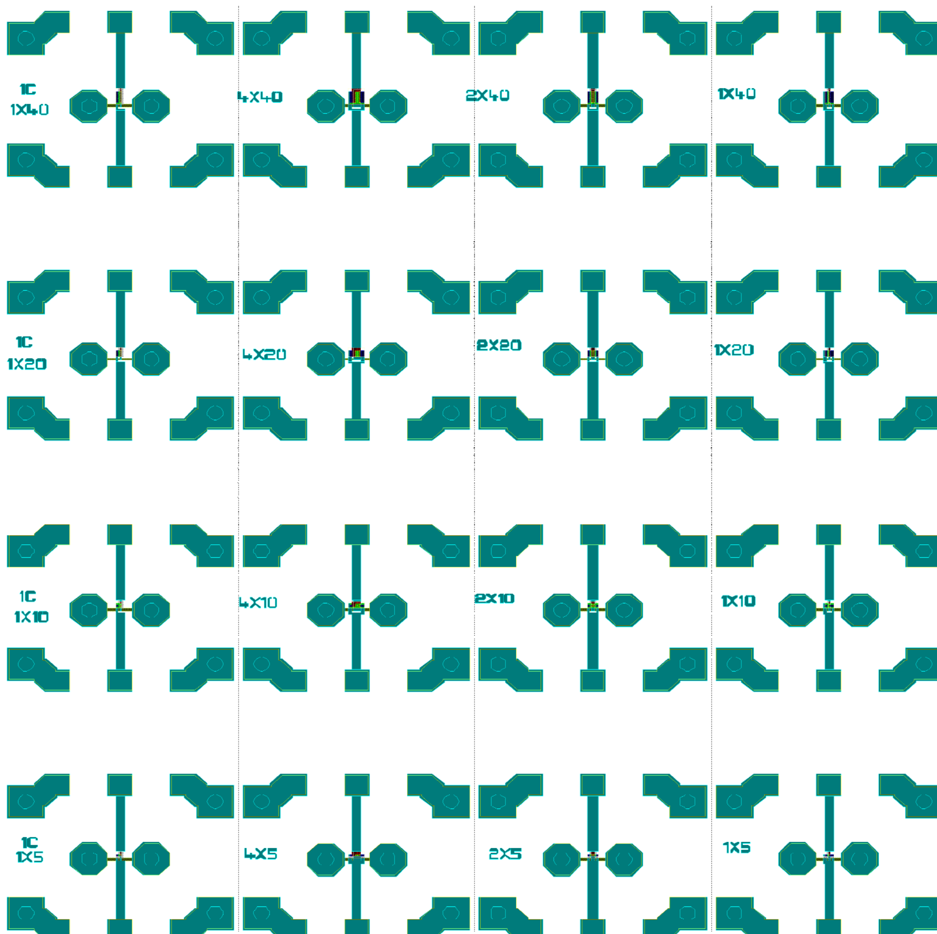

Figure 4.7. Test structure layout of some of the InGaP/GaAs transistors.

Each emitter finger of the HBT has a width of 2 μm. The length of the emitter finger vary from 5 μm to 40 μm. The first column of transistors in Figure 4.7 has only one collector contact. Caswell Technology provided measurements for this structure, but said that it would not be used. The transistors in the second column has 4 emitter fingers. Only the '4x40' device has some limited measurements available. The third column shows the two finger devices. The last column show the standard single finger devices.

Table 4.24. Available measurements from Caswell Technology.

Device Name	Number of fingers	Finger Length (μm)	No. measured devices	Measurement types
1X5	1	5	37 / 40 3 3	Forward / Reverse Gummel s-parameters at various bias f_t extraction s-parameters
1x10	1	10	38 / 39 3 3	Forward / Reverse Gummel s-parameters at various bias f_t extraction s-parameters
1x20	1	20	39 / 40 3 4	Forward / Reverse Gummel s-parameters at various bias f_t extraction s-parameters
1x40	1	40	29 / 37 28 3 4	Forward / Reverse Gummel Cold-Capacitor s-parameters s-parameters at various bias f_t extraction s-parameters
2X5	2	5	38 / 40 4 4	Forward / Reverse Gummel s-parameters at various bias f_t extraction s-parameters
2X10	2	10	39 / 40 4 4	Forward / Reverse Gummel s-parameters at various bias f_t extraction s-parameters
2X20	2	20	39 / 39 4 4	Forward / Reverse Gummel s-parameters at various bias f_t extraction s-parameters
2X40	2	40	28 / 37 29 3 3	Forward / Reverse Gummel Cold-Capacitor s-parameters s-parameters at various bias f_t extraction s-parameters
4x40	4	40	3	IV measurements
4x40C	4	40	3	IV measurements
P4x40	4	40	3	IV measurements
P4x40C	4	40	3	IV measurements

Table 4.24 shows the measurements of good devices provided by Caswell Technology.

Some of the measurements of the devices were unusable. The number of measurements of each type that was measured correctly, vary due to the number of damaged devices. These measurements were removed from the list of available measurements in Table 4.24. The last three devices in Table 4.24 are not displayed in Figure 4.7.

There are no IV-measurement for the single and two finger devices. IV-curves were constructed from the bias points of the active s-parameter. This made it very difficult to find the collector resistance, quasi saturation and avalanche effect from the IV-curves. The collector resistance R_{CX} had to be found indirectly, first by finding the total base/collector resistance from the reverse Gummel measurement, and then optimizing R_{BX} from the passive cold capacitor measurement. The measured IV-curves for the four finger devices show no sign of quasi saturation or avalanche effect within the measured region. Therefore, these effects are disregarded in the modelling of these devices.

A MATLAB program was developed for administration and processing of all the measurements. Figure 4.8 shows the program menu for the MATLAB program 'EEsofplot'.

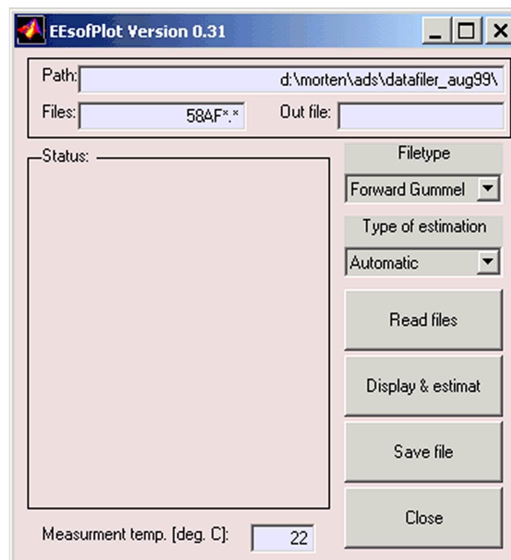

Figure 4.8. MATLAB program.

In this program, the measurements and file types are specified. The program will then display all the files graphically and make parameter estimations for some of the parameters in the VBIC model. This estimations will be start values for optimizations in ADS. 'EEsofplot' also makes a statistical mean of all the measured devices of the same transistor type. The statistical mean is saved in a format that is readable for ADS.

The single finger 1x40 µm device was selected to test the parameter extraction algorithm. The results of this is shown in Section 4.4.3. A model of the two finger 2x40 µm device have also been made with the same kind of results as for the single finger 1x40 µm device in Section 4.4.3. Models for single and two finger devices of shorter lengths have been made by using the transistor scaling parameter in the VBIC implementation on ADS. This has been done with satisfactory results.

4.4.2 Calibration and de-embedding

Caswell Technology including the probe test pads in the calibration for all the measurements on the chip. The reference plane were calibrated to the edge of the pads. In order to model the device, the reference plane should be at the base/collector/emitter contacts of the active device. The measured devices must be de-embedded. Unfortunately, a de-embedding structure was not available from Caswell Technology. But, a very good (according to Caswell Technology) passive model library were available for HP LIBRA. Figure 4.9 shows an example of the test structure for a single finger device. The layout of the test structure were analysed, and the feed structure to the base (shown in the area inside the dot-dashed line) and the feed structure of the collector including the grounding of the emitter (shown in the area inside the dashed line), were simulated. The resulting s-parameter files from the surrounding components were added to the VBIC model in Agilent ADS. The VBIC model was in fact embedded instead of de-embedding all the measurements.

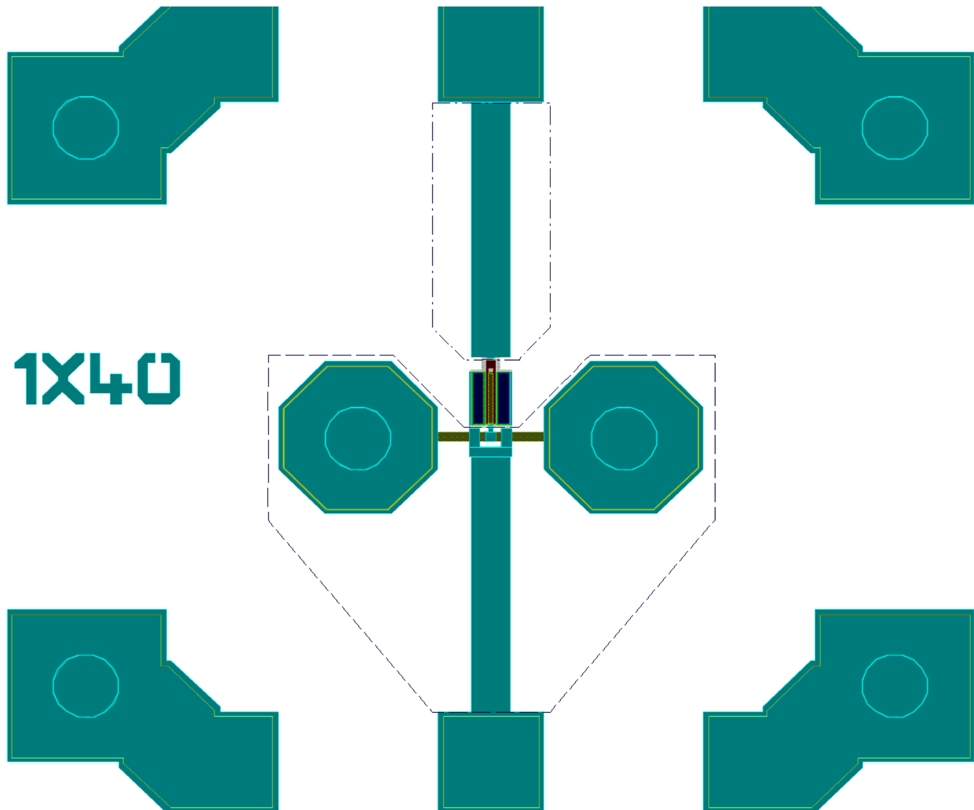

Figure 4.9. Test structure for single finger 1x40 transistor.

4.4.3 Results for a single finger 1x40μm device

Table 4.25 shows the parameters in the VBIC model as they were being extracted. Column four shows the starting values estimated from “EEsofplot”. Values marked with “*” were just an initial “guess”. The initial guess for N_R was set equal to N_F. In *Step 6* the total base-collector resistance R_{BC_TOT} was found. The base resistance was found together in *Step 9*. The collector resistance R_{CX} was then calculated. *Step 5* was omitted.

Table 4.25. VBIC parameters and their extracted values.

Step	Parameter	x	Initial	1. iteration	2. iteration	3. iteration	4. iteration
1	R_{TH}	1	**650**				
	C_{TH}	10^{-9}	**1.4**				
2	I_{BEI}	10^{-25}	1.59	5.97	6.30	**6.10**	
	N_{EI}	1	1.125	1.156	1.158	**1.157**	
	I_{BEN}	10^{-15}	174	6.54	7.56	**6.99**	
	N_{EN}	1	3.840	4.391	4.463	**4.424**	
	I_S	10^{-25}	2.69	3.56	3.54	**3.55**	
	N_F	1	1.022	1.027	1.028	**1.028**	
3	I_{BCI}	10^{-15}	13.7	5.31	5.34	**5.35**	
	N_{CI}	1	1.861	1.787	1.787	**1.787**	
	I_{BCN}	10^{-12}	968	2.98	2.97	**2.97**	
	N_{CN}	1	5.738	4.404	4.404	**4.404**	
	N_R	1	1.019*	1.038	1.038	**1.038**	
4	R_E	1	3.14	4.53	4.56	4.50	**4.51**
6	R_{BC_Tot}	1	7.51	6.71	6.78	6.78	**6.77**
7	X_{II}	1	3*	4.20	4.20	4.18	**4.18**
8	I_{KF}	1	0*	0.441	0.387	0.442	**0.443**
9	C_{JE}	10^{-14}	1*		8.50	7.94	**7.94**
	C_{JC}	10^{-14}	1*		7.01	8.19	**8.22**
	C_{BEO}	10^{-15}	1*		8.77	13.3	**13.2**
	C_{BCO}	10^{-14}	0.1*		2.26	1.30	**1.26**
	R_{BX}	1	2*		4.77	4.84	**4.84**
	L_B	10^{-12}	1*		22.7	24.1	**24.2**
	L_C	10^{-12}	1*		0.054	0	**0**
	L_E	10^{-12}	1*		0.082	0	**0**

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Table 4.25. VBIC parameters and their extracted values.

Step	Parameter	x	Initial	1. iteration	2. iteration	3. iteration	4. iteration
10	P_E	1	0.946		1.23	1.11	**1.12**
	M_E	1	0.107		0.127	0.108	**0.110**
	A_{JE}	1	0.138		0.078	0.150	**0.147**
	P_C	1	1.11		1.12	1.11	**1.11**
	M_C	1	0.563		0.548	0.485	**0.483**
	A_{JC}	1	0.01		0.001	0.001	**0.001**
	FC	1	0.975		0.997	0.997	**0.997**
11	T_F	10^{-12}	10.6		11.8	11.1	**11.1**
	I_{TF}	10^{-3}	0.424		1.13	1.46	**1.47**
	V_{TF}	1	5.73		8.36	6.82	**7.11**
	X_{TF}	1	-0.751		-0.681	-0.701	**-0.699**
	Q_{TF}	1	0		0	0	**0**
	T_D	10^{-12}	0		2.57	2.74	**2.72**

Each step and iteration in Table 4.25 are based on the results obtained in earlier steps. After performing *Step 2-8*, these steps were repeated in a second iteration. After the second iteration, parameter values from the two iterations were compared and since the difference were small, the extraction continued on to *Step 9*.

The starting values of *Step 10* were found as described in Section 4.2.4. Table 4.26 shows the optimal (correct) values for the junction capacitances C_{JE} and C_{JC}, which were used to find the starting values. Optimized values were then found.

The starting values of *Step 11* were found as described in Section 4.2.6. Table 4.27 shows the optimal (correct) values for the transit time, which were used to find the starting values. Optimized values were then found.

In *Step 9* the R_{BX} was found. This parameter also changes the DC response of the device, therefore iteration 3 were started from *Step 2*. After iteration 3 were completed, the results from iteration 2 and iteration 3 were compared. The changes in values for *Step 2* and *Step 3* were very small, therefore there were no need for further iterations of these steps. There were some changes especially in *Step 8* to *Step 11*. A fourth iteration were preformed from *Step 4*.

There were only very small changes in the parameter values after iteration 4. No further iterations were needed.

Table 4.26. Optimal and calculated values for the junction capacitances.

Base Voltage [V]	-2.5	-1.5	-1.0	-0.5	0.0	0.5	0.7	0.9	1.1
Optimal (Sim) C_{JE} [10^{-14} F]	7.43	7.69	7.86	8.10	8.50	9.40	10.0	10.9	11.5
Calculated C_{JE} [10^{-14} F]	7.40	7.68	7.88	8.15	8.50	9.36	10.0	11.0	11.5
Optimal (Sim) C_{JC} [10^{-14} F]	3.59	4.38	4.99	5.87	7.01	10.1	12.4	17.6	78.7
Calculated C_{JC} [10^{-14} F]	3.63	4.35	4.90	5.70	7.01	9.81	12.3	17.9	78.3

In Table 4.26, the calculated junction capacitances C_{JE} and C_{JC}, were calculated from the estimated values of P_E, M_E, A_{JE}, P_C, M_C, A_{JC} and FC using (4.10). By comparing the optimal values to the calculated, the validity of the junction capacitance equations were evaluated. The difference of the optimal values and the calculate values were neglectable. This indicate that the equations describing the junction capacitances are very good.

Table 4.27. Optimal and calculated values for the forward transit time.

Collector Voltage	2 V				3 V				5 V			
I_C [mA]	2	4	10	20	2	4	10	20	2	4	10	20
Optimal (Sim) T_f [ps]	5.03	4.65	3.78	3.38	6.02	5.60	4.96	4.17	7.52	6.96	5.77	4.90
Calculated T_f [ps]	5.61	4.59	3.80	3.47	6.18	5.28	4.58	4.30	7.14	6.43	5.89	5.67
Abs. relative error [%]	11.3	1.29	0.53	2.66	2.49	5.89	7.66	2.88	5.32	7.76	1.91	15.5
Constant (Sim) T_f [ps]	5.12											
Abs. relative error [%]	1.79	10.1	35.5	51.5	14.9	8.57	3.23	22.8	31.9	26.4	11.3	4.49

In Table 4.27 the forward transit time T_f was calculated from the estimated values of T_F, I_{TF}, V_{TF}, X_{TF} and Q_{TF} using (4.11). By comparing the optimal values to the calculated, the validity of the forward transit time equation were evaluated. There were some differences between the optimal and calculated values. A small part of the difference may originate from the assumption that the measured voltages and currents are equal to the intrinsic voltages and currents that are used in (4.11). The rest of the difference may indicate that the equation describing the bias-dependence of T_f does not correctly describe the complete bias dependence of T_f.

Even though the equation for T_f does not describe the optimal values with high accuracy, it predicts much better values than the use of a constant T_f. This was evaluated and discussed in [7]. In Table 4.27, the absolute relative error from the optimal values are listed both for the bias dependent T_f and for the constant T_f. The average of the absolute relative errors is 5.44 %, with the use of the bias dependent T_f, compared to 18.5 % without bias dependence of T_f.

The VBIC model with the parameters extracted in Table 4.25 were simulated and compared to the measurements.

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Figure 4.10 and Figure 4.11 show the forward and reverse Gummel plots. The green/blue curves are the results from the measured devices. The red lines are the simulated results. The simulated results are well within the measured results.

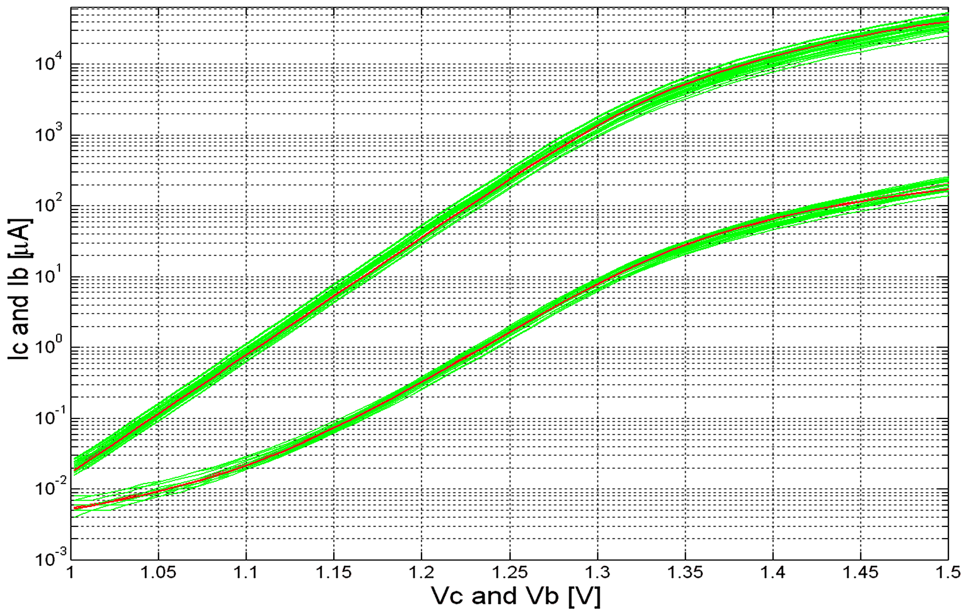

Figure 4.10. Forward Gummel plot.

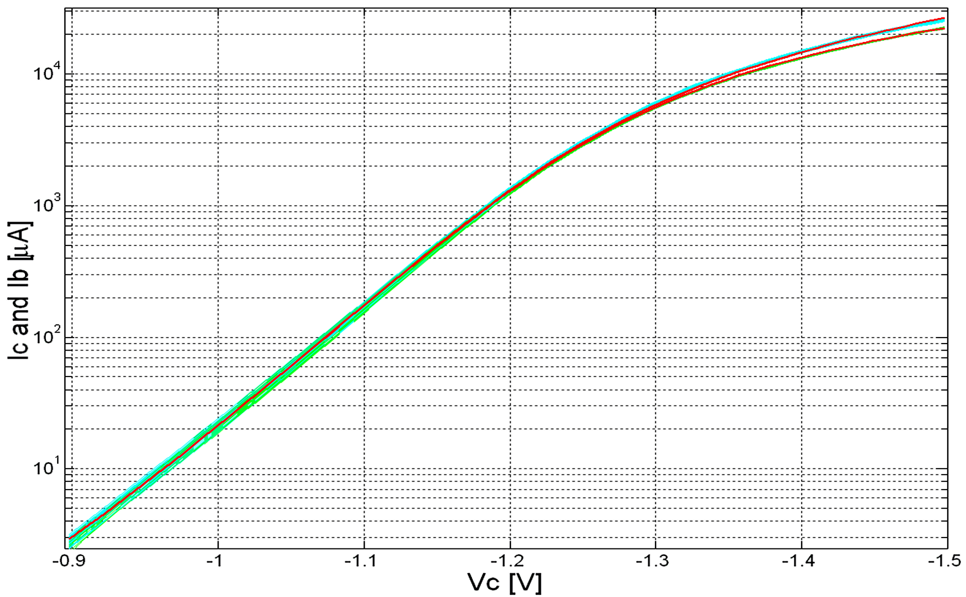

Figure 4.11. Reverse Gummel plot.

Figure 4.12 and Figure 4.13 show the collector current and respectively the base voltage versus the collector-emitter voltage. The red lines are the simulated curves.

The blue crosses are the measured values. The measured values and the simulated curves matches very well. There are a slight difference in the base voltage for the highest base current. But the error is less than 15 mV.

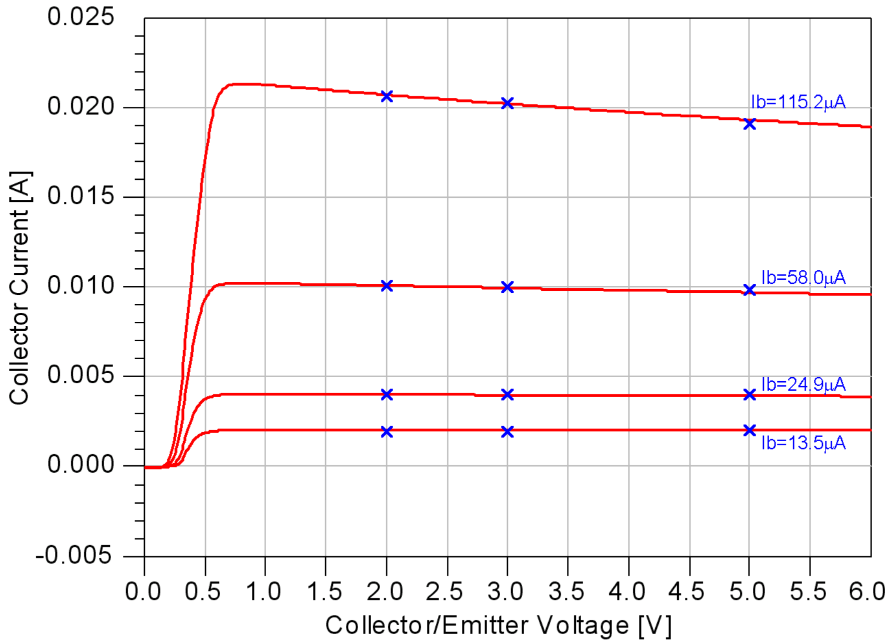

Figure 4.12. I_C versus V_{CE} plot.

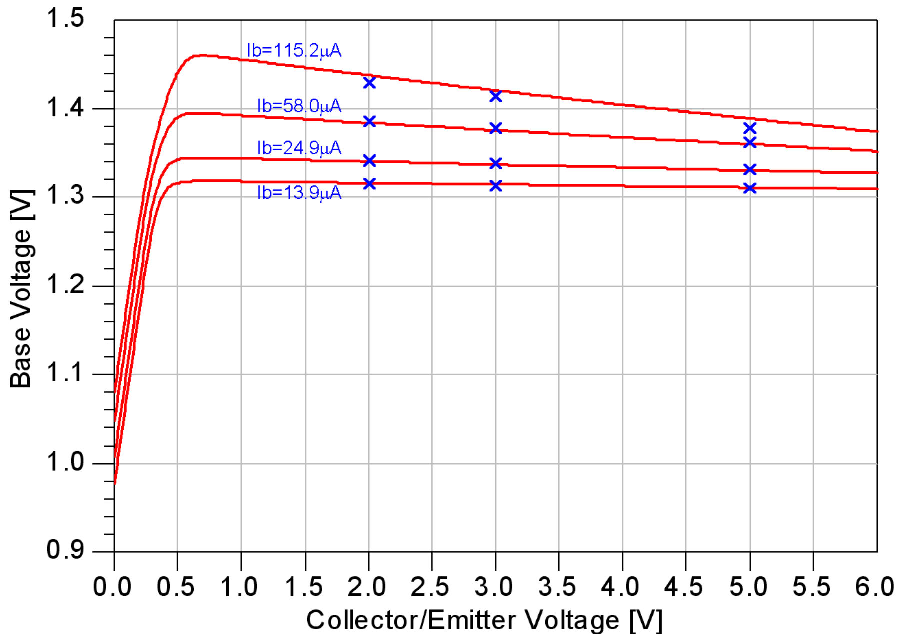

Figure 4.13. V_B versus V_{CE} plot.

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Figure 4.14 and Figure 4.15 show the Cold-Capacitor s-parameter measurements. Only every other base voltage listed in Table 4.26 were plotted to reduce over crowding of the figures. The measurements range from V_b = -2.5 V to V_b = 1.1 V.

In Figure 4.14, the red lines and crosses indicates S_{11}, and the green lines and crosses indicates $-S_{22}$. S_{22} is rotated 180 degrees in Figure 4.14 in order to be plotted in the same figure. In Figure 4.15, the red lines and crosses indicates the magnitude of S_{21} in dB, and the green lines and crosses indicates the phase of S_{21} in degrees. In both figures the solid lines indicates the simulated curves, while crosses indicates the measured values. The S_{12} was not plotted, due to reciprocity.

The measured values and the simulated curves matches very well for all curves except some minor differences in the results for V_b = 1.1 V.

Overall, the extracted model shows a great match to the Cold-Capacitor measurement.

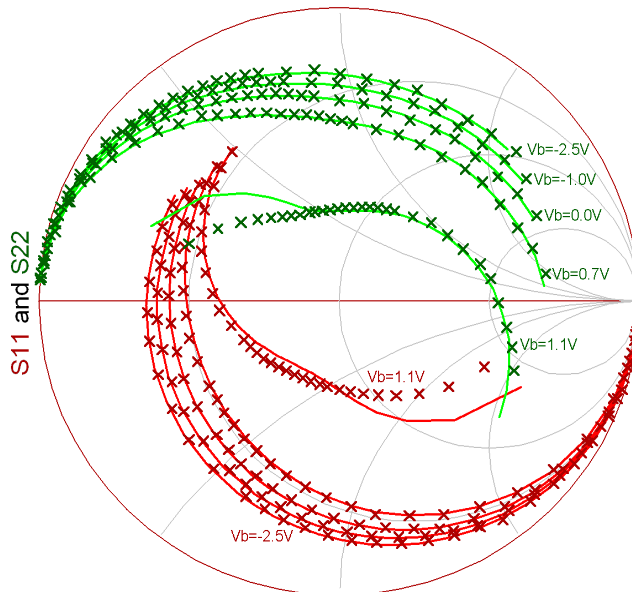

Figure 4.14. Cold Capacitor: S_{11} and S_{22}.

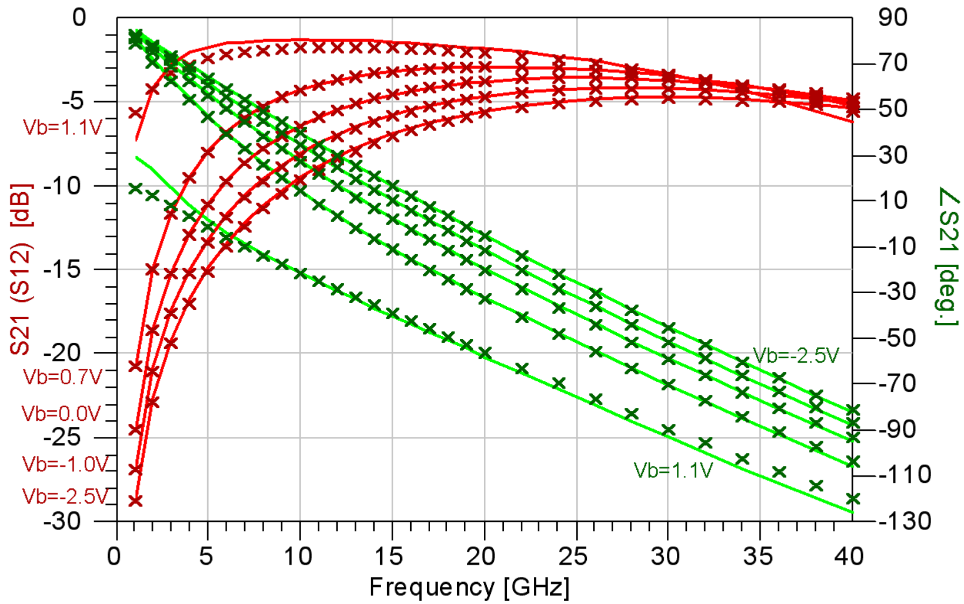

Figure 4.15. Cold Capacitor: S_{21} and S_{12} plot.

The active s-parameters have been measured at three different collector-emitter voltages, and at four different collector currents for each collector-emitter voltage. Only the results representing the upper and lower part of the I_C-V_{CE} region are displayed, i.e. only the lowest (I_c = 2 mA) and the highest (I_c = 20 mA) collector currents. In the area in the middle of the I_C-V_{CE} region (I_c = [4,10] mA), the extracted model matches the measured s-parameters better than in the upper and lower regions, and are therefore not shown. All three different collector-emitter voltages are plotted for these collector currents.

Figure 4.16 - 4.19 show the s-parameters for the lowest collector current I_c = 2 mA. All three collector-emitter voltages (V_{ce} = [2,3,5] V) are plotted. In all the figures, the solid lines indicate simulated curves, while crosses indicate the measured values. In Figure 4.16, the red lines and crosses indicate S_{11} and the green lines and crosses indicate S_{22}. In Figure 4.17 - 4.19, the red lines and crosses indicate the magnitude of S_{21} and S_{21} both in dB, and the green lines and crosses indicate the phase of S_{21} and S_{21} both in degrees.

There are a some difference between the measured values and the simulated curves, but overall the model matches the measured s-parameters very well over the whole frequency span up to 40 GHz. S_{12} have the highest mismatch. There is a maximum magnitude error of about 3.5 dB and a phase error of 20 degrees at 40 GHz. This may be due to uncertainties in the calibration, i.e. ‘omit isolation’ etc.

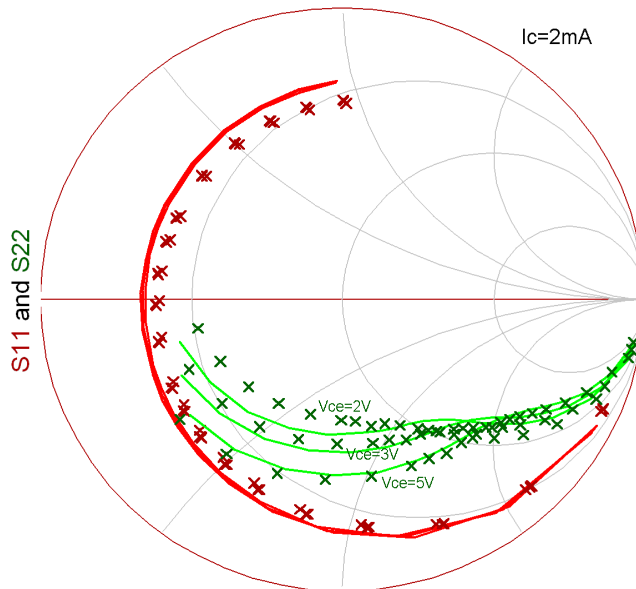

Figure 4.16. Active s-parameters: S_{11} and S_{22} (I_c = 2 mA, V_{ce} = [2,3,5] V).

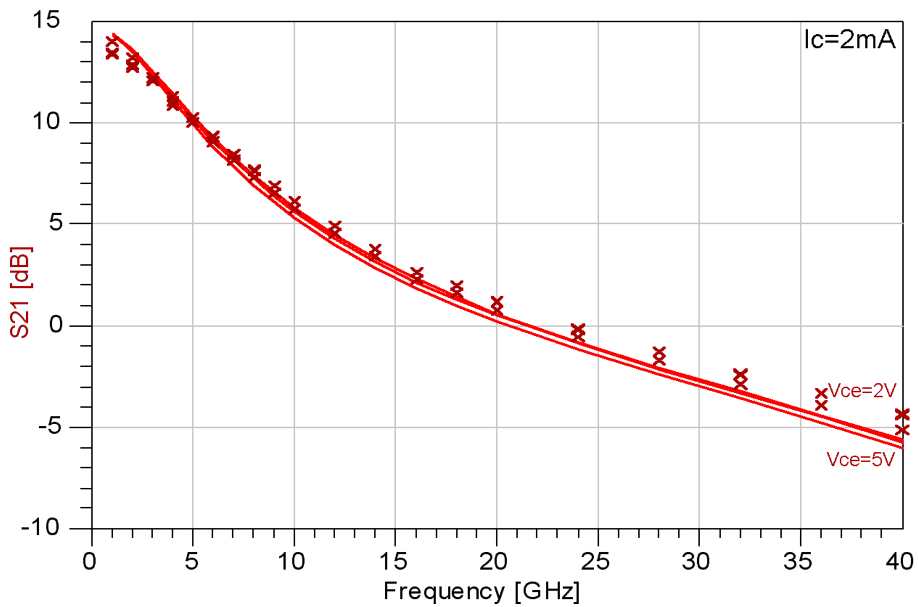

Figure 4.17. Active s-parameters: S_{21} magnitude (I_c = 2 mA, V_{ce} = [2,3,5] V).

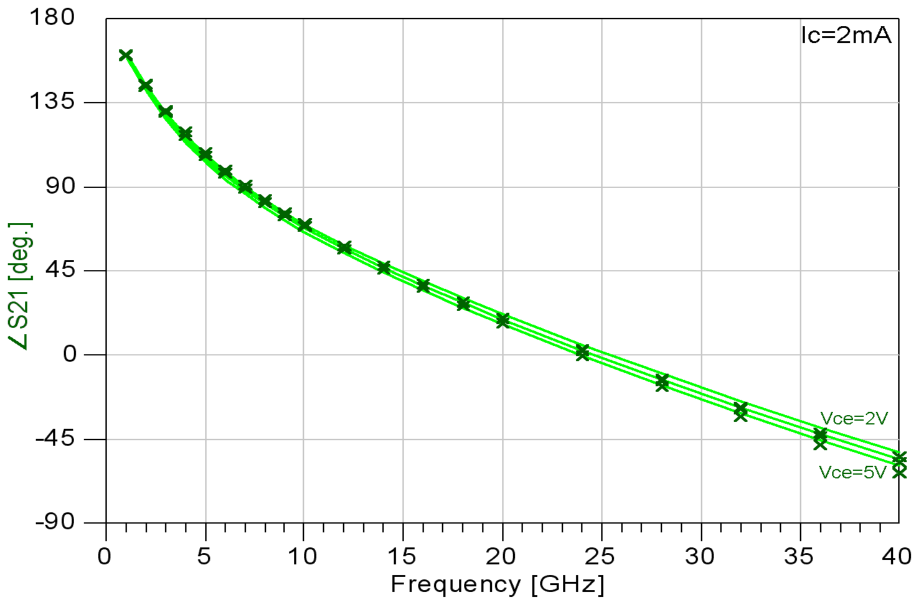

Figure 4.18. Active s-parameters: S_{21} phase (I_c = 2 mA, V_{ce} = [2,3,5] V).

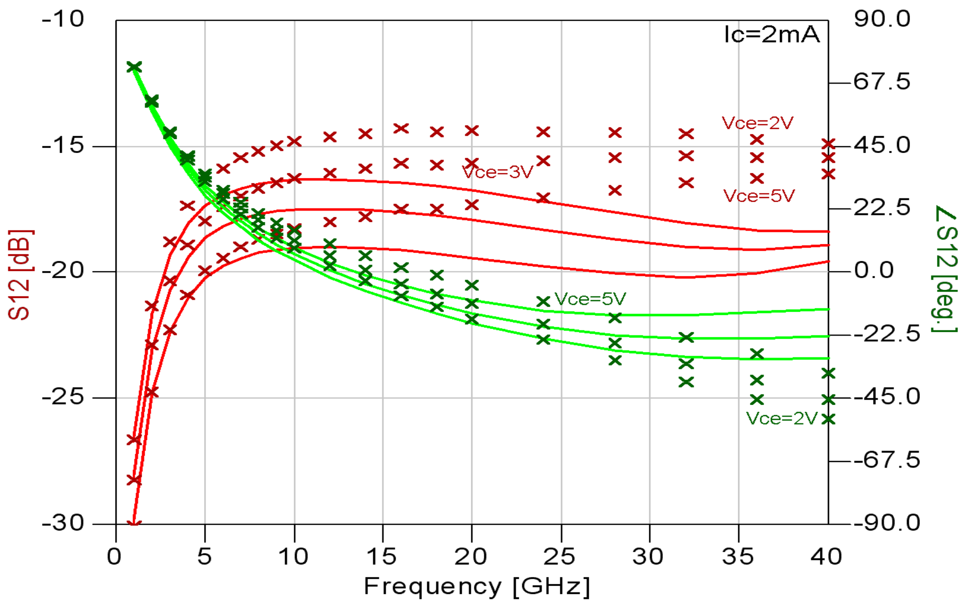

Figure 4.19. Active s-parameters: S_{12} (I_c = 2 mA, V_{ce} = [2,3,5] V).

Figure 4.20 - 4.23 show the s-parameters for the highest collector current I_c = 20 mA. All three collector-emitter voltages (V_{ce} = [2,3,5] V) are plotted. In all the figures, the colour choice are the same as for the figures with the low collector current.

There are a some difference between the measured values and the simulated curves, but overall the model matches the measured s-parameters very well over the whole frequency span up to 40 GHz. The extracted model parameters also predicts the Kink-effect [89] in S_{22} very well. S_{21} and S_{12} have the highest mismatch. There is a maximum magnitude error of about 1.5 dB and a maximum phase error of about 15 degrees.

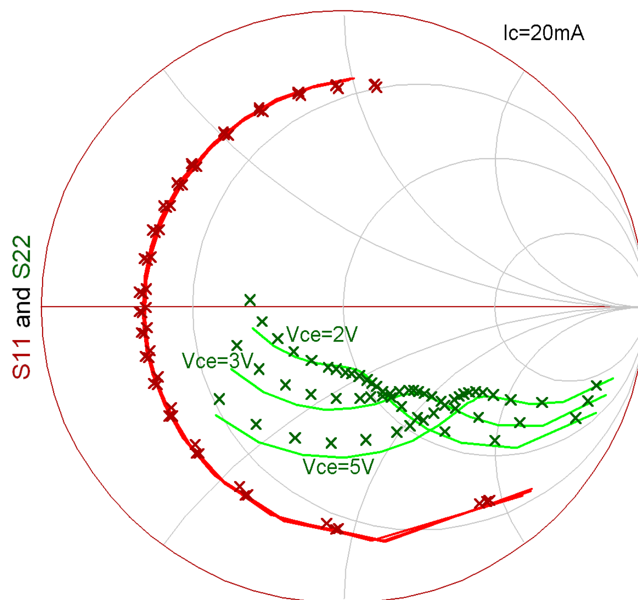

Figure 4.20. Active s-parameters: S_{11} and S_{22} (I_c = 20 mA, V_{ce} = [2,3,5] V).

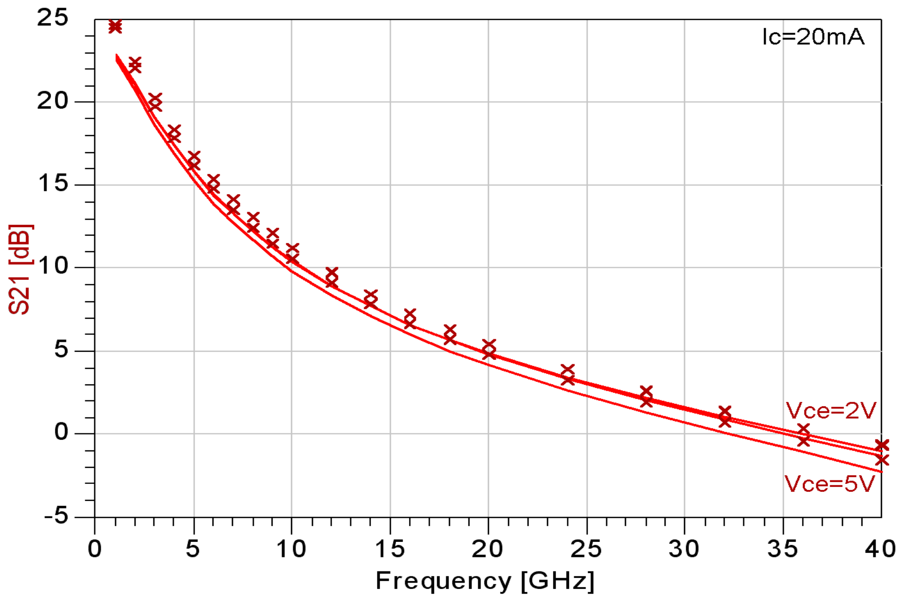

Figure 4.21. Active s-parameters: S_{21} magnitude (I_c = 20 mA, V_{ce} = [2,3,5] V).

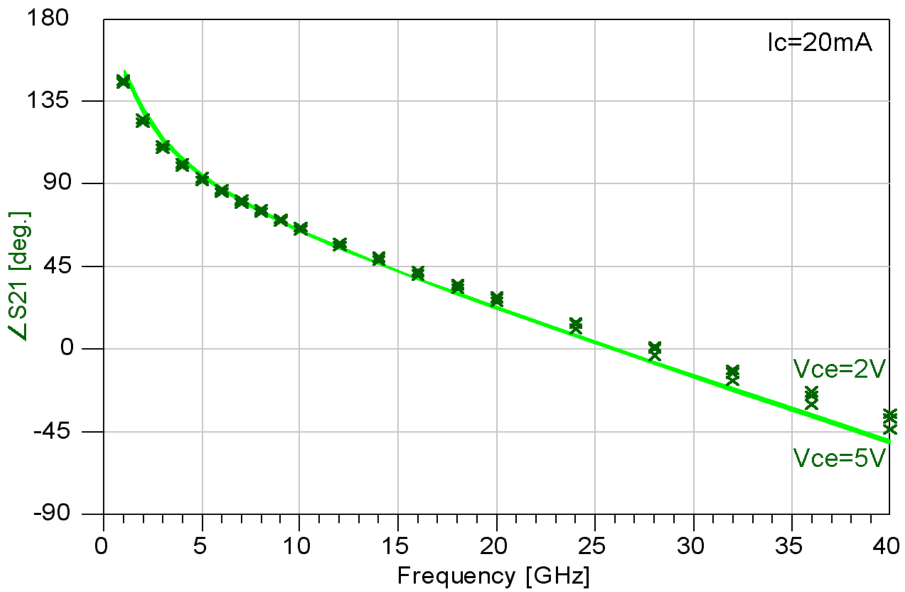

Figure 4.22. Active s-parameters: S_{21} phase (I_c = 20 mA, V_{ce} = [2,3,5] V).

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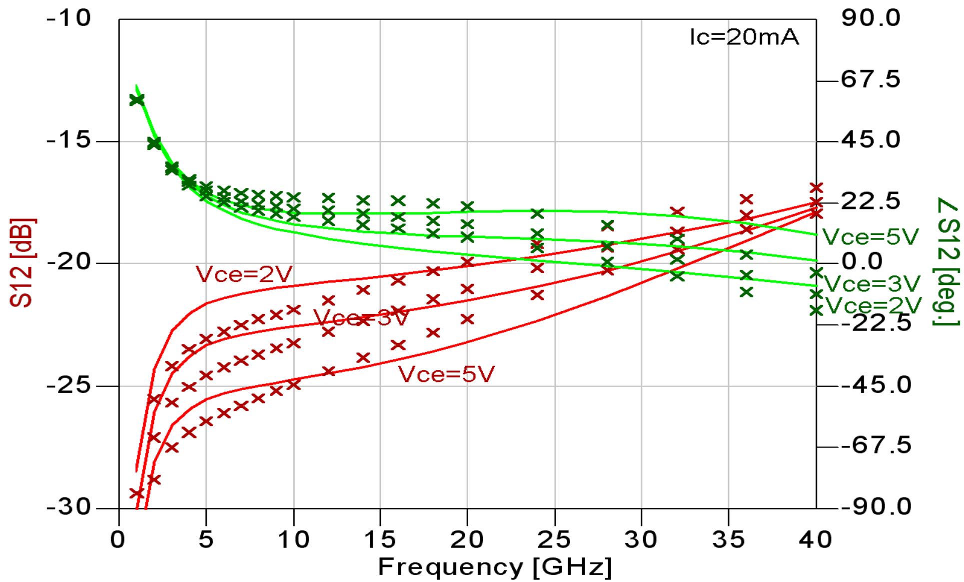

Figure 4.23. Active s-parameters: S_{12} (I_c = 20 mA, V_{ce} = [2,3,5] V).

The practical parameter extraction algorithm presented in Section 4.3.2 applied to the InGaP/GaAs HBT's provided by Caswell Technology, leads to a model that matches the measured data with high accuracy. Only four iterations are needed to acquire a set of very good parameters for the VBIC model.

4.5 Results for the SiGe/Si HBT

4.5.1 Devices and Instrumentation

The SiGe transistors had an emitter up structure, just as the InGaP/GaAs from Caswell Technology. But there were a major difference in the connections to the probe pads. The collector was connected to the ground. The base was connected to the left centre pad, and the emitter was connected to the right centre pad. This can be seen in Figure 3.25. With this layout structure, the transistors are connected as an emitter-follower, and all the measurement on the transistors were accordingly.

Figure 4.24 shows the layout of the 20 transistors available. All the transistors had a emitter finger length of 10 µm. The width of the emitter fingers varied from 0.4 µm to 1.6 µm. There were single-, 2- and 8-finger transistors. Table 4.28 shows what kind of transistors that were available.

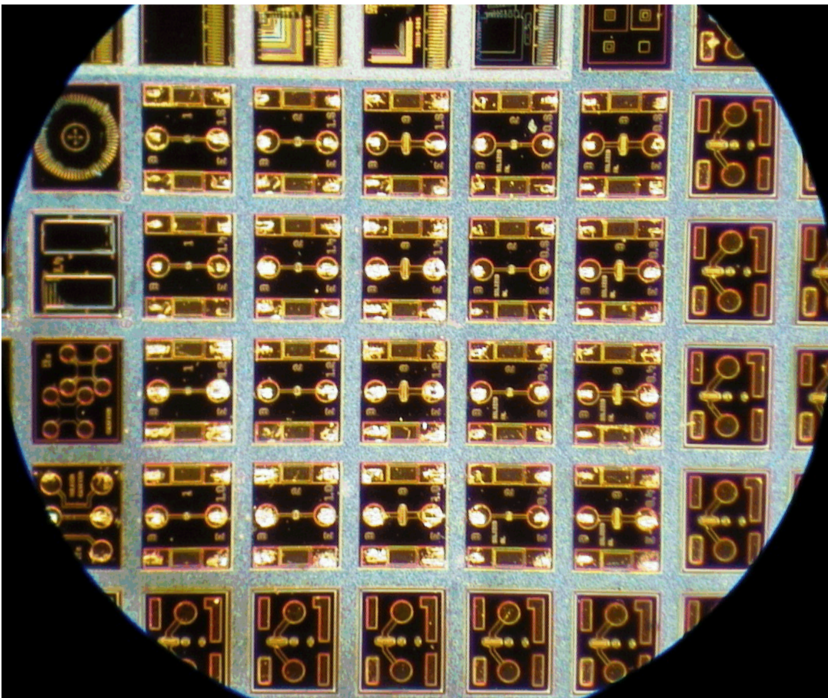

Figure 4.24. Layout of the 20 SiGe transistors.

Only one transistor of each type was available, except for the 2- and 8-finger of emitter width 0.4 µm and 0.6 µm, where two specimens were available.

Table 4.28. Available SiGe transistor types.

	Single Finger	2-Finger	8-Finger
Emitter width [µm]	1.0, 1.2, 1.4, 1.6	0.4, 0.6, 1.0, 1.2, 1.4, 1.6	0.4, 0.6, 1.0, 1.2, 1.4, 1.6
Damaged Devices	1.0, 1.2	1.0, 1.2	1.0, 1.2

All the transistors in the upper row of Table 4.28 were measured. The measurements were carried out on a probe station with a Vector Network Analyser (VNA), and a programmable automatic DC power supply. The instrumentation for all the measurements is listed below.

- Summit 9000 Cascade probe station.
- PicoProbe 50A-GSG-100-P, Ground-Signal-Ground 100μm pitch probes.
- CS-5 GGB Industries calibration substrate.
- HP 8510C 40 GHz 2.4mm Vector Network Analyser.
- HP 4142B Programmable DC Power source.
- PC with Software, cables, mercury thermometer, etc.

In Figure 4.25 the measurement setup with probe station, the VNA and the computer is shown. The DC power supply is located in a rack under the table.

Figure 4.25. Probe station and the measurement setup.

4.5.2 DC Calibrations and Measurements

The HP 4142B was connected to the backside of HP 8510C VNA, and the dc was fed through the VNA in the same cables as used for s-parameter measurements. The instruments were controlled by HP VEE software. Some features, i.e. cold capacitor measurement, had to be implemented in the HP VEE program for this type of devices.

Calibration:

The HP 4142B is capable of applying and measuring both currents and voltages on each port. The measurement reference is inside the unit itself. The resistances of the cables including the probes have to be measured, in order to de-embed the dc measurements. Two different measurements were carried out to characterize the

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cables. First, the series resistance was found by measuring the short on the CS-5 calibration substrate. Two shorts where measured. Second, the shunt resistance was found by measuring an open with the probes lifted. The open was measured only once. This should ideally be infinite.

The shunt resistance is much higher than the series resistance, so the series resistance was calculated by disregarding the shunt resistance and opposite. Table 4.29 shows the measured values and the resistances.

Table 4.29. DC calibration results.

	Port 1			Port 2		
	Short 1	**Short 2**	**Open**	**Short 1**	**Short 2**	**Open**
Measured Voltage [V]	$40.0 \cdot 10^{-3}$	$40.0 \cdot 10^{-3}$	20.00	$40.0 \cdot 10^{-3}$	$40.0 \cdot 10^{-3}$	20.00
Measured Current [A]	$13.8 \cdot 10^{-3}$	$13.8 \cdot 10^{-3}$	$20.17 \cdot 10^{-6}$	$26.2 \cdot 10^{-3}$	$26.4 \cdot 10^{-3}$	$20.06 \cdot 10^{-6}$
Calculates resistance [Ω]	2.89	2.89	992K	1.53	1.52	997K

In the modelling a series resistance of 2.89 Ω and a shunt resistance of 992 kΩ will be used on port 1. On port 2 a series resistance of 1.53 Ω and a shunt resistance of 997 kΩ will be used.

Measurements:

Measuring SiGe transistors may be difficult due to the oxidation of aluminium on the probe pads. The probes had to be placed, with slide, on the probe pads 3-4 times to be able to scratch through the oxidation and insure good connection. In Figure 4.24 the scratch marks are highly visible.

Table 4.30 shows all the types of DC measurements that were performed, and all the measurement ranges.

Table 4.30. DC measurement types and measurement ranges.

Type	Transistor	Range
Forward Gummel	All except 8x1.4, 8x1.6	V_{EC}=[0, -0.95]V 100 steps
	8x1.4, 8x1.6	V_{EC}=[0, -1.00]V 100 steps
Reverse Gummel	All except 8x1.4, 8x1.6	V_{BC}=[0, 0.95]V 100 steps
	8x1.4, 8x1.6	V_{BC}=[0, 1.00]V 100 steps
Active IV	1x1.4	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 200]μA Step=10μA
	1x1.6	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 230]μA Step=10μA
	2x0.4, 2x0.6	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 300]μA Step=20μA
	2x1.4, 2x1.6	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 400]μA Step=20μA
	8x0.4	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 340]μA Step=20μA
	8x0.6	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 380]μA Step=20μA
	8x1.4, 8x1.6	V_{EC}=[0, -3.0]V 200 steps, I_B=[0, 1.0]mA Step=50μA

Table 4.30. DC measurement types and measurement ranges.

Type	Transistor	Range
Breakdown IV	1x1.6	V_{EC}=[0, -4.5]V 200 steps, I_B=[0, 25]μA Step=5.0μA
	2x1.6	V_{EC}=[0, -4.5]V 200 steps, I_B=[0, 40]μA Step=5.0μA
	2x1.6	V_{EC}=[0, -4.5]V 200 steps, I_B=[0, 100]μA Step=10μA

Figure 4.26 shows the probes, the SiGe chip, and the placement of the mercury thermometer. The temperature in the room was noted for each measurement that was performed. The accuracy of the mercury thermometer was about 0.5 degrees. In the parameter extraction, in Section 4.5.4 and Section 4.5.5, the corresponding temperature was inserted for each measurement.

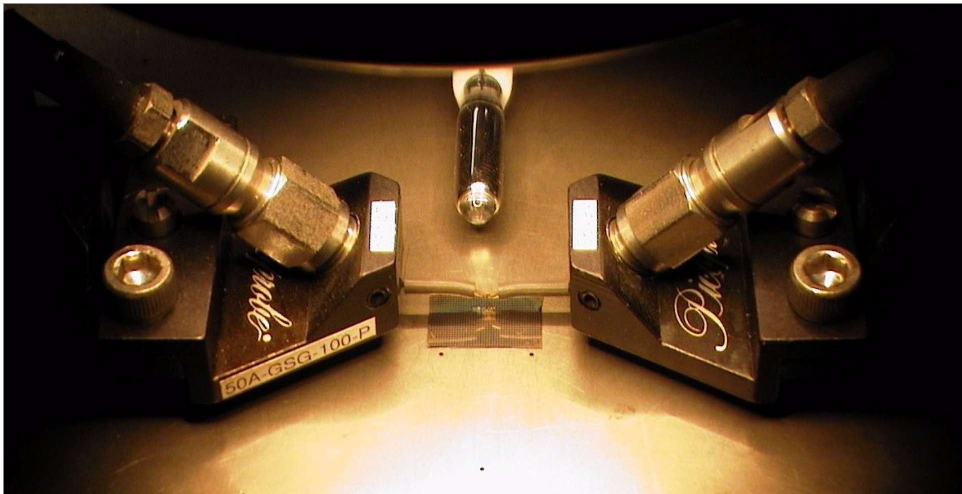

Figure 4.26. The probes and the mercury thermometer.

4.5.3 S-Parameter Calibrations and Measurements.

Calibration:

Before the calibration procedure can start, it is important that the power level from the VNA does not drive the transistor into compression. A theoretical maximum output power level can be calculated by assuming an ideal class A operation from a normal bias point. The gain of the transistors in an emitter follower circuit may be about 6 dB. To ensure linear operation the input power level should be at least 20 dB lower than the maximum input power level. These values are shown in column 3-5 in Table 4.31. The maximum output level from the VNA is 2 dBm [90]. The built in attenuators in the VNA can be set in steps of 10 dB attenuation. The dynamic range and accuracy of the VNA reduces when the attenuation increase. Therefore the attenuators should be set to as low attenuation as possible. Table 4.31 shows the estimated power levels from three different transistors and the required level of attenuation in the VNA. Since all the measurements are low level linear measurements, both ports were set to the same attenuation.

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Table 4.31. Estimated maximum power level and HP 8510 attenuation.

	Normal Bias	Class A P_{out} max	Class A P_{in} max	Linear P_{in} max	P_{out} HP 8510 Port 1&2	HP 8510 Attenuator
1x1.6x10	V_{CE}=2V, I_E=5mA	7 dBm	1 dB	-19 dBm	2 dBm	20 dB
2x1.6x10	V_{CE}=2V, I_E=10mA	10 dBm	4 dB	-16 dBm	2 dBm	20 dB
8x1.6x10	V_{CE}=2V, I_E=40mA	16 dBm	10 dB	-10 dBm	2 dBm	10 dB

The LRM (Line-Reflect-Match) calibration procedure was used with the probes on a CS-5 calibration substrate from GGB Industries. The calibration substrate was rather worn, so it was sometimes difficult to get a good calibration. The calibration was evaluated by re-measuring some of the calibration components. The temperature in the room changed rather much during the day, due to the direct sunlight. This caused especially phase drift in the measurement equipment. Re-calibration was done every 3-4 hours. The complete measurement series of all the transistors including the DC took about 2 days.

Measurements and de-embedding:

There were no de-embedding structures available on the chip. The pads and the line from the pads to the transistor should have been de-embedded from the measurements. Instead, the VBIC model was embedded with an ideal line at the emitter and at the base. The Agilent LineCalc was used, with $\varepsilon_r = 10.7$ for Si, to find the characteristic impedance and the electrical length from the length and the width of the physical line. This was only an approximation, since the accuracy of the dimensions of the physical line were rather poor. A capacitor, C_{PAD}, was added at the end of the ideal lines, as a pad model. The value of this capacitor was unknown, and had to be included in the parameter extraction algorithm. It was chosen to find this capacitor in *Step 9*, in Section 4.5.4.

Table 4.32 shows all the types of s-parameter measurements that were performed, and all the measurement ranges. The frequency range was 0.1 GHz to 40 GHz.

Table 4.32. S-parameter measurement types and measurement ranges.

Type	Transistor	Range
Cold Capacitor	All	V_B=[-2.4, 0.4]V step=0.4V
Active s-parameter	1x1.4	V_{EC}=-[0.5, 3.0]V Step=-0.5V, I_B=[10, 210]µA Step=50µA
	1x1.6	V_{EC}=-[0.5, 3.0]V Step=-0.5V, I_B=[10, 230]µA Step=55µA
	2x0.4, 2x0.6	V_{EC}=-[0.5, 3.0]V Step=-0.5V, I_B=[10, 290]µA Step=70µA
	2x1.4, 2x1.6	V_{EC}=-[0.5, 3.0]V Step=-0.5V, I_B=[10, 385]µA Step=75µA
	8x0.4	V_{EC}=-[0.5, 3.0]V Step=-0.5V, I_B=[10, 340]µA Step=85µA
	8x0.6	V_{EC}=-[0.5, 3.0]V Step=-0.5V, I_B=[10, 370]µA Step=90µA
	8x1.4, 8x1.6	V_{EC}=-[0.5, 3.0]V Step=-0.5Vs, I_B=[0.02, 1]mA Step=140µA

The room temperature was noted for each measurement that was performed. The corresponding temperature was inserted for each measurement used in the parameter extraction.

4.5.4 Results for a single finger 1x1.6x10μm SiGe transistor

Table 4.33 shows the parameters in the VBIC model as they were being extracted. The starting values were just an initial “guess”. No attempt was made to estimate good starting values. This confirmed that the parameter extraction algorithm works well with just an initial “guess’. This may result in more iterations.

The process required two steps more than the parameter extraction for the InGaP/GaAs transistor. This is mainly due to the quasi saturation and distributed base parameters that had to be included in the extraction for the SiGe transistors.

Table 4.33. VBIC parameters and their extracted values for the 1x1.6x10.

Step	Param.	x	Initial value	1. iter.	2. iter.	3. iter.	4. iter.	5. iter.	6. iter.
1	R_{TH}	1	**564**						
	C_{TH}	10^{-9}	**-**						
2	I_{BEI}	10^{-18}	1	1.30	1.30	**1.30**			
	N_{EI}	1	1.1	1.019	1.020	**1.020**			
	I_S	10^{-18}	1	193	195	**195**			
	N_F	1	1.1	1.042	1.040	**1.040**			
3	I_{BCI}	10^{-18}	1	7.18	7.31	**7.33**			
	N_{CI}	1	1.2	1.0004	1.0004	**1.0004**			
	N_R	1	1.1	1.012	1.012	**1.012**			
4	R_E	1	5	7.02	6.05	6.48	6.33	6.37	**6.34**
5	R_{CX}	1	5	8.87	5.38	2.68	1.94	1.89	**1.86**
6	R_{BX}	1	5	0.502	2.93	4.57	5.67	6.02	**5.98**
	I_{KR}	10^{-6}	0	609	677	653	654	655	**655**
7	X_{II}	1	3	6.53	6.47	6.54	6.61	6.61	**6.62**
8	I_{KF}	10^{-3}	0	12.5	12.8	12.6	12.7	12.7	**12.7**
	V_{EF}	1	0	200	111	233	240	244	**246**
	R_{CI}	1	0	40.4	12.1	35.2	36.0	36.0	**36.0**
	V_O	10^{-3}	0	386	24.3	596	538	512	**491**
	G_{AMM}	10^{-12}	0	71.8	3.26	9.21	9.34	9.46	**9.51**
	H_{RCF}	1	1	1.98	1.55	0.316	0.350	0.379	**0.384**
	C_{PAD}	10^{-15}	0		42.5	33.5	32.9	32.9	**32.9**
	C_{JE}	10^{-15}	1		42.2	43.5	43.3	43.7	**43.3**

Table 4.33. VBIC parameters and their extracted values for the 1x1.6x10.

Step	Param.	x	Initial value	1. iter.	2. iter.	3. iter.	4. iter.	5. iter.	6. iter.
9	C_{JC}	10^{-15}	1		17.4	25.5	26.2	27.4	**27.2**
	C_{BEO}	10^{-15}	1		0.173	0.104	0.107	0.105	**0.104**
	C_{BCO}	10^{-15}	1		21.8	48.4	48.5	47.8	**47.7**
	L_B	10^{-12}	1		8.44	0.0555	0.132	0.0762	**0.0763**
	L_C	10^{-12}	1		164	77.0	81.2	74.5	**74.4**
	L_E	10^{-12}	1		159	91.3	101	91.1	**92.4**
10	P_E	1	0.946		1.16	1.21	1.22	1.27	**1.22**
	M_E	1	0.107		0.493	0.510	0.512	0.534	**0.508**
	A_{JE}	10^{-3}	0.138		0.418	0.100	0.101	0.103	**0.106**
	P_C	1	1		0.334	0.714	0.758	0.801	**0.750**
	M_C	1	0.563		0.187	0.235	0.238	0.230	**0.230**
	A_{JC}	10^{-3}	0.01		40.6	81.7	91.8	101	**105**
	FC	1	0.975		0.796	0.960	0.976	0.985	**0.971**
11	T_F	10^{-12}	5		4.50	2.16	2.09	2.03	**2.04**
	I_{TF}	10^{-3}	10		69.3	42.0	39.7	43.5	**43.5**
	V_{TF}	1	1		0.148	2.21	3.04	2.80	**2.75**
	X_{TF}	1	0		0.476	1.50	1.60	1.60	**1.60**
	Q_{TF}	1	0		0.00725	0.650	0.684	0.676	**0.676**
12	A_{VC1}	1	0		13.3	16.7	17.0	17.4	**16.9**
	A_{VC2}	10^{-3}	0		139	397	432	438	**399**
	R_{BI}	1	10		24.7	28.8	26.0	26.9	**26.9**

Each step and iteration in Table 4.33 are based on the results obtained in preceding steps. After performing *Step 2-8*, these steps were repeated in a second iteration. In the second iteration, it was decided to continue into *Step 9*, since some parameters from the next steps influence the DC performance.

The third iteration were started from *Step 2*. After iteration 3 were complete, the results from iteration 2 and iteration 3 were compared. The changes in values for *Step 2* and *Step 3* were very small, therefore there were no need for further iterations of these steps.

The fourth iteration were preformed from *Step 4*.

Two more iterations had to be performed until the values between consecutive iterations where small enough. The inclusion of the quasi saturation parameters and base distribution R_{BI}, made it necessary to perform six iterations.

In all the curves presented below, there are solid lines and crosses. The crosses, with colours blue, dark red and dark green, indicate measured values. The solid lines, with colours red, light red and light green, indicate simulated values.

Figure 4.27 shows the forward Gummel plot. The simulated results matches the measured results very well. At the low current end of the base current the measured results have reached the accuracy limit of the measurement equipment. At the low current end of the emitter current, the deviation from a straight line is due to the ≈1 MΩ shunt resistance measured in the DC calibration.

Figure 4.28 shows the reverse Gummel plot. A slight deviation in the emitter current is observed for medium currents, but overall the simulated results matches the measured results quite well. At the low current end of both the emitter and base current, the deviation from a straight line is due to the ≈1 MΩ shunt resistance measured in the DC calibration.

Figure 4.29 shows the emitter current versus the collector-emitter voltage. This figure include the ordinary IV measurement up to $V_{CE} = 3$ V, and the breakdown IV curves up to $V_{CE} = 4.5$ V. There are a slight difference between the measured and the simulated emitter current at the highest currents around $V_{CE} = 0.5$ V. But the error is less than 4 %. Overall, the measured values matches the simulated curves very well.

The breakdown IV curves should have been measured at higher currents for higher accuracy in the extraction of the weak avalanche parameters.

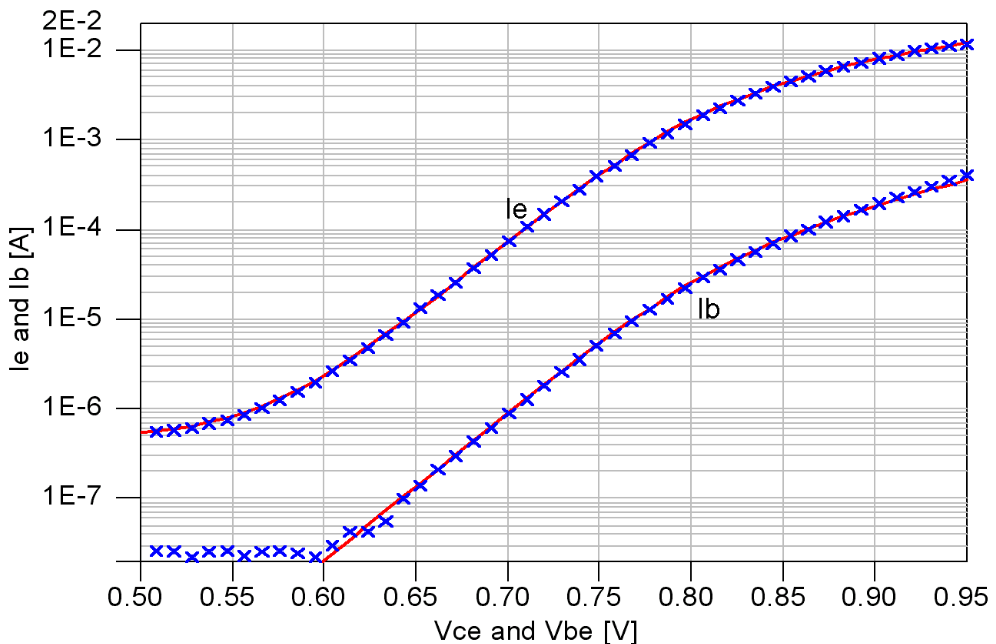

Figure 4.27. Forward Gummel plot.

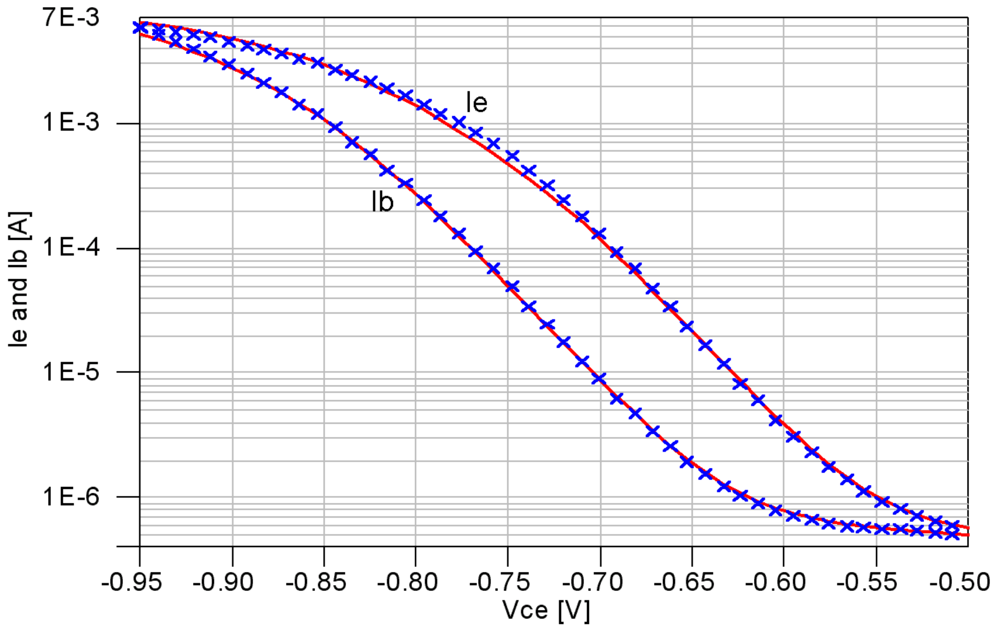

Figure 4.28. Reverse Gummel plot.

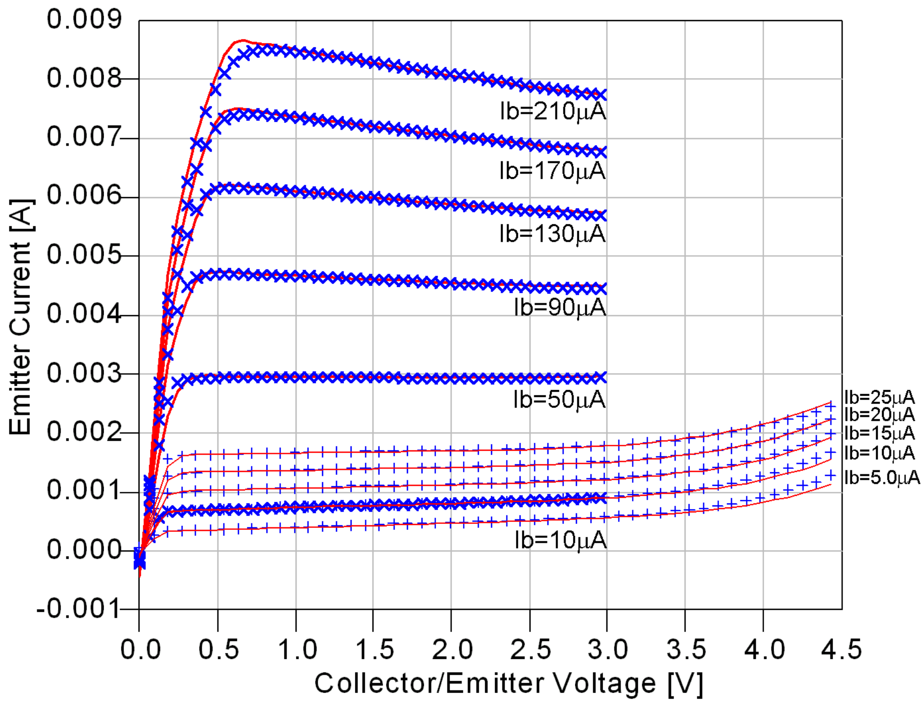

Figure 4.29. I_E versus V_{CE} plot.

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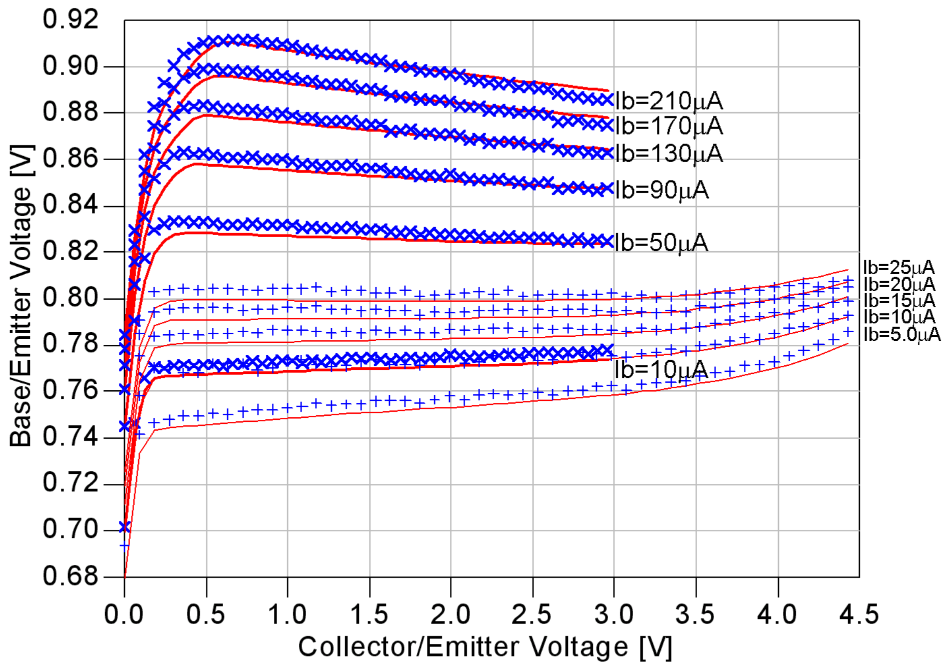

Figure 4.30. V_{BE} versus V_{CE} plot.

Figure 4.30 shows the base-emitter voltage versus the collector-emitter voltage. This figure include the ordinary IV measurement up to V_{CE} = 3 V, and the breakdown IV curves up to V_{CE} = 4.5 V. The simulated values are slightly lower than the measured valued. The error is less than 8 mV (1%). Overall, the measured values matches the simulated curves very well.

Figure 4.31 and Figure 4.32 show the Cold-Capacitor s-parameter measurements. Only every other base voltage listed in Table 4.26 were plotted to reduce over crowding of the figures. The measurements range from V_b = -2.0V to V_b = 0.4V.

In Figure 4.31, the red lines and crosses indicates S_{11}, and the green lines and crosses indicates -S_{22}. S_{22} is rotated 180 degrees in Figure 4.31 in order to be plotted in the same figure. In Figure 4.32, the red lines and crosses indicates the magnitude of S_{21} in dB, and the green lines and crosses indicates the phase of S_{21} in degrees. The S_{12} was not plotted, due to reciprocity.

The measured values and the simulated curves matches quite well for all curves up to at least 10 GHz. There are some differences, especially in the phase, for all the s-parameters at the highest frequencies. More comments on the deviations will be given later in this section. Overall, the extracted model shows a good match to the Cold-Capacitor measurement.

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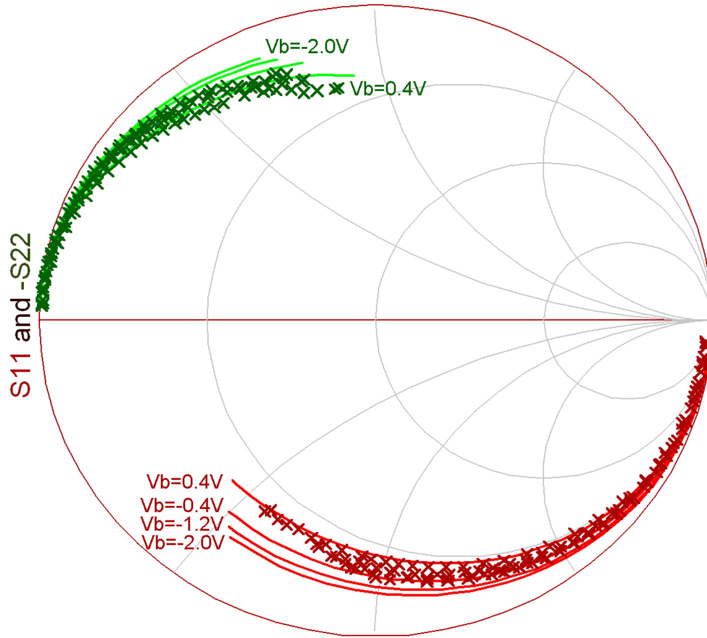

Figure 4.31. Cold Capacitor: S_{11} and $-S_{22}$.

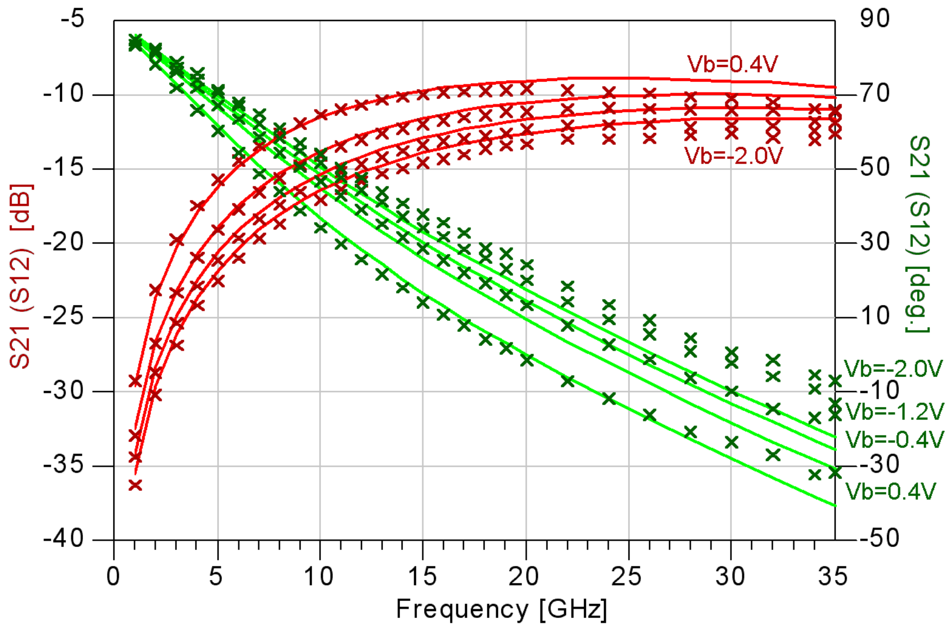

Figure 4.32. Cold Capacitor: S_{21} and S_{12} plot.

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Figure 4.33 - 4.35 show the s-parameters for a base current I_B = 10 µA. Three collector-emitter voltages, V_{ce} = [1, 2, 3] V, are plotted. This covers the lower part of the IV diagram in Figure 4.29.

There are some differences between the measured values and the simulated curves. The largest difference occur at the highest frequencies in all the s-parameters. In S_{11} there is only a small phase error. In S_{22} there is some small errors in both amplitude and phase. In S_{21} and S_{12} there is an increasing phase error at the highest frequencies. More comments on the deviations will be given later in this section. Overall, the extracted model shows a good match to the s-parameter measurement.

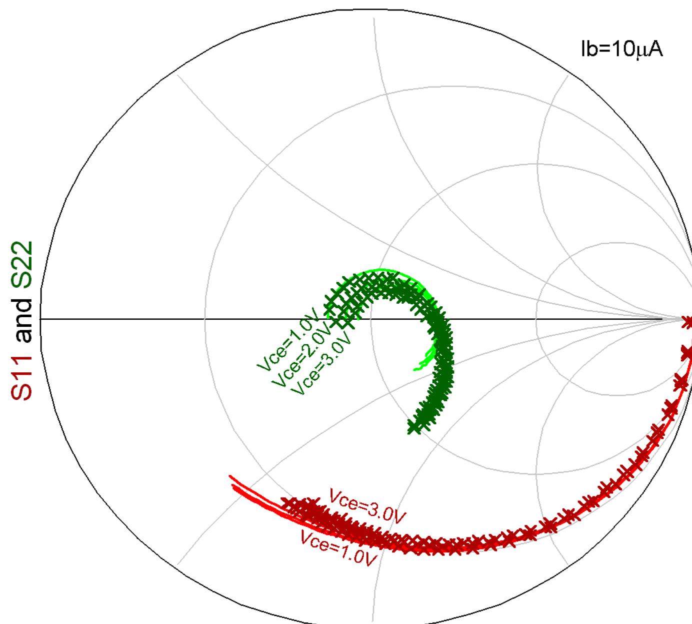

Figure 4.33. Active s-parameters: S_{11} and S_{22} (I_b = 10 µA, V_{ce} = [1,2,3] V).

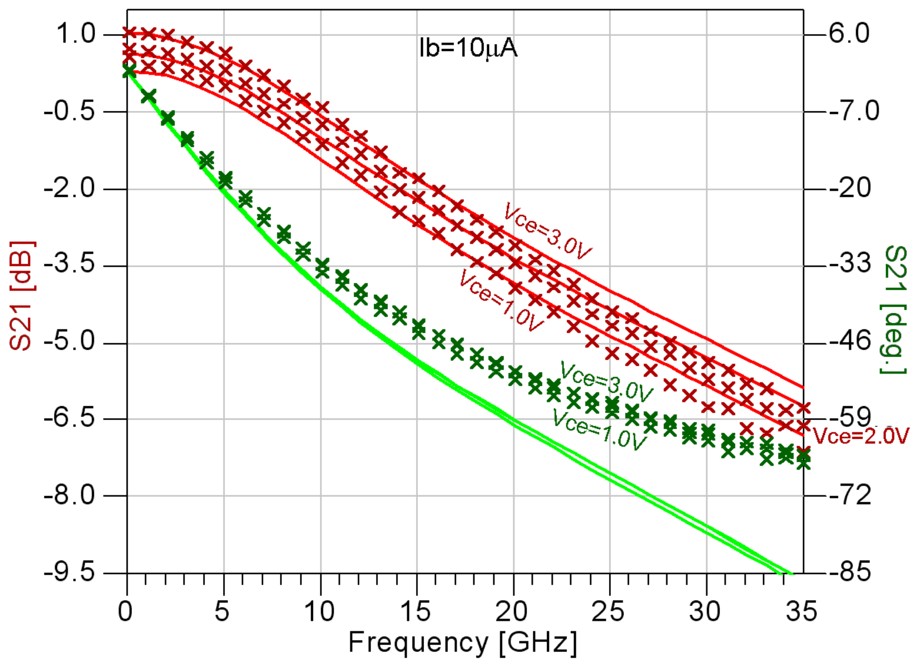

Figure 4.34. Active s-parameters: S_{21} (I_b = 10 μA, V_{ce} = [1,2,3] V).

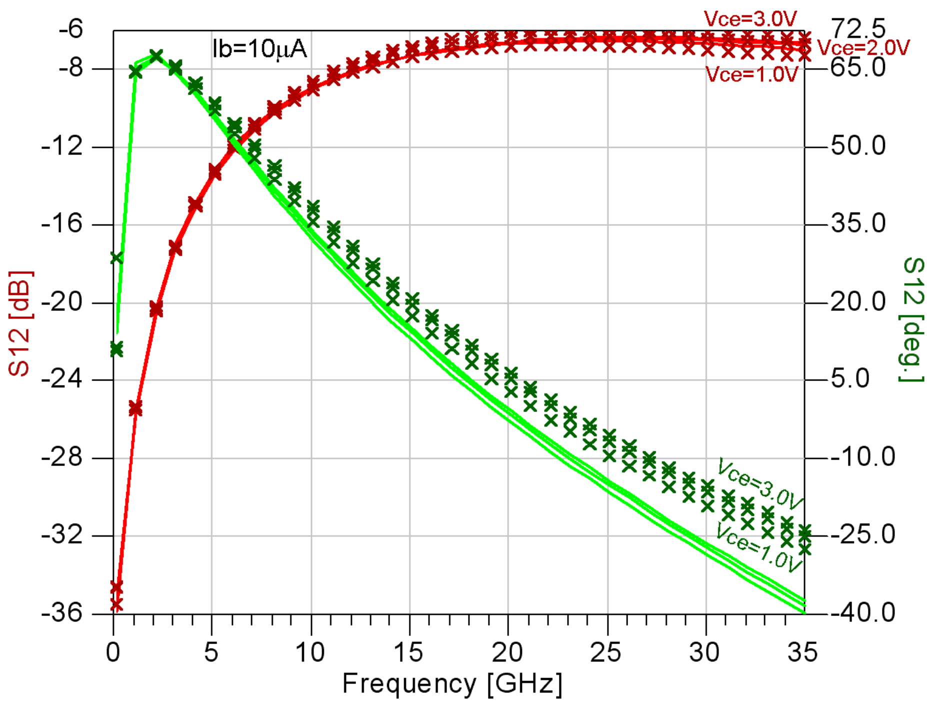

Figure 4.35. Active s-parameters: S_{12} (I_b = 10 μA, V_{ce} = [1,2,3] V).

Figure 4.36 - 4.38 show the s-parameters for a base current I_B = 230 μA. Three collector-emitter voltages, V_{ce} = [1, 2, 3] V, are plotted. This covers the higher part of the IV diagram in Figure 4.29.

There are some differences between the measured values and the simulated curves, especially at the highest frequencies. In S_{11} there is only a small phase error. In S_{22} there is some errors in both amplitude and phase. In S_{21} there is an increasing phase error up to about 25 degrees at the highest frequencies, there is also an amplitude error less than 0.8 dB. In S_{12} there is an increasing phase error up to about 16 degrees at the highest frequencies, there is also an amplitude error less than 1.3 dB. More comments on the deviations will be given later in this section. Overall, the extracted model shows a good match to the s-parameter measurement.

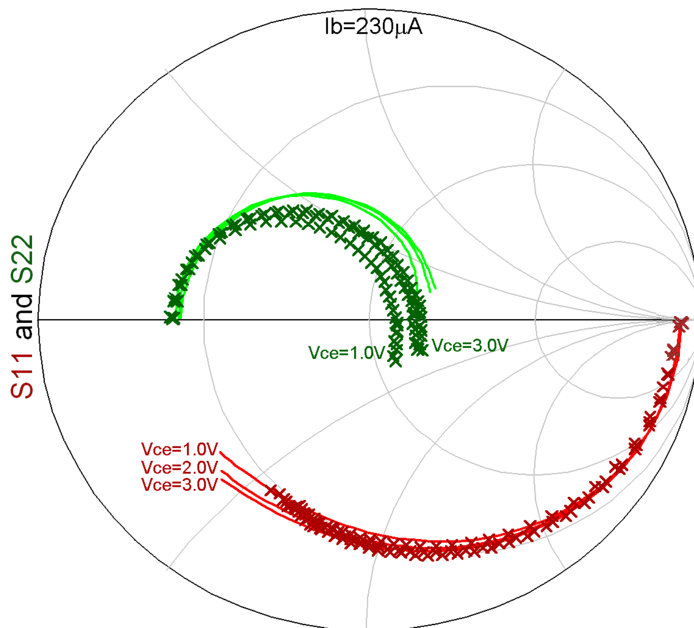

Figure 4.36. Active s-parameters: S_{11} and S_{22} (I_b = 230 μA, V_{ce} = [1,2,3] V).

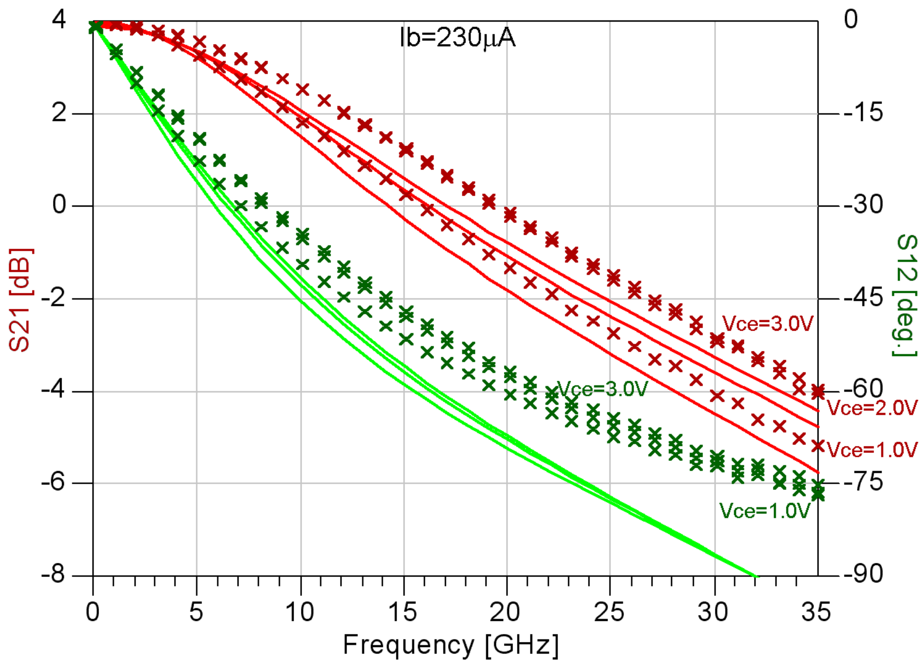

Figure 4.37. Active s-parameters: S_{21} (I_b = 230 μA, V_{ce} = [1,2,3] V).

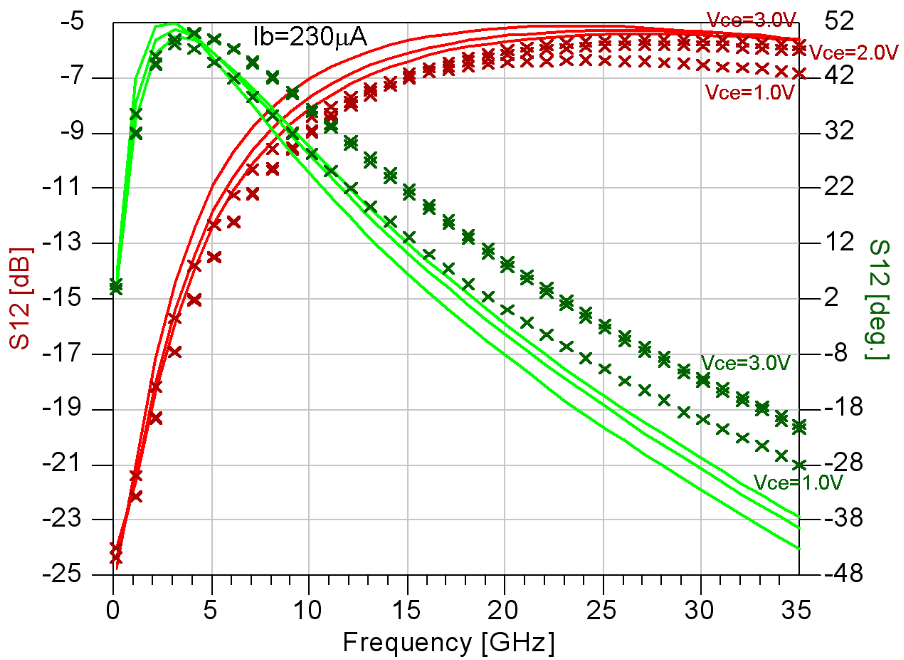

Figure 4.38. Active s-parameters: S_{12} (I_b = 230 μA, V_{ce} = [1,2,3] V).

There are four main reasons for the deviations observed in Figure 4.31 - 4.38. First, the lack of information on the feed network from the pads to the transistors will introduce errors in the simulated results. Second, the uncertainty in the calibration, due to a worn calibration substrate, may cause errors. Third, the temperature in the room changed a lot during the measurements, causing errors. Fourth, only one transistor of this type was measured.

Normally, a model should be extracted to fit the statistical average of many measured transistors. This reduces the effects of oddly behaving transistors, and in addition, some of the measurement errors will also be reduced.

4.5.5 Results for a 8-finger 8x1.6x10μm SiGe transistor

Each individual finger could have been modelled by the VBIC model, and the fingers coupled together by lines and parasitics elements. This was not possible, due to the lack of information on the transistors. The 8-finger transistor is modelled as one transistor.

Table 4.34 shows the parameters in the VBIC model as they were being extracted. The starting values were scaled values from the results of the single finger transistor.

The process required one step less than the parameter extraction for the single finger transistor. This is mainly due to good starting values.

Table 4.34. VBIC parameters and their extracted values for the 8x1.6x10.

Step	Param.	x	Initial value	1. iter.	2. iter.	3. iter.	4. iter.	5. iter.
1	R_{TH}	1	**125**					
	C_{TH}	10^{-9}	**-**					
2	I_{BEI}	10^{-18}	10.4	5.12	6.07	**6.02**		
	N_{EI}	1	1.020	1.0009	1.0093	**1.0093**		
	I_{BEN}	10^{-9}	1	1.55	1.59	**1.59**		
	N_{EN}	1	5	7.327	7.14	**7.14**		
	I_S	10^{-18}	58.6	70.2	73.8	**73.7**		
	N_F	1	1.040	1.0171	1.0213	**1.0214**		
3	I_{BCI}	10^{-18}	58.6	20.9	18.7	**18.8**		
	N_{CI}	1	1.0004	1.0003	1.0000	**1.0000**		
	N_R	1	1.012	1.0032	1.0073	**1.0074**		
4	R_E	1	0.80	0.733	0.646	0.241	0.386	**0.392**
5	R_{CX}	1	0.23	2.48	2.36	1.03	0.903	**0.879**
6	R_{BX}	1	0.75	0.288	0.237	0.958	1.91	**2.51**
	I_{KR}	10^{-3}	5.24	6.03	6.47	6.84	6.79	**6.81**
7	X_{II}	1	6.62	8.48	8.85	8.70	8.72	**8.74**

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Table 4.34. VBIC parameters and their extracted values for the 8x1.6x10.

Step	Param.	x	Initial value	1. iter.	2. iter.	3. iter.	4. iter.	5. iter.
8	I_{KF}	10^{-3}	101.6	110	100	102	102	**102**
	V_{EF}	1	246	190	54.3	76.7	76.1	**76.1**
	R_{CI}	1	4.5	3.69	3.55	5.66	5.63	**5.63**
	V_O	10^{-3}	491	683	688	832	845	**795**
	G_{AMM}	10^{-12}	9.51	6.36	0.564	0.392	0.388	**0.384**
	H_{RCF}	1	0.384	0.522	0.851	0.902	1.15	**1.24**
9	C_{PAD}	10^{-15}	**32.9**					
	C_{JE}	10^{-15}	346		246	232	263	**266**
	C_{JC}	10^{-15}	218		41.8	43.4	50.0	**49.6**
	C_{BEO}	10^{-15}	8.32		24.4	11.8	0.192	**0.282**
	C_{BCO}	10^{-15}	382		189	231	260	**268**
	L_B	10^{-12}	9.50		2.06	2.35	1.08	**0.784**
	L_C	10^{-12}	9.30		3.23	6.65	4.82	**4.19**
	L_E	10^{-12}	11.6		168	113	101	**102**
10	P_E	1	1.22		1.55	1.75	1.77	**1.76**
	M_E	1	0.508		0.969	0.989	0.990	**0.990**
	A_{JE}	10^{-3}	0.106		1.64	16.7	16.4	**16.4**
	P_C	1	0.750		0.429	0.401	0.404	**0.405**
	M_C	1	0.230		0.0172	0.0887	0.0813	**0.0818**
	A_{JC}	10^{-3}	105		0.108	0.100	0.100	**0.100**
	FC	1	0.971		0.977	0.991	0.992	**0.992**
11	T_F	10^{-12}	2.04		3.16	4.51	4.60	**4.57**
	I_{TF}	10^{-3}	43.5		16.4	26.7	27.0	**25.2**
	V_{TF}	1	2.75		4.99	9.39	12.2	**15.29**
	X_{TF}	1	1.60		0.279	0.157	0.165	**0.177**
	Q_{TF}	1	0.676		0.00289	0.000	0.000	**0.000**
	T_D	10^{-12}	0		0.0907	0.321	0.482	**0.463**
12	A_{VC2}	1	16.9		16.8	16.8	17.1	**17.1**
	A_{VC1}	10^{-3}	399		400	236	243	**240**
	R_{BI}	1	26.9		37.3	24.6	22.8	**22.3**

Each step and iteration in Table 4.34 is based on the results obtained in previous steps. After performing *Step 2-8*, these steps were repeated in a second iteration. In

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the second iteration, it was decided to continue into *Step 9*, since some parameters from the next steps influence the DC performance.

The third iteration were started from *Step 2*. After iteration 3 were complete, the results from iteration 2 and iteration 3 were compared. The changes in values for *Step 2* and *Step 3* were very small, therefore there were no need for further iterations of these steps.

The fourth iteration were preformed from *Step 4*.

Only one more iteration had to be performed until the values between consecutive iterations where small enough.

In all the curves presented below, there are solid lines and crosses. The crosses, with colours blue, dark red and dark green, indicate measured values. The solid lines, with colours red, light red and light green, indicate simulated values.

Figure 4.39 shows the forward Gummel plot. The simulated results matches the measured results very well. At the low current end of the base current the measured results have reached the accuracy limit of the measurement equipment. At the low current end of the emitter current, the deviation from a straight line is due to the ≈1 MΩ shunt resistance measured in the DC calibration.

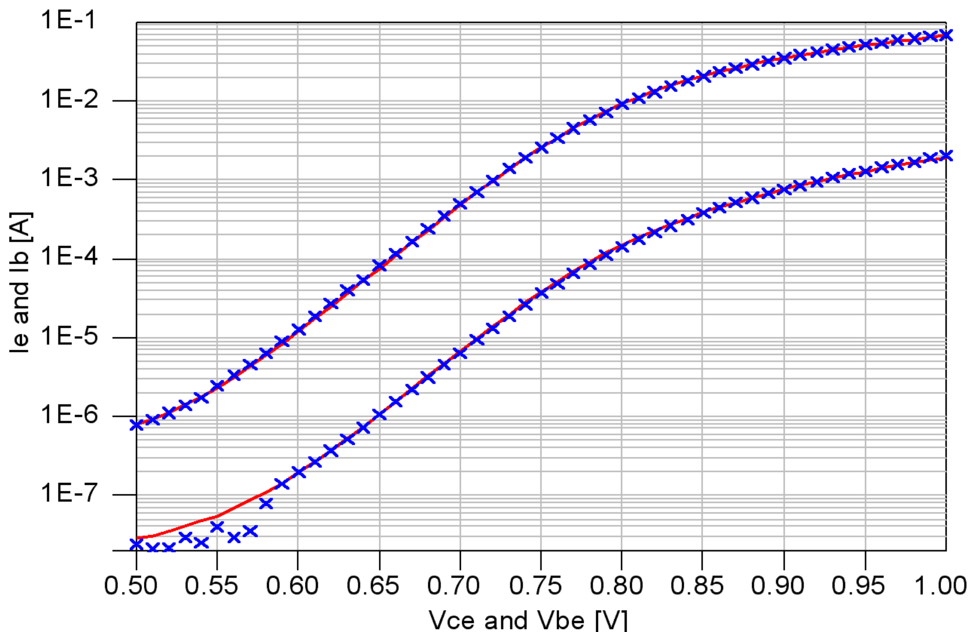

Figure 4.39. Forward Gummel plot.

Figure 4.40 shows the reverse Gummel plot. A slight deviation in the emitter current is observed for medium currents, just as for the single finger transistor, but overall the simulated results matches the measured results quite well. At the low current end of both the emitter and base current, the deviation from a straight line is due to the ≈1 MΩ shunt resistance measured in the DC calibration.

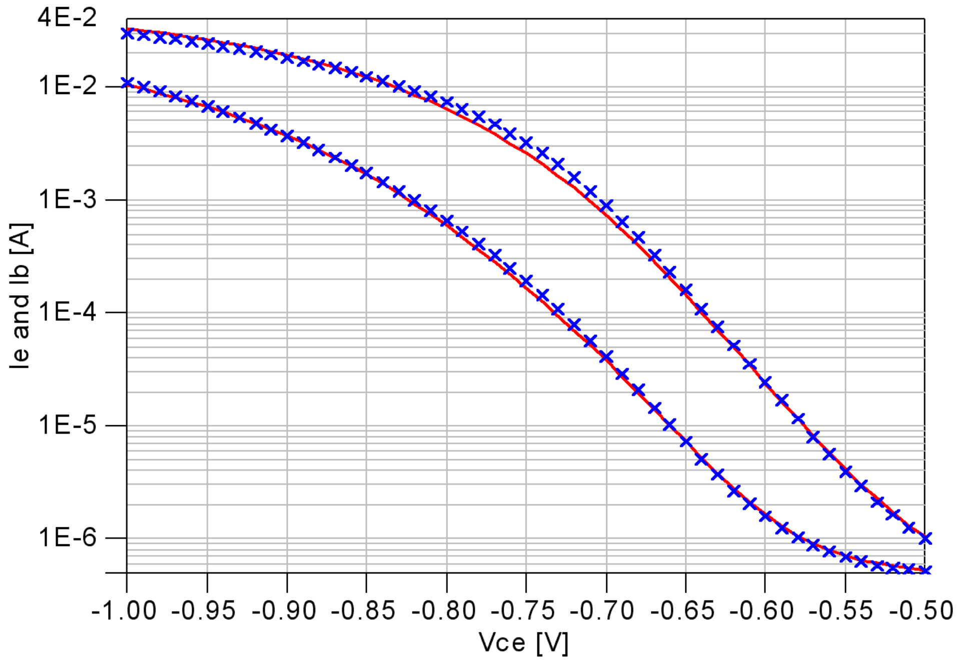

Figure 4.40. Reverse Gummel plot.

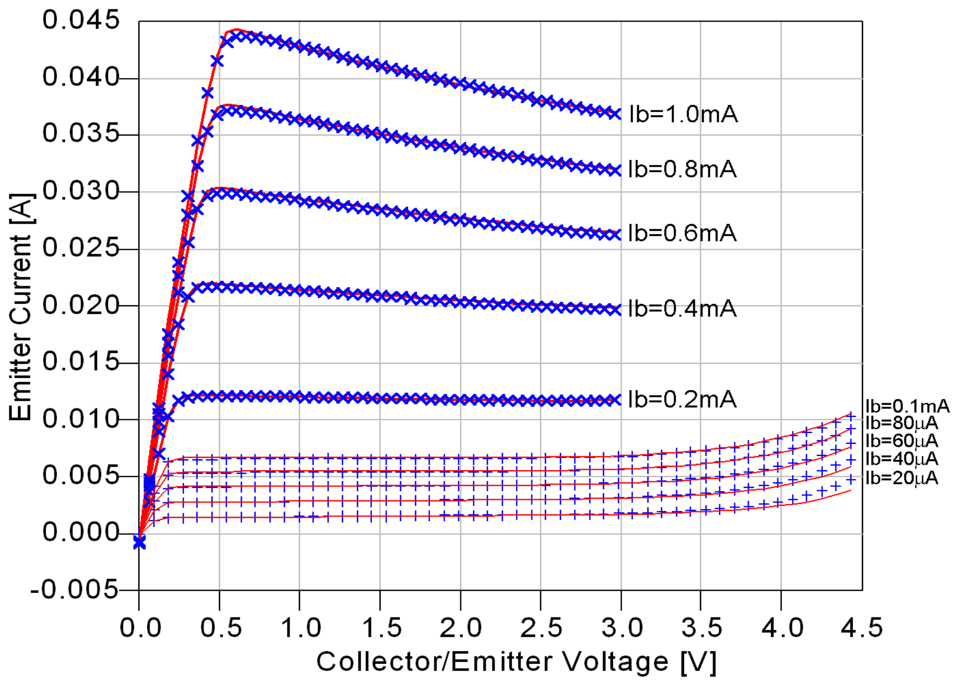

Figure 4.41. I_E versus V_{CE} plot.

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Figure 4.41 shows the emitter current versus the collector-emitter voltage. This figure include the ordinary IV measurement up to V_{CE} = 3 V, and the breakdown IV curves up to V_{CE} = 4.5 V. There are a slight difference between the measured and the simulated emitter current at the highest currents around V_{CE} = 0.5 V. But the error is less than 2.5 %. Overall, the measured values matches the simulated curves very well.

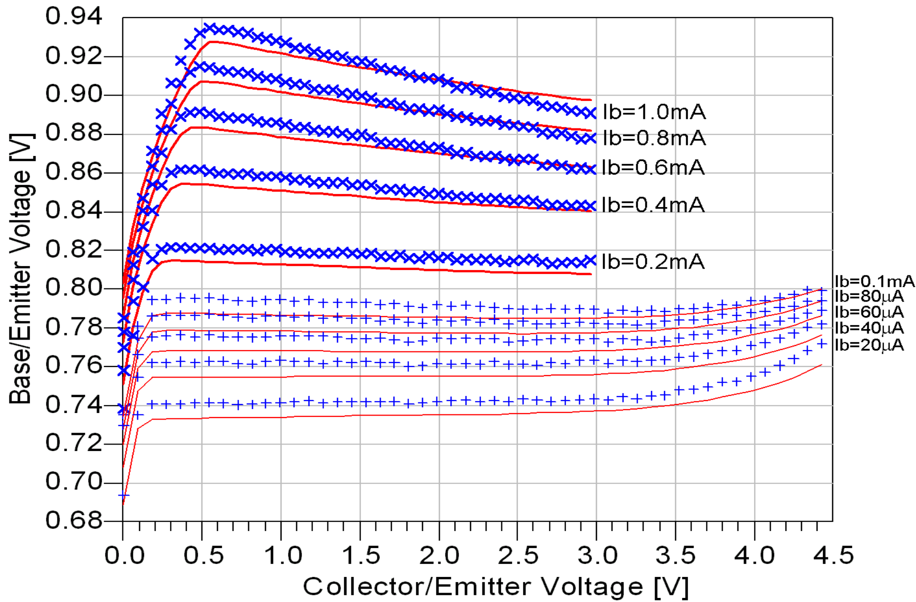

Figure 4.42. V_{BE} versus V_{CE} plot.

Figure 4.42 shows the base-emitter voltage versus the collector-emitter voltage. This figure include the ordinary IV measurement up to V_{CE} = 3 V, and the breakdown IV curves up to V_{CE} = 4.5 V. The simulated values are slightly lower than the measured values. The error is less than 8 mV (1 %). Overall, the measured values matches the simulated curves very well.

Figure 4.43 and Figure 4.44 show the Cold-Capacitor s-parameter measurements. Only every other base voltage listed in Table 4.26 were plotted to reduce over crowding of the figures. The measurements range from V_b = -2.0 V to V_b = 0.4 V.

In Figure 4.43, the red lines and crosses indicates S_{11}, and the green lines and crosses indicates $-S_{22}$. S_{22} is rotated 180 degrees in Figure 4.43 in order to be plotted in the same figure. In Figure 4.44, the red lines and crosses indicates the magnitude of S_{21} in dB, and the green lines and crosses indicates the phase of S_{21} in degrees. The S_{12} was not plotted, due to the fact that it was almost identical to the S_{21}.

There are some amplitude and phase differences, for all the s-parameters. More comments on the deviations will be given later in this section. Overall, the extracted model shows a good match to the Cold-Capacitor measurement.

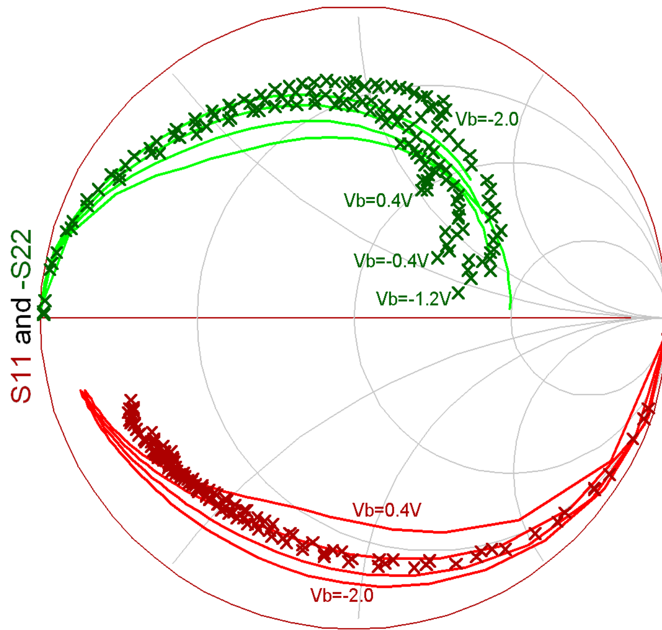

Figure 4.43. Cold Capacitor: S_{11} and $-S_{22}$.

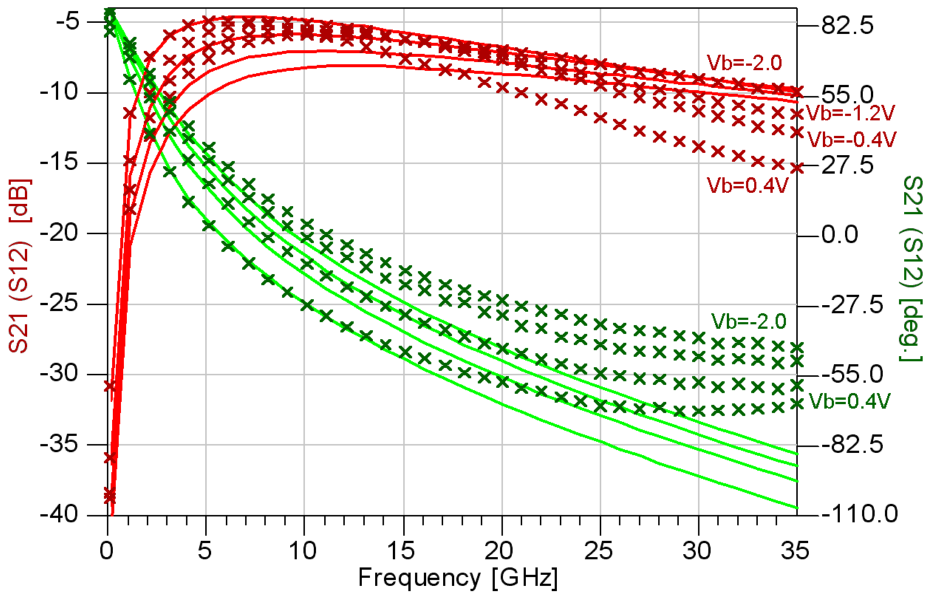

Figure 4.44. Cold Capacitor: S_{21} and S_{12} plot.

Figure 4.45 - 4.47 show the s-parameters for a base current $I_B = 0.16$ mA. Three collector-emitter voltages, $V_{ce} = [1, 2, 3]$ V, are plotted. This covers the lower part of the IV diagram in Figure 4.41.

There are some differences between the measured values and the simulated curves. In S_{11} there is only a small phase error. In S_{22} there is some small errors in both amplitude and phase. In S_{21} the simulated curves have a very small dependence on the applied bias. This causes a maximum amplitude error of 1 dB and a maximum phase error of 8 degrees. In S_{12} the simulated curves also have a very small dependence on the applied bias. This causes a maximum amplitude error of 2 dB and a maximum phase error of 8 degrees. More comments on the deviations will be given later in this section. Overall, the extracted model shows a very good match to the s-parameter measurement.

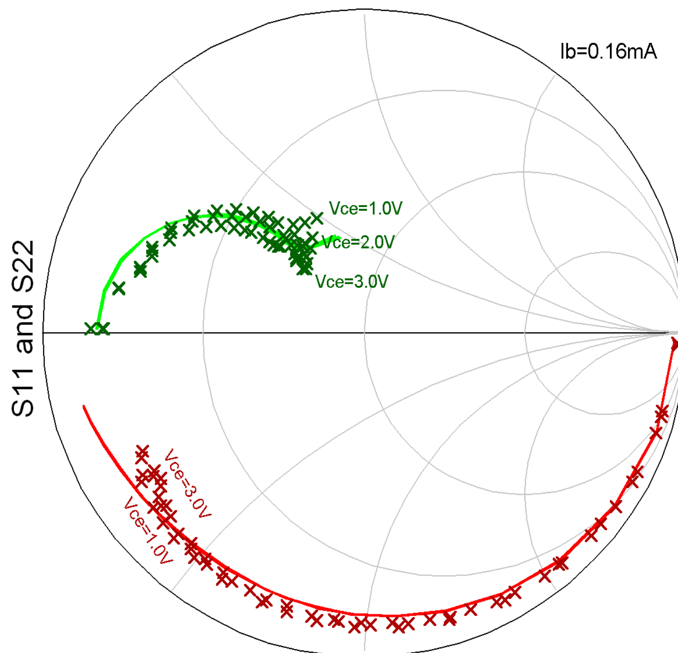

Figure 4.45. Active s-parameters: S_{11} and S_{22} ($I_b = 160$ µA, $V_{ce} = [1,2,3]$ V).

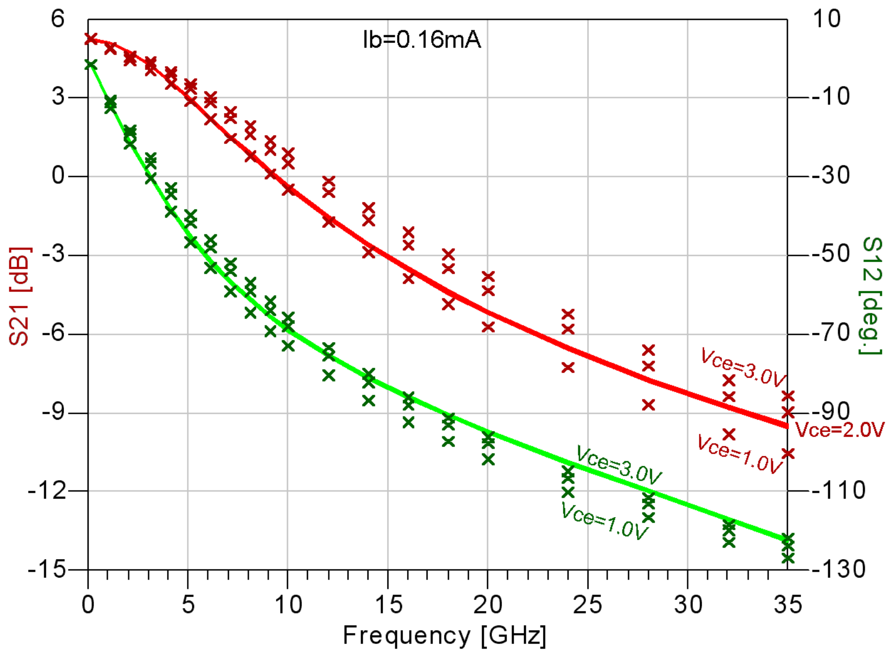

Figure 4.46. Active s-parameters: S_{21} (I_b = 160 µA, V_{ce} = [1,2,3] V).

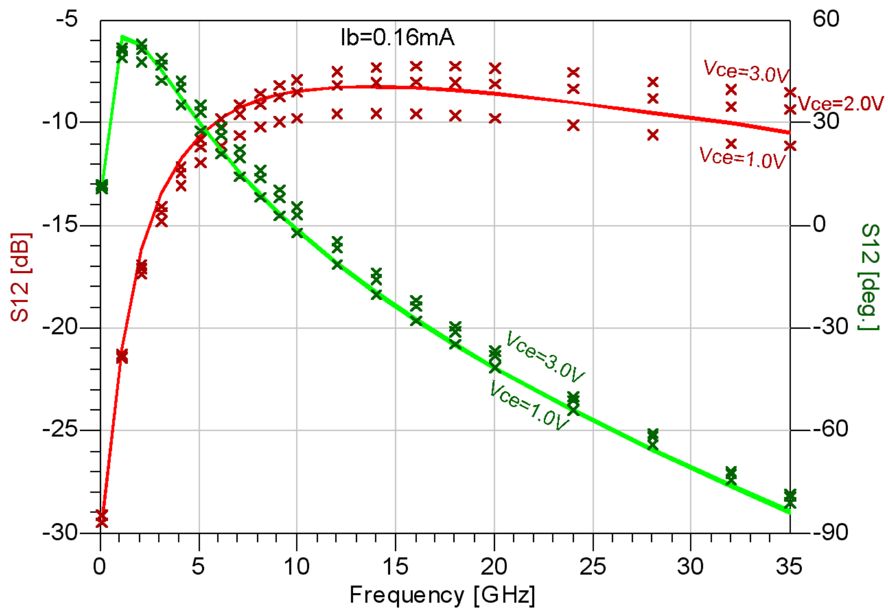

Figure 4.47. Active s-parameters: S_{12} (I_b = 160 µA, V_{ce} = [1,2,3] V).

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Figure 4.48 - 4.50 show the s-parameters for a base current I_B = 1.0 mA. Three collector-emitter voltages, V_{ce} = [1, 2, 3] V, are plotted. This covers the higher part of the IV diagram in Figure 4.41.

There are some differences between the measured values and the simulated curves. In S_{11} there is only a small phase error. In S_{22} there is some small errors in both amplitude and phase. In S_{21} the simulated curves have a very small dependence on the applied bias. This causes a maximum amplitude error of 1.5 dB and a maximum phase error of 12 degrees. In S_{12} the simulated curves also have a very small dependence on the applied bias. This causes a maximum amplitude error of 3.5 dB and a maximum phase error of 10 degrees. More comments on the deviations will be given later in this section. Overall, the extracted model shows a very good match to the s-parameter measurement.

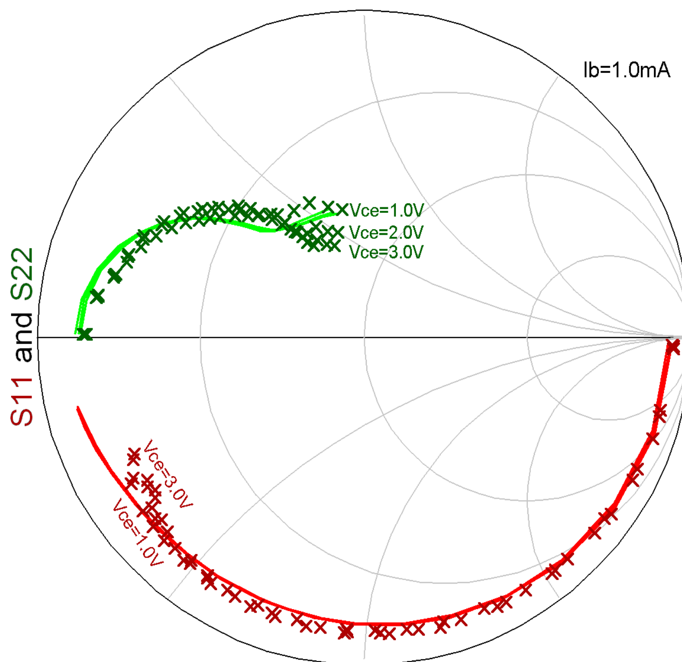

Figure 4.48. Active s-parameters: S_{11} and S_{22} (I_b = 1.0 mA, V_{ce} = [1,2,3] V).

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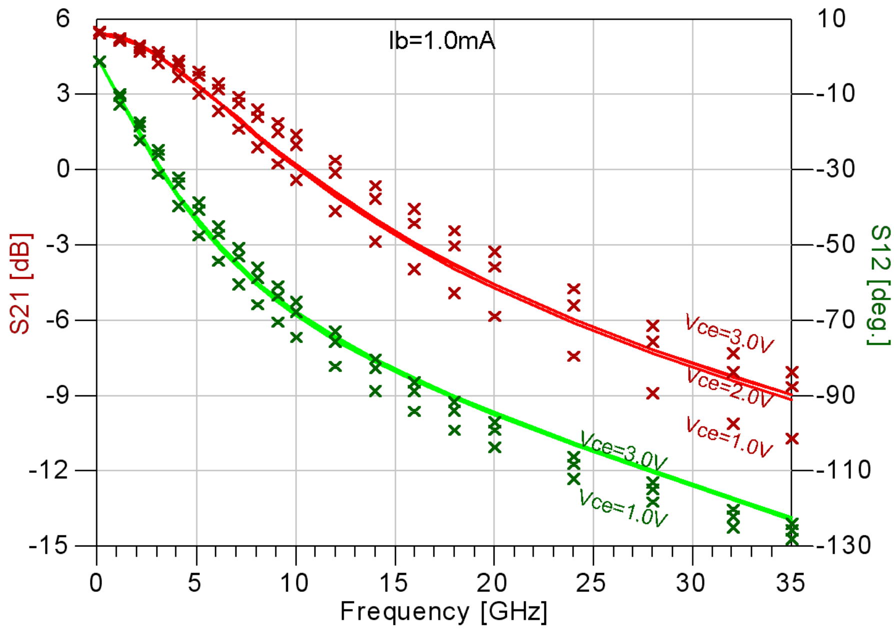

Figure 4.49. Active s-parameters: S_{21} (I_b = 1.0 mA, V_{ce} = [1,2,3] V).

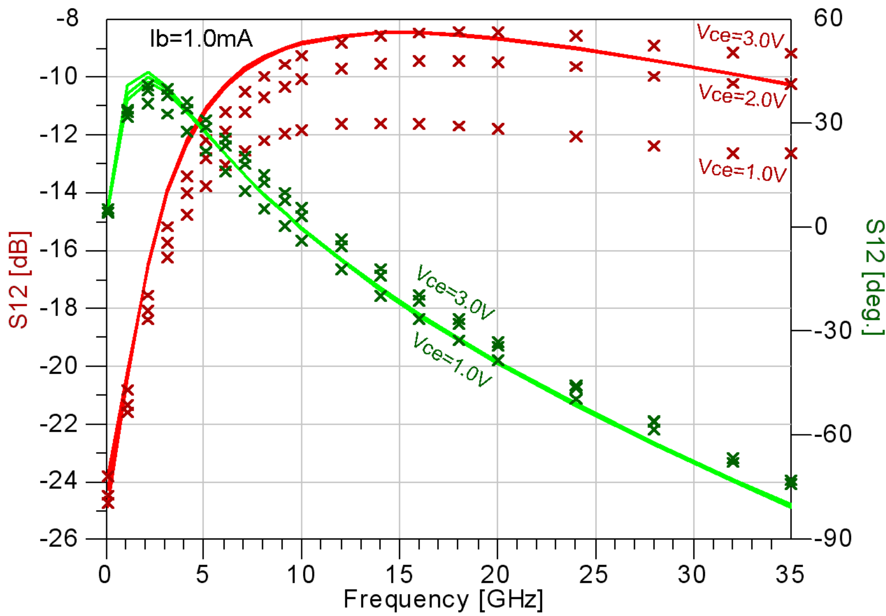

Figure 4.50. Active s-parameters: S_{12} (I_b = 1.0 mA, V_{ce} = [1,2,3] V).

The same four main reasons for the deviations for the single finger transistor, are applicable to this 8-finger transistor.

One of the reason for the very small dependence of the applied bias voltage observed in the Figures 4.46, 4.47, 4.49 and 4.50, is that in parameter extraction the V_{TF} parameter is found to be a very high voltage. This leads to almost no voltage dependence of T_F. The cause of this may be explained from the following. When optimizing in ADS, other errors (described earlier) may cause the overall error in the optimization to increase when V_{TF} is set to lower values. This means that by forcing a high value of V_{TF} the curves matches the measured values better.

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4.6 Conclusion

In this chapter, an overview of the modelling concepts is given. Based on several requirements the VBIC model was chosen for all the practical modelling. An overview of all the parameters associated with VBIC model is given together with an explanation on how to find values for these parameters. From this, a practical parameter extraction method for the VBIC model was developed. This method is the first published practical parameter extraction technique for the VBIC model used on an InGaP/GaAs HBT, as far as the author knows. The method was published by the author in 2000 [6], and can be found in Appendix A.2.

The main features of the extraction method are:

- Only a few common measurements are needed (forward Gummel, reverse Gummel, IV, cold capacitor s-parameter, active s-parameter measurements).
- Easy and practical to use for the circuit designer.
- Good accuracy with only a few iterations.
- No expensive and specialized parameter extraction software is required. The only software needed is a circuit simulator (and MATLAB to get a good set of start values).

The method includes the extraction of the bias dependent forward transit time. The parameter extraction and an evaluation of the transit time implementation in the VBIC model were published by the author in 2001 [7], and can be found in Appendix A.3.

The extraction method was evaluated on a single finger, 1x40, InGaP/GaAs HBT from Caswell Technology. Only four iterations were required to fit the measurements very well. There is less than 1 % error in both the I_C-V_{CE} and V_{BE}-V_{CE} plots in Figure 4.12 and 4.13. At I_c = 20 mA and V_{ce} = [2,3,5] V, S_{21} and S_{12} have the largest error. The maximum magnitude and phase error in the whole frequency range up to 40 GHz are less than 1.5 dB and 15 degrees.

This chapter also includes measurements and modelling of SiGe HBT's. Models for a single finger and a 8-finger transistor were extracted. All the dc characteristics of the modelled transistors have less than 3.5 % error. Some amplitude and phase errors are observed in the s-parameters, especially for the single finger. The errors are caused by uncertainties in the calibration due to a worn calibration substrate, high temperature drift during the measurements, and uncertainties in the physical dimensions/properties caused by lack of information from the foundry. Overall, the extracted models fit the measurements quite well.

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Chapter 5 Power Amplifiers

In the resent years, the focus on power amplifiers has increased significantly, especially in the telecommunication industry, where high production volume, low cost, high performance and small size are important factors.

In this chapter, some of the aspects of designing power amplifiers are discussed. A power amplifier is designed with aid of the thermal estimation technique developed in Chapter 3. The VBIC model for the InGaP/GaAs single finger transistor from Caswell Technology is used as the basic building element.

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5.1 Power Amplifier (PA) Requirements

5.1.1 Linearity and Efficiency

The required linearity and efficiency of a PA depend greatly on the application. The modulation techniques that uses a constant envelope, like FM, PSK and FSK, does not require linear amplification. But, for modulation- and access-techniques that involves QAM, CDMA, OFDM and multi-carrier amplification, the linearity is very important.

There are several different ways to specify and measure the effects of the non-linear behaviour of an amplifier. 3. order intercept point (IP_3), carrier to intermodulation distortion (IMD), spectral regrowth, adjacent channel power ratio (ACPR), noise power ratio (NPR), are some of the different requirements and measurements used.

The efficiency of an amplifier can be specified by the collector (drain) efficiency $\eta = P_{RFo}/P_{DC}$, the overall efficiency $\eta = P_{RFo}/(P_{DC}+P_{RFi})$, or by the most commonly used power added efficiency (PAE) $\eta = (P_{RFo}-P_{RFi})/P_{DC}$.

The efficiency of an amplifier depends on which modulation technique that is used. For modulation techniques involving amplitude variations, the efficiency depends on the average output power. Modulation techniques with high peak to average output power ratio usually have poor average efficiency. The linearity requirements at the peak output power of the amplifier determines the backoff of the amplifier.

Improving the linearity often leads to a higher RF operating power, and indirectly improves the efficiency of a PA.

5.1.2 Linearization Techniques

There are many techniques that can be used to increase the amplifier linearity. Different applications will require different types of linearization techniques. There are three main types of linearization as illustrated in Figure 5.1:

- *Predistortion*:

  Analog predistortion: The basic idea is to design a nonlinear circuit in front of the PA, in such a way that the overall circuit becomes linear. An example is given in [91].

  Digital predistortion: In this technique, a model, usually a simple and short power series of the AM-AM and AM-PM characteristics of the PA, is used to compute a lookup table. The digital input signal is then predistorted by the use of the lookup table. The output of the PA is demodulated and compared to the digital input signal, and used to re-compute the lookup table. An example is given in [92].

- *Feedback*:

  Resistive feedback: A classical technique that is traditionally used mostly at low frequencies. But today, especially in an MMIC design, the resistive feedback is used at RF and microwave frequencies due to higher gain of the transistors.

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Second harmonic injection: The second harmonic at the output of the amplifier is fed back to the input, with correct amplitude and phase. An example is given in [93].

Envelope feedback: The envelope is detected at the input and output of the amplifier and compared. The difference is added to the input with correct amplitude and phase. An example is given in [94].

- *Feed Forward*: In the feed forward technique, a small part of the output signal is subtracted from the input signal and amplified in an error amplifier. The error signal is added to the output signal with correct amplitude and phase. An example is given in [95].

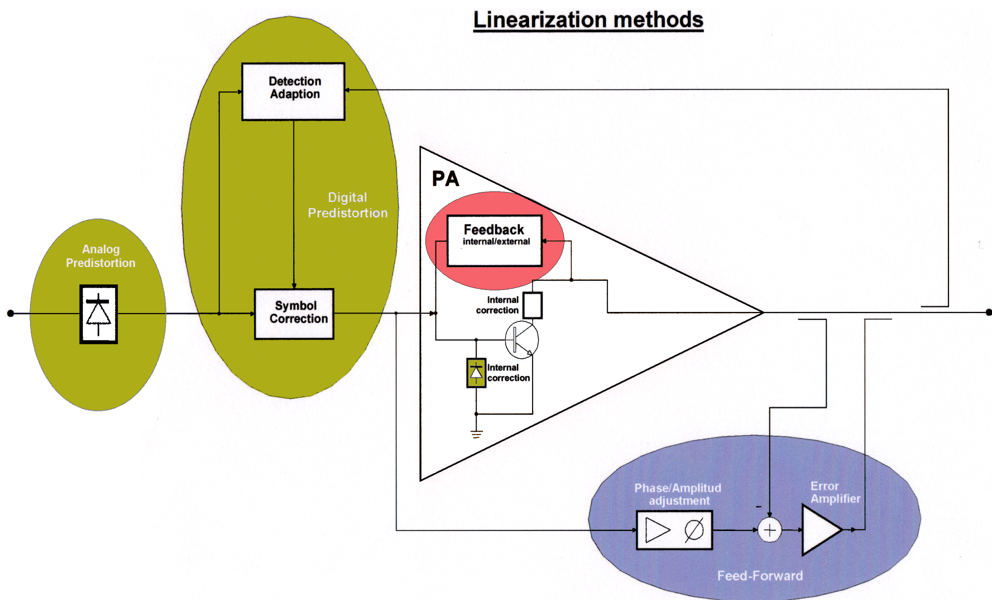

Figure 5.1. Different methods of linearization.

5.1.3 Power Amplifier Types

The most common microwave amplifier types are classified in classes named class A, AB, B, C, E, F and some others. In class A, AB, B and C, the main difference is the biasing of the transistors. In class E and F, the transistor operates as a switch. Some other amplifier structures are known as Kahn, Doherty and Chireix, named after their inventors. Detailed discussion on PA's and classes are given in [96-98].

5.2 Design of an MMIC Power Amplifier

5.2.1 Specifications

The goal here was to design parts of an MMIC power amplifier, using a thermal analysis based on the method developed in Chapter 3, and the electrical model extracted for the InGaP/GaAs process from Caswell Technology, in Chapter 4. The amplifier is not intended for any special application. The specification can therefore be chosen freely. Table 5.1 shows the chosen specifications.

Table 5.1. Power Amplifier specifications.

Property	Specification
Output power P_{out}	> 2 W (33dBm)
Centre frequency f_c	5.0 GHz
Band width within 1dB B	> 10% of f_c
Operating class	A
Operating voltage V_{DC}	5 V
Operating current for each finger $I_{DC,f}$	20 mA

Class A operation has a theoretical efficiency of 50 %. From the specification of the output power, the PA must therefore be able to handle at least a dissipated DC power of 4.0 W. The basic transistor 1x40 can dissipate, on average, a power of 0.1 W. Therefore, at least 40 transistors must be used. 64 transistors should be a sufficient number.

5.2.2 Thermal Design

The temperature increase and the temperature difference between the transistor fingers in a PA design are very important, and should be reduced as much as possible. The thermal coupling between the transistor fingers can be reduce by moving the power dissipating devices as far away from each other as possible. Unfortunately, this increase the area of the chip. The junction temperature can also be reduced by using as much metal as possible in the lines connecting the emitters to the via holes.

The best thermal device in Chapter 3 is the 4-finger P4x40C transistor. Figure 5.2 shows the full layout of the original P4x40C transistor. 16 of these transistors have to be used. There are many possible placements of the 16 transistors. In a power amplifier design, the area of the chip and the size of the power combining network has to be considered. Keeping this in mind, placing the 16 transistors ‘face’ to ‘face’ and ‘back’ to ‘back’ in a row results in a compact and very good thermal layout. The layout of the original P4x40C transistor is changed slightly. Two modified P4x40C transistors are combined into a 8 finger building block, P8x40CM. Figure 5.3 shows the full layout of this building block. Both the P4x40C and the new P8x40CM have ballast resistors connected to the base. More about this in Section 5.2.3.

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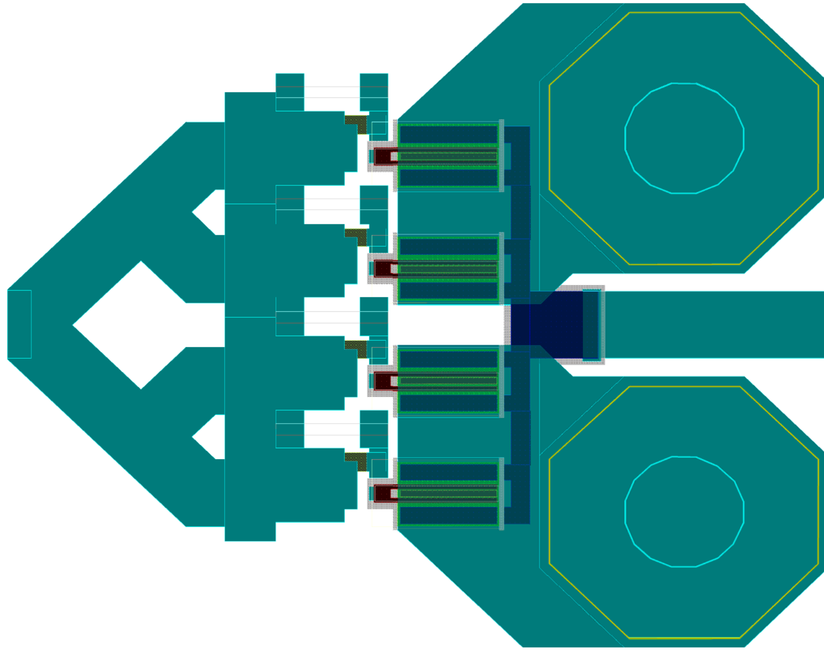

Figure 5.2. The full layout of the original P4x40C.

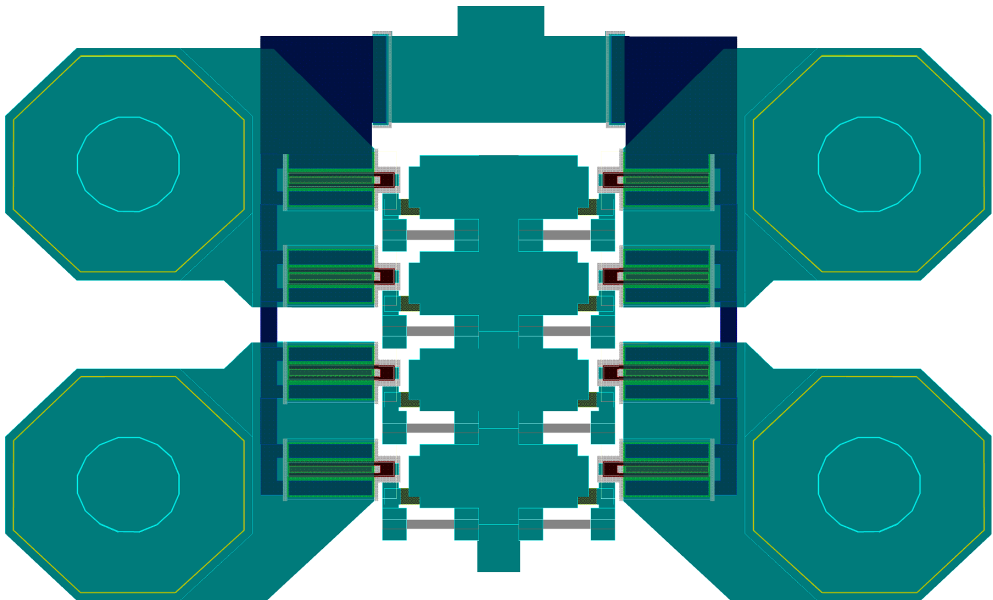

Figure 5.3. The full layout of the P8x40CM

The thermal simulations were carried out at three ambient temperatures, 25 °C, 45 °C and 65 °C. The simulation time, for each ambient temperature, was approximately

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2 hours for the complete power amplifier. This calculation time can easily be reduced by optimizing the MATLAB code, using more symmetry and utilize the fact that some of the image sources placed farthest below the substrate backside can be approximated with point sources. Table 5.2 - 5.4 show the results from *Part A* and *Part B* (Section 3.2.5), in the thermal simulation, for each of the 64 fingers at different ambient temperatures. Each row shows the thermal resistance of the four fingers placed side by side.

The number in brackets indicate the value chosen to be used in the VBIC model. The chosen numbers have the same relative placement inside the estimated interval, as the results in [3, 4] in Section 3.4.6 have to the estimated interval in that section.

Table 5.2. R_{TH} interval of the 64 fingers at 25 °C ambient temperature.

Finger number	*A - B (Selected)*	*A - B (Selected)*	*A - B (Selected)*	*A - B (Selected)*
R_{th} finger 1 - 4	697-939 (866)	744-1008 (923)	744-1008 (923)	697-939 (866)
R_{th} finger 5 - 8	715-966 (891)	763-1036 (954)	763-1036 (954)	715-966 (891)
R_{th} finger 9 - 12	718-970 (894)	766-1041 (959)	766-1041 (959)	718-970 (894)
R_{th} finger 13 - 16	721-973 (897)	769-1043 (961)	769-1043 (961)	721-973 (897)
R_{th} finger 17 - 20	722-976 (900)	770-1046 (963)	770-1046 (963)	722-976 (900)
R_{th} finger 21 - 24	724-977 (901)	772-1047 (965)	772-1047 (965)	724-977 (901)
R_{th} finger 25 - 28	725-978 (902)	773-1048 (966)	773-1048 (966)	725-978 (902)
R_{th} finger 29 - 32	725-978 (902)	773-1049 (966)	773-1049 (966)	725-978 (902)

Table 5.3. R_{TH} interval of the 64 fingers at 45 °C ambient temperature.

	A - B (Selected)	*A - B (Selected)*	*A - B (Selected)*	*A - B (Selected)*
R_{th} finger 1 - 4	744-997 (921)	796-1072 (989)	796-1072 (989)	744-997 (921)
R_{th} finger 5 - 8	765-1027 (948)	817-1103 (1017)	817-1103 (1017)	765-1027 (948)
R_{th} finger 9 - 12	768-1032 (953)	820-1107 (1021)	820-1107 (1021)	768-1032 (953)
R_{th} finger 13 - 16	770-1035 (956)	822-1110 (1024)	822-1110 (1024)	770-1035 (956)
R_{th} finger 17 - 20	772-1037 (958)	824-1113 (1026)	824-1113 (1026)	772-1037 (958)
R_{th} finger 21 - 24	773-1038 (959)	826-1114 (1028)	826-1114 (1028)	773-1038 (959)
R_{th} finger 25 - 28	774-1040 (960)	827-1116 (1029)	827-1116 (1029)	774-1040 (960)
R_{th} finger 29 - 32	775-1040 (961)	827-1116 (1029)	827-1116 (1029)	775-1040 (961)

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Table 5.4. R_{TH} interval of the 64 fingers at 65 °C ambient temperature.

	A - B (Selected)	*A - B (Selected)*	*A - B (Selected)*	*A - B (Selected)*
R_{th} finger 1 - 4	791-1054 (975)	847-1135 (1049)	847-1135 (1049)	791-1054 (975)
R_{th} finger 5 - 8	813-1087 (1005)	869-1168 (1078)	869-1168 (1078)	813-1087 (1005)
R_{th} finger 9 - 12	817-1091 (1009)	873-1173 (1083)	873-1173 (1083)	817-1091 (1009)
R_{th} finger 13 - 16	819-1094 (1012)	876-1176 (1086)	876-1176 (1086)	819-1094 (1012)
R_{th} finger 17 - 20	821-1097 (1014)	878-1178 (1088)	878-1178 (1088)	821-1097 (1014)
R_{th} finger 21 - 24	822-1098 (1015)	879-1180 (1090)	879-1180 (1090)	822-1098 (1015)
R_{th} finger 25 - 28	824-1100 (1017)	880-1181 (1091)	880-1181 (1091)	824-1100 (1017)
R_{th} finger 29 - 32	824-1100 (1017)	880-1181 (1091)	880-1181 (1091)	824-1100 (1017)

The PA is dissipating 6.4 W. At this dissipated power level, in a real device, the backside of the substrate can not be assumed to have the same temperature as the ambient temperature in the room. If the chip is mounted in a package, and the package is connected to a heat sink, the total connecting thermal resistance from the backside to the ambient air will consist of several thermal resistances in series. A practical value of the total connecting thermal resistance may be around 3 K/W. The backside will have a temperature of approximately 20 °C above the ambient air. The results in Table 5.3 will therefore be used for the electrical simulations in the next sections.

At an ambient temperature of 45 °C the PA will have an overall average junction temperature interval of T_j = [79.4, 107]°C (98.6°C). The transistors in the amplifier have a very good layout and thermal shunt, making the junction temperature only change from T_j = [74.4, 99.7]°C (92.1°C) for the transistor with the lowest junction temperature to T_j = [82.7, 112]°C (103°C) for the transistor with the highest junction temperature.

The layout of the eight P8x40CM blocks is shown in Figure 5.4, together with the isothermal and 3D plots. The plots are calculated at an ambient temperature of 45 °C, and with a total dissipated power of 6.4 W. Only half of the isothermal plot is shown. The total length of the transistor row is 2.92 mm.

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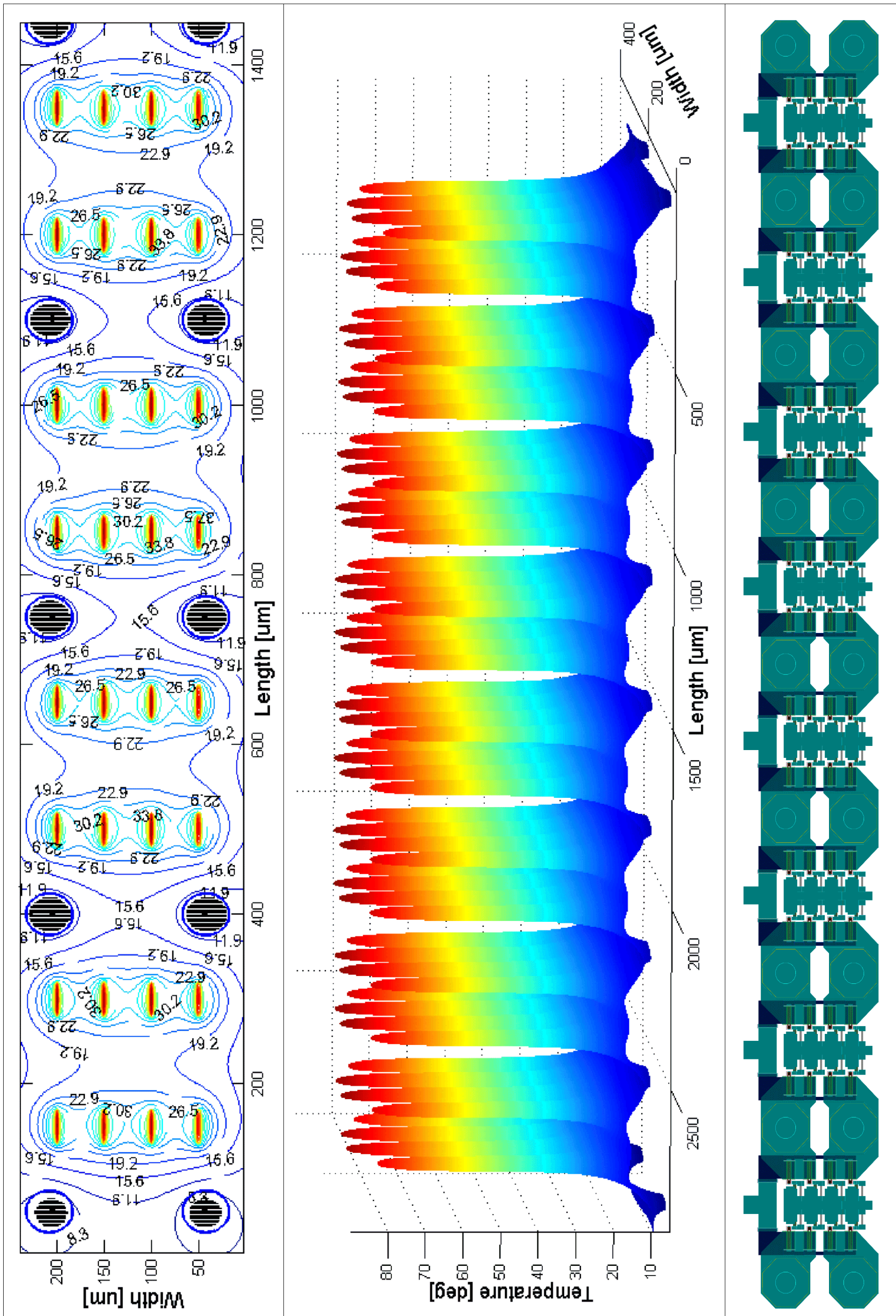

Figure 5.4. Isothermal plot, 3D plot, and the layout of eight P8x40CM blocks.

5.2.3 Electrical Properties of the 8-Finger P8x40CM Block

The 8-finger P8x40CM block is built up of eight single finger VBIC models connected by microstrip lines. Each base is connected to a 1.2 KΩ ballast resistor. The ballast resistor is recommended by Caswell to avoid current collapse in the total circuit at high currents and voltages. A 0.5 pF ‘boot strap’ capacitor is connected in parallel to the ballast resistor. Figure 5.5 shows the schematic diagram, from ADS, over the P8x40CM and the single finger VBIC model. Each finger in Figure 5.5 is assigned a different thermal resistance according to its position in the total amplifier. The values shown are for the P8x40CM block at the end of the transistor row.

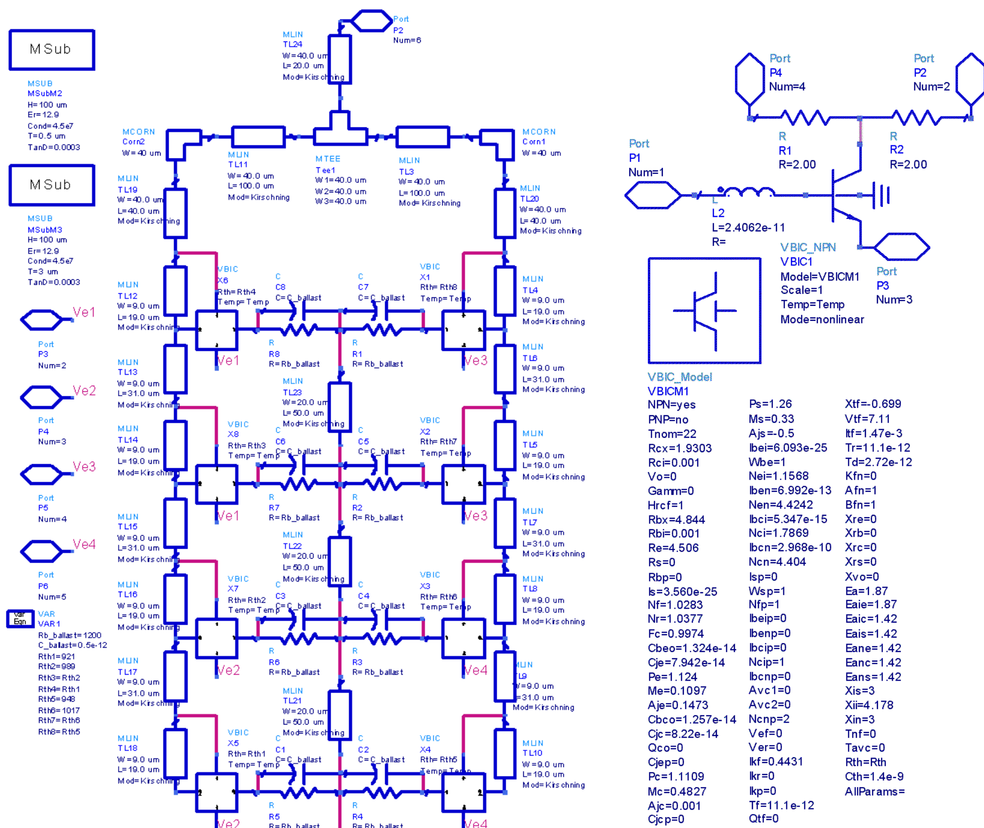

Figure 5.5. The schematic diagram over the P8x40CM and the VBIC transistor.

Figure 5.6 shows S_{11} and S_{22} for the P8x40CM block at V_{DC} = 5 V and I_{DC} = 80 mA. Figure 5.7 shows S_{21} in dB for the P8x40CM block (red curve) and S_{21} for two original P4x40C (blue curve) connected in phase. At high frequencies, a gain increase is observed in the P8x40CM, making it more broadband. This is due to the phasing of each finger in the P8x40CM. At very high frequencies the P8x40CM starts looking more like a travelling wave amplifier.

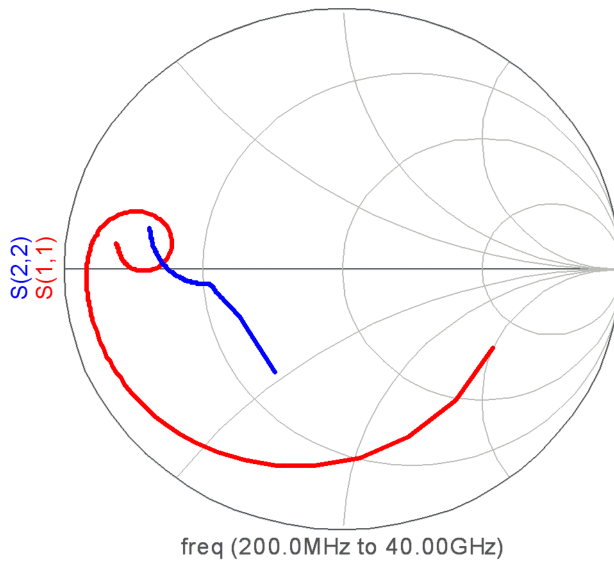

Figure 5.6. S_{11} and S_{22} for the P8x40CM block.

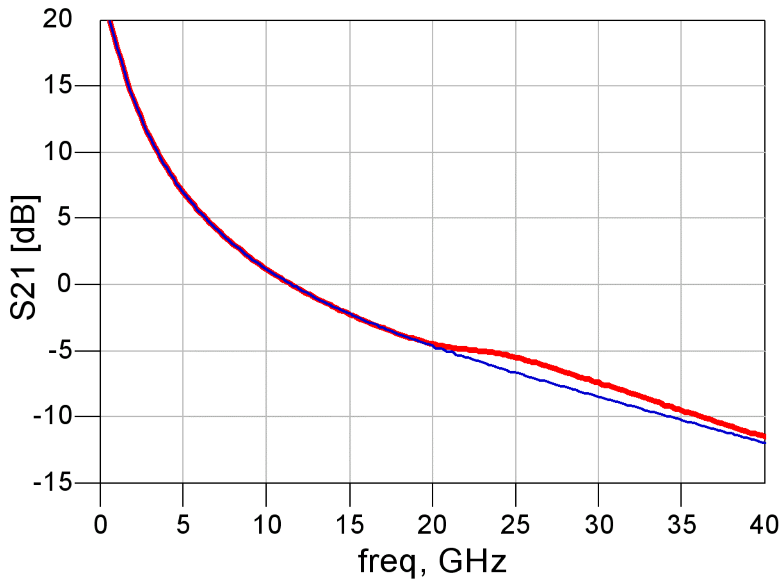

Figure 5.7. S_{21} for the P8x40CM block (red) and two P4x40C (blue).

5.2.4 The Combined Power Amplifier

The input and output of the P8x40CM block has to be combined. A 'bus-bar' power combinder is chosen for this task. The design of the 'bus-bar' follows the procedure outlined in [101]. The 'bus-bar' has many attractive properties. It is compact, it makes DC connection to all the devices very easy and it shorts out all odd modes of possible oscillations.

In a complete analysis of a 'bus-bar', a full 2.5D analysis should be performed. The design here is only based on transmission lines in ADS. Figure 5.8 shows a basic 'bus-bar' block. Several blocks can be connected together to build up a full power combinder.

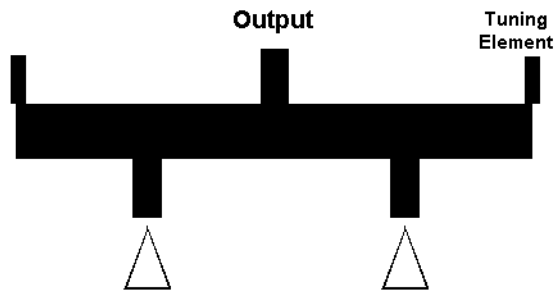

Figure 5.8. Basic 'bus bar' building block.

It was not necessary to use the tuning elements in the 'bus-bar' designed here. The network connecting the outputs of the 'bus-bar' blocks are optimized in ADS to achieve maximum gain in the power amplifier. The output network is designed using series inductances (microstrip lines) and shunt capacitances at the connection points.

A 'bus-bar' is also used to design the input network. The complete layout of the power amplifier is 2.92 mm wide and 1.11 mm long. This layout does not include the bias network and the bond/probe pads. Ideal bias networks are used in the simulation of the power amplifier. Figure 5.9 shows the layout of the complete power amplifier.

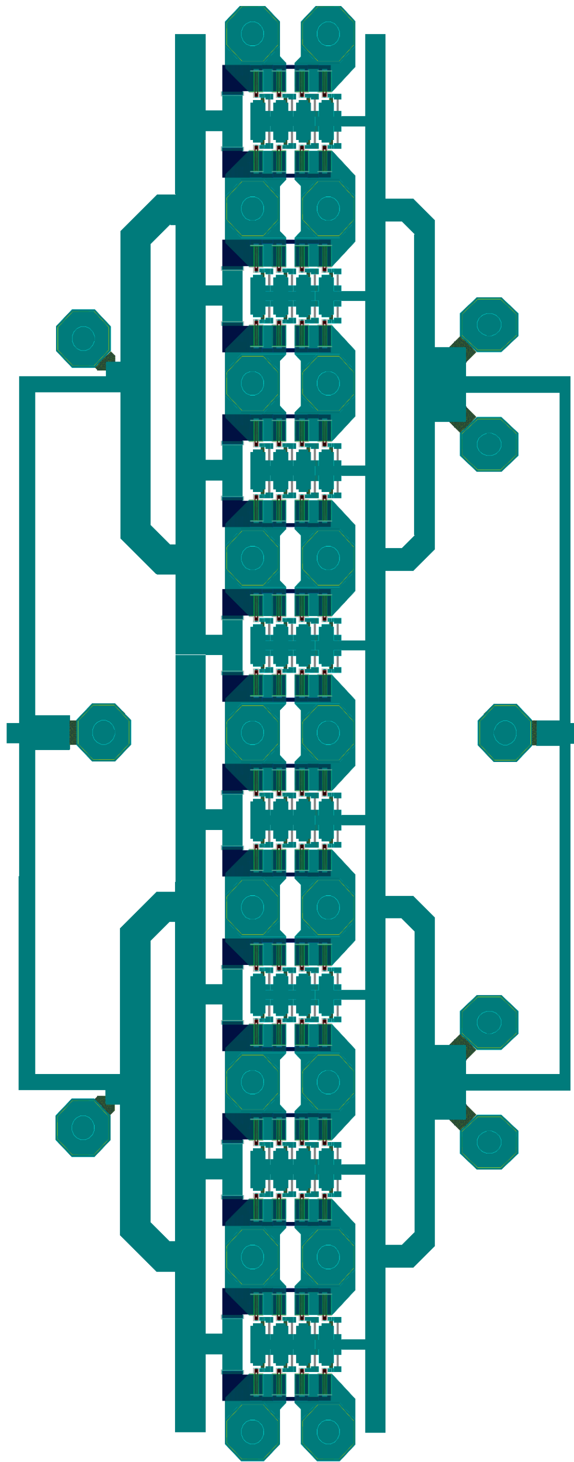

Figure 5.9. The complete layout of the amplifier.

5.2.5 Results of the Combined Power Amplifier

Figure 5.8 shows the IV curves of the combined PA. The marker m1 indicate the chosen bias point, V_{DC} = 5.0 V, I_{DC} = 1.28 A. All the following figures are measures at this chosen bias point.

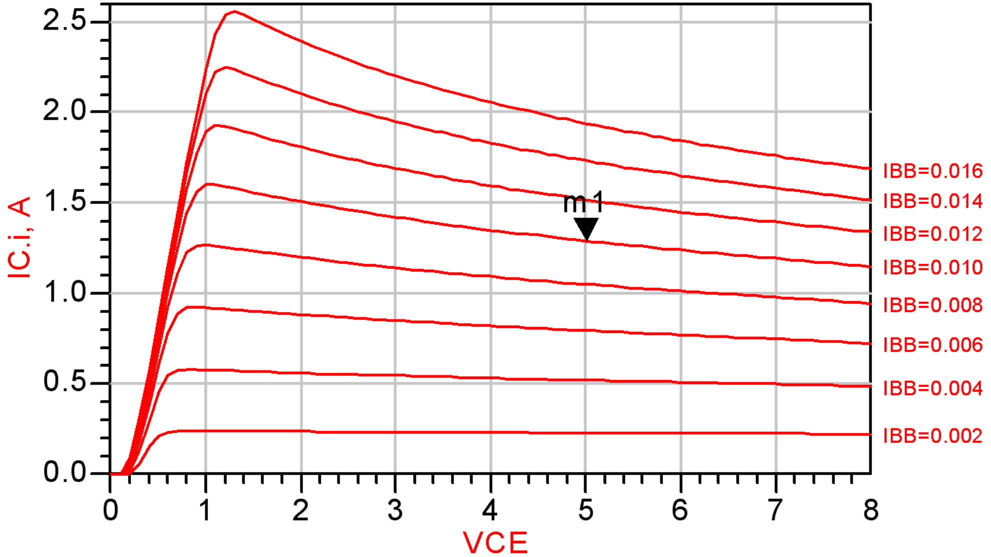

Figure 5.10. IV curves of the complete power amplifier.

Figure 5.11 - 5.14 show the small signal s-parameters for the chosen bias point.

In Figure 5.15 the stability factor K and the source/load stability circles are shown. K>1 for all frequencies above 100 MHz, which indicate that the amplifier is unconditional stable. This is also shown by the stability circles, which are completely outside or cover the entire Smith diagram. For frequencies below 100 MHz, the real bias circuits must be included in the simulations in order to evaluate the stability. This has not been done.

Figure 5.16 and 5.17 show the AM-AM and the AM-PM transfer characteristics. A ‘glitch’ is observed in these figures (and in some of the figures later) at high gain compression. This is probably due to some simulator artifacts, and may not be observed in a measured device.

The power added efficiency (PAE) is shown in Figure 5.18.

Figure 5.19 shows the power in the fundamental frequency and the harmonics up to a order of 5.

Figure 5.20 and 5.21 show the third and fifth order intermodulation distortion.

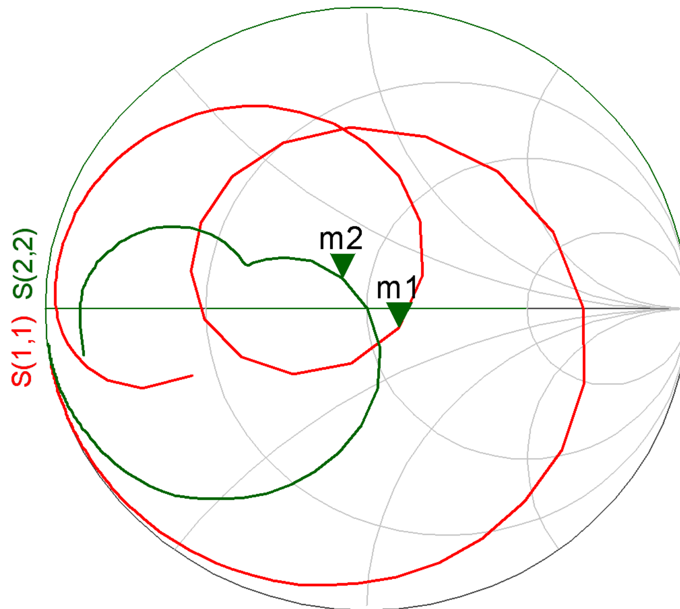

Figure 5.11. S_{11} and S_{22} at the chosen bias point.

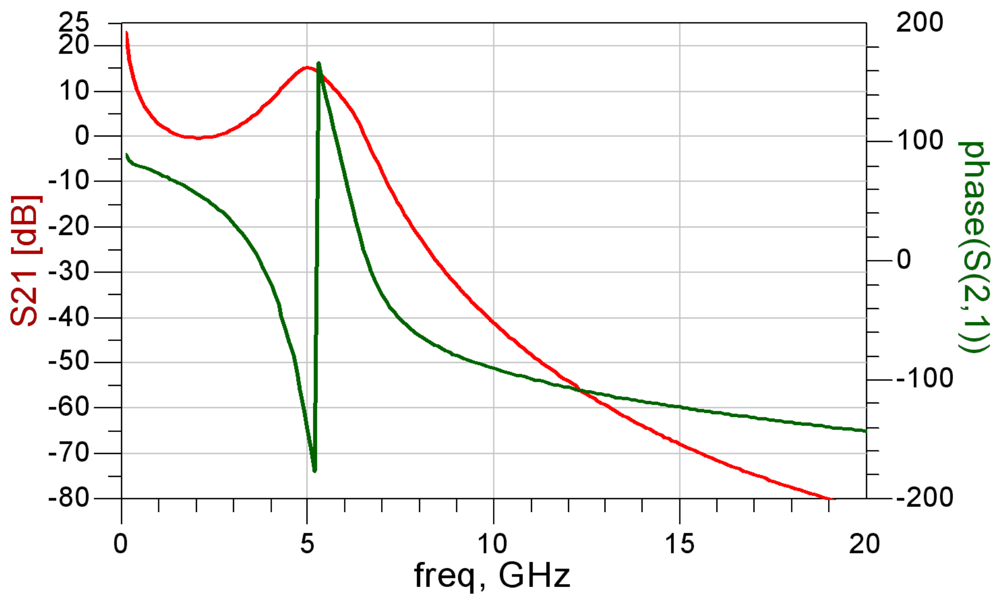

Figure 5.12. S_{21} at the chosen bias point.

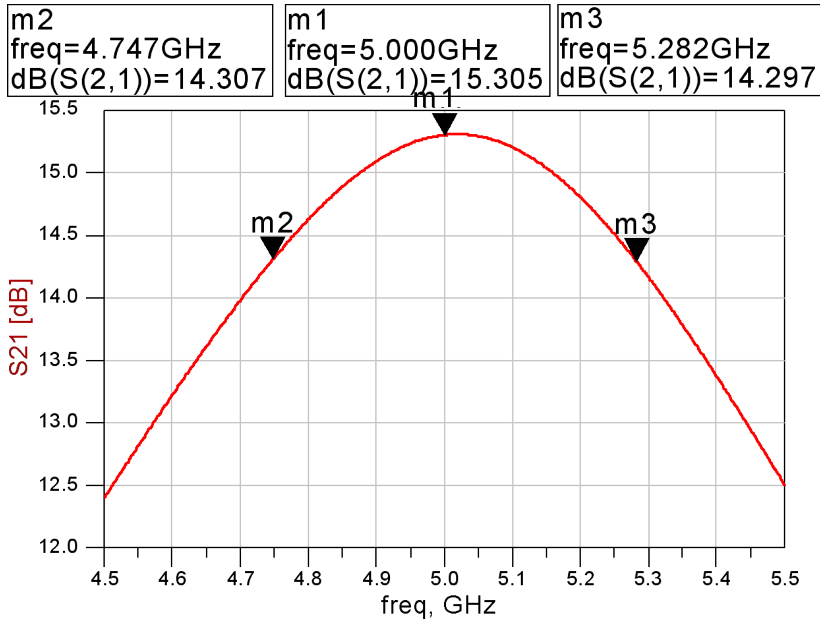

Figure 5.13. Detailed view of S_{21} at the chosen bias point.

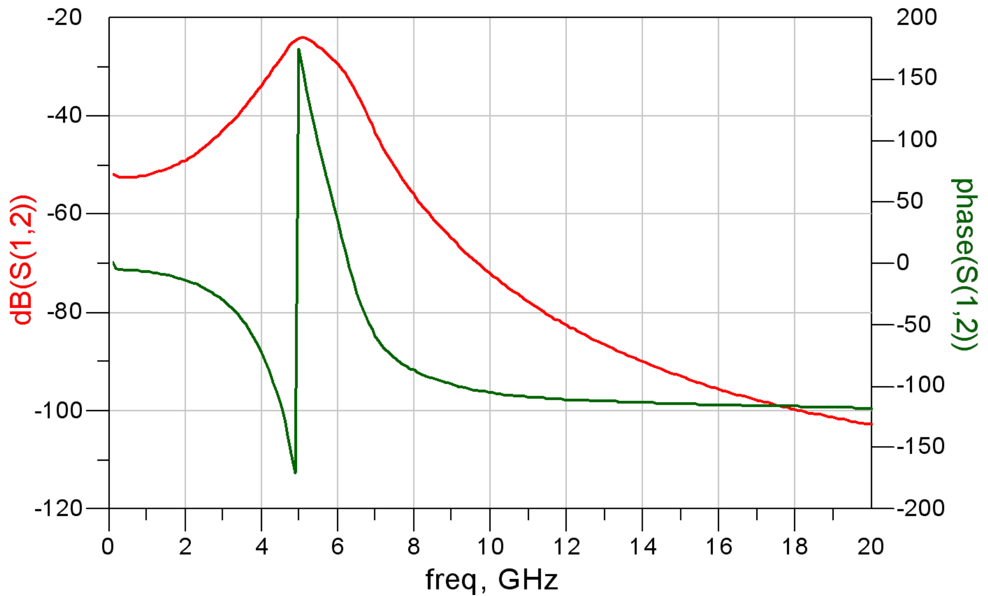

Figure 5.14. S_{12} at the chosen bias point.

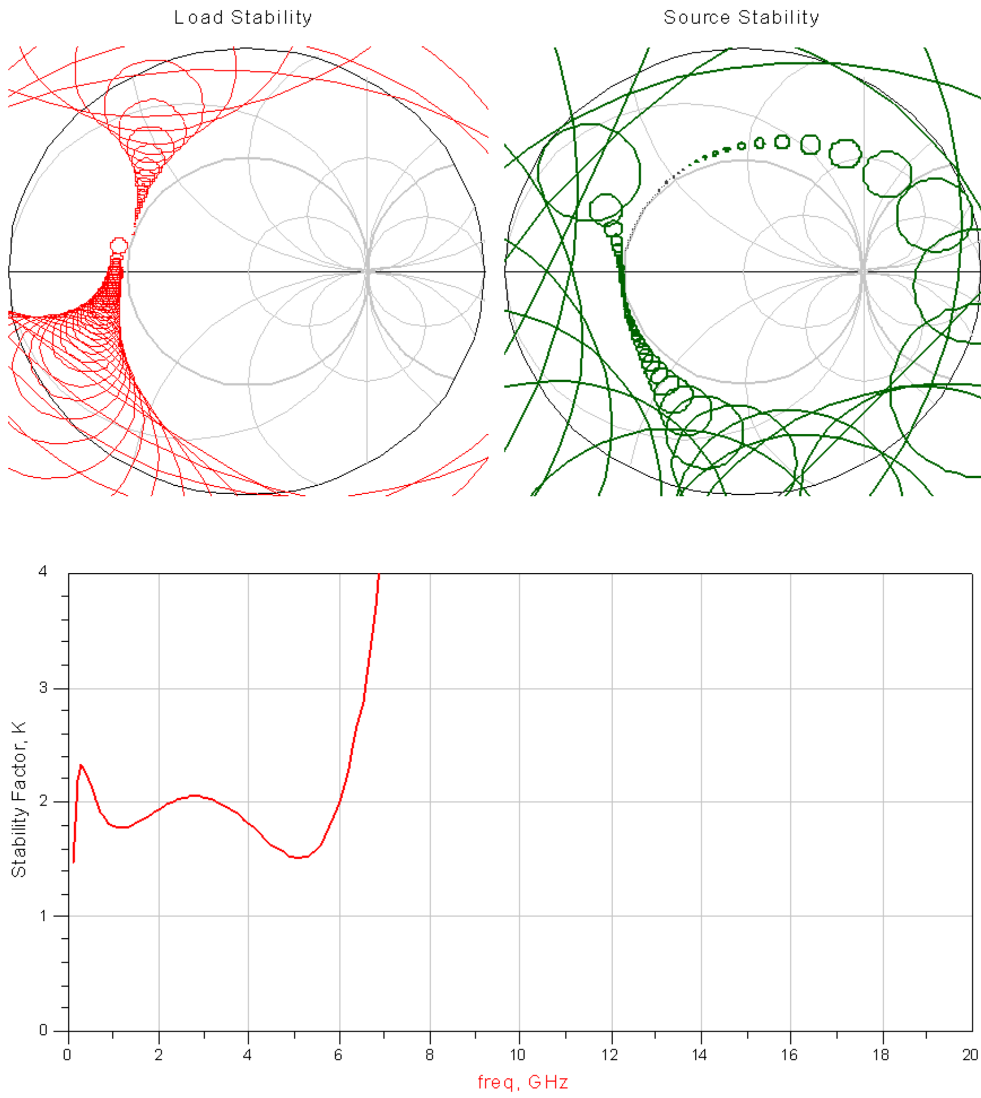

Figure 5.15. Stability factor K, load and source stability circles.

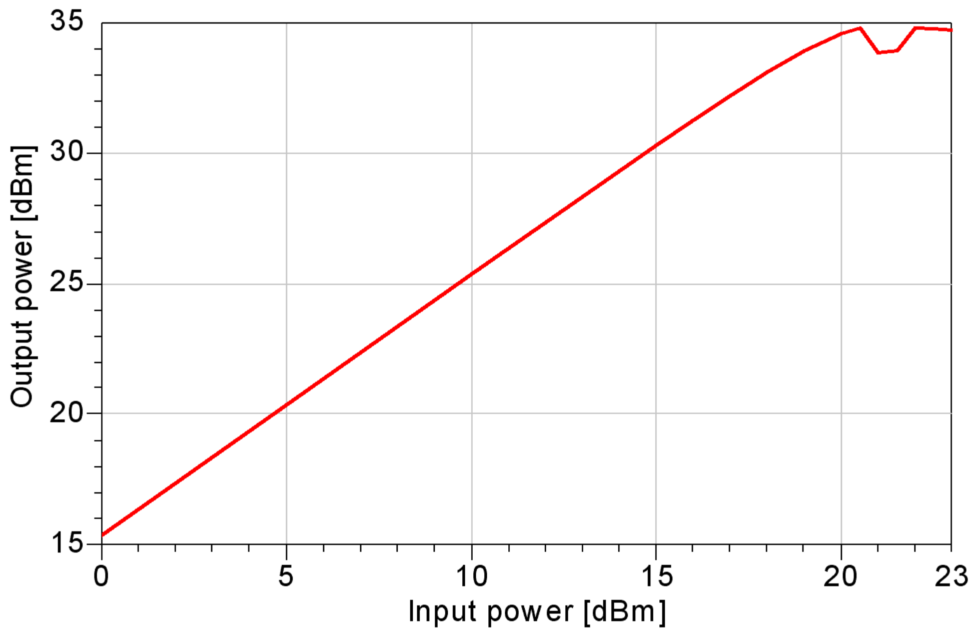

Figure 5.16. AM-AM transfer characteristic.

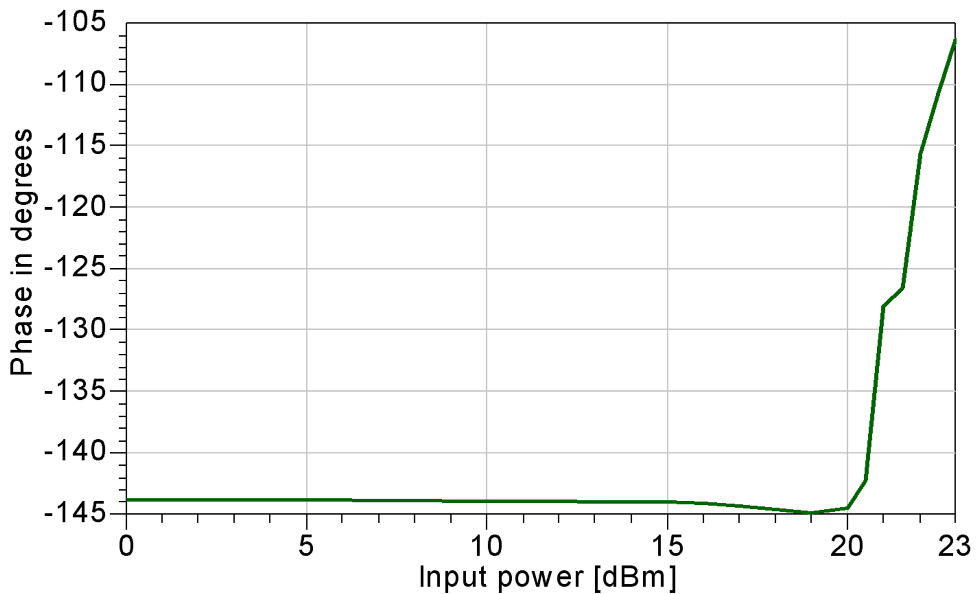

Figure 5.17. AM-PM transfer characteristic.

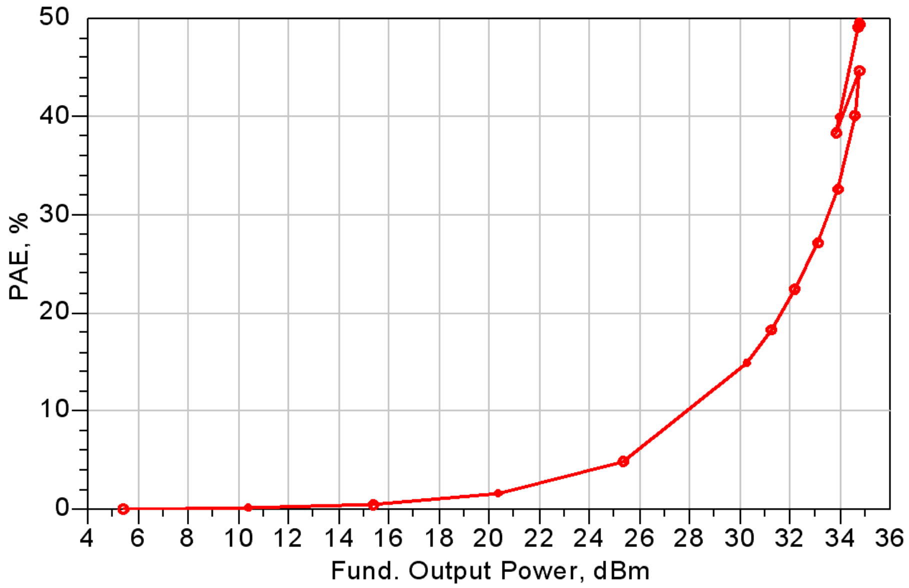

Figure 5.18. Power added efficiency.

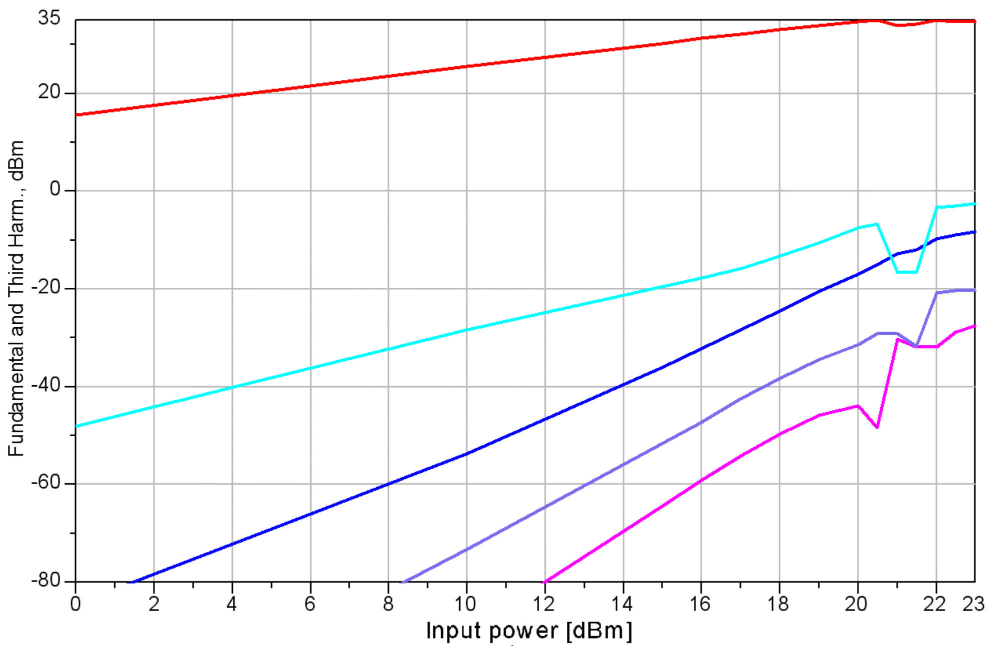

Figure 5.19. Fundamental and harmonic frequencies.

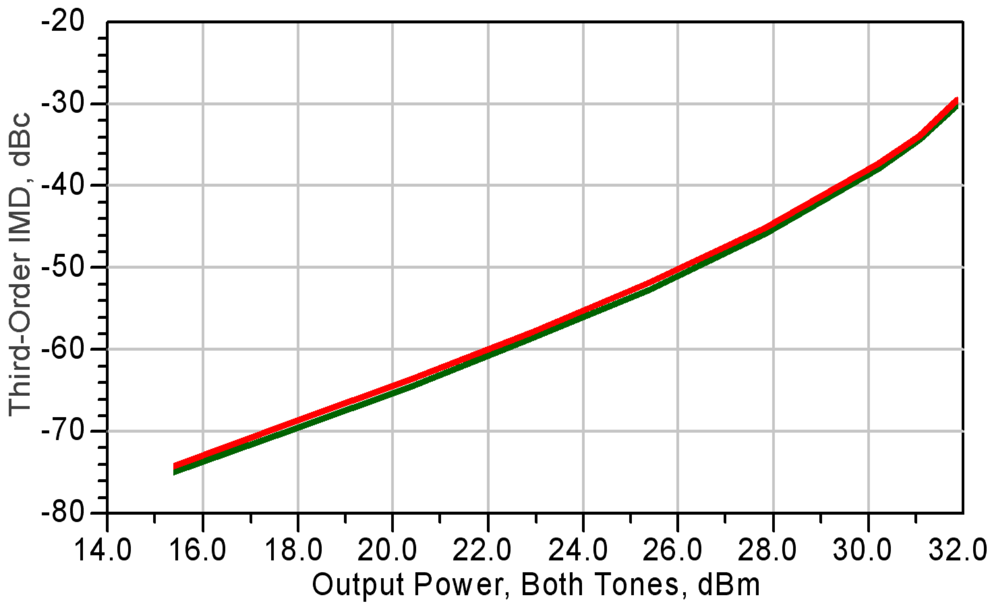

Figure 5.20. Third order intermodulation distortion.

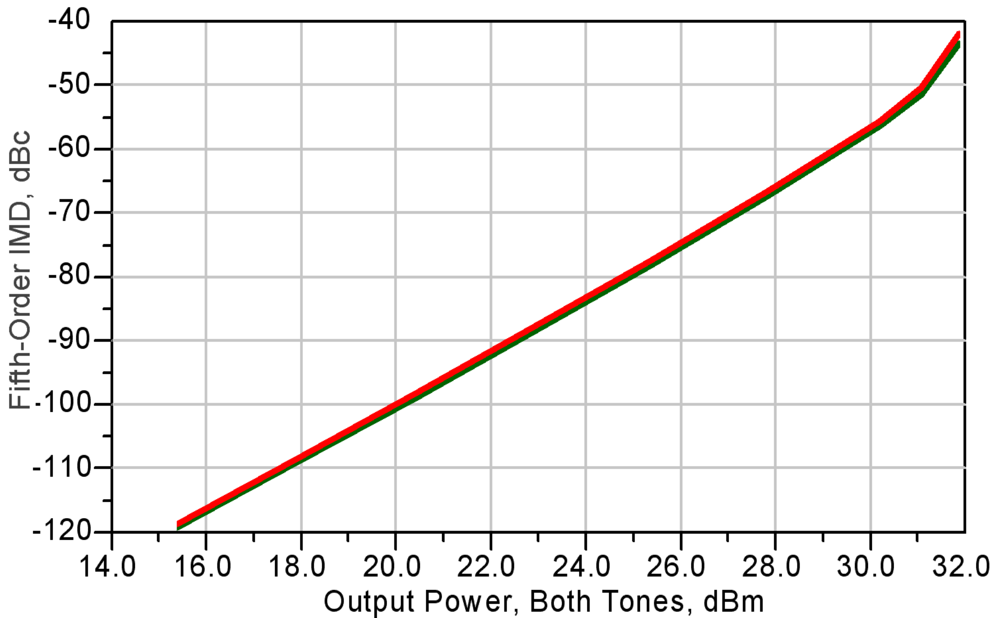

Figure 5.21. Fifth order intermodulation distortion.

Table 5.2 summarize the most important results of the power amplifier.

Table 5.5. Power amplifier results.

Property	Results
Maximum output power P_{out}	2.88 W (34.8 dBm)
Band width within 1dB B	535 MHz (10.7 %)
Transducer Power Gain at centre frequency G	15.3 dB
1 dB compression point P_{1dB}	34.5 dBm
Third order intercept point TOI	49.9 dBm
PAE at 33 dBm	27.2 %
Gain compression at 33 dBm	0.285 dB
Phase error at 33 dBm	-0.728 degrees
Second harmonics at 33 dBm	-46.6 dBc
Third harmonics at 33 dBm	-57.6 dBc
Fourth harmonics at 33 dBm	-71.4 dBc
Fifth harmonics at 33 dBm	-82.8 dBc
Third order intermodulation distortion IMD_3 at 31.9 dBm	-30.1 dBc
Fifth order intermodulation distortion IMD_5 at 31.9 dBm	-43.6 dBc
Stability K	> 1 for [0.1,20] GHz

5.3 Conclusion

In this chapter a very linear class A power amplifier has been designed using the InGaP/GaAs HBT's from Caswell technology. The thermal junction estimation technique developed in Chapter 3 has been used to make a very good thermal layout of the power amplifier. The estimated average junction temperature is 98.6 °C above the ambient temperature, calculated with a total dissipated power of 6.4 W at an ambient temperature of 45 °C. The maximum junction temperature difference between the transistor fingers is less than 11 °C.

The estimated thermal resistance of each finger was used in the VBIC model extracted in Chapter 4.

The PA was constructed with a 'bus bar' power combinder at both input and output, and optimized for maximum gain with a 10 % bandwidth. The PA had a small signal transducer power gain of 15.3 dB and a maximum output power of 34.8 dBm. The 1 dB compression point was simulated to be 34.5 dBm, and the third order intercept point was 49.9 dBm. At 33 dBm output power the PAE was 27.2 %, the gain compression was 0.285 dB and the phase error -0.728 degrees. The PA was unconditionally stable for all frequencies above 100 MHz.

The bias circuits must be included for a complete stability analysis at low frequencies. In a complete stability analysis of a PA, the 'bus bar' should be analysed in a 2.5D simulator. This has not been performed here.

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Chapter 6 Conclusion

The main focus in this thesis have been to address the key problems encountered at circuit level when designing MMIC power amplifiers. Two of the main problems are thermal design issues and the modelling of the non-linear transistors. These problems have been addressed in Chapter 3 and Chapter 4.

A new practical technique for estimating the junction temperature and thermal resistance of an HBT has been developed in Chapter 3. This technique was published by the author in 2002 [5], and can be found in Appendix A.1. The new technique estimates an interval for the junction temperature and the thermal resistance, from a few physical properties and the layout of the transistors. The new technique has good accuracy and short simulation time in a mathematical program like MATLAB.

A practical parameter extraction method for the VBIC model, used on an InGaP/GaAs HBT, was developed in Chapter 4. The method was published by the author in 2000 [6], and can be found in Appendix A.2. Only a few common measurements are needed to extract parameters with good accuracy for the model. The only software needed is a circuit simulator. The parameter extraction and an evaluation of the implementation of the bias dependent forward transit time in the VBIC model were published by the author in 2001 [7], and can be found in Appendix A.3.

Both techniques developed in Chapter 3 and Chapter 4, have been applied to several InGaP/GaAs HBT's from Caswell Technology. The results of this have been compared to results given in [3, 4] and to measurements provided by Caswell Technology, and correspond very well with these.

In Chapter 5 a very linear class A MMIC power amplifier has been designed using the thermal junction estimation technique developed in Chapter 3 and the parameter extraction method for the VBIC model developed in Chapter 4. The power amplifier has a very good thermal layout. The power amplifier was constructed with a 'bus bar' power combinder at both input and output.

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6.1 Future works

In this section some of the possibilities for further research are presented.

- The thermal properties of transistors and amplifiers, are very important. Measurements of electrical properties at different temperatures are necessary to completely characterize transistors and amplifiers. A prototype of a temperature controlled chuck, named 'Chuck Berry', for the Cascade probe station has been made. A paper describing 'Chuck Berry' has been proposed [102], and can be found in Appendix A.4. Further testing and development of 'Chuck Berry' should be performed.
- The possibility of using the Kirchoffs transformation [39] in the technique for estimating the junction temperature, may be investigated. This should result in an improved technique that produces a single result, and not an interval for the junction temperature.
- In the last year, the Department of telecommunication, NTNU, and TriQuint Semiconductor, Inc. signed an agreement for MMIC prototyping. This agreement include TriQuint's InGaP/GaAs HBT's. Using 'Chuck Berry', new models for this process should be made to include all of the temperature parameters in the VBIC model
- The power amplifier partly designed in Chapter 5 can be produced and tested. For comparison, a power amplifier with a bad thermal layout should also be produced and investigated.
- A complete program for making thermal layouts and calculating the thermal properties, should be made in order to simplify good design of power amplifiers.

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APPENDIX A Published papers:

1. M. Olavsbråten, ”A Simple Practical Technique for Estimating the Junction Temperature and the Thermal Resistance of a GaAs HBT”, *2002 IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1005-1008, Seattle 2002

2. M. Olavsbråten, “ A Practical Method of Parameter Extraction for the VBIC Model used on a GaAs HBT”, *GAAS 2000 Conference Proceedings*, pp. 56-59, Paris 2000

3. M. Olavsbråten, “Parameter Extraction and Evaluation of the Bias Dependence of Tf, for the VBIC Model used on a GaAs HBT”, *GAAS 2001 Conference Proceedings*, pp. 315-318, London 2001

4. M. Olavsbråten, L. Indresæter, “A Low Cost Temperature-Controlled Chuck for a Cascade Probestation”, *Proposed for the 2003 IEEE MTT-S International Microwave Symposium*