

Multilevel Power Electronic Converters for Electrical Motor Drives

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I PREFACE

All my life I've been fond of technical gadgetry. Why they work, and often after disassembling, why they DON'T.

My first amazement to power electronics, actually without knowing it, was when I bought my first electronic speed controller for my radio-controlled electrical model car (one of many). Right out of the box the car was equipped with a simple speed controller made out of resistors. They got very hot, and the battery went flat all too early. After buying a new electronic speed controller, the car was controlled smoothly, the controller was cold, and my batteries lasted longer. What an invention! Years later, after attending the university, I discovered that the new electronic speed controller was a simple Buck-converter.

After taking power electronics classes at the university, I was hooked on the topic. Controlling large amount of power by electronics, without almost any losses. It was clear, I wanted to work with power electronics.

For my Master's thesis, I was fortunate to do my work at University of Madison, Wisconsin under the supervision of Professor T. A. Lipo at Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). At WEMPEC I met M. D. Manjrekar, who at that time was a Ph.D. student at the university. He introduced me to multilevel power conversion, and for 6 months I worked with him on the topic. The interest grew, and as I was offered a Ph.D. student position at NTNU, I was very sure that I wanted to work with multilevel converters. The unique mixture of power electronics and environment at WEMPEC brought me back for a few months during spring 2002.

There are many I would like to thank through all these years. First, I would like to thank my advisor Prof. Roy Nilsen for his support over the years, and for his belief in me. Second, I would like to thank all the colleagues at Department of Electrical Power Engineering, NTNU, for their help and support. Two students gave valuable help in the project, and should be noted, a big thanks to Jonas Beverfjord and Christian Dick. A special note of thanks to my colleague Sigurd Øvrebø. For 10 years now, he has been a very good friend and discussion partner. During the last stressful months, Sigurd has been a stable shoulder to cry and laugh on. Thanks again, Sigurd. I owe my family big thanks for their constant support and encouragement, particularly my uncle, Per, for reading through this manuscript. Last but not least I pay gratitude to Lill-Mari for reminding that there are more things in life than power electronics.

Again, thank you all!

The road to the doctoral degree has not always been an easy one. But I've gained a lot of knowledge, both technical and human.

“Minds are like parachutes, they only function when open”

-Thomas Dewar

A handwritten signature in black ink that reads "Richard Lund". The signature is written in a cursive style with a prominent loop at the end of the last name.

Trondheim 10. jan. 2005

Richard Lund

II ABSTRACT

Power electronic converters are widely used in industrial power conversion systems both for utility and drives applications. As the power level increases, the voltage level is increased accordingly to obtain satisfactory efficiency. During the last years, the voltage rating of fast switching high voltage semiconductors such as the Insulated Gate Bipolar Transistor (IGBT) has increased. Still, there is a need for series connection of switching devices. In this area of applications, the Multilevel Converter has shown growing popularity.

The fundamental advantages of the Multilevel Converter topologies are low distorted output waveforms and limited voltage stress on the switching devices. The main disadvantages are higher complexity and more difficult control.

In this thesis, Multilevel Converters are analysed for large motor drive applications. The main focus has been on converter losses, output waveform quality and control.

Analytical expressions for both switching and conduction losses for 4- and 5-level Diode Clamped Converters have been developed. The investigation shows that the losses can be reduced by utilizing a multilevel topology for a 1 MW drive. This work is presented in [46]. The same reduction in losses is proven for a 2300V/ 3 MW drive.

Analytical expressions for the harmonic losses in 3-level converters have been developed for 2 different Carrier Based PWM schemes, presented in [56], [57] and [58]. Also Space Vector PWM are investigated and compared by simulations, in addition to 4- and 5-level Carrier Based PWM.

DC-bus balancing in both 3- and 5-level converters is discussed. Balancing in 3-level converters can be achieved by proper control. Balancing in 5-level converters can be achieved by proper arrangement of isolated DC-supplies.

One 40kW 3-level converter and one 5kW 5-level converter has been designed and built. Experimental verification of the analytical and simulated results is shown.

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INTRODUCTION

Introduction to Multilevel Converters

Multilevel Converters (MLCs) have been attracting attention in recent years, and have been proposed as the best choice in several medium and high voltage applications. Such applications can be Static VAR Compensators [1] and Large Electrical Drives, as in [2] and [3].

In the extrapolation of converters to higher power levels, the fundamental question of increasing the converter current rating (devices in parallel) or the converter voltage rating (devices in series) always has to be answered. The conduction losses in converters favour the increased voltage approach. All these factors contribute to the necessity for multilevel converter topologies or series connection of devices in traditional converter topologies.

As mentioned, for high voltage applications, the main advantage of a multilevel structure is the active clamping of the voltage levels. Series connections in traditional solution for high power converters is complex with fast switching devices because of simultaneous switching and correct static and dynamic voltage sharing of series devices.

Other advantages for the MLC topologies are lower distortion at the output, reduced EMC/EMI problems and in some cases, lower overall losses. The disadvantages are more complex control and increased mechanical complexity.

MLCs have also been shown to be a promising technology for low voltage and low power applications by using MOSFETs instead of IGBTs. Low voltage power-MOSFETs have achieved a significant cost advantage at about 5:1 compared to IGBTs, because of the widespread use in automotive and power supplies industry [5]. In [5], a 3-level converter for low power drives (1kW/110V) is developed using modest priced 150V MOSFETs. In [30], a multilevel converter for automotive dual (14V/42V) battery system is presented. A switch-mode power

amplifier is constructed in [6]. This MOSFET based cascaded H-bridge converter has a rating of $\pm 100\text{V}/100\text{A}$.

Numerous topologies and modulation strategies have been introduced and widely studied in literature, as presented in Chapter 1 and 2. Thanks to the high technological level of new power devices, especially the IGBT, these converters have gained more attention than current source converters in the high power applications the last years. For high power electrical motor drives the 3-level diode clamped converter, originally named Neutral Point Clamped (NPC) converter was one of the first topologies [11] that attracted attention.

Several large vendors have adopted this 3-level topology for their medium voltage drives. ABB is using the 3-level topology in both their ACS 1000 and ACS 6000 series, with output voltages from 2.3 kV to 4.16 kV, and power range from 315 kVA-27 MVA [7]. Siemens SIMOVERT MV [8] is also utilising this topology with voltage and power range 2.3 kV-6.6 kV and 660 kVA-9 MVA, respectively. Not only European vendors, but also Asian vendors such as Mitsubishi employ the popular 3-level converter [10].

Other vendors have adopted other topologies for their converters. Robicon [25] is using a Cascaded Multicell topology for their medium voltage drives. One of the disadvantages of this topology is the need for isolated DC-bus supplies. Robicon is using a multi-winding transformer on the input side to accomplish this. Hence, input currents with very low distortion are generated. Alstom has introduced a new series of converters in the medium voltage range called SYMPHONY [9]. The topology used is a capacitor clamped converter with a 4-level output voltage.

Even though there exist several topologies on the market, the diode clamped converter seems to be the most popular multilevel converter topology.

An ongoing research project at NTNU, called *All Electric Ship* is dealing with issues in electrification of ships. Applications could be main propulsion, positioning thrusters, winches and actuation etc. A typical system of such a system is shown in Figure 0.1.

For main propulsion in the megawatt range, multilevel conversion is a promising alternative. The maximum power rating of low voltage Pulse Width Modulated (PWM) converter drives is limited by practical current ratings such as motor and cables ($\sim 2500\text{A}$). Hence at the widely used 690V voltage, the limit today is $\sim 3\text{MVA}$ [7]. Even though improved components and knowledge move this limit up to 5 MVA, motor and converter manufacturers prefer the medium voltage range (2.3 kV-6.6 kV) at this power level. Also, as more electrical equipment is introduced in the ship, the power consumption is increased, and it is likely to believe that medium voltages become more common in the main supply. Direct connection to this voltage is preferable to avoid transformers, thus the need for high voltage converters is increasing.

The wish for a solution without a transformer omits the cascaded multi cell topology, leaving only the diode clamped and the capacitor clamped topologies as alternatives. Since the diode clamped converter is the most common, the work in this thesis is mainly concentrated on this topology.

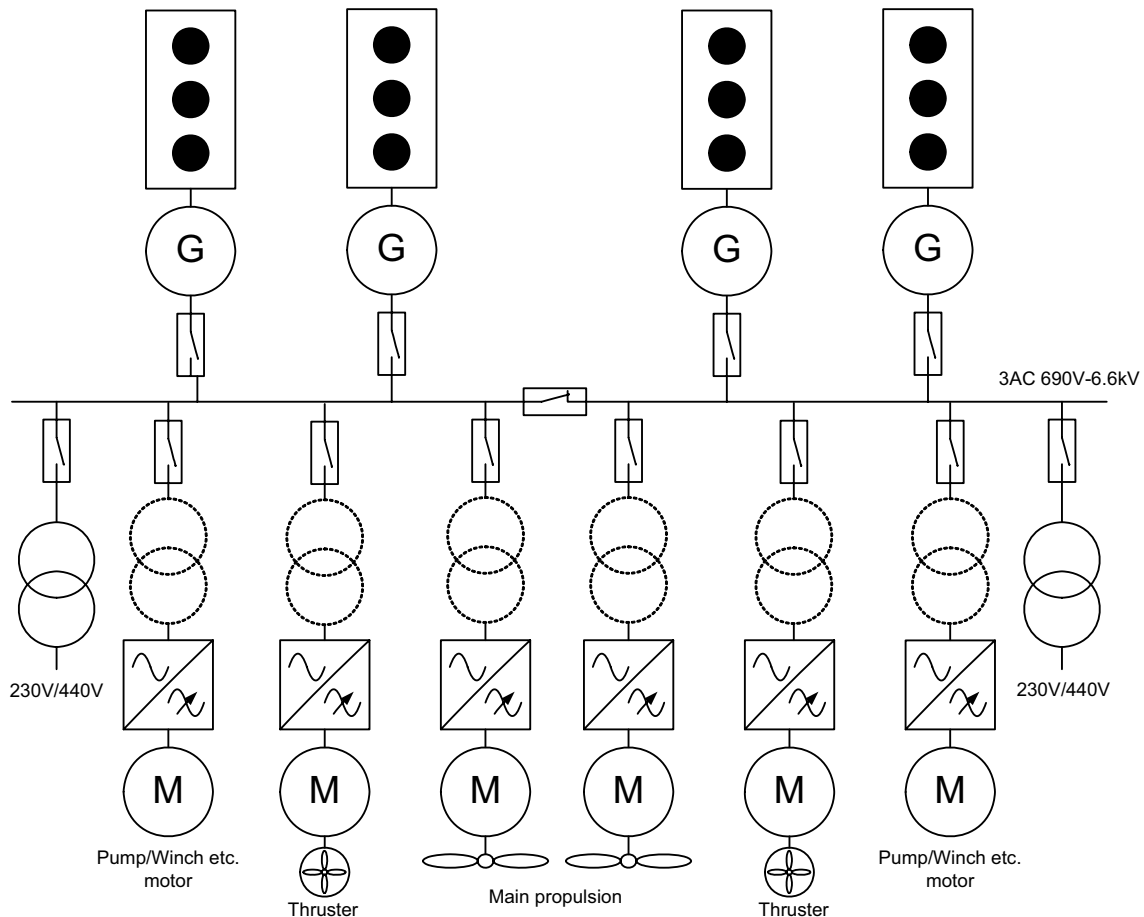


Figure 0.1: Typical all electric ship system.

Outline of the Thesis

The thesis is organized into eight different chapters, each chapter covering important aspects of Multilevel Converters (MLCs). Many MLC topologies have evolved the last decade, and Chapter 1 gives an overview of the state of the art of different Multilevel Converter topologies.

In addition to all the different topologies presented the last years, a corresponding amount of modulation schemes have been developed. Both synchronous and asynchronous Pulse Width Modulation (PWM) is presented. Carrier based PWM and Space Vector PWM (SVPWM) are investigated in detail. Simulation models for the different modulation methods have also been developed.

One of the main parts of this thesis is the investigation of the switching and conduction losses for MLCs. Chapter 3 presents analytical expressions for

calculation of the conduction- and switching losses for 4- and 5-level Diode Clamped Converters. By this, a direct comparison to utilization of different switches in the same topologies, and comparison between different topologies can be performed without time consuming simulations.

This comparison is performed in Chapter 4. A 1 MW/1500 V converter based on 2-, 3-, 4- and 5-level topologies, and a 3 MW/ 2300 V converter (3-, 4-, 5-level) are analysed and compared.

To verify the theory and simulations of harmonics and DC-bus balancing, laboratory models have been designed and built. A short presentation of a 40 kW 3-level, and a 5 kW 5-level converter is shown in Chapter 5.

In Chapter 6, the harmonic losses at the output of MLCs are analysed. For the 3-level converter, analytical equations are simplified and developed for two different modulation techniques. Extensive simulations are performed for other kinds of modulation strategies for the 3-level topology, and also for 4- and 5-level topologies. The analytical expressions and simulations are supported by measurements in the laboratory.

One important area of research in MLC is the DC-bus balancing of the capacitor voltages in the DC-link. Problem description and simulation models are developed in Chapter 7 for 3-level and 5-level converters. Measurements on the experimental prototypes are performed for verification of the theory.

Finally, conclusions, discussion and scope of further work are presented in Chapter 8.

In this thesis, different computer programs have been utilized to simplify the analysis: MATLAB [68] has been used for general analysis, numerical modelling and general plotting, KREAN [67] and Saber Designer [70] have been used for electrical circuit analysis, and MAPLE [69] has been a valuable tool for analytical mathematics. In addition, Microsoft Office has been used for typing the manuscript and for making spreadsheets.

NOMENCLATURE

α_i	: <i>Switching angle</i>
$\underline{\alpha}^s$: <i>α -axis vector, stator coordinates</i>
$\underline{\beta}^s$: <i>β -axis vector, stator coordinates</i>
ζ_s^s	: <i>Angle of reference voltage vector w.r.t. $\underline{\alpha}^s$</i>
$\zeta_s^{s'}$: <i>Angle of reference voltage vector w.r.t. nearest \underline{u}_{L1}</i>
ω	: <i>Angular speed</i>
φ	: <i>Phase angle</i>
$\varphi_1, \varphi_2, \varphi_3, \varphi_4$: <i>Crossing angles between switching areas</i>
\underline{a}	: <i>Scaling space vector</i>
a_α, a_β	: <i>Coordinates of left corner of transformed vector space</i>
b_α, b_β	: <i>Coordinates of right corner of transformed vector space</i>
CSI	: <i>Current Source Inverter</i>
C	: <i>Capacitor</i>
c_α, c_β	: <i>Coordinates of upper/lower corner of transformed vector space</i>
DSP	: <i>Digital Signal Processor</i>
d	: <i>Duty cycle</i>
D_{ij}	: <i>Diode, number i in phase j</i>
$E(I)$: <i>Dynamic switching energy</i>

E_{REC}	: Diode turn-off energy
E_{ON}, E_{OFF}	: Transistor switching energy, turn on/off
ESR_n	: Equivalent Series Resistance
F	: Generalized function
f_s	: Fundamental output frequency
f_{sw}	: Switching frequency
f	: frequency
GTO	: Gate Turn-off Thyristor
$H(i)$: Peak harmonic component
h_{ji}	: switching function element
H	: switching function element
i	: Current
i	: General integer
\underline{I}_{in}	: DC-bus current vector
\underline{I}_{out}	: Converter output current vector
i_{np}	: Neutral point current
I_C	: Collector current
$I_{C,N}$: Rated collector-emitter current
$I_{cap,rms,n}$: Harmonic capacitor RMS current
Δi_N	: Ripple current
Δi_n	: Nominal ripple current
$\Delta I_{N,rms}$: RMS ripple current
\hat{I}	: Peak current
I_{avg}	: Average current
I_{rms}	: RMS current
$I_{cap,rms,n}$: Harmonic capacitor RMS current

<i>IGBT</i>	: <i>Insulated Gate Bipolar Transistor</i>
<i>j</i>	: <i>General integer</i>
<i>j</i>	: <i>Phase index, $j=a, b, c$</i>
<i>j</i>	: $\sqrt{-1}$
<i>k</i>	: <i>General integer, $k=1, \dots$</i>
$k_{1,T}, k_{2,T}$: <i>Switching loss constants</i>
<i>MOSFET</i>	: <i>Metal Oxide Field Effect Transistor</i>
<i>MLC</i>	: <i>Multilevel Converter</i>
<i>M</i>	: <i>Modulation index</i>
m_{ji}	: <i>Average switching function</i>
M_s	: <i>Modulation index for SVPWM</i>
M_3	: <i>Modulation index for 3. harm signal</i>
<i>n</i>	: <i>Number of output levels in converter structure</i>
n_{cell}	: <i>Number of converter cell</i>
<i>NPC</i>	: <i>Neutral Point Clamped</i>
n_{uout}	: <i>Number of available switch combinations</i>
<i>PWM</i>	: <i>Pulse Width Modulation</i>
P_{sw}	: <i>Switching losses</i>
P_c	: <i>Conduction losses</i>
$P_{c,out}$: <i>Converter output voltage</i>
$P_{cap,tot}$: <i>Total capacitor power losses</i>
<i>RMS</i>	: <i>Root-Mean-Square value</i>
r_f	: <i>Forward conducting resistance</i>
S_j	: <i>Multi pole switch</i>
<i>SVPWM</i>	: <i>Space Vector Pulse Width Modulation</i>
T_{ij}	: <i>Transistor, number i in phase j</i>
T_{sw}	: <i>Switching period</i>

T_p	: <i>Fundamental period</i>
t	: <i>Time</i>
τ	: <i>Sample time</i>
T	: <i>Time period</i>
T	: <i>Temperature</i>
t_μ	: <i>Microscopic time</i>
U_{dc}	: <i>DC-bus voltage</i>
$u_{trii}(t)$: <i>Carrier signal, number i</i>
$u_{stj}(t)$: <i>Control signal, $j=a, b, c$</i>
$u'_{stj}(t), u''_{stj}(t),$ $u'''_{stj}(t)$: <i>Modified control signals</i>
\underline{U}_0	: <i>Zero voltage vector</i>
$\underline{U}_{S1}, \underline{U}_{S2}$: <i>Small voltage vectors</i>
\underline{U}_M	: <i>Medium voltage vectors</i>
$\underline{U}_{L1}, \underline{U}_{L2}$: <i>Large voltage vectors</i>
\underline{u}_U	: <i>Induced voltage vector</i>
\underline{U}_{out}	: <i>Converter output voltage vector</i>
\underline{U}_{in}	: <i>DC-bus voltage vector</i>
$\underline{u}_{st,ref}$: <i>Reference voltage vector</i>
$u_{com1}(t), u_{com2}(t)$: <i>Common mode injection signals</i>
U_f	: <i>Dynamic forward voltage</i>
U_{f0}	: <i>Static forward voltage</i>
U_{CE}	: <i>Collector–emitter voltage</i>
U_{GE}	: <i>Gate-emitter voltage</i>
VSI	: <i>Voltage Source Inverter</i>

1 OVERVIEW OF MULTILEVEL TOPOLOGIES

1.1 Introduction

During the last 20 years, several multilevel converter topologies have evolved. A brief presentation of the different topologies is presented in the following.

The multilevel converter main components are an array of power semiconductor switches and a stack of capacitor voltage sources.

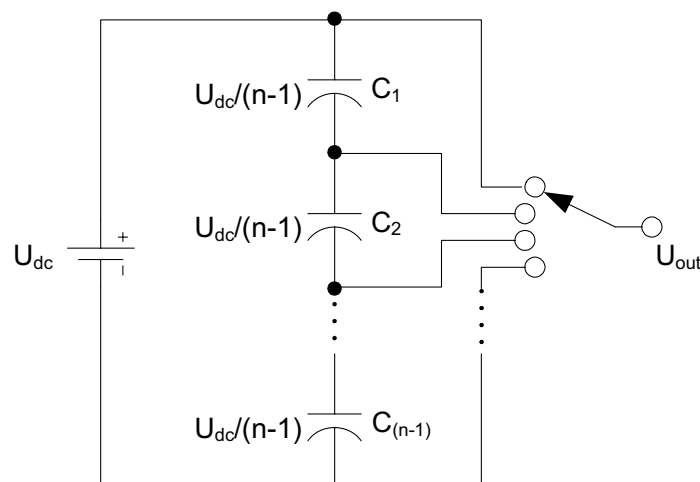


Figure 1.1: One phase leg of a generalized n -level converter.

By connecting the output of the converter to the stack of capacitors a multilevel output voltage is achieved. Figure 1.1 shows one phase leg of a generalised n -level converter. It consists of a DC-source, $n-1$ capacitors, and a n -pole switch. By connecting the switch to different poles, n -levels can be synthesised at the output terminal with respect to the negative DC-rail.

1.2 Configurations with Diode Clamps

The oldest reference to multilevel power conversion is often stated to start with the paper presented by Nabae et al. [11]. The resultant PWM waveform from this Neutral Point Clamped (NPC) topology (3-level) showed considerably better spectral performance compared to a conventional PWM VSI (2-level). This NPC converter has been extended to higher number of levels in [14]. Figure 1.2 (left) shows one phase-leg of a 5-level Diode Clamped Converter. One phase leg consists of $2 \cdot (n-1)$ active switches and $(n-1)(n-2)$ clamping diodes. The total DC-bus voltage $U_{dc}=4V$ is evenly distributed across the DC-capacitors, C_1-C_4 ($U_{C1}=U_{C2}=U_{C3}=U_{C4}=V$). Hence, an output voltage of $0, V, 2V, 3V$ and $4V$ is possible at the output with respect to the negative DC-rail.

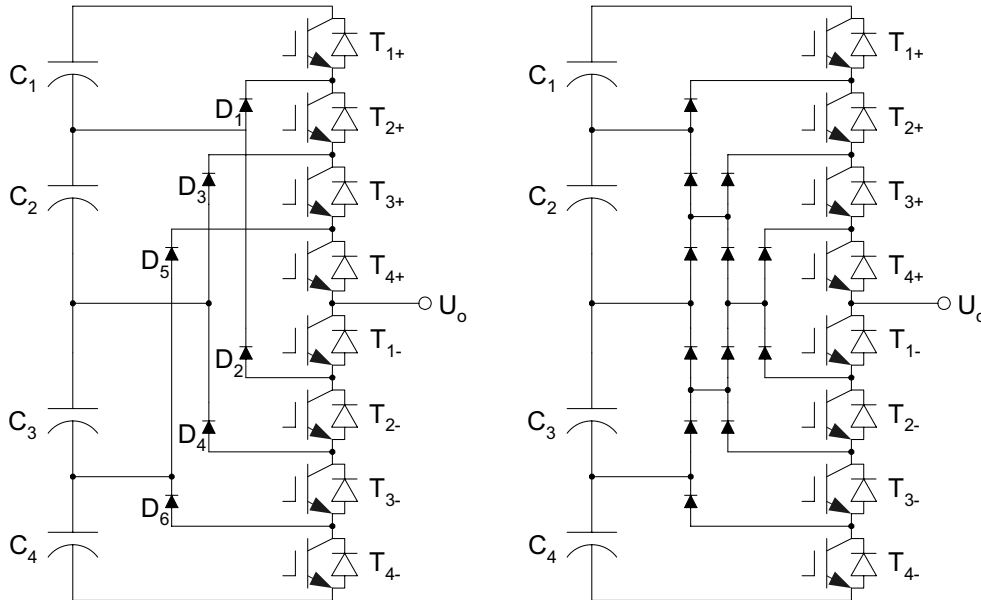


Figure 1.2: 5-level Diode Clamped Converter: Conventional (left). Pyramid connected clamping diodes (right).

These five levels are obtained by closing a set of four switches (Table 1-1). This creates a bi-directional current path connecting two of the clamping diodes back-to-back from the taps on the DC-bus to the output.

It should be noted that Diode Clamped Converters with odd number of levels ($n = 3, 5, 7, \dots$) offer a neutral point access. It is also possible to synthesize topologies with even number of levels ($n = 4, 6, 8, \dots$). Converters with even number of levels have a handicap in single phase applications where a neutral point is needed. These topologies have on the other hand proven to be well suited for drive applications ([15] and [16]). Although each active switching device is only required to block a voltage level of $U_{dc}/n-1$, the clamping diodes must have different voltage ratings. When closing the four lower switches ($T_{1-}-T_{4-}$) in a 5-level topology (Figure 1.2, left), D_2 must block $3V$ ($3U_{dc}/4$) and D_2 needs to block $2V$ ($U_{dc}/2$). Similar, by closing the four upper switches ($T_{1+}-T_{4+}$), D_5 must withstand $3U_{dc}/4$ and $D_5, U_{dc}/2$.

Table 1-1: Switch combinations for a 5-level Diode Clamped Converter.

Output	T ₁₊	T ₂₊	T ₃₊	T ₄₊	T ₁₋	T ₂₋	T ₃₋	T ₄₋
4V	ON	ON	ON	ON	OFF	OFF	OFF	OFF
3V	OFF	ON	ON	ON	ON	OFF	OFF	OFF
2V	OFF	OFF	ON	ON	ON	ON	OFF	OFF
1V	OFF	OFF	OFF	ON	ON	ON	ON	OFF
0	OFF	OFF	OFF	OFF	ON	ON	ON	ON

Assuming that the voltage rating of the clamping diodes are the same as the active switching devices, the number of diodes is $(n-1) \cdot (n-2)$ pr. phase. An interesting approach is to configure the diodes in a pyramid as presented in [17] and shown in Figure 1.2 (right). By this configuration, each clamping diode will have to block the same voltage, but the total number of diodes is the same as for the conventional topology.

A Cascaded Diode Clamped Converter has been presented in [18], and this topology is shown in Figure 1.3. This converter consists of a main NPC converter with an auxiliary NPC converter at the neutral point. The auxiliary converter is common for all bridge-legs. For a 5-level converter this topology only needs 16 active switching devices. The drawback is the voltage rating of the main converter devices. A blocking voltage of $U_{dc}/2$ is needed.

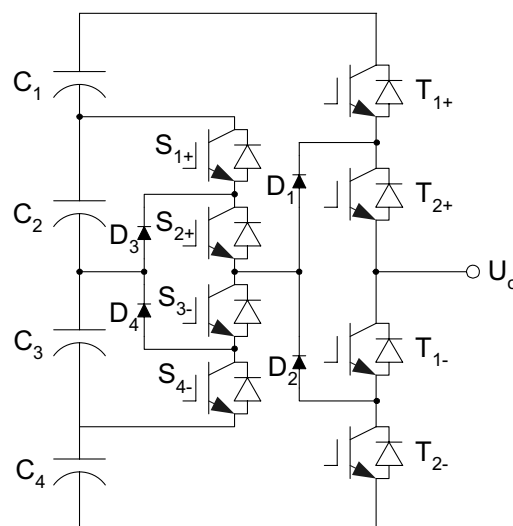


Figure 1.3: Cascaded Diode Clamped Converter.

The switching configurations for the Cascaded Diode Clamped Converter are given in Table 1-2. By using the auxiliary converter, the innermost dc-bus taps are accessed.

Table 1-2: Switch combinations for a 5-level Cascaded Diode Clamped Converter.

Output	T ₁₊	T ₂₊	T ₁₋	T ₂₋	S ₁₊	S ₂₊	S ₁₋	S ₂₋
4V	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
3V	OFF	ON	ON	OFF	ON	ON	OFF	OFF
2V	OFF	ON	ON	OFF	OFF	ON	ON	OFF
1V	OFF	ON	ON	OFF	OFF	OFF	ON	ON
0	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF

1.3 Capacitor Clamped Converters

Another approach to multilevel power conversion is to use clamping capacitors instead of clamping diodes. This topology was presented in [12], and is also referred as a Flying Capacitor Converter. It consists of $2 \cdot (n-1)$ active switches, $(n-1) \cdot (n-2)/2$ clamping capacitors and $(n-1)$ main DC-bus capacitors. A 5-level converter is shown in Figure 1.4. If each capacitor has a voltage of V , the converter can synthesize $0, V, 2V, 3V$ and $4V$ at the output.

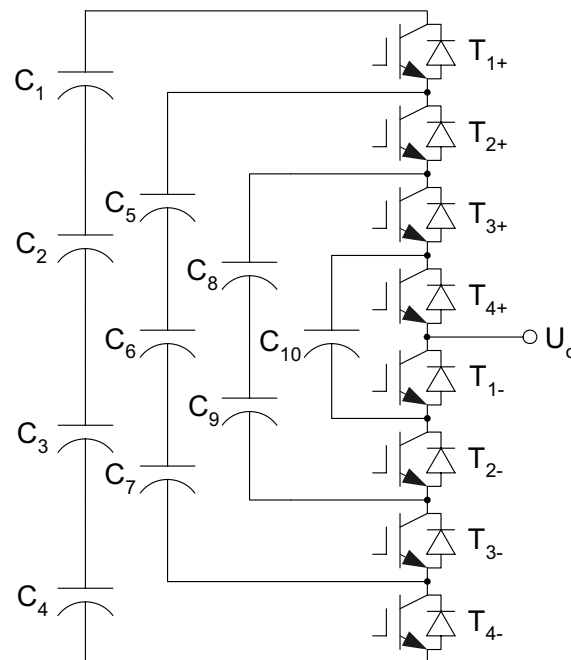


Figure 1.4: 5-level Capacitor Clamped Converter.

The Flying Capacitor Converter is more flexible in switch combinations for different voltage levels than the diode clamped converter as listed in Table 1-3. However, a problem with this topology is the complicated control of the floating

capacitor voltages [13]. Balancing of the different capacitor voltages is beyond the scope of this thesis, and will not be discussed any further.

Table 1-3: Switch combinations for a 5-level Capacitor Clamped Converter.

Output	Switching combinations (conducting switches)					
4V	$T_{1+} - T_{4+}$					
3V	$T_{1+} - T_{3+}$ and T_{1-}	$T_{2+} - T_{4+}$ and T_{4-}	$T_{1+}, T_{3-},$ T_{3+} and T_{4+}			
2V	T_{1+}, T_{2+}, T_{1-} and T_{2-}	$T_{3+}, T_{4+},$ T_{1-} and T_{2-}	$T_{1+}, T_{3+},$ T_{1-} and T_{3-}	$T_{1+}, T_{1-},$ T_{2-} and T_{3-}	$T_{2+}, T_{3+},$ T_{2-} and T_{4-}	$T_{2+}, T_{3+},$ T_{1-} and T_{2-}
1V	T_{1+}, T_{1-}, T_{2-} and T_{3-}	$T_{4+}, T_{2-},$ T_{3-} and T_{4-}	$T_{3+}, T_{1-},$ T_{3-} and T_{4-}			
0	$T_{1-} - T_{4-}$					

1.4 Multilevel Multiple Three-Phase Converters

Multilevel output can also be achieved by adding and phase-shifting several 3-phase 2-level VSIs by using a multi-winding transformer as shown in Figure 1.5 (left). Another approach presented in [19] is to arrange the converters in a delta configuration as shown in the middle of Figure 1.5.

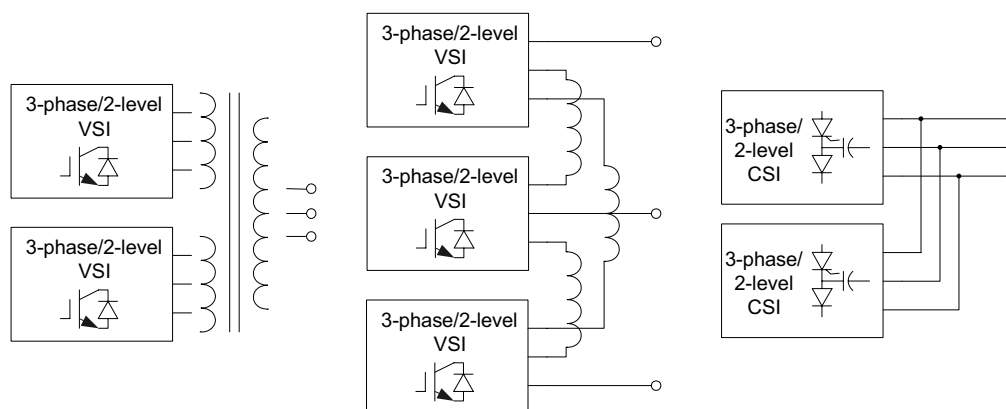


Figure 1.5: Multilevel Converters by serial connection of several 3-phase 2-level VSI/CSIs.

Both of these topologies need extra interconnecting reactances or transformers, thus the converters become bulky and lossy. An alternative approach is presented in [20] using Current Source Inverters (CSIs), shown in Figure 1.5 (right).

1.5 Cascaded Multicell Converters

This class of Multilevel Converters is based on series connection of single-phase converters, and the earliest reference is probably [21] back in 1973, and used for plasma stabilisation in [22]. It was also introduced for Static VAR applications in [24] and for drive applications in [25]. One topology consists of single-phase H-bridge which is connected in series, forming a phase-leg. As can be seen in Figure 1.6, the output can be $0, \pm V$ and $\pm 2V$, if the capacitor voltages are $U_{C1} = U_{C2} = V$, and hence a 5-level output is obtained. If n_{cell} is the number of single-phase H-bridges per phase-leg, $n = 2 \cdot n_{cell} + 1$ levels is obtained at the output. This arrangement is called an Order-1 configuration [27]. In [23] and [26] an extension of this topology is presented. By letting $U_{C1} = V$ and $U_{C2} = 2V$, the output can be $0, \pm V, \pm 2V$ and $\pm 3V$. Thus a 7-level output is obtained. In general, $n = 2^{n_{cell} + 1} - 1$ levels are obtained at the output. This arrangement is called an Order-2 configuration. It is also possible to let $U_{C1} = V$ and $U_{C2} = 3V$, the output is then $0, \pm V, \pm 2V, \pm 3V$ and $\pm 4V$. Thus a 9-level output is obtained. In general, $n = 3^{n_{cell}}$ levels are obtained at the output (Order-3 configuration).

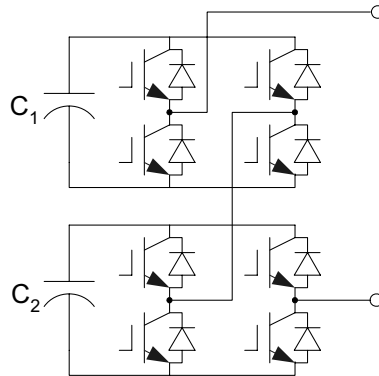


Figure 1.6: 5-level Cascaded Multicell Converter using series connection of single-phase H-bridge converters.

Another approach is to connect single phase converters in series with the output of each phase of a multiple phase converter. In [28] and [29] a topology based on a 3-phase NPC converter and 3 single phase H-bridges is presented (Figure 1.7). By letting $U_{C1} + U_{C2} = 3V$ and $U_{C3} = V$, the output can be $0, \pm V, \pm 2V, \pm 3V$ and $\pm 4V$. Thus a 9-level output is obtained. It is possible to operate the converter without any supply of the low voltage converter. To obtain this, no active power can be transferred over the small voltage converter.

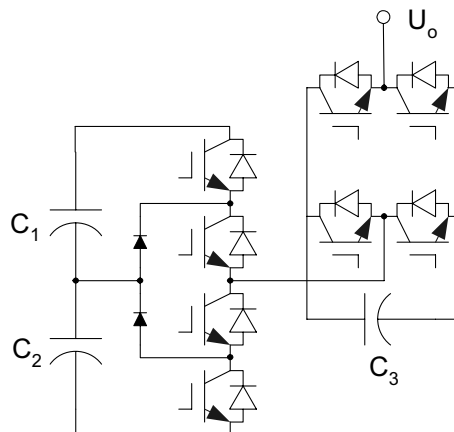


Figure 1.7: 9-level Hybrid Asymmetric Converter.

1.6 Generalized Multilevel Converter

In [30] a generalized structure of a Multilevel Converter is presented, one phase leg of such a 5-level converter is shown in Figure 1.8.

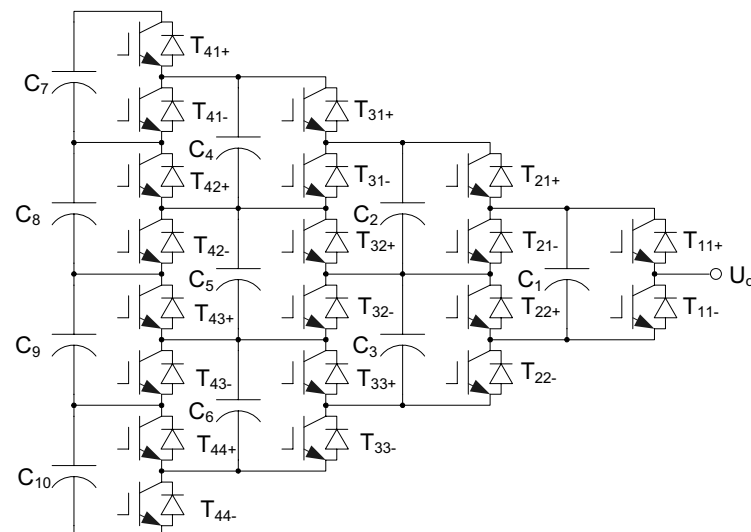


Figure 1.8: Generalized 5-level converter leg.

The uttermost switches (T_{11+} - T_{x1+} and T_{11-} - T_{xx-} , $x=1..4$) are used to synthesize the desired voltage waveforms, The rest of the devices are used for clamping and balancing of the capacitors voltages. The switching rules are as follows: each switch pole is an independent switching unit, i.e. T_{xx+} and T_{xx-} are complementary. Any adjacent two switches are complementary. This means that if any switch state is set, the others are known. An Example: if T_{41+} is on, T_{41-} is off. T_{42+} , T_{43+} and T_{44+} are on. T_{42-} , T_{43-} and T_{44-} are off. The switch combinations are similar to those found for the Capacitor Clamped Converter in Table 1-3, i.e. one combination for 0 and 4V, three combinations for 1V and 3V, and finally four combinations for 2V (C_1 - $C_{10}=V$). From the converter in Figure 1.8 it is also possible to deduce other

topologies. By removing the inner switches (except the freewheeling diodes) and the inner capacitors, the Diode Clamped Converter with pyramid stacked diodes in Figure 1.2 (right) can be extracted. By removing the inner switches with freewheeling diodes, the Capacitor Clamped Converter in Figure 1.4 can be deduced. These topologies are shown in Figure 1.9.

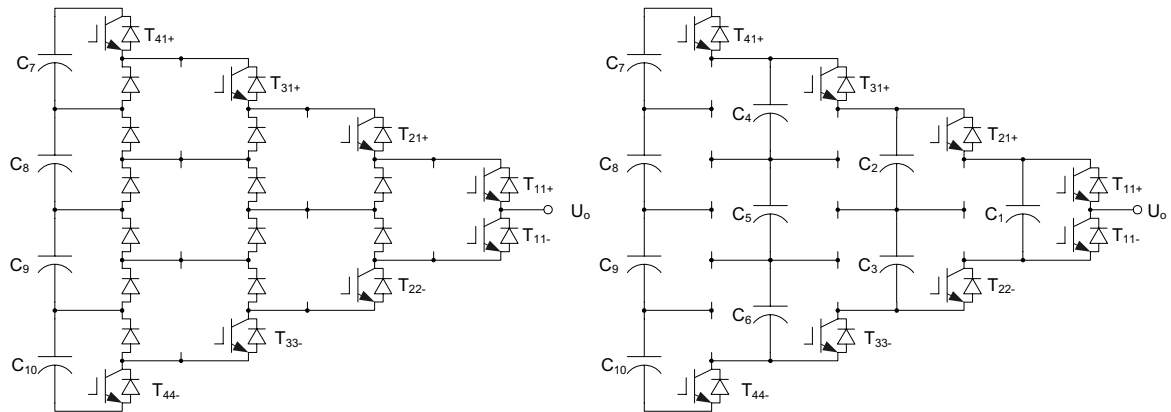


Figure 1.9: Deduced converter topologies: Diode Clamped Converter (left), Capacitor Clamped Converter (right).

1.7 Comparison of Topologies

In Table 1-4, a comparison of the main different topologies is given. The table shows the number of primary switching devices, DC capacitors and output levels for all 3 phases.

Table 1-4: Comparison of converter topologies (3 phases), $k=1\dots$

Topology	Primary switching devices	DC Capacitors	Output levels
Diode Clamped	$6k$	k	$k+1$
Capacitor Clamped	$6k$	$3k-2$	$k+1$
Cascaded Multicell Converter 1-Order	$12k$	$3k$	$2k+1$
Cascaded Multicell Converter 2-Order	$12k$	$3k$	$2^{k+1}-1$
Cascaded Multicell Converter 3-Order	$12k$	$3k$	3^k

The Cascaded Multicell topology can generate the most number of levels from a given number of switching devices and DC-busses. E.g., for a 5-level Diode Clamped or Capacitor Clamped Converter ($k=4$), 24 primary switching devices are needed. By using 24 primary switching devices in a Cascaded Multicell Converter

($k=2$), 9 levels are generated at the output. The main problem with this topology is that a separate, isolated DC-supply is needed for every DC-bus level and phase. Further, the Capacitor Clamped topology is presented in the literature as difficult to control, and needs balancing capacitors. The Diode Clamped topology has its disadvantages such as the unequal voltage rating of the clamping diodes. Balancing issues for high number of levels as discussed in Chapter 7 are also a concern, but the technology is proven for 3-level converters as discussed in the introduction chapter. The main focus in this thesis will hence be on Diode Clamped Converters.

2 MODULATION STRATEGIES FOR MULTILEVEL CONVERTERS

Since the introduction of multilevel power converters, a number of different topologies have been discussed. A lot of research has been performed to control the output waveform of these converters. Numerous modulation strategies have been presented in the literature, the most interesting are summarized in [31], [32] and [33].

2.1 Overview of Modulation Strategies

Multilevel modulation can be divided into two main categories, Synchronous Modulation and Asynchronous Modulation. Figure 2.1 shows a block diagram of the most popular methods used.

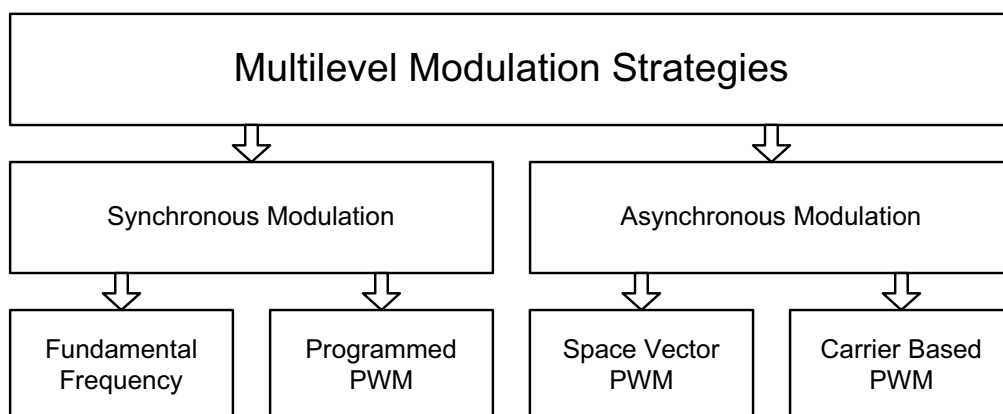


Figure 2.1: Schematic overview of multilevel modulation strategies.

2.2 Synchronous Modulation

Synchronous Modulation methods are a class of modulation schemes where the switching of the devices is synchronized with the reference voltages. In these methods the switching frequency is low and usually equal to the fundamental frequency (e.g. 50-200 Hz).

2.2.1 Fundamental Frequency Modulation

Fundamental Frequency Modulation is used for slow switching semiconductors such as Gate Turn-off Thyristors (GTOs). This scheme of modulation is a synchronous modulation method, since there is only one commutation of the switches per fundamental cycle of the output voltage. By utilizing such a modulation strategy, the output level waveform has a stepped shape. Figure 2.2 shows an output waveform for 3-level and 5-level converter respectively.

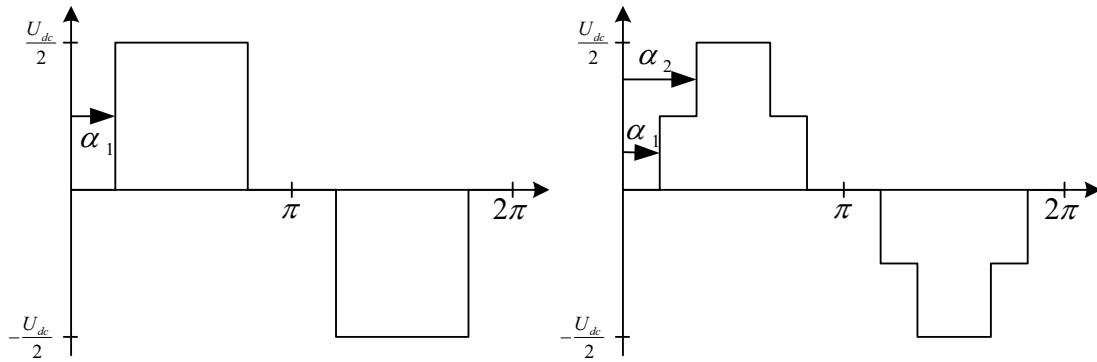


Figure 2.2: Stepped output waveform, 3-level (left), 5-level (right).

This strategy needs only low switching frequency capability from the devices. However, it is possible to optimize the switching angles α_i , ($i=1..m$) for a given modulation index M , so as to minimize a set of dominant harmonics in the output. By Fourier analysis, the k^{th} harmonic of a n -level waveform can be derived as follows:

$$H(k) = \frac{4}{\pi k} \frac{U_{dc}}{2} \frac{2}{n-1} \sum_{i=1}^m \cos(k\alpha_i) \quad (2.1)$$

Because of half-wave symmetry of the waveform, only odd harmonic component will exist, thus $k=1, 3, 5, 7, \dots$. The switching angles $\underline{\alpha} = [\alpha_1, \alpha_2, \dots, \alpha_m]^T$ are shown in Figure 2.2. From the figure, the following yields:

$$\alpha_1 < \alpha_2 < \dots < \alpha_m < \frac{\pi}{2} \quad (2.2)$$

It may be verified that if all the switching angles are set to zero, the output falls back to a conventional 2-level waveform and the fundamental voltage in this case is given by:

$$H(1)_{\max} = \frac{4 U_{dc}}{\pi 2} \quad (2.3)$$

In general, there exist m degrees of freedom due to m α_i 's. For the 3-level modulation only one parameter can be controlled, the fundamental component, $H(1)$ when one switching per. device and fundamental period is used. For a 4-level and 5-level converter, two independent parameters exist. This can be use to eliminate one dominant harmonic. It may be noted that the 5th is the most dominant harmonic since the even harmonics are cancelled because of the half wave symmetry and triple harmonics are eliminated in a three-phase three-wire system. Hence, the following set of equations has to be solved:

$$H(1) = \frac{U_{dc}}{2} M \quad , \quad H(5) = 0 \quad (2.4)$$

where $0 \leq M \leq 4/\pi$. Eq. (2.1) yields:

$$H(1) = \frac{U_{dc}}{\pi} [\cos \alpha_1 + \cos \alpha_2] \quad , \quad H(5) = \frac{U_{dc}}{5\pi} [\cos(5\alpha_1) + \cos(5\alpha_2)] \quad (2.5)$$

To solve these equations, a technique described in [26] can be used. Suppose a vector of angles $\underline{\alpha} = [\alpha_1, \alpha_2, \dots, \alpha_m]^T$ satisfies a set of equations $f_i(\underline{\alpha}) = 0$ to be solved. Then, one can formulate an equivalent minimization problem as follows; Let:

$$F(\underline{\alpha}) = \sum_{i=1}^m f_i(\underline{\alpha})^2 \quad (2.6)$$

$F(\underline{\alpha})$ is always non-negative, and therefore, if values of α exist for which $F(\alpha) = 0$, these have to be the minimum points for $F(\underline{\alpha})$. When $F(\underline{\alpha})$ is zero, each $f_i(\underline{\alpha})$ must be zero, thus the solution of the set of the equations is to search for the minima of Eq.(2.6). For a 5-level converter, the optimization functions can be found from Eq. (2.4)-(2.6):

$$\begin{aligned} f_1(\alpha_1, \alpha_2) &= \frac{U_{dc}}{\pi} \left[\cos \alpha_1 + \cos \alpha_2 - \frac{\pi}{2} M \right] \\ f_2(\alpha_1, \alpha_2) &= \frac{U_{dc}}{5\pi} [\cos(5\alpha_1) + \cos(5\alpha_2)] \end{aligned} \quad (2.7)$$

This leads to the final optimization function:

$$F(\alpha_1, \alpha_2) = \left(\frac{U_{dc}}{\pi} \right)^2 \left[\left(\cos \alpha_1 + \cos \alpha_2 - \frac{\pi}{2} M \right)^2 + \frac{1}{5^2} (\cos(5\alpha_1) + \cos(5\alpha_2))^2 \right] \quad (2.8)$$

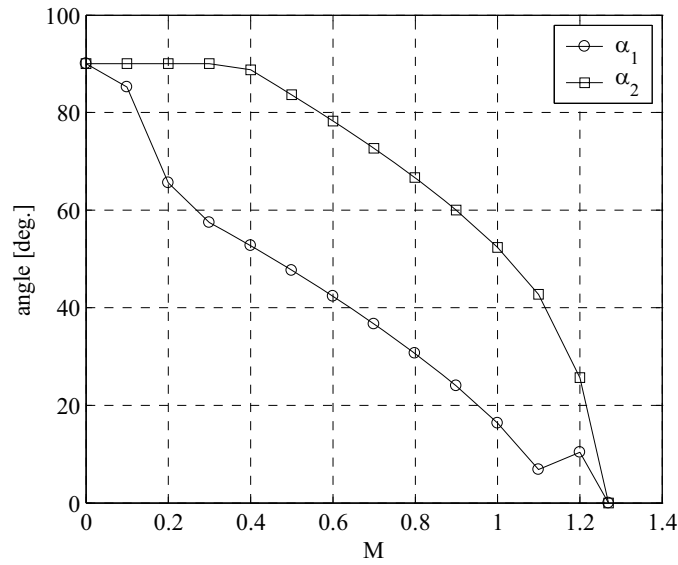


Figure 2.3: Switching angles for a 5-level converter.

Eq. (2.8) can be solved in MATLAB optimization toolbox and the results from the simulations are given in Figure 2.3.

To simulate the output waveforms in this chapter, MATLAB has been used. Figure 2.4 shows a simplified simulation schematic where u_a , u_b and u_c are the converter output voltages and u_{an} , u_{bn} and u_{cn} are the load voltages for a , b and c phase respectively. u_n is the neutral point voltage of the load, also referred to as common-mode or zero-sequence voltage. If a symmetrical load is used, it can be shown that the zero-sequence voltage is:

$$u_n(t) = \frac{1}{3}(u_a(t) + u_b(t) + u_c(t)) \quad (2.9)$$

Figure 2.5 shows the simulated output voltages for the fundamental frequency modulation at modulation depth $M=0.8$, resulting in switching angles at $\alpha_1=30.7^\circ$ and $\alpha_2=66.6^\circ$. From top, the converter phase voltage, the line voltage, the zero sequence voltage, and the load phase voltage are shown. At bottom, the harmonics from the load phase voltage is shown.

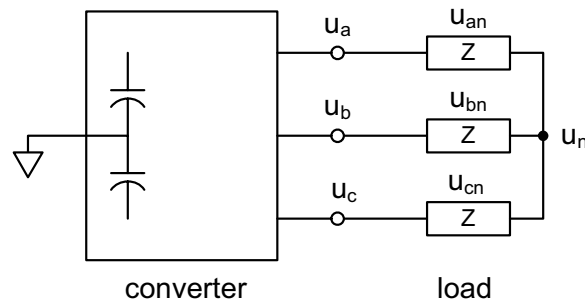


Figure 2.4: Simplified converter simulation model.

The triple harmonics in the load phase voltage are non-exciting, due to the symmetrical three phase system. Also the 5th harmonic is zero, caused by the harmonic elimination.

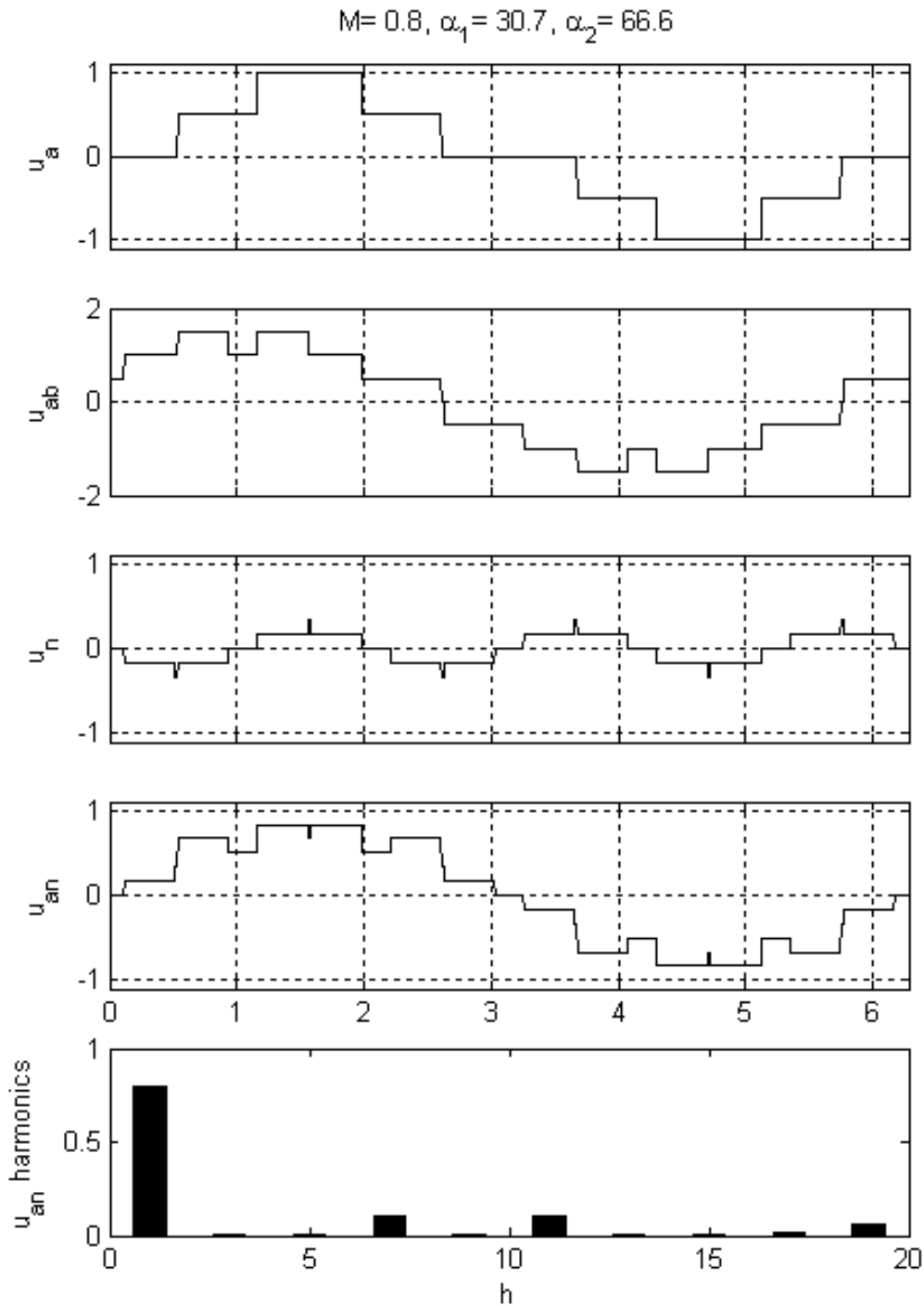


Figure 2.5: Stepped wave output waveforms from 5-level converter.

2.2.2 Programmed PWM

It is also possible to extend the Fundamental Frequency Modulation by introducing more switching angles in the output waveform as illustrated in Figure 2.6. This will introduce notches in the output waveform, and the number of commutations will increase per. fundamental cycle. This method is called Programmed PWM. By doing this, several harmonic components can be eliminated in the output waveform. In Figure 2.6, four angles can be controlled, thus three harmonics can be eliminated in addition to control of the fundamental voltage. To find the switching angles, the same method presented in Eq.(2.1)-(2.2) and (2.6) can be used. As more switching angles are introduced, the waveform converges to a classical PWM pattern.

Finding the optimized switching angles is quite computation intensive, and in a real application they are calculated off-line, and stored in look-up tables in the control system.

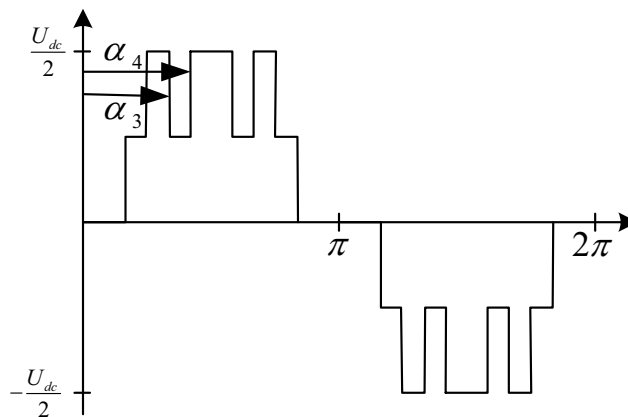


Figure 2.6: Programmed PWM for a 5-level converter.

2.3 Asynchronous Modulation

In this class of modulation methods, the switching is asynchronous with the reference voltages. This will introduce sub-harmonics of the fundamental component in the output voltage, but at high switching frequency (e.g. >1 kHz) the amplitude of the sub harmonics are small, and the asynchronous modulation method can be used [54].

2.3.1 Carrier Based PWM

Sinusoidal Carrier Based Pulse Width Modulation (CBPWM) is a classical approach, and is widely used in the literature. Figure 2.7 shows one phase of a Generalized Diode Clamped converter, which consists of $2(n-1)$ active devices. T_{ij+} and T_{ij-} are complementary (except for delay at turn on), where $i=1..(n-1)$ and $j=a$,

b, c. A generalized sinusoidal CBPWM strategy is shown in Figure 2.8. $(n-1)$ carriers, $u_{tri(i)}(t)$, are distributed in bands from -1 to +1.

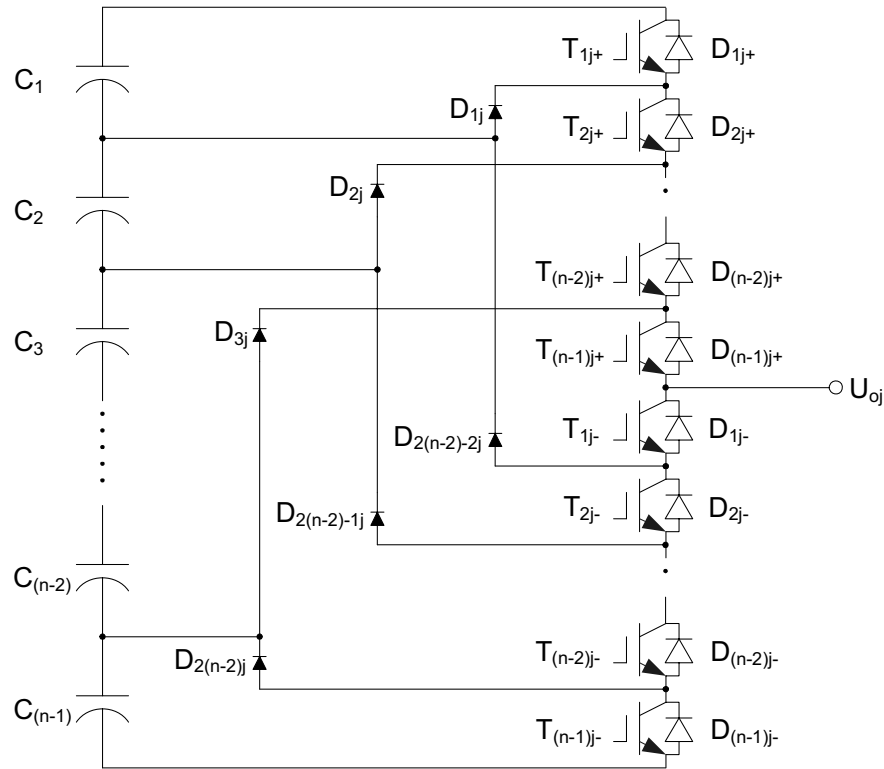


Figure 2.7: Generalized n -level Diode Clamped Converter (DCC).

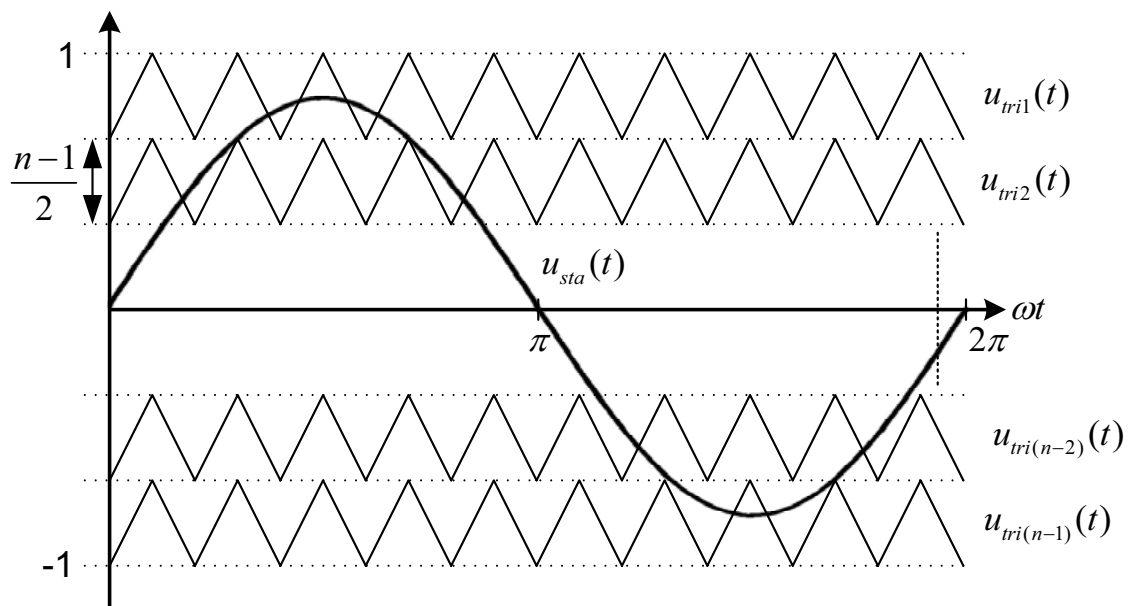


Figure 2.8: Generalized sinusoidal CBPWM.

The control signals for sinusoidal CBPWM are:

$$\begin{aligned} u_{sta}(t) &= M \sin(\omega t) \\ u_{stb}(t) &= M \sin(\omega t - 2\pi/3) \\ u_{stc}(t) &= M \sin(\omega t + 2\pi/3) \end{aligned} \quad (2.10)$$

where M is the modulation index, and ω the angular frequency. Of course, \cos functions can also be used in Eq.(2.10), \sin functions are only used for convenience. Both \sin/\cos are named sinusoidal function, and give the same characteristics/performance.

Switching of transistor T_{ij+} (i.e transistor number i in phase j) is done by the following algorithm:

$$\begin{aligned} \text{if } u_{stj}(t) > u_{trii}(t) \text{ then } T_{ij+} \text{ on} \\ \text{else } T_{ij+} \text{ off} \end{aligned}$$

The duty cycles, i.e average on-times for the switching devices within a switching period, can be expressed as:

$$d_{ij}(t) = \frac{n-1}{2} u_{stj}(t) + \frac{2i-n+1}{2} \quad (2.11)$$

When $u_{stj}(t)$ is inside band i . In addition,

$$\begin{aligned} \text{if } u_{stj}(t) > \text{band } i \text{ then } d_{ij+}(t) = 1 \\ \text{else if } u_{stj}(t) < \text{band } i \text{ then } d_{ij+}(t) = 0 \end{aligned}$$

E.g, if the control signal $u_{sta}(t)$ in Figure 2.8 is larger than the carrier signal $u_{tril}(t)$, transistor T_{1a+} in Figure 2.7 is turned on. Else, transistor T_{1a+} is off.

Figure 2.9 shows an example of the duty cycles at $M=0.8$ for 3-, 4- and 5-level converters respectively.

Looking at a 3-level converter, the borders of the two carrier bands become trivial:

$$M \sin(\omega t) = 0 \Leftrightarrow \omega t = \arcsin(0) \quad (2.12)$$

For the 4- and 5-level topology, the crossings will be as in (2.13) and (2.14) respectively.

$$M \sin(\omega t) = \frac{1}{3} \Leftrightarrow \omega t = \arcsin\left(\frac{1}{3M}\right) \quad (2.13)$$

$$M \sin(\omega t) = \frac{1}{2} \Leftrightarrow \omega t = \arcsin\left(\frac{1}{2M}\right) \quad (2.14)$$

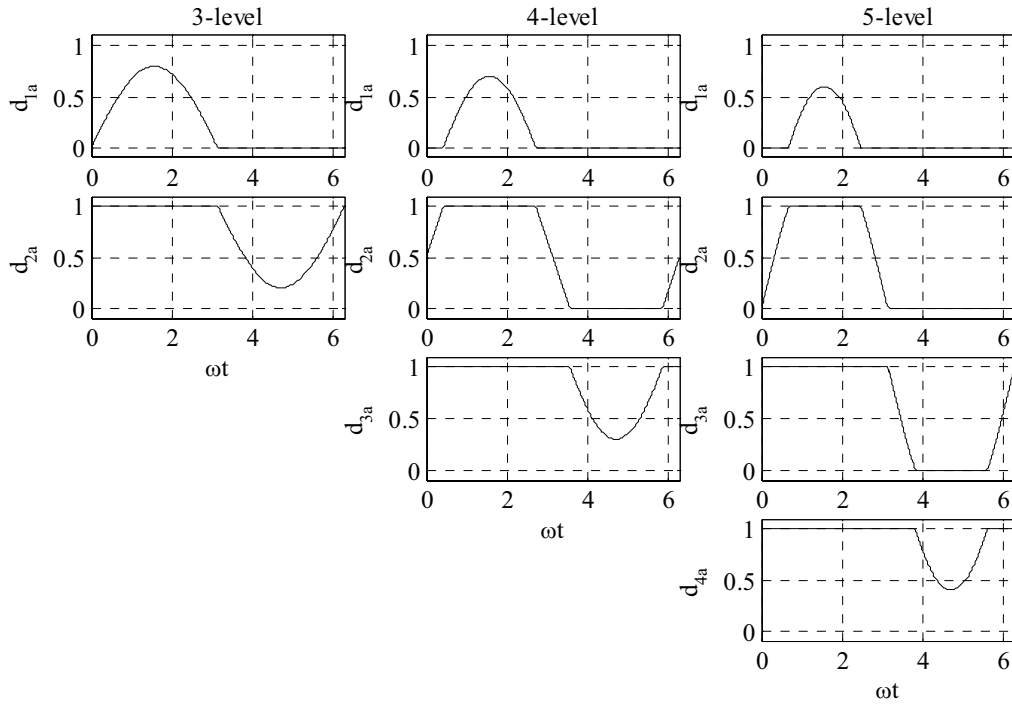


Figure 2.9: Duty cycles for 3-, 4-, and 5-level converters for $M=0.8$.

From this, the expressions for the duty cycles for phase a can be expressed as:

For the 3-level topology, the upper positive transistor T_{1a+} is switched on/off when the control signal is positive, while the lower positive transistor T_{2a+} is turned on. When the control signal is negative, the upper transistor is turned off, and T_{2a+} is switching. T_{1a-} and T_{2a-} are complementary to T_{1a+} and T_{2a+} respectively.

$$d_{1a} = \begin{cases} M \sin(\omega t) & , \quad 0 < \omega t < \pi \\ 0 & , \quad \pi < \omega t < 2\pi \end{cases} \quad (2.15)$$

$$d_{2a} = \begin{cases} 1 & , \quad 0 < \omega t < \pi \\ M \sin(\omega t) + 1 & , \quad \pi < \omega t < 2\pi \end{cases} \quad (2.16)$$

The 4-level topology has three carrier bands controlling the three positive transistors. The upper positive transistor T_{1a+} is switched on/off when the control signal is in the upper carrier band, and is switched off in the two lower bands. The middle positive transistor is switched on/off in the middle band, switched on in the upper band, and switched off in the lower band. The lower positive transistor is switched on/off in the lower band, and switched off in the two upper bands. From this, the duty cycles are:

$$d_{1a} = \begin{cases} 0 & , \quad 0 < \omega t < \arcsin(\frac{1}{3M}) \\ \frac{3}{2} M \sin(\omega t) - \frac{1}{2} & , \quad \arcsin(\frac{1}{3M}) < \omega t < \pi - \arcsin(\frac{1}{3M}) \\ 0 & , \quad \pi - \arcsin(\frac{1}{3M}) < \omega t < 2\pi \end{cases} \quad (2.17)$$

$$d_{2a} = \left\{ \begin{array}{ll} \frac{3}{2} M \sin(\omega t) + \frac{1}{2} , & 0 < \omega t < \arcsin(\frac{1}{3M}) \\ 1 , & \arcsin(\frac{1}{3M}) < \omega t < \pi - \arcsin(\frac{1}{3M}) \\ \frac{3}{2} M \sin(\omega t) + \frac{1}{2} , & \pi - \arcsin(\frac{1}{3M}) < \omega t < \pi + \arcsin(\frac{1}{3M}) \\ 0 , & \pi + \arcsin(\frac{1}{3M}) < \omega t < 2\pi - \arcsin(\frac{1}{3M}) \\ \frac{3}{2} M \sin(\omega t) + \frac{1}{2} , & 2\pi - \arcsin(\frac{1}{3M}) < \omega t < 2\pi \end{array} \right\} \quad (2.18)$$

$$d_{3a} = \left\{ \begin{array}{ll} 1 , & 0 < \omega t < \pi + \arcsin(\frac{1}{3M}) \\ \frac{3}{2} M \sin(\omega t) + \frac{3}{2} , & \pi + \arcsin(\frac{1}{3M}) < \omega t < 2\pi - \arcsin(\frac{1}{3M}) \\ 1 , & 2\pi - \arcsin(\frac{1}{3M}) < \omega t < 2\pi \end{array} \right\} \quad (2.19)$$

Similarly, the same rules apply for *the 5-level converter*. Here, the four positive transistors are controlled using four bands. The upper positive transistor T_{1a+} is switched on/off when the control signal is in the upper band etc. This gives the duty cycles for the 5-level topology:

$$d_{1a} = \left\{ \begin{array}{ll} 0 , & 0 < \omega t < \arcsin(\frac{1}{2M}) \\ 2M \sin(\omega t) - 1 , & \arcsin(\frac{1}{2M}) < \omega t < \pi - \arcsin(\frac{1}{2M}) \\ 0 , & \pi - \arcsin(\frac{1}{2M}) < \omega t < 2\pi \end{array} \right\} \quad (2.20)$$

$$d_{2a} = \left\{ \begin{array}{ll} 2M \sin(\omega t) , & 0 < \omega t < \arcsin(\frac{1}{2M}) \\ 1 , & \arcsin(\frac{1}{2M}) < \omega t < \pi - \arcsin(\frac{1}{2M}) \\ 2M \sin(\omega t) , & \pi - \arcsin(\frac{1}{2M}) < \omega t < \pi + \arcsin(\frac{1}{2M}) \\ 0 , & \pi + \arcsin(\frac{1}{2M}) < \omega t < 2\pi \end{array} \right\} \quad (2.21)$$

$$d_{3a} = \left\{ \begin{array}{ll} 1 , & 0 < \omega t < \pi \\ 2M \sin(\omega t) + 1 , & \pi < \omega t < \pi + \arcsin(\frac{1}{2M}) \\ 0 , & \pi + \arcsin(\frac{1}{2M}) < \omega t < 2\pi - \arcsin(\frac{1}{2M}) \\ 2M \sin(\omega t) + 1 , & 2\pi - \arcsin(\frac{1}{2M}) < \omega t < 2\pi \end{array} \right\} \quad (2.22)$$

$$d_{4a} = \left\{ \begin{array}{ll} 0 , & 0 < \omega t < \pi + \arcsin(\frac{1}{2M}) \\ 2M \sin(\omega t) + 2 , & \pi + \arcsin(\frac{1}{2M}) < \omega t < 2\pi - \arcsin(\frac{1}{2M}) \\ 0 , & 2\pi - \arcsin(\frac{1}{2M}) < \omega t < 2\pi \end{array} \right\} \quad (2.23)$$

For the b and c phase, the duty cycles are the same as in Eq. (2.15)-(2.23) only shifted $-2\pi/3$ and $-4\pi/3$ respectively.

By using the expressions for the duty cycles, a simplified implementation of the modulation method in a digital control system is obtained. The duty cycle values can be used directly in the PWM units of a DSP.

It should be noted that duty cycle calculations as presented here, can be easily performed for control voltages with third harmonic injection to increase the modulation depth, or any kind of added common mode voltage.

Output waveforms for the CBPWM strategies are shown in Figure 2.10-Figure 2.12 for $M=0.8$. The different voltages simulated, are as indicated in Figure 2.4, which shows the simplified converter model.

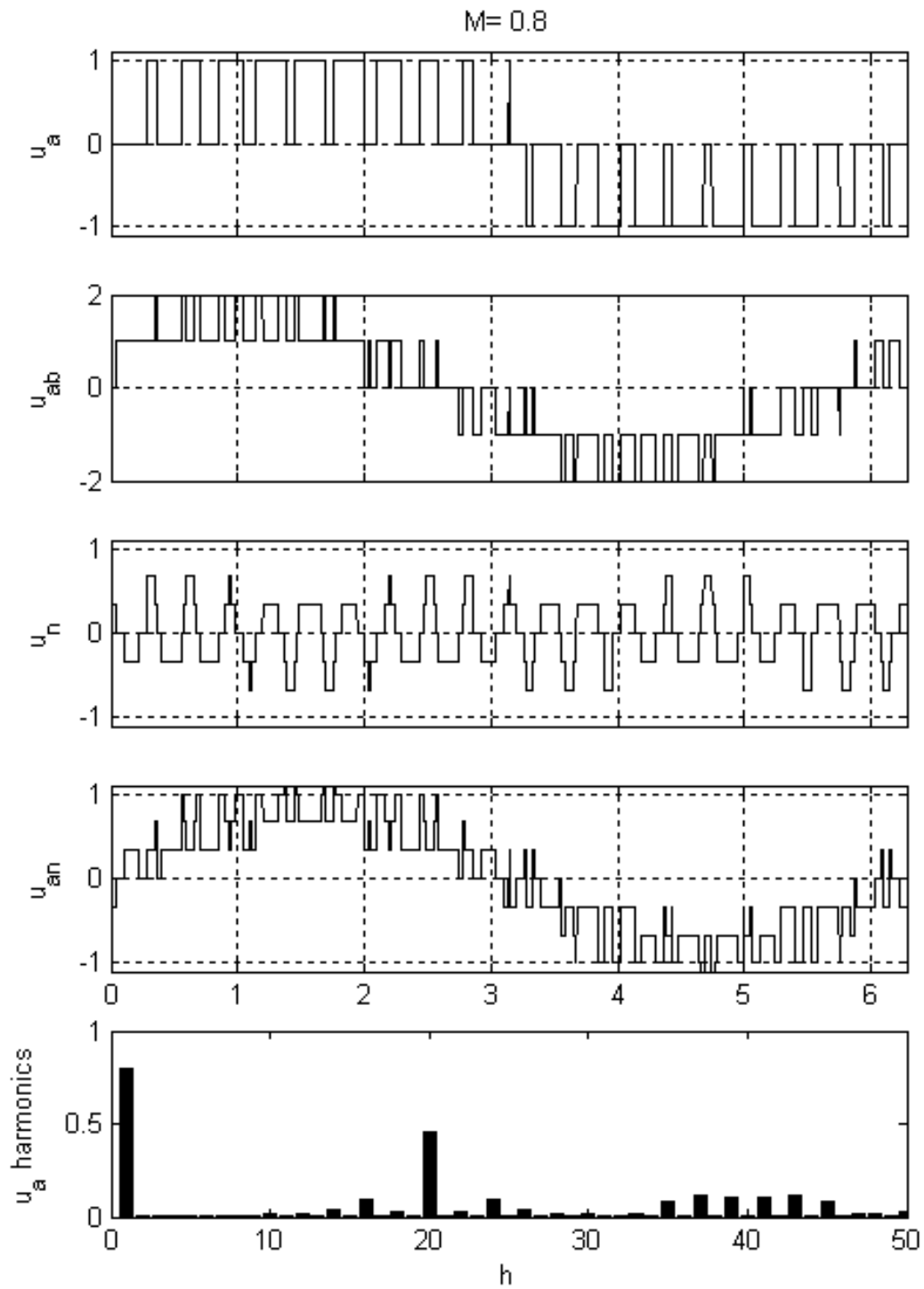


Figure 2.10: CBPWM output waveforms for a 3-level converter.

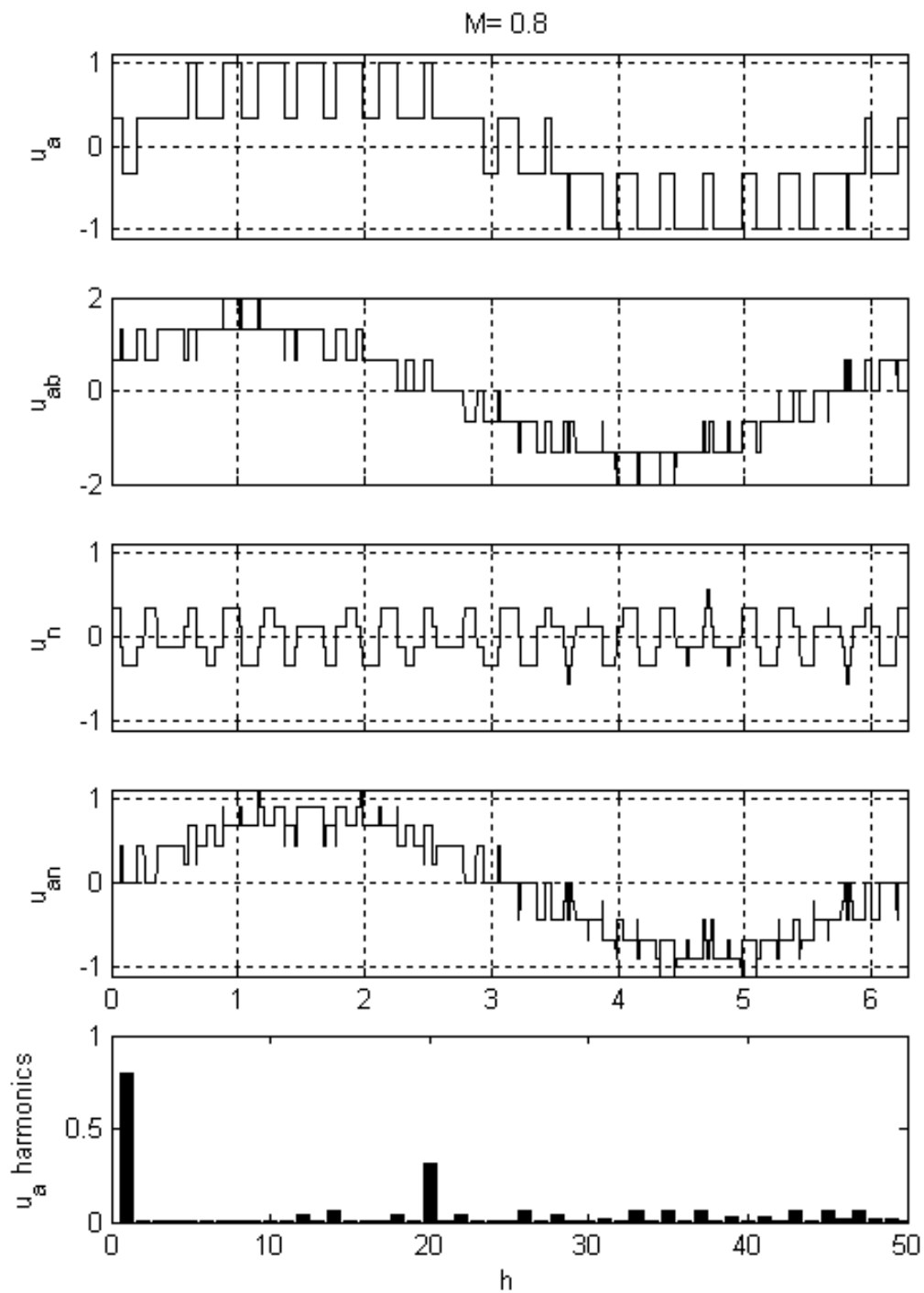


Figure 2.11: CBPWM output waveforms for a 4-level converter.

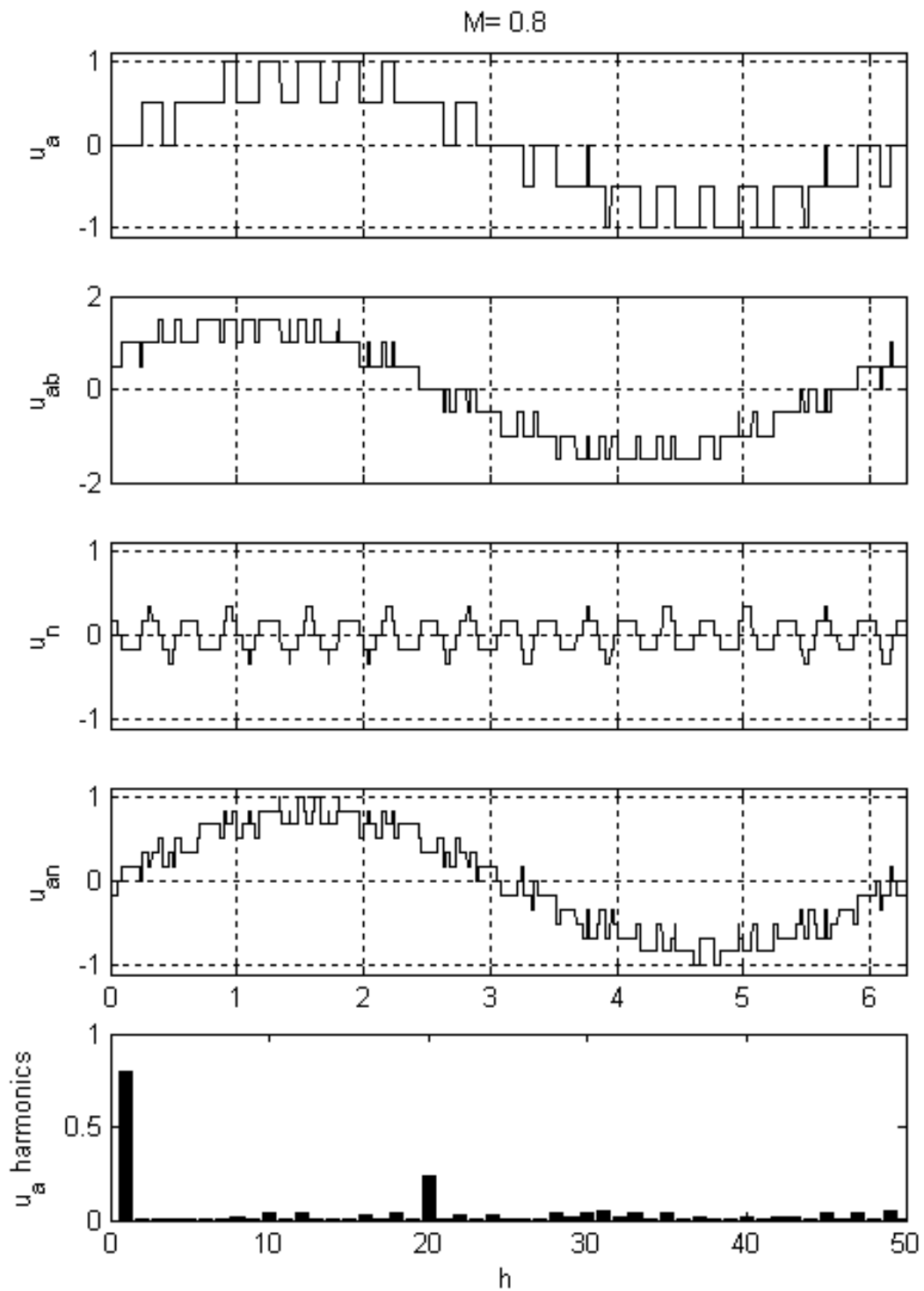


Figure 2.12: CBPWM output waveforms for a 5-level converter.

2.3.2 Space Vector PWM

As for all the others modulation strategies presented in this thesis, the Space Vector PWM (SVPWM) for multilevel converters evolves from modulation schemes for 2-level converters. [35] gives a nice overview of modulation strategies for this converter topology. In the last 20 years, numerous SVPWM strategies have been proposed for the 2-level converter. In the last 10 years, several SVPWM for multilevel converters has been proposed. The popularity of the SVPWM strategy is because of the direct digital implementation in today's DSP-based control systems [35]. Other advantages are lower harmonic distortion, and extended modulation depth compared to classical sinusoidal PWM modulation.

In a three-phase n -level converter, the number of available switch combinations is given by:

$$n_{uout} = n^3 \quad (2.24)$$

For a 2-level converter this yields 8 combinations, for the 3-level 27 combinations and so on. Figure 2.13 shows a comparison of the output vector-space for different levels.

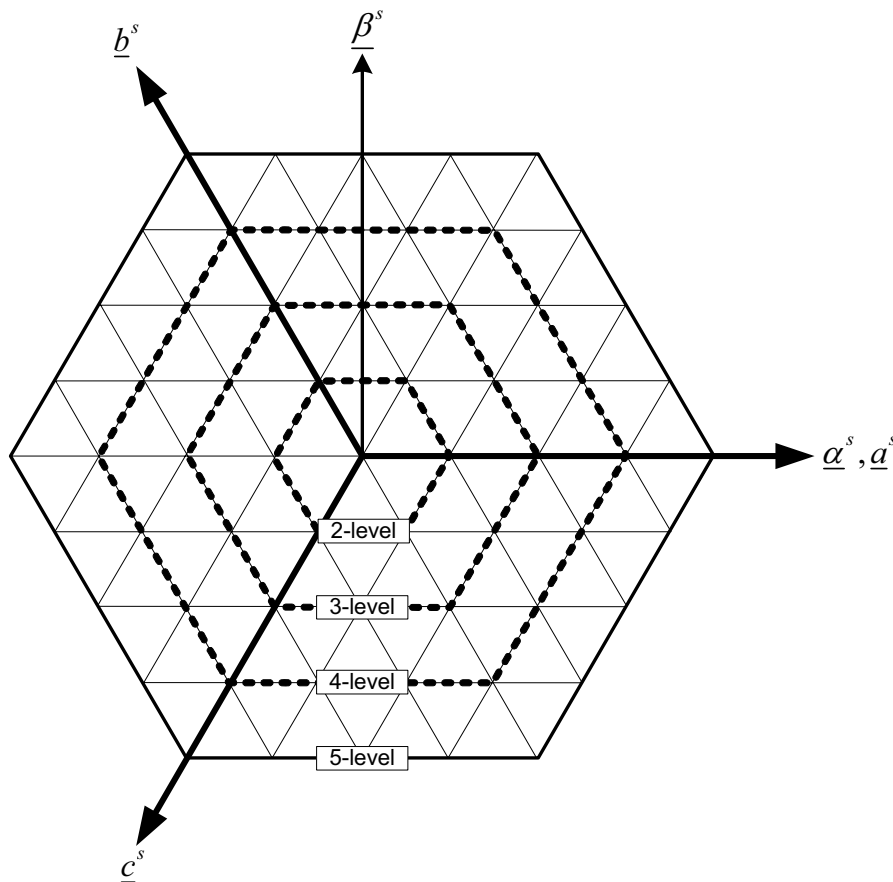


Figure 2.13: Comparison of the respective output vector-spaces for multilevel converters.

3-level Space Vector PWM

It should be noted that some of the switching combinations are redundant, two or more switch combinations gives the same output voltage vector. It's well known that only 7 different voltage vectors are available in a 2-level topology. For the 3-level converter the number of different voltage vectors is 18. Figure 2.14 shows the vector-space for a 3-level converter with redundant states. P and N denote the upper and lower DC-bus respectively. Neutral point connection is denoted with 0 .

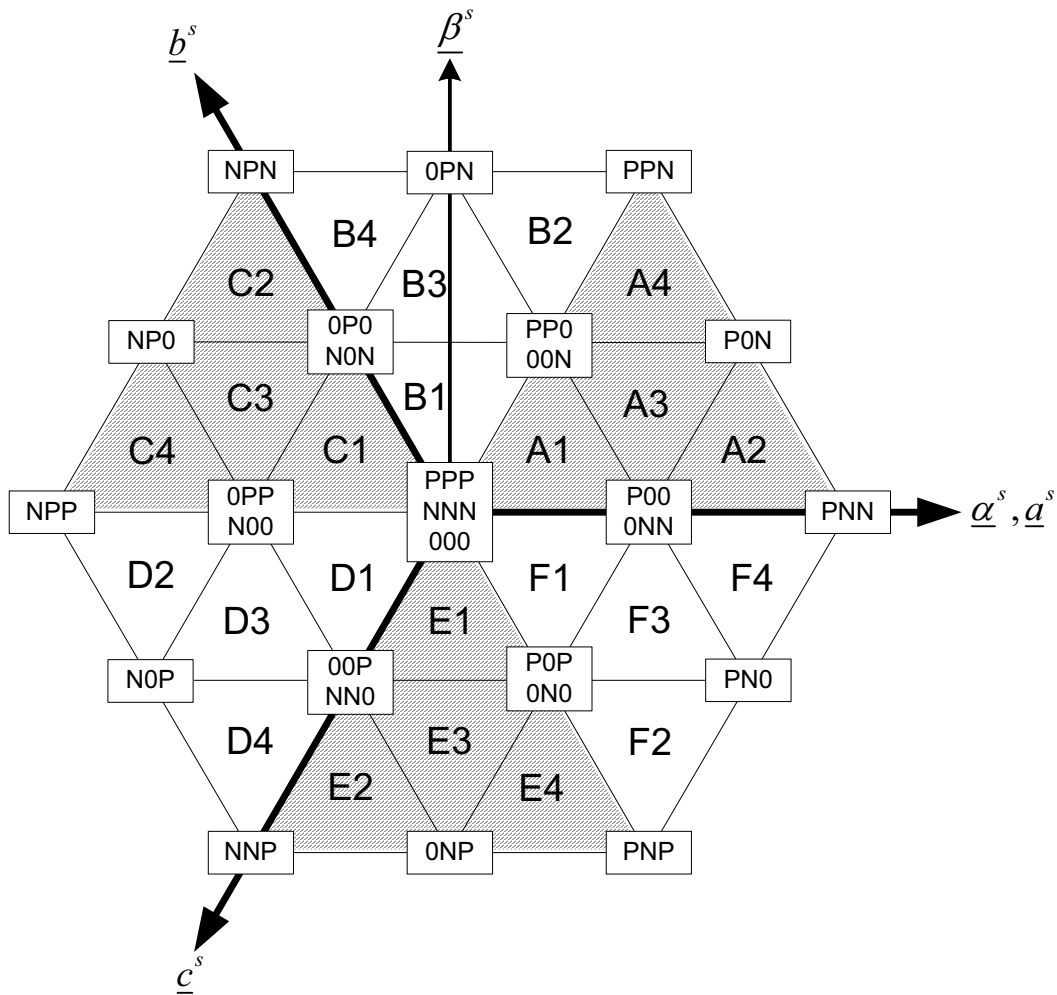


Figure 2.14: Space vector diagram of a 3-level converter.

Available vectors can be divided into four groups (Figure 2.15): Zero vectors as \underline{U}_0 , Small vectors as \underline{U}_{S1} and \underline{U}_{S2} , Medium vectors as \underline{U}_M , and Large vectors as \underline{U}_{L1} and \underline{U}_{L2} :

$$\begin{aligned}
 \underline{U}_0 &= 0 & \underline{U}_{S1} &= \frac{U_{dc}}{3} & \underline{U}_{S2} &= \frac{U_{dc}}{3} e^{j\frac{\pi}{3}} \\
 \underline{U}_M &= \frac{U_{dc}}{\sqrt{3}} e^{j\frac{\pi}{6}} & \underline{U}_{L1} &= \frac{2U_{dc}}{3} & \underline{U}_{L2} &= \frac{2U_{dc}}{3} e^{j\frac{\pi}{3}}
 \end{aligned} \tag{2.25}$$

The reference vector is defined as:

$$\underline{U}_{s,ref}^s = \frac{U_{dc}}{\sqrt{3}} M_s e^{j\zeta_s^s} \quad (2.26)$$

where M_s is the SVPWM modulation index. It can be shown that the relationship between the CBPWM modulation factor M , and M_s is:

$$M = \frac{2}{\sqrt{3}} M_s \approx 1.15 M_s \quad (2.27)$$

Hence, the DC-bus utilization is 15% better for SVPWM compared to sinusoidal CBPWM.

Calculation of duty cycles

Figure 2.15 shows sector A of a 3-level vector space. From Figure 2.15, the duty cycles can be found for the respective vectors from voltage/time balance during one switching period T_{sw} .

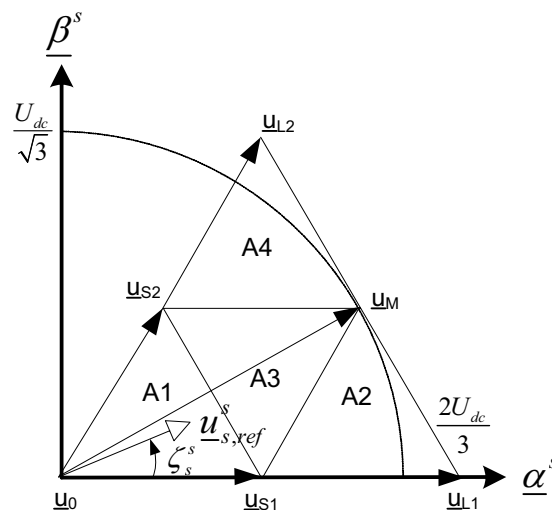


Figure 2.15: Switching vectors in sector A.

In triangle $A1$, two small vectors and one zero vector are used. From voltage/time balance we have:

$$T_{sw} \underline{U}_{s,ref}^s = T_{sw} (d_0 \underline{U}_0 + d_{s1} \underline{U}_{s1} + d_{s2} \underline{U}_{s2}) \quad (2.28)$$

$$T_{sw} \frac{U_{dc}}{\sqrt{3}} M_s e^{j\zeta_s^s} = T_{sw} U_{dc} (d_0 \underline{0} + d_{s1} \frac{1}{3} + d_{s2} \frac{1}{3} e^{j\frac{\pi}{3}}) \quad (2.29)$$

Decomposed into real- and imaginary quantities gives:

$$\frac{1}{\sqrt{3}} \cos(\zeta_s^s) = (d_{s1} \frac{1}{3} + d_{s2} \frac{1}{6}) \quad (2.30)$$

$$\frac{1}{\sqrt{3}} \sin(\zeta_s^s) = (d_{S1} \frac{1}{3} + d_{S2} \frac{1}{2\sqrt{3}}) \quad (2.31)$$

For the real and imaginary part respectively. The sum of the vector durations must sum up to the total switching period:

$$\begin{aligned} T_{sw}(d_0 + d_{S1} + d_{S2}) &= T_{sw} \\ d_0 + d_{S1} + d_{S2} &= 1 \end{aligned} \quad (2.32)$$

This gives the duty cycles in triangle $A1$:

$$d_{S1} = M_s(\sqrt{3} \cos(\zeta_s^s) - \sin(\zeta_s^s)), \quad d_{S2} = 2M_s \sin(\zeta_s^s), \quad d_0 = 1 - d_{S1} - d_{S2} \quad (2.33)$$

In triangle $A2$, one small-, one medium- and one large vector are used:

$$T_{sw} \underline{U}_{s,ref}^s = T_{sw} (d_{S1} \underline{U}_{S1} + d_{L1} \underline{U}_{L1} + d_M \underline{U}_M) \quad (2.34)$$

$$T_{sw} \frac{U_{dc}}{\sqrt{3}} M_s e^{j\zeta_s^s} = T_{sw} U_{dc} (d_{S1} \frac{1}{3} + d_{L1} \frac{2}{3} + d_M \frac{1}{\sqrt{3}} e^{j\frac{\pi}{6}}) \quad (2.35)$$

Using the same methods as for triangle $A1$, the duty cycles are:

$$d_M = 2M_s \sin(\zeta_s^s), \quad d_{L1} = -1 + M_s(\sqrt{3} \cos(\zeta_s^s) + \sin(\zeta_s^s)), \quad d_{S1} = 1 - d_M - d_{L1} \quad (2.36)$$

In triangle $A3$, two small vectors and one medium vector is utilized:

$$T_{sw} \underline{U}_{s,ref}^s = T_{sw} (d_{S1} \underline{U}_{S1} + d_{S2} \underline{U}_{S2} + d_M \underline{U}_M) \quad (2.37)$$

$$T_{sw} \frac{U_{dc}}{\sqrt{3}} M_s e^{j\zeta_s^s} = T_{sw} U_{dc} (d_{S1} \frac{1}{3} + d_{S2} \frac{1}{3} e^{j\frac{\pi}{3}} + d_M \frac{1}{\sqrt{3}} e^{j\frac{\pi}{6}}) \quad (2.38)$$

Again, using the same methods as for triangle $A1$, the duty cycles are:

$$d_{S1} = 1 - 2M_s \sin(\zeta_s^s), \quad d_{S2} = 1 + M_s(\sin(\zeta_s^s) - \sqrt{3} \cos(\zeta_s^s)), \quad d_m = 1 - d_{S1} - d_{S2} \quad (2.39)$$

Triangle $A4$ is similar to triangle $A2$, utilizing one small, one medium and one large vector:

$$T_{sw} \underline{U}_{s,ref}^s = T_{sw} (d_{S2} \underline{U}_{S2} + d_M \underline{U}_M + d_{L1} \underline{U}_{L2}) \quad (2.40)$$

$$T_{sw} \frac{U_{dc}}{\sqrt{3}} M_s e^{j\zeta_s^s} = T_{sw} U_{dc} (d_{S2} \frac{1}{3} e^{j\frac{\pi}{3}} + d_M \frac{1}{\sqrt{3}} e^{j\frac{\pi}{6}} + d_{L2} \frac{2}{3} e^{j\frac{\pi}{3}}) \quad (2.41)$$

Again, using the same methods as for triangle $A1$, the duty cycles are:

$$\begin{aligned} d_{S2} &= 2 + M_s(\sqrt{3} \cos(\zeta_s^s) - \sin(\zeta_s^s)), \quad d_M = M_s(\sqrt{3} \cos(\zeta_s^s) - \sin(\zeta_s^s)) \\ d_{L2} &= 1 - d_M - d_{S2} \end{aligned} \quad (2.42)$$

The duty cycles for the other sectors (B, D, E, F, G) are exactly the same, except for $\zeta_s^s = \zeta_s^{s'}$. Where $\zeta_s^{s'}$ is the angle with respect to the closest \underline{U}_{LI} -axis.

Finding the triangle number k

For a 2-level converter, finding one of the six sectors is trivial, since the sector borders are only dependent on the reference angle ζ_s^s . For a 3-level converter the problem is more complicated. In [37], the problem is solved by simplification of the vector space into a 2-level vector space which is moved around in the 3-level space by applying offsets to the origin. In [36] the solution is done by a coordinate transform of the reference axis.

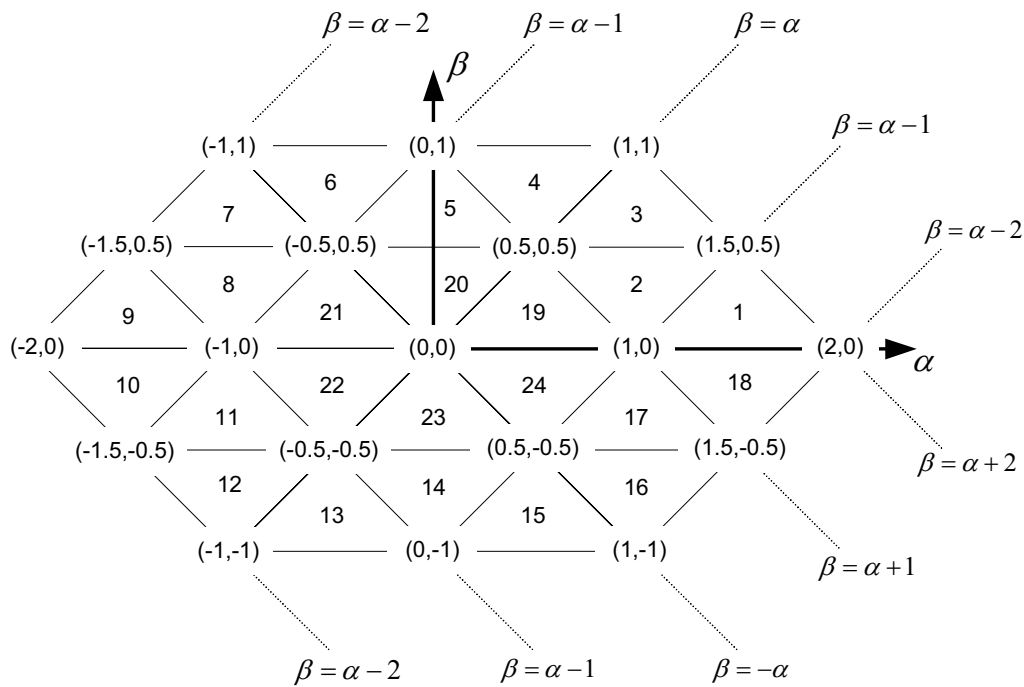


Figure 2.16: Transformed vectorspace with triangle numbers.

Another solution is presented here, and instead of changing the reference axis, the vector-space is transformed by transforming the coordinates of the vector space by a factor of $(1, \sqrt{3})/3U_{dc}$ as shown in Figure 2.16. By this, a simpler set of coordinates for the corners of the triangles are found. Also, the reference voltage is transformed.

Defining that the left corner of each triangle is always A (a_α, a_β), the right corner B (b_α, b_β) and either the upper or lower corner C (c_α, c_β). As can be seen from the transformed vector space only the coordinates for A (a_α, a_β) have to be found, since corner B and the α -component to corner C is fixed in position with respect to A. The β -component to corner C can be found from the sign of the β -component of the reference voltage. To find the corresponding coordinates, the following calculation has to be done:

```

i=1; while (i-1>-uα+uβ) i=i-1;
j=-2; while (j+1< uα+uβ) j=j+1;

```

Where i and j are integers $[-2..2]$, and u_α and u_β are the real and imaginary components of the transformed reference voltage, respectively. The coordinates of the A corner is then found from the intersection of the straight lines $\beta = \alpha + 1$ and $\beta = -\alpha + j$:

$$a_\alpha = \frac{1}{2}(j-i), \quad a_\beta = \frac{1}{2}(i+j), \quad b_\alpha = a_\alpha + 1, \quad b_\beta = a_\beta, \quad c_\alpha = a_\alpha + \frac{1}{2} \quad (2.43)$$

Depending on the sign of u_β , the final c_β is:

$$c_\beta = a_\beta + \frac{\text{sign}(u_\beta)}{2} \quad (2.44)$$

Hence, the triangle for the reference voltage vector is located. Figure 2.17 shows a result from a simulation displaying the triangle number for the reference vector at modulation depth $M=0.8/M_s=0.693$. When the location of the reference vector is found, there exist several ways of arranging the different output switching vectors of the converter. As for 2-level SVPWM [35] there exist a variety of different SVPWM methods for the 3-level topology. Because of the large number of available switching states, the configurations are numerous. Figure 2.18 shows one way of placing the different output vectors in sector A of the vector space. This method is presented in [34]. As will be shown in Chapter 7, this method is very useful for balancing of the DC-bus voltages. Figure 2.19 shows a simulation where the output waveforms are displayed for the SVPWM method described. The 3.harmonic component in the phase-leg voltage is caused by the modulation strategy, and will be cancelled in the load phase voltages and line-line voltages.

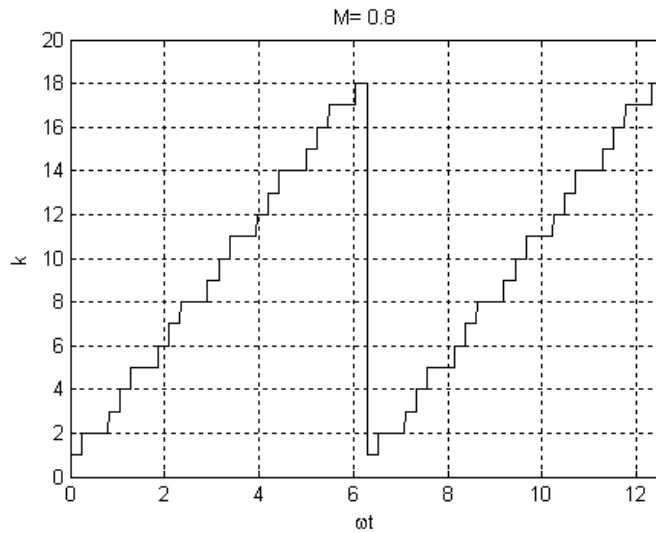


Figure 2.17: Triangle (k) selection at $M=0.8$.

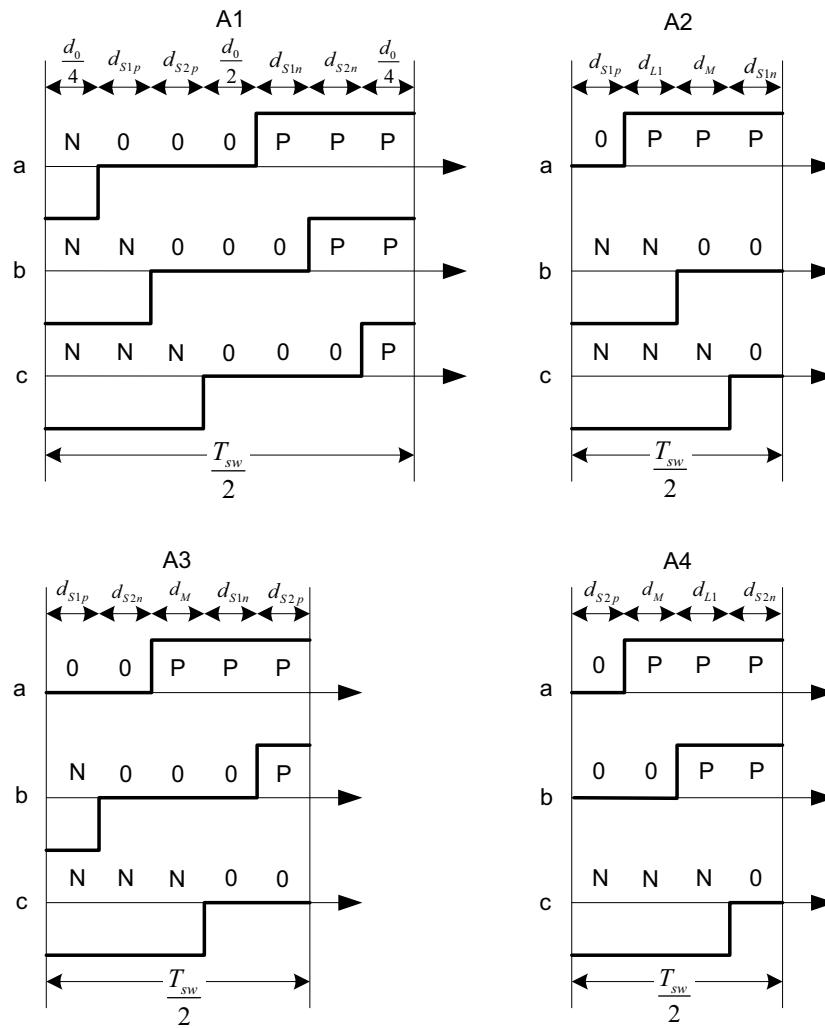


Figure 2.18: Vector placement for SVPWM in Sector A.

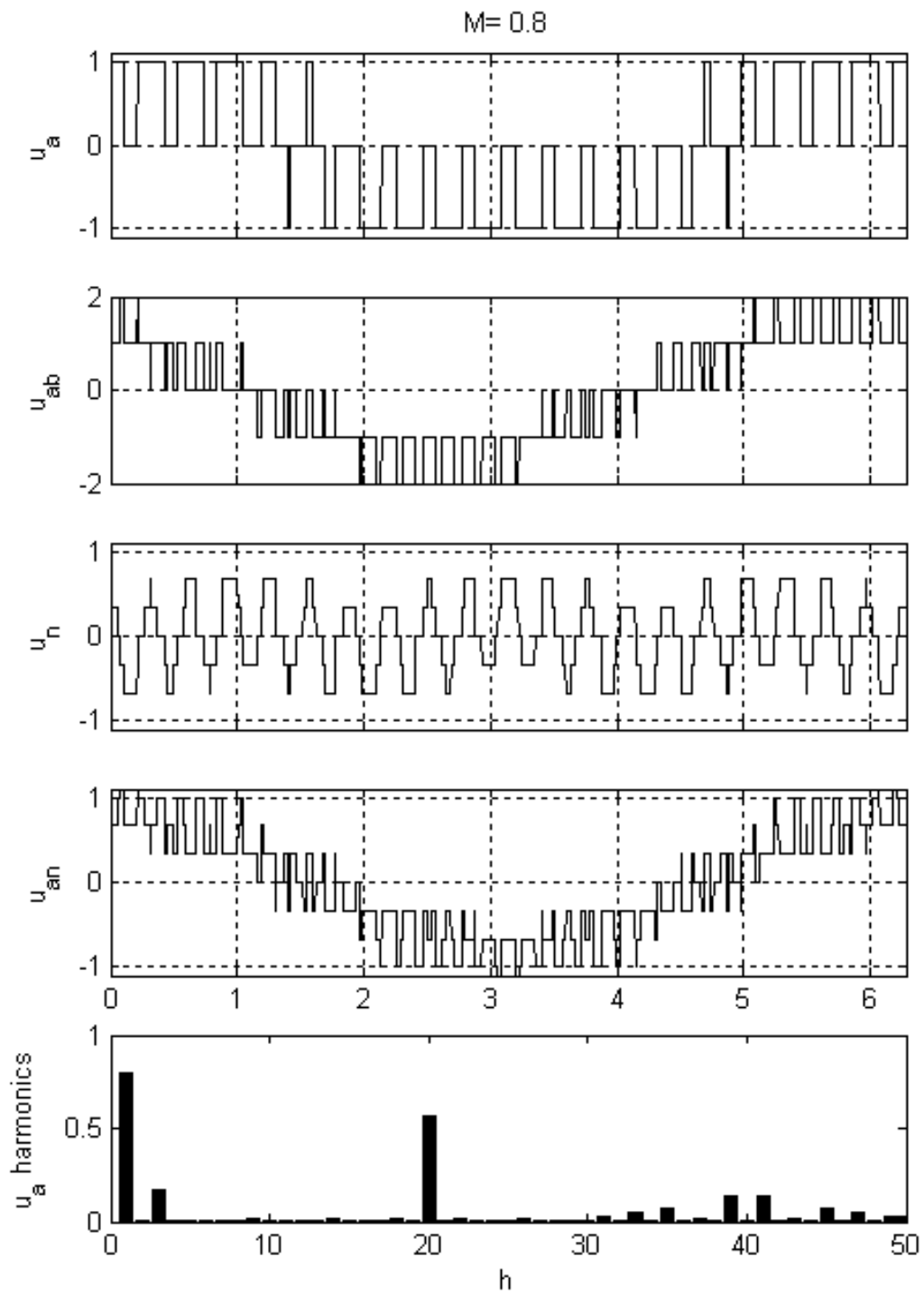


Figure 2.19: Output waveform for 3-level SVPWM.

2.4 Carrier Based PWM vs. Space Vector PWM for MLC

Space Vector PWM (SVPWM) gives a direct calculation of the duty cycles for the switches. In Carrier Based PWM (CBPWM), the duty cycles can be derived from the control signals as shown in Chapter 2.3.1 and visualized in Figure 2.9. From this, it is clear that the corresponding control signals for Space Vector PWM can be found from the duty cycles. When comparing SVPWM and CBPWM it is convenient to write the control signals for sinusoidal modulation as:

$$\begin{aligned} u_{sta}(t) &= M \cos(\omega t) \\ u_{stb}(t) &= M \cos(\omega t - 2\pi / 3) \\ u_{stc}(t) &= M \cos(\omega t + 2\pi / 3) \end{aligned} \quad (2.45)$$

This corresponds to $\omega t = \zeta_s^s$ in Figure 2.15. When $\omega t = 0$, the control signal in the a-phase in Eq.(2.45) is at it's maximum.

2-level SVPWM

For 2-level SVPWM it is well known that the corresponding control signals are [35]:

$$u'_{stj}(t) = u_{stj}(t) + u_{com1}(t) \quad (2.46)$$

Where $j=a, b, c$ and the common term introduced is:

$$u_{com1}(t) = -\frac{1}{2} [\max(u_{sta}, u_{stb}, u_{stc}) + \min(u_{sta}, u_{stb}, u_{stc})] \quad (2.47)$$

By employing these control signals, the nearest three switching vectors are used in one switching cycle and the active switching vectors will be centred in the switching period, as in Space Vector PWM. In Figure 2.20, the modified control signal for phase a is plotted for three different modulation indexes.

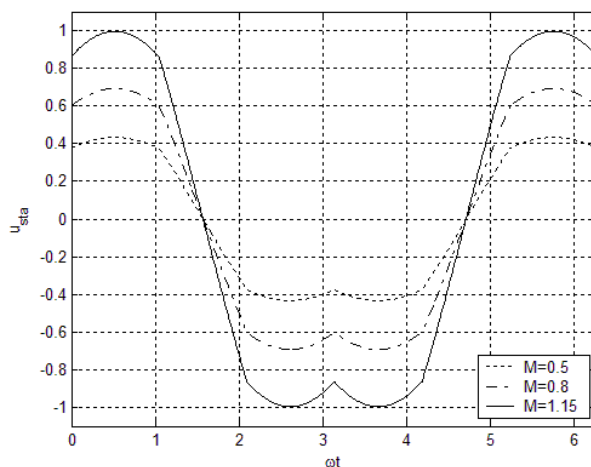


Figure 2.20: a-phase control signals for 2-level SVPWM.

3-level SVPWM

For a 3-level converter, the problem of finding the corresponding control signals is more difficult since the vector space is rather complicated. In [38] a solution is presented based on the calculations from the duty cycles in each of the triangles in the vector space. In [38] a solution is presented based on the calculations from the duty cycles in each of the triangles in the vector space. [39] introduce a set of control voltages which are simplified in comparison to [38]. They also show that by employing Eq.(2.46) for multilevel modulation, the active switching vectors will not be centred, and thus not optimal. The control voltages are as follows:

$$u_{stj}''(t) = \left[u_{stj}'(t) + u_{com1}(t) + 1 \right] \bmod \left(\frac{2}{n-1} \right) \quad (2.48)$$

Where $u_{stj}'(t)$ and $u_{com1}(t)$ are as in Eq. (2.45) and (2.47), and n is the number of levels. This is to identify which of the control signals which are responsible for the first and last transaction in each switching period. An additional common mode signal has to be introduced to position the first and last switching transition:

$$u_{com2}(t) = \frac{1}{n-2} - \frac{1}{2} \left[\max(u_{sta}'', u_{stb}'', u_{stc}'') + \max(u_{sta}'', u_{stb}'', u_{stc}'') \right] \quad (2.49)$$

Finally, the signals in Eq.(2.46) and (2.49) are added together with the original control signals to obtained the modified control signals:

$$u_{stj}'''(t) = u_{stj}'(t) + u_{stj}''(t) + u_{com2}(t) \quad (2.50)$$

This set of control signals coincide with those obtained in [38] for 3-level modulation. They are also the same as the Switching Frequency Optimal PWM (SFO PWM) strategy presented in [40] and [41] by Steinke.

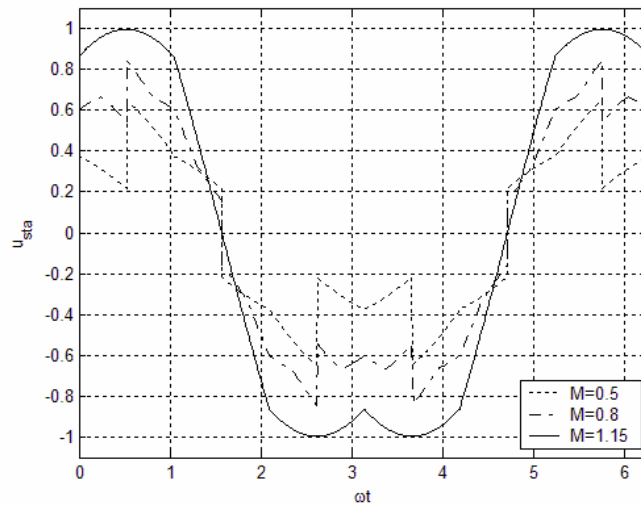


Figure 2.21: a-phase control signals for 3-level SVPWM.

Figure 2.21 shows the modified control signal for phase a for three different modulation indexes. From the figure, it can be observed that for $M=2/\sqrt{3}\approx 1.15$ (maximum modulation index), the 3-level control signals coincide with the modified signals for 2-level SVPWM. As will be shown in Chapter 6.4, the SVPWM method presented here shows better harmonic performance for lower modulation indexes than Sinusoidal PWM and Sinusoidal PWM with 3rd harmonic injection.

3 ANALYTICAL LOSS CALCULATIONS

When designing a converter it is useful to have analytical formulas to calculate electrical stresses in the switching devices at different loading. This chapter is based on a method presented in [42] and [43]. The method calculates the discontinuous currents in Pulse Width Modulated (PWM) converters with high switching frequency. The method transforms discontinuous currents or voltages to continuous, which are almost similar with respect to power losses. In [42] and [43], a 2-level converter is analyzed. In [44], the calculations for a 3-level converter can be found. This chapter gives a deduction of the losses in 4- and 5-level converters, and some of the theory is also presented in [46].

By using analytical expressions, time consuming time domain simulations are avoided, and comparison between different topologies and switching devices can be done efficiently.

3.1 Analytically Method for Calculating Discontinuous Currents

The method samples the discontinuous current or voltage within a switching interval, T_{sw} , and transforms it into a continuous microscopic mean or RMS signal (Figure 3.1). By integrating the continuous microscopic mean or RMS signal over a switching period, a good approximation of the actual mean and RMS value is obtained, which is the macroscopic value. When the switching frequency is high (typical > 10 times fund.), the current shape in one switching interval is almost linear, and the error will be small. The error will decrease with increasing switching frequency. Eq. (3.1) shows the expressions for these values:

$$i_{T,avg} = \frac{1}{T_{sw}} \int_{-d(\tau)\frac{T_{sw}}{2}}^{d(\tau)\frac{T_{sw}}{2}} i_T(\tau) d\tau = d(\tau)i_T(\tau), \quad i_{T,rms}^2 = \frac{1}{T_{sw}} \int_{-d(\tau)\frac{T_{sw}}{2}}^{d(\tau)\frac{T_{sw}}{2}} i_T^2(\tau) d\tau = d(\tau)i_T^2(\tau) \quad (3.1)$$

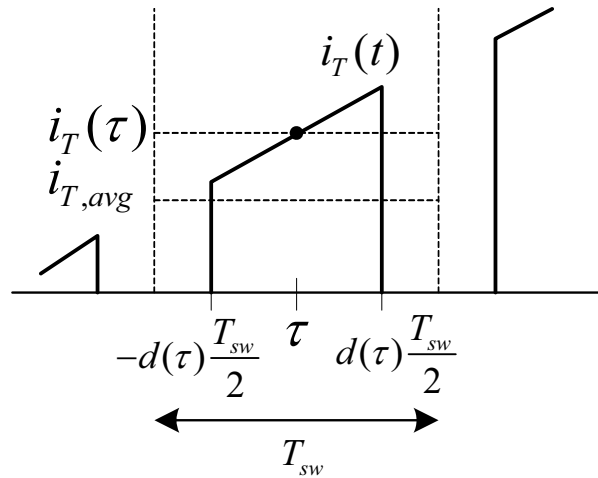


Figure 3.1: Switching waveform through device during one switching period, T_{sw} .

3.1.1 Modelling the conducting losses

The forward conducting properties in semiconductors can be approximated by a forward voltage drop, U_{f0} , and an ohmic resistance, r_f , in series with the forward voltage:

$$U_f(t) = U_{f0} + r_f \cdot I(t) \quad (3.2)$$

Figure 3.2 (left) shows a typical forward characteristic for a 1200V/200A IGBT from Semikron. To the right is shown an illustration of the approximated characteristic.

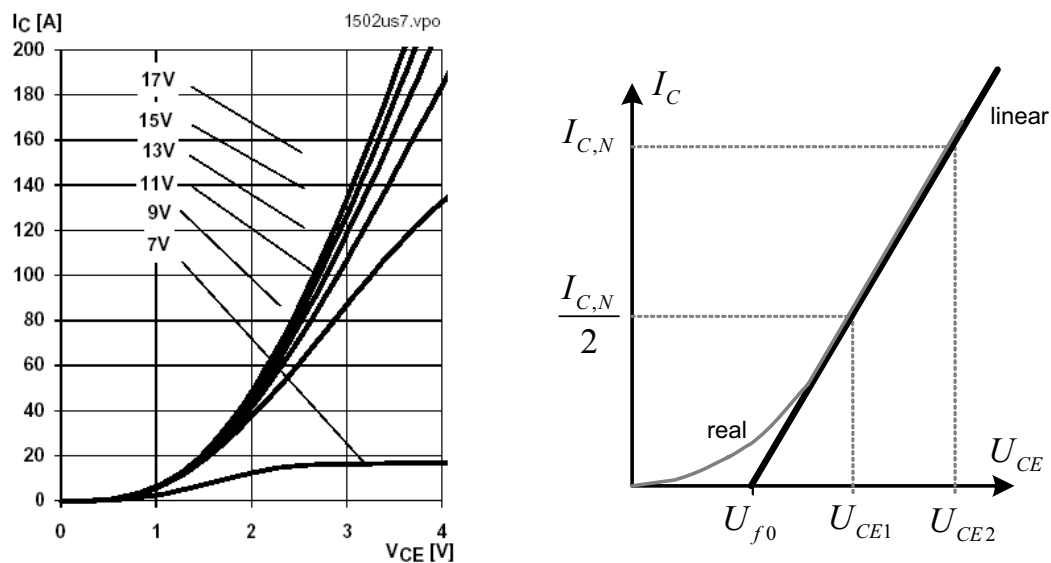


Figure 3.2: Forward voltage drop characteristic for a switching device. Left: SKM200GB123D IGBT. Right: Linear approximation.

U_{CE2} and U_{CE1} are the voltage across the device at rated current $I_{C,N}$ and half the rated current respectively. From this, the static forward voltage U_{f0} can be expressed as:

$$U_{f0} = 2U_{CE1} - U_{CE2} \quad (3.3)$$

r_f can be found from:

$$r_f = 2 \frac{U_{CE2} - U_{CE1}}{I_{C,N}} \quad (3.4)$$

Thus, the conducting losses will be:

$$P_c = \frac{1}{T_p} \int_{T_p} U_f(t) \cdot I(t) dt \quad (3.5)$$

T_p is the duration of the fundamental period. Inserting Eq.(3.2) and recognizing the formulas for mean and RMS value of the discontinuous current gives:

$$P_c = U_{f0} \cdot I_{avg} + r_f \cdot I_{rms}^2 \quad (3.6)$$

Where:

$$I_{avg} = \frac{1}{T_p} \int_{T_p} I(t) dt \quad , \quad I_{rms}^2 = \frac{1}{T_p} \int_{T_p} I(t)^2 dt \quad (3.7)$$

3.1.2 Modelling the switching losses

Because of the non-ideal behaviour of today's high power semiconductor devices such as the IGBT there will be switching losses at both turn-on and turn-off in hard switching converter topologies. This is caused by the non-instantaneous rise/fall in the current/voltage in the device. Figure 3.3 shows typical device waveforms at switching. The over-shoot in the current at turn-on is caused by the reverse recovery of the freewheeling diode commutating through the IGBT. The over-shoot in the voltage at turn-off is caused by the leakage-inductance in the switching circuit [45]. At turn-on both the dv/dt and id/dt can be controlled by changing the gate resistance of the driver. Decreasing the gate resistance increases the dv/dt and di/dt , hence lower losses is obtained. As the rise-time of the current increases, the peak current is increased. This means there is a trade-off many power electronics designers have to face. At turn-off the current can no longer be controlled completely by the gate resistance because of the bipolar behaviour of the IGBT. After the emitter current in the drift-zone has been turned off, a large number of majority carriers is still left in the drift zone. These p-charge carriers have to recombine or be reduced by re-injection (tail-current).

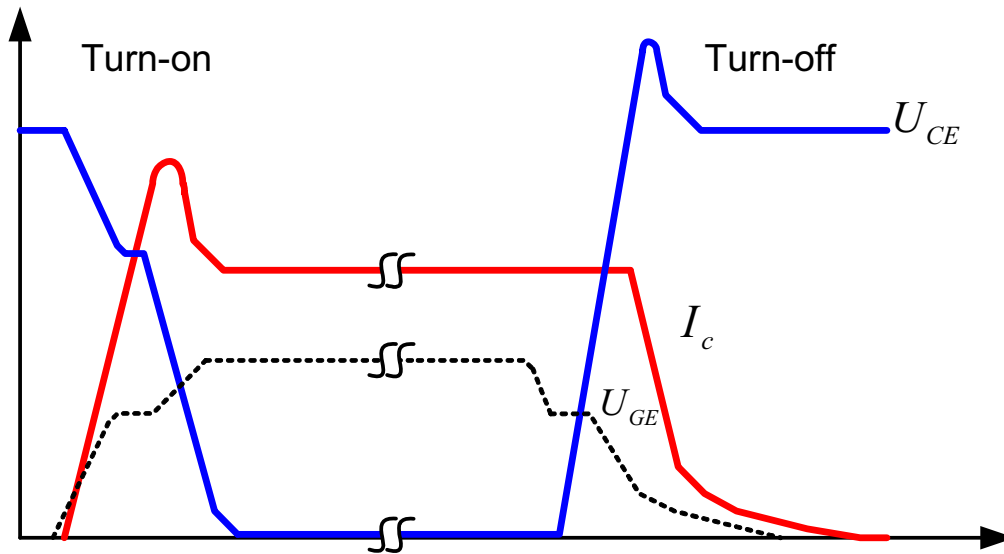


Figure 3.3: Typical turn-on and turn-off waveforms for an IGBT.

There exist a variety of ways to calculate the switching losses in a device. A widely used approach is to start with a measurement of the switching energy emitted for a given set of voltage, junction temperature, gate resistance etc. This characteristic is often given in component datasheets as shows in Figure 3.4 for the same IGBT as in Figure 3.2.

The switching energy as a function of the current can be approximated to have a parabolic shape:

$$E_{sw}(I) = U_{CE} [k_{1,T}I(t) + k_{2,T}I(I)^2] \quad (3.8)$$

where $k_{1,T}$ and $k_{2,T}$ are constants of proportionality to be decided from the datasheet. The switching energy can also be approximated to have a straight line shape ($k_{2,T} = 0$). U_{CE} is the voltage across the device when switching.

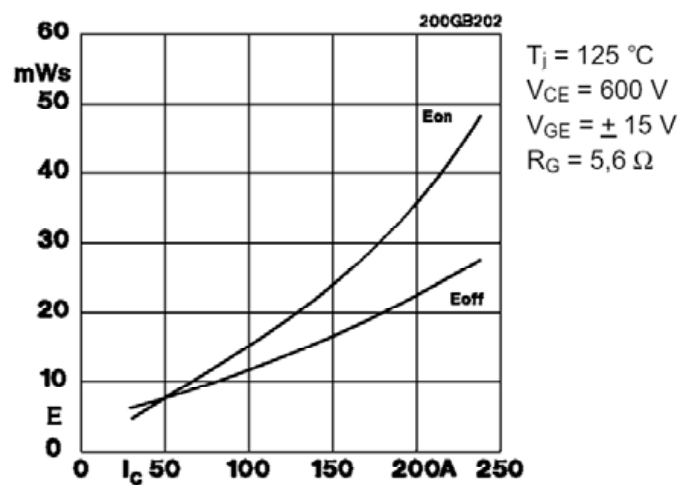


Figure 3.4: Switching losses for SKM200GB123D IGBT.

By this, an expression for the average switching losses in a device can be formed:

$$P_{sw,avg} = \frac{U_{dc}}{(n-1)} \frac{1}{2\pi} f_{sw} \int (k_{1,T}I(t) + k_{2,T}I(t)^2) d\omega t \quad (3.9)$$

where U_{dc} is the DC link voltage, n the number of levels, and f_{sw} is the switching frequency. The integral limits will depend on the instances where the respective components are switching. If this averaging is to be acceptable, the switching period, T_{sw} , must be less than the thermal time constant for the semiconductor.

As described, the switching losses are highly dependent on gate resistance and power circuit layout of the converter. The analytical expressions developed in this chapter are based on the given switching energy at the given parameters from the datasheets.

3.2 Switching Signals and Load Currents

This chapter's analytical loss calculations are based on the sinusoidal Carrier Based Pulse Width Modulation (CBPWM) presented in Chapter 3.3.

All the deviations in this chapter are based on pure sinusoidal load currents on the form:

$$\begin{aligned} i_a(t) &= \hat{I} \sin(\omega t - \varphi) \\ i_b(t) &= \hat{I} \sin(\omega t - 2\pi/3 - \varphi) \\ i_c(t) &= \hat{I} \sin(\omega t + 2\pi/3 - \varphi) \end{aligned} \quad (3.10)$$

3.3 3-level Converter

Figure 3.5 shows one phase-leg of a 3-level converter. This topology can produce 3 levels at the output with respect to the neutral point n . Table 3-1 shows the possible output voltages and the conducting devices for each switching state.

Table 3-1: Conducting devices in 3-level converter.

Switching state				$\frac{2u_{oj-n}}{U_{dc}}$	Conducting devices	
T_{1j+}	T_{2j+}	T_{1j-}	T_{2j-}		$i_j > 0$	$i_j < 0$
1	1	0	0	1	T_{1j+}, T_{2j+}	D_{1j+}, D_{2j+}
0	1	1	0	0	D_{1j}, T_{2j+}	D_{2j}, T_{1j-}
0	0	1	1	-1	D_{1j-}, D_{2j-}	T_{1j-}, T_{2j-}

Freewheeling diodes D_{1j+}, D_{2j+} share the same current, and thus, the same current shape. This also holds for D_{1j-}, D_{2j-} only shifted by 180° with respect to the upper

freewheeling diodes. Hence, these devices has the same losses. This is also observed for T_{1+} , T_{2-} , T_{2+} , T_{1-} and the clamping diodes D_{1j} and D_{2j} . An example from a KREAN simulation is shown in Figure 3.6.

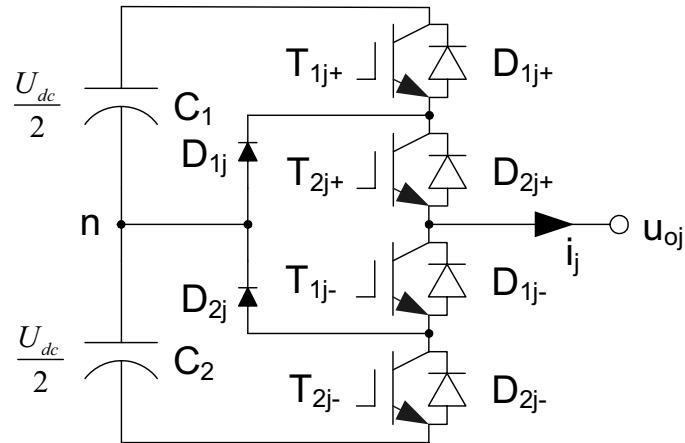


Figure 3.5: One phase leg of a 3-level converter.

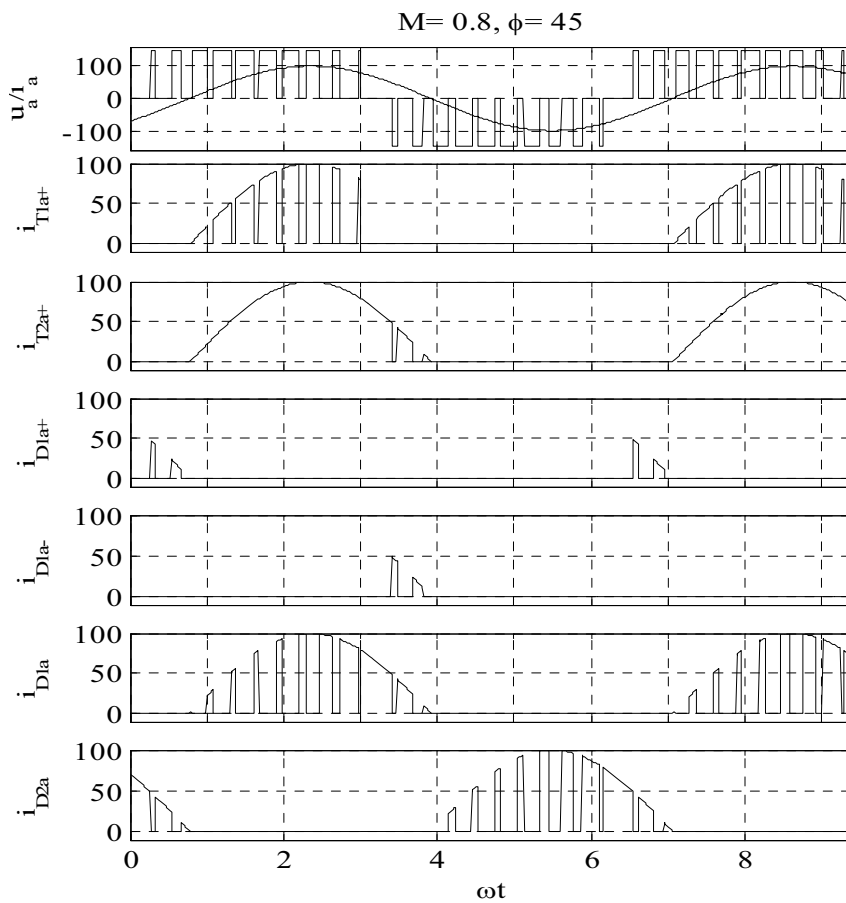


Figure 3.6: Typical output waveforms for 3-level converter simulated in KREAN.

In [44], the losses for the 3-level topology are calculated. For the switching losses the following equations apply:

$$P_{T1a+,sw} = \frac{U_{dc} f_{sw} \hat{I}}{4\pi} \left(k_{1,T} (1 + \cos \varphi) + \frac{1}{2} k_{2,T} \hat{I} \left(\frac{1}{2} \sin |2\varphi| + \pi - |\varphi| \right) \right) \quad (3.11)$$

$$P_{T2a+,sw} = \frac{U_{dc} f_{sw} \hat{I}}{4\pi} \left(k_{1,T} (1 - \cos \varphi) + \frac{1}{2} k_{2,T} \hat{I} \left(|\varphi| - \frac{1}{2} \sin |2\varphi| \right) \right) \quad (3.12)$$

$$P_{D1a+,sw} = \frac{U_{dc} f_{sw} \hat{I}}{4\pi} \left(k_{1,T} (1 - \cos \varphi) + \frac{1}{2} k_{2,T} \hat{I} \left(|\varphi| - \frac{1}{2} \sin |2\varphi| \right) \right) \quad (3.13)$$

$$P_{D1a+,sw} = \frac{U_{dc} f_{sw} \hat{I}}{4\pi} \left(2k_{1,T} + \frac{\pi}{2} k_{2,T} \hat{I} \right) \quad (3.14)$$

Eq. (3.11)-(3.14) apply for $-\pi < \varphi \leq \pi$.

The mean and RMS values of the currents have the following expressions, where $-\pi < \varphi \leq \pi$:

$$I_{T1a+,avg} = \frac{M\hat{I}}{4\pi} \left(\sin |\varphi| + (\pi - |\varphi|) \cos \varphi \right) \quad (3.15)$$

$$I_{T1a+,rms}^2 = \frac{M\hat{I}^2}{4\pi} \left(1 + \frac{4}{3} \cos \varphi + \frac{1}{3} \cos(2\varphi) \right) \quad (3.16)$$

$$I_{T2a+,avg} = \frac{\hat{I}}{4} - \frac{M\hat{I}}{4\pi} \left(\sin |\varphi| - |\varphi| \cos \varphi \right) \quad (3.17)$$

$$I_{T2a+,rms}^2 = \frac{\hat{I}^2}{4} - \frac{M\hat{I}^2}{4\pi} \left(1 - \frac{4}{3} \cos \varphi + \frac{1}{3} \cos(2\varphi) \right) \quad (3.18)$$

$$I_{D1a+,avg} = \frac{M\hat{I}_N}{4\pi} \left(\sin |\varphi| - |\varphi| \cos \varphi \right) \quad (3.19)$$

$$I_{D1a+,rms}^2 = \frac{M\hat{I}^2}{4\pi} \left(1 - \frac{4}{3} \cos \varphi + \frac{1}{3} \cos(2\varphi) \right) \quad (3.20)$$

$$I_{D1a+,avg} = \frac{\hat{I}}{\pi} - \frac{M\hat{I}}{4\pi} \left(\cos \varphi + \frac{2}{\pi} \sin |\varphi| - \frac{2}{\pi} |\varphi| \cos \varphi \right) \quad (3.21)$$

$$I_{D1a+,rms}^2 = \frac{\hat{I}^2}{4} - \frac{M\hat{I}^2}{2\pi} \left(1 + \frac{1}{3} \cos(2\varphi) \right) \quad (3.22)$$

3.4 4-level Converters

3.4.1 Topology and performance

Figure 3.7 shows one phase-leg of a 4-level converter. It consists of six switches in series. Ideally, the maximum voltage that will be applied to each switch under normal conditions is $1/3$ of the dc-link voltage U_{dc} .

Three capacitors are connected in series at the DC-link in order to partition the voltage into four voltage levels, thereby the name 4-level converter. Four clamp diodes are also introduced in each bridge leg as shown below to make a current path to the middle voltage levels. Table 3-2 summarizes the conducting devices for all the switching states.

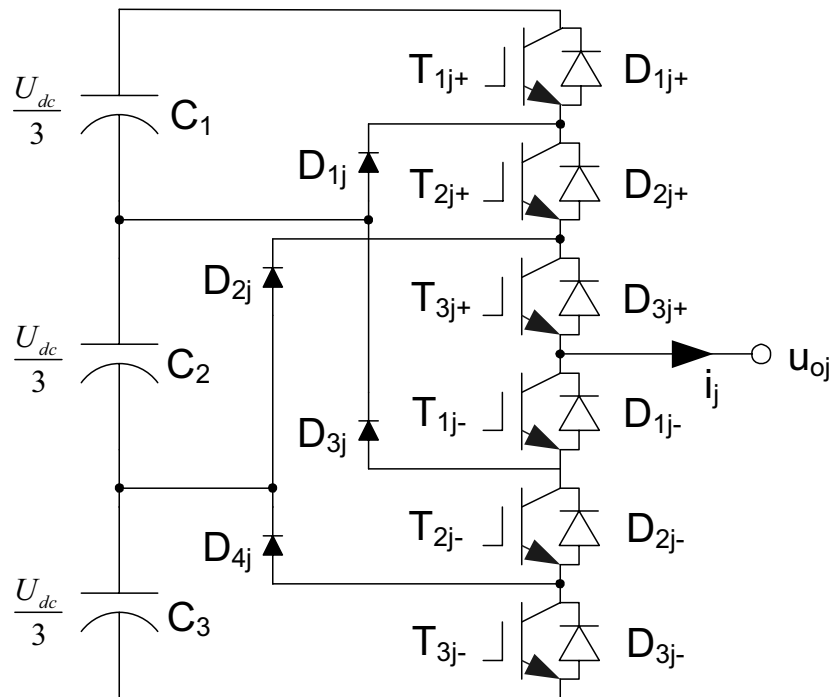


Figure 3.7: One phase leg of a 4-level converter.

Figure 3.7 shows the following: When the upper three switches are on, the clamping diode D_{2j} has to withstand a voltage of $2/3U_{dc}$. If devices with equal voltage rating are used, series connection is necessary. This is also true for D_{3j} when the three lower switches are on.

As shown in Table 3-2 the current waveform in D_{1j+} , D_{2j+} , D_{3j+} must be the same, this also applies for D_{1j-} , D_{2j-} , D_{3j-} , only shifted 180° . Hence, the losses are equal. Furthermore, from symmetry, the waveforms for T_{1j+}/T_{3j-} , T_{2j+}/T_{2j-} and T_{3j+}/T_{1j-} are the same, respectively, only shifted 180° . This also applies to D_{1j}/D_{4j} . Some of the current waveforms are shown in Figure 3.8 (KREAN simulation).

Table 3-2: Conducting devices in 4-level converter.

Switching state						$\frac{6u_{oj-n}}{U_{dc}}$	Conducting devices	
T_{1j+}	T_{2j+}	T_{3j+}	T_{1j-}	T_{2j-}	T_{3j-}		$i_j > 0$	$i_j < 0$
1	1	1	0	0	0	3	$T_{1j+}, T_{2j+}, T_{3j+}$	$D_{1j+}, D_{2j+}, D_{3j+}$
0	1	1	1	0	0	1	D_{1j}, T_{2j+}, T_{3j+}	D_{3j}, T_{1j-}
0	0	1	1	1	0	-1	D_{2j-}, T_{3j+}	D_{4j}, T_{2j-}, T_{1j-}
0	0	0	1	1	1	3	$D_{1j-}, D_{2j-}, D_{3j-}$	$T_{1j-}, T_{2j-}, T_{3j-}$

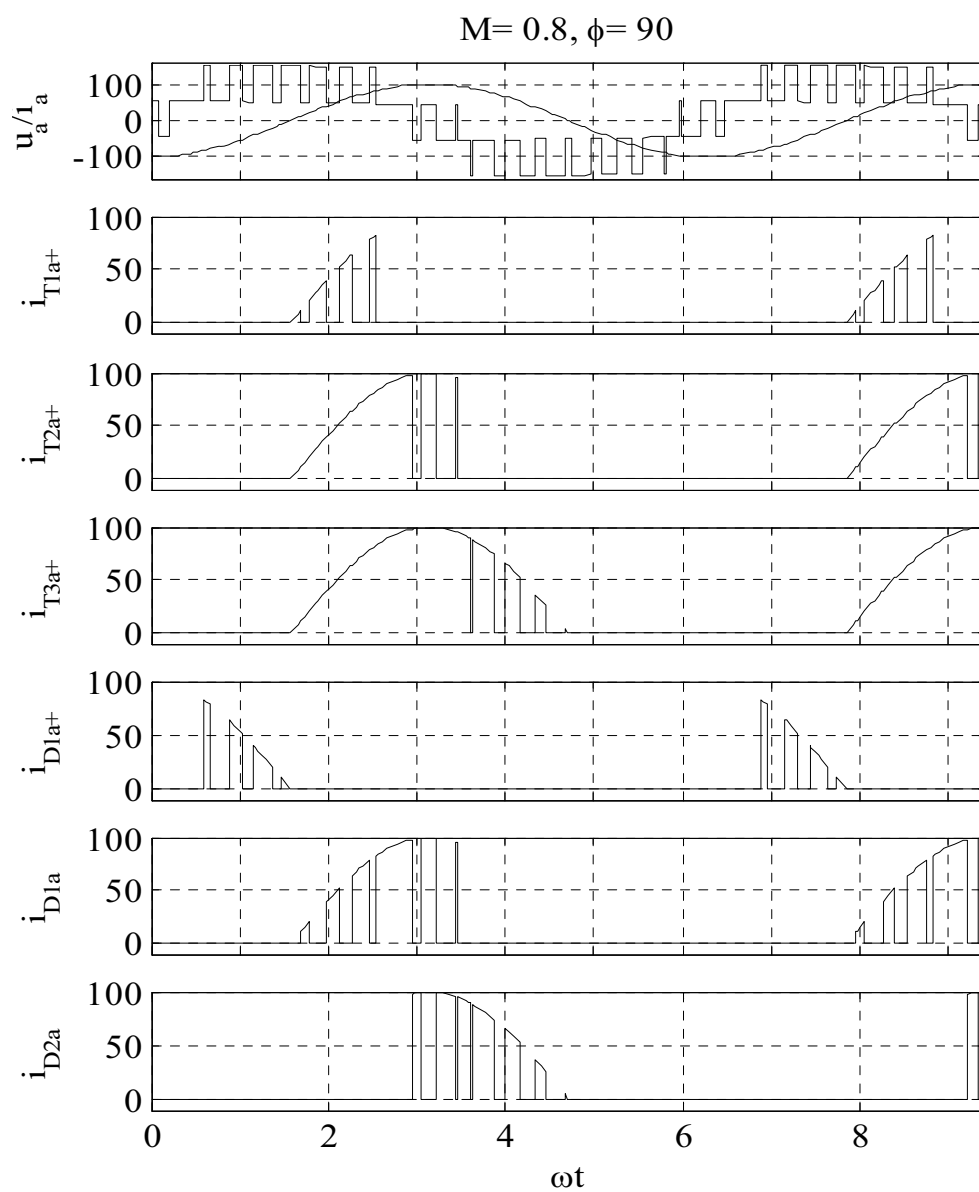


Figure 3.8: Typical output waveforms for 4-level converter simulated in KREAN.

In the 4-level topology, there are occasions where the clamping diodes are conducting, but do not have switching losses. An example is shown in Figure 3.9. T_{2j+} is switching and T_{3j+} is closed. When T_{2j+} is on, D_{1j} is conducting, and when T_{2j+} is off, D_{2j} is conducting. Since T_{1j+} is off, no reverse voltage is applied across D_{1j} , thus no switching losses occurs.

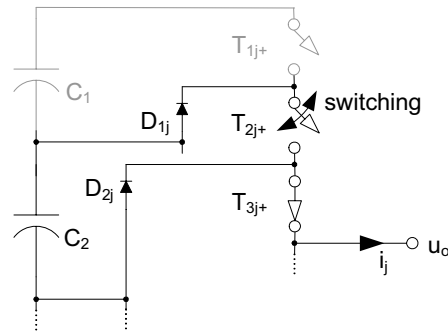


Figure 3.9: Switching to upper intermediate level in a 4-level converter.

All other areas where this occurs are shown in Figure 3.10. The figure also shows the conducting/switching areas for the other devices. The freewheeling devices are not shown because their conducting/switching areas are only when full positive/negative DC-bus voltage and negative/positive current occurs, respectively (see Figure 3.8 and Table 3-2).

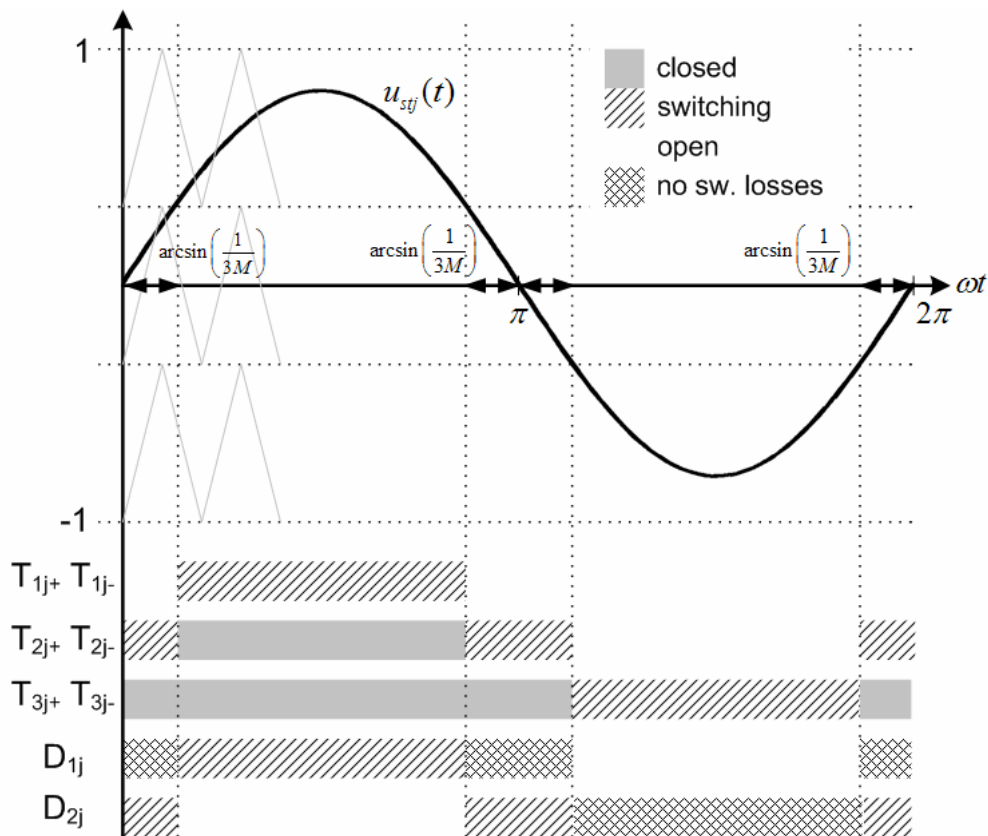


Figure 3.10: Switching devices in a 4-level converter.

3.4.2 Conducting losses

Average and RMS values for the currents can be found from Eq.(3.1). The duty cycles are given in Chapter 2.3.1. From Figure 3.10, the integral limits can be found. It can be shown through simulations and symmetry that the expressions will be the same for both inductive and capacitive load angles. Here, only the integral limits for inductive loads are shown.

3.4.2.1 For T_{1a+} and T_{3a-}

$M < 1/3$:

In this region T_{1j+} and T_{3j-} are open, thus, no conduction losses occur:

$$I_{T_{1a+},avg} = 0, I_{T_{1a+},rms} = 0 \quad (3.23)$$

$M > 1/3$:

From Figure 3.10, the expressions will be as follows for the mean and RMS value:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$I_{T_{1a+},avg} = 0, I_{T_{1a+},rms} = 0 \quad (3.24)$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$\begin{aligned} I_{T_{1a+},avg} &= \frac{1}{2\pi} \int_{\varphi}^{\pi - \arcsin(\frac{1}{3M})} d_{1a} \cdot id\omega t \\ &= \frac{\hat{I}}{24\pi \cdot M} \left(\begin{array}{l} -\cos(\varphi)\sqrt{9M^2 - 1} + \sin(|\varphi|)(9M^2 + 1) \\ +9M^2 \cos(\varphi)(\pi - \arcsin(\frac{1}{3M}) - |\varphi|) - 6M \end{array} \right) \end{aligned} \quad (3.25)$$

$$\begin{aligned} I_{T_{1a+},rms}^2 &= \frac{1}{2\pi} \int_{\varphi}^{\pi - \arcsin(\frac{1}{3M})} d_{1a} \cdot i^2 d\omega t \\ &= \frac{\hat{I}^2}{216\pi \cdot M^2} \left(\begin{array}{l} \sqrt{9M^2 - 1}(18M^2 - 2\cos^2(\varphi) + 1 + 18M^2 \cos^2(\varphi)) \\ + \sin(|\varphi|)\cos(\varphi)(2 - 27M^2) + 27M^2(\arcsin(\frac{1}{3M}) - \pi) \\ + 4M \cos(\varphi) + |\varphi| \end{array} \right) \end{aligned} \quad (3.26)$$

$$\varphi < \arcsin(1/(3M))$$

$$\begin{aligned} I_{T_{1a+},avg} &= \frac{1}{2\pi} \int_{\arcsin(\frac{1}{3M})}^{\pi - \arcsin(\frac{1}{3M})} d_{1a} \cdot id\omega t \\ &= \frac{-\hat{I} \cos(\varphi)}{24\pi} \left(\frac{2}{M} \sqrt{9M^2 - 1} - 9M\pi + 18M \arcsin(\frac{1}{3M}) \right) \end{aligned} \quad (3.27)$$

$$\begin{aligned}
I_{T_{1a+},rms}^2 &= \frac{1}{2\pi} \int_{\arcsin(\frac{1}{3M})}^{\pi - \arcsin(\frac{1}{3M})} d_{1a} \cdot i^2 d\omega t \\
&= \frac{\hat{i}^2}{216\pi M} \left(\sqrt{9M^2 - 1} \left(36M - \frac{4}{M} \cos^2(\varphi) + \frac{2}{M} + 36M \cos^2(\varphi) \right) \right. \\
&\quad \left. + 27M(2 \arcsin(\frac{1}{3M}) - \pi) \right)
\end{aligned} \tag{3.28}$$

Both the average and the RMS value of the current are plotted in Figure 3.11. As the modulation index is increasing, the duty cycle of transistor T_{1a+} is increased, and hence the current.

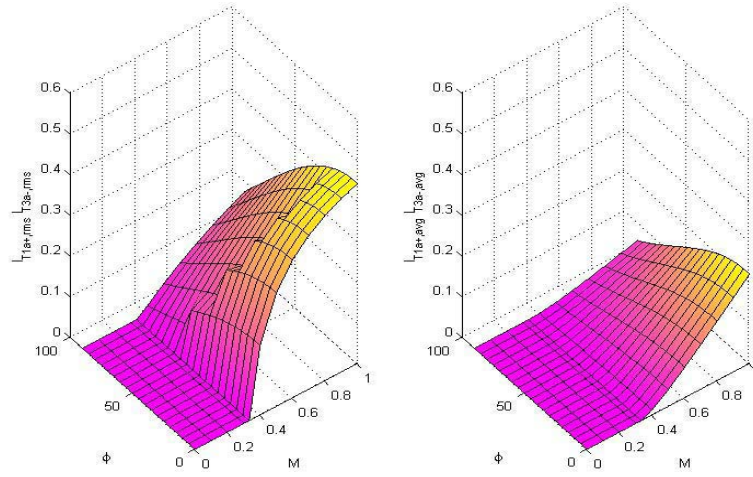


Figure 3.11: RMS and average currents in T_{1j+} and T_{3j-} .

3.4.2.2 For T_{2a+} and T_{2a-}

$M < 1/3$:

$$I_{T_{2a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi + \varphi} d_{2a} \cdot i d\omega t = \frac{\hat{i}}{8\pi} (3M \cos(\varphi)\pi + 4) \tag{3.29}$$

$$I_{T_{2a+},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi + \varphi} d_{2a} \cdot i^2 d\omega t = \frac{\hat{i}^2}{8\pi} (8M \cos(\varphi) + \pi) \tag{3.30}$$

$M > 1/3$:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$\begin{aligned}
I_{T2a+,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot id\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{12\pi} \left(\frac{\sqrt{9M^2-1}}{M} \cos(\varphi) + 6 + 9 \cos(\varphi) \cdot M \cdot \arcsin(\frac{1}{3M}) \right)
\end{aligned} \tag{3.31}$$

$$\begin{aligned}
I_{T2a+,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot i^2 d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{108\pi M^2} \left(27M^2 \sqrt{9M^2-1} + 27M^2 (4M \cos(\varphi) + \arcsin(\frac{1}{3M})) \right. \\
&\quad \left. + \sqrt{9M^2-1} \cos(2\varphi) (9M^2-1) + 2 \sin(|2\varphi|) \right)
\end{aligned} \tag{3.32}$$

$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$

$$\begin{aligned}
I_{T2a+,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi-\arcsin(\frac{1}{3M})} id\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{2\pi} \left(\frac{\sqrt{9M^2-1}}{6M} \cos(\varphi) + 1 + \frac{3}{2} \cos(\varphi) \cdot M \cdot \arcsin(\frac{1}{3M}) \right)
\end{aligned} \tag{3.33}$$

$$\begin{aligned}
I_{T2a+,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi-\arcsin(\frac{1}{3M})} i^2 d\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{-\hat{I}^2}{216\pi M^2} (-27 \sin(|2\varphi|) M^2 + 2 \sin(|2\varphi|) + 54 M^2 \varphi - 54 M^2 \pi)
\end{aligned} \tag{3.34}$$

$\varphi < \arcsin(1/(3M))$

$$\begin{aligned}
I_{T2a+,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} d_{2a} \cdot id\omega t + \int_{\arcsin(\frac{1}{3M})}^{\pi-\arcsin(\frac{1}{3M})} id\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{2\pi} \left(\frac{\sqrt{9M^2-1}}{6M} \cos(\varphi) + 1 + \frac{3}{2} \cos(\varphi) \cdot M \cdot \arcsin(\frac{1}{3M}) \right)
\end{aligned} \tag{3.35}$$

$$\begin{aligned}
I_{T2a+,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} d_{2a} \cdot i^2 d\omega t + \int_{\arcsin(\frac{1}{3M})}^{\pi-\arcsin(\frac{1}{3M})} i^2 d\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{-\hat{I}^2}{108\pi M^2} \left(\sqrt{9M^2-1} (27M^2 + 9M^2 \cos(2\varphi) - \cos(2\varphi)) \right. \\
&\quad \left. + 27M^2 \arcsin(\frac{1}{3M}) - 108M^3 \cos(\varphi) - 27M^2 \pi \right)
\end{aligned} \tag{3.36}$$

The middle transistor T_{2a+} has the largest conduction losses when the modulation function is high, and the power factor is close to unity. When the power factor decreases, the clamping diodes are conducting, resulting in lower conduction losses in T_{2a+} .

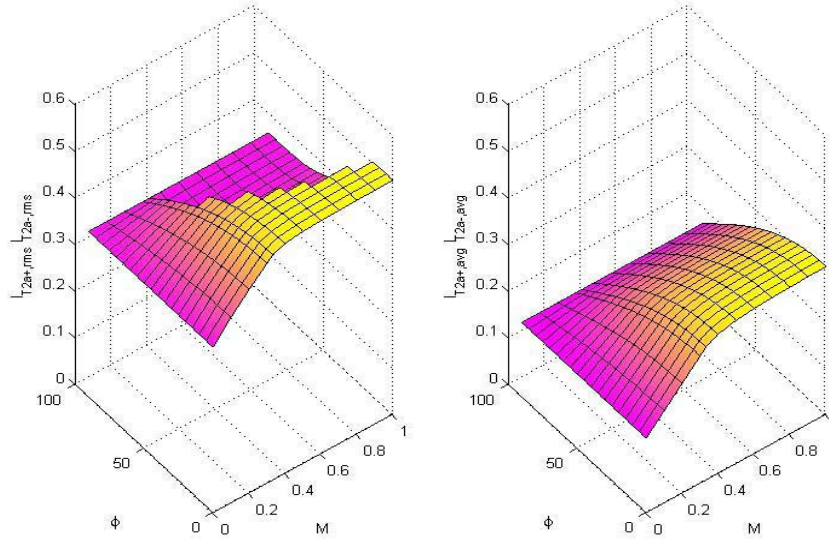


Figure 3.12: RMS and average currents in T_{2j+} and T_{2j-} .

3.4.2.3 For T_{3a+} and T_{1a-}

$M < 1/3$:

$$I_{T_{3a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} i d\omega t = \frac{\hat{I}}{\pi} \quad (3.37)$$

$$I_{T_{3a+},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} i^2 d\omega t = \frac{\hat{I}^2}{4} \quad (3.38)$$

$M > 1/3$:

$\pi - \arcsin(1/(3M)) < \varphi < \pi$

$$I_{T_{3a+},avg} = \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} i d\omega t + \int_{\pi+\arcsin(\frac{1}{3M})}^{2\pi-\arcsin(\frac{1}{3M})} d_{3a} \cdot i d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} i d\omega t \right) \quad (3.39)$$

$$= \frac{\hat{I}}{24\pi M} \left(\begin{array}{l} -2\sqrt{9M^2 - 1} \cos(\varphi) + 24M \\ +9M^2 (\pi \cos(\varphi) - \cos(\varphi) \arcsin(\frac{1}{3M})) \end{array} \right)$$

$$\begin{aligned}
I_{T_{3a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} i^2 d\omega t + \int_{\pi+\arcsin(\frac{1}{3M})}^{2\pi-\arcsin(\frac{1}{3M})} d_{3a} \cdot i^2 d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{216\pi M^2} \left(\sqrt{9M^2 - 1} (2 \cos(2\varphi) - 54M^2 - 18M^2 \cos(2\varphi)) \right. \\
&\quad \left. + 9M^2 (9\pi - 6 \arcsin(\frac{1}{3M})) \right)
\end{aligned} \tag{3.40}$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$\begin{aligned}
I_{T_{3a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\varphi} id\omega t - \int_{\pi+\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{3a}) \cdot id\omega t \right) \\
&= \frac{\hat{I}}{24\pi M} \left(-\sqrt{9M^2 - 1} \cos(\varphi) + 30M \right. \\
&\quad \left. + 9M^2 (-\sin(|\varphi|) + |\varphi| \cos(\varphi) - \cos(\varphi) \arcsin(\frac{1}{3M})) - \sin(|\varphi|) \right)
\end{aligned} \tag{3.41}$$

$$\begin{aligned}
I_{T_{3a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\varphi} i^2 d\omega t - \int_{\pi+\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{3a}) \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{432\pi M^2} \left(\sqrt{9M^2 - 1} (2 \cos(2\varphi) - 54M^2 - 18M^2 \cos(2\varphi)) + 2 \sin(|2\varphi|) \right. \\
&\quad \left. + M^2 (108\pi + 54\varphi + 216 \cos(\varphi)M - 54 \arcsin(\frac{1}{3M}) - 27 \sin(|2\varphi|)) \right)
\end{aligned} \tag{3.42}$$

$$\varphi < \arcsin(1/(3M))$$

$$I_{T_{3a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} id\omega t = \frac{\hat{I}}{\pi} \tag{3.43}$$

$$I_{T_{3a+},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} i^2 d\omega t = \frac{\hat{I}^2}{4} \tag{3.44}$$

For the lower positive transistor T_{3a+} the plots of the currents are shown in Figure 3.13. For $M < 1/3$, the transistor is closed, resulting in large conduction losses, this also holds for $M > 1/3$ and power factors near unity when the clamping diodes are not conducting.

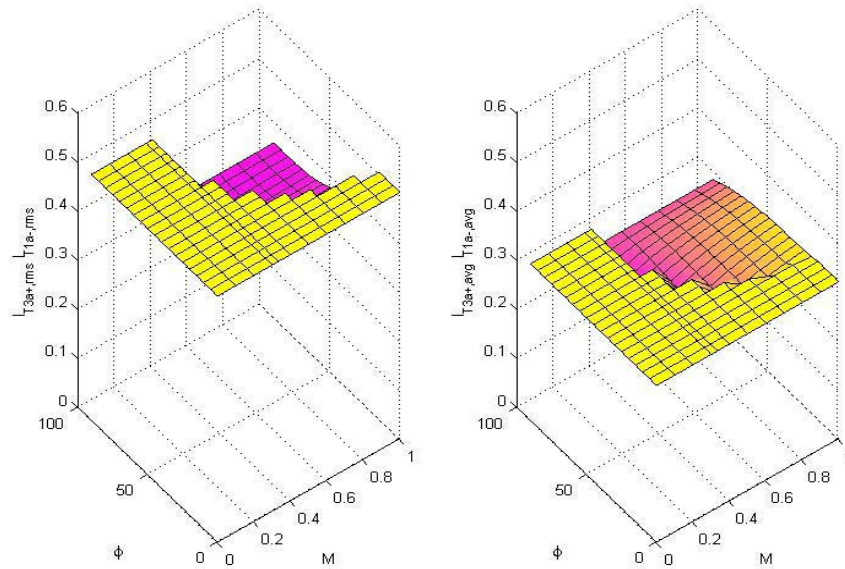


Figure 3.13: RMS and average currents in T_{3j+} and T_{1j-} .

3.4.2.4 For the freewheeling diodes D_{1a-} , D_{2a-} , D_{3a-} , D_{1a+} , D_{2a+} and D_{3a+} $M < 1/3$:

$$I_{D1a-,avg} = 0, I_{D1a-,rms} = 0 \quad (3.45)$$

$M > 1/3$:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$\begin{aligned} I_{D1a-,avg} &= \frac{1}{2\pi} \left(\int_{\pi + \arcsin(\frac{1}{3M})}^{2\pi - \arcsin(\frac{1}{3M})} (1 - d_{3a}) \cdot id \omega t \right) \\ &= \frac{\hat{I} \cos(\varphi)}{24\pi M} \left(2 \cdot \sqrt{9M^2 - 1} + 9M^2 (2 \arcsin(\frac{1}{3M}) - \pi) \right) \end{aligned} \quad (3.46)$$

$$\begin{aligned} I_{D1a-,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi + \arcsin(\frac{1}{3M})}^{2\pi - \arcsin(\frac{1}{3M})} (1 - d_{3a}) \cdot i^2 d \omega t \right) \\ &= \frac{\hat{I}^2}{216\pi M^2} \left(\sqrt{9M^2 - 1} (-2 \cos(2\varphi) + 54M^2 + 18M^2 \cos(2\varphi)) \right. \\ &\quad \left. + 27M^2 (2 \arcsin(\frac{1}{3M}) - \pi) \right) \end{aligned} \quad (3.47)$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$\begin{aligned}
I_{D1a-,avg} &= \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{3a}) \cdot i d\omega t \right) \\
&= \frac{\hat{I}}{24\pi M} \left(\begin{array}{l} \sqrt{9M^2-1} \cos(\varphi) + 9M^2 (\sin(|\varphi|) - |\varphi| \cos(\varphi) + \cos(\varphi) \arcsin(\frac{1}{3M})) \\ -6M + \sin(|\varphi|) \end{array} \right) \quad (3.48)
\end{aligned}$$

$$\begin{aligned}
I_{D1a-,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{3a}) \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{432\pi M^2} \left(\begin{array}{l} \sqrt{9M^2-1} (-2\cos(2\varphi) + 54M^2 + 18M^2 \cos(2\varphi)) - 2\sin(|2\varphi|) \\ + M^2 (-54\varphi - 216\cos(\varphi)M + 54\arcsin(\frac{1}{3M}) + 27\sin(|2\varphi|)) \end{array} \right) \quad (3.49)
\end{aligned}$$

$$\varphi < \arcsin(1/(3M))$$

$$I_{D1a-,avg} = 0, I_{D1a-,rms} = 0 \quad (3.50)$$

The freewheeling diodes are only conducting when $M > 1/3$. When the power factor is decreased, and $M > 1/3$, the freewheeling diodes are carrying more current, resulting in larger conduction losses as Figure 3.14 shows.

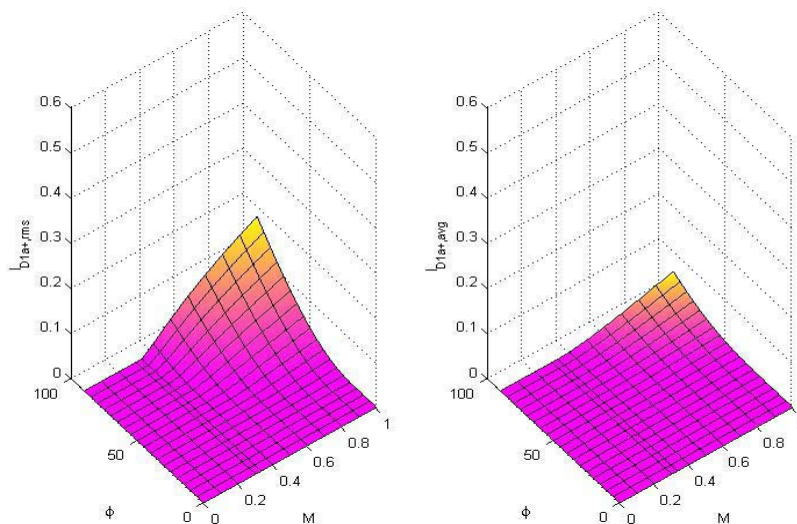


Figure 3.14: RMS and average currents in the freewheeling diodes.

3.4.2.5 For clamping diodes D_{1a} and D_{4a}

$M < 1/3$:

$$I_{D1a-,avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} d_{2a} \cdot i d\omega t = \frac{\hat{I}}{8\pi} (3M \cos(\varphi)\pi + 4) \quad (3.51)$$

$$I_{D1a,rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} d_{2a} \cdot i^2 d\omega t = \frac{\hat{I}^2}{8\pi} (8M \cos(\varphi) + \pi) \quad (3.52)$$

M>1/3:

$\pi - \arcsin(1/(3M)) < \varphi < \pi$

$$\begin{aligned} I_{D1a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot id\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot id\omega t \right) \\ &= \frac{\hat{I}}{12\pi M} \left(\sqrt{9M^2 - 1} \cos(\varphi) + 6M + 9M^2 \cos(\varphi) \arcsin(\frac{1}{3M}) \right) \end{aligned} \quad (3.53)$$

$$\begin{aligned} I_{D1a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot i^2 d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot i^2 d\omega t \right) \\ &= \frac{\hat{I}^2}{108\pi M^2} \left(\sqrt{9M^2 - 1} (-\cos(2\varphi) + 27M^2 + 9M^2 \cos(2\varphi)) \right. \\ &\quad \left. + M^2 (108 \cos(\varphi) M + 27 \arcsin(\frac{1}{3M})) \right) \end{aligned} \quad (3.54)$$

$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$

$$\begin{aligned} I_{D1a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi-\arcsin(\frac{1}{3M})} (1-d_{1a}) id\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot id\omega t \right) \\ &= \frac{\hat{I}}{24\pi M} \left(3\sqrt{9M^2 - 1} \cos(\varphi) - \sin(|\varphi|) + 18M \right. \\ &\quad \left. - 9M^2 (\sin(|\varphi|) + \pi \cos(\varphi) - 3 \cos(\varphi) \arcsin(\frac{1}{3M}) - \varphi \cos(\varphi)) \right) \end{aligned} \quad (3.55)$$

$$\begin{aligned} I_{D1a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi-\arcsin(\frac{1}{3M})} (1-d_{1a}) i^2 d\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} d_{2a} \cdot i^2 d\omega t \right) \\ &= \frac{\hat{I}^2}{432\pi M^2} \left(\sqrt{9M^2 - 1} (2 \cos(2\varphi) - 54M^2 - 18M^2 \cos(2\varphi)) - 6 \sin(|2\varphi|) \right. \\ &\quad \left. + M^2 \left(-162\varphi - 216 \cos(\varphi) M - 54 \arcsin(\frac{1}{3M}) \right) \right. \\ &\quad \left. + 81 \sin(|2\varphi|) + 162\pi \right) \end{aligned} \quad (3.56)$$

$\varphi < \arcsin(1/(3M))$

$$\begin{aligned} I_{D1a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} d_{2a} \cdot id\omega t + \int_{\arcsin(\frac{1}{3M})}^{\pi-\arcsin(\frac{1}{3M})} (1-d_{1a}) \cdot id\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{2a} \cdot id\omega t \right) \\ &= \frac{\hat{I}}{24\pi M} \left(4\sqrt{9M^2 - 1} \cos(\varphi) + 36M^2 \cos(\varphi) \arcsin(\frac{1}{3M}) + 12M - 9M^2 \cos(\varphi) \pi \right) \end{aligned} \quad (3.57)$$

$$\begin{aligned}
I_{D1a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} d_{2a} \cdot i^2 d\omega t + \int_{\arcsin(\frac{1}{3M})}^{\pi - \arcsin(\frac{1}{3M})} (1 - d_{1a}) \cdot i^2 d\omega t \right. \\
&\quad \left. + \int_{\pi - \arcsin(\frac{1}{3M})}^{\pi + \varphi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{216\pi M^2} \left(\sqrt{9M^2 - 1} \left(-108M^2 - 36M^2 \cos(2\varphi) + 4 \cos(2\varphi) \right) \right. \\
&\quad \left. - 108M^2 \arcsin\left(\frac{1}{3M}\right) + 216M^3 \cos(\varphi) + 81M^2 \pi \right)
\end{aligned} \tag{3.58}$$

The upper clamping diode D_{1a} has the largest conducting losses at high power factors, when the middle positive transistor is conducting and the upper positive transistor is not.

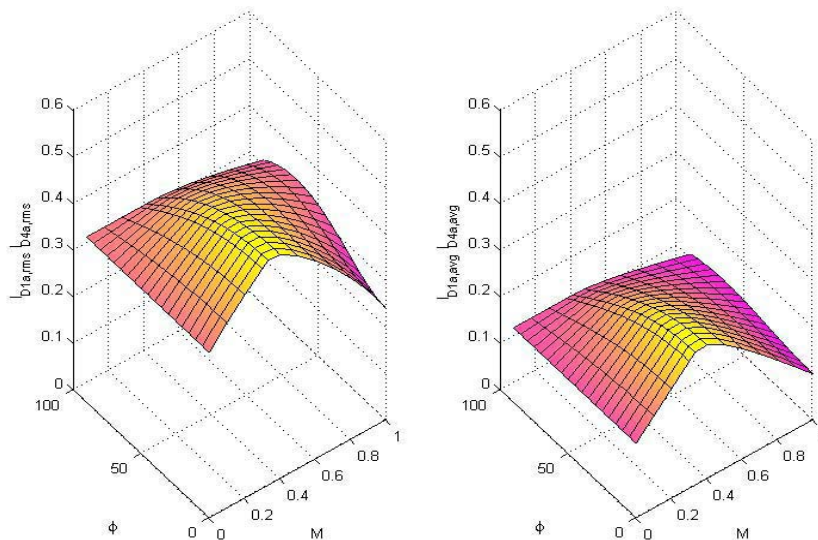


Figure 3.15: RMS and average currents in the clamping diodes D_{1j} and D_{4j} .

3.4.2.6 For clamping diode D_{2a} and D_{3a}

$M < 1/3$:

$$I_{D2a,avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi + \varphi} (1 - d_{2a}) \cdot i d\omega t = \frac{\hat{I}}{8\pi} (4 - 3M \cos(\varphi)\pi) \tag{3.59}$$

$$I_{D2a,rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi + \varphi} (1 - d_{2a}) \cdot i^2 d\omega t = \frac{\hat{I}^2}{8\pi} (\pi - 8M \cos(\varphi)) \tag{3.60}$$

$M > 1/3$:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$\begin{aligned}
I_{D2a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} (1-d_{2a})id\omega t + \int_{\pi+\arcsin(\frac{1}{3M})}^{2\pi-\arcsin(\frac{1}{3M})} d_{3a} \cdot id\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{2a})id\omega t \right) \\
&= \frac{\hat{I}}{24\pi M} \left(\begin{aligned} &-4\sqrt{9M^2-1}\cos(\varphi)+12M \\ &+9M^2(\pi\cos(\varphi)-4\cos(\varphi)\cdot\arcsin(\frac{1}{3M})) \end{aligned} \right) \quad (3.61)
\end{aligned}$$

$$\begin{aligned}
I_{D2a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} (1-d_{2a})i^2d\omega t + \int_{\pi+\arcsin(\frac{1}{3M})}^{2\pi-\arcsin(\frac{1}{3M})} d_{3a} \cdot i^2d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{2a})i^2d\omega t \right) \\
&= \frac{\hat{I}^2}{216\pi M^2} \left(\begin{aligned} &\sqrt{9M^2-1}(4\cos(2\varphi)-108M^2-36M^2\cos(2\varphi))+81M^2\pi \\ &+108M^2(-2\cos(\varphi)M-\arcsin(\frac{1}{3M})) \end{aligned} \right) \quad (3.62)
\end{aligned}$$

$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$

$$\begin{aligned}
I_{D2a,avg} &= \frac{1}{2\pi} \left(\int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} (1-d_{2a})id\omega t + \int_{\pi+\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{3a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{24\pi M} \left(\begin{aligned} &-3\sqrt{9M^2-1}\cos(\varphi)-\sin(|\varphi|)+18M \\ &+9M^2(-3\cos(\varphi)\cdot M\cdot\arcsin(\frac{1}{3M})-\sin(|\varphi|)+|\varphi|\cos(\varphi)) \end{aligned} \right) \quad (3.63)
\end{aligned}$$

$$\begin{aligned}
I_{D2a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} (1-d_{2a})i^2d\omega t + \int_{\pi+\arcsin(\frac{1}{3M})}^{\pi+\varphi} d_{3a} \cdot i^2d\omega t \right) \\
&= \frac{\hat{I}^2}{432\pi M^2} \left(\begin{aligned} &\sqrt{9M^2-1}(2\cos(2\varphi)-54M^2-18M^2\cos(2\varphi))+6\sin(|2\varphi|) \\ &+M^2(162\varphi+216\cos(\varphi)M-54\arcsin(\frac{1}{3M})-81\sin(|2\varphi|)) \end{aligned} \right) \quad (3.64)
\end{aligned}$$

$\varphi < \arcsin(1/(3M))$

$$\begin{aligned}
I_{D2a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} (1-d_{2a}) \cdot id\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{2a}) \cdot id\omega t \right) \\
&= \frac{\hat{I}}{12\pi} \left(-\sqrt{9M^2-1}\cos(\varphi)+6-9\cos(\varphi)M\arcsin(\frac{1}{3M}) \right) \quad (3.65)
\end{aligned}$$

$$\begin{aligned}
I_{D2a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} (1-d_{2a}) \cdot i^2d\omega t + \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} (1-d_{2a}) \cdot i^2d\omega t \right) \\
&= \frac{\hat{I}^2}{108\pi M^2} \left(\begin{aligned} &\sqrt{9M^2-1}(-\cos(2\varphi)+27M^2+9M^2\cos(2\varphi)) \\ &-108M^3\cos(\varphi)+27M^2\arcsin(\frac{1}{3M}) \end{aligned} \right) \quad (3.66)
\end{aligned}$$

The lower positive clamping diode D_{2a} is conducting when only the lower positive transistor is on and the output current is positive, resulting in large conducting losses at low power factors as Figure 3.16 shows.

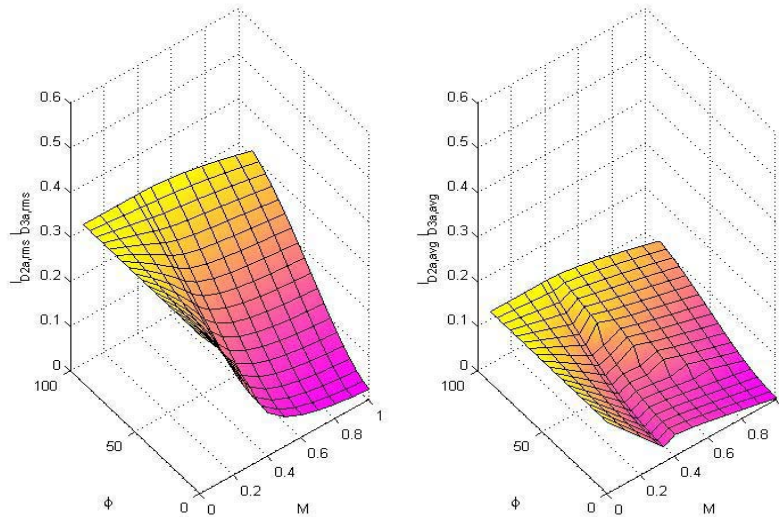


Figure 3.16: RMS and average currents in the clamping diodes D_{2j} and D_{3j} .

From the above equations and plots, the worst case components for conduction losses are the middle transistors T_{2a+} and T_{2a-} . They have the largest conduction losses when the modulation function is high, and the power factor is close to 1.0. When the power factor decreases, the clamping diodes are conducting, resulting in lower conduction losses in T_{2a+} and T_{2a-} . For the lower positive transistor T_{3a+} and the upper negative transistor T_{1a-} , the conduction losses are high for $M < 1/3$, since they are closed. When $M > 1/3$ and power factors near unity and the clamping diodes are not conducting, the duty cycle is large, resulting in high losses.

3.4.3 Switching losses

For 4-level converters, the cases where the amplitude modulation factor M is larger or smaller than $1/3$ lead to two different sets of formulas. In addition three different sets of formulas will be valid depending on the phase angle φ and the amplitude modulation factor M according to Eq. (2.10).

The switching losses are calculated from Eq.(3.9), using integral limits corresponding to the intervals in Figure 3.10. From symmetry, the general equations for inductive and capacitive load will be the same, hence only the integration limits valid for inductive loads are presented here, and the equations are valid for $-\pi < \varphi \leq \pi$, i.e. both rectifier and inverter operation.

Only the expressions for phase a is shown, since the losses for the b - and c -phase will be the same.

3.4.3.1 For T_{1a+} and T_{3a-}

The general formulas for switching losses in each component will be:

$M < 1/3$:

By inspecting Figure 3.10, the case where $M < 1/3$ gives a simpler set of equations. In this area T_{1j+} and T_{3j-} are open. Hence, no switching losses occur.

$M > 1/3$:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$P_{T_{1a+},sw} = 0 \quad (3.67)$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$\begin{aligned} P_{T_{1a+},sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi - \arcsin(\frac{1}{3M})} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{108\pi M^2} \left(\begin{aligned} &6k_{1,T} \left(\sqrt{9M^2 - 1} \cos(\varphi) M - \sin(|\varphi|) M + 3M^2 \right) \\ &+ k_{2,T} \hat{I} \left(\begin{aligned} &\sqrt{9M^2 - 1} (\cos^2(\varphi) - \sin^2(|\varphi|)) + \sin(|\varphi|) \cos(\varphi) (9M^2 - 2) \\ &+ 9M^2 (\pi - |\varphi| - \arcsin(\frac{1}{3M})) \end{aligned} \right) \end{aligned} \right) \quad (3.68) \end{aligned}$$

$$\varphi < \arcsin(1/(3M))$$

$$\begin{aligned} P_{T_{1a+},sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\arcsin(\frac{1}{3M})}^{\pi - \arcsin(\frac{1}{3M})} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{108\pi M} \left(\begin{aligned} &12k_{1,T} \sqrt{9M^2 - 1} \cos(\varphi) \\ &+ \frac{k_{2,T} \hat{I}}{M} \left(2\sqrt{9M^2 - 1} (\cos^2(\varphi) - \sin^2(|\varphi|)) + 9M^2 (\pi - 2 \arcsin(\frac{1}{3M})) \right) \end{aligned} \right) \quad (3.69) \end{aligned}$$

As the plot of the relative switching losses in Figure 3.17 shows, the losses are increasing with increased modulation index for $M > 1/3$.

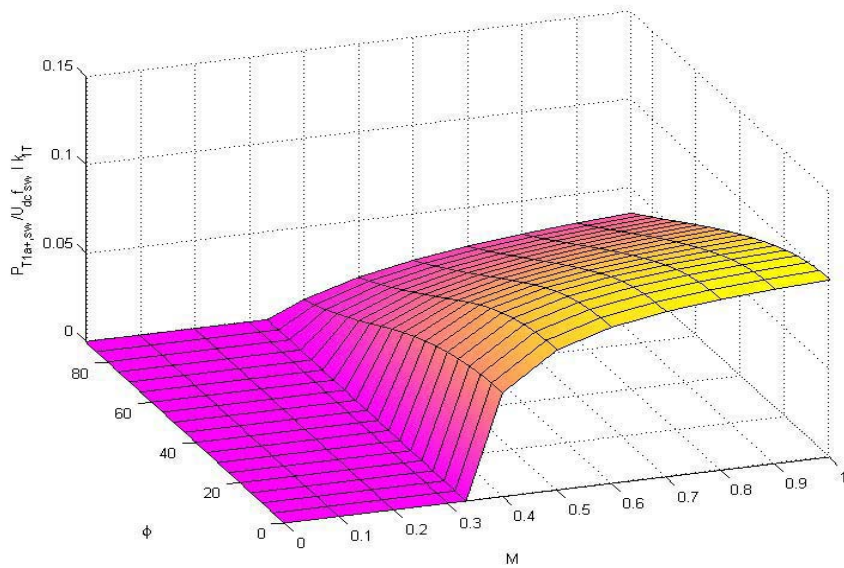


Figure 3.17: Relative switching losses in T_{1j+} and T_{3j-} .

3.4.3.2 T_{2a+} and T_{2a-}

$M < 1/3$:

$$P_{T_{2a+,sw}} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi+\varphi} k_{1,T} i + k_{2,T} i^2 d\omega t = \frac{U_{dc} f_{sw} \hat{I}}{12\pi} (4k_{1,T} + k_{2,T} \hat{I} \pi) \quad (3.70)$$

$M > 1/3$:

$\pi - \arcsin(1/(3M)) < \varphi < \pi$

$$\begin{aligned} P_{T_{2a+,sw}} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} k_{1,T} i + k_{2,T} i^2 d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} k_{1,T} i + k_{2,T} i^2 d\omega t \right) \\ &= \frac{U_{dc} f_{sw} \hat{I}}{54\pi M} \left(\begin{aligned} &6k_{1,T} (\cos(\varphi) \sqrt{9M^2 - 1} + 3M) \\ &+ \frac{k_{2,T} \hat{I}}{M} (\sqrt{9M^2 - 1} \cos(2\varphi) + 9 \arcsin(\frac{1}{3M}) M^2) \end{aligned} \right) \end{aligned} \quad (3.71)$$

$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$

$$\begin{aligned} P_{T_{2a+,sw}} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}_N}{54\pi M} \left(\begin{aligned} &6k_{1,T} \sin(|\varphi|) \\ &+ \frac{k_{2,T} \hat{I}_N}{M} (\sqrt{9M^2 - 1} (-\cos^2(\varphi) + \sin^2(|\varphi|)) + 9 \arcsin(\frac{1}{3M}) M^2) \end{aligned} \right) \end{aligned} \quad (3.72)$$

$$\varphi < \arcsin(1/(3M))$$

$$\begin{aligned}
 P_{T_{2a+},sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} k_{1,T}i + k_{2,T}i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{3M})}^{\pi + \varphi} k_{1,T}i + k_{2,T}i^2 d\omega t \right) \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{54\pi M} \left(\begin{aligned} &k_{1,T}(-6\sqrt{9M^2 - 1} \cos(\varphi) + 18M) \\ &+ \frac{k_{2,T} \hat{I}}{M} \left(-\sqrt{9M^2 - 1} \cos(2\varphi) + 9M^2 \arcsin(\frac{1}{3M}) \right) \end{aligned} \right) \quad (3.73)
 \end{aligned}$$

From Figure 3.18 the positive transistor T_{2a+} , has the highest switching losses at $M < 1/3$ when it is switched the whole fundamental period. Switching losses will also occur for $M > 1/3$, but decreasing with increased modulation index.

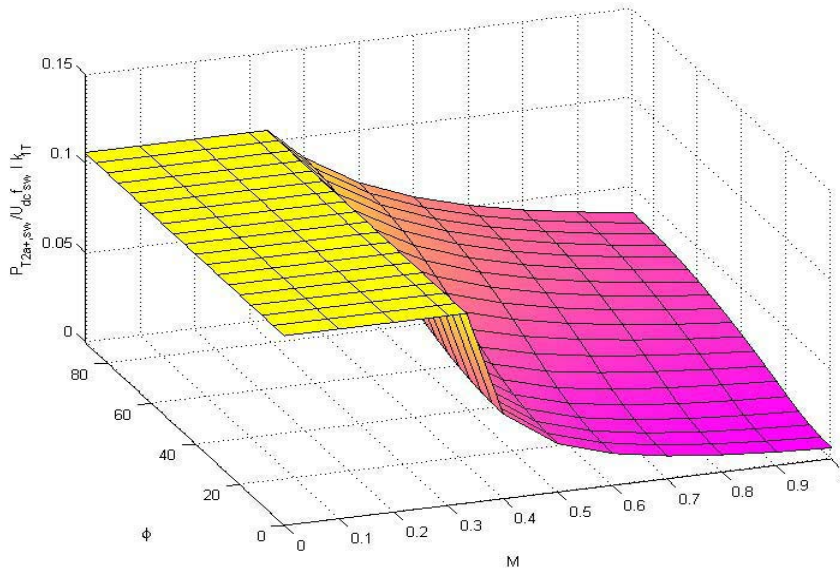


Figure 3.18: Relative switching losses in T_{2j+} and T_{2j-} .

3.4.3.3 For T_{3a+} and T_{1a-}

$M < 1/3$:

By inspecting Figure 3.10, the case where $M < 1/3$ gives a simpler set of equations. In this area T_{3j+} and T_{1j-} are closed. Hence, no switching losses occur.

$M > 1/3$:

In this region the transistor have switching losses when the output voltage is negative and the output current is positive, i.e at low power factors, as Figure 3.19 shows:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$\begin{aligned}
P_{Ta3+,sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{3M})}^{2\pi - \arcsin(\frac{1}{3M})} k_{1,T}i + k_{2,T}i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{108\pi M^2} \left(\begin{aligned} &-12k_{1,T}M\sqrt{9M^2-1} \cos(\varphi) \\ &+k_{2,T}\hat{I} \left(2\cdot\sqrt{9M^2-1} \cos(2\varphi) + 9M^2(\pi - 2\arcsin(\frac{1}{3M})) \right) \end{aligned} \right) \quad (3.74)
\end{aligned}$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$\begin{aligned}
P_{T3a+,sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{3M})}^{\pi + \varphi} k_{1,T}i + k_{2,T}i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{108\pi M^2} \left(\begin{aligned} &6k_{1,T}M \left(3M - \sqrt{9M^2-1} \cos(\varphi) - \sin(|\varphi|) \right) \\ &+k_{2,T}\hat{I} \left(\sqrt{9M^2-1} \cos(2\varphi) + \frac{1}{2} \sin(|2\varphi|) (2-9M^2) \right) \\ &+9M^2 (|\varphi| - \arcsin(\frac{1}{3M})) \end{aligned} \right) \quad (3.75)
\end{aligned}$$

$$\varphi < \arcsin(1/(3M))$$

$$P_{T3a+,sw} = 0 \quad (3.76)$$

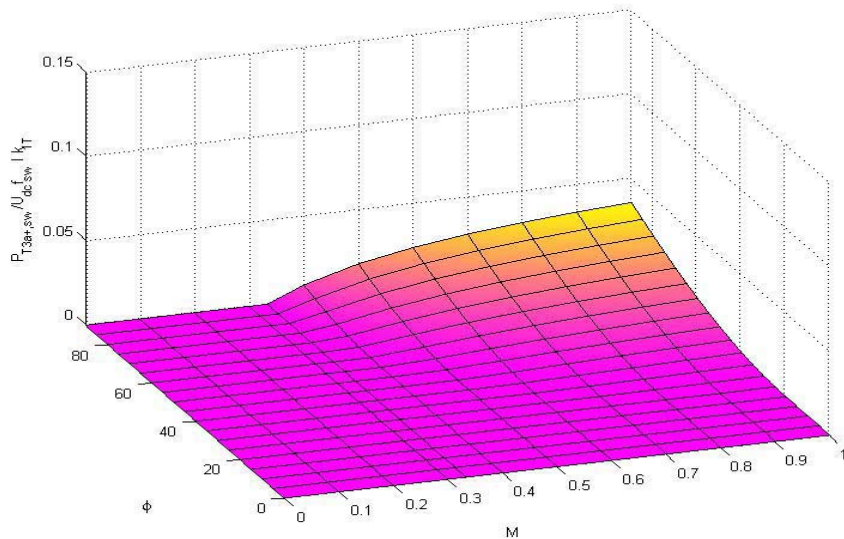


Figure 3.19: Relative switching losses in T_{3j+} and T_{1j-}.

3.4.3.4 For freewheeling diodes D_{1a-}, D_{2a-}, D_{3a-}, D_{1a+}, D_{2a+} and D_{3a+} M < 1/3:

In this region the freewheeling diodes are not part of the switching process, thus no switching losses occur.

M > 1/3:

In this region, the positive freewheeling diodes are only part of the switching process when the output voltage is positive and the output current negative. Thus, the switching losses increase with decreased power factor as Figure 3.20 shows:

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$P_{D1a-,sw} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{3M})}^{2\pi - \arcsin(\frac{1}{3M})} k_{1,D}i + k_{2,D}i^2 d\omega t$$

$$= \frac{U_{dc} f_{sw} \hat{I}}{108\pi M^2} \left(\begin{array}{l} -12k_{1,D}M\sqrt{9M^2 - 1} \cos(\varphi) \\ + k_{2,D}\hat{I} \left(2 \cdot \sqrt{9M^2 - 1} \cos(2\varphi) + 9M^2 (\pi - 2 \arcsin(\frac{1}{3M})) \right) \end{array} \right) \quad (3.77)$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$P_{D1a-,sw} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{3M})}^{\pi + \varphi} k_{1,D}i + k_{2,D}i^2 d\omega t$$

$$= \frac{-U_{dc} f_{sw} \hat{I}}{108\pi M^2} \left(\begin{array}{l} 6k_{1,D}M \left(\sqrt{9M^2 - 1} \cos(\varphi) + \sin(|\varphi|) - 3M \right) \\ + k_{2,D}\hat{I} \left(\begin{array}{l} -\sqrt{9M^2 - 1} \cos(2\varphi) \\ + \frac{1}{2} \sin(|\varphi|) (9M^2 - 2) + 9M^2 (\arcsin(\frac{1}{3M}) - |\varphi|) \end{array} \right) \end{array} \right) \quad (3.78)$$

$$\varphi < \arcsin(1/(3M))$$

$$P_{D1a-,sw} = 0 \quad (3.79)$$

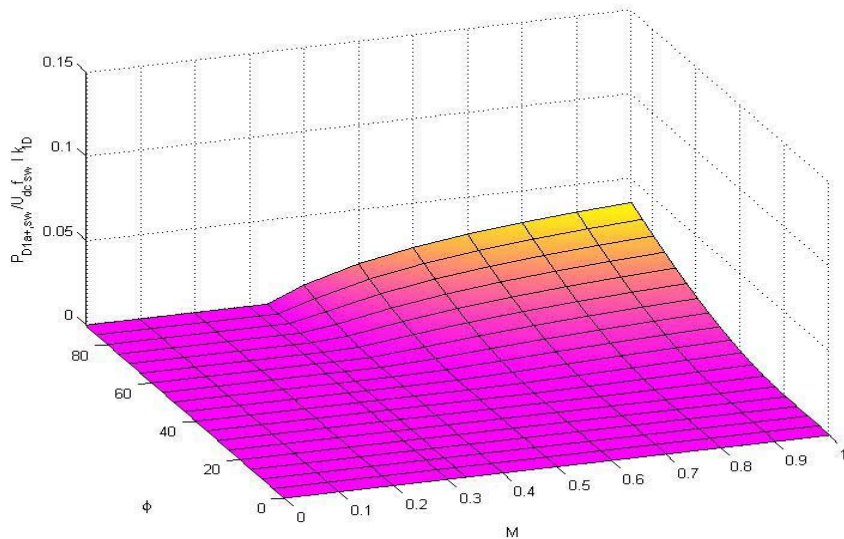


Figure 3.20: Relative switching losses in the freewheeling diodes.

3.4.3.5 For clamping diodes D_{1a} and D_{4a}

$M < 1/3$:

By inspecting Figure 3.10, no switching losses will occur in the clamping diodes D_{1j} and D_{4j} since no voltage is applied across these devices.

$M > 1/3$:

In this region, the upper clamping diode will have switching losses at commutation with the upper transistor. As the modulation index is increasing, the losses will increase, as indicated in Figure 3.21.

$$\pi - \arcsin(1/(3M)) < \varphi < \pi$$

$$P_{D1a,sw} = 0 \quad (3.80)$$

$$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$$

$$\begin{aligned} P_{D1a,sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi - \arcsin(\frac{1}{3M})} k_{1,D} i + k_{2,D} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{216\pi M^2} \left(\begin{array}{l} 12k_{1,D} \left(\sqrt{9M^2 - 1} \cos(\varphi) M - \sin(|\varphi|) M + 3M^2 \right) \\ + k_{2,D} \hat{I} \left(\begin{array}{l} 2\sqrt{9M^2 - 1} \cos(2\varphi) - 2\sin(|2\varphi|) \\ + 9M^2 (\sin(|2\varphi|) - 2|\varphi| + 2\pi - 2\arcsin(\frac{1}{3M})) \end{array} \right) \end{array} \right) \end{aligned} \quad (3.81)$$

$$\varphi < \arcsin(1/(3M))$$

$$\begin{aligned} P_{D1a,sw} &= \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\arcsin(\frac{1}{3M})}^{\pi - \arcsin(\frac{1}{3M})} k_{1,D} i + k_{2,D} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{108\pi M^2} \left(\begin{array}{l} 12k_{1,D} M \sqrt{9M^2 - 1} \cos(\varphi) \\ + k_{2,D} \hat{I} \left(2\sqrt{9M^2 - 1} \cos(2\varphi) + 9M^2 (\pi - 2\arcsin(\frac{1}{3M})) \right) \end{array} \right) \end{aligned} \quad (3.82)$$

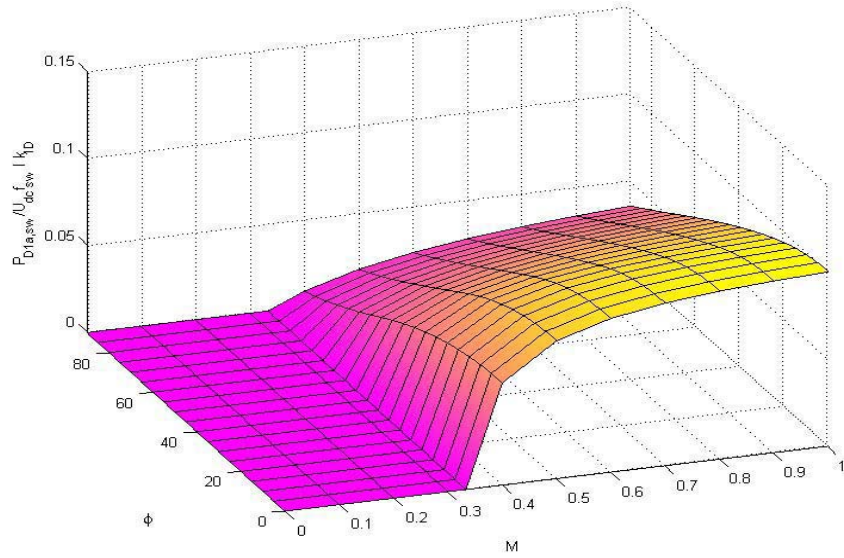


Figure 3.21: Relative switching losses in clamping diodes D_{1j} and D_{3j} .

3.4.3.6 For clamping diodes D_{2a} and D_{3a}

$M < 1/3$:

$$P_{D2a,sw} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi+\varphi} k_{1,D} i + k_{2,D} i^2 d\omega t = \frac{U_{dc} f_{sw} \hat{I}}{12\pi} (4k_{1,D} + k_{2,D} \hat{I} \pi) \quad (3.83)$$

$M > 1/3$:

$\pi - \arcsin(1/(3M)) < \varphi < \pi$

$$P_{D2a,sw} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{3M})} k_{1,D} i + k_{2,D} i^2 d\omega t + \int_{2\pi-\arcsin(\frac{1}{3M})}^{\pi+\varphi} k_{1,D} i + k_{2,D} i^2 d\omega t \right) \quad (3.84)$$

$$= \frac{U_{dc} f_{sw} \hat{I}}{54\pi M^2} \left(6k_{1,D} M \left(\sqrt{9M^2 - 1} \cos(\varphi) + 2M \right) + k_{2,D} \hat{I} \left(-\sqrt{9M^2 - 1} \cos(2\varphi) + 9M^2 \arcsin(\frac{1}{3M}) \right) \right)$$

$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$

$$P_{D2a,sw} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \int_{\pi-\arcsin(\frac{1}{3M})}^{\pi+\arcsin(\frac{1}{3M})} k_{1,D} i + k_{2,D} i^2 d\omega t \quad (3.85)$$

$$= \frac{U_{dc} f_{sw} \hat{I}}{54\pi M^2} \left(6k_{1,D} M \sin(|\varphi|) + k_{2,D} \hat{I} \left(-\sqrt{9M^2 - 1} \cos(2\varphi) + 9M^2 \arcsin(\frac{1}{3M}) \right) \right)$$

$$\varphi < \arcsin(1/(3M))$$

$$P_{D_{2a,sw}} = \frac{U_{dc}}{3} \frac{1}{2\pi} f_{sw} \left(\int_{\varphi}^{\arcsin(\frac{1}{3M})} k_{1,D} i + k_{2,D} i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{3M})}^{\pi + \varphi} k_{1,D} i + k_{2,D} i^2 d\omega t \right) \quad (3.86)$$

$$= \frac{U_{dc} f_{sw} \hat{I}}{54\pi M^2} \left(6k_{1,D} M \left(-\sqrt{9M^2 - 1} \cos(\varphi) + 3M \right) + k_{2,D} \hat{I} \left(-\sqrt{9M^2 - 1} \cos(2\varphi) + 9M^2 \arcsin\left(\frac{1}{3M}\right) \right) \right)$$

For the lower clamping diode, the switching losses will be largest when $M < 1/3$ and it is commutating with the lower positive transistor T_{3a+} . When $M > 1/3$ the losses will increase with decreased power factor.

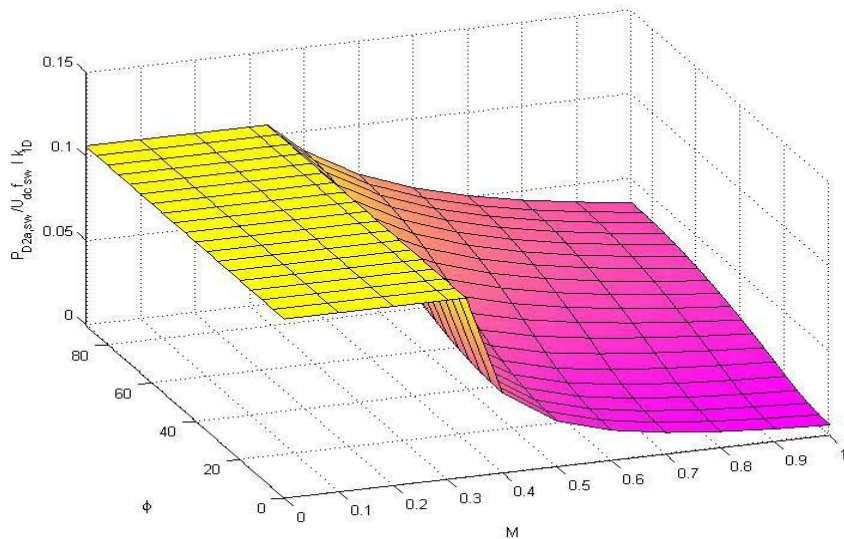


Figure 3.22: Relative switching losses in clamping diodes D_{2j} and D_{3j} .

3.4.4 Evaluation of the expressions

By thorough simulations in Saber, the expressions for the RMS and average currents are evaluated. The verification is done in the modulation range $M = [0.2, 1]$ and $\varphi = [-150^\circ, 150^\circ]$, with a switching frequency at 1500Hz , and a load current of $100 A_{RMS}$. In Appendix A the results are displayed. The worst case is the deviation for $i_{D_{2a}}$ for $M = 1$ and $\varphi = 0^\circ$. at $0.737 A$ between simulated and calculated value. This is caused by the low accuracy of the expressions in this region, where both simulated and analytical values are small. The expressions for the switching losses are not evaluated, because ideal switching devices are used in the simulations.

3.5 5-level Converter

3.5.1 Topology and performance

The 5-level converter consists of eight active switches connected in series in each bridge leg (Figure 3.23). Ideally, the maximum voltage that will be applied to each switch under normal conditions is $U_{dc}/4$. Four equal capacitors are connected in series at the DC-link in order to partition the voltage into five voltage levels. In addition, six clamping diodes give access to the intermediate voltage levels. In Table 3-3, the conducting devices for different output conditions are shown.

As mentioned in 3.4.1 for the 4-level topology, there will exist cases where the clamping diodes must block more than $U_{dc}/4$. When T_{1j+} - T_{4j+} are closed, D_{2j} must block $U_{dc}/2$ and D_{3j} must block $3U_{dc}/4$. This is also true for D_{4j} and D_{5j} when T_{1j-} - T_{4j-} are closed.

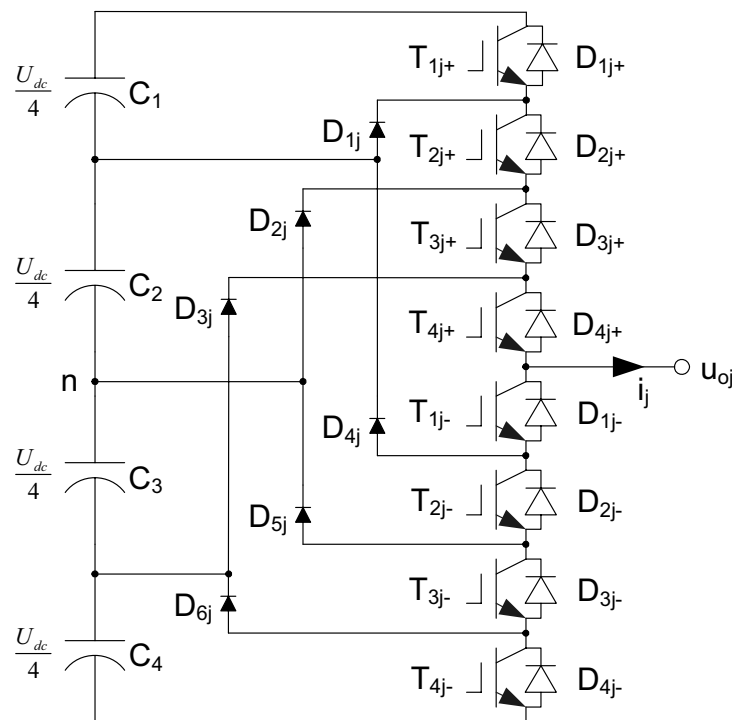


Figure 3.23: One phase leg of a 5-level converter.

Similar to the 4-level topology, the freewheeling diodes D_{1j+} - D_{4j+} share the same current waveform. This is also true for D_{1j-} - D_{4j-} only shifted 180° . For the switches, $T_{1j+}/T_{4j-}, T_{2j+}/T_{3j-}, T_{3j+}/T_{2j-}, T_{4j+}/T_{1j-}$ share the same waveform, also shifted. This also holds for the opposite clamping diodes $D_{1j}/D_{6j}, D_{2j}/D_{5j}$ and D_{3j}/D_{4j} . Figure 3.25 shows some typical simulated output waveforms.

Table 3-3: Conducting devices in 5-level converter.

Switching state				$\frac{4u_{oj-n}}{U_{dc}}$	Conducting devices	
T_{1j+}	T_{2j+}	T_{3j+}	T_{3j+}		$i_j > 0$	$i_j < 0$
1	1	1	1	2	$T_{1j+}, T_{2j+}, T_{3j+}, T_{4j+}$	$D_{1j+}, D_{2j+}, D_{3j+}, D_{4j+}$
0	1	1	1	1	$D_{1j}, T_{2j+}, T_{3j+}, T_{4j+}$	D_{4j}, T_{1j-}
0	0	1	1	0	D_{2j}, T_{3j+}, T_{4j+}	D_{5j}, T_{1j-}, T_{2j-}
0	0	0	1	-1	D_{3j}, T_{4j+}	$D_{6j}, T_{1j-}, T_{2j-}, T_{3j-}$
0	0	0	0	-2	$D_{1j-}, D_{2j-}, D_{3j-}, D_{4j-}$	$T_{1j-}, T_{2j-}, T_{3j-}, T_{4j-}$

For the clamping diodes there exists states where the device is switching, but no switching losses occur as for the 4-level converter. This is because no voltage is applied when the switching occur (ref. Figure 3.9 for 4-level converter). Figure 3.24 summarizes these areas. In addition, the figure shows the conduction/switching properties for the other devices in the topology.

Because of the complexity of the derived equations for the 5-level topology, the results from the calculations are shown in Appendix B.

As for the 4-level topology, the expressions for the RMS and average currents are evaluated in Saber (see Appendix B.2.3 for details). The verification are done in the modulation range $M = [0.2, 1]$ and $\varphi = [-150^\circ, 150^\circ]$, with a switching frequency at 1500Hz, and a load current of $100A_{RMS}$. For the 5-level topology, the same simulation parameters as for the 4-level converter apply. Again, the worst deviations in percent are for the freewheeling diode i_{D1a} . The accuracy of the simulations are poor at this current level, and is the cause of this large deviation. At $M = 0.8$ and $\varphi = -45^\circ$, the calculated RMS and average currents are $0.219A$ and $0.006A$ respectively. The worst case in amperes is for the clamp diode i_{D3a} at $M = 0.6$ and $\varphi = 90^\circ$, where the deviation between simulated and calculated current value is $1.163 A$ for a load current of $100 A_{RMS}$.

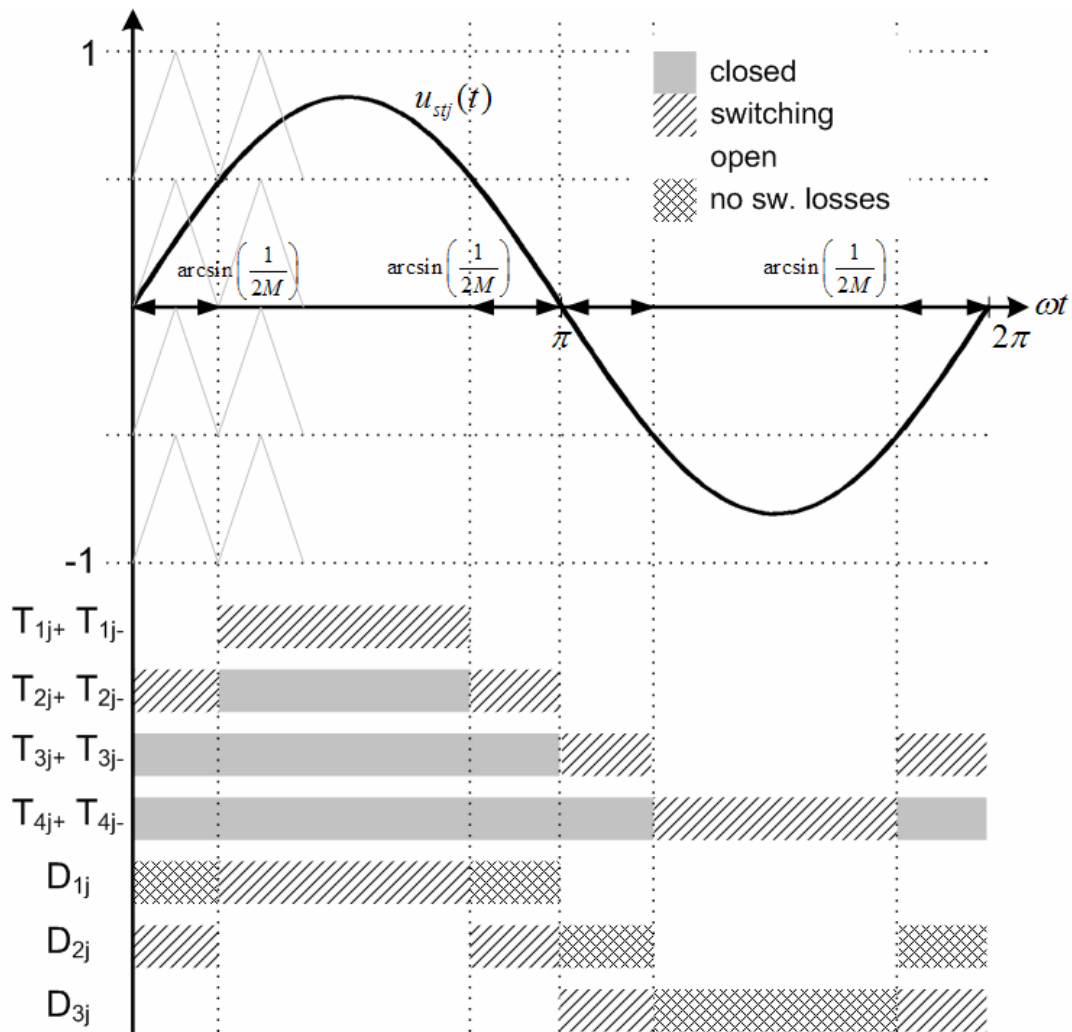


Figure 3.24: Switching devices in a 5-level converter.

3.6 Conclusion

The analytical expressions developed for 4-level and 5-level converters are shown to be quite exact and should be useful for dimensioning purposes and loss comparison. Case studies will be shown in the next chapter.

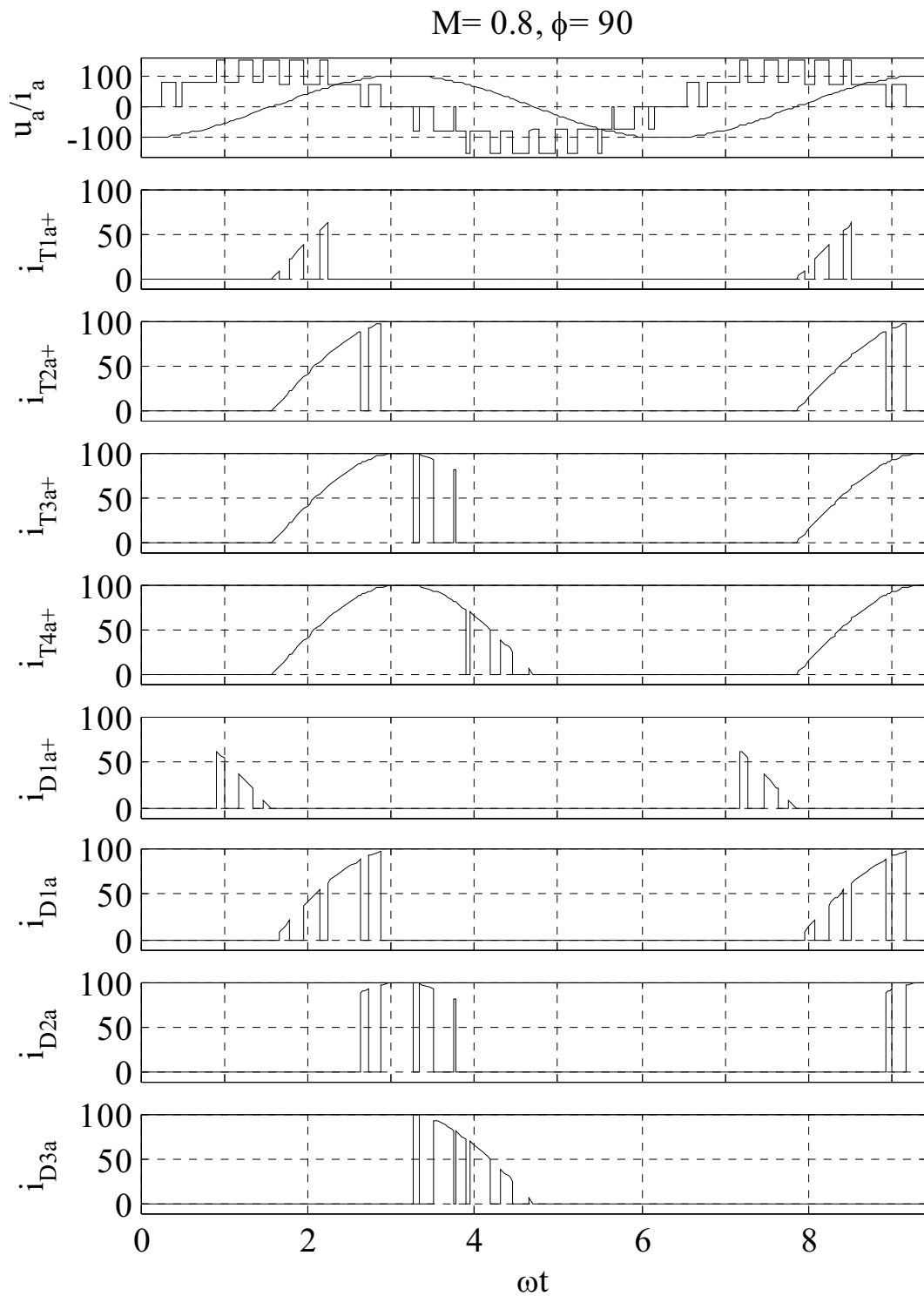


Figure 3.25: Typical output waveforms for a 5-level converter simulated in KREAN.

4 LOSS CALCULATIONS- CASE STUDIES

In the previous chapter a set of analytical loss equations for 4-level and 5-level converters are developed. From this, dimensioning of the switching devices can be done, avoiding time consuming numerical simulations. By the set of equations, calculations can be performed for different parameters. Different topologies at different load conditions and different switching devices can easily be compared.

4.1 Drive Parameters

In this case, a 1 MW drive is considered. The motors main parameters are listed in Table 4-1.

Table 4-1: Motor parameters.

ABB HXR 500LJ2 induction motor	
Output power	1000 [kW]
Nominal voltage	1500 [V] Y-connected
Nominal frequency	50 [Hz]
Nominal current	428 [A]
$\cos\phi$	0.926
Nominal speed	2986 [rpm]

For the semiconductor components, IGBTs from EUPEC are used. The current rating is selected as 800 A. The voltage ratings are selected from the converter topology and the DC-bus voltage. Table 4-2 summarizes the important parameters from the datasheets.

Table 4-2: Components used in the different converters.

Parameter	Topology		
	2-level	3-level	4- and 5-level
IGBT (Eupec)	FZ 800 R33 KF2	FZ 800 R17 KF6B2	FF 800 R12 KL4C
Rated Volt. U_{CEN}	3300V	1700V	1200V
Rated Curr. I_{CN}	800A	800A	800A
IGBT U_f ¹⁾	2.0V	1.4V	1.25V
IGBT r_f ¹⁾	0.0029 Ω	0.0023 Ω	0.0014 Ω
Diode U_f ¹⁾	1.2V	1.0V	1.0V
Diode r_f ¹⁾	0.0020 Ω	0.0014 Ω	0.00090 Ω
IGBT $E_{ON}+E_{OFF}$ ²⁾	2900mJ@1800V	595 mJ@900 V	250mJ@600V
Diode E_{REC} ²⁾	1000mJ@1800V	110mJ@900V	60mJ@600V

¹⁾ @ $T_j = 125^\circ\text{C}$, $U_{GE} = 15\text{V}$ ²⁾ $T_j = 125^\circ\text{C}$, $I_C = I_{CN}$

For simplicity, the freewheeling diode in the IGBT module is used for the clamping diode. This means that the same devices are used in the respective converters. For the 4- and 5-level converters, some of the clamping diodes must block more than the rated voltage, thus a series connection is performed for these devices.

When a set of analytical expressions is developed, it is easy to make comparisons to different converter topologies in a spreadsheet. For comparison, the rest of the parameters are as follows:

- Constant Load and $\cos\phi$: $I_{load}=428\text{ A}$, $\cos\phi=0.93$
- U/f constant control. Modulation index proportional to speed
- Switching frequency 1000 Hz
- DC-bus voltage 2450 V

From Table 4-2, the worst case power losses for the different components can be calculated. The results are shown in Figure 4.1-Figure 4.4, where the conduction losses (left), switching losses (middle) and total losses (right) are plotted with respect to modulation index and load angle. The other parameters are as listed above. For the 2-level converter the worst case component is the transistors, where the switching losses are dominating. As lower voltage IGBTs (1200V and 1700V) are used for the multilevel structures, the conduction losses dominates at this

switching frequency. The most stressed components are thus the inner transistors (e.g. T_{2j+}/T_{1j-} for the 3-level converter).

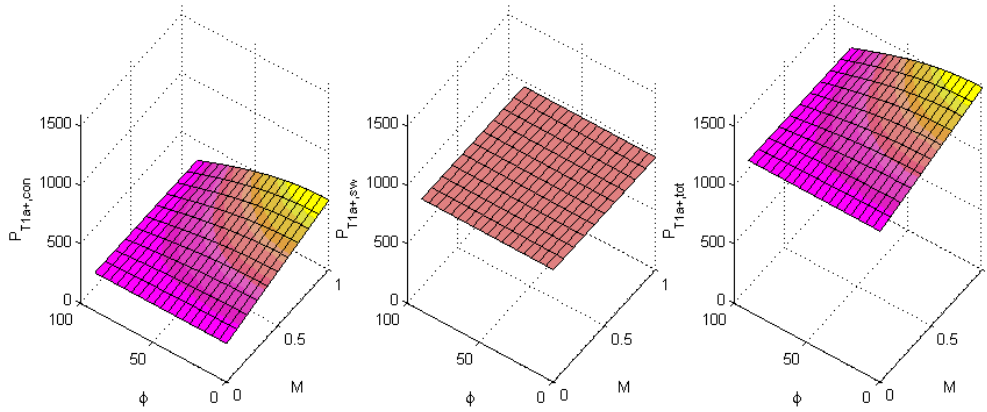


Figure 4.1: Losses in T_{1a+} for the 2-level converter.

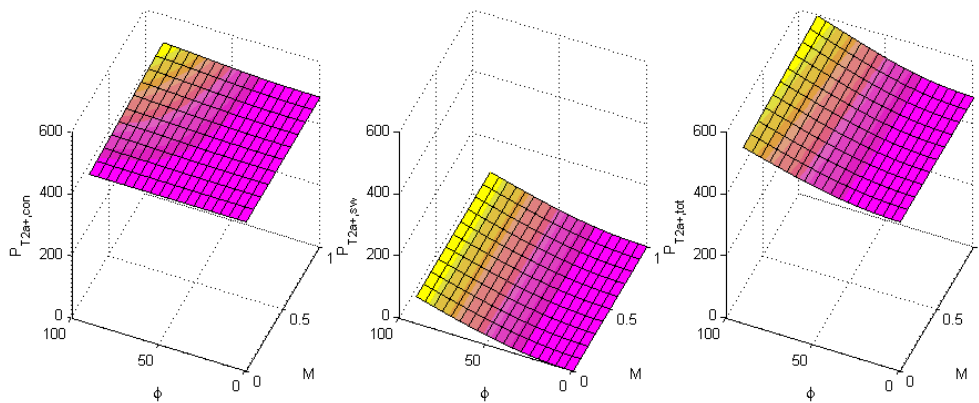


Figure 4.2: Losses in T_{2a+} for the 3-level converter.

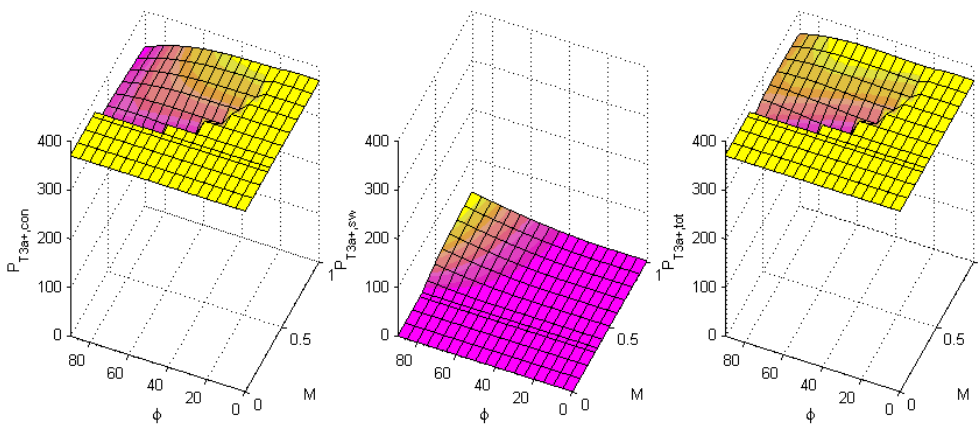


Figure 4.3: Losses in T_{3a+} for the 4-level converter.

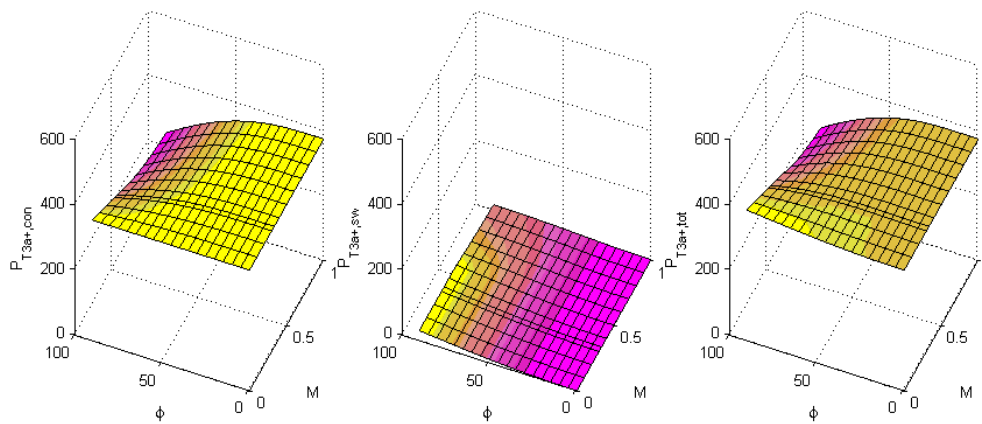


Figure 4.4: Losses in T_{3a+} for the 5-level converter.

4.2 Losses with Constant DC-bus Voltage

Figure 4.5 shows the switching losses for the respective converters. From Table 4-2 it is observed that the 3300V IGBTs used for the 2-level converter have large switching losses caused by the large drift layer needed to block the large voltage. Thus, the 2-level topology will have large switching losses at this voltage level.

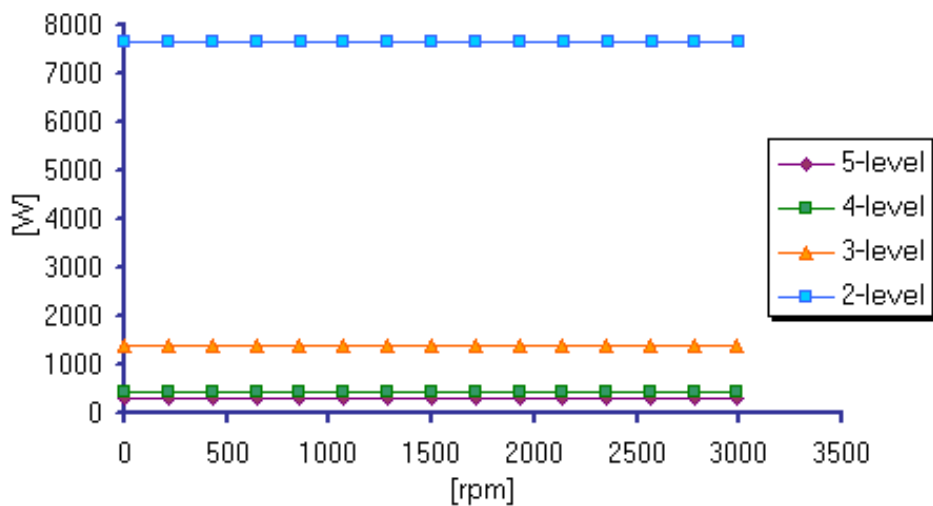


Figure 4.5: Switching losses.

Figure 4.6 shows the conduction losses. Because the 2-level topology has fewer devices, the losses are expected to be small, since the voltage rating doesn't influence the conduction parameters of the IGBTs that much.

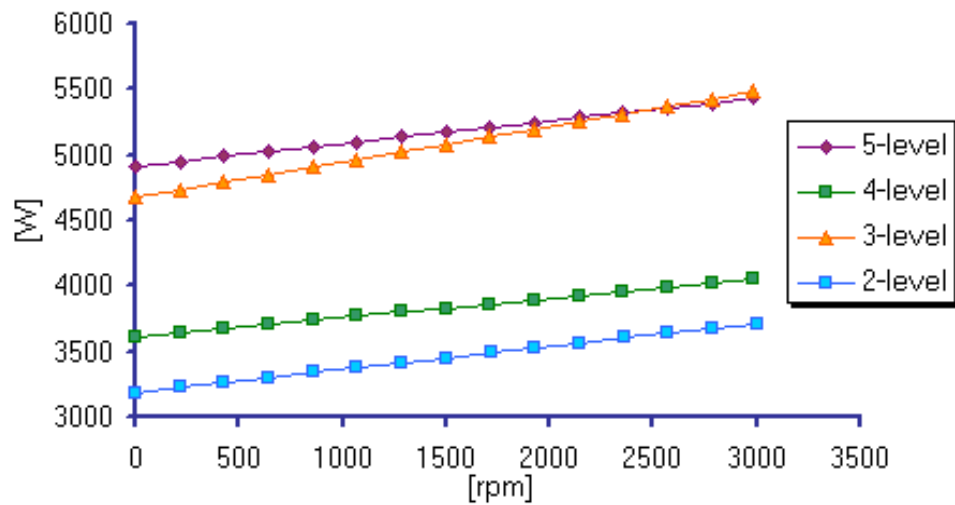


Figure 4.6: Conduction losses.

The relatively large conduction losses for the 5-level converter, is due to the poor utilization of the switches at this voltage level. This will be shown in Chapter 4.3.

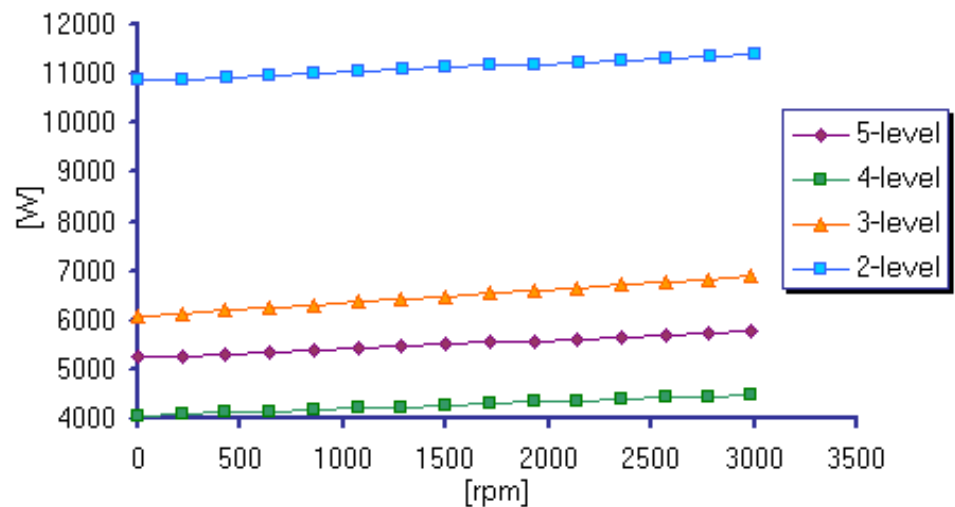


Figure 4.7: Total losses.

Figure 4.7 and Figure 4.8 shows the total losses and the normalized total losses respectively. From this, a reduction in the total losses can be achieved by using a multilevel topology. By using a 3-level converter, a reduction of 40% can be achieved. The 4-level topology is superior to the 5-level topology. This is caused by the use of the same IGBTs for the two topologies. In the next chapter a modified approach will be used, as to utilize the switching devices equally.

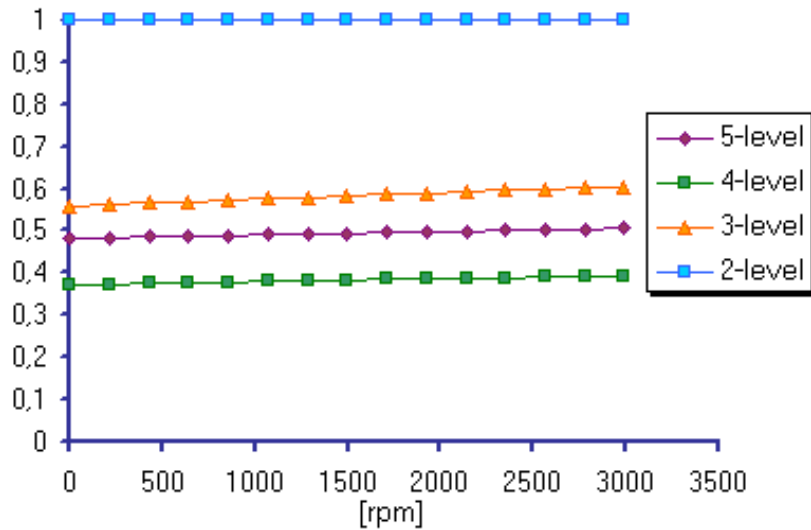


Figure 4.8: Total losses normalized to the 2-level converter.

4.3 Losses at Equal Device Voltage Utilization

In Chapter 4.2, the equal DC-bus voltage and the different IGBT modules used, leads to different device voltage utilization.

Table 4-3 summarized the voltage utilization for the different topologies. In a real converter, the voltage utilization is usually selected to be around 50-70 % of the rated voltage of the switch. The switching causes over voltages across the devices because of stray inductances in the DC-bus structure and in the modules internally during commutation. By use of overvoltage snubbers or intelligent gate driving, the utilization can be increased, but careful design is necessary.

Table 4-3: Voltage utilization for different topologies.

Topology	IGBT voltage rating	DC-bus voltage rating	Voltage utilization
2-level	3300 V	2450 V	0.74
3-level	1700 V	2450 V	0.72
4-level	1200 V	2450 V	0.68
5-level	1200 V	2450 V	0.51

As Table 4-3 shows, the voltage utilization of the 2-, 3- and 4-level converter is close to the limit what is unacceptable. In a real application, overvoltages might occur, and voltage shoot-through can happen. Table 4-4 shows a listing with a more conservative utilization of the devices (0.6). In the third column, the ideal blocking voltage of each IGBT is shown, without any overvoltages owing to the

switching. The total DC-bus voltage, and the maximum line-to-line voltage is shown at sinusoidal PWM, and it is observed that the 5-level converter is much more utilized in this case.

Table 4-4: The different topologies at equal device utilization, (0.6).

Topology	IGBT volt rating	Ideal IGBT volt.	DC-bus volt.	Max. output volt.	Constant load current at max 1 MW output
2-level	3300 V	1980 V	1980 V	1212 V	517 A
3-level	1700 V	1020 V	2040 V	1248 V	502 A
4-level	1200 V	720 V	2160 V	1322 V	474 A
5-level	1200 V	720 V	2880 V	1763 V	355 A

By using the same utilization factor of the voltages, a more proper comparison can be performed. As the DC-bus voltage is changed, the output voltage is changed. The output current of the converter is adjusted so that the output power is the same for the different topologies (right column of Table 4-4), where the maximum output power is 1 MW at $M=1.0$. Other parameters such as switching frequency and $\cos\phi$ are the same as in the pervious chapter: 1kHz and 0.9, respectively. Figure 4.9 to Figure 4.12 show the results.

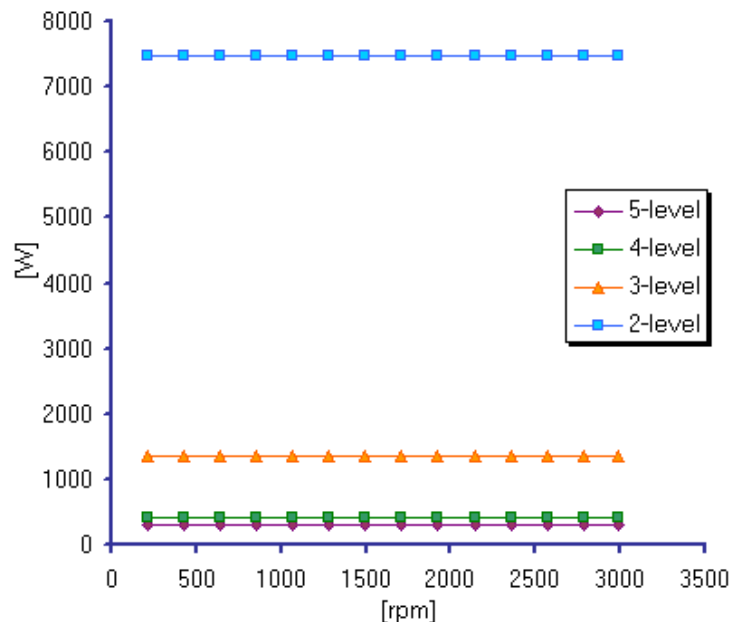


Figure 4.9: Switching losses at equal voltage utilization.

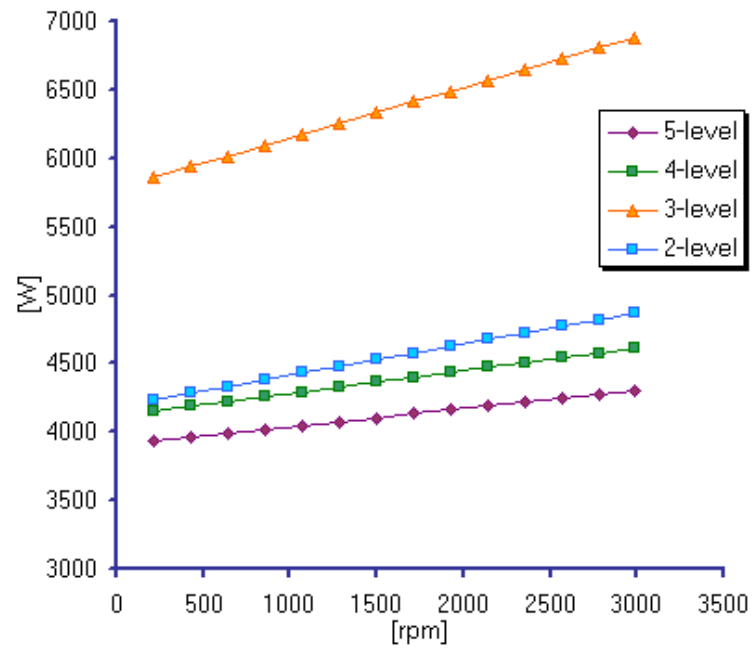


Figure 4.10: Conduction losses at equal voltage utilization.

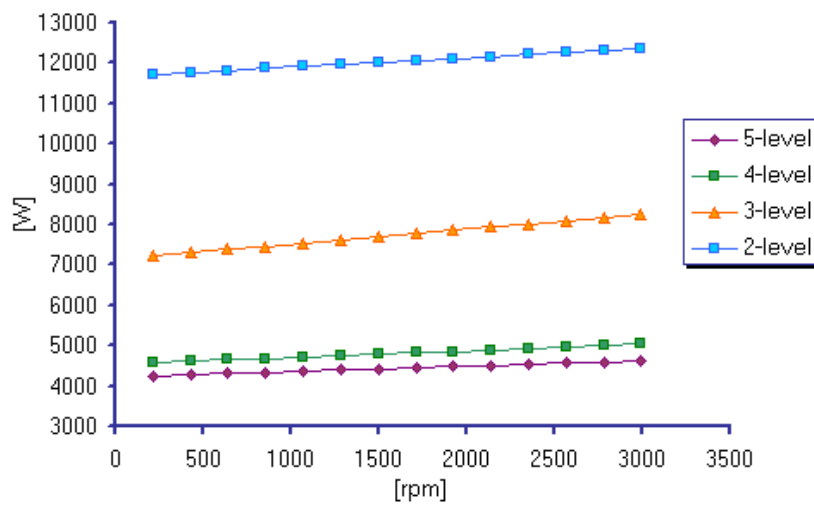


Figure 4.11: Total losses at equal voltage utilization.

From Figure 4.12 it can be observed that by utilizing the switches equally, the 5-level converter has lower losses than the 4-level converter. Again it is observed that at this power and voltage level, the multilevel topologies are superior to the 2-level converter with respect to losses.

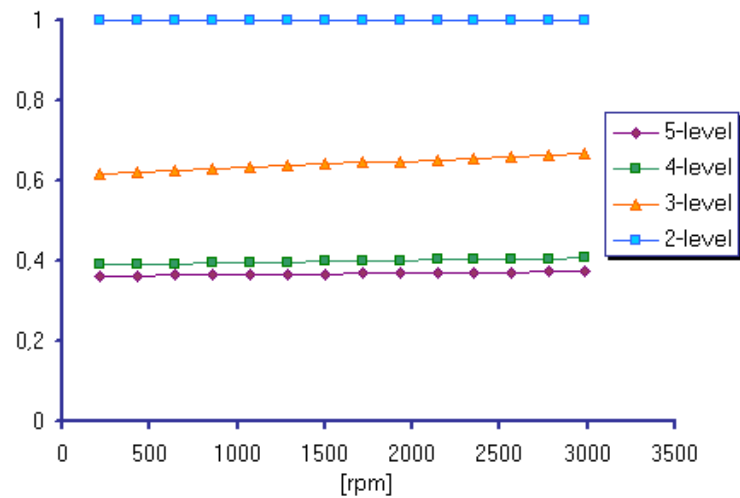


Figure 4.12: Total losses normalized to the 2-level converter at equal voltage utilization.

Since a multilevel structure synthesizes a more sinusoidal shaped output voltage, the switching frequency can be decreased further for the same current ripple at the output, thus the switching losses are reduced further. Figure 4.5 and Figure 4.9 show that the switching losses are a minor part of the total losses in a multilevel converter. By this, the switching frequency can be increased, and the output waveform further enhanced. Hence, the output filter requirements decrease and might be omitted.

4.4 Losses in Medium Voltage Drives

Medium Voltage Drives (MVD) are defined to operate at the line voltage levels 2.3 kV-7.2 kV. The different classes are listed in Table 4-5. For drives from 1 MW to ~10 MW the 2.3 kV, 3.3 kV and the 4.16 kV voltages are used. These drives are usually utilizing a Voltage Source Inverter (VSI). The 6.0 kV and 6.6 kV class are essentially the same, except that they are used for different nominal frequencies (50 and 60 Hz, respectively). This is also true for the 6.9/7.2 kV class. These converters are usually Load Commutated Inverters (LCI), where the output power is in the range 5-50 MW.

A 2.3 kV megawatt converter is used as a case study. The modulation index is kept constant at $M=1.0$. The load is linear increased from 100A-800A, resulting in a maximum output power of 3 MW. The load is scales up from the motor used in Chapter 4.1:

- Maximum output voltage line-line 2300 V
- Maximum output power 3 MW
- Constant $\cos\phi = 0.93$

- U/f constant
- Load is linear from 100A-800A RMS
- Switching frequency 1000 Hz
- DC-bus voltage 3750 V

Table 4-5: Medium voltage drive classes and the semiconductor blocking voltage (at voltage utilization 0.6).

		Rated line-line voltage						
		2.3 kV	3.3 kV	4.16kV	6.0 kV	6.6 kV	6.9 kV	7.2 kV
DC-bus voltage		3.8 kV	5.4 kV	6.8 kV	9.8 kV	10.8 kV	11.3 kV	11.8 kV
Rated IGBT voltage	2-level	6.5 kV						
	3-level	3.3 kV	4.5 kV	5.5 kV				
	4-level	2.5 kV	3.3 kV	4.5 kV	5.5 kV	6.5kV	6.5kV	6.5 kV
	5-level	1.7 kV	2.5 kV	3.3 kV	4.5 kV	4.5 kV	5.5 kV	5.5 kV

Table 4-6: Components used in the 2300V converters.

Parameter	Topology		
	3-level	4-level	5-level
IGBT (Eupec)	FZ 800 R33 KF2	FZ 1000 R25 KF1	FZ 800 R17 KF6B2
Rated Volt. U_{CEN}	3300V	2500V	1700V
Rated Curr. I_{CN}	800A	1000A	800A
IGBT U_f ¹⁾	2.0V	1.6V	1.4V
IGBT r_f ¹⁾	0.0029 Ω	0.0022 Ω	0.0023 Ω
Diode U_f ¹⁾	1.2V	1.0V	1.0V
Diode r_f ¹⁾	0.0020 Ω	0.0013 Ω	0.0014 Ω
IGBT $E_{ON}+E_{OFF}$ ²⁾	2900mJ@1800V	2500 mJ@1200 V	595 mJ@900 V
Diode E_{REC} ²⁾	1000mJ@1800V	700mJ@1200V	110mJ@900V

¹⁾ @ $T_j = 125^\circ\text{C}$, $U_{GE} = 15\text{V}$ ²⁾ @ $T_j = 125^\circ\text{C}$, $I_C = I_{CN}$

The semiconductor devices used are listed in Table 4-6, and the results are shown in Figure 4.13-Figure 4.16. At this voltage, the switching devices utilization is

0.57, 0.5 and 0.55 for the 3-, 4- and 5-level topologies respectively. The 5-level converters devices are better utilized in this case compared to the case in Chapter 4.2. By doing this, the 5-level topology has the lowest losses of the compared topologies. By comparing the normalized losses in Figure 4.16 for the 2300 V drive to Figure 4.12 for the 1 MW drive, the losses for the 4- and 5-level topology compared to the 3-level topology are about the same, 60%.

To summarize, by using a multilevel structure, a decrease in the total losses can be obtained also at this voltage/power level.

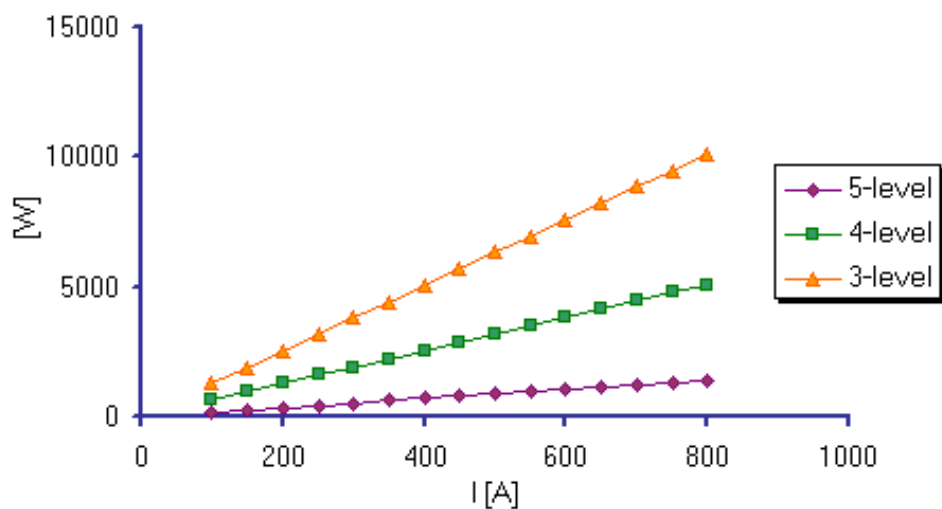


Figure 4.13: Switching losses in 2300 V drive.

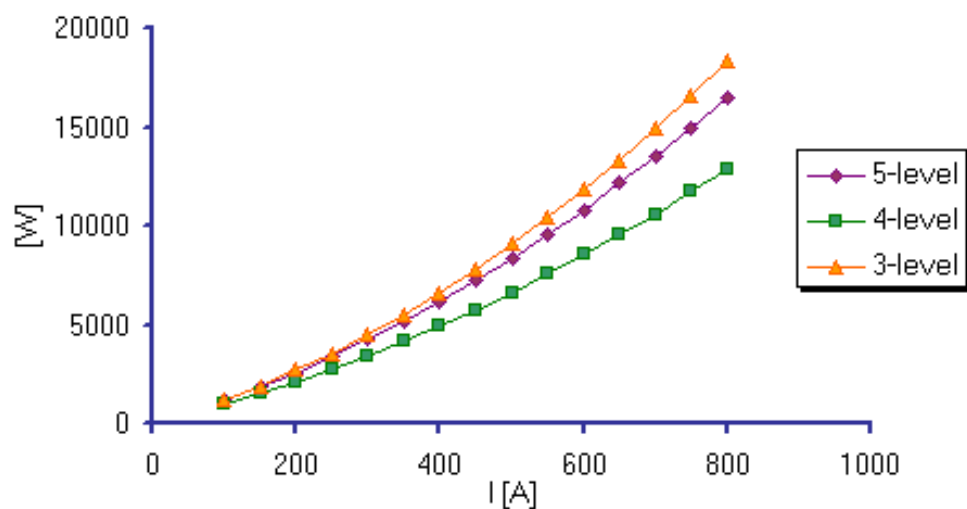


Figure 4.14: Conduction losses in 2300 V drive.

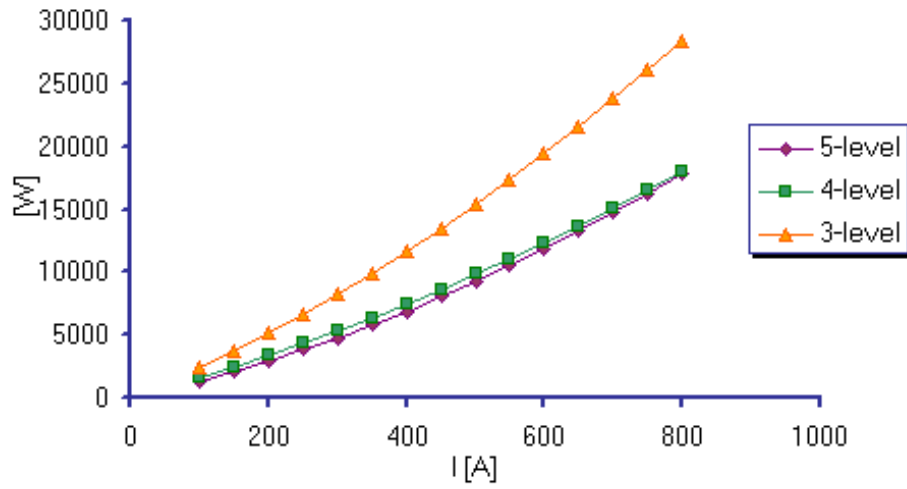


Figure 4.15: Total losses in 2300 V drive.

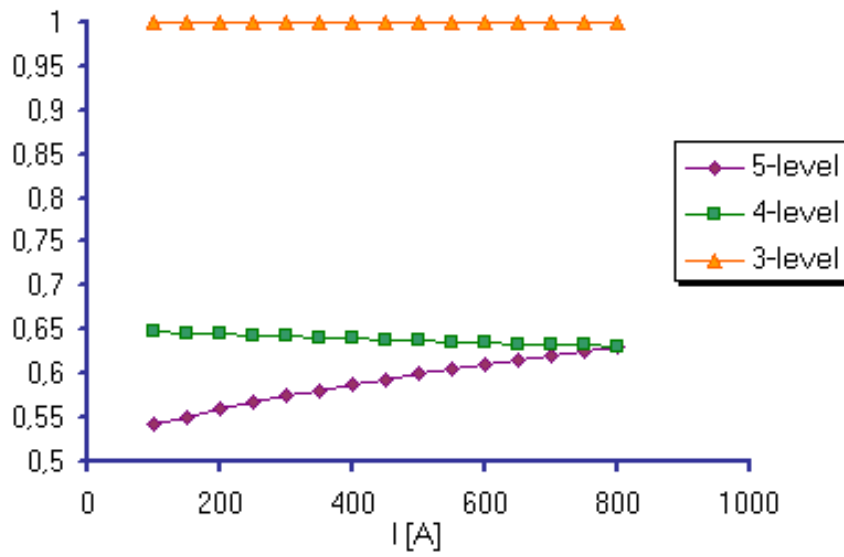


Figure 4.16: Total losses in 2300 V drive normalized to the 3-level drive.

5 CONSTRUCTION OF PROTOTYPES

To verify the theoretical analysis, two different multilevel converters have been designed and built:

- 3-level 3-phase Diode Clamped 400V/40kW IGBT converter
- 5-level 3-phase Diode Clamped 230V/5kW IGBT converter

5.1 3-level 40kW IGBT Converter

A newly developed 2-level converter at the research group [47], is used as a base for this converter design.

5.1.1 Dimensioning of the switching components

By using the analytical calculation for the losses developed, it's easier to estimate the temperatures in the switching devices. The module available and most suitable for the converter at the construction time was the Semikron SKM 200 GB 123 [48]. This is a 1200V/200A IGBT with two IGBTs/diodes in each module. The electrical parameters are listed in Table 5-1. For simplicity, the IGBT module is also used as clamping diodes.

To calculate the temperatures in the modules, also the thermal parameters of the device, heat sink and surroundings are needed. Thermal calculations in its least complicated form can be done by an thermal equivalent electric circuit as shown in Figure 5.1 (right). The power loss is equivalent to a current source. According to the thermal resistance R_{th} of the different parts of the system, the temperature can be calculated (analog to a voltage). Also the partitioning of the modules will influence the temperatures. In this design, the partitioning of the modules is done as shown in Figure 5.1 (left). By this, the modules in the bridge-leg will have the same thermal stresses because of symmetry. The heat sink used for the converter is the LA V 15-400 from Fisher Elektronik [49].

Table 5-1: Main parameters for Semikron SKM 200 GB 123.

Semikron SKM 200 GB 123			
Rated Volt. U_{CEN}	1200V	Diode U_f ¹⁾	1.15V
Rated Curr. I_{CN}	200A	Diode r_f ¹⁾	0.0045 Ω
IGBT U_f ¹⁾	1.8V	IGBT $E_{ON}+E_{OFF}$ ²⁾	77mJ@600V
IGBT r_f ¹⁾	0.009 Ω	Diode E_{REC} ²⁾	7.5mJ@600V
$R_{thjc,igbt}$ ³⁾	0.09 C ^o /W	R_{thch} ³⁾	0.038 C ^o /W
$R_{thjc,diode}$ ³⁾	0.25 C ^o /W		

¹⁾ @ $T_j = 125^\circ\text{C}$, $U_{GE} = 15\text{V}$ ²⁾ @ $T_j = 125^\circ\text{C}$, $I_C = I_{CN}$ ³⁾ see Figure 5.1 (left)

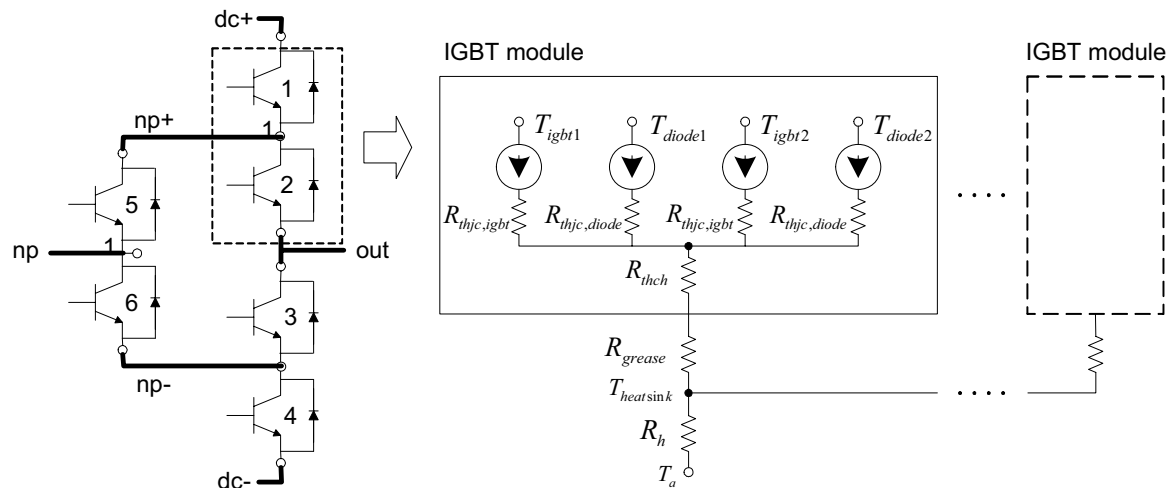


Figure 5.1: Module partitioning for one phase (left). Thermal equivalent circuit (right).

Thermal resistance of the LA V 15-400 is 0.045 C^o/W, and the thermal grease resistance is 0.005 C^o/W. DC-bus voltage is 540V, switching frequency is 1kHz. Output power at max. speed is 40kW ($I_{load}=75\text{A}$, $\cos\phi=0.9$), and the ambient temperature $T_a=25\text{C}^\circ$. Figure 5.2 and Figure 5.3 show the total power losses and the temperatures in the components respectively. The very low losses in the freewheeling diodes D_1 - D_4 are caused by the high power factor. From the figures it can be seen that the converter can handle this power level. Temperatures are under 110 C^o, which is a good margin from critical temperature at 125C^o.

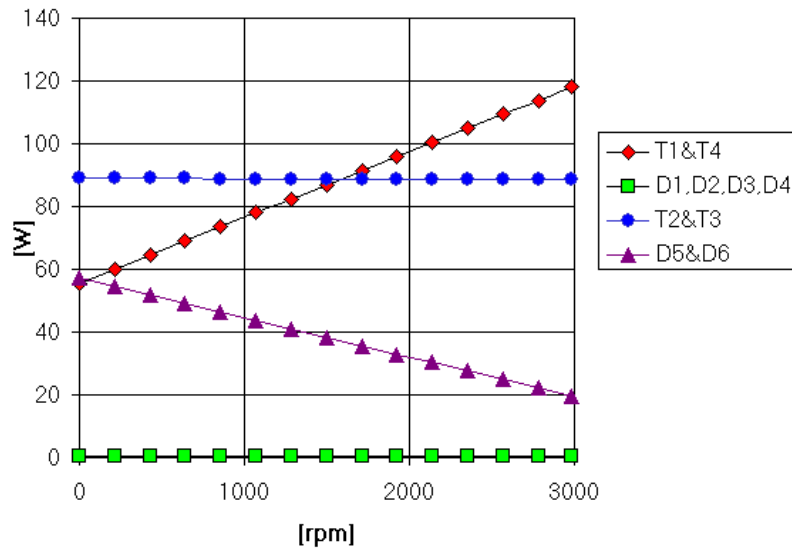


Figure 5.2: Total power losses in the respective components.

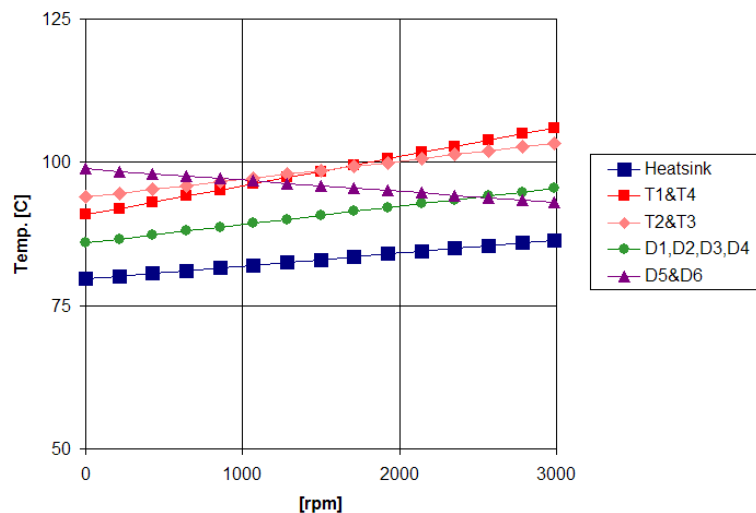


Figure 5.3: Temperatures in switching components.

5.1.2 Sizing of the DC-bus capacitors

In [44], an analytical expression for the total RMS current in the capacitors is found. The generalized expression for the power losses in a capacitor is:

$$P_{cap,tot} = \sum_{n=1} ESR_n I_{cap,rms,n}^2 \quad (5.1)$$

If the ESR (Equivalent Series Resistance) is independent of frequency, the total RMS current can be used. In electrolytic capacitors this is not true. In this converter, PEH 169 VV 433GQ electrolytics from RIFA are used, in Figure 5.4, the ESR is plotted as a function of the frequency.

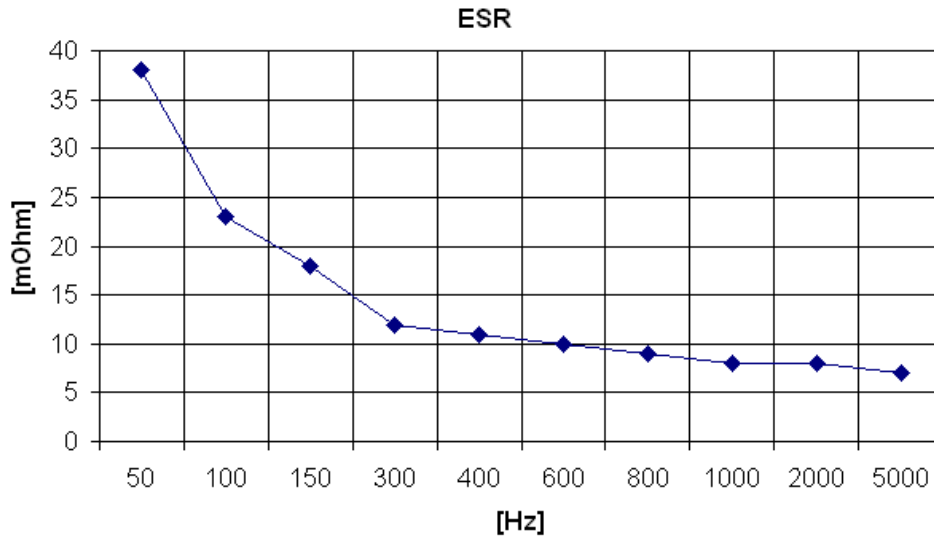


Figure 5.4: ESR(f) for RIFA PEH 169 VV 433GQ.

From [44], the worst case for the capacitor current is for $M = \sqrt{3}/3$ and $\cos\phi = 1$. This case is then simulated in KREAN, and the current harmonics are used in Eq.(5.1). By using 2 capacitors in parallel, and 2 in series with a thermal resistance of $2\text{ C}^\circ/\text{W}$, the hotspot temperature of the capacitors becomes 61 C° , which is acceptable.

5.1.3 Schematic overview of the components

A simplified schematic view of the 3-level converter is shown in Figure 5.5.

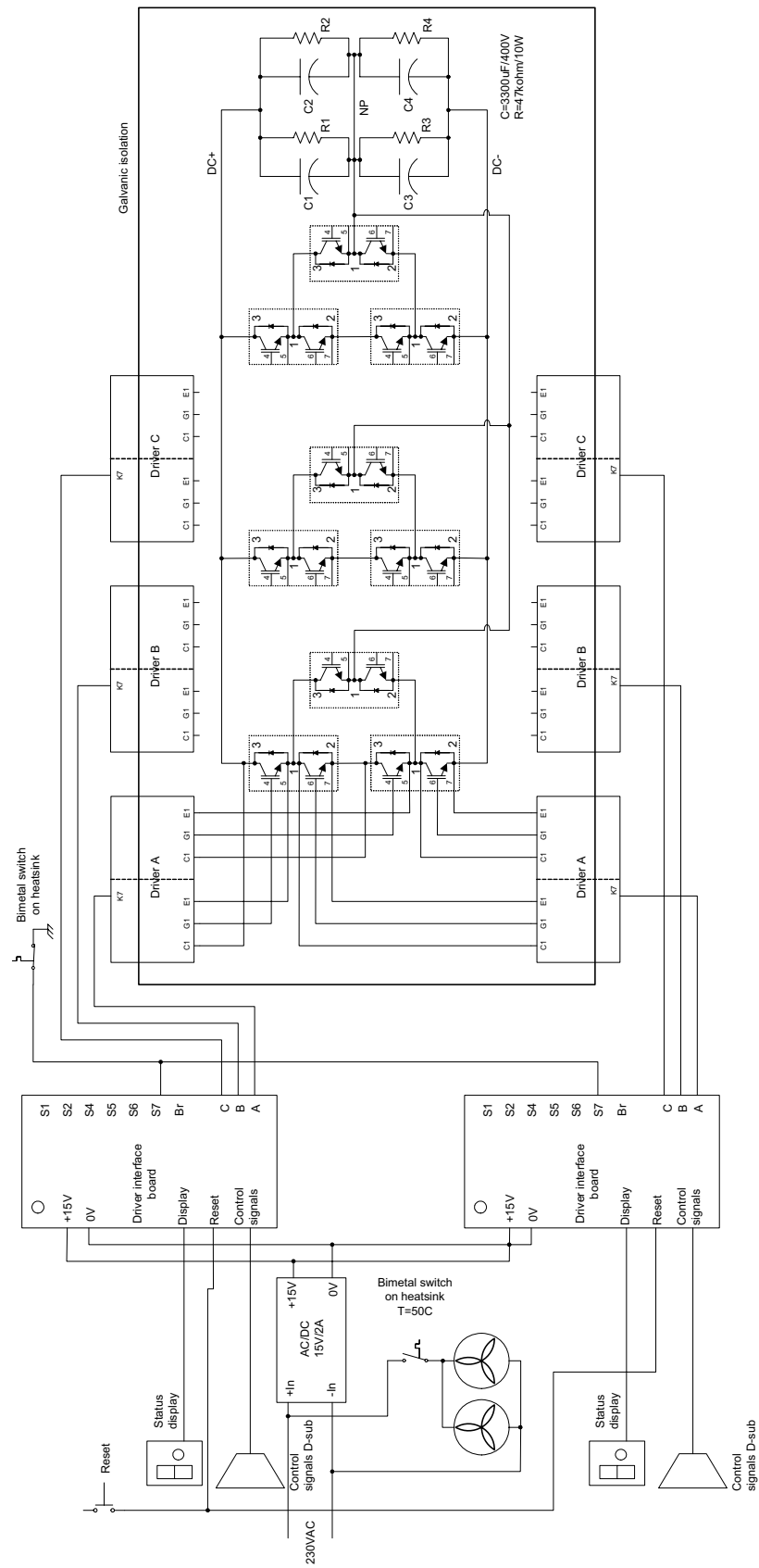


Figure 5.5: Schematic of the converter.

5.1.4 DC-bus layout

Because of the many devices, 18 in total for a 3-phase converter, the interconnections of the different modules are essential to obtain a low-inductance DC-bus. The final layout is shown in Figure 5.6.

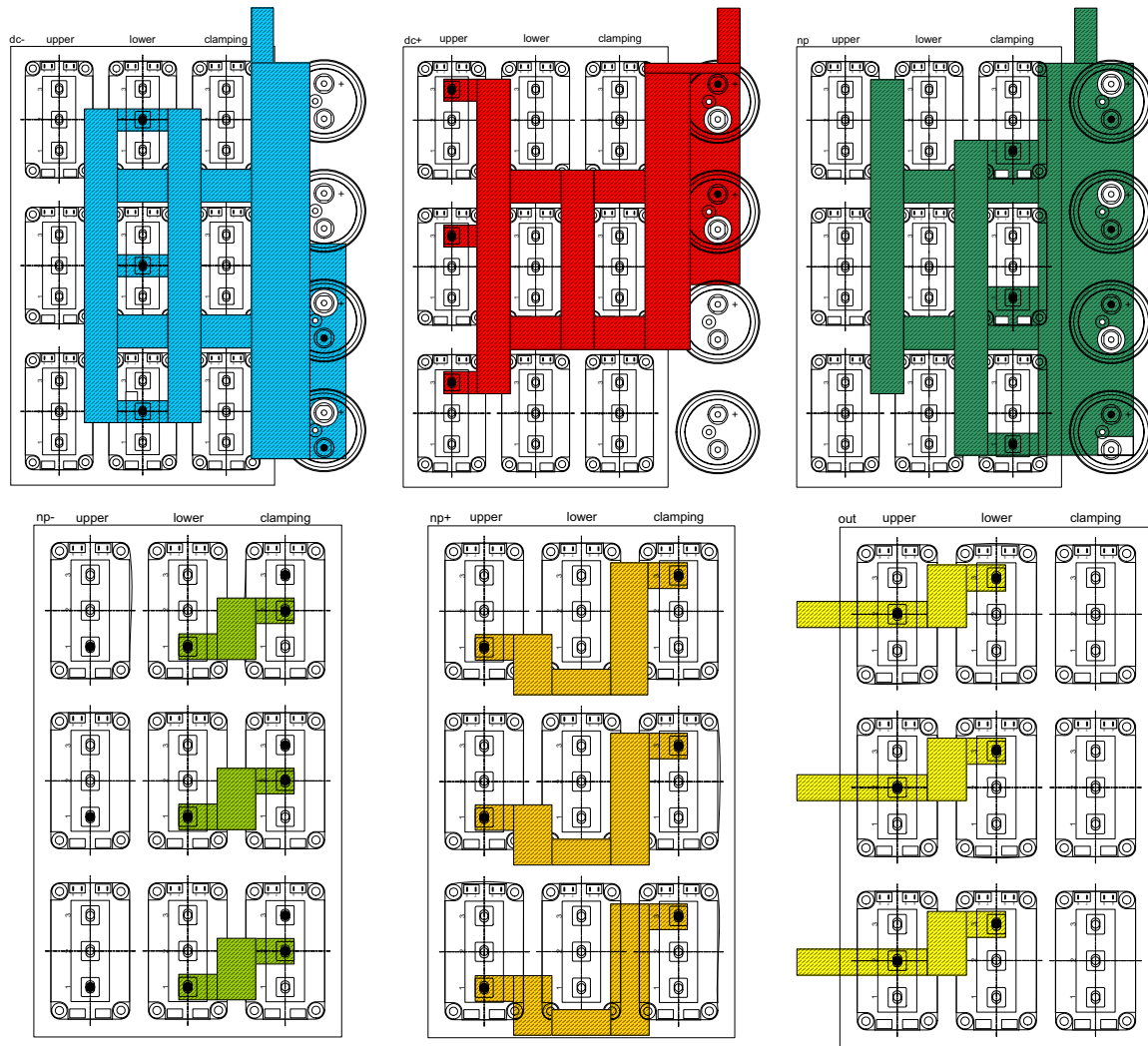


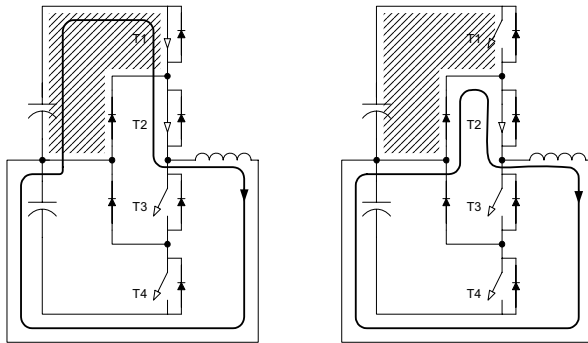
Figure 5.6: DC-bus layout (referring to Figure 5.1).

5.1.5 Dual-pulse switching

To verify the design of the DC-bus, a method called dual-pulse testing can be used. An air inductor of 75 μ H is used as a load. By switching the transistor on/off with two narrow pulses (about 20-30 μ s), the current through the inductor is ramped up, and turn-off at rated current can be investigated. This cycle is repeated at low frequency (typical 1Hz), thus the average losses are minimal.

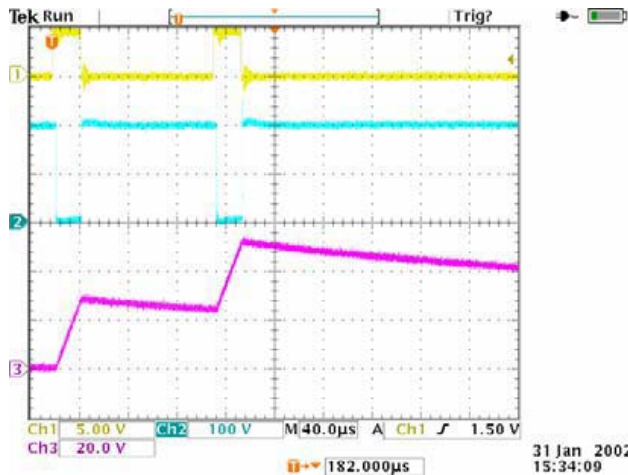
Figure 5.7 shows how to test the upper commutation path, and the principle of dual-pulse testing is shown in Figure 5.8. Figure 5.9 shows the voltage at turn-off for T1. An overshoot in the voltage across T1 is caused by the leakage inductance

in the commutation path. The maximum voltage is 504V, which is acceptable at this current level. If unacceptable voltages occur, the turn-off can be slowed down by increasing the gate-resistance of the gate-driver.



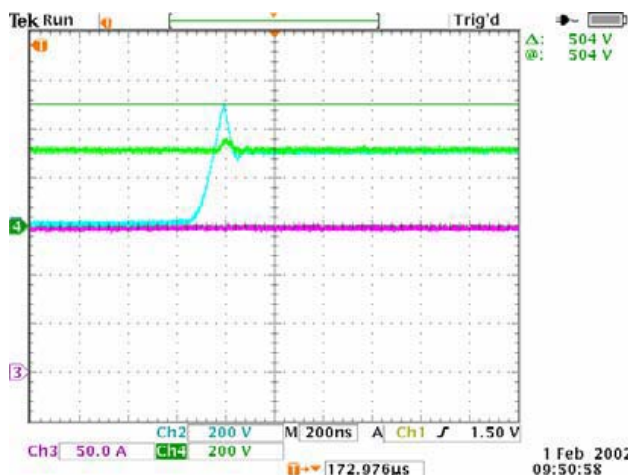
T2 on and T1 is switching. 300 VDC between DC+ og NP.

Figure 5.7: Upper commutation path.



CH1: gate T1
 CH2: T1 100V/div
 CH3: Inductor current 20A/div

Figure 5.8: Dual-pulse example.

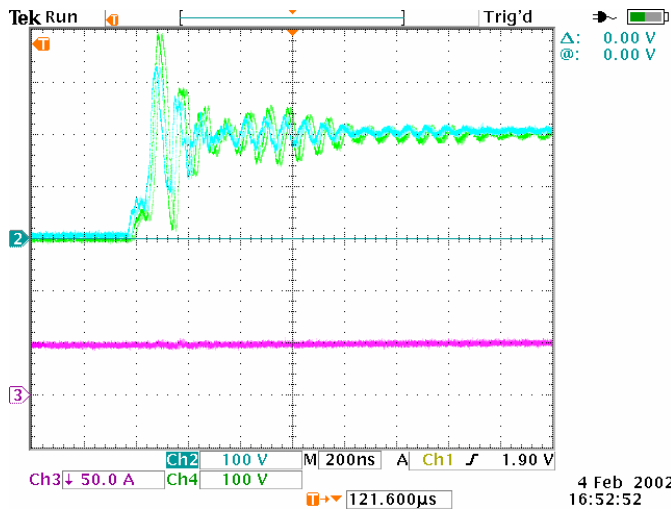


T1 Turnoff at 150A and 300VDC

CH2: T1 200V/div
 CH3: Inductor current 50A/div
 CH4: DC+ NP voltage 200V/div

Figure 5.9: T1 turn-off.

Figure 5.10 shows the turn-off of the upper clamping diode, the ringing in the waveform is caused by the reverse recovery in the diode.



Turn-off for upper clamping diode at 200 VDC (400 VDC DC+, DC-)

CH2: upper cl. diode 100 V/div

CH3: Inductor current 50A/div

Figure 5.10: Turn-off for upper clamping diode.

For testing of the leakage inductances in the other commutation path, the converter must be configured as shown in Figure 5.11.

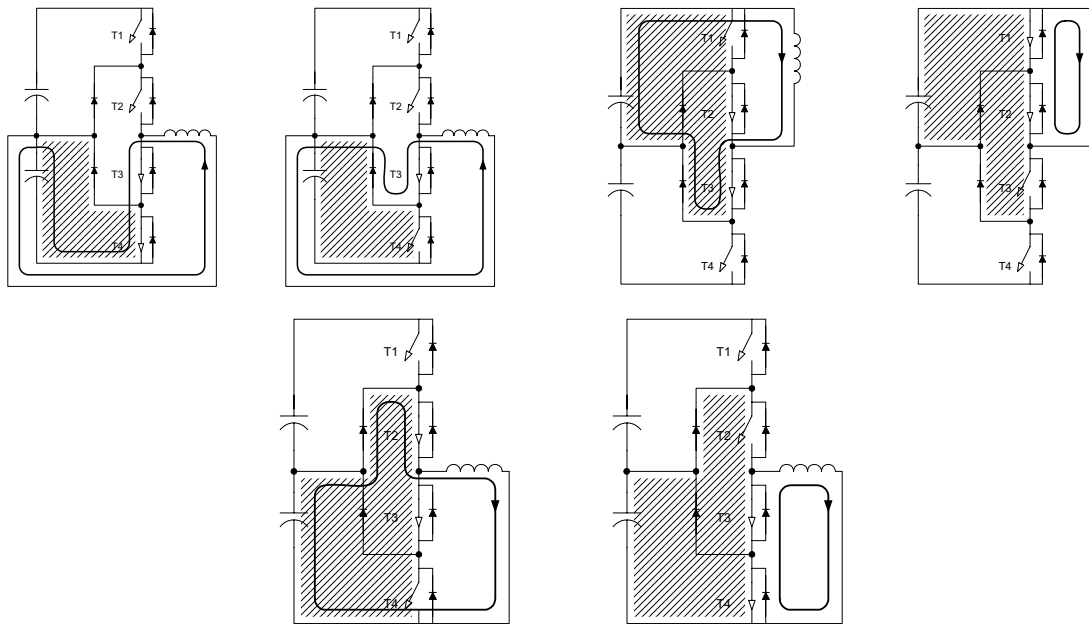


Figure 5.11: Different configurations for testing of commutation- paths.

The waveforms for these configurations are more or less equal to the first configuration, and over-voltages are within the safe operating areas of the devices.

Pictures of the converter

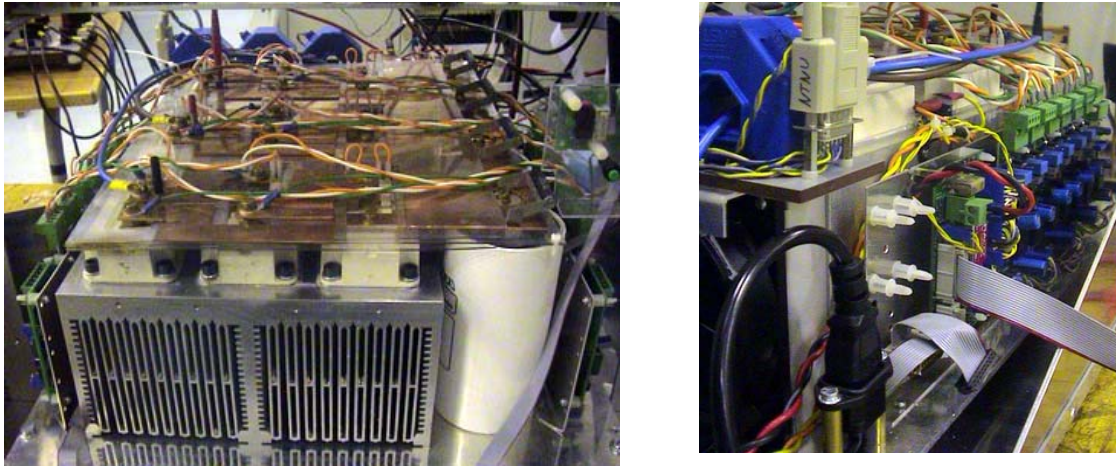


Figure 5.12: Picture of 3-level converter, front (left) and side (right).

5.2 5-level 3kW IGBT Converter

To verify further testing of the theory, a cheap and small 5-level converter has been constructed. Figure 5.13 shows a schematic of the converter.

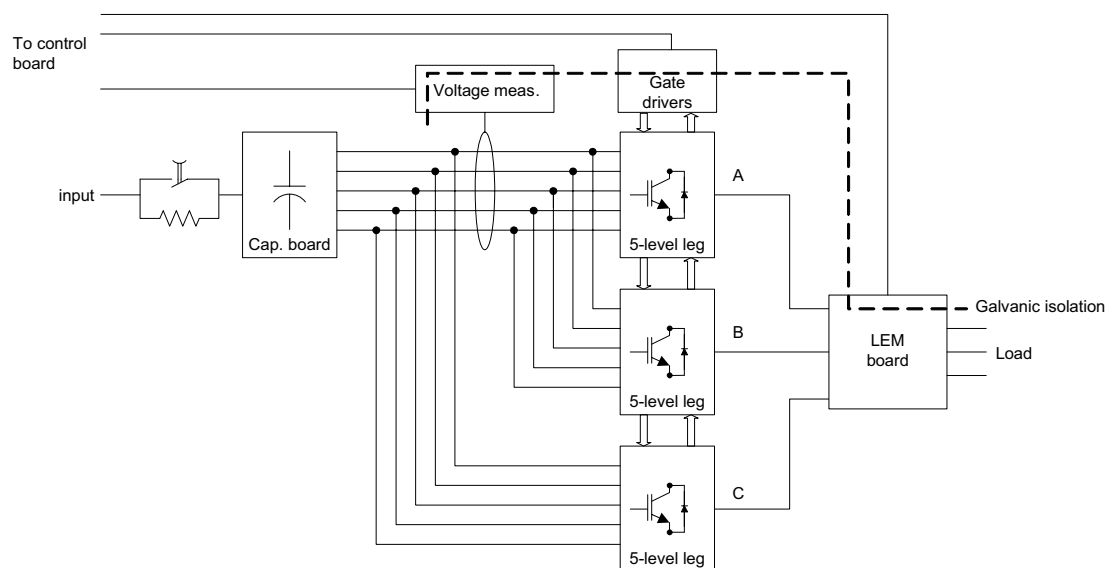


Figure 5.13: Simplified schematic overview of 5-level converter.

5.2.1 Main power circuit

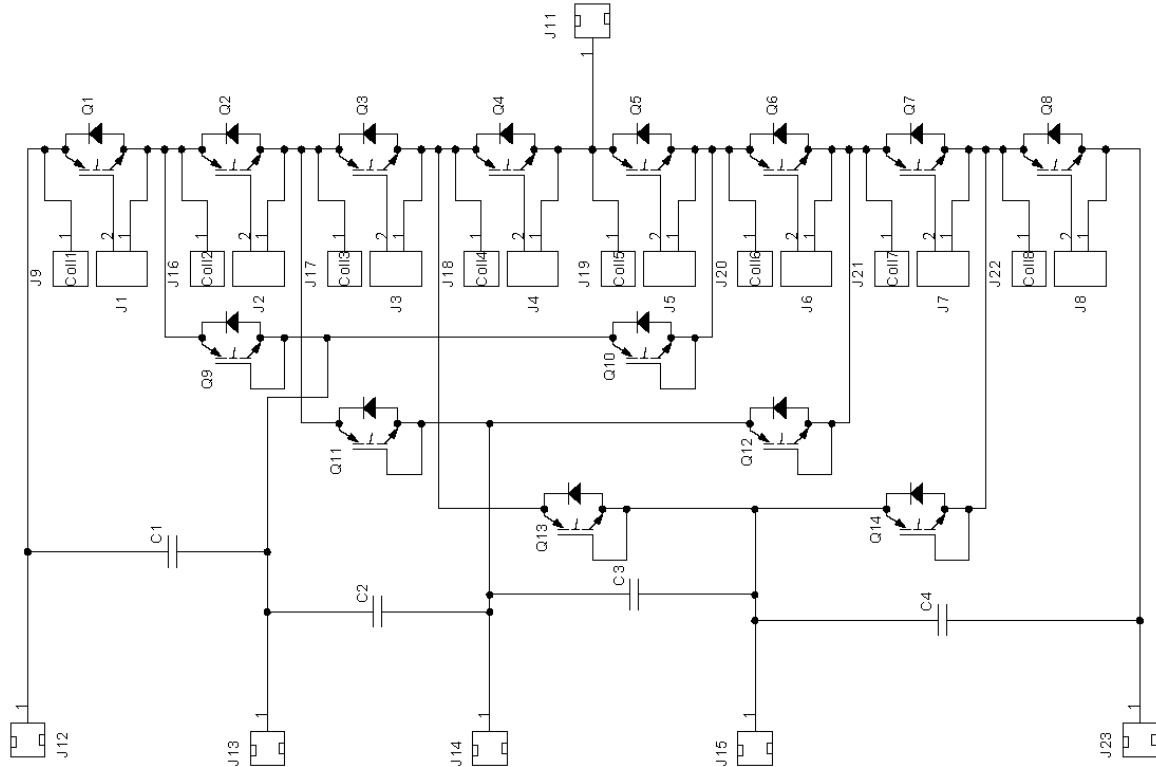


Figure 5.14: Main power circuit.

The main power circuit is constructed with the IRG4IBC30FD 600V/17A IGBT from IRF [51]. The capacitors on the main power board are polyester capacitors to limit possible over-voltages at turn off. The main DC-bus capacitors are located on it's own board (Figure 5.13). One main board forms one phase of the converter, thus three boards are needed for 3-phase power conversion. For clamping diodes, the same IGBTs are used, only with a shorted gate.

5.2.2 Gate driver

A 5-level 3-phase topology needs in total 24 gate drivers. Hence a small and cheap gate driver is constructed. It is based on an integrated dual driver from Agilent [52]. Both turn-on delay (1 μ s) and over-current protection (10A) are incorporated in the design. Figure 5.15 shows the schematic of the driver.

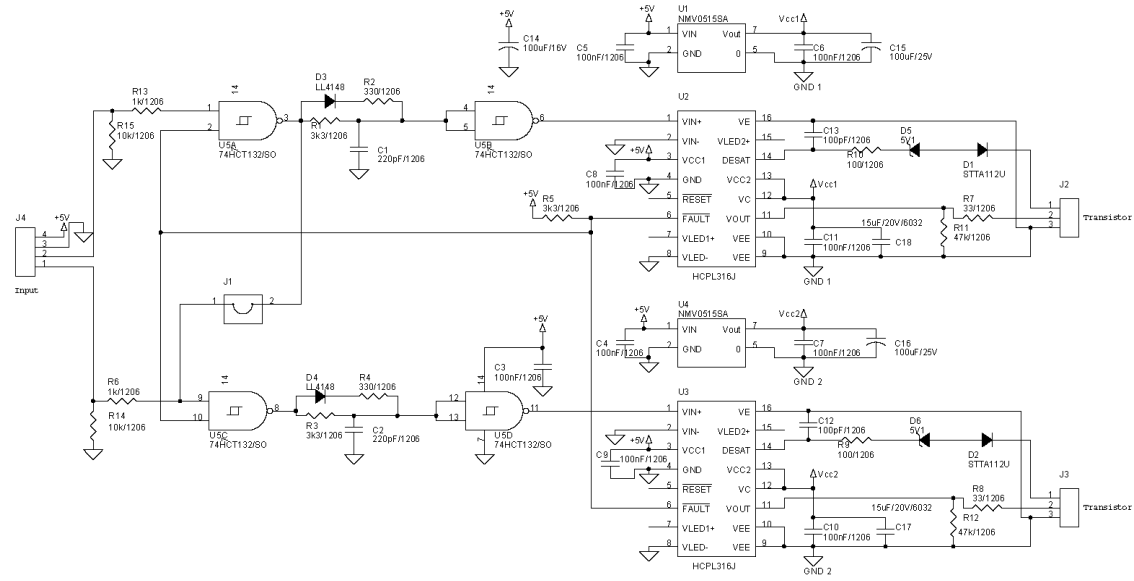


Figure 5.15: Gate driver.

Pictures of the converter

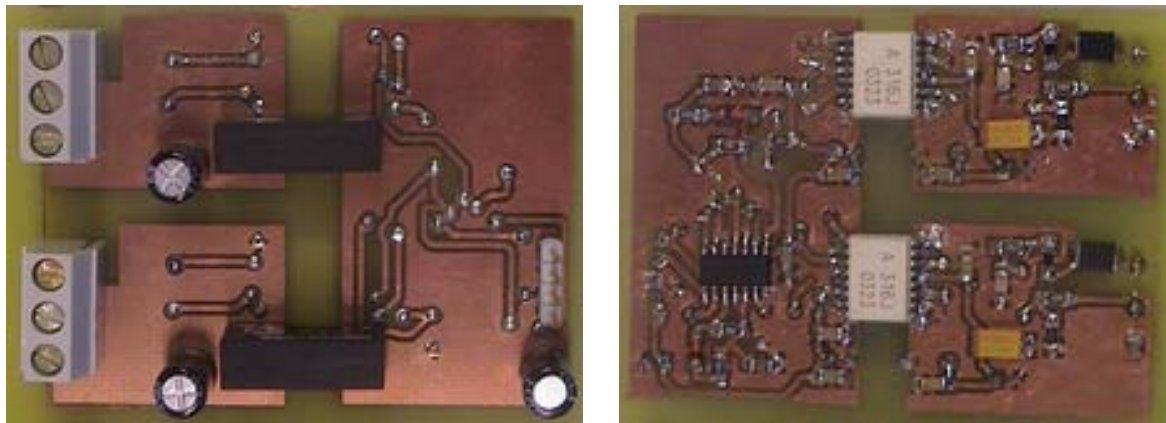


Figure 5.16: Picture of gate driver, top side (left), bottom side (right).



Figure 5.17: Pictures of the 5-level converter.

6 HARMONICS

Because of the stepwise synthesized output waveform of a multilevel converter, a more sinusoidal waveform is generated, creating a number of advantages. The stepwise waveform reduces the dv/dt of the output voltage. This can reduce the capacitive currents, and lifetime of cable and motor isolation will increase. For a drive application a lower dv/dt will also reduce bearing current problems.

The reduced voltage distortion will also reduce the current ripple, and hence the need for a output filter will decrease or disappear completely. Also EMC/EMI concerns are reduced.

6.1 Harmonic Current

In an electrical motor drive, the leakage inductance of the machine and the inertia of the mechanical system acts as a low-pass filter for the harmonic components generated by the converter [53]. In spite of this, some distortion will remain, giving harmonic losses and fluctuations in the electromagnetic torque. The harmonic currents primarily determine the copper losses of the machine.

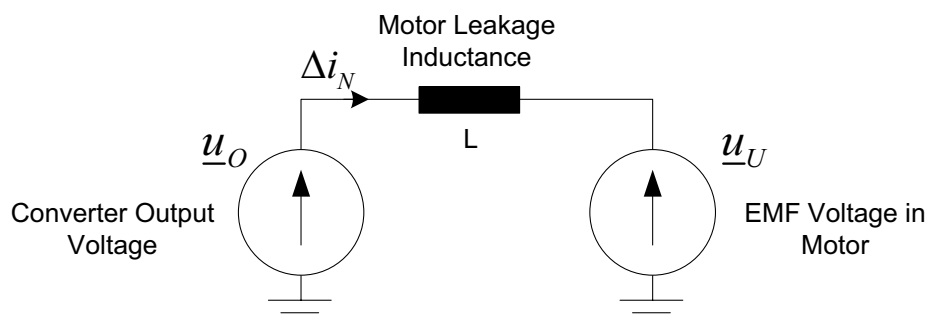


Figure 6.1: Equivalent circuit of an AC load.

An equivalent circuit for an AC machine is shown in Figure 6.1. \underline{u}_O is the output voltage of the converter, and \underline{u}_U is the induced voltage in the machine. L is the leakage inductance in the machine. The equivalent circuit can also be used for a

grid connected converter, where \underline{u}_U is the grid voltage, and L the line inductance. Δi_N is the ripple current.

6.2 Analytical Calculations of harmonic current for 3-level PWM

In [55], analytical equations for the harmonic current in a 2-level converter for several PWM strategies is analysed. Investigations for a 3-level converter is performed in [56] and [57] below, and repeated here. This is for pure cosine/sinusoidal modulation only. In addition analytical calculation for 3rd harmonic injection is performed in this chapter. The method to compute the equations is based upon previous work done in [55], and the equivalent circuit is as shown in Figure 6.1.

6.2.1 Symmetry and space vectors

Because of symmetry, it is sufficient to analyse a 60° interval as seen in Figure 6.2. The output state space vectors from the converter can be expressed as [55]:

$$\underline{u}_o = \frac{2}{3} \left(u_a + \underline{a}u_b + \underline{a}^2u_c \right) \quad , \quad \underline{a} = \left(-\frac{1}{2} + j\frac{\sqrt{3}}{2} \right) \quad (6.1)$$

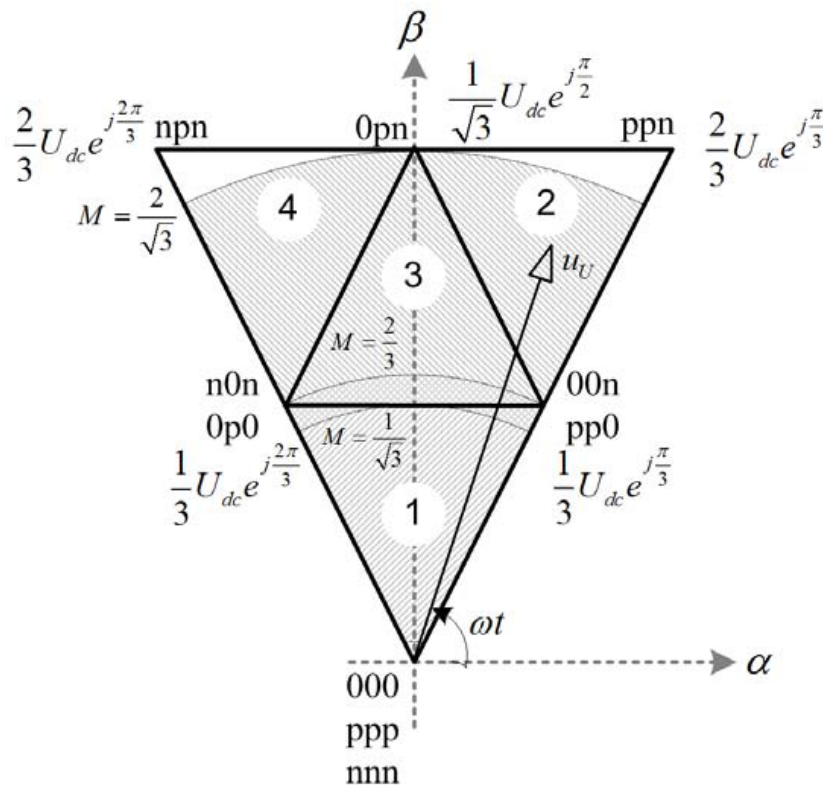


Figure 6.2: Output space vectors in a 60° interval.

The total space vector is a function of the duty ratio of each bridge leg and the space vectors corresponding to the apexes of the triangle. The function is depending on which area the travelling space vector is in. For \underline{u}_O in area 2:

$$\underline{u}_{O,2} = d_{oon} \underline{u}_{oon} + d_{opn} \underline{u}_{opn} + d_{ppn} \cdot \underline{u}_{ppn} + d_{ppo} \cdot \underline{u}_{ppo} \quad (6.2)$$

d_{xxx} ($x=0, n, p$) is the duty cycle of each voltage vector within a switching interval. To analyse the ripple current, the switching intervals must be analysed for every area in Figure 6.2. This is done in [44] and presented in Table 6-1.

Table 6-1: Switching sequences.

Area	Angle	$t_\mu = 0$	Switching sequence			$t_\mu = T_{sw}/2$
1	$\pi/3$ to $\pi/2$	00n	000	0p0	pp0	
1	$\pi/2$ to $2\pi/3$	n0n	00n	000	0p0	
2	$\pi/3$ to $\varphi(M)$	00n	0pn	ppn	pp0	
3	$\varphi(M)$ to $\pi/2$	00n	0pn	0p0	pp0	
3	$\pi/2$ to $\varphi(M)$	n0n	00n	0pn	0p0	
4	$\varphi(M)$ to $2\pi/3$	n0n	npn	0pn	0p0	

E.g: $0pn$ means that bridge leg a is connected to the neutral point, bridge leg b and bridge leg c are connected to the positive and negative DC-bus respectively.

6.2.2 Method of derivation

Three different calculations exist, depending on the modulation index, M . The three sectors are depicted in Figure 6.2. From the equivalent scheme, the ripple current can be derived from [55]:

$$\frac{d\underline{\Delta i}_N}{dt_\mu} = \frac{1}{L} [\underline{u}_O - \underline{u}_U(\tau)] \quad (6.3)$$

t_μ is the microscopic time within a switching interval, between 0 and T_{sw} . The following derivation of currents must be done in every area in Figure 6.2, below are listed the ripple currents in area 2:

$$\begin{aligned}
\underline{\Delta i}_{Nt\mu 1}(\tau) &= d_{oop} \left[\underline{u}_{oop} - \underline{u}_{O,2}(\tau) \right] \frac{T_{sw}}{2L} \\
\underline{\Delta i}_{Nt\mu 2}(\tau) &= \underline{\Delta i}_{Nt\mu 1}(\tau) + d_{opn} \left[\underline{u}_{opn} - \underline{u}_{O,2}(\tau) \right] \frac{T_{sw}}{2L} \\
\underline{\Delta i}_{Nt\mu 3}(\tau) &= \underline{\Delta i}_{Nt\mu 2}(\tau) + d_{ppn} \left[\underline{u}_{ppn} - \underline{u}_{O,2}(\tau) \right] \frac{T_{sw}}{2L} \\
\underline{\Delta i}_{NtTsw/2}(\tau) &= \underline{\Delta i}_{Nt\mu 3}(\tau) + d_{ppo} \left[\underline{u}_{ppo} - \underline{u}_{O,2}(\tau) \right] \frac{T_{sw}}{2L} = 0
\end{aligned} \tag{6.4}$$

Eq.(6.4) is decomposed into the stator oriented coordinate system by:

$$\begin{aligned}
\Delta i_{Nt\mu x, \alpha}(\tau) &= \text{Re}(\underline{\Delta i}_{Nt\mu x}(\tau)) \\
\Delta i_{Nt\mu x, \beta}(\tau) &= \text{Im}(\underline{\Delta i}_{Nt\mu x}(\tau))
\end{aligned} \tag{6.5}$$

The sum of the squares of the phase currents can be transformed to the stator oriented coordinate system α and β [55].

$$\Delta i_{N,R}^2 + \Delta i_{N,S}^2 + \Delta i_{N,T}^2 = \frac{3}{2} \left[\Delta i_{N,\alpha}^2 + \Delta i_{N,\beta}^2 \right] = \frac{3}{2} |\Delta \underline{i}_N|^2 \tag{6.6}$$

The microscopic derivation of the ripple current within a switching interval is:

$$\begin{aligned}
&\frac{1}{t_{\mu,i+1} - t_{\mu}} \int_{t_{\mu}}^{t_{\mu,i+1}} \left[\Delta i_{N\alpha}^2(t_{\mu}) + \Delta i_{N\beta}^2(t_{\mu}) \right] dt_{\mu} \\
&= \frac{1}{3} \left[\begin{aligned} &\Delta i_{N\alpha,i+1}^2 + \Delta i_{N\alpha,i+1} \Delta i_{N\alpha,i} + \Delta i_{N\alpha,i}^2 \\ &+ \Delta i_{N\beta,i+1}^2 + \Delta i_{N\beta\alpha,i+1} \Delta i_{N\beta,i} + \Delta i_{N\beta,i}^2 \end{aligned} \right]
\end{aligned} \tag{6.7}$$

The local RMS values (related to half a switching interval) of the current ripple can be expressed as shown in Eq.(6.8) for area 2:

$$\begin{aligned}
\Delta i_{N,abc,rms}^2(\tau) &= \frac{2}{T_{sw}} \int_0^{T_{sw}/2} \left[\Delta i_{N,a}^2(t_{\mu}) + \Delta i_{N,b}^2(t_{\mu}) + \Delta i_{N,c}^2(t_{\mu}) \right] dt_{\mu} \\
&= \frac{3}{T_{sw}} \int_0^{T_{sw}/2} \left[\Delta i_{N,\alpha}^2(t_{\mu}) + \Delta i_{N,\beta}^2(t_{\mu}) \right] dt_{\mu}
\end{aligned} \tag{6.8}$$

Since the modulation methods have sixfold space symmetry, the global RMS currents must be integrated over the entire 60° interval and divided by 3:

$$\Delta I_{N,rms}^2 = \frac{1}{3} \frac{3}{\pi} \int_{\pi/3}^{2\pi/3} \Delta i_{N,abc,rms}^2 d\omega t \tag{6.9}$$

From the above discussion, it is now possible to develop expressions for any kind of sinusoidal control voltages with any kind of additional zero sequence voltage.

6.2.3 Analytical equations for pure sinusoidal CBPWM

The simplest case is with pure sinusoidal/cosine control voltages as described in Chapter 2.3.1. The control signals are:

$$\begin{aligned} u_{sta}(t) &= M \cos(\omega t) \\ u_{stb}(t) &= M \cos\left(\omega t - \frac{2\pi}{3}\right) \\ u_{stc}(t) &= M \cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \quad (6.10)$$

Referred to Figure 6.2, the cosine modulation function are introduced because in order to coincide with the vector space in Figure 6.2. When $\omega t = 0$, the voltage is at it's maximum in the α -axis. In [56] and [57], the results from the calculations are:

M = [2/3 to 2/√3], (uttermost sector):

$$\Delta I_{N,rms}^2 = \frac{\Delta i_n^2}{54\pi} \left(\begin{array}{l} -48\sqrt{3}M^3 - 24\sqrt{3}M^3 \cos(\varphi_2)^3 + 24\varphi_1 - 24\varphi_2 \\ +108M^2\varphi_1 + 36\sqrt{3}M^2 - 36M^3 - 81M^3 \sin(\varphi_1) - 108M \sin(\varphi_1) \\ +54M^2 \sin(\varphi_1) \cos(\varphi_1) - 54\sqrt{3}M^2 \cos(\varphi_1)^2 + 36\sqrt{3}M \cos(\varphi_1) \\ +9\sqrt{3}M^3 \cos(\varphi_1) + 24\sqrt{3}M^3 \cos(\varphi_1)^3 - 108M^2\varphi_2 - 108M \sin(\varphi_2) \\ +96M^2\pi + 27M^4\pi + 16\pi - 36\sqrt{3}M \cos(\varphi_2) - 9\sqrt{3}M^3 \cos(\varphi_2) \\ -54\sqrt{3}M^2 \cos(\varphi_2)^2 - 54M^2 \sin(\varphi_2) \cos(\varphi_2) - 81M^3 \sin(\varphi_2) \end{array} \right) \quad (6.11)$$

φ_1 and φ_2 are the angles when the reference vector are crossing from area 2→area 3 and area 3→area 4 in Figure 6.2 respectively.

M = [1/√3 to 2/3], (middle sector):

$$\Delta I_{N,rms}^2 = \frac{\Delta i_n^2}{18\pi} \left(\begin{array}{l} \frac{1}{18}(-16\sqrt{3}M^3 - 8\sqrt{3}M^3 \cos(\varphi_4)^3 - 8\varphi + 8\varphi_4 - 36M^2\varphi_3 \\ -6\sqrt{3}M^2 + 36M^2 \sin(\varphi_3) \cos(\varphi_3) - 24\sqrt{3}M \cos(\varphi_3) - 24\sqrt{3}M^3 \cos(\varphi_3) \\ +8\sqrt{3}M^3 \cos(\varphi_3)^3 + 36M^2\varphi_4 + 8M^2\pi + 9M^4\pi + 24\sqrt{3}M \cos(\varphi_4) \\ +24\sqrt{3}M^3 \cos(\varphi_4) - 36M^2 \sin(\varphi_4) \cos(\varphi_4) - 12M^3 \end{array} \right) \quad (6.12)$$

φ_3 and φ_4 are the angles when the reference vector are crossing from area 1→area 3 and area 3→area 1 in Figure 6.2 respectively.

M < 1/√3, (innermost sector):

$$\Delta I_{N,rms}^2 = \frac{\Delta i_n^2}{18\pi} \left(M^2(9M^2\pi - 12M - 6\sqrt{3} + 8\pi - 16\sqrt{3}M) \right) \quad (6.13)$$

where

$$\Delta i_n = \frac{U_{dc} T_{sw}}{8L} \quad (6.14)$$

In [44], the analytical expressions for the angles that give the crossings between the different areas in Figure 6.2 are computed:

$$\varphi_1(M) = \pi - \varphi_2(M) \quad (6.15)$$

$$\varphi_2(M) = \pi + \operatorname{atan} \left(\frac{\frac{1}{3} \sqrt{3} (1 + \sqrt{-3 + 9M^2})}{-1 + \frac{1}{3} \sqrt{-3 + 9M^2}} \right) \quad (6.16)$$

$$\varphi_3(M) = \pi - \varphi_4(M) \quad (6.17)$$

$$\varphi_4(M) = \frac{5\pi}{6} + \operatorname{atan} \left(\frac{\frac{2}{3} \left(2 + \frac{\sqrt{3}}{2} \left(-\frac{1}{3} \sqrt{3} - \sqrt{-1 + 3M^2} \right) \right)}{\left(-\frac{1}{3} \sqrt{3} - \sqrt{-1 + 3M^2} \right)} \right) \quad (6.18)$$

These expressions are made for solvers that returns a negative value of the atan() expression.

The size of the middle sector is small, ranging from $M=0.577$ to $M=0.666$. By extending the range for the uttermost sector, and the number of expressions for the ripple current, reduces to two. Hence Eq. (6.11) applies to the common range $M=[1/\sqrt{3} \ 2/\sqrt{3}]$, and computation of φ_3 and φ_4 is also avoided.

By eliminating the angle expressions for Eq.(6.11), a simplified expression of the ripple current can be derived. Letting $\varphi_1 = \pi/3$ and $\varphi_2 = 2\pi/3$ in Eq.(6.11), a simplified equation yields from $M = 1/\sqrt{3}$ to $M = 2/\sqrt{3}$:

$M=[1/\sqrt{3}$ to $2/\sqrt{3}]$:

$$\Delta I_{N,rms}^2 = \Delta i_n^2 \left(\frac{4}{27} \pi - \frac{2}{3} M^3 + \frac{10}{9} \pi M^2 - \frac{4}{3} \sqrt{3} M + \frac{1}{2} \pi M^4 - \frac{19}{9} \sqrt{3} M^3 + \frac{2}{3} \sqrt{3} M^2 \right) \quad (6.19)$$

Figure 6.3 shows a plot of the full solution in Eq.(6.11) and (6.13), in addition to the approximated solution in Eq.(6.19). A simulation in MATLAB is also shown, to verify the results.

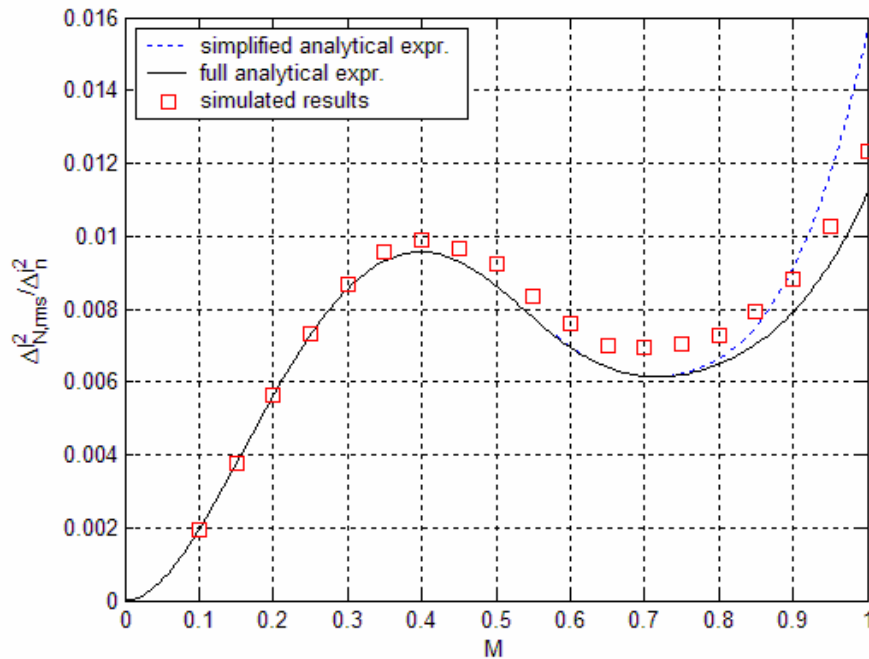


Figure 6.3: Comparison between analytical expressions and simulated values for sinusoidal modulation.

6.2.4 Analytical equations for sinusoidal CBPWM with 3rd harmonic injection

By injecting a common 3rd harmonic component of 1/6 of the fundamental in the control signals, the modulation range can be extended to $M = 2/\sqrt{3} \approx 1.15$ [55]. In [55], it is shown that this type of modulation also decrease the ripple current for a 2-level converter. In this chapter, it is shown that this also holds true for a 3-level converter. 3rd harmonic injection is introduce in the control signals the following way:

$$\begin{aligned}
 u_{sta}(t) &= M(\cos(\omega t) - M_3 \cos(3\omega t)) \\
 u_{stb}(t) &= M\left(\cos\left(\omega t - \frac{2\pi}{3}\right) - M_3 \cos(3\omega t)\right) \\
 u_{stc}(t) &= M\left(\cos\left(\omega t + \frac{2\pi}{3}\right) - M_3 \cos(3\omega t)\right)
 \end{aligned} \tag{6.20}$$

where $M_3=1/6$. Figure 6.4 shows a plot of the influence of the 3rd harmonic injection in the control signal. Since triple harmonics will disappear in the load phase-, and line-voltages in a 3-phase load, any 3rd harmonic injection can be performed in the control signals.

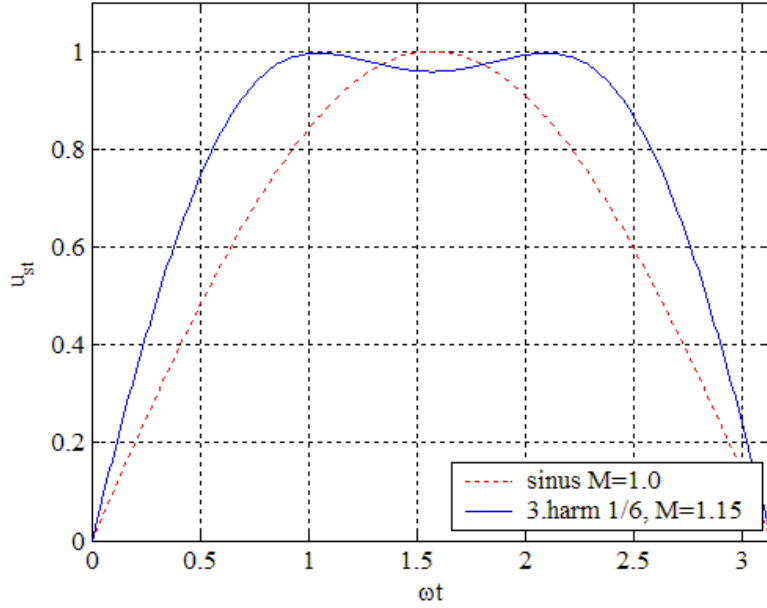


Figure 6.4: Comparison of pure sinus and sinus with 3.harm injection at $M=1.0$ and 1.15 respectively.

Using the same method described in the previous, the analytical expressions can be extracted. The solution is as follows:

$M=[1/\sqrt{3}, 2/\sqrt{3}]$, (middle and uttermost sector):

$$\Delta i_{N,rms}^2 = \frac{\Delta i_n^2}{\pi} \left(\begin{aligned} & \frac{8\pi}{27} - 2M^2\varphi_2 - \frac{109}{3888}\sin(3\varphi_2)M^5 - \frac{4}{3}\sin(\varphi_2)M - \frac{109}{3888}\cos(3\varphi_2 + \frac{\pi}{6})M^5 \\ & + \frac{109}{3888}\sin(3\varphi_2 + \frac{\pi}{3})M^5 - \frac{1}{27}\cos(3\varphi_2 + \frac{\pi}{6})M^3 - \frac{5}{27}\sin(3\varphi_2 + \frac{\pi}{3})M^3 \\ & + \frac{4}{9}\varphi_1 - \frac{4}{9}\varphi_2 - \frac{5\sqrt{3}}{12}M^2 - \frac{8\sqrt{3}}{9}M^3 + \cos(\varphi_1 + \frac{\pi}{6})M^3 + 2\varphi_1M^2 \\ & + \frac{1}{9}\sin(3\varphi_1 + \frac{\pi}{3})M^3 + \frac{1}{9}\cos(3\varphi_1 + \frac{\pi}{6})M^3 + \frac{4\pi}{9}M^4 + \frac{145\pi}{81}M^2 \\ & - \sin(\varphi_2)M^3 - \frac{2}{3}\sin(2\varphi_2 + \frac{\pi}{3})M^2 - \frac{1}{3}\sin(2\varphi_2)M^2 - \frac{1}{3}\sin(2\varphi_2 + \frac{\pi}{6})M^2 \\ & + \frac{2}{27}\sin(3\varphi_2 + \frac{\pi}{3})M^3 - \sin(\varphi_2 + \frac{\pi}{3})M^3 - \frac{4}{3}\sin(\varphi_2 + \frac{\pi}{3})M \\ & + \frac{4}{3}\cos(\varphi_1 + \frac{\pi}{6})M - \frac{1}{3}\sin(2\varphi_1 + \frac{\pi}{3})M^2 + \frac{1}{3}\sin(2\varphi_1)M^2 \\ & - \frac{2}{3}\cos(2\varphi_1 + \frac{\pi}{6})M^2 - \sin(\varphi_1)M^3 - \frac{4}{3}\sin(\varphi_1)M - \frac{127}{315}M^3 \end{aligned} \right) \quad (6.21)$$

where φ_1 and φ_2 are defined in (6.15) and (6.16).

$M=[0 \text{ to } 2/\sqrt{3}]$, (inner sector):

$$\Delta i_{N,rms}^2 = \frac{\Delta i_n^2}{\pi} \left(-\frac{5}{14} M^3 + \frac{7}{16} M^4 \pi - \frac{11}{24} \sqrt{3} M^2 + \frac{17}{36} M^2 \pi - \frac{8}{9} M^3 \sqrt{3} \right) \quad (6.22)$$

As for the pure sinusoidal modulation, the expression can be simplified by letting $\varphi_1 = \pi/3$ and $\varphi_2 = 2\pi/3$ in Eq.(6.21):

$M=[1/\sqrt{3}, 2/\sqrt{3}]$, (middle and uttermost sector):

$$\Delta i_{N,rms}^2 = \frac{\Delta i_n^2}{\pi} \left(\begin{array}{l} \frac{91\pi}{81} M^2 + \frac{4\pi}{9} M^4 + \frac{7}{12} \sqrt{3} M^2 + \\ \frac{4\pi}{27} - \frac{127}{315} M^3 - \frac{19}{9} \sqrt{3} M^3 - \frac{4}{3} \sqrt{3} M \end{array} \right) \quad (6.23)$$

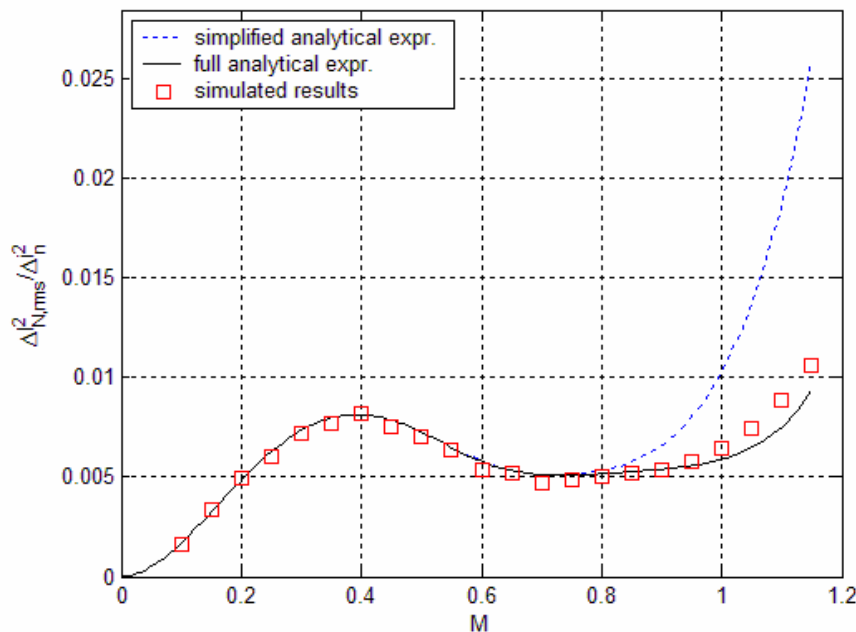


Figure 6.5: Comparison between analytical expressions and simulated values for sinusoidal with added 3.harmonic injection.

Figure 6.5 shows a plot of the full solution in Eq.(6.22) and (6.21), in addition to the simplified solution in Eq.(6.23). A simulation in MATLAB is also shown, to verify the results. From the plot, it can be observed that the simplified solution converges from the full solution/simulated values, and the accuracy is poor for $M > 0.8$. The full solution shows good accuracy according to simulations.

6.2.5 Verification by experiments

To verify the results, a test setup as shown in Figure 6.6 is used.

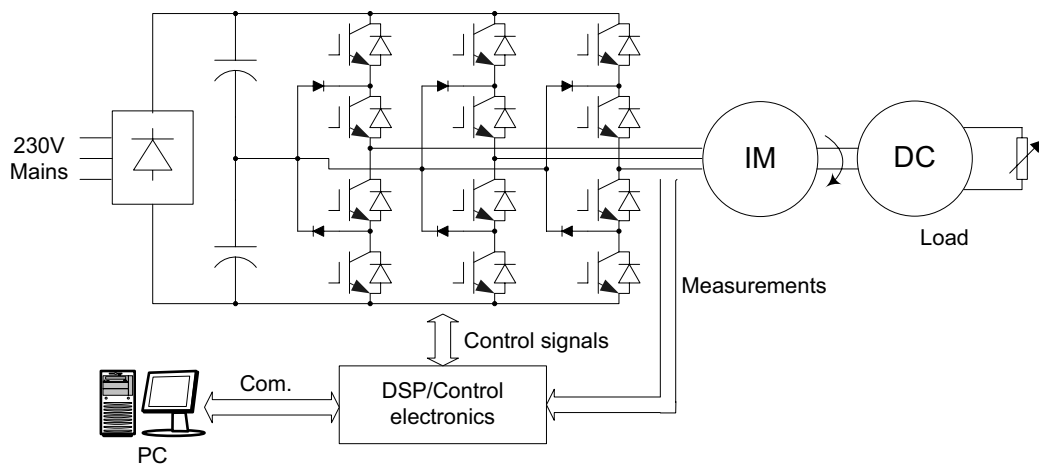


Figure 6.6: Laboratory setup.

The primary data for the setup is summarized in the table below. The 3-level converter used is described in Chapter 5.1.

Table 6-2: Data on laboratory setup.

Component	Data
3-level NPC Converter	40kW, fsw=1kHz, 315Udc
Induction machine	15kW, 230V, $L_{\sigma}=3.2\text{mH}$
Load	15kW DC-machine with variable load
DSP/Control board	TMS320F2812 based

In Figure 6.7, a plot of the output waveforms is shown at nearly full load and speed for pure sinusoidal modulation is shown. The output current for the different modulations method are measured at different modulation indexes. By using MATLAB, the waveforms are analysed, and the ripple current extracted. The results are shown in Figure 6.8 and Figure 6.9 respectively.

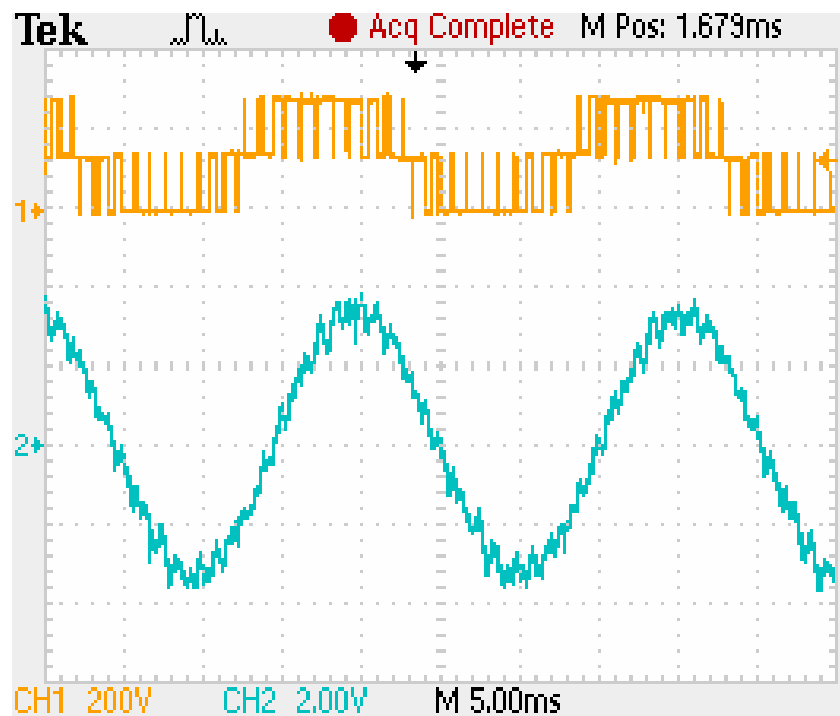


Figure 6.7: Output waveforms for sinusoidal modulation at $M=0.98$. Trace1: Pole voltage [200V/div]. Trace 2: Phase current [33.3A/div].

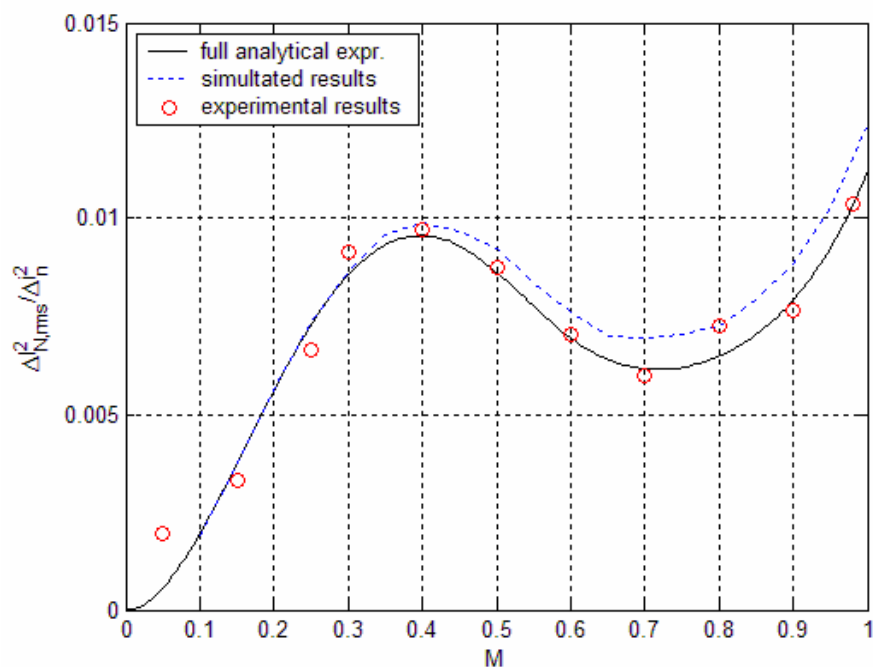


Figure 6.8: Results from pure sinusoidal modulation.

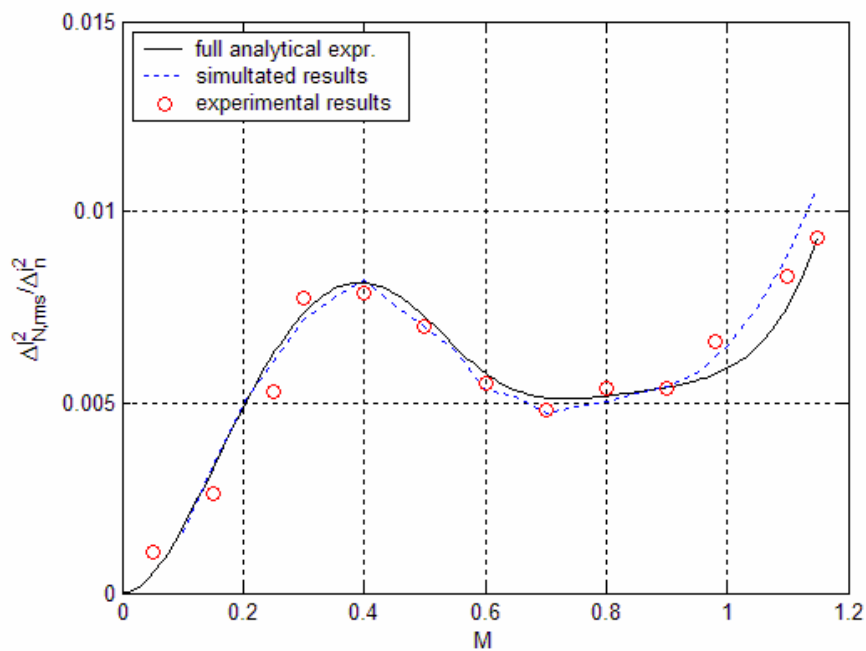


Figure 6.9: Results from sinusoidal modulation with added 3rd harmonic.

As seen from the experimental results, the analytical solutions match the simulations and the experimental results fairly well. By introducing a 3rd harmonic component in the control signals, an increase in the modulation range of 15% can be achieved. Also the harmonic current is lowered as plotted in Figure 6.10.

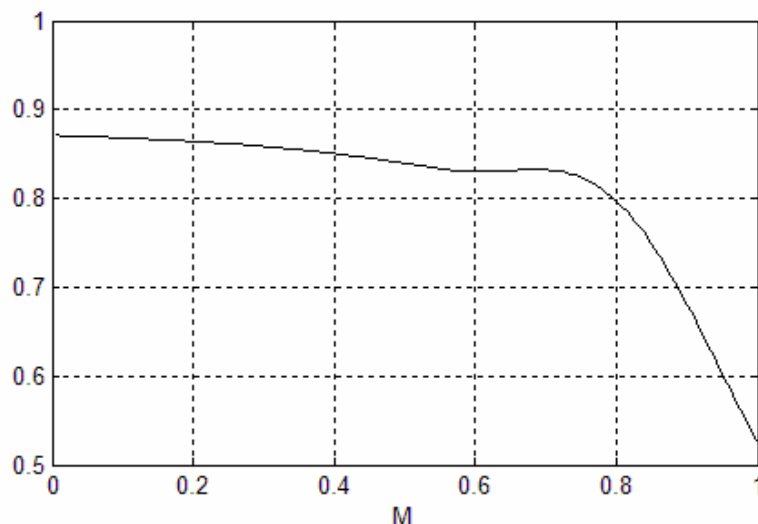


Figure 6.10: Relative loss factor between the 2 different modulation strategies.

6.3 Simulated harmonics for 3-level PWM

Chapter 6.2 has proved that it is possible to deduce analytical equations for simple 3-level PWM strategies such as pure sinusoidal Carrier Based PWM (CBPWM)

and sinusoidal CBPWM with 3rd harmonic injection. As shown in the previous section, the complexity of the analytical solution is quite high, and analytical solutions for more advanced modulation strategies are likely to be very complex. However, it is possible to simulate the resulting harmonic current to compare to the already developed analytical solutions.

For this purpose MATLAB is used. The basis for the simulation is the model in Figure 6.1. First, the different modulation methods are programmed in a module that produces the desired switching output voltages from the converter u_o . The motor phase voltage can be calculated by subtracting the common mode voltage from this. By Fourier analysis, the 1st harmonic value can be found, and subtracted from the motor phase voltage. The resulting voltage is the ripple voltage across the motor's leakage inductance. From integration, the ripple current $\Delta i_{N,rms}$ in the motor can be found. In Chapter 6.2, a reference harmonic current is used:

$$\Delta i_n = \frac{U_{dc} T_{sw}}{8L} \quad (6.24)$$

where U_{dc} is the DC-bus voltage and T_{sw} is the switching period. By dividing the total RMS current by the expression in Eq.(6.24), a dimensionless performance factor can be extracted:

$$\frac{\Delta i_{N,rms}^2}{\Delta i_n^2} \quad (6.25)$$

Eq.(6.25) gives a figure of merit, independent of switching frequency, DC-bus voltage and filtering inductances. The squared expressions are introduced because the harmonic losses are proportional to the square of the current. In the simulation study, five different switching strategies have been used. First the sinusoidal CBPWM (denoted *sinus* in the plots) and sinusoidal CBPWM with 3rd harmonic injection (*sinus w/3h*) are simulated for verification. The proposed method (*Lipo*) that centres the vectors for a 3-level converter (Eq.(2.50)), and the corresponding space vector control signal for 2-level modulation in Eq.(2.46), denoted *CV* is are simulated. Finally, the space vector method presented in Chapter 2.3.2 is simulated, denoted *SV*.

Figure 6.11 shows typical motor current waveforms by using different modulation methods. All other parameters are the same. To the left is plotted output currents at low modulation index ($M=0.4$), and high modulation index to the right ($M=1.0$). As can be seen from the figures, it can be observed that the Space Vector method gives particular good spectral performance, especially at lower modulation indexes. The reason for this is that all switches in each phase leg are switching in both half periods of the fundamental output waveform (see Figure 2.18). Other 3-level modulation methods are only switching two switches in each leg. This will lead to higher switching losses for the Space Vector modulation method presented here.

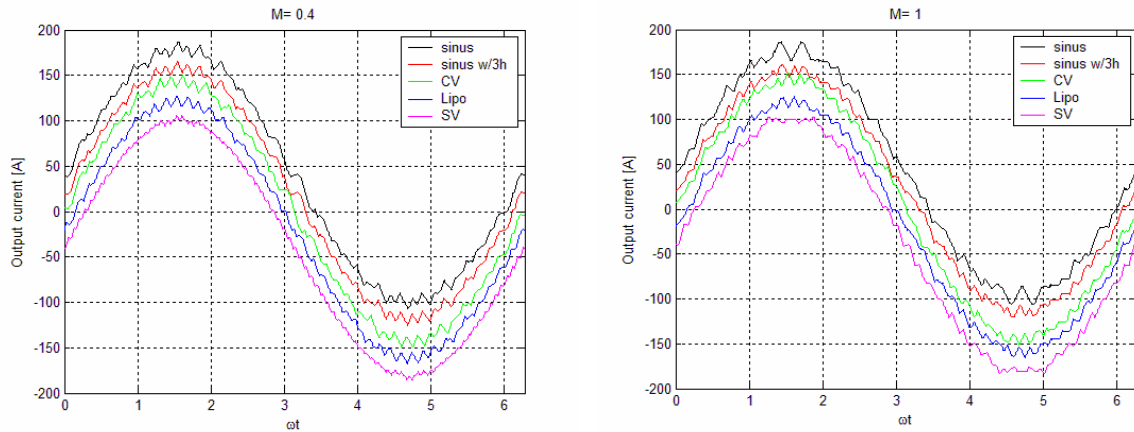


Figure 6.11: Simulated motor currents for different modulation strategies at $M=0.4$ (left) and $M=1$ (right). Offsets are introduced for better viewing.

The results from the simulations are shown in Figure 6.12. As before mentioned, the Space Vector modulation method utilises all the switches for $M < 0.57$, and hence lower harmonic current in this region occur.

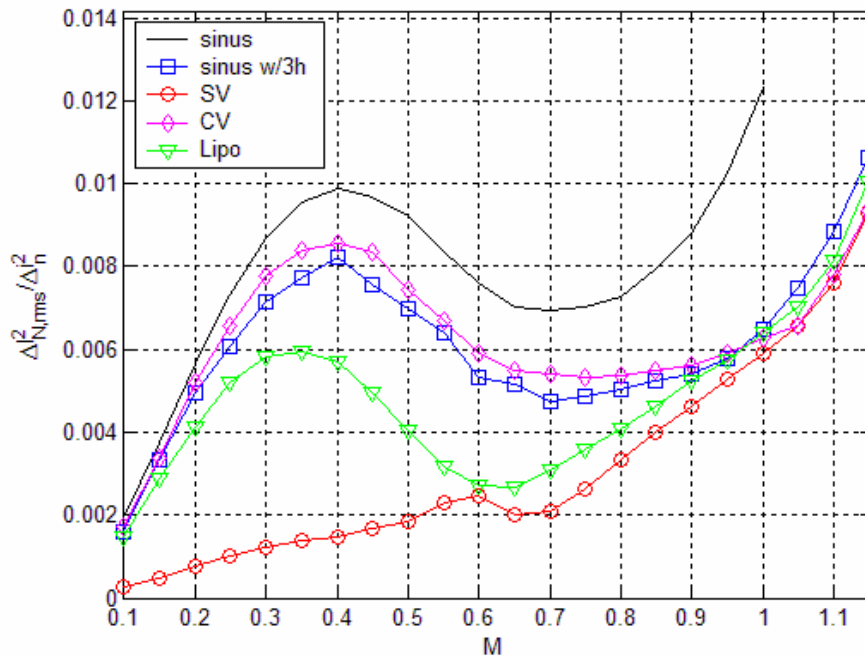


Figure 6.12: Harmonic current for different 3-level modulation schemes.

Even in the high modulation region ($M > 0.57$), the Space Vector modulation shows better performance together with the modulation method from [39] (*Lipo*). Also, the control signals associated for 2-level space vector modulation (*CV*), shows non-optimal performance applied in the 3-level topology, and it equals sinusoidal modulation with 3rd harmonic injection. Finally, the two sinusoidal modulation

methods show inferior performance to the other, but have an advantage in easy implementation.

6.4 Harmonics for 4-level and 5-level PWM

As mentioned in Chapter 6.3, the analytical expressions for more advanced modulation method for the 3-level topology become complicated. For 4- and 5-level topologies, even more complex expressions are likely to be expected. From this, the only way to compare multilevel converters is by simulations. In the following, extensive simulations have been performed for sinusoidal Carrier Based PWM (CBPWM) for different converter topologies. Figure 6.13 shows the results from the simulations.

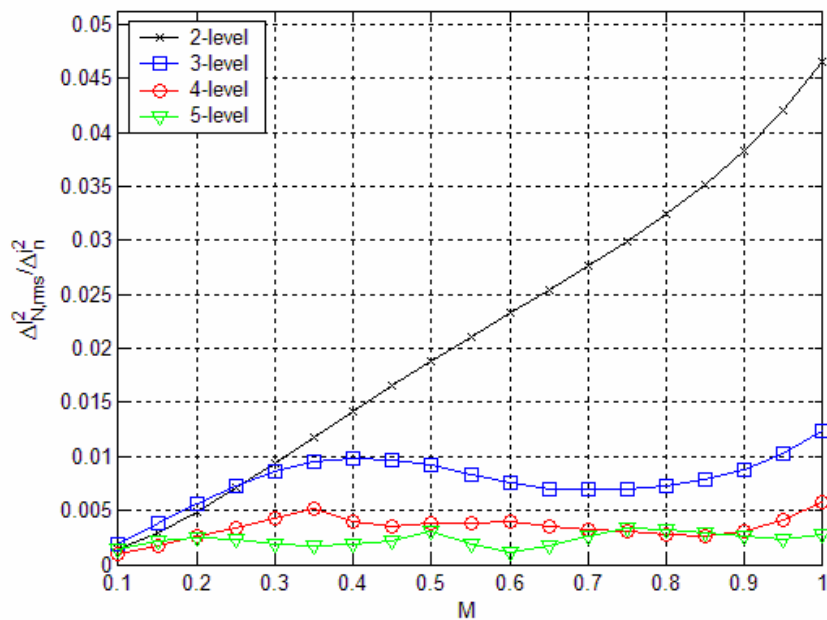


Figure 6.13: Harmonic currents for sinusoidal CBPWM for different topologies.

As expected, the harmonic current is decreasing as the number of levels n is increased. However, the gain in harmonic performance is decreased as n is increasing. Figure 6.14 shows the same results as Figure 6.13, only normalized to the 2-level topology. From the figure, the spectral quality of a 3-level converter is increased at higher modulation depths compared to a 2-level converter. The 4- and 5-level converter show lower harmonic losses, but taken the complexity of these converters into consideration, the 3-level topology yields the most reduction in harmonic losses.

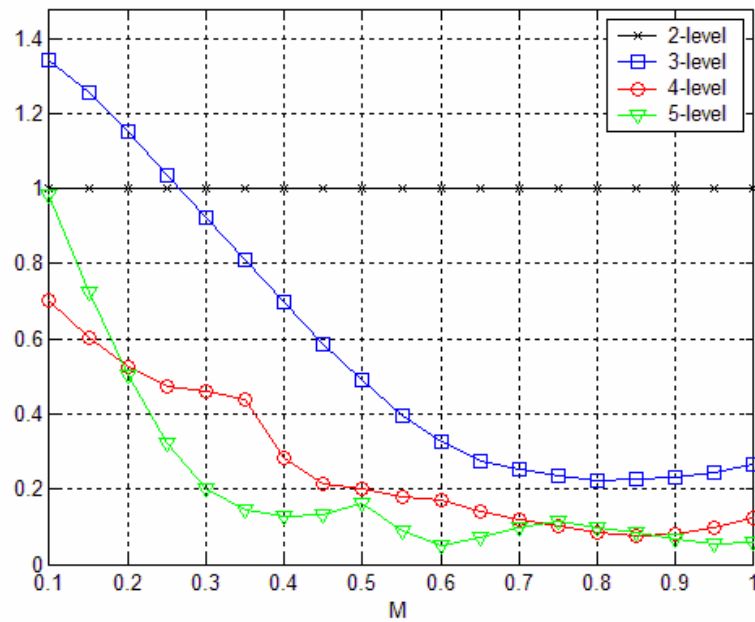


Figure 6.14: Normalized harmonic currents.

6.5 Conclusion

Analytical expressions for the ripple current on the AC-side of a 3-level converter are developed for 2 different modulation strategies. Experimental measurements on a three-level prototype in the lab and simulations are done to verify the analytical expressions. Extensive simulations on different 3-level modulations strategies has been done, and also 4- and 5-level sinusoidal CBPWM. The results shows that by extending the converter topology to a multilevel converter, harmonic currents can be reduced significantly. Complexity of the converter and control taken into account, the 3-level topology seems to be an interesting topology.

7 DC-BUS BALANCING

One inherent problem with the diode clamped multilevel converters is the balancing of the capacitor voltages in the DC-link. This is particularly a problem in systems where the DC-bus is fed from a single supply connected to only the upper and lower stack of the DC-link capacitors. The fundamental reason for the unbalance, is that unequal current is drawn from the different throws in the DC-link.

7.1 Switching Functions

To address some of the problems with balancing, it is necessary to model the currents in the DC-link. In [59] the currents are modelled by use of switching functions. The theory is repeated here, and gives a very nice visualization of the balancing problems.

Figure 7.1 shows a general multilevel converter. The multi pole switch S_j ($j = a, b, c$) can have i distinct positions, $i = (n-1)/2, \dots, 0, \dots, -(n-1)/2$, called t_{ij} . The number of inverter poles (one for each line output) is 3. In order to maintain continuity of the three phase currents, at least one of the throws has to be connected to a pole at a given instance of time (the throws are the interconnections from the DC-buses to the multi pole switches). In addition, each switch S_j may be connected to only one voltage terminal at any given instance of time. Mathematically, these constraints can be expressed using switching function formulations. Let h_{ji} be the switching function connecting input voltage u_i to the output current i_j be defined as:

$$h_{ji}(t) = \begin{cases} 1, & \text{if } t_{ij} \text{ is closed} \\ 0, & \text{else} \end{cases}, \text{ then } \sum_{i=-\frac{n-1}{2}}^{\frac{n-1}{2}} h_{ji}(t) = 1 \quad (7.1)$$

The output voltages and input currents can be described by:

$$U_j(t) = \sum_{i=-\frac{n-1}{2}}^{\frac{n-1}{2}} h_{ji}(t) \cdot U_i(t) \quad \text{and} \quad I_i(t) = \sum_{j=a,b,c} h_{ji}(t) \cdot I_j(t) \quad (7.2)$$

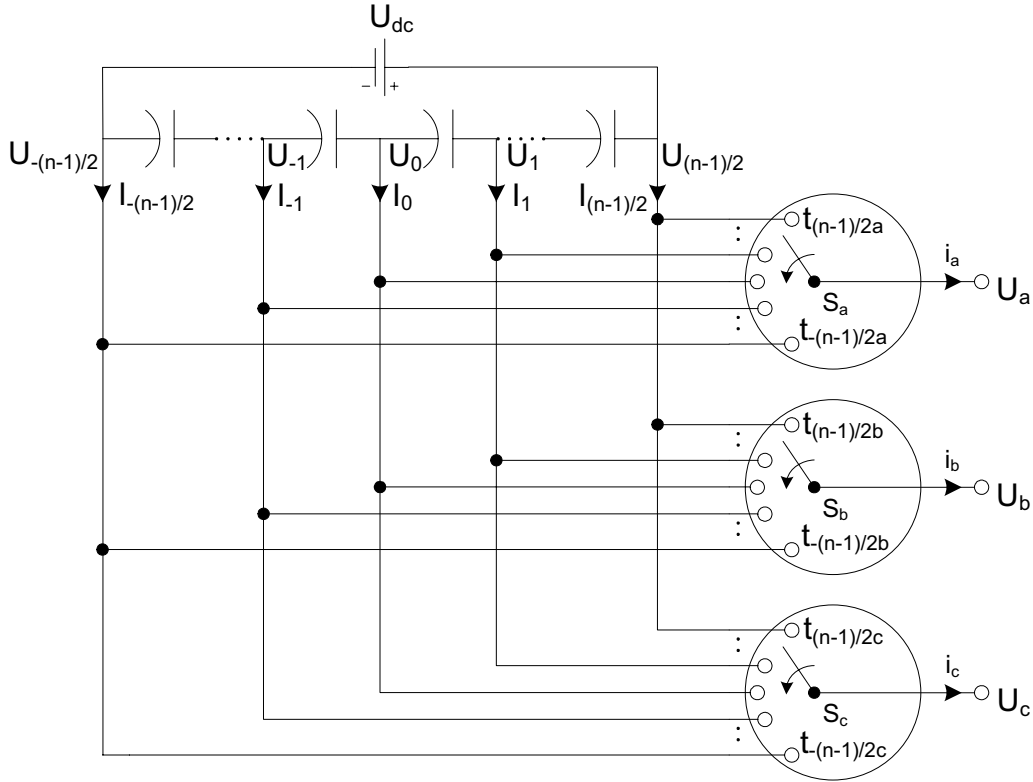


Figure 7.1: General multilevel converter.

Eq.(7.2) can be rewritten in a more compact form as:

$$\underline{U}_{out}(t) = H(t)\underline{U}_{in}(t) \quad \text{and} \quad \underline{I}_{in}(t) = H(t)^T \underline{I}_{out}(t) \quad (7.3)$$

Where:

$$\begin{aligned} \underline{U}_{out}(t) &= [U_a(t) \quad U_b(t) \quad U_c(t)]^T \\ \underline{I}_{out}(t) &= [I_a(t) \quad I_b(t) \quad I_c(t)]^T \\ \underline{U}_{in}(t) &= \left[U_{\frac{n-1}{2}}(t) \quad \dots \quad U_0(t) \quad \dots \quad U_{-\frac{n-1}{2}}(t) \right]^T \\ \underline{I}_{in}(t) &= \left[I_{\frac{n-1}{2}}(t) \quad \dots \quad I_0(t) \quad \dots \quad I_{-\frac{n-1}{2}}(t) \right]^T \end{aligned} \quad (7.4)$$

$$\underline{H}(t) = \begin{bmatrix} h_{a-\frac{n-1}{2}} & \dots & h_{a-\frac{n-1}{2}} \\ h_{b-\frac{n-1}{2}} & \dots & h_{b-\frac{n-1}{2}} \\ h_{c-\frac{n-1}{2}} & \dots & h_{c-\frac{n-1}{2}} \end{bmatrix} \quad (7.5)$$

When the repetition frequency of the switching function is much higher than the frequency of the output voltage, Eq.(7.3) can be approximated by:

$$\begin{aligned} \underline{U}_{out}(t) &= \underline{M}(t)\underline{U}_{in}(t) \\ \underline{I}_{in}(t) &= \underline{M}(t)^T \underline{I}_{out}(t) \end{aligned} \quad (7.6)$$

$$m_{ji}(\tau) = \frac{1}{T} \int_{\tau}^{t+T} h_{ji}(t) dt \quad (7.7)$$

Thus, m_{ji} is the average switching function, without taking switching into concern. As will be shown, this gives better visual understanding of the problem, and analysis becomes simpler.

7.2 Evaluation of the method

To evaluate the expressions for the DC-link currents, a comparison between a KREAN simulation and switching function simulation in MATLAB for a 3-level converter. The simulations have been done with pure sinusoidal load current. An example is shown in Figure 7.2.

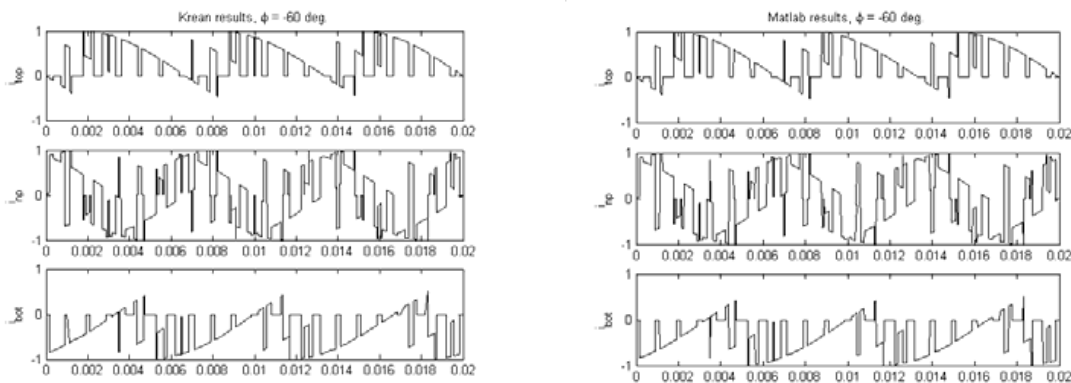


Figure 7.2: Simulations done with modulation index $M=0.8$ and current angle $\varphi=-60^\circ$, KREAN (left), MATLAB (right).

By using (7.7) the analysis is simplified, but the method gives good accuracy for the frequencies lower than the switching frequency.

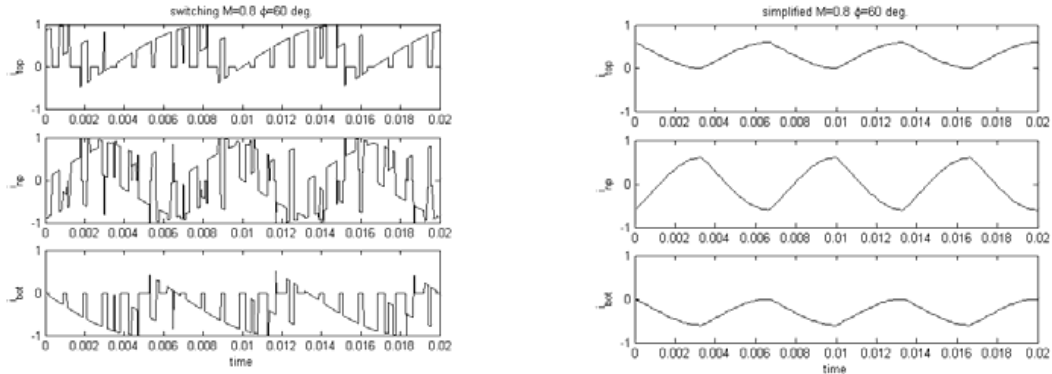


Figure 7.3: Simulations done with modulation index $M=0.8$ and current angle $\varphi=60$ (inductive load), switching (left), simplified (right).

Figure 7.4 shows the harmonics for the DC-bus currents for the switching and simplified method, respectively. The method of averaging is very accurate for lower harmonics, which causes the neutral point to fluctuate. Hence the simplifying method is very useful to illustrate DC-bus balancing problems.

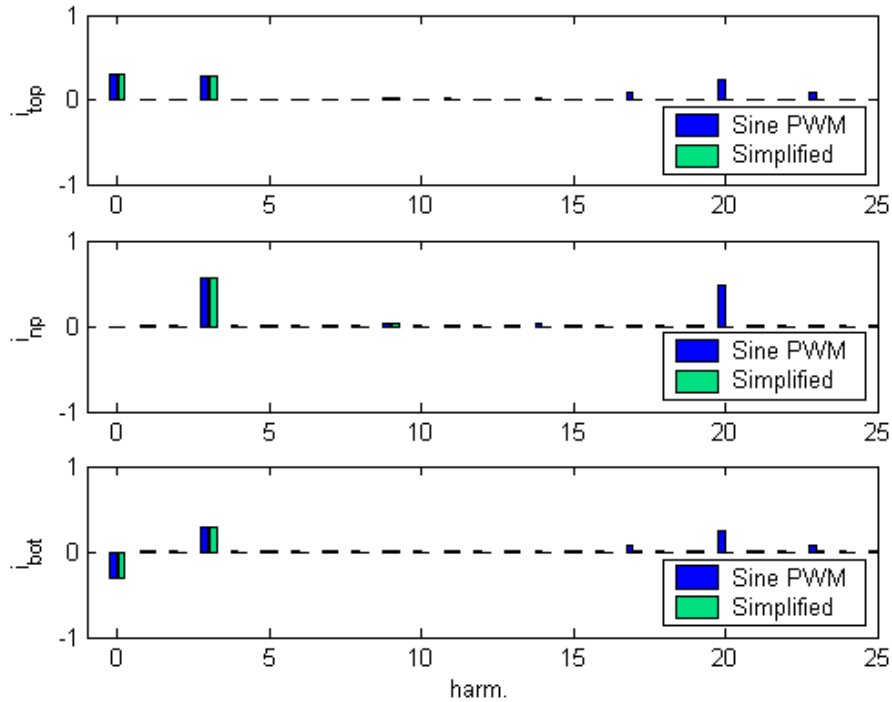


Figure 7.4: Shows a close-up view of the first 25 harmonics in Figure 7.3.

The load currents are pure sinusoidal, and can be represented by:

$$\begin{aligned} \underline{I}_o(t) &= [I_a(t) \quad I_b(t) \quad I_c(t)]^T \\ &= \hat{I} [\sin(\omega t - \varphi) \quad \sin(\omega t - \frac{2\pi}{3} - \varphi) \quad \sin(\omega t + \frac{2\pi}{3} - \varphi)]^T \end{aligned} \quad (7.8)$$

7.3 DC-bus balancing in 3-level converters

7.3.1 Switching vectors and current flow

For a 2-level inverter, the phase outputs can either be connected to the P- or the N-terminal of the dc-bus. Thus there are $2^3 = 8$ states for the voltage vector. Each phase of the 3-level converter can be connected to either the positive (P), the negative (N), or the neutral point (0) of the DC-bus, hence there are $3^3 = 27$ voltage states for the space vector. Figure 7.5 shows the 27 possible switching state vectors. References [60] and [61] give an overview of the problem with voltage balancing.

Not all vectors are affecting the neutral point (NP) balance, only the vectors generated by connecting *one or two* of the outputs to the NP point do. The vectors that do not affect the NP balance are called large vectors (*PNN, PPN, NPN, NPP, NNP, PNP*), and zero vectors (*PPP, NNN, 000*). In Table 7-1, all the switching state vectors that affect the neutral point balance are listed. The small vectors that cause the neutral point current to flow in the same direction as the phase currents are called positive small vectors. When the neutral point current is flowing in the opposite direction, the vectors are called negative small vectors. As can be seen from Figure 7.5, the small vectors have redundancy, i.e. the same space vector can be generated by two different switching combinations. The vectors *PON, OPN, NPO, NOP, ONP, PNO* are called medium vectors and do also affect the NP balance. They have no redundancy.

In Figure 7.6 examples of different vectors are drawn, and it shows how they affect the NP current flow. From the figure, it should be noted that the small vectors connect the load to only one capacitor, and the large vectors connect the load exclusively to the positive and negative bus-bars.

Table 7-1: Neutral point current for different space vectors.

Positive small vectors	i_{np}	Negative small vectors	i_{np}	Medium vectors	i_{np}
ONN	i_a	POO	$-i_a$	PON	i_b
PPO	i_c	OON	$-i_c$	OPN	i_a
NON	i_b	OPO	$-i_b$	NPO	i_c
OPP	i_a	NOO	$-i_a$	NOP	i_b
NNO	i_c	OOP	$-i_c$	ONP	i_a
POP	i_b	ONO	$-i_b$	PNO	i_c

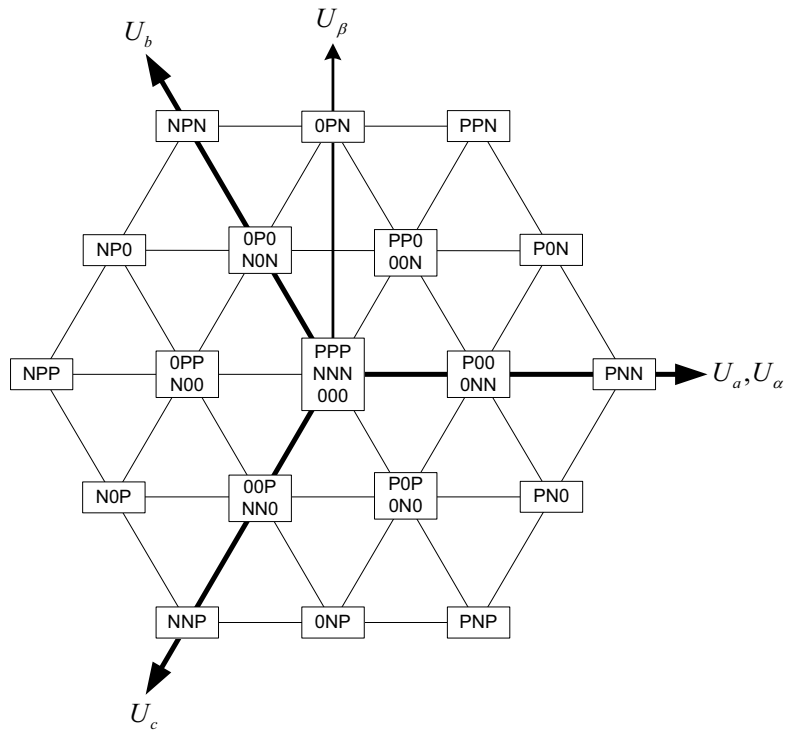
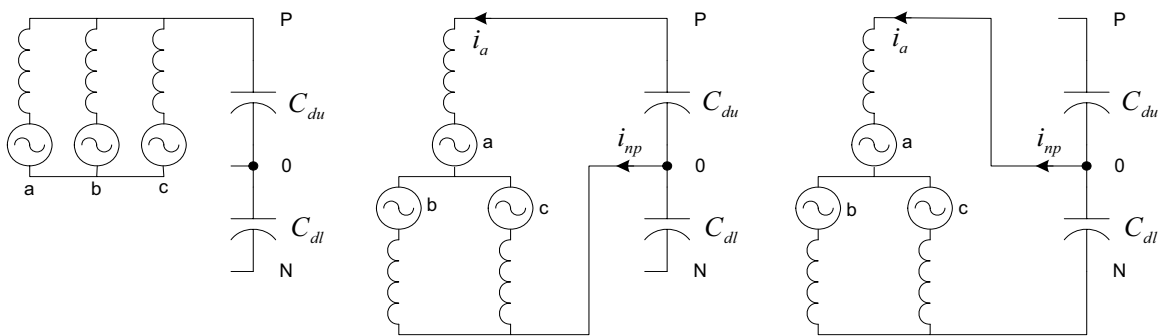
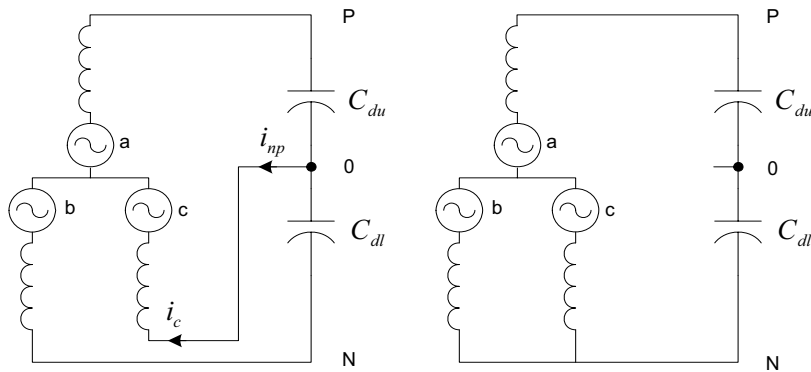


Figure 7.5: Vector output space for 3-level converter.



a) Zero vector (PPP) b) Negative small vector (P00) c) Positive small vector (0NN)



d) Medium vector (PNO) e) Large vector (PNN)

Figure 7.6: Examples of possible switching state vectors.

The relationship between the capacitor currents and the NP current can be expressed as follows:

$$i_{c1} - i_{c2} = i_{np} \quad (7.9)$$

The capacitor voltages can be expressed as:

$$u_{c1} + u_{c2} = U_{dc} \quad (7.10)$$

If the total dc bus voltage is assumed constant:

$$\frac{dU_{dc}}{dt} = \frac{du_{c1}}{dt} + \frac{du_{c2}}{dt} = 0 \quad (7.11)$$

and hence:

$$\frac{i_{c1}}{C_{c1}} + \frac{i_{c2}}{C_{c1}} = 0 \quad (7.12)$$

if $C_1 = C_2 = C$ then

$$i_{c1} = -i_{c2} \quad (7.13)$$

By using Eq.(7.9), the NP current becomes

$$i_{np} = -2i_{c2} = 2i_{c1} \quad (7.14)$$

From this, it is shown that a non-zero mean neutral point current will cause a non-zero capacitor current, and this will cause the capacitor voltages to discharge/charge.

If the floating capacitor voltages become unbalanced, the redundant small vectors in Table 7-1 has to be used to recover balance. Unbalance causes over-voltages across both switching devices and capacitors, and failure can occur. If either the upper or lower capacitor is fully discharged, the output voltage falls back to a conventional 2-level waveform.

The space vector algorithm presented in Chapter 2.3.2 uses the duty cycles of the small vectors to balance out the DC-bus voltages, Figure 7.7 shows the vector placement in sector A. The inner area $A1$ and $A3$ utilize two different small vectors, which are split as follows:

$$d_{s1} = d_{s1p} + d_{s1n} \quad , \quad d_{s2} = d_{s2p} + d_{s2n} \quad (7.15)$$

d_{s1p} and d_{s2p} are the duty cycles for the positive small vectors, and d_{s1n}/d_{s2n} are the duty cycles for the negative small vectors in Table 7-1 respectively. Area $A2$ and $A4$ utilize only one small vector, d_{s1} and d_{s2} respectively. By varying the duration of the positive and negative vectors, the neutral current is controlled, and hence the neutral point voltage. Two control parameters: f_1 and f_2 are introduced, such that:

$$\begin{aligned}
 d_{s1p} &= f_1 \cdot d_1 \\
 d_{s1n} &= (1 - f_1) \cdot d_1 \\
 d_{s2p} &= f_2 \cdot d_2 \\
 d_{s2n} &= (1 - f_2) \cdot d_2
 \end{aligned}
 \tag{7.16}$$

By varying f_1 and f_2 , the neutral point current/voltage is controlled, without affecting the total duty cycles of the vectors without introducing any additional switching. f_1 and f_2 have the same effect on the neutral point current, and in the following, f_1 will be used to balance out the neutral point voltage.

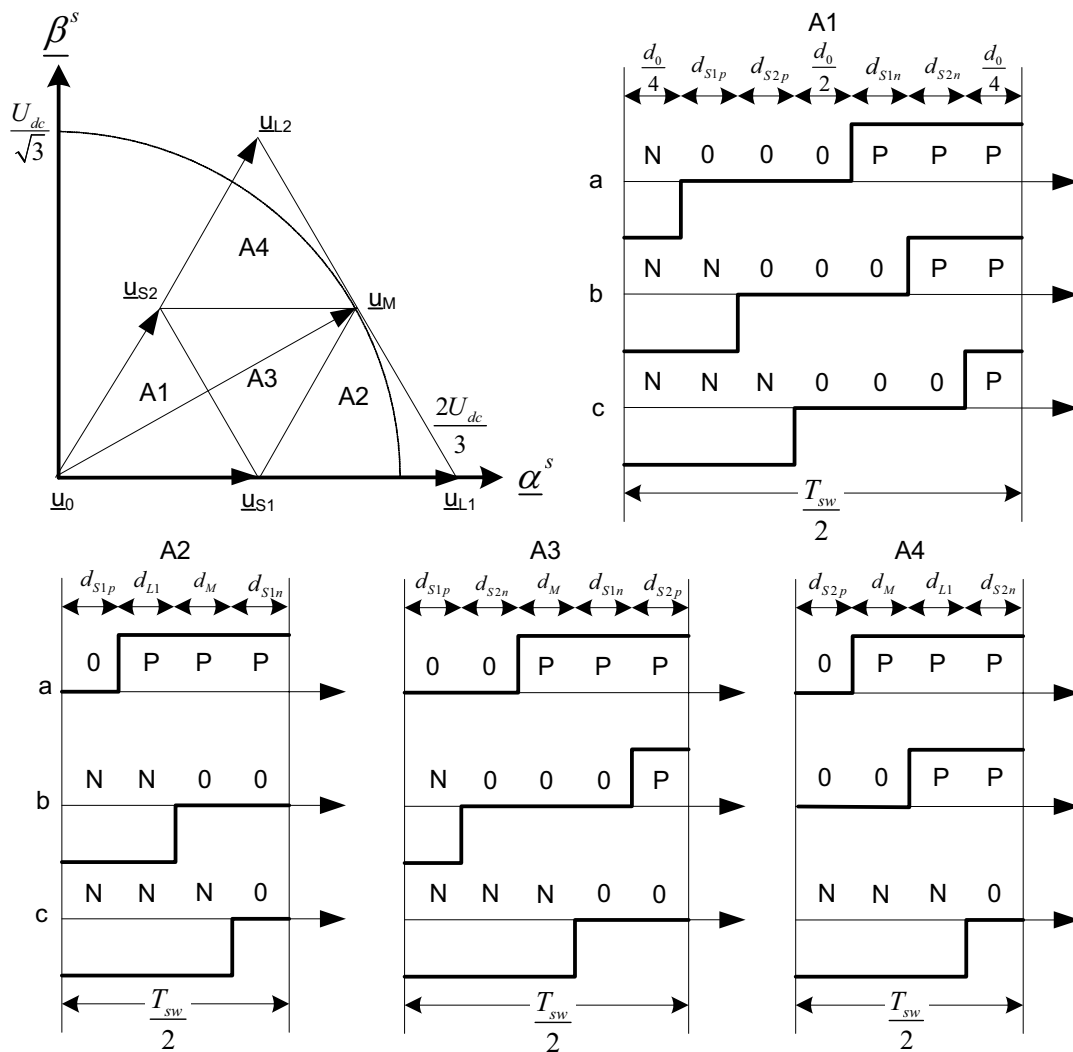


Figure 7.7: Vector placement for SVPWM in sector A.

Figure 7.8 to Figure 7.10 show results from simulations carried out for different modulation indexes and load angles. From the figures, it can be seen that the neutral point current, and hence the neutral point voltage can be controlled in the whole operating area.

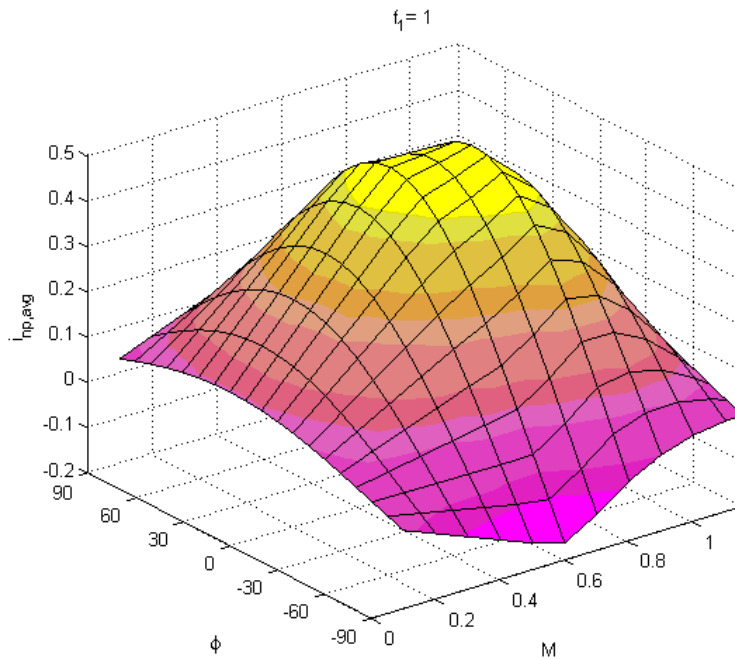


Figure 7.8: Plot of the average neutral point current in a 3-level converter for different load angles and modulation indexes at $f_1=1.0$.

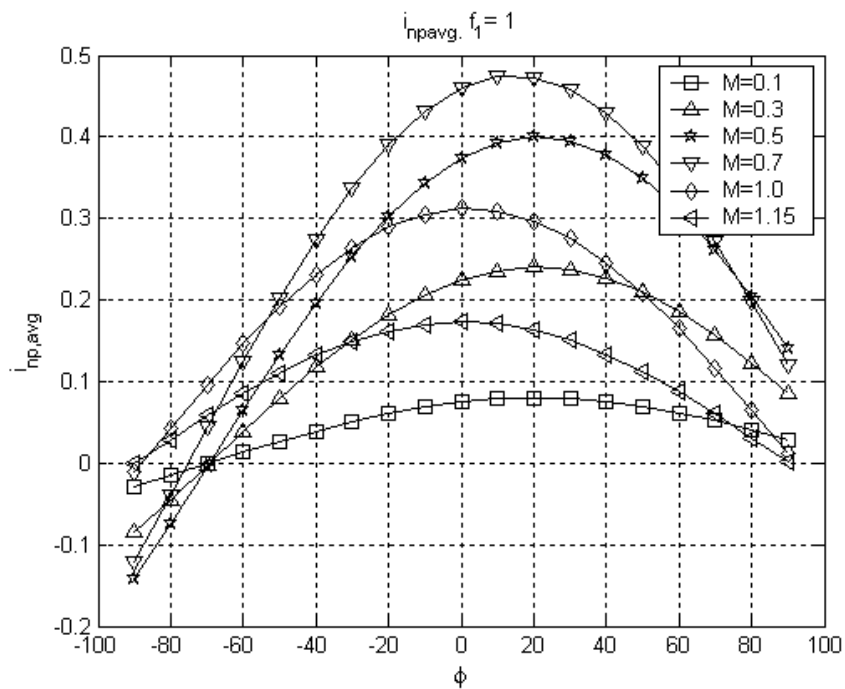


Figure 7.9: Same as Figure 7.8, in 2D, i.e $f_1=1.0$.

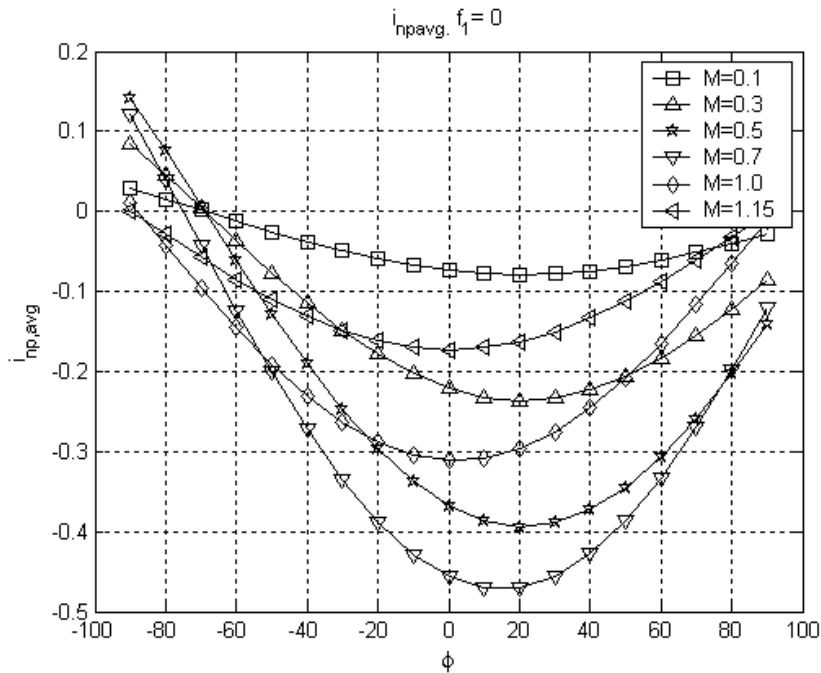


Figure 7.10: Plot of the average neutral point current for different load angles and modulation indexes at $f_1=0.0$.

The average switching functions are a powerful tool to visualize the DC-bus currents. Figure 7.11 shows a simulation of the neutral point current. For high modulation indexes, $M_s > 0.5$, the NP-current contains a large amount of 3rd harmonic component, for $M_s < 0.5$ the current contains only higher harmonics as switching frequency and above. This is shown in detail in Figure 7.12, where the lowest harmonic component present is at the switching frequency (20th harmonic) for $M_s < 0.5$.

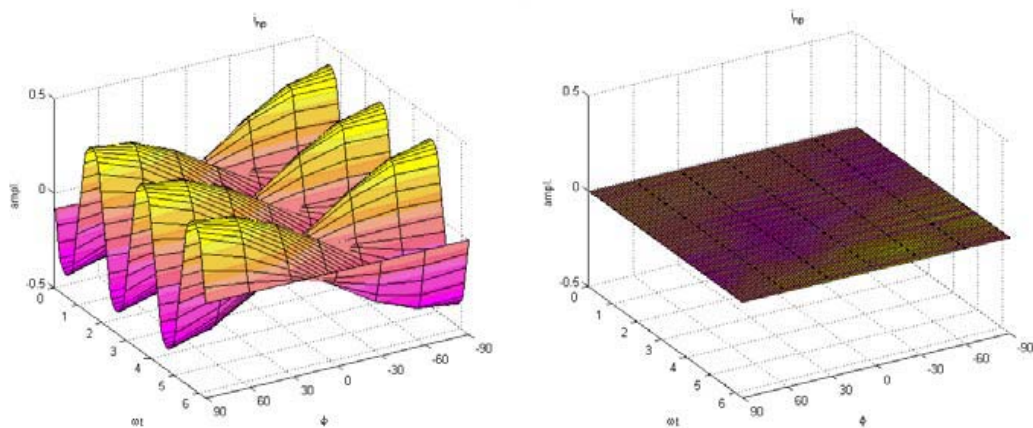


Figure 7.11: Average time domain simulation at $M_s=0.8$ (left) and $M_s=0.4$ (right), and $f_1=0.5$.

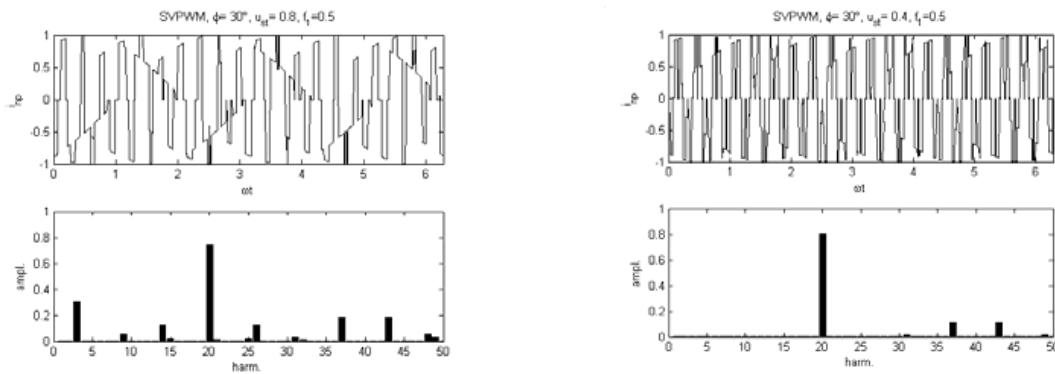


Figure 7.12: Harmonic analysis of the NP-current for $M_s=0.8$ (left), $M_s=0.4$ (right).

From Eq.(7.14) the same harmonics in the NP-current appear in the capacitor currents. For $M_s < 0.5$ there is no 3rd harmonic current flowing in the DC-capacitors. This is an advantage, because lower harmonics are often the dimensioning design criteria for the capacitors power losses caused by the capacitors relatively high ESR value at these frequencies (see Chapter 5.1.2 and [44]).

7.3.2 Experimental verification

To verify the simulations, the same setup as shown in Figure 6.6 and Table 6-2 is used, except that the load is exchanged with a star-connected RL-load, at $R=12\Omega$ and $L=3.3\text{mH}$. The results are shown in Figure 7.13 to Figure 7.16 at two different modulation indexes, $M_s=0.45$ and $M_s=0.8$. By using the control variable f_i , the DC-bus voltage can be controlled efficiently. From Figure 7.16, small fluctuations can be seen in the DC-bus voltages after about 1.7 sec. caused by the 3. harmonic current flowing in the capacitor at high modulation indexes as simulated in Figure 7.11.

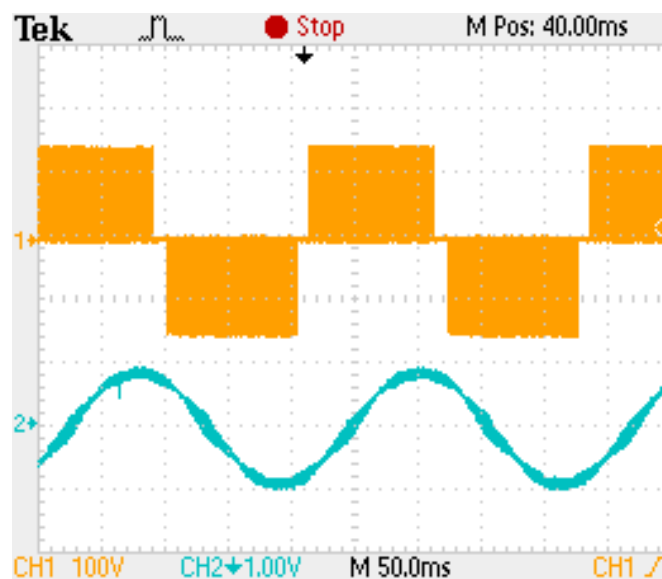


Figure 7.13: Output waveforms for space vector modulation modulation at $M_s=0.45$. Trace1: Pole voltage [100V/div]. Trace 2: Phase current [15A/div].

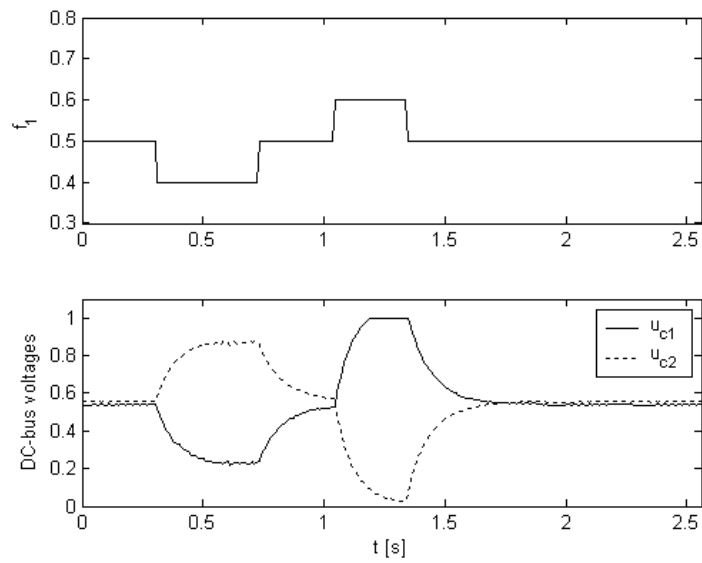


Figure 7.14: Control voltage f_1 and DC-bus voltages at $M_s=0.45$.

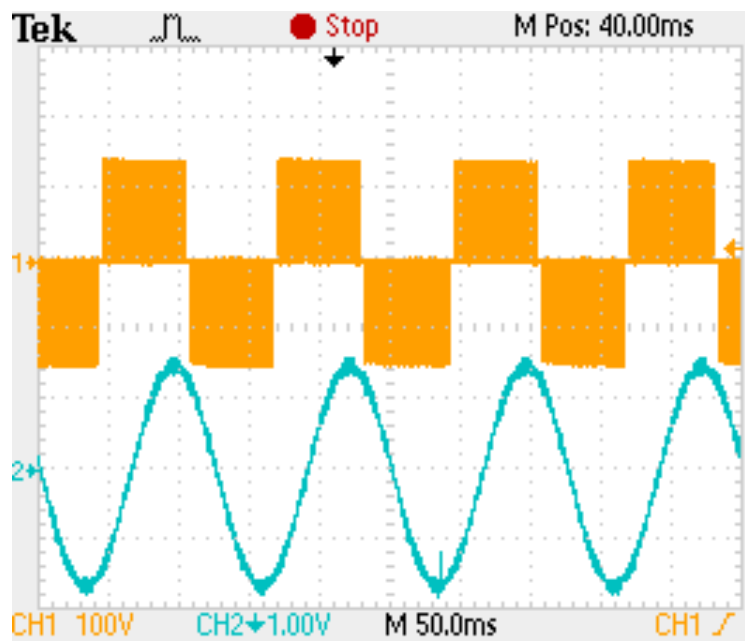


Figure 7.15: Output waveforms for space vector modulation modulation at $M_s=0.8$. Trace 1: Pole voltage [100V/div]. Trace 2: Phase current [15A/div].

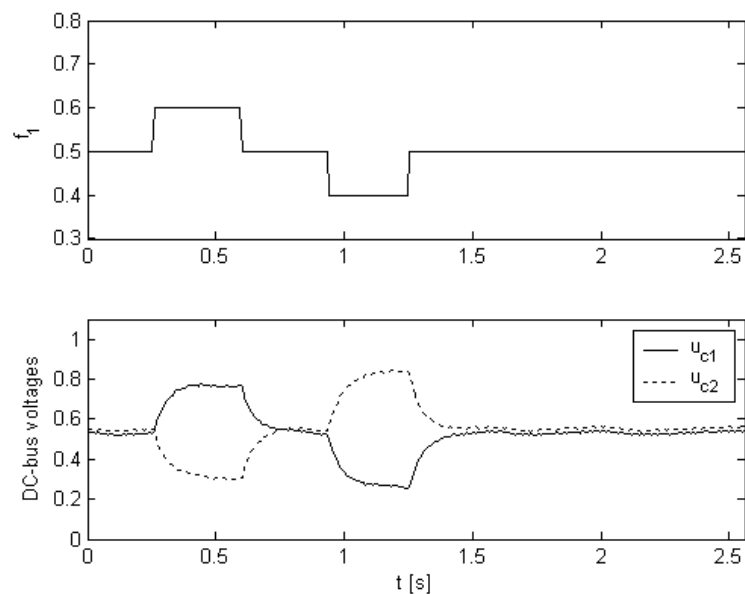


Figure 7.16: Control voltage f_1 and DC-bus voltages at $M_s=0.8$.

7.4 DC-bus balancing in 5-level converters

7.4.1 Simulation of DC-bus balancing

In the literature, and from the discussions in the previous chapter, DC-bus voltage fluctuations can be controlled for a 3-level converter with a single supply. For the 5-level converter, this is necessarily not true. One of the first papers that addressed the need for separate supply for each voltage levels in a 5-level converters is [62]. In [63], a 4th leg is used to actively stabilize the different levels. Later, [64] and [65] showed, by using a 5-level active rectifier connected in a back-to-back configuration, that it was possible to control the different voltage levels independently.

By using the average switching functions, the DC-bus currents can be visualised, as shown in Figure 7.17 and Figure 7.18. Only i_2 and i_1 are plotted, since i_{-2} and i_{-1} are the same, only with the opposite sign and phase. In Figure 7.19 (left) a close up view of the currents are shown. From the figures it should be noted that the current drawn from the intermediate DC-links are larger than for the uttermost. By using sinusoidal CBPWM, this implies that the uttermost DC-bus capacitors tend to charge, and the intermediate tends to discharge. This is illustrated by a KREAN simulation in Figure 7.19 (right). In the lower plot, it is clear that by using this type of modulation, that the voltages becomes unbalanced, and the intermediate capacitor voltages decrease to zero.

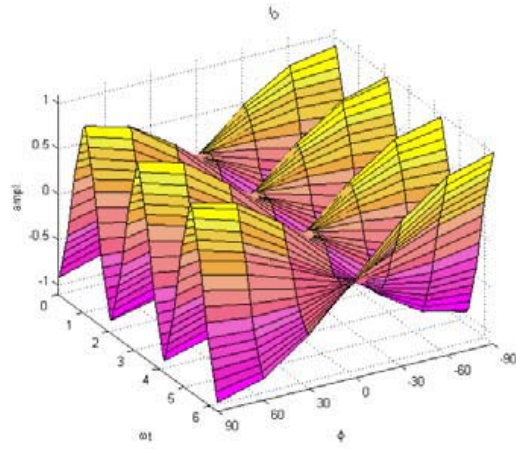
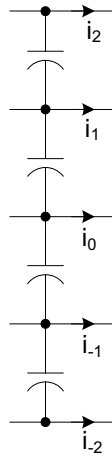


Figure 7.17: DC-bus currents in 5-level converter (left).3D plot of the middle DC-link current i_0 at $M=0.8$. (right).

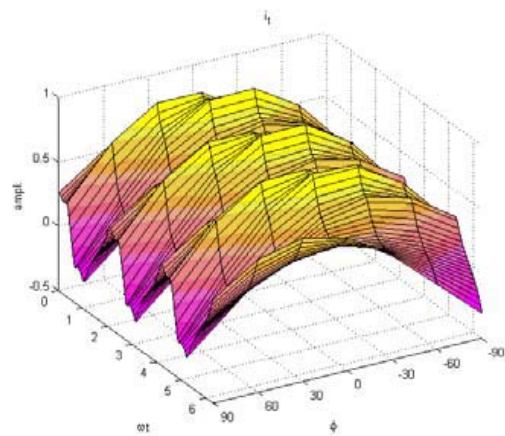
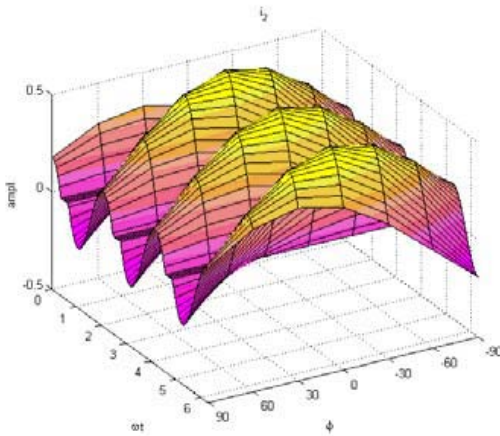


Figure 7.18: 3D plot of the DC-link currents at $M=0.8$, upper current i_2 (left), and medium current i_1 (right).

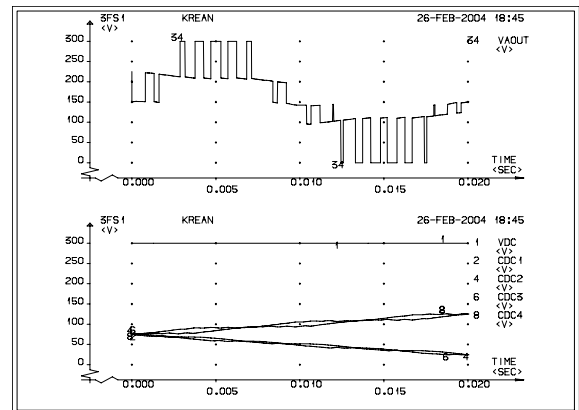
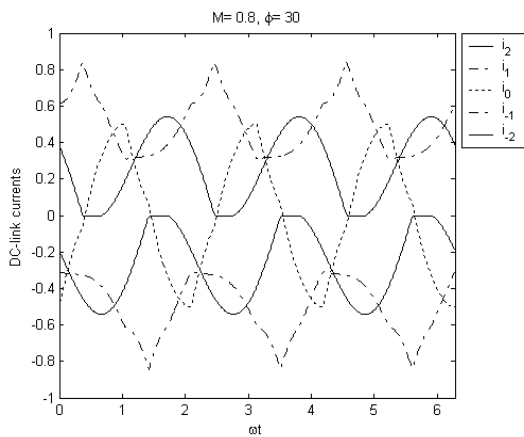


Figure 7.19: Close up view of the DC-link currents (left), and KREAN simulation (right) at $M=0.8$ and $\phi=30^\circ$.

As shown, by using standard modulation, the DC-bus in 5-level converters can not be balanced by a single DC-supply. In [59] a new modulation scheme is proposed, and by using this scheme, it is possible to balance the voltages by drawing equal amount of currents from the DC-link nodes. The disadvantage of this method is that the output voltage is limited because the modulation method utilizes all voltage levels within half a period of a fundamental output cycle, and modulation efficiency is decreased. A modulation method presented in [66] is reported to balance the DC-link voltages. Investigations show that this method also has a limit in output voltage, because the total modulation index is the mean value of the control signals use to balance the DC-link voltages. Also, to minimize the current drawn from the intermediate tapplings of the DC-bus, the output waveform will converge to a 3-level.

Hence, to balance the voltages, and obtain full waveform quality, it seems necessary to feed the DC-bus by more than 1 supply. By using a separate supply for each dc-link level, the balancing issues are solved. However, this solution is expensive. By using two symmetrical supplies as in Figure 7.20 (middle), the dc-bus is balanced with respect to the neutral point, but because of the equal current drawn from the intermediate DC-link nodes, unbalance will occur. The final solution is to use two asymmetrical supplies as shown to the right in Figure 7.20. By using this configuration the intermediate levels are supplied with a separate supply, and hence, the DC-link will be balanced. Figure 7.21 shows simulation examples with two symmetrical and asymmetrical supplies. With the asymmetrical supply, balancing of the DC-bus voltage is obtained.

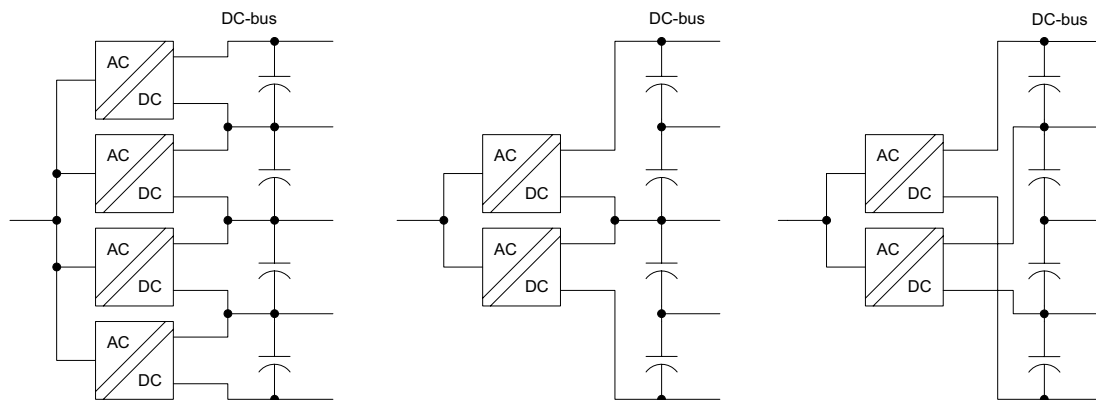


Figure 7.20: DC-bus supply for 5-level converter.

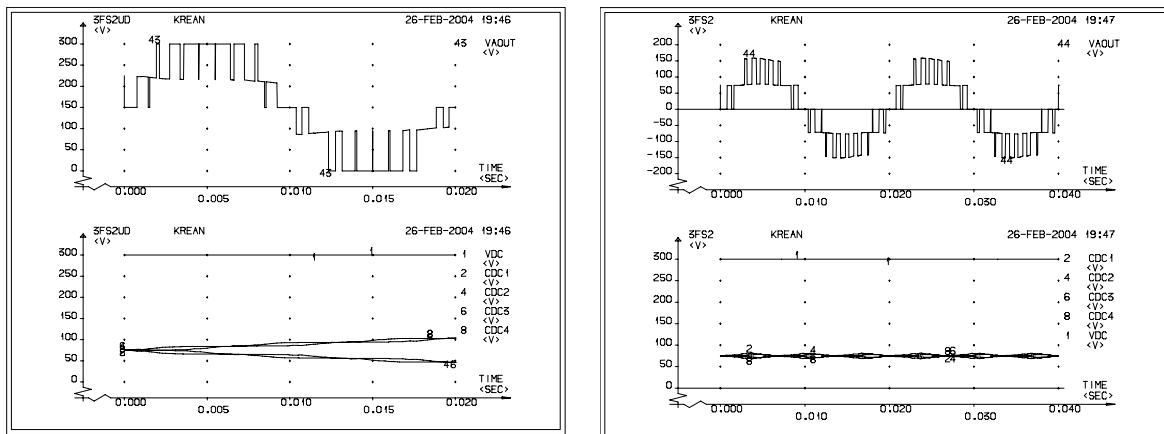


Figure 7.21: Two symmetrical supplies (left), asymmetrical supplies (right).

7.4.2 Verification by experiment

In Figure 7.22, the experiment setup used is shown. Only one phase of the 5-level converter constructed in Chapter 6 was used since the controller only has 12 independent PWM outputs. However, the principle of voltage balancing will be as for a three phase system. The currents drawn from the dc-bus will be $1/3$ of a three phase system. In addition, the charging/discharging frequency will be $1/3$ for this one phase system. The DSP controller board is the same as given in Chapter 6.2.5. Each AC-DC supply is 100V, thus giving a total DC-bus voltage of 200V. The load is an RL-load with $L_{load}=85\text{mH}$ and $R_{load}=50\Omega$.

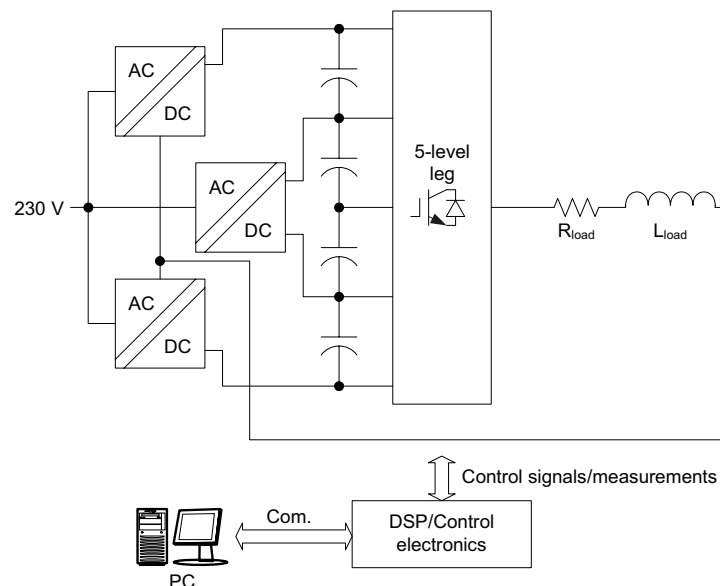


Figure 7.22: Experimental 5-level setup.

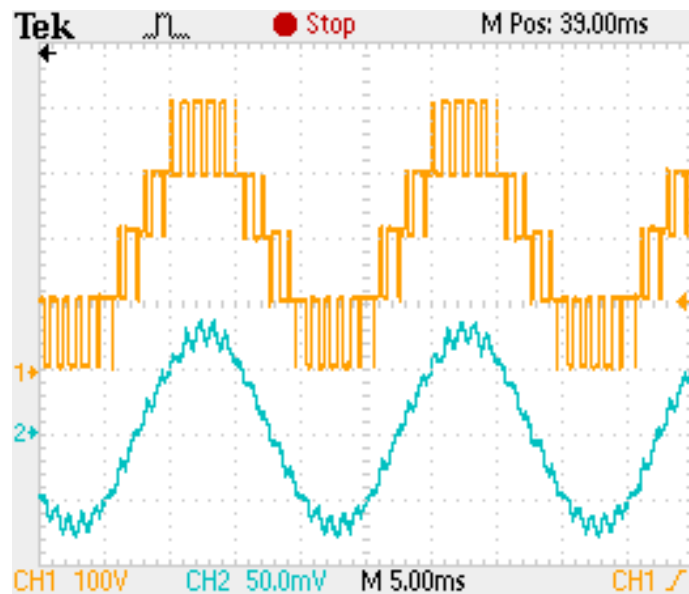


Figure 7.23: Output waveforms for 5-level converter at modulation index $M=0.8$. Trace1: Pole voltage [50V/div]. Trace 2: Phase current [1A/div].

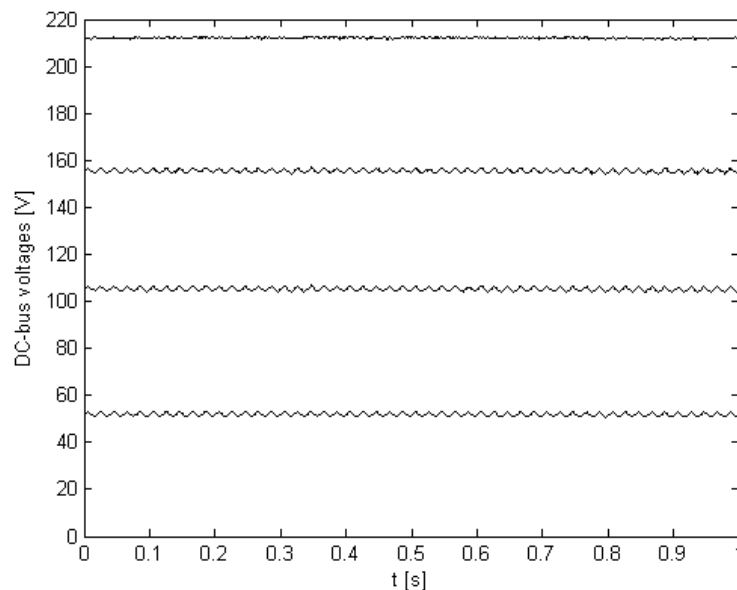


Figure 7.24: DC-bus voltages at $M=0.8$.

The figure shows that by connecting an isolated supply which supplies the intermediate DC-bus nodes, balanced condition is obtained.

7.4.3 Rectifier solutions in 5-level converters

As mentioned, the 5-level topology can balance the DC-bus by utilizing two asymmetrical DC-supplies. By simulation, it can be shown as in Figure 7.25, that the power drawn from the DC-supplies are not equal.

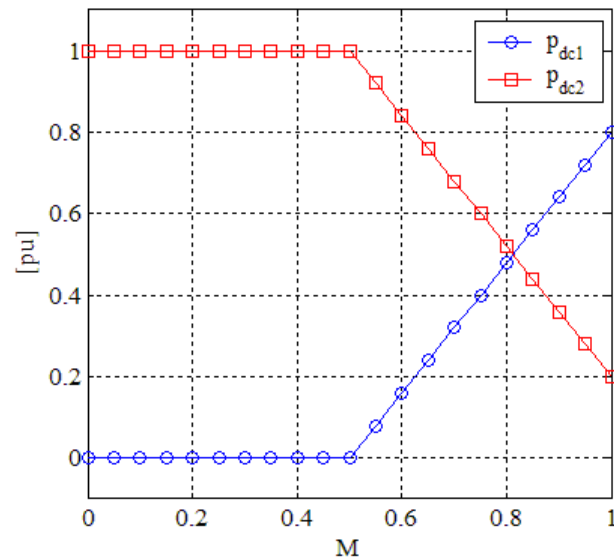


Figure 7.25: Distribution of DC-bus power for two asymmetrical DCbus supplies in a 5-level converter at pure resistive load at the output. p_{dc1} is the power from the main supply and p_{dc2} is the power from the intermediate supply.

One often used solution in large electrical motor drives is a 12-pulse rectifier solution [54]. By using two separate rectifiers in series supplied by a transformer with two separate secondary 3-phase windings, better current waveforms on the input side is obtained. One of the secondary sides is connected in a star configuration, and one is connected in delta configuration. The currents in the delta configuration will be phase shifted 30° with respect to the other windings. Hence, the first harmonic on the input side will be the 12th. Generally, harmonics will be $12k \pm 1$, where k is a non zero integer. Such a 12-pulse rectifier arrangement can be used as an asymmetrical DC-supply for a 5-level converter, but since the power of the two DC-supplies varies, the harmonic cancellation will not happened at all loads. This is indicated in Figure 7.26 and Figure 7.27, where a typical load case is simulated.

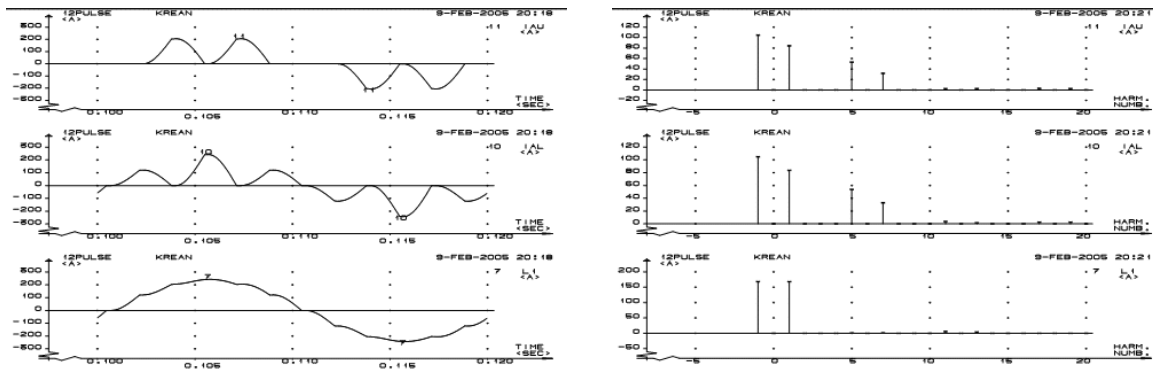


Figure 7.26. Input currents using a 12-pulse rectifier. Left: star-connected (top), delta-connected (middle), and total (bottom). Right. Corresponding harmonics. DC-power is the same in the two rectifiers.

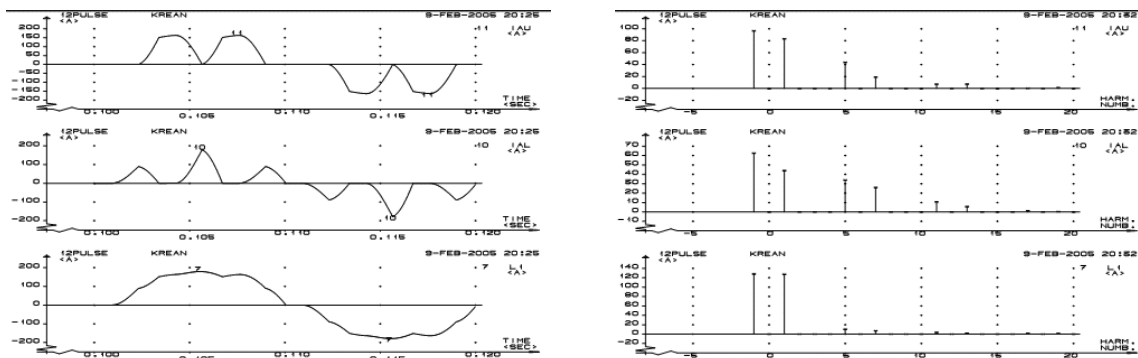


Figure 7.27: Input currents using a 12-pulse rectifier. Left: star-connected (top), delta-connected (middle), and total (bottom). Right: Corresponding harmonics. DC-power is lowered to the half in the intermediate rectifier (middle traces).

In Figure 7.26, the DC-bus power is equal in the two rectifiers, and full 12-pulse performance is obtained. In Figure 7.27, the power to the intermediate rectifier is lowered to the half of the outer rectifier, and lower harmonics in the total input current can be seen (e.g. 5th and 7th). An disadvantage of this 12-pulse rectifier arrangement is that each of the rectifiers must be dimensioned for the full DC-power since the power is depending on the modulation index as shown in Figure 7.25.

7.5 Conclusions

In this chapter, the problems with DC-bus balancing are discussed. The principles of average switching functions are used to visualize the behaviour of the DC-link currents. For the 3-level topology, space vector modulation is used to actively balance the neutral point. If the number of levels is increased, the balancing problems are more difficult to overcome. Some simulations and verifications in the lab on a 5-level converter are performed to illustrate the problem. By using two asymmetrical isolated DC-supplies, the DC-bus is balanced. Some simulations of a 12-pulse rectifier indicate that this is not an optimum solution in an asymmetrical arrangement. Active rectifiers can be a solution and might be costly and complex, but is not discussed any further in this thesis.

8 CONCLUSIONS AND SCOPE OF FURTHER WORK

8.1 Discussion and Conclusion

This thesis is dealing with important aspects concerning multilevel power conversion. In the First Chapter, a brief summary of the different topologies is given. From this, the Diode Clamped topology is chosen for further investigation. This is because of its increasing popularity in industrial applications and its promising performance. The Cascaded Multicell topology can generate the highest number of levels from a given number of switching devices and DC-busses. The main problem with this topology is that a separate, isolated DC-supply is needed for every DC-bus level and phase. Further, the Capacitor Clamped topology is presented in the literature as difficult to control, and needs balancing capacitors.

In the Second Chapter, modulation strategies are discussed. Main focus is on carrier based and space vector PWM. A generalization of carrier based modulation is given and simulation models show the differences between the different topologies and modulation methods.

One of the main focuses of the work is presented in chapters 3 and 4. Losses in multilevel converters, both dynamic and static losses, is not documented in the literature to a large extent. Sinusoidal carrier based PWM has been used to develop analytical expressions for both switching and conduction losses for 4- and 5-level topologies. Hence, easier comparison of different topologies, different use of switches etc. can be performed without time consuming simulations. There exists a variety of modulation methods for a given converter topology, but these are not compared with respect to losses. However, sinusoidal carrier PWM are one of the simplest schemes, and gives a good foundation for comparison. Chapter 4 shows a comparison of a 1 MW/1500 V drive. Already by using a 3-level topology, the losses can be reduced to about 60% of a conventional 2-level converter at same

loading and switching frequency. The main reason for this, is the very high switching losses of IGBTs in this voltage range (3300 V). In this case, the 4-level topology is superior to the 5-level topology, caused by the use of the same IGBTs (1200V) at this voltage level. Further, a 2300 V/3 MW drive was analysed for 3, 4 and 5-levels respectively. A better voltage utilization of the switches leads to the lowest losses for the 5-level topology. Hence, the losses are lowered by about 40% compared to a 3-level topology.

Further, analytical expressions for the ripple current on the AC-side of a 3-level converter are developed for 2 different modulation strategies. Experimental measurements on a three-level prototype in the lab and simulations are done to verify the analytical expressions. Extensive simulations on different 3-level modulations strategies has been done, and also 4- and 5-level sinusoidal CBPWM. The results shows that by extending the converter topology to a multilevel, harmonic currents can be reduced significantly. Complexity of the converter and control taken into account, the 3-level topology seems to be the most interesting topology.

One of the drawbacks of Diode Clamped Converters are problems with balancing of the DC-bus voltages when a single supply is used. In Chapter 7, the problems with DC-bus balancing are discussed. The principles of average switching functions are used to visualize the behaviour of the DC-link currents. For the 3-level topology, space vector modulation is used to actively balance the neutral point. If the number of levels is increased, the balancing problems are more difficult to overcome. Some simulations and verifications in the lab on a 5-level converter are performed to illustrate the problem. By using two asymmetrical isolated DC-supplies, the DC-bus is balanced.

8.2 Scope of Further work

Since the Multilevel Converter research area is large, and the technology quite young, there are still quite a few unfinished aspects to be solved.

First, the analytical loss calculations in Chapter 3 are only performed for 4-, and 5-level Diode Clamped Converters. A generalization of the expressions would be preferable, to extend it to n -levels. Further, loss calculations for other topologies should be developed to compare different topologies with losses. The loss expressions are only general in the form as average-, RMS-current and switching losses for each component in the converter topology. Models of the semiconductor components should be developed, and included in the generalized expressions. By this, optimization of the converter can better be achieved, as semiconductor parameters can be varied. For the 3-level topology, the SVPWM schemes should also be analysed for losses.

In Chapter 6, quite complicated expressions for the harmonic current in 3-level converters are developed, even if simplification is performed. The PWM methods used for the expressions are as simple as possible. In spite of this, the more advanced modulation methods should not only be simulated as in this thesis, but also be derived analytically.

For the balancing of the DC-bus voltages in 5-level converters, mainly converter operation is investigated in this thesis. Multilevel rectifiers should be investigated to balance the voltages in the DC-link. As the investigation in Chapter 7 shows, the rectifier can be simplified if asymmetrical DC-sources are used. Hence, the rectifier topology might also be simplified.

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APPENDIX

A RESULTS FROM SIMULATIONS OF A 4-LEVEL CONVERTER

The expressions for the RMS and average currents in the respective devices are verified by simulations in Saber with sinusoidal current sources. The load current is $100 A_{RMS}$. Verification where done in the modulation range $M = [0.2, 1]$ and $\varphi = [-150^\circ, 150^\circ]$, using a switching frequency of 1500 Hz. Figure A.1 and Figure A.2 shows the results. A significant deviation exist for in the clamping diode i_{D2a} for $\varphi = -45^\circ$, and in the freewheeling diode i_{D1a} for $\varphi = 0^\circ$. These deviations are caused, because the current levels are very low at these instances. For i_{D1a} the calculated currents are 0.53A and 0.02A for the RMS and average current respectively. The contribution to the total power loss will be minor. The worst deviation for i_{D2a} is for $M = 1$ and $\varphi = 0^\circ$, at 0.737 A.

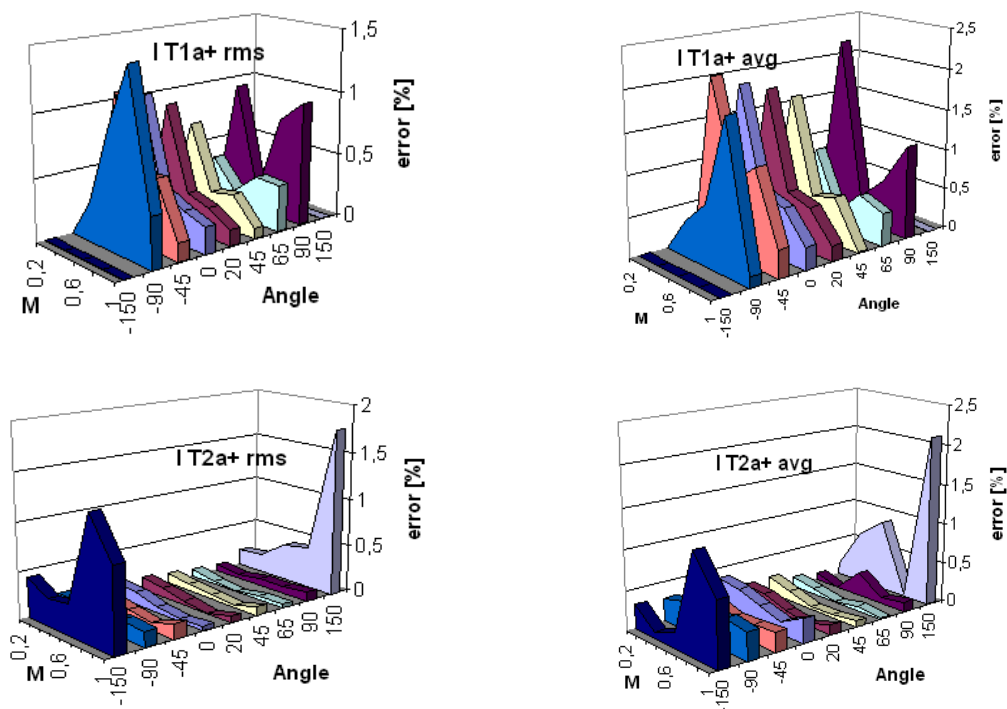


Figure A.1: Deviation for currents through components in the 4-level converter.

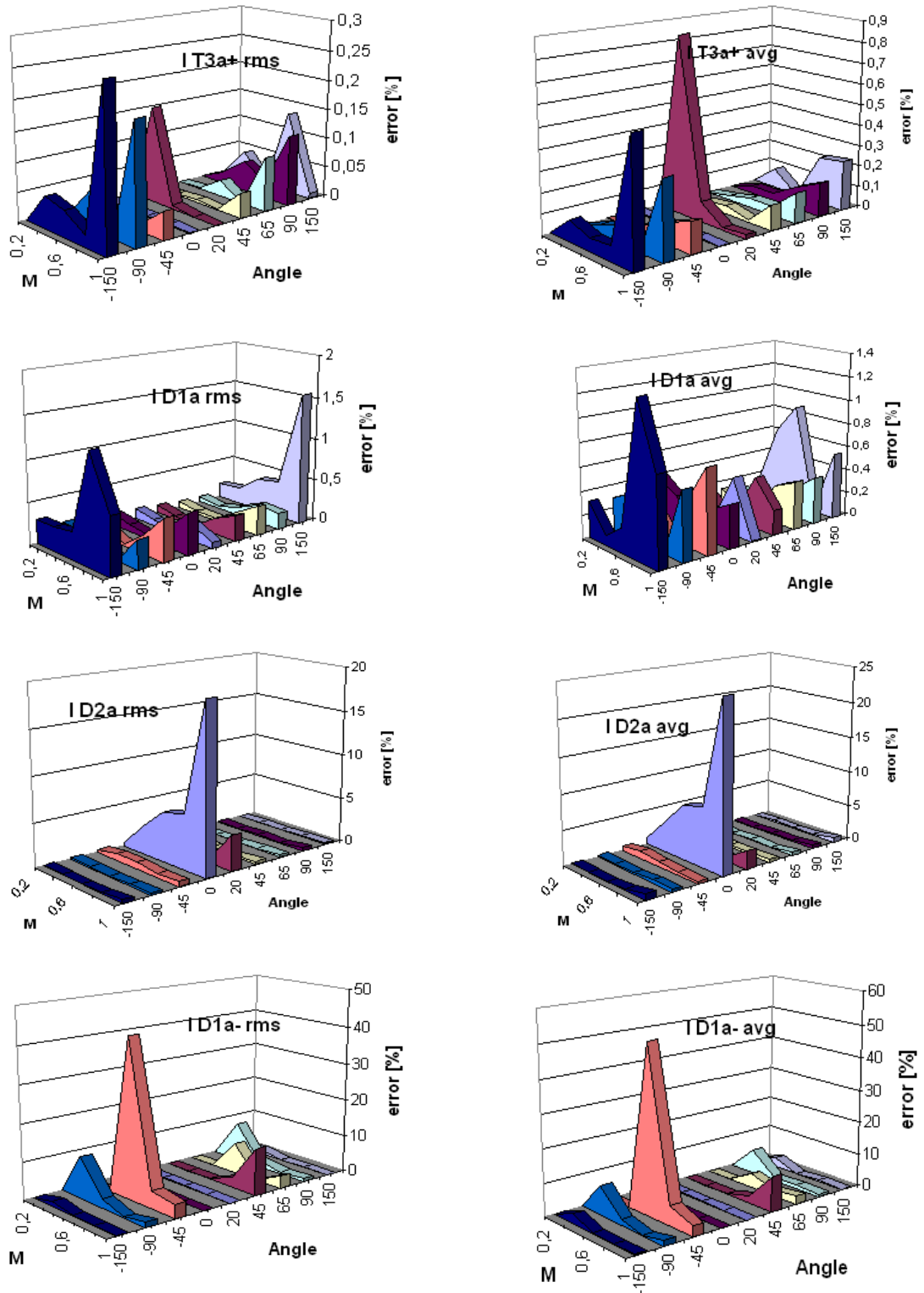


Figure A.2: Deviation in percent for currents through components in the 4-level converter (cont.).

B LOSS CALCULATIONS FOR 5-LEVEL CONVERTERS

B.1 Switching losses

For 4-level converters, a different set of formulas will be valid when operating with amplitude modulation factor less than 1/3. For 5-level converters, this limit is decreased to 1/2. Like for 4-level converters, inductive or capacitive load does not make any difference for the general formulas.

B.1.1 $M > 1/2$

The general formulas for switching losses in each component will be:

For T_{1a+} and T_{4a-} :

$$\pi - \arcsin(1/(2M)) < \varphi < \pi$$

$$P_{T_{1a+,sw}} = 0 \quad (\text{B.1})$$

$$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$$

$$\begin{aligned} P_{T_{1a+,sw}} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{array}{l} 4k_{1,T} \left(\sqrt{4M^2 - 1} \cos(\varphi) M - \sin(|\varphi|) M + 2M^2 \right) \\ + k_{2,T} \hat{I} \left(\begin{array}{l} \sqrt{4M^2 - 1} \cos(2\varphi) + \sin(2|\varphi|) (2M^2 - 1) \\ + 4M^2 (\pi - |\varphi| - \arcsin(\frac{1}{2M})) \end{array} \right) \end{array} \right) \end{aligned} \quad (\text{B.2})$$

$$\varphi < \arcsin(1/(2M))$$

$$\begin{aligned} P_{T_{1a+,sw}} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M} \left(\begin{array}{l} 4k_{1,T} \sqrt{4M^2 - 1} \cos(\varphi) \\ + \frac{k_{2,T} \hat{I}}{M} \left(\sqrt{4M^2 - 1} \cos(2\varphi) + 2M^2 (\pi - 2 \arcsin(\frac{1}{2M})) \right) \end{array} \right) \end{aligned} \quad (\text{B.3})$$

For T_{2a+} and T_{3a-} :

$$\pi - \arcsin(1/(2M)) < \varphi < \pi$$

$$\begin{aligned} P_{T_{2a+},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi} \left(4k_{1,T} (1 + \cos(\varphi)) + k_{2,T} \hat{I} (\sin(2|\varphi|) + 2\pi - 2\varphi) \right) \end{aligned} \quad (\text{B.4})$$

$$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$$

$$\begin{aligned} P_{T_{2a+},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} k_{1,T} i + k_{2,T} i^2 d\omega t \\ &= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{aligned} &4k_{1,T} \left(2M^2 \cos(\varphi) - M\sqrt{4M^2 - 1} \cos(\varphi) + M \sin(|\varphi|) \right) \\ &+ k_{2,T} \hat{I} \left(-\sqrt{4M^2 - 1} \cos(2\varphi) + \sin(2|\varphi|) + 4 \arcsin(\frac{1}{2M}) M^2 \right) \end{aligned} \right) \end{aligned} \quad (\text{B.5})$$

$$\varphi < \arcsin(1/(2M))$$

$$\begin{aligned} P_{T_{2a+},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} k_{1,T} i + k_{2,T} i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} k_{1,T} i + k_{2,T} i^2 d\omega t \right) \\ &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M} \left(\begin{aligned} &4k_{1,T} (-\sqrt{4M^2 - 1} \cos(\varphi) + M + M \cos(\varphi)) + \frac{k_{2,T} \hat{I}}{M} \\ &\left(-\sqrt{4M^2 - 1} \cos(2\varphi) + M^2 (\sin(2|\varphi|) + 4 \arcsin(\frac{1}{2M}) + 2\varphi) \right) \end{aligned} \right) \end{aligned} \quad (\text{B.6})$$

For T_{3a+} and T_{2a-} :

$$\pi - \arcsin(1/(2M)) < \varphi < \pi$$

$$\begin{aligned} P_{T_{3a+},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \left(\int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} k_{1,T} i + k_{2,T} i^2 d\omega t + \int_{2\pi - \arcsin(\frac{1}{2M})}^{\pi + \varphi} k_{1,T} i + k_{2,T} i^2 d\omega t \right) \\ &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M^2} \left(\begin{aligned} &4k_{1,T} M \left(\sqrt{4M^2 - 1} \cos(\varphi) + M - M \cos(\varphi) \right) \\ &+ k_{2,T} \hat{I} \left(-\sqrt{4M^2 - 1} \cos(2\varphi) - M^2 \sin(|2\varphi|) + 4M^2 \arcsin(\frac{1}{2M}) \right) \\ &- 2M^2 \pi + 2M^2 |\varphi| \end{aligned} \right) \end{aligned} \quad (\text{B.7})$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned}
 P_{T3a+,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} k_{1,T}i + k_{2,T}i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{aligned} &4k_{1,T}M \left(\sqrt{4M^2 - 1} \cos(\varphi) + \sin(|\varphi|) - 2M \cos(\varphi) \right) \\ &+ k_{2,T} \hat{I} \left(-\sqrt{4M^2 - 1} \cos(2\varphi) - \sin(|2\varphi|) + 4M^2 \arcsin(\frac{1}{2M}) \right) \end{aligned} \right) \quad (B.8)
 \end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$\begin{aligned}
 P_{T3,SW} &= \frac{V_d}{4} \frac{1}{2\pi} f_{sw} \int_{\pi}^{\pi + \varphi} k_{1,T}i + k_{2,T}i^2 d\omega t \\
 &= \frac{V_d f_{sw} \hat{I}}{32\pi} \left(4k_{1,T} (1 - \cos(\varphi)) + k_{2,T} \hat{I} (2\varphi - \sin(|2\varphi|)) \right) \quad (B.9)
 \end{aligned}$$

For T_{4a+} and T_{1a-} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned}
 P_{T4a+,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{2M})}^{2\pi - \arcsin(\frac{1}{2M})} k_{1,T}i + k_{2,T}i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M^2} \left(\begin{aligned} &-4k_{1,T}M \sqrt{4M^2 - 1} \cos(\varphi) \\ &+ k_{2,T} \hat{I}_N \left(\sqrt{4M^2 - 1} \cos(2\varphi) + 2M^2 \pi - 4M^2 \arcsin(\frac{1}{2M}) \right) \end{aligned} \right) \quad (B.10)
 \end{aligned}$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned}
 P_{T4a+,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{2M})}^{\pi + \varphi} k_{1,T}i + k_{2,T}i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{aligned} &4k_{1,T}M \left(2M - \sqrt{4M^2 - 1} \cos(\varphi) - M \sin(|\varphi|) \right) \\ &+ k_{2,T} \hat{I} \left(\sqrt{4M^2 - 1} \cos(2\varphi) + \sin(|2\varphi|) (1 - 2M^2) \right) \\ &+ 4M^2 \left(|\varphi| - \arcsin(\frac{1}{2M}) \right) \end{aligned} \right) \quad (B.11)
 \end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$P_{T4a+,sw} = 0 \quad (B.12)$$

For D_{1a-} , D_{2a-} , D_{3a-} , D_{4a-} , D_{1a+} , D_{2a+} , D_{3a+} and D_{4a+} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned}
 P_{D_{1a-},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{2M})}^{2\pi - \arcsin(\frac{1}{2M})} k_{1,D} i + k_{2,D} i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M^2} \left(\begin{array}{l} -4k_{1,D} M \sqrt{4M^2 - 1} \cos(\varphi) \\ +k_{2,D} \hat{I} \left(\sqrt{4M^2 - 1} \cos(2\varphi) + 2M^2 \pi - 4M^2 \arcsin(\frac{1}{2M}) \right) \end{array} \right) \quad (B.13)
 \end{aligned}$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned}
 P_{D_{1a-},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi + \arcsin(\frac{1}{2M})}^{\pi + \varphi} k_{1,D} i + k_{2,D} i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{array}{l} 4k_{1,D} M \left(2M - \sqrt{4M^2 - 1} \cos(\varphi) - \sin(|\varphi|) \right) \\ +k_{2,D} \hat{I} \left(\begin{array}{l} \sqrt{4M^2 - 1} \cos(2\varphi) \\ + \sin(2|\varphi|) (1 - 2M^2) + 4M^2 (|\varphi| - \arcsin(\frac{1}{2M})) \end{array} \right) \end{array} \right) \quad (B.14)
 \end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$P_{D_{1a-},sw} = 0 \quad (B.15)$$

For D_{1a} and D_{6a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$P_{D_{1a},sw} = 0 \quad (B.16)$$

$\arcsin(1/(3M)) < \varphi < \pi - \arcsin(1/(3M))$

$$\begin{aligned}
 P_{D_{1a},sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} k_{1,D} i + k_{2,D} i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{array}{l} 4Mk_{1,D} \left(\sqrt{4M^2 - 1} \cos(\varphi) - \sin(|\varphi|) + 2M \right) \\ +k_{2,D} \hat{I} \left(\begin{array}{l} \sqrt{4M^2 - 1} \cos(2\varphi) + \sin(2|\varphi|) (1 - 2M^2) \\ +4M^2 (-|\varphi| + \pi - \arcsin(\frac{1}{2M})) \end{array} \right) \end{array} \right) \quad (B.17)
 \end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$\begin{aligned}
P_{D1a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} k_{1,D}i + k_{2,D}i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M^2} \left(\begin{aligned} &4k_{1,D}M\sqrt{4M^2 - 1} \cos(\varphi) \\ &+ k_{2,D} \hat{I} \left(\sqrt{4M^2 - 1} \cos(2\varphi) + 2M^2 (\pi - 2 \arcsin(\frac{1}{2M})) \right) \end{aligned} \right) \quad (B.18)
\end{aligned}$$

For D_{2a} and D_{3a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned}
P_{D2a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi} k_{1,D}i + k_{2,D}i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi} \left(4k_{1,D} (1 + \cos(\varphi)) + k_{2,D} \hat{I} (\sin(2|\varphi|) + 2\pi - 2|\varphi|) \right) \quad (B.19)
\end{aligned}$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned}
P_{D2a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} k_{1,D}i + k_{2,D}i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{aligned} &4k_{1,D}M \left(2M \cos(\varphi) - \sqrt{4M^2 - 1} \cos(\varphi) + \sin(|\varphi|) \right) \\ &+ k_{2,D} \hat{I} \left(-\sqrt{4M^2 - 1} \cos(2\varphi) + \sin(2|\varphi|) + 4M^2 \arcsin(\frac{1}{2M}) \right) \end{aligned} \right) \quad (B.20)
\end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$\begin{aligned}
P_{D2a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} k_{1,D}i + k_{2,D}i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} k_{1,D}i + k_{2,D}i^2 d\omega t \right) \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M^2} \left(\begin{aligned} &4k_{1,D}M \left(-\sqrt{4M^2 - 1} \cos(\varphi) + M \cos(\varphi) + M \right) \\ &+ k_{2,D} \hat{I} \left(\begin{aligned} &-\sqrt{4M^2 - 1} \cos(2\varphi) \\ &+ M^2 (\sin(2|\varphi|) + 4 \arcsin(\frac{1}{2M}) - 2\varphi) \end{aligned} \right) \end{aligned} \right) \quad (B.21)
\end{aligned}$$

For D_{3a} and D_{4a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned}
P_{D3a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} k_{1,D} i + k_{2,D} i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi M^2} \left(\begin{aligned} &4k_{1,D} M \left(\sqrt{4M^2 - 1} \cos(\varphi) + M - M \cos(\varphi) \right) \\ &+ k_{2,D} \hat{I} \left(-\sqrt{4M^2 - 1} \cos(2\varphi) - M^2 \sin(2|\varphi|) + 4M^2 \arcsin(\frac{1}{2M}) \right) \\ &- 2M^2 \pi + 2M^2 |\varphi| \end{aligned} \right) \quad (B.22)
\end{aligned}$$

$$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$$

$$\begin{aligned}
P_{D3a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} k_{1,D} i + k_{2,D} i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{64\pi M^2} \left(\begin{aligned} &4k_{1,D} M \left(\sqrt{4M^2 - 1} \cos(\varphi) + \sin(|\varphi|) - 2M \cos(\varphi) \right) \\ &+ k_{2,D} \hat{I} \left(-\sqrt{4M^2 - 1} \cos(2\varphi) - \sin(2|\varphi|) + 4M^2 \arcsin(\frac{1}{2M}) \right) \end{aligned} \right) \quad (B.23)
\end{aligned}$$

$$\varphi < \arcsin(1/(2M))$$

$$\begin{aligned}
P_{D3a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi}^{\pi + \varphi} k_{1,D} i + k_{2,D} i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi} \left(4k_{1,D} (1 - \cos(\varphi)) + k_{2,D} \hat{I} (2|\varphi| - \sin(2|\varphi|)) \right) \quad (B.24)
\end{aligned}$$

B.1.2 $M < 1/2$

Since T_{1j+} and T_{4j-} are open and T_{1j-} and T_{4+} are closed in this interval, they will have no switching losses. Neither the freewheeling diodes $D_{1j+}-D_{4j+}$ and $D_{1j-}-D_{4j-}$ will have switching losses. Similar, the outermost clamping diodes D_{1j} and D_{6j} never switches in this interval.

For T_{2a+} and T_{3a-} :

$$\begin{aligned}
P_{T2a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi} k_{1,T} i + k_{2,T} i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi} \left(4k_{1,T} (\cos(\varphi) + 1) + k_{2,T} \hat{I} (\sin(2|\varphi|) + 2\pi - 2|\varphi|) \right) \quad (B.25)
\end{aligned}$$

For T_{3a+} and T_{2a-} :

$$\begin{aligned}
P_{T3a,sw} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\pi}^{\pi + \varphi} k_{1,T} i + k_{2,T} i^2 d\omega t \\
&= \frac{U_{dc} f_{sw} \hat{I}}{32\pi} \left(4k_{1,T} (1 - \cos(\varphi)) + k_{2,T} \hat{I} (2|\varphi| - \sin(2|\varphi|)) \right) \quad (B.26)
\end{aligned}$$

For D_{2a} and D_{5a} :

$$\begin{aligned}
 P_{D_{2a,sw}} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi} k_{1,D} i + k_{2,D} i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{32\pi} \left(4k_{1,D} (\cos(\varphi) + 1) + k_{2,D} \hat{I} (\sin(2|\varphi|) + 2\pi - 2|\varphi|) \right)
 \end{aligned} \tag{B.27}$$

For D_{3a} and D_{4a} :

$$\begin{aligned}
 P_{D_{3a,sw}} &= \frac{U_{dc}}{4} \frac{1}{2\pi} f_{sw} \int_{\varphi}^{\pi+\varphi} k_{1,D} i + k_{2,D} i^2 d\omega t \\
 &= \frac{U_{dc} f_{sw} \hat{I}}{16\pi} (4k_{1,D} + k_{2,D} \hat{I} \pi)
 \end{aligned} \tag{B.28}$$

B.2 Conducting losses

As for the 4-level topology in Chapter 3.4.2, the expressions are based on Eq.(3.1). By using Figure 3.24 the integral limits for the respective devices can be found.

The formulas below are related to phase a . In a 3-phase converter, the expressions for the other two phases will be similar as stated before. Hence, the expressions are:

B.2.1 $M > 1/2$

For T_{1a+} and T_{4a-} :

$$\pi - \arcsin(1/(2M)) < \varphi < \pi$$

$$I_{T_{1a+,avg}} = 0 \tag{B.29}$$

$$I_{T_{1a+,rms}}^2 = 0 \tag{B.30}$$

$$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$$

$$\begin{aligned}
 I_{T_{1a+,avg}} &= \frac{1}{2\pi} \int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} d_{1a} \cdot i d\omega t \\
 &= \frac{\hat{I}}{8\pi \cdot M} \left(\begin{array}{l} -\cos(\varphi) \sqrt{4M^2 - 1} + \sin(|\varphi|) (4M^2 + 1) \\ +4M^2 \cos(\varphi) (\pi - \arcsin(\frac{1}{2M}) - |\varphi|) - 4M \end{array} \right)
 \end{aligned} \tag{B.31}$$

$$\begin{aligned}
I_{T_{1a+},rms}^2 &= \frac{1}{2\pi} \int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} d_{1a} \cdot i^2 d\omega t \\
&= \frac{\hat{I}^2}{48\pi \cdot M^2} \left(\begin{aligned} &\sqrt{4M^2 - 1}(12M^2 - \cos(2\varphi) + 4M^2 \cos(2\varphi)) \\ &+ \sin(2|\varphi|)(1 - 6M^2) + 4M^2(3 \arcsin(\frac{1}{2M}) - 3\pi) \\ &+ 8M \cos(\varphi) + 3|\varphi| \end{aligned} \right) \tag{B.32}
\end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$\begin{aligned}
I_{T_{1a+},avg} &= \frac{1}{2\pi} \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} d_{1a} \cdot id\omega t \\
&= \frac{\hat{I} \cos(\varphi)}{4\pi} \left(\frac{-1}{M} \sqrt{4M^2 - 1} + 4M\pi - 4M \arcsin(\frac{1}{2M}) \right) \tag{B.33}
\end{aligned}$$

$$\begin{aligned}
I_{T_{1a+},rms}^2 &= \frac{1}{2\pi} \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} d_{1a} \cdot i^2 d\omega t \\
&= \frac{\hat{I}^2}{24\pi M} \left(\begin{aligned} &\sqrt{4M^2 - 1} \left(12M - \frac{1}{M} \cos(2\varphi) + 4M \cos(2\varphi) \right) \\ &+ 6M(2 \arcsin(\frac{1}{2M}) - \pi) \end{aligned} \right) \tag{B.34}
\end{aligned}$$

For T_{2a+} and T_{3a-} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned}
I_{T_{2a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I} M}{2\pi} (\sin(|\varphi|) + \cos(\varphi)\pi + \cos(\varphi)|\varphi|) \tag{B.35}
\end{aligned}$$

$$\begin{aligned}
I_{T_{2a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2 M}{6\pi} (3 + \cos(2\varphi) + \cos(\varphi)) \tag{B.36}
\end{aligned}$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned}
I_{T_{2a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} id\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{8\pi M} \left(\sqrt{4M^2 - 1} \cos(\varphi) + 4M + 4M^2 \cos(\varphi) \cdot \arcsin(\frac{1}{2M}) - \sin(|\varphi|) \right) \tag{B.37}
\end{aligned}$$

$$\begin{aligned}
I_{T_{2a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{-\hat{I}^2}{48\pi M^2} \left(\begin{aligned} &\sqrt{4M^2 - 1} (-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) \\ &+ 3M^2 (4|\varphi| - 4\pi + 4 \arcsin(\frac{1}{2M}) - 8M - 2M \cos(2\varphi)) \\ &+ \sin(2|\varphi|)(1 - 6M^2) \end{aligned} \right) \tag{B.38}
\end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$\begin{aligned}
I_{T_{2a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} d_{2a} \cdot id\omega t + \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} id\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{4\pi} \left(\begin{aligned} &\frac{\sqrt{4M^2 - 1}}{M} \cos(\varphi) + 2M \sin(|\varphi|) \\ &+ 2M \cos(\varphi)(2 \arcsin(\frac{1}{2M}) - |\varphi|) \end{aligned} \right) \tag{B.39}
\end{aligned}$$

$$\begin{aligned}
I_{T_{2a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} d_{2a} \cdot i^2 d\omega t + \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{-\hat{I}^2}{\pi M^2} \left(\begin{aligned} &\sqrt{4M^2 - 1} (12M^2 + 4M^2 \cos(2\varphi) - \cos(2\varphi)) \\ &+ 12M^2 \arcsin(\frac{1}{2M}) - 16M^3 \cos(\varphi) - 6M^2 \pi - 12M^3 - 4M^3 \cos(2\varphi) \end{aligned} \right) \tag{B.40}
\end{aligned}$$

For T_{3a+} and T_{2a-} :

$\pi - \arcsin(1/(3M)) < \varphi < \pi$

$$\begin{aligned}
I_{T_{3a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} id\omega t + \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} d_{3a} \cdot id\omega t + \int_{2\pi - \arcsin(\frac{1}{2M})}^{\pi + \varphi} d_{3a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{4\pi M} \left(\begin{aligned} &\sqrt{4M^2 - 1} \cos(\varphi) + 4M \\ &+ 2M^2 (2 \cos(\varphi) \arcsin(\frac{1}{2M}) - \sin(|\varphi|) - \cos(\varphi)\pi + \cos(\varphi)|\varphi|) \end{aligned} \right) \tag{B.41}
\end{aligned}$$

$$\begin{aligned}
I_{T_{3a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} i^2 d\omega t + \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} d_{3a} \cdot i^2 d\omega t + \int_{2\pi - \arcsin(\frac{1}{2M})}^{\pi + \varphi} d_{3a} \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{24\pi M^2} \left(\begin{aligned} &\sqrt{4M^2 - 1} (-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) \\ &+ 4M^2 (-2 \cos(2\varphi)M + 6 \arcsin(\frac{1}{2M}) + 8M \cos(\varphi) - 6M) \end{aligned} \right) \tag{B.42}
\end{aligned}$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned} I_{T_{3a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} id\omega t + \int_{\pi}^{\pi+\arcsin(\frac{1}{2M})} d_{3a} \cdot id\omega t \right) \\ &= \frac{\hat{I}}{8\pi M} \left(\sqrt{4M^2 - 1} \cos(\varphi) + 4M \right. \\ &\quad \left. + 4M^2 \cos(\varphi) \arcsin(\frac{1}{2M}) + \sin(|\varphi|) \right) \end{aligned} \quad (\text{B.43})$$

$$\begin{aligned} I_{T_{3a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} i^2 d\omega t + \int_{\pi}^{\pi+\arcsin(\frac{1}{2M})} d_{3a} \cdot i^2 d\omega t \right) \\ &= \frac{\hat{I}^2}{48\pi M^2} \left(\sqrt{4M^2 - 1} (-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) - \sin(|2\varphi|) \right. \\ &\quad \left. + M^2 \left(12\pi - 12\varphi - 8\cos(2\varphi)M \right. \right. \\ &\quad \left. \left. + 12\arcsin(\frac{1}{2M}) + 6\sin(|2\varphi|) - 24M \right) \right) \end{aligned} \quad (\text{B.44})$$

$\varphi < \arcsin(1/(2M))$

$$I_{T_{3a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi} id\omega t + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} d_{3a} \cdot id\omega t = \frac{\hat{I}}{2\pi} (2 - M \sin(|\varphi|) + M \cos(\varphi) |\varphi|) \quad (\text{B.45})$$

$$\begin{aligned} I_{T_{3a+},rms}^2 &= \frac{1}{2\pi} \int_{\varphi}^{\pi} i^2 d\omega t + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} d_{3a} \cdot i^2 d\omega t \\ &= \frac{\hat{I}^2}{12\pi} (3\pi + 8M \cos(\varphi) - 6M - 2M \cos(2\varphi)) \end{aligned} \quad (\text{B.46})$$

For T_{4a+} and T_{1a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned} I_{T_{4a+},avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{2M})} id\omega t + \int_{\pi+\arcsin(\frac{1}{2M})}^{2\pi-\arcsin(\frac{1}{2M})} d_{4a} \cdot id\omega t + \int_{2\pi-\arcsin(\frac{1}{2M})}^{\pi+\varphi} id\omega t \right) \\ &= \frac{\hat{I}}{4\pi M} \left(-\sqrt{4M^2 - 1} \cos(\varphi) + 4M \right. \\ &\quad \left. + 2M^2 (\cos(\varphi)\pi - 2\cos(\varphi) \arcsin(\frac{1}{2M})) \right) \end{aligned} \quad (\text{B.47})$$

$$\begin{aligned} I_{T_{4a+},rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{2M})} i^2 d\omega t + \int_{\pi+\arcsin(\frac{1}{2M})}^{2\pi-\arcsin(\frac{1}{2M})} d_{4a} \cdot i^2 d\omega t + \int_{2\pi-\arcsin(\frac{1}{2M})}^{\pi+\varphi} i^2 d\omega t \right) \\ &= \frac{\hat{I}^2}{24\pi M^2} \left(\sqrt{4M^2 - 1} (\cos(2\varphi) - 12M^2 - 4M^2 \cos(2\varphi)) \right. \\ &\quad \left. + 12M^2 (\pi - \arcsin(\frac{1}{2M})) \right) \end{aligned} \quad (\text{B.48})$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$I_{T4a+,avg} = \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{2M})} id\omega t + \int_{\pi+\arcsin(\frac{1}{2M})}^{\pi+\varphi} d_{4a} \cdot id\omega t \right) \quad (B.49)$$

$$= \frac{\hat{I}}{8\pi M} \left(\begin{array}{l} -\sqrt{4M^2-1} \cos(\varphi) + 12M - \sin(|\varphi|) \\ +4M^2(-\sin(|\varphi|) + |\varphi| \cos(\varphi) - \cos(\varphi) \arcsin(\frac{1}{2M})) \end{array} \right)$$

$$I_{T4a+,rms}^2 = \frac{1}{2\pi} \left(\int_{\varphi}^{\pi+\arcsin(\frac{1}{2M})} i^2 d\omega t + \int_{\pi+\arcsin(\frac{1}{2M})}^{\pi+\varphi} d_{4a} \cdot i^2 d\omega t \right) \quad (B.50)$$

$$= \frac{\hat{I}^2}{48\pi M^2} \left(\begin{array}{l} \sqrt{4M^2-1}(\cos(2\varphi) - 12M^2 - 4M^2 \cos(2\varphi)) + \sin(|2\varphi|) \\ +M^2(12\pi + 12|\varphi| + 32\cos(\varphi)M - 12\arcsin(\frac{1}{2M}) - 6\sin(|2\varphi|)) \end{array} \right)$$

$\varphi < \arcsin(1/(2M))$

$$I_{T4a+,avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} id\omega t = \frac{\hat{I}}{\pi} \quad (B.51)$$

$$I_{T4a+,rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} i^2 d\omega t = \frac{\hat{I}^2}{4} \quad (B.52)$$

For D_{1a-} , D_{2a-} , D_{3a-} , D_{4a-} , D_{1a+} , D_{2a+} , D_{3a+} and D_{4a+} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$I_{D1a-,avg} = \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{2M})}^{2\pi-\arcsin(\frac{1}{2M})} (1-d_{4a}) \cdot id\omega t \right) \quad (B.53)$$

$$= \frac{\hat{I}}{4\pi M} \left(\begin{array}{l} \sqrt{4M^2-1} - 2M^2(\pi - 2\arcsin(\frac{1}{2M})) \\ -4M + \sin(|\varphi|) \end{array} \right)$$

$$I_{D1a-,rms}^2 = \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{2M})}^{2\pi-\arcsin(\frac{1}{2M})} (1-d_{4a}) \cdot i^2 d\omega t \right) \quad (B.54)$$

$$= \frac{\hat{I}^2}{24\pi M^2} \left(\begin{array}{l} \sqrt{4M^2-1}(-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) \\ +6M^2(2\arcsin(\frac{1}{2M}) - \pi) \end{array} \right)$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned} I_{D1a-,avg} &= \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{2M})}^{\pi+\varphi} (1-d_{4a}) \cdot id\omega t \right) \\ &= \frac{\hat{I}}{8\pi M} \left(\begin{array}{l} \sqrt{4M^2-1} \cos(\varphi) + 4M^2 (\sin(|\varphi|) - |\varphi| \cos(\varphi) + \cos(\varphi) \arcsin(\frac{1}{2M})) \\ -4M + \sin(|\varphi|) \end{array} \right) \end{aligned} \quad (\text{B.55})$$

$$\begin{aligned} I_{D1a-,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{2M})}^{\pi+\varphi} (1-d_{4a}) \cdot i^2 d\omega t \right) \\ &= \frac{\hat{I}^2}{48\pi M^2} \left(\begin{array}{l} \sqrt{4M^2-1} (-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) - \sin(|2\varphi|) \\ + M^2 (-12|\varphi| - 32 \cos(\varphi)M + 12 \arcsin(\frac{1}{2M}) + 6 \sin(|2\varphi|)) \end{array} \right) \end{aligned} \quad (\text{B.56})$$

$\varphi < \arcsin(1/(2M))$

$$I_{D1a-,avg} = 0 \quad (\text{B.57})$$

$$I_{D1a-,rms}^2 = 0 \quad (\text{B.58})$$

For D_{1a} and D_{6a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned} I_{D1a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} d_{2a} \cdot id\omega t \right) \\ &= \frac{\hat{I} M}{2\pi} (\sin(|\varphi|) + \cos(\varphi)\pi + \cos(\varphi)|\varphi|) \end{aligned} \quad (\text{B.59})$$

$$\begin{aligned} I_{D1a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} d_{2a} \cdot i^2 d\omega t \right) \\ &= \frac{\hat{I}^2 M}{6\pi} (3 + \cos(2\varphi) + \cos(\varphi)) \end{aligned} \quad (\text{B.60})$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$\begin{aligned} I_{D1a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi-\arcsin(\frac{1}{2M})} (1-d_{1a}) id\omega t + \int_{\pi-\arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot id\omega t \right) \\ &= \frac{\hat{I}}{4\pi M} \left(\begin{array}{l} \sqrt{4M^2-1} \cos(\varphi) - \sin(|\varphi|) + 4M \\ + 2M^2 (-\sin(|\varphi|) - \pi \cos(\varphi) + 2 \cos(\varphi) \arcsin(\frac{1}{2M}) - |\varphi| \cos(\varphi)) \end{array} \right) \end{aligned} \quad (\text{B.61})$$

$$\begin{aligned}
I_{D1a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi - \arcsin(\frac{1}{2M})} (1 - d_{1a}) i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot i^2 d\omega t \right) \\
&= \frac{-\hat{I}^2}{24\pi M^2} \left(\begin{array}{l} \sqrt{4M^2 - 1}(-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) + \sin(|2\varphi|) \\ + M^2 \left(12\varphi + 16 \cos(\varphi)M + 12 \arcsin(\frac{1}{2M}) - 6 \sin(|2\varphi|) \right) \\ -12\pi - 12M - 4M \cos(2\varphi) \end{array} \right) \quad (B.62)
\end{aligned}$$

$\varphi < \arcsin(1/(2M))$

$$\begin{aligned}
I_{D1a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} d_{2a} \cdot id\omega t + \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} (1 - d_{1a}) \cdot id\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{2\pi M} \left(\begin{array}{l} \sqrt{4M^2 - 1} \cos(\varphi) + M^2 \left(4 \cos(\varphi) \arcsin(\frac{1}{2M}) + \sin(|\varphi|) \right) \\ - \cos(\varphi) |\varphi| - \cos(\varphi) \pi \end{array} \right) \quad (B.63)
\end{aligned}$$

$$\begin{aligned}
I_{D1a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} d_{2a} i^2 d\omega t + \int_{\arcsin(\frac{1}{2M})}^{\pi - \arcsin(\frac{1}{2M})} (1 - d_{1a}) i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} d_{2a} i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{12\pi M^2} \left(\begin{array}{l} \sqrt{4M^2 - 1}(-12M^2 - 4M^2 \cos(2\varphi) + \cos(2\varphi)) + \\ M^2(-12 \arcsin(\frac{1}{2M}) + 2M \cos(2\varphi) + 6M\pi + 8M \cos(\varphi) + 6M) \end{array} \right) \quad (B.64)
\end{aligned}$$

For D_{2a} and D_{5a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$\begin{aligned}
I_{D2a,avg} &= \frac{1}{2\pi} \left(\int_{\varphi}^{\pi} (1 - d_{2a}) id\omega t + \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} d_{3a} \cdot id\omega t + \int_{2\pi - \arcsin(\frac{1}{2M})}^{\pi + \varphi} d_{3a} \cdot id\omega t \right) \\
&= \frac{\hat{I}}{4\pi M^2} \left(\begin{array}{l} 4M^2(-\sin(|\varphi|) - \cos(\varphi)\pi + \cos(\varphi)|\varphi| + \cos(\varphi) \cdot \arcsin(\frac{1}{2M})) \\ + 4 + \cos(\varphi)\sqrt{4M^2 - 1} \end{array} \right) \quad (B.65)
\end{aligned}$$

$$\begin{aligned}
I_{D2a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} (1 - d_{2a}) i^2 d\omega t + \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} d_{3a} \cdot i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{24\pi M^2} \left(\begin{array}{l} \sqrt{4M^2 - 1}(-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) \\ + 4M^2(-2 \cos(2\varphi)M + 3 \arcsin(\frac{1}{2M}) - 6M) \end{array} \right) \quad (B.66)
\end{aligned}$$

$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$

$$I_{D_{2a},avg} = \frac{1}{2\pi} \left(\int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} (1 - d_{2a}) id\omega t + \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} d_{3a} \cdot id\omega t \right) = \frac{\hat{I} \sin(|\varphi|)}{4\pi M} \quad (\text{B.67})$$

$$I_{D_{2a},rms}^2 = \frac{1}{2\pi} \left(\int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} (1 - d_{2a}) i^2 d\omega t + \int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} d_{3a} \cdot i^2 d\omega t \right) \quad (\text{B.68})$$

$$= \frac{\hat{I}^2}{24\pi M^2} \left(\sqrt{4M^2 - 1} (-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) + M^2 (-8 \cos(2\varphi)M + 12 \arcsin(\frac{1}{2M}) - 24M) \right)$$

$\varphi < \arcsin(1/(2M))$

$$I_{D_{2a},avg} = \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} (1 - d_{2a}) id\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} (1 - d_{2a}) id\omega t + \int_{\pi}^{\pi + \varphi} d_{3a} id\omega t \right) \quad (\text{B.69})$$

$$= \frac{-\hat{I}}{4\pi M} \left(\sqrt{4M^2 - 1} \cos(\varphi) - 4M + 4M^2 (\cos(\varphi) \arcsin(\frac{1}{2M}) + \sin(|\varphi|) - \cos(\varphi)|\varphi|) \right)$$

$$I_{D_{2a},rms}^2 = \frac{1}{2\pi} \left(\int_{\varphi}^{\arcsin(\frac{1}{2M})} (1 - d_{2a}) i^2 d\omega t + \int_{\pi - \arcsin(\frac{1}{2M})}^{\pi} (1 - d_{2a}) i^2 d\omega t + \int_{\pi}^{\pi + \varphi} d_{3a} i^2 d\omega t \right) \quad (\text{B.70})$$

$$= \frac{\hat{I}^2}{24\pi M^2} \left(\sqrt{4M^2 - 1} (-\cos(2\varphi) + 12M^2 + 4M^2 \cos(2\varphi)) - 8M^3 \cos(2\varphi) + 12M^2 \arcsin(\frac{1}{2M}) - 24M^3 \right)$$

For D_{3a} and D_{4a} :

$\pi - \arcsin(1/(2M)) < \varphi < \pi$

$$I_{D_{3a},avg} = \frac{1}{2\pi} \left(\int_{\pi}^{\pi + \arcsin(\frac{1}{2M})} (1 - d_{3a}) id\omega t + \int_{\pi + \arcsin(\frac{1}{2M})}^{2\pi - \arcsin(\frac{1}{2M})} d_{4a} id\omega t + \int_{2\pi - \arcsin(\frac{1}{2M})}^{\pi + \varphi} (1 - d_{3a}) id\omega t \right) \quad (\text{B.71})$$

$$= \frac{\hat{I}}{2\pi M} \left(-\sqrt{4M^2 - 1} \cos(\varphi) + M^2 (-4 \cos(\varphi) \cdot \arcsin(\frac{1}{2M}) + 2 \cos(\varphi)\pi + \sin(|\varphi|) - |\varphi| \cos(\varphi)) \right)$$

$$\begin{aligned}
I_{D3a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi}^{\pi+\arcsin(\frac{1}{2M})} (1-d_{3a})i^2 d\omega t + \int_{\pi+\arcsin(\frac{1}{2M})}^{2\pi-\arcsin(\frac{1}{2M})} d_{4a}i^2 d\omega t \right. \\
&\quad \left. + \int_{2\pi-\arcsin(\frac{1}{2M})}^{\pi+\varphi} (1-d_{3a})i^2 d\omega t \right) \\
&= \frac{\hat{I}^2}{12\pi M^2} \left(\sqrt{4M^2-1}(\cos(2\varphi)-12M^2-4M^2\cos(2\varphi)) \right. \\
&\quad \left. + 2M^2(-4\cos(\varphi)M-6\arcsin(\frac{1}{2M})+M\cos(2\varphi)+3M+3\pi) \right)
\end{aligned} \tag{B.72}$$

$$\arcsin(1/(2M)) < \varphi < \pi - \arcsin(1/(2M))$$

$$\begin{aligned}
I_{D3a,avg} &= \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{2M})}^{\pi+\varphi} d_{4a}id\omega t + \int_{\pi}^{\pi+\arcsin(\frac{1}{2M})} (1-d_{3a}) \cdot id\omega t \right) \\
&= \frac{-\hat{I}}{4\pi M} \left(\sqrt{4M^2-1}\cos(\varphi) + \sin(|\varphi|) - 4M \right. \\
&\quad \left. + 2M^2(2\cos(\varphi) \cdot \arcsin(\frac{1}{2M}) + \sin(|\varphi|) - |\varphi|\cos(\varphi)) \right)
\end{aligned} \tag{B.73}$$

$$\begin{aligned}
I_{D3a,rms}^2 &= \frac{1}{2\pi} \left(\int_{\pi+\arcsin(\frac{1}{2M})}^{\pi+\varphi} d_{4a}i^2 d\omega t + \int_{\pi}^{\pi+\arcsin(\frac{1}{2M})} (1-d_{3a}) \cdot i^2 d\omega t \right) \\
&= \frac{-\hat{I}^2}{24\pi M^2} \left(\sqrt{4M^2-1}(-\cos(2\varphi)+12M^2+4M^2\cos(2\varphi)) - \sin(|2\varphi|) \right. \\
&\quad \left. + M^2 \left(-12\varphi - 16\cos(\varphi)M + 12\arcsin(\frac{1}{2M}) \right) \right. \\
&\quad \left. + 6\sin(|2\varphi|) - 12M - 4M\cos(2\varphi) \right)
\end{aligned} \tag{B.74}$$

$$\varphi < \arcsin(1/(2M))$$

$$I_{D3a,avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} (1-d_{3a}) \cdot id\omega t = \frac{\hat{I}M}{2\pi} (\sin(|\varphi|) - \cos(\varphi)|\varphi|) \tag{B.75}$$

$$I_{D3a,rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} (1-d_{3a}) \cdot i^2 d\omega t = \frac{-\hat{I}^2 M}{6\pi} (4\cos(\varphi) - 3 - \cos(2\varphi)) \tag{B.76}$$

B.2.2 M < 1/2

For the case where the amplitude modulation factor is less than 1/2, we get a somewhat simpler set of formulas. The reason for treating this case explicitly, is that the formulas with integration limits including $\arcsin(1/(2M))$ no longer make any sense. This also means that Ta1+ (and Ta4-) always will be open and Ta4+ (and Ta1-) always will be closed. The integration limits are only shown for inductive load, but the general formulas will be the same.

For T_{1a+} and T_{4a-} :

$$I_{T_{1a+},avg} = 0 \quad (\text{B.77})$$

$$I_{T_{1a+},rms}^2 = 0 \quad (\text{B.78})$$

For T_{2a+} , T_{3a-} , D_{1a} and D_{6a} :

$$I_{T_{2a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi} d_{2a} \cdot id\omega t = \frac{\hat{I} \cdot M}{2\pi} (\sin(|\varphi|) + \cos(\varphi)\pi - \cos(\varphi)|\varphi|) \quad (\text{B.79})$$

$$I_{T_{2a+},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi} d_{2a} \cdot i^2 d\omega t = \frac{\hat{I}^2 \cdot M}{6\pi} (3 + \cos(2\varphi) + 4\cos(\varphi)) \quad (\text{B.80})$$

For T_{3a+} and T_{2a-} :

$$I_{T_{3a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi} id\omega t + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} d_{3a} \cdot id\omega t = \frac{\hat{I}}{2\pi} (2 - M \sin(|\varphi|) + M \cos(\varphi)|\varphi|) \quad (\text{B.81})$$

$$\begin{aligned} I_{T_{3a+},rms}^2 &= \frac{1}{2\pi} \int_{\varphi}^{\pi} i^2 d\omega t + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} d_{a3} \cdot i^2 d\omega t \\ &= \frac{\hat{I}^2}{12\pi} (3\pi + 8M \cos(\varphi) - 6M - 2M \cos(2\varphi)) \end{aligned} \quad (\text{B.82})$$

For T_{4a+} and T_{1a-} :

$$I_{T_{4a+},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} id\omega t = \frac{\hat{I}}{\pi} \quad (\text{B.83})$$

$$I_{T_{4a+},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} i^2 d\omega t = \frac{\hat{I}^2}{4} \quad (\text{B.84})$$

For D_{1a-} , D_{2a-} , D_{3a-} , D_{4a-} , D_{1a+} , D_{2a+} , D_{3a+} and D_{4a+} :

$$I_{D_{1a-},avg} = 0 \quad (\text{B.85})$$

$$I_{D_{1a-},rms}^2 = 0 \quad (\text{B.86})$$

For D_{1a} and D_{6a} :

$$I_{D_{1a},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi} d_{2a} \cdot id\omega t = \frac{\hat{I} M}{2\pi} (\sin(|\varphi|) + \cos(\varphi)\pi - \cos(\varphi)|\varphi|) \quad (\text{B.87})$$

$$I_{D_{1a},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi} d_{2a} \cdot i^2 d\omega t = \frac{\hat{I}^2 M}{6\pi} (3 + \cos(2\varphi) + 4\cos(\varphi)) \quad (\text{B.88})$$

For D_{2a} and D_{5a} :

$$I_{D_{2a},avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi} (1-d_{2a}) \cdot id\omega t + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} d_{3a} \cdot id\omega t \quad (B.89)$$

$$= \frac{\hat{I}}{2\pi} (-M \sin(|\varphi|) - M \cos(\varphi)\pi + 2 + 2M \cos(\varphi)|\varphi|)$$

$$I_{D_{2a},rms}^2 = \frac{1}{2\pi} \int_{\varphi}^{\pi} (1-d_{2a}) \cdot i^2 d\omega t + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} d_{3a} \cdot i^2 d\omega t \quad (B.90)$$

$$= \frac{\hat{I}^2}{12\pi} (3\pi - 12M - 4M \cos(2\varphi))$$

For D_{3a} and D_{4a} :

$$I_{D_{3a},avg} = \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} (1-d_{3a}) \cdot id\omega t = \frac{\hat{I} M}{2\pi} (\sin(|\varphi|) - M \cos(\varphi)|\varphi|) \quad (B.91)$$

$$I_{D_{3a},rms}^2 = \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} (1-d_{3a}) \cdot i^2 d\omega t = \frac{\hat{I}^2 M}{6\pi} (-4 \cos(\varphi) + 3 + \cos(2\varphi)) \quad (B.92)$$

B.2.3 Evaluation of the expressions

As for the 4-level topology, the expressions are evaluated in Saber. The verification are done in the modulation range $M = [0.2, 1]$ and $\varphi = [-150^\circ, 150^\circ]$, with a switching frequency at 1500Hz, and a load current of 100A_{RMS}. For the 5-level topology, the same simulation parameters as for the 4-level converter apply. Again, the worst deviations in % are for the freewheeling diode $i_{D_{1a}}$. The accuracy of the simulations are poor at this current level, and is the cause of this large deviation. At $M = 0.8$ and $\varphi = -45^\circ$, the calculated RMS and average currents are 0.219A and 0.006A respectively. The worst case in amperes is for the clamp diode $i_{D_{3a}}$ at $M = 0.6$ and $\varphi = 90^\circ$, where the deviation between simulated and calculated current value is 1.163 A for a load current of 100 A_{RMS}.

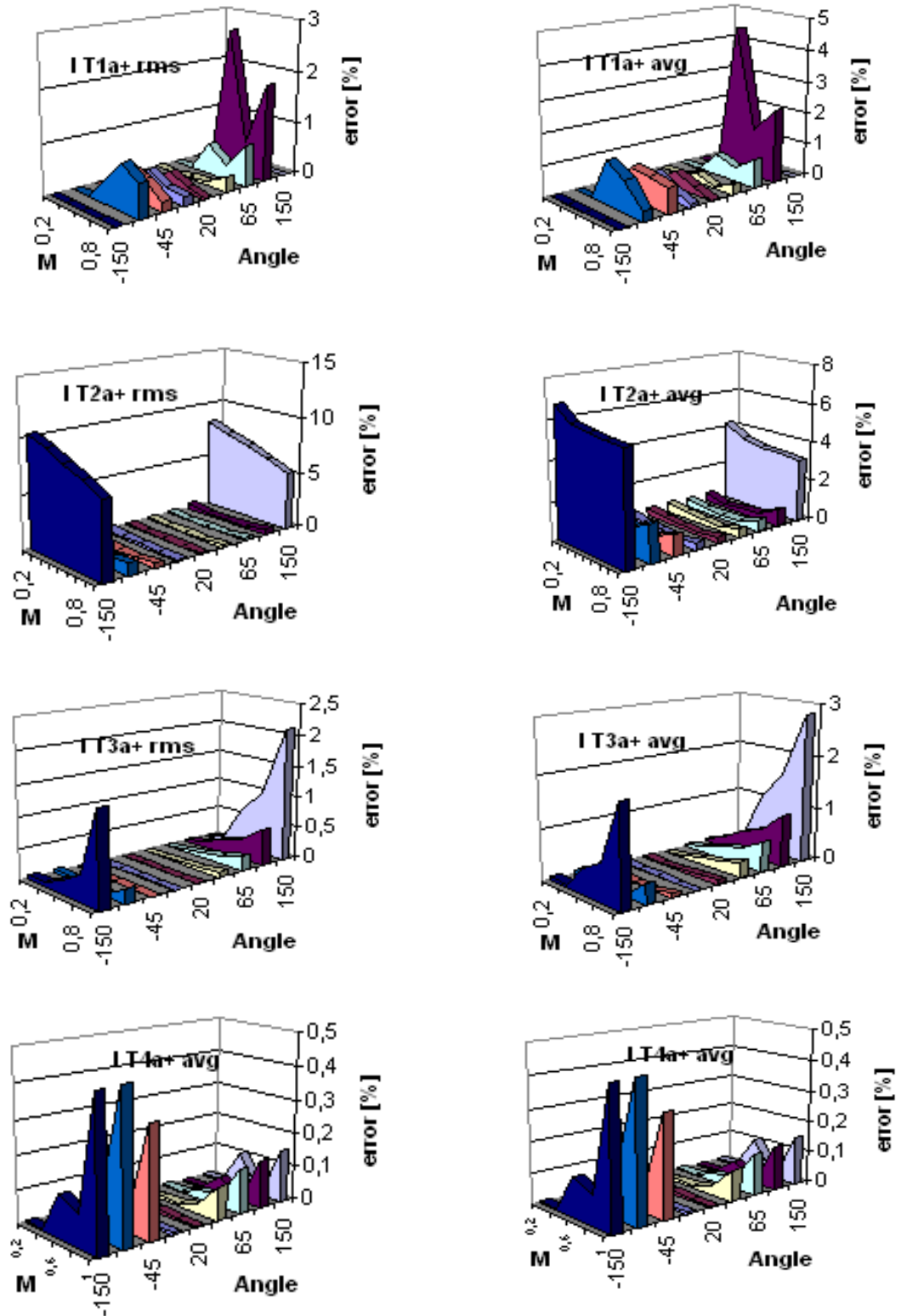


Figure B.1: Deviation in percent for currents through components in the 5-level converter.

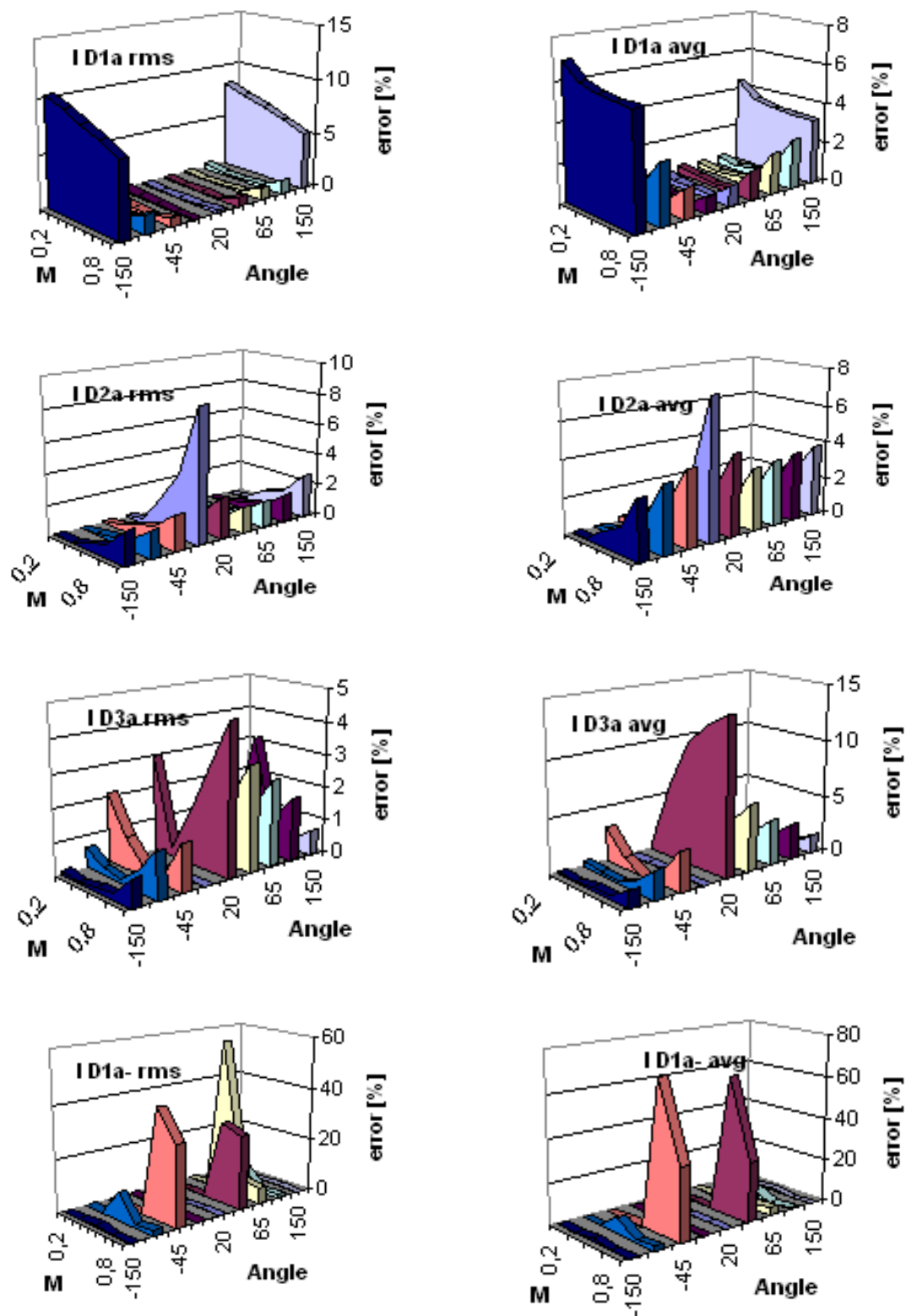


Figure B.2: Deviation in percent for currents through components in the 5-level converter (cont.).