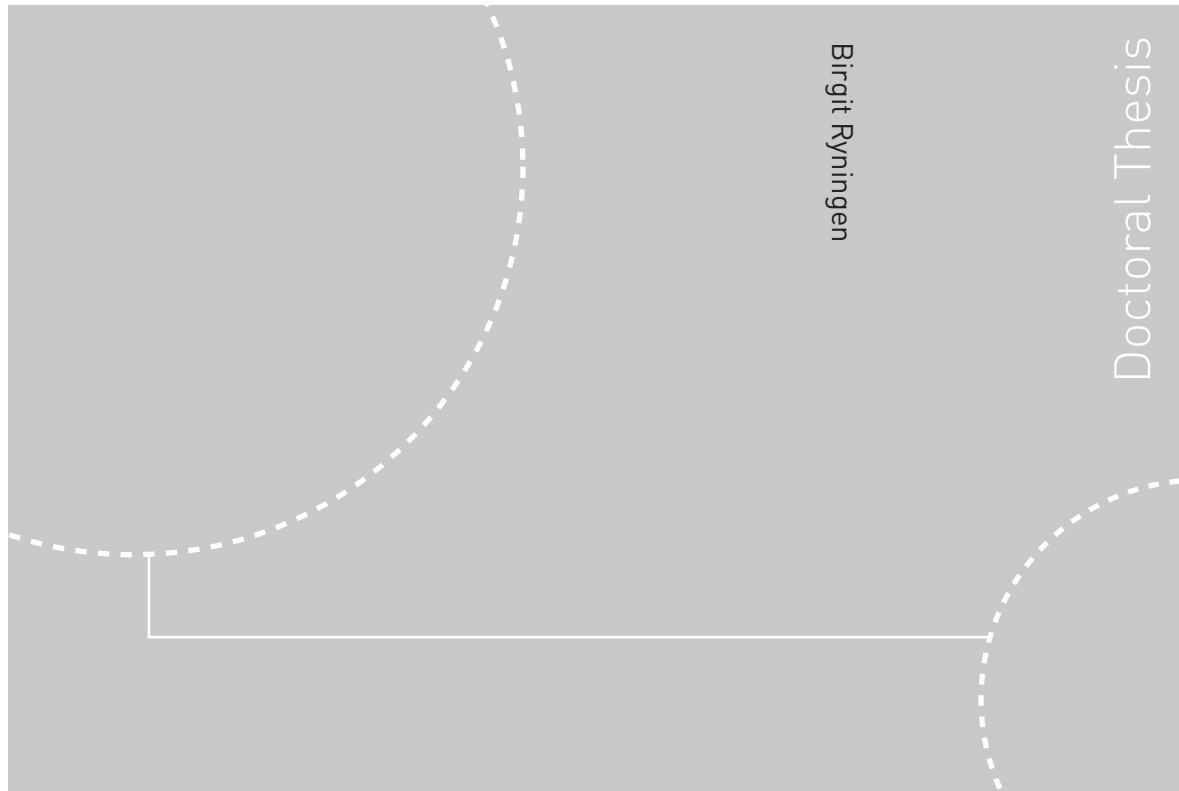


Doctoral Theses at NTNU, 2008:103

Birgit Ryningen

# Formation and growth of crystal defects in directionally solidified multicrystalline silicon for solar cells



Birgit Ryningen

Doctoral Thesis

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Norwegian University of  
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Thesis for the degree of  
philosophiae doctor  
Faculty of Natural Sciences and Technology  
Department of Materials Science and Engineering

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Thesis for the degree of philosophiae doctor

Trondheim, October 2008

Norwegian University of  
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## Preface

The work presented in this thesis has mainly been conducted at the Norwegian University of Science and Technology (NTNU) at the Department of Materials Science and Engineering. The thesis was completed in the period from September 2004 to May 2008 as a part of the research project *Crystalline Silicon Solar Cells – Cost Reduction* Sponsored by the Norwegian Research Council and partners (NTNU, SINTEF, IFE, Elkem Solar, REC and ScanWafer)

During 2006 I spent six months at the Research Center for Photovoltaic at the National Institute of Advanced Industrial Science and Technology (AIST) in Tsukuba, Japan. The stay was a cooperation between Elkem Solar and AIST. I have also had two stays (for three and one week, respectively) during 2007 at the Solar Cell Laboratory at Institute for Energy Technology (IFE) at Kjeller, Norway.

This thesis consists of two parts. Part one is an introduction where relevant theory is presented. The second part contains the results of the experimental work presented as articles already published or to be published and one project report. The following articles/report are included in this thesis:

- I. Birgit Rynningen, Kazi Saima Sultana, Elin Stubhaug, Otto Lohne and Paul Christian Hjemås, *DISLOCATION CLUSTERS IN MULTICRYSTALLINE SILICON*, 22<sup>nd</sup> European Photovoltaic Solar Energy Conference (EU PVSEC), Milan, Italia, 2007
- II. Birgit Rynningen, Otto Lohne and Michio Kondo, *CHARACTERISATION OF SOLAR GRADE (SoG) MULTICRYSTALLINE SILICON WAFERS MADE FROM METALLURGICALLY REFINED MATERIAL*, 22<sup>nd</sup> European Photovoltaic Solar Energy Conference (EU PVSEC), Milan, Italia, 2007
- III. Birgit Rynningen, Otto Lohne and Arve Holt, *Gettering of solar grade (SoG) multicrystalline silicon wafers made from metallurgical refined material*, report for the project *Silicon – Cost Reduction* (grant No. 153207) which is supported by the Norwegian Research Council and partners (NTNU, SINTEF, IFE, REC, ScanWafer and Elkem Solar).
- IV. Birgit Rynningen, Rannveig Kvande, Martin Bellmann and Otto Lohne, *The effect of crucible coating and the temperature profile on minority carrier lifetime in directionally solidified multicrystalline silicon ingots*, to be published
- V. Birgit Rynningen, Gaute Stokkan and Otto Lohne, *On the growth of dislocation clusters in directionally solidified multicrystalline silicon ingots by slip on the  $\{1\bar{1}0\} <110>$  slip systems*, to be published
- VI. Birgit Rynningen, Gaute Stokkan, Chiara Modanese and Otto Lohne, *Growth of dislocation clusters in directional solidified multicrystalline silicon*, 23<sup>rd</sup> European Photovoltaic Solar Energy Conference (EU PVSEC), Valencia, Spain, 2008



## Acknowledgements

Otto Lohne has been my supervisor through these years and I would like to thank him for all the drawings he has done at the black board in the *corner-room*, eagerly introducing me to the utterly complicated world of crystal structures. Thank you for always having time to discuss crystallography.

Lars Arnberg has been my co-supervisor and I will thank him for taking time to ask me of my progress and to read through everything I have written.

Rannveig Kvande and Gaute Stokkan have both been my office mates, and I have enjoyed their company in the office, in the lab and at social gatherings. It has been nice working with both of you, and it has been even nicer when we did not work.

Øyvind Mjøs was the one who introduced me to the laboratories at NTNU and to the theory of casting. Thank you for being patient and funny.

A cooperation between Elkem Solar AS and AIST gave me the opportunity to stay in Japan for half a year. Not only was I allowed to have a closer look at the photo voltaic research going on in Japan, but I was also given the chance to practice judo in the land of its origin. Thanks to Ragnar Tronstad and Christian Dethloff at Elkem Solar for giving me this chance and to Michio Kondo-san at AIST for welcoming me in his research group. Yoshiko Miyanuma-san took care of me during my stay, and she deserves a warm thanks. I had the pleasure to share office with Jan Ove Odden, Stefan Dewolf, Arno Smets and Chia-Wen Chang and I want to thank them not only for being my colleagues, but also for becoming my friends.

Hiroyuki Date-san and Svein Grandum at Elkem's office in Tokyo deserve great thanks for their generously welcome and their support.

Christina Roe Steen at the Human Resource Consultant at Elkem was in charge of all the practicalities concerning my stay in Japan. Her task turned out to be rather complicated, and I will thank her for being so nice and patient. Cathrine Bjerke Dalheim at KPMG had to help us out with the Japanese and Norwegian tax authorities, and I owe her my warm gratitude for not having to pay too much tax.

During both my stays at the Solar Cell Laboratory at IFE, Arve Holt took his time to help me conducting gettering experiments and making solar cells. Thank you for being so helpful. The others of the solar cell group at IFE also deserve thanks for being both cheerful and skilful, making it both nice and useful to visit their lab.

Thanks deserve also Paul Hjemås at REC ScanWafer in Glomfjord for providing silicon feedstock, wafers and red-zone material.

At NTNU and SINTEF there are many who deserves to be thanked: Morten Karlsen for conducting several EBSD-maps and for all the discussions on grain orientations, Birgitte Karlsen and Torild Krogstad for etching, Anne Lise Dons and Marissa di Sabatino for education on GDMS, Halvor Dalaker for helping me out with the solidification experiment

with the Elkem material, Aksel Alstad for help with 3D-drawings, Espen Olsen and Ragnar Fagerberg (project directing), Chiara Modanese (EBSD), Elin Stubhaug and Yanjun Li (TEM), Martin Bellman (modelling), Janne Siren Fjærestad (CDI), Kazi Sultana (dislocation counting), Kristine Narland, Eivind Øvrelid, Mohammad M'hamdi, Jarle Hjelen and Martin Syvertsen (discussions) and the lunch group for payday-lager and early morning rock-climbing.

The Judo group at NTNUI deserves a huge thanks and a shime waza for letting me get out my frustrations on them, and especially Vibeke, Lars, Jarle and Kim for always wanting to practice judo, also outside regular training hours. Double thanks to Lars, not only for the fighting, but also for reading through my thesis and for drinking a lot of coffee at *Stripa*. My Afghan judo-friends, especially Farhad and Shafiq, also deserve special thanks for giving me some perspective.

Thanks to Tone and Yngve for giving me lodging when I moved to Trondheim and for inviting me to several dinners after I moved out. I hope to make it up to you a little bit later.

My parents have always believed in me. Thank you for teaching me to read and write and for always encouraging me and telling me to focus. I could never have written anything if it were not for you. My sister and her big family also deserve a warm tank for not giving up on me despite all my travelling, training and working, and for always being there.

Anders has been patient and caring all the time, and he has even sometimes been interested in my work. Thank you for reading through everything; theory, articles, posters, reports... - but most of all; thank you for being there for me and for being who you are.

~

*You'll probably find that it suits your book  
to be a bit cleverer than you look.*

*Observe that the easiest method by far  
is to look a bit stupider than you are.*

- Piet Hein

## Summary of publications

Included in this thesis are five publications and one report. The common theme is characterisation of directionally solidified multicrystalline silicon for solar cells. Material characterisation of solar cell silicon is naturally closely linked to both the casting process and to the solar cell processing: Many of the material properties are determined by the casting process, and the solar cell processing will to some extent determine which properties will influence the solar cell performance.

Solar grade silicon (SoG-Si) made by metallurgical refining route and supplied by Elkem Solar was directionally solidified and subsequently characterised, and a simple solar cell process was applied. Except from some metallic co-precipitates in the top of the ingot, no abnormalities were found, and it is suggested that within the limits of the tests performed in this thesis, the casting and the solar cell processing, rather than the assumed higher impurity content, was the limiting factor.

It is suggested in this thesis that the main quality problem in multicrystalline silicon wafers is the existence of dislocation clusters covering large wafer areas. The clusters will reduce the effect of gettering and even if gettering could be performed successfully, the clusters will still reduce the minority carrier mobility and hence the solar cell performance. It has further been pointed out that ingots solidified under seemingly equal conditions might have a pronounced difference in minority carrier lifetime. Ingots with low minority carrier lifetime have high dislocation densities. The ingots with the substantially higher lifetime seem all to be dominated by twins. It is also found a link between a higher undercooling and the ingots dominated by twins. It is suggested that the two types of ingots are subject to different nucleation and crystal growth mechanisms: For the ingots dominated by dislocations, which are overrepresented, the crystal growth is randomly nucleated at the crucible bottom and the subsequent growth is governed by dislocations. For the other type of ingots which is dominated by twins and has a higher minority carrier lifetime, a higher undercooling has occurred before crystal nucleation. It is suggested that this undercooling can reach the critical value for dendritic nucleation to occur (10 K). After dendritic nucleation, subsequent crystal growth is dominated by twins.

Nucleation and multiplication mechanisms for dislocations are complex, and investigations on a microscopic scale have been performed. Mechanisms such as punch-out from precipitates with a thermal expansion coefficient different from that of the silicon matrix, intergranular – and intragranular hardening and development of strain fields due to differences in the elasticity module between different grains are thought to play a role in the nucleation of dislocations higher up in the cast. The multiplication has been explained by a macroscopic stress field at the solidification front, stresses developed during cooling and pinning by oxygen impurities.

For dislocations nucleated by an angular grain boundary a multiplication and growth mechanism is proposed where dislocations can cross slip and line up at certain crystallographic directions during crystal growth.





## Definition of brackets used for crystal orientations

Crystallographic directions and planes are distinguished by use of a standard bracket notation. The brackets used and their definitions are given in Table A.

**Table A: The brackets used for crystal orientations and their definitions**

<b>Brackets</b>	<b>Definition</b>
[ ]	Directions
< >	Equivalent directions
( )	Planes
{ }	Equivalent planes

---

# Content

<b>1</b>	<b>Introduction .....</b>	<b>3</b>
1.1	Solar cells .....	3
1.2	Outline of the thesis.....	4
1.2.1	Microstructures in silicon for solar cells .....	5
1.2.2	Raw material .....	5
1.2.3	Sample preparation.....	5
<b>2</b>	<b>Feedstock.....</b>	<b>7</b>
2.1	Purification of MG-Si.....	7
2.1.1	The Siemens process .....	7
2.1.2	Fluidised bed .....	9
2.1.3	Purification via casting.....	10
2.1.3.1	Impurity distribution in directionally solidified ingots .....	10
2.1.4	Metallurgical refining route .....	12
2.1.5	Direct metallurgical route.....	12
2.1.6	Chemical refining route.....	13
2.1.7	Electrolysis .....	14
2.2	Recycling.....	14
2.3	A wafer-manufacturer's challenges .....	16
<b>3</b>	<b>Multicrystalline silicon.....</b>	<b>17</b>
3.1	Crystal structures.....	17
3.2	Directional solidification.....	17
3.2.1	Crystal growth mechanisms .....	18
3.3	Defects.....	22
3.3.1	Point defects .....	22
3.3.2	Grain boundaries .....	22
3.3.2.1	Deformation twins.....	23
3.3.3	Precipitates .....	24
<b>4</b>	<b>Dislocations .....</b>	<b>25</b>
4.1	Structure .....	25
4.2	Nucleation of dislocations.....	26
4.2.1	Nucleation of dislocations at stress concentrators.....	26
4.2.2	Nucleation of dislocations at grain boundaries .....	26
4.2.2.1	Thermal expansion coefficients and elasticity modules.....	26
4.2.2.2	Intragranular- and intergranular hardening .....	27
4.2.2.3	Grain boundaries .....	27
4.3	Dislocation mobility.....	27
4.3.1	Glide .....	28
4.3.1.1	Cross slip.....	30
4.3.2	Climb.....	30
4.3.3	Impurity effects on dislocation motion .....	31
4.3.4	Image forces .....	32
4.4	Dislocation multiplication.....	32
4.4.1	Multiplication by Frank-Read sources .....	32
4.4.2	Multiplication by multiple cross glide .....	34

4.4.3	Multiplication by Bardeen-Herring sources.....	34
<b>5</b>	<b>Detection of dislocations in silicon .....</b>	<b>35</b>
5.1	Detection of dislocations by surface methods.....	35
5.1.1	The HF:HNO <sub>3</sub> -system.....	36
5.1.2	The HF:CrO <sub>3</sub> -system.....	36
5.1.3	Sample preparation by polishing and Sopori etching.....	36
5.1.4	Detection of dislocations by PVScan.....	38
<b>6</b>	<b>Recombination and trapping.....</b>	<b>41</b>
6.1	Recombination .....	41
6.1.1	Shockley-Read-Hall (SRH) recombination.....	42
6.1.2	Recombination activity of contaminated dislocations in silicon.....	43
6.1.3	Trapping .....	46
6.2	Measuring minority carrier lifetime .....	46
6.2.1	Quasi Steady State Photo Conductance (QSSPC).....	47
6.2.2	Microwave Photo Conductance Decay ( $\mu$ -PCD).....	48
6.2.3	Carrier Density Imaging (CDI) .....	48
<b>7</b>	<b>Conclusions of the publications.....</b>	<b>49</b>
7.1	Casting.....	49
7.2	Characterisation of SoG-Si multicrystalline wafers made from metallurgically refined material .....	49
7.3	Dislocation clusters .....	49
<b>8</b>	<b>Suggestions for further work .....</b>	<b>51</b>
8.1	Characterisation of SoG-Si.....	51
8.2	Dislocation clusters .....	51
	<b>References .....</b>	<b>53</b>

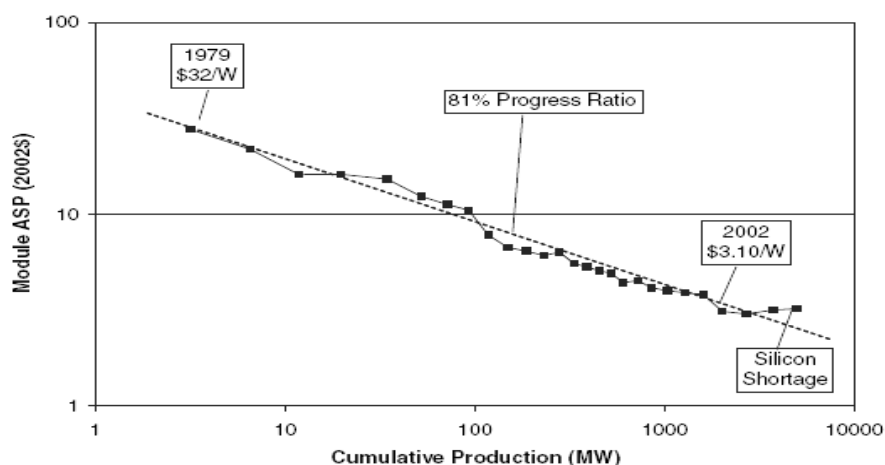
# 1 Introduction

## 1.1 Solar cells

The photovoltaic industry has grown fast in the recent years, and has experienced 5 years of over 40% annual growth in module production [1]. Several milestones for the industry's growth are summarised in [1]:

- In 2000, the total accumulated module production since the beginning of the industry surpassed  $1\text{GW}_{\text{peak}}$  ( $\text{GW}_{\text{p}}^{\text{i}}$ ). With an optimistic estimate of 2000 hours of sunshine a year, the resulting penergy output is 2 TWh.
- In 2003, the photovoltaic industry processed more square metres of silicon wafers than the microelectronics industry. Less silicon was used, however, because solar cell wafers are thinner than standard integrated circuit wafers.
- By 2004, the industry was producing over  $1\text{GW}_{\text{p}}$  per year.
- In 2006, the world solar cell production reached  $2.2\text{GW}_{\text{p}}$  and the world solar photovoltaic (PV) market installations was  $1.7\text{GW}_{\text{p}}$  [2].
- The European goal for the PV industry is to decrease the module cost to  $1\text{€}/\text{W}_{\text{p}}$  and to have  $3\text{GW}_{\text{p}}$  installed by 2010 [3].

At the time of birth for the terrestrial photovoltaic industry in the mid-1970s, the conventional assumption was that crystalline silicon solar cells, which were descended from space solar cells, were too expensive as a terrestrial energy source. Thin film solar cells were expected to emerge and to dominate the market. In fact, crystalline silicon solar cells were quite expensive and the module price in 1978 was around  $\$70/\text{W}$  in current US-dollars [1]. Today, 30 years later, crystalline silicon still dominates the marked, being responsible for 91% of the power module market (95% when including ribbon silicon) [4]. Due to the current feedstock shortage, however, the cost might not be reduced as fast or as much as expected (see Figure 1), and other technologies might thus get the chance to develop and to decrease the crystalline silicon domination in the photovoltaic marked [5].



**Figure 1: Historical plot of module price. Data are from Strategies Unlimited and Navigant Consulting. All prices are corrected to 2002 US dollars [1].**

<sup>i</sup> Watt peak stands for peak power at Standard Test Conditions (STC); that is the output power achieved by a module under solar radiation of  $1000\text{Wm}^{-2}$  at  $25^{\circ}\text{C}$  ambient temperature and Air Mass 1.5 spectrum (AM 1.5).

## 1.2 Outline of the thesis

Due to the raw material shortage, alternative raw material supplies are entering the silicon market, and the solar industry is confronted with new challenges: New impurities might be present and the feedstock might be available in other forms and shapes than today. This variety in raw material needs to be considered in the future, and a solar grade standard defining impurity limits for different casting and solar cell processes would make life easier for the solar cell manufacturers.

As the raw material supply is changing, the drive for higher efficiencies and lower cost are constantly present. The European Union (EU) has a declared goal to increase the efficiency of solar cells from about 15% to 20% by the year 2010 for multicrystalline silicon cells and to 22% efficiency for monocrystalline silicon cells [3]. Hence, there is a need for a deeper understanding of how different silicon feedstock qualities are affecting the efficiency of the solar cell.

An overview over the EU's roadmap to 2030 for silicon and PV research is given in Table 1. As can be seen, emphasis is given to new feedstock and defect research.

**Table 1: EU's roadmap to 2030 for silicon and PV research [6]**

Materials	2008 - 2013	2013 - 2020	2020 - 2030 and beyond
Industry manufacturing aspects	<ul style="list-style-type: none"> <li>■ <b>Polysilicon targets</b> Consumption 5 g/W<sub>p</sub> Cost 15-25 €/kg (dependent on quality) Wafer thickness &lt;150 μm</li> <li>■ <b>Critical issues</b> Si availability</li> </ul>	<ul style="list-style-type: none"> <li>■ <b>Polysilicon targets</b> Consumption &lt;3 g/W<sub>p</sub> Cost 13-20 €/kg (dependent on quality) Wafer thickness &lt;120 μm</li> </ul>	<ul style="list-style-type: none"> <li>■ <b>Polysilicon targets</b> Consumption &lt;2 g/W<sub>p</sub> Cost &lt; 10-15 €/kg (dependent on quality) Wafer thickness &lt;100 μm</li> </ul>
Applied/advanced technology aspects	<ul style="list-style-type: none"> <li>■ New Si feedstock</li> <li>■ Improved crystal growth</li> <li>■ Reusable crucibles which introduce only small amounts of impurities into the silicon</li> <li>■ Low kerf loss sawing</li> <li>■ Fracture mechanics of thin wafers</li> <li>■ Metal pastes suited for thin wafers</li> <li>■ Low-cost encapsulants</li> <li>■ New frames and supporting structures</li> <li>■ Recycling</li> <li>■ Low-impact manufacturing</li> <li>■ Safe processes</li> </ul>	<ul style="list-style-type: none"> <li>■ New Si feedstock</li> <li>■ Low defect (high electronic quality) silicon wafers</li> <li>■ Improved wafering</li> <li>■ Wafer equivalents</li> <li>■ Improved encapsulants</li> <li>■ Avoidance of hazardous materials</li> <li>■ Safe processes</li> <li>■ Conductive adhesives or other solder free solutions for module interconnection</li> </ul>	<ul style="list-style-type: none"> <li>■ New Si feedstock</li> <li>■ Low defect (high electronic quality) silicon wafers</li> <li>■ Improved wafering</li> <li>■ Wafer equivalents</li> <li>■ New encapsulants</li> <li>■ Safe processes</li> </ul>
Basic research and fundamentals	<ul style="list-style-type: none"> <li>■ Defect characterisation and control in silicon</li> <li>■ New feedstock technologies</li> <li>■ Advanced wafering technologies</li> <li>■ Wafer equivalent technologies</li> </ul>	<ul style="list-style-type: none"> <li>■ Defect control in silicon</li> <li>■ New feedstock technologies</li> <li>■ Novel wafering technologies</li> <li>■ Wafer equivalent technologies</li> <li>■ New materials for metal contacts</li> <li>■ New encapsulants</li> </ul>	<ul style="list-style-type: none"> <li>■ Wafer equivalent technologies</li> <li>■ New materials for metal contacts and cell/module manufacture</li> <li>■ New encapsulants</li> </ul>

### 1.2.1 Microstructures in silicon for solar cells

Localised regions with high dislocation densities are known to be rather detrimental for solar cell performance [7], [8]. Sopori et al. (2005) claim an efficiency loss due to defect clusters in solar cells of more than 3-4 absolute percent points [9].

Many mechanisms are correlated with the dislocation clusters: They may act as precipitation sites for metal impurities, which will further decrease the minority carrier lifetime close to a dislocation [10]. The metal precipitates formed at dislocation sites will not, in contrast to dissolved metal impurities, be affected by the standard gettering processes in the solar cell production (phosphorous diffusion and aluminium alloying) [11], [12]. Dislocations may on the other hand act as internal gettering sites during cooling, and thus have a positive effect on the overall minority carrier lifetime [13], but when dislocations are clustered in large numbers over large areas, the lifetime will be severely reduced in these areas.

Dislocations in general and especially dislocation clusters as well as precipitates are the main focus areas in this thesis. The aim has been to get an overview of the dislocation cluster and precipitate distribution, and to suggest some sources for the dislocation cluster formation. Commercially available wafers and wafers from ingots made in the Crystalox DS 250 pilot scale furnace at The Norwegian University of Science and Technology (NTNU) were used for the investigations.

### 1.2.2 Raw material

Elkem Solar AS is one of the companies that have entered the solar grade silicon (SoG-Si) market. They have developed a metallurgical refining route to obtain SoG-Si. There have already been reported cell efficiencies in solar cells made from this material that equal the level of commercial cells [14], [15], [16], and more than 18 % efficiency in a cell produced in a high efficiency solar cell process line [17]. Thin film silicon solar cells on Elkem Solar SoG-Si substrates are also reported with good results [18]. Even though Elkem Solar has reported satisfactory efficiency in cells made from their material, it is desirable to investigate the material further. The cell efficiency is dependent on microstructure (grain boundaries, crystal orientation, dislocations etc) and chemical composition (impurities, doping, gettering etc). It is however still not entirely understood how all these effects interact with each other. It is not either known which is (are) the most important efficiency limiting parameter(s) in Elkem Solar's SoG-material.

A multicrystalline ingot made out of 100 % SoG-silicon supplied by Elkem Solar was cast in the Crystalox pilot furnace, and wafers from this ingot were used for the investigations.

### 1.2.3 Sample preparation

Due to the newly established characterisation and preparation laboratory at NTNU, the contributions to develop routines at the lab, such as polishing and etching, are part of the work done in connection with this thesis. A new method for measuring the liquid/solid interface during crystal growth and another to study inclusions by scanning electron microscope (SEM) on polished, but not etched wafers were also developed.

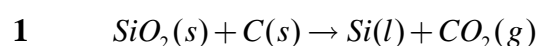




## 2 Feedstock

Silicon is one of the most abundant elements on earth, and silicon bound to oxygen makes up 75 % of the Earth's crust [19]. It exists, among other rock types, in quartz as silicon dioxide.

Metallurgical grade (MG) silicon is produced by carbothermic reduction of quartz in melting plants in the metallurgical industry, as roughly described in equation 1. The product consists of 98-99% silicon and about 1-2% of impurities which are mainly iron, aluminium, phosphorus, calcium, titanium, carbon and boron. The consumption of electric energy is 11-13 kWh/kg produced MG-Si [20].

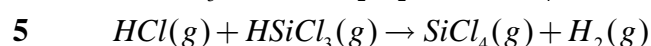
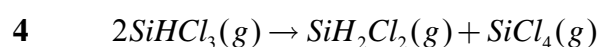
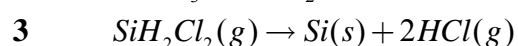
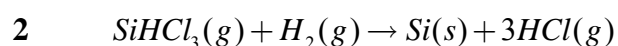


### 2.1 Purification of MG-Si

Traditionally, MG-Si has been purified by the Siemens process which gives electronic grade (EG) silicon called polycrystalline silicon, or just polysilicon, and has a purity of 99,9999999%. After purifying, ultra pure monocrystalline silicon is obtained by a Czochralski (Cz) crystal pulling process or by float zone (FZ). The top and bottom of the silicon crystal (called tops and tails) contain small amounts of impurities and dislocations and are therefore cut off. This cut-off and polysilicon which is not pure enough for the electronic industry goes to the solar industry, and up to about year 2002, this was enough to cover the material need for the solar cell industry. After 2002, however, the demand for feedstock surpassed the supply. This has led to a silicon shortage and a price increase as shown in Figure 1. In the following, the Siemens process and some alternative purification methods will be introduced.

#### 2.1.1 The Siemens process

In the Siemens process, silgrain (>99.6 % purity) is used [21]. Silgrain is then reacted with hydrochloric acid in the presence of a copper catalyst. The main product obtained is trichlorosilane ( $\text{SiHCl}_3$ ), which is purified through fractional distillation. The separated  $\text{SiHCl}_3$  is decomposed and reduced at high temperature ( $T > 1000^\circ\text{C}$ ) on high-purity silicon rods, as described in equation 2 and 3. By-products are formed as shown in the equations 4 and 5. For each mole Si converted to polysilicon, 3 to 4 moles of  $\text{SiCl}_4$  is produced, binding large amounts of chlorine and valuable silicon [22]. A sketch of the Siemens reactor is given in Figure 2. The resulting polysilicon has typically an impurity level of  $10^{-9}$ .



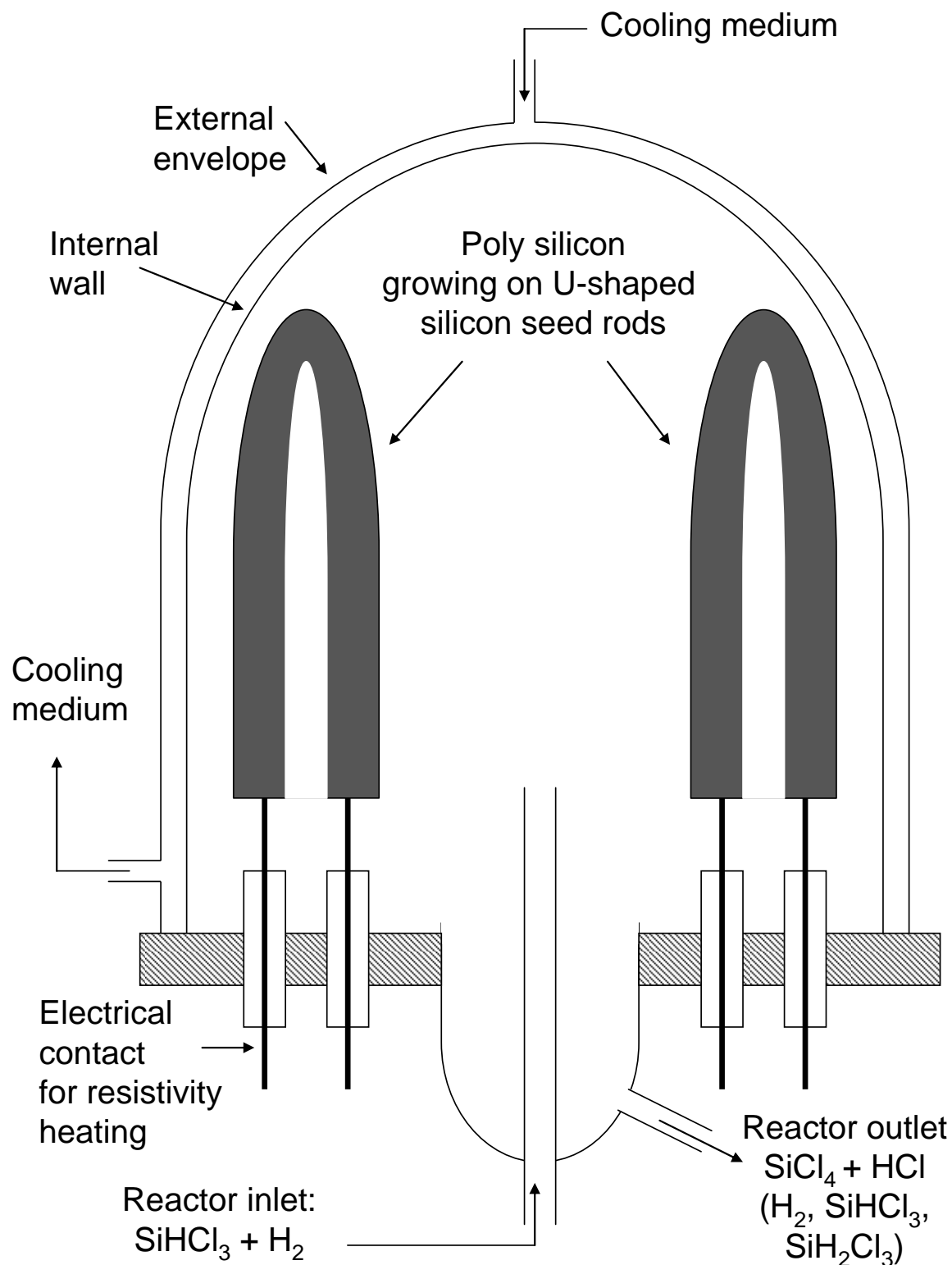
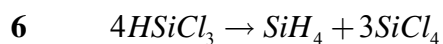


Figure 2: A sketch of a Siemens reactor used to produce polysilicon

The Siemens process is highly energy consuming (120-160 kWh/kg produced polysilicon [23]). To avoid deposition on the inner surface of the reactor chamber, this has to be cooled.

### 2.1.2 Fluidised bed

The raw material for the fluidised bed reaction [24] is silane which can be prepared by the reaction of magnesium silicide ( $Mg_2Si$ ) with acids or by boiling trichlorosilane on a bed containing a catalyst. This reaction produces silane and silicon tetrachloride according to equation 6. The most commonly used catalysts for this process are metal halides, particularly aluminium chloride.



A schematic presentation of silane decomposition in a fluidised bed reactor is shown in Figure 3. Preheated silane and hydrogen gas enter at the bottom of the reactor. When silane gas is further heated by the heated reactor walls, it thermally decomposes to solid silicon and hydrogen gas. Most of the solid silicon deposits on the surface of particles in the reactor, causing the particles to grow.

The hydrogen gas and some entrained silicon powder exit the top of the reactor. During continuous production, silicon product will be removed from the reactor to ensure mass balance while seed particles will be added or generated to ensure constant average particle size.

The fluidised bed reactor is governed by the overall reaction, given in equation 7.

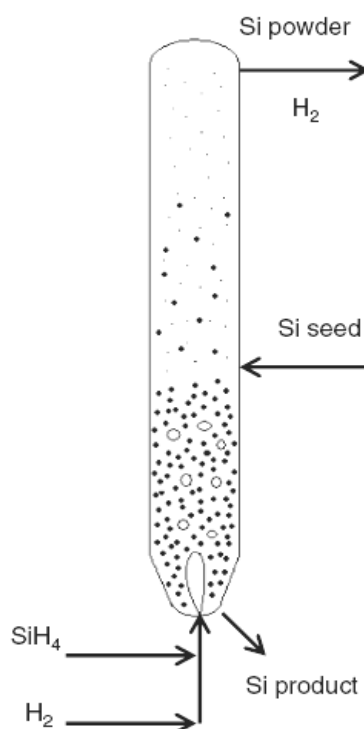
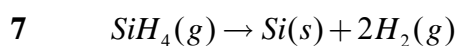


Figure 3: Sketch of a fluidised bed reactor [25].

### 2.1.3 Purification via casting

Because of the low segregation coefficient (often less than  $10^{-5}$ ) for most impurities in silicon, solidification is a well known and frequently used purifying process. The purification can be done by means of Czochralski crystal pulling, float zone melting or by directional solidification [26], [27].

Crystal pulling as well as zone melting are very effective purification methods, but are also extremely expensive and require at least double purification of the metallurgical grade silicon before satisfactory solar cell quality is obtained. Two of the impurities which are not removed by directional solidification is the common doping elements boron and phosphorous with segregation coefficients 0.8 and 0.35, respectively [28], [29]. Another important impurity not removed by directional solidification is oxygen. These will thus largely remain in the bulk of the ingot after directional solidification and must be removed by other means.

A typical example of an impurity distribution is given in Figure 4.

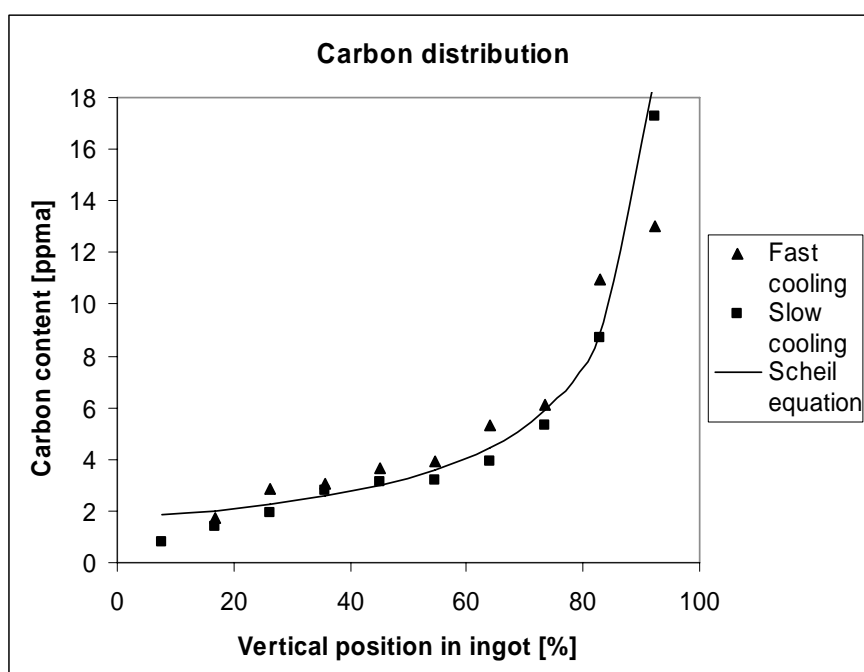


Figure 4: The carbon distribution in a directionally solidified multicrystalline ingot measured and calculated by Scheil's equation [30] using a distribution coefficient of 0.058 [31]. 100% represents the top of the ingot.

#### 2.1.3.1 Impurity distribution in directionally solidified ingots

Due to the fact that most elements are more soluble in liquid than in solid silicon, impurities dissolved in the melt will segregate and the element concentration in the ingot will in most cases increase upwards in the ingot following Scheil's equation [32] when the melt solidifies from the bottom and up; see equation 8. The exponential distribution will create a heavily contaminated thin layer at the top of the resulting ingot; see Figure 4 for an example of a typical distribution.

$$8 \quad C_s^* = kC_0(1 - f_s)^{(k-1)}$$

where

$C_s^*$ : Is the solid composition at the solid/liquid interface

$k$ : Equilibrium distribution coefficient

$C_0$ : Starting composition

$f_s$ : The fraction of solid

The Scheil equation assumes no diffusion in the solid state, complete mixing in the liquid state and equilibrium at the solid/liquid interface. If convection is not sufficient to provide complete mixing in the liquid phase, solute atoms are rejected by the advancing solid at a greater rate than they can diffuse into the bulk of the melt. A concentration gradient is thus developed ahead of the solid. This enriched region will determine the rate of solute incorporation into the solid front. This region is called a diffusion boundary layer and is denoted  $\delta$ . Scheil's equation can still be used if an effective distribution coefficient,  $k_{eff}$ , given by equation 9 and 10 [33], [34] is used instead of the equilibrium coefficient. Here,  $v$  is the growth velocity and  $D$  is the diffusion coefficient of the impurity element in the liquid.

$$9 \quad k_{eff} = \frac{k}{k + (1 - k)e^{-\Delta}}$$

$$10 \quad \Delta = \frac{v\delta}{D}$$

Precipitates may form after saturation is met, and Scheil's equation will no longer be valid. The amount of super saturation needed for precipitates to form will vary with the chemical composition and the growth conditions in the system.

In addition to the Scheil distribution the impurity distribution will depend on diffusion. Impurities will diffuse into the solidified silicon from the crucible walls and bottom as well as from the coating. Back-diffusion can also occur as impurities diffuse from the heavily contaminated top layer back into the bulk material after solidification, or from the boundary layer during solidification. Both in-diffusion from the crucible and coating and back-diffusion are temperature dependent and the impurity distribution varies with varying temperature profile during growth and the subsequent cooling.

Boron is an acceptor in silicon, and multicrystalline silicon ingots made by directional solidification are often pre-doped with boron. A small amount of boron is added together with the feedstock prior to melting and solidification. Boron is most commonly used because it is the doping element with the distribution coefficient closest to 1 ( $k_0 = 0.8$  [29]). The distribution profile will thus not vary as much with height as the other doping elements.

### 2.1.4 Metallurgical refining route

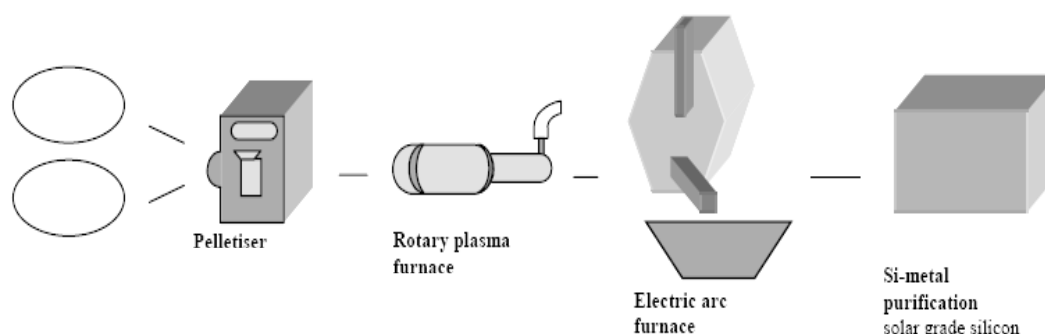
Elkem Solar AS has developed a metallurgical refining route. This route is now being up-scaled to industrial scale and is assumed to be more cost effective and less energy consuming than the traditional route. According to Peter et al. (2005) [15], the energy consumption for the future metallurgical refining plant is calculated to be in the range of 25-30 kWh/kg and the energy payback time will thus be reduced.

Information about details in the process and the impurity content in the final SoG-Si is not available, but an overview of the main steps in the refining process is given here:

Adding calcium-containing compounds to MG-Si melt with subsequently repeated directional solidifications [35] or with subsequent leaching [36], [37] are two known purifying methods. Elkem Solar's metallurgical route is based on the last of the two and on their latest patent on the topic [38]: A calcium-containing compound in a small amount is added to molten silicon. The silicon is cast at a relatively high cooling rate and the solidified silicon is crushed and thereafter purified by two leaching steps. In the first leaching step the silicon is treated with an aqueous solution of  $\text{FeCl}_3$  or  $\text{FeCl}_3$  and  $\text{HCl}$  which causes disintegration of the silicon, and in the second leaching step the silicon is treated with an aqueous solution of  $\text{HF}$  or  $\text{HF}$  and  $\text{HNO}_3$ . This process will prominently reduce impurities such as Fe, Al, Ti, P and to some extent B. Calcium is present as a potential impurity during this process, the final SoG-Si is however reported to contain very little calcium [38].

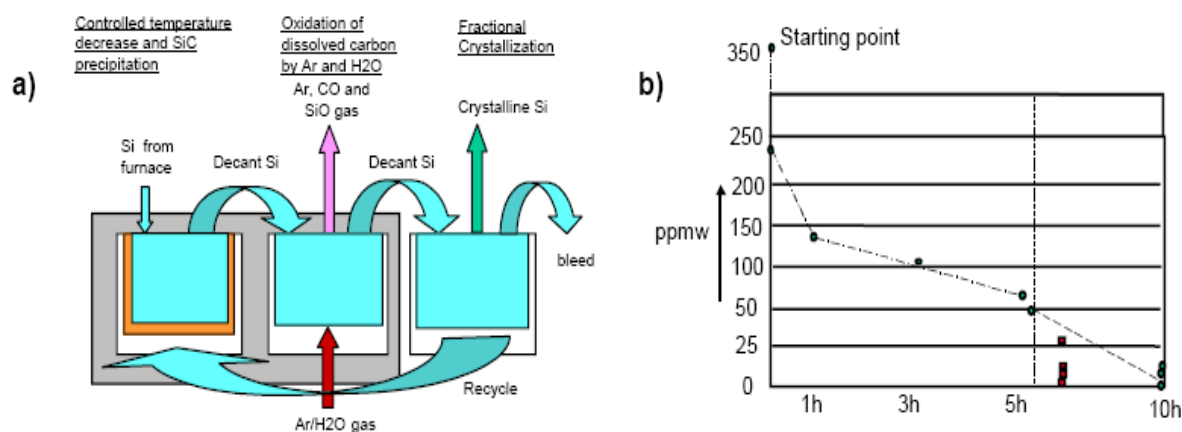
### 2.1.5 Direct metallurgical route

An alternative approach to the purification of MG-Si is to use high-purity raw materials in the carbotermic reduction process, that is, ultra pure quartz and ultra pure carbon, and thus obtain SoG-Si more directly. The purity of the raw materials will greatly reduce the requirements on purification of the silicon. Sintef and the Energy research Centre of the Netherlands (ECN) have developed a process, called Solsilc, based on high purity quartz and high purity carbon black. This process is today being industrialised by Fesil Sunergy. A schematic presentation of the Solsilc process is given in Figure 5 and the subsequent carbon removal step and results are given in Figure 6.



**Figure 5: Schematic process sequence of production of SoG-Si by the Solsilc process [39]**

Due to the fact that the high purity raw materials come in powdered form, the process starts with a pelletizing step. The next two steps (production of SiC in a rotary plasma furnace [40] and production of Si from the SiC in a submerged arc furnace [20]) replaces a single step in the MG-Si production where both steps are performed simultaneously in a submerged arc furnace [41].



**Figure 6: a) Process for carbon removal applied after the Solsilc process and b) the results from carbon removal [39]**

The liquid silicon which is produced by carbothermic reduction at high temperature (up to 2000 °C) contains a high concentration of dissolved carbon, usually several hundred ppm [39]. Virtually all of this carbon has to be removed to make the Si suitable for ingot production. Figure 6 shows the approach to carbon removal in the Solsilc process. First, during a controlled cooling, the excess carbon is precipitated as SiC and separated by filtration. This results in Si saturated with carbon at the melting point (~70 ppm<sub>w</sub>, according to [39]). Next, by an oxidative melt treatment followed by solidification, the carbon is reduced to less than 5 ppm<sub>w</sub>. Figure 6 b) shows the results. Typical carbon concentrations which have been obtained in the final SoG-Si are ≤3 ppm<sub>w</sub> with a yield of the silicon of 70 %.

The Si produced via the Solsilc route is meant to be suitable as feedstock for directional solidification or Cz-growth. The resulting carbon content that originates from the quartz and carbon black can be up to the 1-10 ppm level, whereas the limits allowed in polysilicon feedstock are around the 1 ppb level or lower. Hence, the segregation of contaminants to the liquid phase which occurs during directional solidification is essential in order to produce solar grade ingots.

### 2.1.6 Chemical refining route

The principle of reducing silicon tetrachloride by zinc in order to produce SoG-Si has earlier been investigated (for example [42], [43], [44]), but has not been commercialised.

A recent cooperation between Hydro Solar and Umicore, called HyCore, has however resulted in a process based on zinc reduction (Figure 7) which is going to be commercialised by 2010. Two pilot scale plants are at the present running in Belgium, and a third is currently being built at Herøya, Norway. The last pilot is planned to be operational during this year (2008), and the first industrial step, with 1200 tons installed capacity, is planned in operation by 2010. The product is SoG-Si with sufficient purity for monocrystalline pulling, which is 99.999% Si [45].

An important step in the HyCore process is the electrolysis of the by-product ZnCl<sub>2</sub> which is recycled in the process.



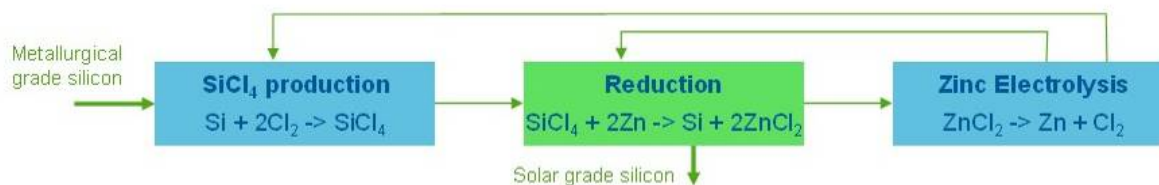


Figure 7: A sketch showing the HyCore process with reduction of silicon tetrachloride gas by zinc [45]

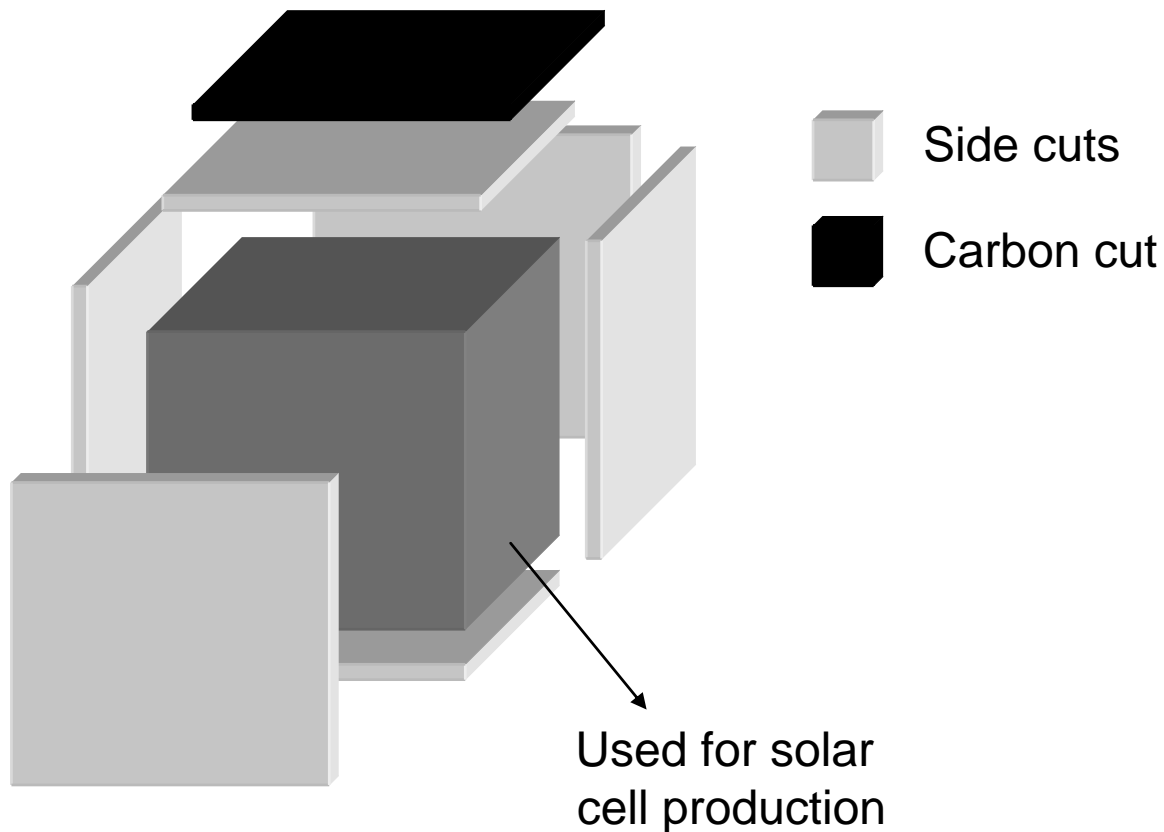
### 2.1.7 Electrolysis

Electrolysis is yet another approach. It has been the standard production method to produce aluminium for more than 100 years and silicon can also be produced by electrolysis. One electrolyse process has been patented by Stubergh (1994) [46]. The process is based on the dissolution of quartz in a fluoride-containing bath at 1000 °C, and decomposition of the quartz into silicon and oxygen. Silicon precipitates at the electrode. Afterwards, the silicon is crushed and cleaned with acid. In order to obtain a clean product, the silicon is melted and thereafter crystallised into ingots for subsequent sawing into wafers. The slag that comes with the silicon from the electrolyte has a high solubility for impurities and can be separated from the silicon. The process has been scaled up to a larger laboratory scale. The work is partly done in cooperation with SINTEF and Institute for Energy Technology (IFE). A company called “Norwegian Silicon Refinery” has been established [47] and they are currently looking for finances to build a pilot plant [48].

## 2.2 Recycling

Approximately 30% of the silicon used to grow a multicrystalline ingot ends up as solar cells [47]. It is therefore important to recycle the off cuts, failed runs, broken wafers and even kerf [49].

After directional solidification, a carbide cut and side-, top- and bottom-cuts, are removed before the ingot is wafered, see Figure 8. The carbide cut is the very top of the ingot with high impurity content due to segregation. The side, top and bottom cuts are removed due to contamination from the crucible walls and coating as well as from the carbide cut layer. The carbide cut is considered waste, but the side cuts together with broken wafers can be recycled by relatively simple means.



**Figure 8:** After directional solidification, carbon cut and side cuts are removed from the ingot. Only the middle part is used for solar cell processing.

The kerf loss during subsequent wafering depends on wire thickness, carbide particle size and wafer thickness, but can in the worst cases be as much as 50%. A European project called *Recycling of Silicon rejects from PV production Cycle* (RE-Si-CLE) was initiated in 1999 with the main objective to demonstrate new technologies allowing for recycling of 75% of the silicon rejects in exhausted wire cutting slurries after the slicing of silicon wafers [50]. The results from this project are not available, but some main process steps investigated are [50], [51]:

- Mechanical separation of SiC and liquid (poly ethane glycol (PEG) or oil) from exhausted slurries by a two-step centrifugation process (the first step is SiC elimination, the second is liquid elimination).
- Magnetic removal of iron particles
- Chemical removal of iron and other metallic impurities
- Plasma purification to remove non-metallic impurities

The amount of end-of-life PV-modules is increasing and recycling of used solar cells [52] and modules [53] are increasingly relevant.

Deutsche Solar in Freiberg has developed a pilot scale module recycling line. By burning off the laminate, solar cells are first removed from the module compound structure. Subsequently the metallisation, anti-reflection coating and pn-junction of the cell are removed in an etching line. The clean wafers, which are the final product of the recycling process, can be processed again in a standard solar cell production line and integrated into a PV module [53]. The

energy payback time for a PV-module with recycled wafers is substantially lower than for the same module based on standard wafer production; 1.6 years as compared to 3.8 years if a middle-European location (irradiation of 1000 kWh/m<sup>2</sup>/year), a performance ratio of 0.75 and a module lifetime of 20 years is assumed. The environmental burden from the recycling process is claimed to be lower than for other end-of-life scenarios (waste at landfill sites or shredder process with subsequent sorting) [54].

### ***2.3 A wafer-manufacturer's challenges***

Due to the large number of new suppliers of silicon feedstock for solar cell applications, the manufacturers are facing many challenges. The feedstock will vary in terms of purity, type of impurities and shape. Questions that need to be answered are: Which impurities can be tolerated at which concentration level for a given process (that is casting, sawing or solar cell processing)? Will the feedstock shape influence the casting process?

Other issues that need to be considered are the price, the energy account and potential unwanted side effects such as for example CO<sub>2</sub>-emission, use of hazardous compounds etc.

### 3 Multicrystalline silicon

The crystal growth will influence the structure of the silicon crystal. This chapter gives an introduction to the Bridgman method for directional solidification and describes different growth mechanisms, the impurity distribution and some important defects.

#### 3.1 Crystal structures

Silicon crystals have diamond structure. The lattice is equivalent to two interpenetrating face-centred cubic (fcc) lattices displaced by  $\frac{1}{4}\langle 111 \rangle$ , with each atom surrounded by four nearest neighbours [55]. The lattice parameter,  $a$ , is 5.43 Å. A diamond lattice is shown in Figure 9.

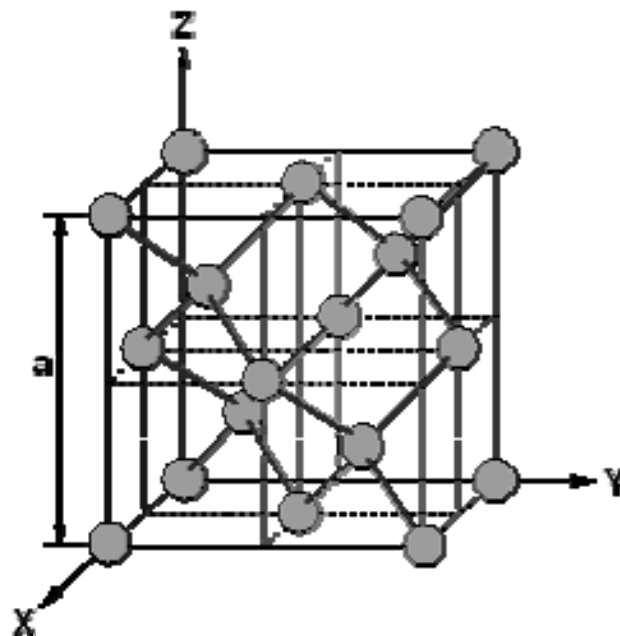
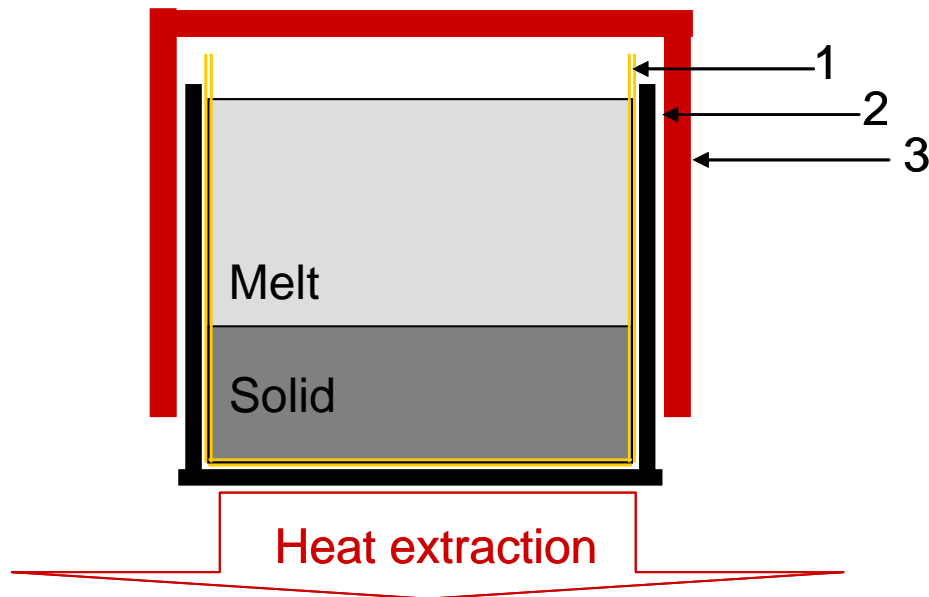


Figure 9: Diamond lattice [56].

#### 3.2 Directional solidification

Three major casting methods are commonly used in silicon solar cell production: Float zone, Czochralski and directional solidification. The first two methods are used to produce single crystals, and will not be treated here. Different ribbon techniques are also gaining more popularity due to the fact that wafer sawing is omitted, but none of these methods are treated in this thesis.

Bridgman is the most commonly used method for producing multicrystalline silicon because it gives columnar growth and a planar front. The basic principles are given in this chapter and a principle sketch is given in Figure 10.



**Figure 10: Principle sketch of a directional solidification setup. 1) quartz crucible coated with silicon nitride, 2) graphite support ring and plate and 3) susceptor which is heated by induction. Heat is extracted from the bottom by moving the heat source upward compared to the crucible and / or cooling the bottom of the crucible.**

The feedstock is charged in a silicon nitride coated quartz crucible and heated until all the silicon is melted. Heat is then extracted from the bottom of the crucible by moving the heat zone up compared to the crucible and / or cooling the bottom of the crucible. Often the crucible is lowered away from the heat zone and simultaneously the bottom is revealed to a cooling source. A temperature gradient is created in the melt and the solidification will start at the bottom and crystals will grow upwards, parallel to the solidification direction. To obtain a directional solidification the solidification heat must be transported through the steadily growing layer of solid silicon. It is necessary to maintain a net heat flux over the solid-liquid interface and the temperature at the lower part of the crucible must be decreased according to the increase in solid silicon thickness to maintain a steady growth rate. The growth rate is proportional to the temperature gradient difference between the solid and the liquid silicon as given in equation 11 [57].

$$11 \quad K_S G_S - K_L G_L = \rho_S H R$$

Where  $K_S$  = the thermal conductivity of solid metal

$K_L$  = the thermal conductivity of liquid metal

$G_S$  = the temperature gradient in the solid at the solid-liquid interface

$G_L$  = the temperature gradient in the liquid at the solid-liquid interface

$R$  = the growth velocity

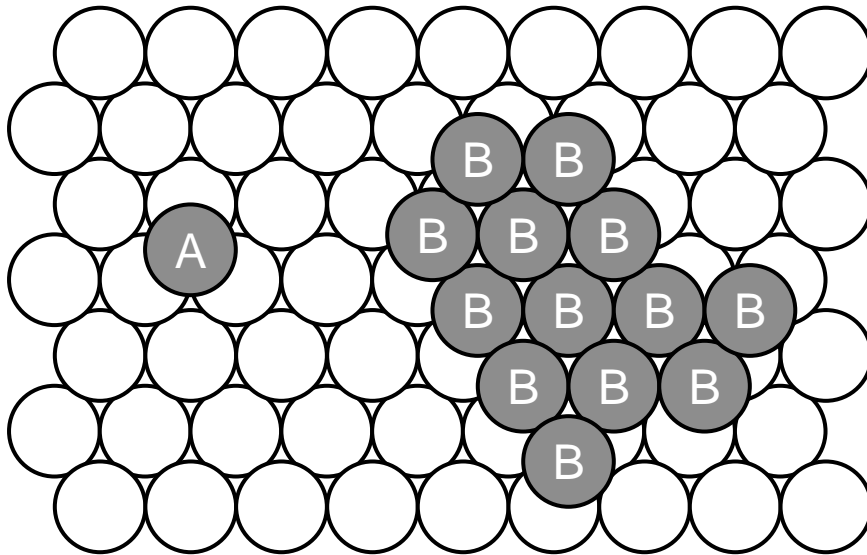
$\rho_S$  = the density of the solid metal

$H$  = heat of fusion

### 3.2.1 Crystal growth mechanisms

The growth mechanism for directionally solidified silicon crystals can be described by the two-dimensional nucleation model [58], see Figure 11. Single atoms absorbed by a flat and defect free solid-liquid interface (solid terrace) are weakly bound to the solid material and might easily re-enter the liquid phase. With increasing undercooling the number of absorbed

atoms increases and they might gather on the solid surface and form a two dimensional nucleus. As the number of Si-Si bonds increases, each atom is more strongly bound to the solid. Once such nuclei are formed, atoms absorbed to the solid terrace will diffuse to the energetically more favourable sites. The resulting lateral growth will proceed rapidly until a new layer is completed, and the formation of a new nucleus on the newly grown layer can form, and layers can be grown upon layers.



**Figure 11:** A sketch of the two-dimensional nucleation model. Atom A is weakly bound to the solid material and might easily re-enter the liquid phase, but the B-atoms are more strongly bound to the solid due to an increased number of Si-Si bonds. Energetically favourable sites are created, and a lateral growth might proceed quickly.

In dislocated material, which may be the case for multicrystalline silicon, energetically favourable sites already exist on the solid-liquid interface in the form of screw dislocations<sup>ii</sup> and there is no need for the nucleation step. For a screw dislocations growth mechanism each layer is completed by a spiral motion where one additional solid layer is completed by one round. The required undercooling for dislocation growth is substantially lower than for dislocation-free growth, <1 K versus 4-9 K [59].

An emerging twin<sup>iii</sup> plane at a crystal plane will also create a nucleation site for crystal growth. Dendritic growth of germanium crystals in the <211> directions bounded by {111} planes from an undercooled melt was described already in 1955 [60], [61], and twins in these dendrites were described the year after [62], [63]. Hamilton and Seidensticker (1960) [64] showed that at least two twin planes must be present for easy propagation in <211> direction. Albon and Owen (1963) [65] showed that the growth mechanism by double twins on a {111} plane is valid for silicon and indium antimonide as well as for germanium. In addition to growth in the <211> direction they also demonstrated growth in the <321> and <110> directions. The appearance of these directions is critically dependent on twin structure and undercooling [65], [66].

<sup>ii</sup> A screw dislocation is a dislocation with a Burgers vector parallel to the dislocation line. Dislocations will be treated in chapter 4.

<sup>iii</sup> Twins are grain boundaries with a high degree of symmetry. Twins are treated in the section about grain boundaries in this chapter

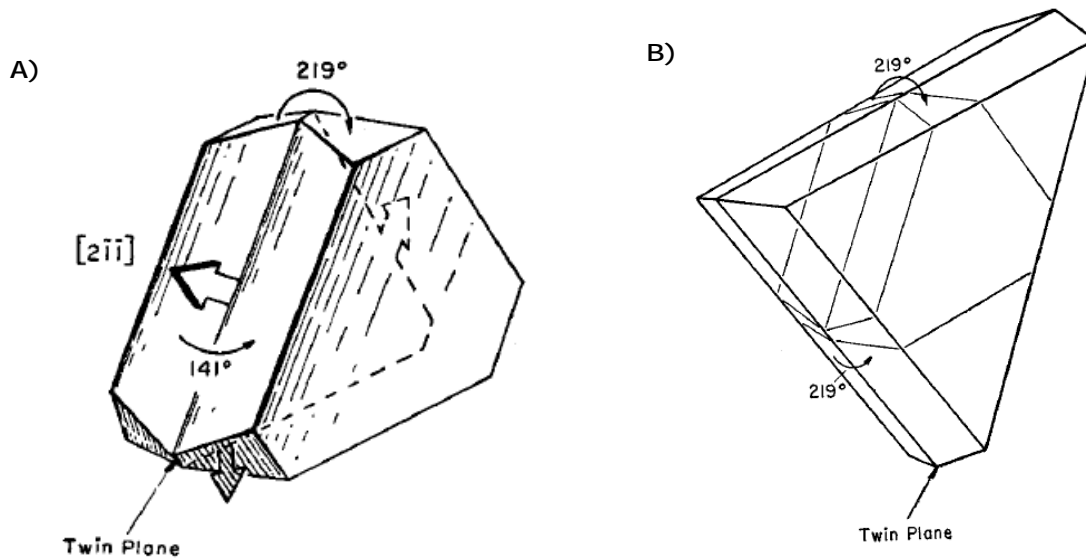


Figure 12: A) A twinned crystal is given to the left. The external angle between the bounding planes is alternately  $141^\circ$  and  $219^\circ$ . The former is a re-entrant corner and the latter a ridge structure. Preferable nucleation sites are at the three re-entrant corners, and if the corners are allowed to grow, B) a trigonal solid is obtained (shown at the right). This structure is bounded by three ridge structures and the parallel side planes. The figures are taken from [64]

Figure 12A shows a germanium crystal with a single twin plane bounded by flat, close-packed  $\{111\}$  facets. There are three directions which have a re-entrant angle and from which growth can proceed rapidly:  $[2\bar{1}\bar{1}]$  (shown),  $[\bar{1}2\bar{1}]$  and  $[\bar{1}\bar{1}2]$ . The rapid growth of these three planes causes them to disappear, leaving a flat crystal with its edges bounded by a ridge structure with no preferable nucleation sites, as shown in Figure 12B; rapid growth therefore ceases. If an additional twin plane parallel to the first is introduced as shown in Figure 13, it is six re-entrant growth sites at six  $\langle 211 \rangle$  directions, and rapid growth will take place in these directions. These nucleation sites will not disappear due to the fact that there will always be re-entrant corners present, as illustrated in Figure 13B.

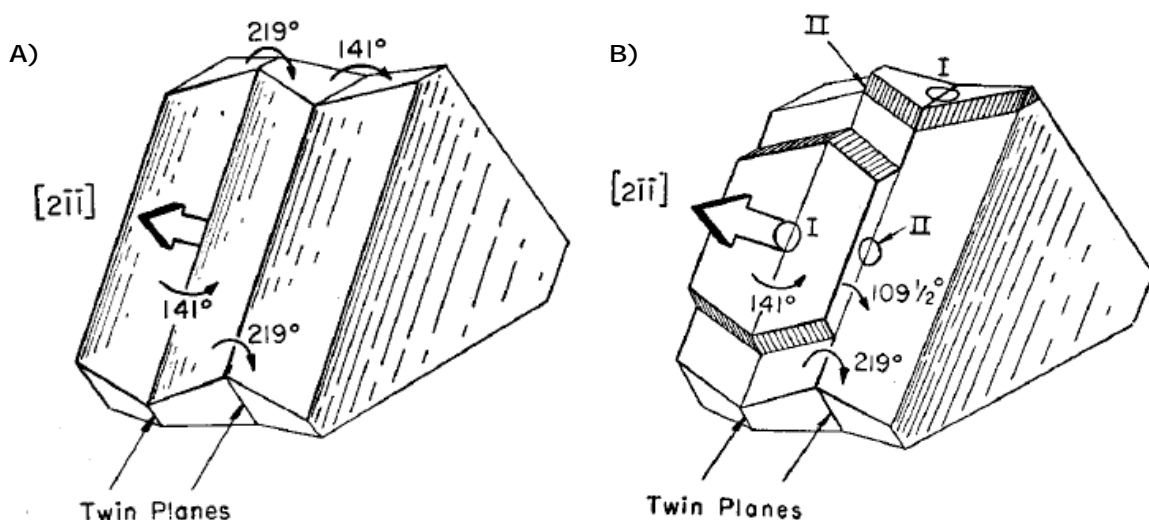
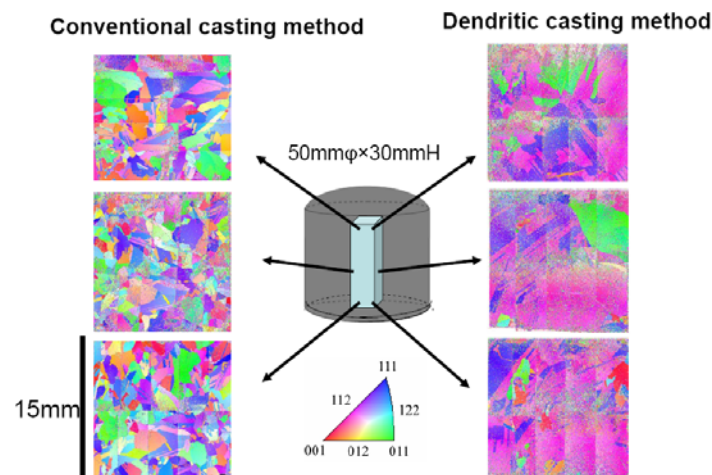


Figure 13: A) A crystal containing two twin planes is found to have six of the favourable re-entrant sites which leads to six equivalent  $\langle 211 \rangle$  growth directions. B) Two nucleation events (I) at two of the re-entrant corners have been allowed to occur. Growth from these has resulted in the development of new  $109.5^\circ$  corners (II) which makes nucleation across the ridge sites feasible. The figures are taken from [64].

Usami et al. (2008) [67] have studied controlled nucleation of directionally solidified silicon, and they report that dendritic growth in the nucleation phase will occur under some specified conditions. According to them, a  $\{111\}$  facet plane and a double twin boundary must be present for what they call *dendritic nucleation* to occur. The dominating grain orientations in a dendritic nucleated ingot, if the undercooling is between 10 K and 50 K, are  $\langle 111 \rangle$  and  $\langle 112 \rangle$ . For conventional silicon growth, the grain orientation will be more random, as made visible in Figure 14 by the same group.



**Figure 14:** The grain orientations for three different heights in a conventional and a dendritic ingot respectively, Fujiwara et al. (2006) [68].

In general, the solid-liquid interface is expected to be rough (on an atomic scale) during solidification, the exception being closely-packed interface planes, corresponding to the  $(111)$ -planes in silicon, where an atomically flat (smooth) interface is observed. The number of energetically favourable sites is much higher on a rough surface and the formation of new layers is therefore easier. As a result, growth rates can be substantially higher in less closely packed grains. This anisotropic growth rate can influence the macroscopic interface. At low growth rate, the macroscopic interface is flat, or non-faceted, whereas the microscopic interface is either rough (less closely packed planes) or smooth (closely-packed planes). For silicon it is expected that growth occur mainly on the  $\{111\}$  planes due to its high entropy of fusion, and the interface will be faceted in micro scale.

At higher undercooling and high growth rate the less closely packed planes will grow substantially faster than the closely packed planes, and the macroscopic interface will be faceted. Fujiwara et al. (2002) [58] and Fujiwara et al. (2004) [69] have confirmed the growth rate dependence on the transition from non-faceted to faceted growth by in-situ observations. They give a critical growth rate just above  $30 \mu\text{m s}^{-1}$ , above which the interface is faceted. They also observed that at high growth rate (faceted growth) the ability of  $\langle 100 \rangle$  grains to grow faster than  $\langle 111 \rangle$  grains favour the growth of the former which will extend laterally on expense of the slower growing  $\langle 111 \rangle$  grains. At lower growth rates, below  $\sim 30 \mu\text{m s}^{-1}$ , the  $\langle 111 \rangle$  grains will be the faster growing due to the lower interface energy of the  $(111)$  planes as compared to the  $(100)$ -planes. Actual growth rates of commercial multicrystalline silicon are below the critical value given by Fujiwara, and in the pilot scale furnace at NTNU a growth rate of  $4 \mu\text{m s}^{-1}$  was observed with typical run parameters [30]. In accordance with



Fujiwara's study, the grains with  $\langle 111 \rangle$  direction are often dominant in commercially multicrystalline material.

### 3.3 Defects

Perfect silicon crystals have a periodic arrangement of atoms. In real crystals, deviation from the crystal symmetry occurs; these are called *defects*. There are many kinds of defects, including: *Point defects*, which are localised in the vicinity of a few atoms in the crystal; *line defects* or *dislocations*, which propagate as lines in the crystal, *planar defects*, such as grain boundaries and stacking faults which extend over an area in the material [70], and precipitates. Dislocations are treated in chapter 4, and a short overview of point defects, grain boundaries and precipitates is given here. Some terms defined in chapter 4 are used in this chapter without further references or explanations.

#### 3.3.1 Point defects

Several types of point defects can be identified in a crystal. A *vacancy* is a defect due to the absence of an atom on a lattice site. In a silicon crystal, such a vacancy will result in four unsatisfied or dangling bonds from the atoms surrounding the vacancy directed inwards towards the vacancy. These dangling bonds may recombine, producing a local distortion of the lattice. Vacancies are important for nucleation of precipitates associated with an expansion in the crystal lattice [71].

The *substitutional* impurities are the most important point defects in semiconductors [70]. In this case, an impurity atom replaces an atom in the host lattice. Small numbers of such substitutional impurities can have a large effect on the electrical conductivity of a semiconductor. The elements of group V (such as P, As, Sb or Bi) will substitute the silicon atoms in the lattice and give rise to an excess of an electron, whereas elements from group III (such as Al, Ga or B) give rise to a deficit of bonding electrons. These substitutional impurities are called *n-doping* and *p-doping* respectively.

It is possible to introduce atoms into a silicon crystal, even if no lattice site is available to them. Such atoms will sit between the host atoms at a non-lattice site, known as interstices of the lattice, and are called *interstitial* atoms. The diamond lattice structure is relatively open and interstitial atoms can easily be accommodated. Cu, Fe, Mn, O and C are common interstitial atoms in silicon [70]. Interstitial atoms diffuse easily in the crystal lattice compared to substitutional atoms and are often referred to as *fast diffusers*.

#### 3.3.2 Grain boundaries

Two grains with different crystal orientation that grow next to each other are divided by a grain boundary. Even though the grains have different orientation they may possess some common lattice sites. If that is the case, the atoms occupying these sites constitute a new lattice, which is called the co-incidence site lattice (CSL). The ratio between the number of atoms per volume in the original lattice to the number of atoms in the CSL defines a number,  $\Sigma$ , that characterises the relation between the two grains, see equation 12.

$$12 \quad \Sigma = \frac{n_{Original}}{n_{CSL}}$$

$n_{Original}$  is the atom density in the original lattice and  $n_{CSL}$  is the atom density in the coincidence site lattice. The  $\Sigma$ -number will thus characterise the boundary between grains and their symmetry. Only certain  $\Sigma$ -numbers are allowed, and for cubic crystals  $\Sigma 3$ -boundaries have the highest degree of symmetry and are called *twin boundaries*, then comes  $\Sigma 5$ ,  $\Sigma 7$ ,  $\Sigma 9$  etc, whereas  $\Sigma n$  have every  $n$ 'th atom in common.

Grain boundaries with no or randomly distributed common atoms between the two grains are called non-CSL boundaries or random grain boundaries, these are more electrically active and have a higher energy than the CSL-boundaries.

Sub-grain boundaries will often exist in a much higher density than regular grain boundaries in multicrystalline silicon. A seemingly large grain can contain a large number of sub-grains. A sub-grain boundary is constituted of a web or line of dislocations. The dislocations might have different orientations and Burgers' vectors, but the combined effect of them is that one part of a grain is rotated relative to another part, but it is only rotated such that the  $\Sigma$ -number will still be one. Sub-grain boundaries may be formed by different types of dislocations; if the dislocations are only edge type (the Burgers vector is normal to the dislocation line), the boundary is called a *pure tilt boundary*, if the dislocations are only screw type (the Burgers vector is parallel to the dislocation line), the boundary is called a *pure twist boundary*. Sub-grain boundaries are shown to be more electrically active than regular grain boundaries [72], and are thus more harmful for solar cell performance.

While grain boundaries are created by two grains growing next to each other, sub-grain boundaries may form between facets during faceted growth. Sub-grain boundaries might also be created due to dislocation nucleation, multiplication and movement at high temperatures and during cooling. A sub-grain is an ordered structure with the dislocations arranged in the energetically most favourable way. For this to happen, it is necessary that the dislocations are able to move in all directions, that is by both slip and either cross-slip or generation of vacancies. Climb, which is necessary if the dislocation has an edge component, is a non-conservative process and requires annihilation or generation of vacancies. The density of vacancies is temperature dependent, and climb may only occur at high vacancy densities and thus high temperatures. The term high temperature means 650 °C for silicon [73].

### 3.3.2.1 Deformation twins

Twinning is a deformation mode which brings about changes in the orientation of the crystal, but not the crystal structure. The crystal might deform by twinning if the crystal experiences homogeneously distributed shear deformation over a given region. Twinning is when the crystal undergoes a change in the stacking order of the [111] bonds from ...ABCABC... to ...ACBACB...

In practice, twinning does not take place uniformly over the whole crystal under stress, but only within rather thin layer regions along the (111) planes in the crystal. The boundary between such a twinned area and the matrix region is called a twin boundary, which is a  $\Sigma 3$

boundary. Twin boundaries observed in diamond structures are parallel to the  $\{111\}$  planes [74].

In any given crystal, twinning deformation is observed to be dominant at low temperatures and under high deformation rates in comparison with slip deformation [75].

In silicon it is, however, believed that most of the twins are growth twins and not deformation twins.

### **3.3.3 Precipitates**

If impurities are present in concentrations larger than their solubility at a given temperature, they may precipitate, usually as compounds of silicon, provided that suitable nuclei are present. These nuclei might be different kind of defects.

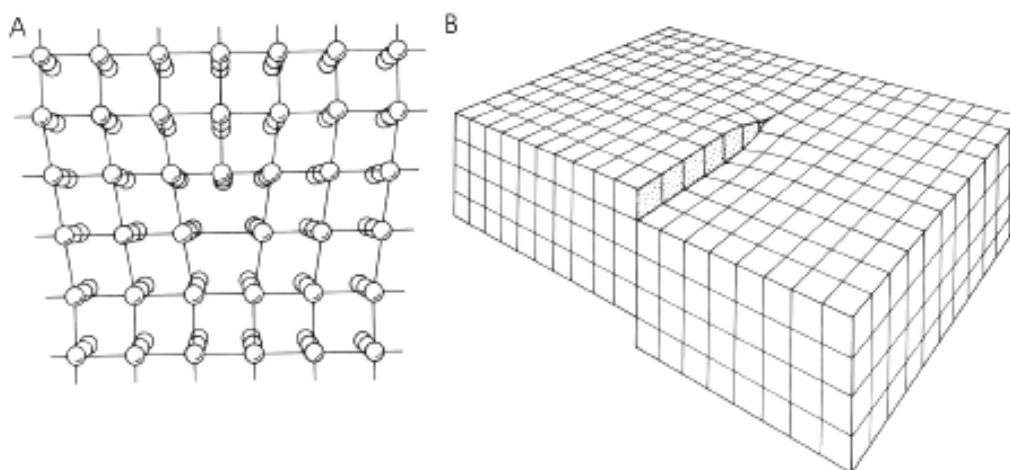
Precipitates may form during solidification, during cooling after growth or during heat treatment at subsequent cell processing. Dislocation loops and stacking faults may form as secondary defects as a consequence of precipitate formation [76]. These secondary dislocation loops originate from strain fields in the crystal and are formed by so-called punch-out mechanisms which are activated by a large difference between the precipitates' volumes and the matrix volume, and is independent of its sign [3]. Talanin and Talanin (2004) [77] claims that the driving force of formation of dislocation loops in mono crystalline silicon made by Czochralski pulling or float zone are carbon interstitial agglomerates formed at impurity centres.

## 4 Dislocations

This chapter includes some basic theories relevant for this study. Structure, nucleation, motion and multiplication of dislocations are treated in the following.

### 4.1 Structure

Dislocations are responsible for the plastic behaviour of crystalline materials, but they may also significantly influence the electrical properties, especially of semiconductors. Two main classes of dislocations exist; edge and screw dislocations, see Figure 15, A and B respectively. The Burgers vector of an edge dislocation is normal to the line of the dislocation, and for a screw dislocation it is parallel to the line of the dislocation. Most dislocations are, however, a mixture of the two.



**Figure 15: A) Edge dislocation, B) Screw dislocation. This figure is taken from [78].**

The use of the Burgers vector in a region holds for any elastic medium containing any distribution of dislocations [78], but it is usually applied to single dislocations or small number of dislocations. The Burgers vectors are conserved at dislocation nodes [78], which are where three or more dislocations meet.

A dislocation line cannot end within an otherwise perfect region of a crystal, but must terminate at a free surface, another dislocation line, a grain boundary, or some other defect [78], [79]. A dislocation generated from a source within a crystal with diamond structure usually assumes a hexagonal shape if the dislocation is isolated from other dislocations. The loop consists of segments of  $60^\circ$  and screw dislocations. The hexagonal shape is also presumed in crystals with relatively high impurity content. [80]

Geometrically, dangling bonds, or unpaired electrons, are aligned along the dislocation core. It is, however, commonly accepted that such geometrically dangling bonds are reconstructed to make bonds between two atoms neighbouring each other along the dislocation line [81].

Impurities are attracted to dislocations. The impurity mobility is higher on dislocations, and pipe diffusion will lead to clusters of impurity atoms and often precipitation. Foreign atoms may influence the dislocation mobility, and precipitates may pin the dislocations.

## **4.2 Nucleation of dislocations**

The thermodynamically stable density of dislocations in a stress-free crystal is zero [82]. There are, however, many dislocation nucleation mechanisms playing a role while growing and cooling a crystal.

### **4.2.1 Nucleation of dislocations at stress concentrators**

One well-known mechanism of dislocation nucleation is when dislocations are punched out from around an inclusion with different thermal expansion coefficient during cooling. The nucleation of dislocations results from the stress produced around the inclusion by the different contraction of the crystal and the inclusion. When the stress reaches a critical value, about  $\mu/30$  [82], dislocations are nucleated. Here  $\mu$  is the shear modulus.

The stress produced around inclusions is also dependent on the inclusion size. Nishino and Imura (1982) have shown that dislocations form in connection with oxygen precipitates in Czochralski-grown crystals when external stress was applied [83]. They observed that dislocations were generated preferentially at oxide precipitates and that the punch-out dislocations propagated on to the slip planes. The plastic flow always took place at the large oxide precipitates (millimetre size) for stress significantly lower than the macroscopic yield stress. The stress to cause the local plastic flow was higher with decreasing precipitate size. More dislocations were punched out to release the increased misfit strain associated with the precipitate as the precipitates grow in size. It is reasonable to assume a similar effect in other systems as well. Transferring these results to precipitates in a directional solidified multicrystalline ingot, the precipitates might be oxides, carbides, nitrides, silicides, metallic or mixtures and the applied stress is obtained during growth and cooling after solidification. One might suspect that less stress is needed to punch out dislocations from bigger inclusions than from smaller ones of same kind. Punch-out from coating particles can also be anticipated.

### **4.2.2 Nucleation of dislocations at grain boundaries**

Many investigations have shown that dislocations can be emitted from grain boundaries [82] and many nucleation mechanisms are suggested. A brief overview is given here.

#### **4.2.2.1 Thermal expansion coefficients and elasticity modules**

The thermal expansion coefficient for silicon is dependent on temperature [84], and it has been claimed that it is dependent on crystal orientation as well. Mazur and Stepanova (2005) [85] have measured the thermal expansion coefficient for monocrystalline silicon in a wide temperature range and for different crystallographic orientations. According to them the temperature dependence of the thermal expansion coefficient in silicon is non-monotonic and anisotropic.

It is, however, generally accepted that the thermal expansion coefficient for cubic crystals is isotropic, but the elastic constants that relate stress to elastic strain according to Hooke's law are anisotropic. The elastic constants are also dependent on temperature [86] and on doping [87], [88]. For cubic crystals three independent constants are needed to determine stress and strain. A crystal subjected to stress will thus have different strain depending on crystal orientation.

#### 4.2.2.2 Intragranular- and intergranular hardening

Stress fields will develop during growth and during the subsequent cooling when grains with different crystallographic orientation grow next to each other, and especially where three or more grains meet, due to intragranular- and intergranular hardening [89]. The stress is generated by thermal expansion and contraction. The average responses of different grains to applied stress are quite inhomogeneous. This is a direct consequence of the interaction between grains and is due to mechanical constraints by the neighbouring grains. The interaction leads to strong non-proportional mean stress evolution.

A major role played by the neighbouring grains on the behaviour of an individual grain can be assigned to the number of surrounding grains: The more surrounding grains, the higher effect, and this effect is more significant than the surface effect.

The intergranular compatibility forces the grain boundary region to deform more than the core of a grain. This is because of differences in crystallographic orientations which will lead to a misfit of the slip planes in the different grains. Each grain will thus respond individually on the applied stress and different slip systems will be activated.

#### 4.2.2.3 Grain boundaries

Dislocations generated by sources within the grains produce large stress concentrations when piled up at a grain boundary. These can further activate grain sources at relatively low applied stress.

It is also suggested that migrating grain boundaries can produce dislocations in the lattice they pass through [82]. The dislocation density increase is dependent on the speed of the movement, and can be as high as a factor of  $\sim 10^4$ . The proposed nucleation mechanism is by accidental mispacking of atoms at the grain boundary when one grain grows at the expense of another [90]. It is however traditionally assumed that grains growing on expense of another can decrease the dislocation density by producing a dislocation sink where dislocation lines might end in the grain being overtaken. For the dislocation density to decrease by this method, it requires that the overtaking grain has a lower dislocation density than the overtaken, and in reality both mechanisms might play a role.

### 4.3 Dislocation mobility

The velocity of dislocation motion under a given stress depends very sensitively on the temperature, but it is not so sensitive to stress under a given temperature. The dislocation velocity in any semiconductor under a given stress increases as the temperature increases. There are two basic types of dislocation movement: *Glide* and *climb*. A dislocation able to move by glide is called *glissile*, while a dislocation which is not is called *sessile*.

### 4.3.1 Glide

Glide or conservative motion occurs when the dislocation moves in the plane that contains both its line and the Burgers vector. Glide of many dislocations results in slip, which can be visible as steps on the crystal surface. This process involves successive displacement of one atom plane over another on so-called slip planes. Conservative motion means that the total number of atoms and lattice sites are conserved. Discrete blocks of crystal between two slip planes remain undistorted.

The slip planes and directions in a crystal have specific crystallographic forms. Slip planes are normally the planes with the highest density of atoms and the direction of slip is the direction in the slip plane corresponding to one of the shortest lattice translation vectors. Often, this direction is one in which the atoms are most closely packed. The plane that must contain both the Burgers vector ( $\mathbf{b}$ ) and the dislocation line and the slip plane-normal to a straight dislocation is defined as  $\mathbf{b} \times \boldsymbol{\xi}$ , where  $\boldsymbol{\xi}$  is the unit vector for the dislocation line. Curved dislocations can also move conservatively, by pure slip, on the cylindrical surface containing  $\mathbf{b}$  and the curved dislocation line.

For edge dislocations, there is only one plane containing both the Burgers vector and the dislocation line. There is thus only one uniquely defined slip plane for an edge dislocation. For screw dislocations, however, the Burgers vector and the dislocation line are parallel and do not define a unique plane. The glide of a screw dislocation is therefore not restricted to one specific plane. The displacement of the atoms and hence the slip step associated with a screw dislocation is parallel to the dislocation line, for that is the direction of the Burger vector. For dislocations with mixed character, the slip plane is determined by the edge component.

For the diamond lattice, there are three groups of six equivalent planes which are possible slip planes;  $\{001\}$ ,  $\{110\}$  and  $\{111\}$ , where the  $\{111\}$  planes are the most likely ones, and are the only slip planes found experimentally [91], [92].

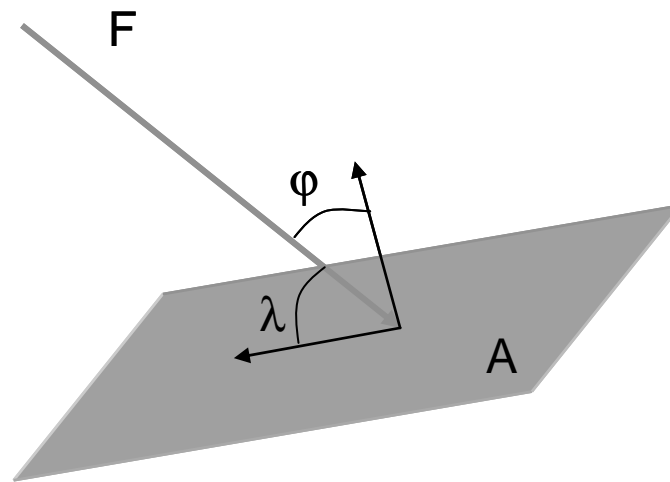
Dislocations are generally energetically most stable and have generally the highest mobility when they lay along the most closely packed directions [93] which are the  $\langle 110 \rangle$  directions in the  $\{111\}$  planes in the diamond structure. Thus, stable dislocations which can undergo glide motion in silicon are either  $60^\circ$  dislocations or screw dislocations [94]. Their dislocation lines make angles of  $60^\circ$  and  $0^\circ$  respectively with the Burgers vector.

The resolved shear stress,  $\sigma$ , for slip in a crystal is given by equation 13.

$$13 \quad \sigma = \frac{F}{A} \cos \phi \cos \lambda$$

$F$  is the applied force on the crystal. The force has a component  $F \cos \lambda$  in the slip direction where  $\lambda$  is the angle between  $F$  and the slip direction, see Figure 16. This force act over the slip surface which has an area  $A / \cos \phi$ , where  $\phi$  is the angle between the  $F$  and the normal to the slip plane. The quantity  $\cos \phi \cos \lambda$  is known as the *Schmid factor*. At stresses higher than  $\sigma$ , slip may start and according to *Schmid's law*, slip will occur on the system having the

highest resolved shear stress. Schmid's law is however not always valid for ultra pure materials [95]. On an atomic scale, the glide process takes place by moving kinks.

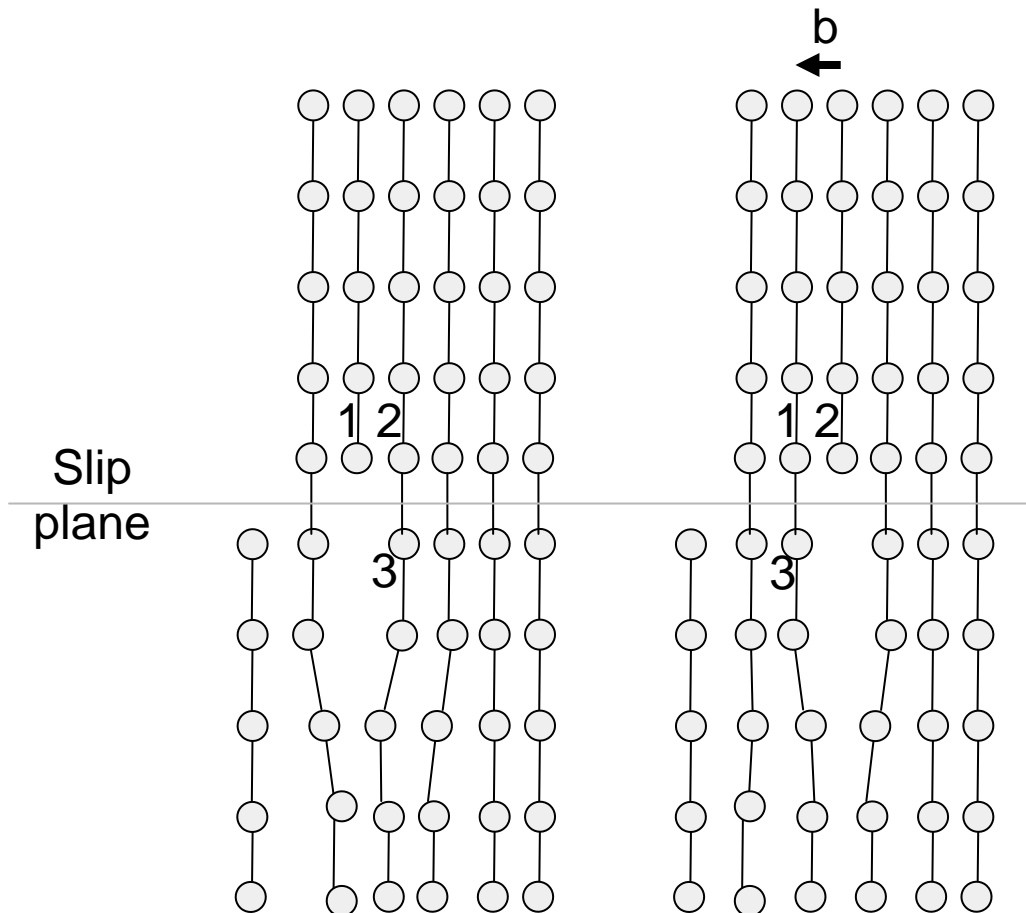


**Figure 16: An applied force on a slip plane in a crystal**

The applied stress required to overcome the lattice resistance to a dislocation movement was early shown to be much smaller than the theoretical shear stress [96], [97]. Well away from the dislocation, the atoms are arranged in a near perfect crystal structure, and the shear stress required to slide them past each other is given by the equation for theoretical shear stress in a perfect lattice. Closer to the dislocation, however, the atom spacing have values far from the ideal and only small changes in atom position of only a few atoms are required to move the dislocation.

Two adjacent atoms across the slide plane are displaced relative to each other by the Burger vector when the dislocation glides past. Thus the slip direction is always parallel to the Burgers vector responsible for the slip, see Figure 17.





**Figure 17: Movement by an edge dislocation by glide. Two adjacent atoms across the slide plane (2 and 3) are displaced relative to each other by the Burgers vector when the dislocation glides past. Thus the slip direction is always parallel to the Burgers vector responsible for the slip.**

#### 4.3.1.1 Cross slip

In general, screw dislocations in silicon tend to move in certain  $\{111\}$  planes, but it can switch from one  $\{111\}$  type plane to another if both planes contain the Burgers vector. This process is called cross slip and glide will continue in the new  $\{111\}$  plane. Only pure screw segments are free to cross slip and to move in both slip planes. Double cross slip is when the screw dislocation cross slip back to the original  $\{111\}$  slip plane. A dislocation can cross slip back and forth between two slip planes.

#### 4.3.2 Climb

Movement of a dislocation out of the glide surface and normal to the Burgers vector is called climb or non-conservative motion. Climb requires diffusion of atoms or vacancies.

At low temperatures, where diffusion is difficult, and in absence of non-equilibrium concentrations of point defects, the movement of dislocations is restricted almost entirely to glide. At high temperatures, however, an edge dislocation can move out of its slip plane by climb. Climb occurs by diffusion or formation of self-interstitials or vacancies, and it is this process of adding matter that refers to the term non-conservative. In silicon, the equilibrium

concentration for vacancies is higher than the equilibrium concentration of self- interstitials, due to a higher diffusivity of interstitials [98]. The self-stress of an edge dislocation does not exert a climb force on the dislocation, the mass transport involved occurs by diffusion and therefore climb requires thermal activation. The most common climb processes involve the diffusion of vacancies either towards or away from the dislocation. The climbing process acts thus as sources and sinks for vacancies.

The total energy change involved in climb is, by definition that of removing matter from the inserted plane to deposit it on a stress-free perfect crystal. At the expense of strain energy and potential energy, energy flows to the dislocation core and is dissipated there as the dislocation climbs.

A short section of a dislocation will climb at a time, in steps called jogs. Jogs are, thus, steps on the dislocation which move it from one slip plane to another. Steps which displace the dislocation within the same slip plane are called kinks. Jogs and kinks are short elements of dislocations with the same Burgers vector as the line on which they lie. The climb does not prevent glide of an edge dislocation, in fact it might rather assist it [99].

Pure screw dislocations cannot climb, but a small edge component or a jog on a screw dislocation will provide a site for the start of climb. A jog on a screw dislocation has edge character and can only glide along the dislocation line. All movements at a right angle to the Burgers vector requires climb. Jogs thus hinder glide of the screw dislocation and result in point defect production during slip.

### 4.3.3 Impurity effects on dislocation motion

Electrically inactive light elements dissolved in silicon do not affect the dislocation velocity while moving under high stress. With decreasing stress, however, the dynamic behaviour of the dislocations will differ from the behaviour in high purity silicon. Dislocations originally in motion under high stress will cease to move when the stress is reduced to 3 MPa in O-doped silicon ( $[O] = 7.4 \cdot 10^{17} \text{ cm}^{-3}$ ) and to 4 MPa in N-doped silicon ( $[N] = 5.4 \cdot 10^{15} \text{ cm}^{-3}$ ) [80].

Donor impurities such as P, As and Sb are reported to enhance the mobility of both  $60^\circ$  and screw dislocations [80], [100], [101], [102], [103]. The increase in dislocation velocity as compared to high purity silicon due to doping with donor impurities under any stress at any temperature is determined only by the donor concentration and is not influenced by the impurity species.

Acceptor impurities such as B and the electrical inactive impurity, C, affect the dislocation velocity very little [80].

Irrespective of the purity of silicon, a dislocation in motion will keep a hexagonal shape consisting of straight segments along the  $\langle 110 \rangle$  directions if it moves at a velocity which is linear to the stress. The dislocation shape becomes irregular when moving in a low-stress range and when velocity is not linear to the stress. The changing of shape of a moving dislocation is reversible [75]. In impure silicon, moving of dislocations in a low stress range will be locally affected by impurity related obstacles on the dislocation line. The dislocations can bow out and pass around the obstacle under stress. If the obstacle is a single atom impurity, the energy needed for a dislocation to pass around is not high enough to affect the

dislocation mobility in the temperature range 500 – 800 °C [80]. Thus the impurity related obstacles that slow down dislocation motion in lower stress regions are thought to be clusters or complexes of impurities which are developed at the core of a slowly moving dislocation. The pipe diffusion of impurities along the dislocation core is thought to play an important role in developing the pinning obstacles. Dislocations will eventually cease to move due to such cluster formation.

#### 4.3.4 Image forces

A dislocation near a free surface experiences forces not encountered in the bulk. The dislocation is attracted toward the surface to minimise its length and thus its energy. To treat this mathematically, image forces are introduced. A dislocation line located at a distance  $d$  from a free surface is mirrored around the surface. The real dislocation and the mirror image will attract each other such that both dislocation lines will bend and be attracted to the surface. The image forces decrease slowly with increasing  $d$ .

### 4.4 Dislocation multiplication

When a dislocation is nucleated, it can be multiplied by different processes. Some of these are explained below.

#### 4.4.1 Multiplication by Frank-Read sources

Consider a dislocation line which is fixed by some unidentified barrier in both ends and is exposed to a shear stress, as shown in Figure 18. The barrier could be dislocation nodes, precipitates etc. The Burgers vector,  $\mathbf{b}$ , will lie in the glide plane, and the shear stress component  $\mathbf{b}\tau$ , will make the dislocation line bow out with a radius which depend upon the amount of shear stress.

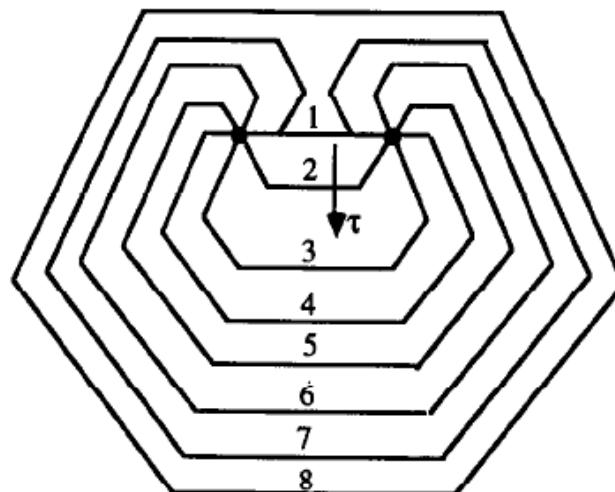
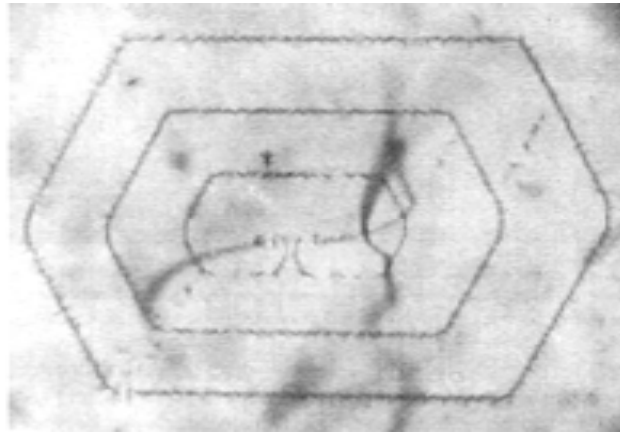


Figure 18: Simulated loop emitted by a Frank-Read source in a (111) slip plane. The source segment (1) is a  $1/2[101]$  screw of length 0.81  $\mu\text{m}$ , positioned at the centre of a model crystal (Temperature = 1 000 K,  $\sigma$  (named  $\tau$  in the figure) = 35 MPa). The illustration is taken from a simulation of dislocation dynamics in silicon done by Moulin et. al. (1997) [104]

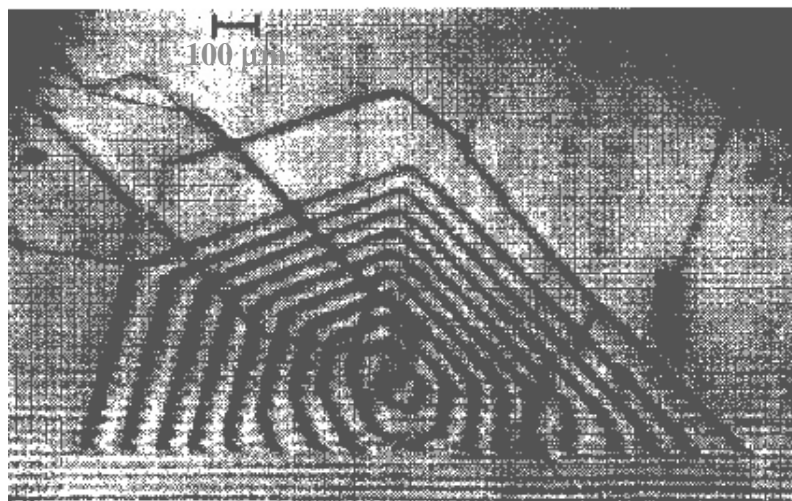
The line will continue to expand at the applied stress and the subsequent events are shown in Figure 18. Segments close to the barriers will buckle out on the rear side and will eventually meet and annihilate. This occurs because the segments, which move in opposite directions under the same stress, have the same Burgers vector but with opposite sense. The result is a larger outer loop, which continues to expand, and the original dislocation line will repeat the process and create a pattern consisting of loop outside loop. A double-ended Frank-Read source in silicon made visible by copper decoration is shown in Figure 19.



**Figure 19: A Frank-Read source in silicon made visible by copper decoration. Taken from the work of W. C. Dash (1957) [105]**

The hexagonal shape of the Frank-Read loops are due to the deep potential valleys for dislocations which extend along the  $\langle 1\bar{1}0 \rangle$  directions in the (111) planes [75].

Single-ended Frank-Read sources can also lead to dislocation multiplication under stress [106], [107], as shown in Figure 20.



**Figure 20: An X-ray topograph of a single ended Frank-Read source close to a surface as published by Authier and Lang (1964) [107]. The sample was heated to 900 °C before it was twisted about its long axis. The dislocation pattern shown in the picture was formed at the crystal's surface. The scale mark is 100 μm.**

#### **4.4.2 Multiplication by multiple cross glide**

Since the glide of a screw dislocation is not restricted to one specific slip plane, screw dislocations can cross glide onto a parallel slip plane. If the stress is greater on the primary plane the jogs will be relatively immobile. However the segments lying in the primary plane can each act as a Frank-Read source. Cross glides can occur frequently and the Frank-Read source may never complete a circle and there will be continuous dislocation lines lying in many parallel slip planes connected by jogs. It is thus possible for a dislocation to multiply in such a way that the slip spreads from plane to plane, producing a wide slip band. Multiple cross glide is a more effective mechanism for multiplication than the Frank-Read source and results in a more rapid multiplication [82].

#### **4.4.3 Multiplication by Bardeen-Herring sources**

A regenerative multiplication known as the Bardeen-Herring source can occur by climb in a similar way to the Frank-Read mechanism illustrated in Figure 18. The difference is that the Bardeen-Herring source does not multiply in the slip plane. An excess of vacancies will cause the dislocation to climb. If the dislocation's anchor points are a dislocation with screw characteristics, the process will be regenerative. The resulting dislocation pattern will look very much like the one obtained from a Frank-Read source, but is not located in the dislocation's slip plane.

## 5 Detection of dislocations in silicon

A wide range of techniques have been used to study dislocations; both surface methods, in which the point of emergence of a dislocation at the surface of a crystal is revealed, and more bulk related techniques. The surface methods used in this thesis is described in this chapter.

### 5.1 Detection of dislocations by surface methods

If a crystal containing dislocations is in an environment which removes atoms from the surface, the rate of which atoms are removed will in general be different where dislocations emerge at the surface than at the surface of the surrounding crystal matrix. The difference in the rate of removal of atoms is due to one or more of the following dislocation properties:

- Lattice distortion and strain fields in and around the dislocation
- The geometry associated with screw components in dislocations which will nucleate the reverse process of crystal growth and produce a surface pit
- Higher concentration of impurities at the dislocations will change the chemistry

If the rate of atom removal is higher at the dislocations than at the matrix, pits are formed, and if the rate is smaller, hillocks are formed. Many methods are available for slow and controlled atom removal from crystal surfaces. The most common are chemical and electrolytic etching. Other methods include thermal etching and sputtering. Common for all techniques is the requirement of a one-to-one correspondence between dislocations and pits or hillocks. As early as in 1953 Vogel et al. [108] showed a one-to-one correspondence between etch pits and edge dislocations in a grain boundary between two germanium crystals. Dash (1956) [109] illustrated the one-to-one correspondence in silicon by diffusion of copper into dislocation etched silicon samples as shown in Figure 21.

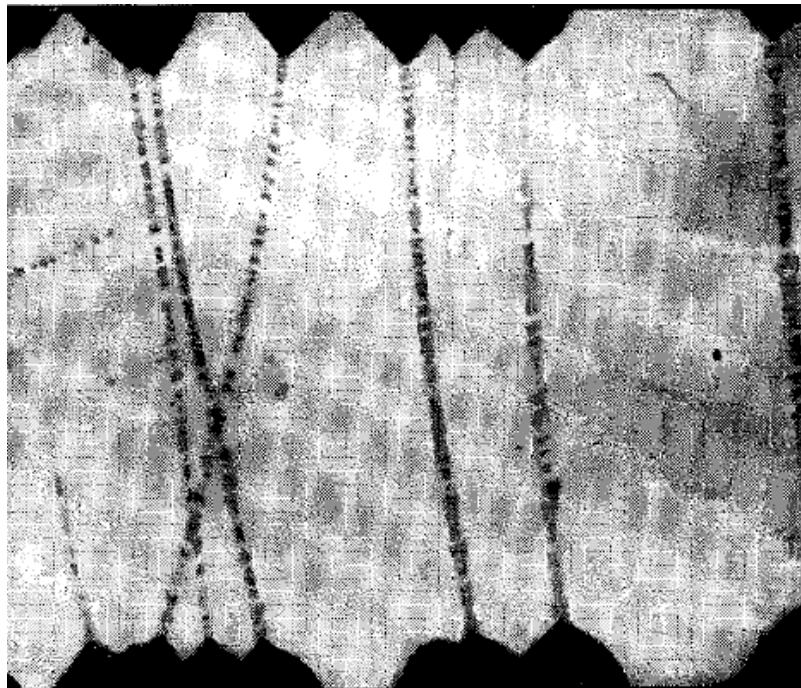


Figure 21: Infra red image of dislocation lines decorated by copper and etch pits in silicon [109]

When it comes to etching of silicon, a number of dislocation etches have been developed [110], [111], [112], [113], [114], [115], [116], [117].

### 5.1.1 The HF:HNO<sub>3</sub>-system

One group of dislocation etches contains HF, HNO<sub>3</sub> and a diluting agent in different ratios. The diluting agent can be water or acetic acid. The latter being the most usable in this context due to the HF:HNO<sub>3</sub>:diluent-system's much greater tolerance for acetic acid than for water as the diluting agent [118]. The etch rate depends on the composition of the acids in the etch solution, the temperature, p- or n-type, the conductivity, defects and the crystal orientation.

The basic reaction in the dissolution of a silicon surface is an oxidation of the silicon followed by removal of the oxide by the HF, the sum-formula of the reaction is given in equation 14 [119]. In order to reveal a crystal defect, that is, to form an etch pit, the defect area must oxidise and be removed faster than the surroundings. If HF is in excess in the etching solution, the oxide is removed as soon as it forms. Under this condition, the formation of etch pits will be determined by the oxidation rate differential [112].

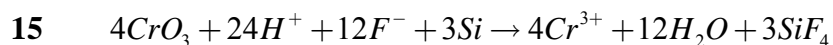


If HF is in limited supply, dissolution of the formed oxide is the rate-controlling step and diffusion of the complexing fluoride species is the important factor. In such a system, the etch rate will be independent of crystal orientation and conductivity [118].

Some compositions of this system can act as chemical polishing [114] and is used to remove saw damages and leaves a relatively smooth surface. The natural tendency of a diffusion-controlled reaction is the development of rounded corners and edges, since the availability of reagent is greater at the corners and edges of the specimen than in the centre [118]. The surface created by the chemical polishing solution will thus be smoothed.

### 5.1.2 The HF:CrO<sub>3</sub>-system

In the systems containing HF and CrO<sub>3</sub> in solution, the Cr<sup>6+</sup> ions will act as oxidation agent. The HF will, as for the HF:HNO<sub>3</sub>-systems, dissolve the formed oxides [113]. The total chemical formula is given in equation 15 below [115].



### 5.1.3 Sample preparation by polishing and Sopori etching

The chemical mechanical polishing procedure developed during the work done in connection with this thesis is as follows: Wafers are mounted on to a planar aluminium plate using a water-soluble wax (Crystalbond<sup>TM</sup> 555 from Electron Microscopy Science). The wafers are heated to at least 54 °C, which is the wax's flow point [120], before a thin layer of wax is applied and the wafer is fitted to a sample holder. After polishing the sample must be reheated and the wafer can be carefully slid off. Figure 22 shows the setup for the wafer-polishing. The

parameters used are shown in Table 2 and the standard procedure developed is given in Table 3.

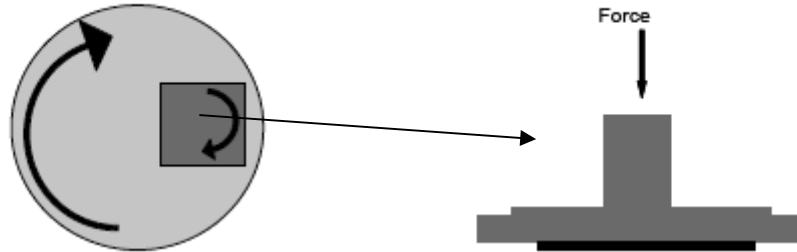


Figure 22: Schematic drawing of the polishing setup seen from above (left) and the wafer sample holder seen from the side (right).

Table 2: Parameters used during wafer polishing

Parameter	Value
Polishing disc rotation speed	300 rpm
Sample rotation speed	300 rpm

Table 3: Polishing procedure

Medium	Mesh / Size	Time/minutes
Grinding paper	500	3
Grinding paper	1 200	3
Polishing pad with diamond spray	9 $\mu\text{m}$	3
Polishing pad with diamond spray	3 $\mu\text{m}$	3
Polishing pad with diamond spray	1 $\mu\text{m}$	3
Polishing pad with slurry	-	1
Polishing pad with water	-	1

The slurry used is Nalco 2350 which is a colloidal silica polishing slurry with a silica particle diameter of 50 - 70 nm [121].

After polishing the wafers are cleaned in RCA clean [122] and DI water and subsequently etched in Sopori etch [116]. The process is given in Table 4.

The etching step (Sopori) was done in 30 seconds or 20 seconds after activation of the acid solution. It was noted that fresh Sopori etch will not immediately start the etching of a wafer. A clean wafer is thus used to activate the etch prior to etching by dipping it into the Sopori solution until reaction starts. It will typically take a few seconds before bubbles are forming on the wafer surface. The etch is furthermore not stable in air atmosphere and it loses effect relatively fast. New Sopori etch should thus be made if the etch is stored between each batch of wafers being etched.



**Table 4: The sequential cleaning and etching procedure. A DI water rinse is performed between each process step, except between HF dip (step 2) and Sopori etch (step 3).**

Step number	Chemical	Composition	Temperature	Time
1	RCA	1 vol. H <sub>2</sub> O <sub>2</sub> (30 %) 1 vol. NH <sub>4</sub> OH (29 %) 5 vol. DI water	70 °C	10 minutes
2	HF dip	5 % HF	25 °C	30 seconds – 2 minutes
3	Sopori	36 vol. HF (49 %) 15 vol. CH <sub>3</sub> COOH (glacial) 2 vol. HNO <sub>3</sub> (70 %)	25 °C	20 or 30 seconds
4	RCA	1 vol. H <sub>2</sub> O <sub>2</sub> (30 %) 1 vol. NH <sub>4</sub> OH (29 %) 5 vol. DI water	70 °C	10 minutes

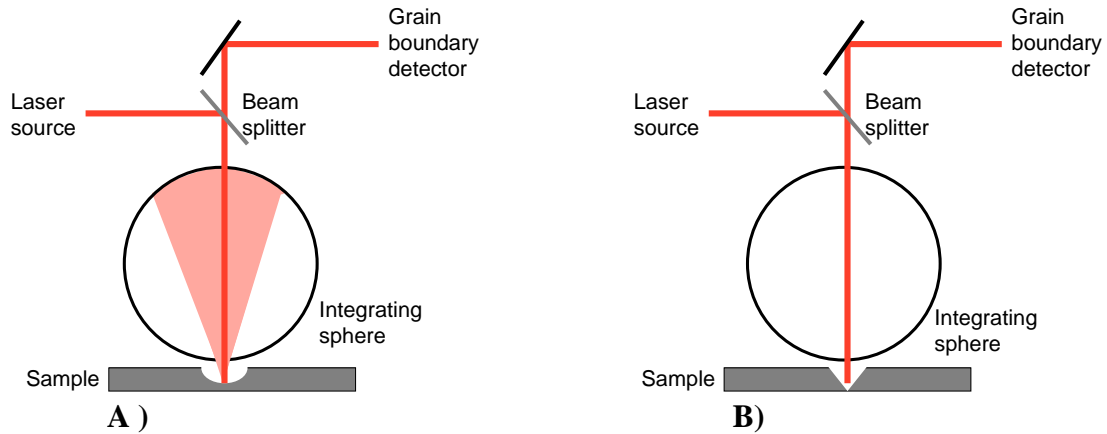
A comparison between wafers etched 30 or 20 seconds in Sopori have shown that the etch pits produced by 30 seconds etching are somewhat too big for some applications. While investigating areas with high dislocation density, these pits grow into each other and it is difficult to count them and to distinguish closely spaced dislocations. Etch pits generated by 20 seconds Sopori etch are in general smaller in diameter. While etch pits produced by 20 seconds in Sopori etch have a size from approximately 3  $\mu\text{m}$  in diameter, the pits from a 30 seconds Sopori etch can have a diameter greater than 6  $\mu\text{m}$ .

Using Sopori etch to reveal dislocations is a well known and well working technique, but care must be taken if the samples are to be analysed by use of PVScan. A bluish thin oxide layer does sometimes form on the surface of an etched wafer. This happens when the Sopori etch used is not fresh. The bluish layer might influence the reflection of the laser beam. A more serious problem is when wafers are not cleaned and dried in a proper way after etching. If an acid- or water droplet sticks to the wafer surface after etching and cleaning, and it is let there to air dry, spots from the droplet will form on the wafer surface. This influences the PVScan measurements as the spots will be counted as dislocations. To avoid this, a spin drier can be used, or the wafers can be washed in ethanol before blow-dried.

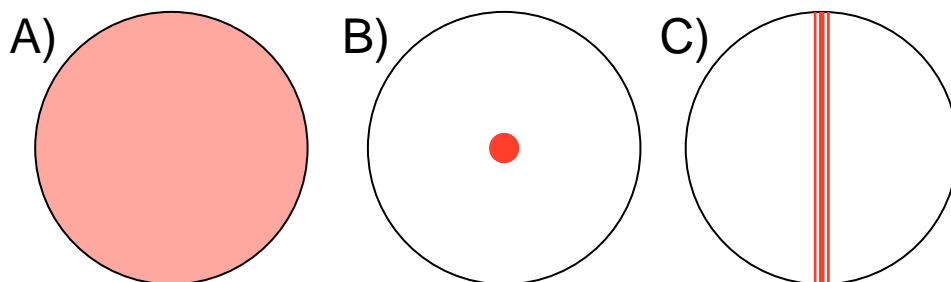
#### 5.1.4 Detection of dislocations by PVScan

Measuring the density of dislocations and grain boundaries using PVScan 6000 (Scanning Defect Mapping System) is based on light reflected from a polished and etched wafer surface [123], as illustrated in Figure 23. A laser beam is scanned across the wafer with a step size down to 25  $\mu\text{m}$  while simultaneously detecting the reflected light in different directions. The method is based on the Sopori etched wafers. Light hitting a spherical dislocation etch pit will be high angle scattered, or scattered diffused, while light scattered from a v-shaped groove originated from a grain boundary will be low angle scattered. An integrated sphere detector will collect the diffuse scattered light whereas the low angle scattered light is detected by another detector. In this way, dislocation and grain boundaries can be distinguished and measured separately simultaneously.

It is shown by Stokkan (2006) [124] that twins located close to each other will cause an interference pattern which scatters light with a high angle in certain directions, creating an arc  $180^\circ$  to the wafer surface. This light will be detected by the integrated sphere detector and twins will thus be measured as dislocations, see Figure 24.



**Figure 23: Reflection of light from a wafer surface, polished and etched with Sopori etch. A) shows high angle, or diffuse, scattering from a spherical dislocation etch pit whereas B) shows low angle scattering from a v-shaped groove originating from a grain boundary.**



**Figure 24: The integrating sphere seen from above. Reflected light is described with red colour. A) shows the diffuse scattered light caused by spherical dislocation etch pits, B) shows the low angle scattered light from a v-shaped groove which is caused by an etched grain boundary and C) shows the diffraction pattern caused by etched multiple twins.**



## 6 Recombination and trapping

### 6.1 Recombination

Recombination refers to the loss of free carriers by a number of mechanisms where a free carrier recombines with a carrier of opposite charge. The mechanisms are the radiative recombination which is just the reverse of the absorption processes, the Auger recombination process where the electron recombining with a hole and gives its excess energy to a second electron instead of emitting light and Shockley-Read-Hall recombination which will be treated later in this chapter. The other two mechanisms will not be treated here.

The recombination rate,  $R$ , is correlated to the minority carrier lifetime for electrons,  $\tau_e$ , and holes,  $\tau_h$ , by the equations 16 and 17, respectively.

$$16 \quad \tau_e = \frac{\Delta n}{R}$$

$$17 \quad \tau_h = \frac{\Delta p}{R}$$

$U$  is the recombination rate,  $\Delta n$  is the number of excess electrons in the conduction band compared to the equilibrium thermal value and  $\Delta p$  is the number of holes in excess in the valence band, also compared to the to the equilibrium thermal value. Recombination can take place at the surfaces or in the bulk, and the total carrier lifetime,  $\tau_{total}$ , is given by 18:

$$18 \quad \frac{1}{\tau_{total}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}}$$

To get information about bulk properties by lifetime measurements, it is according to equation 18 important to eliminate the contribution from the surface recombination. The thinner a sample is, the more dominant will the surface recombination be, due to equation 19.

$$19 \quad \tau_{surface} = \frac{W}{2S}$$

$W$  is the wafer thickness, and  $S$  is the surface recombination velocity which is given by equation 20.

$$20 \quad S = \sigma_s v_{th} N_s$$

$\sigma_s$  is the capture cross section of the surface states,  $N_s$  is the number of surface states and  $v_{th}$  is the mean thermal velocity for the carriers.

When bulk lifetime in a wafer is to be measured, the contribution from the surface term must be eliminated. There are in principle two routes for reducing the surface recombination velocity [125]:

- (i) Reducing the density of surface states,  $N_s$ , which act as recombination sites or the capture cross section,  $\sigma_s$ , of the surface states. The density of surface states can be drastically reduced by deposition or growth of an appropriate passivation film on the semiconductor surface (such as formation of  $\text{SiO}_2$  layer by thermal oxidation) or by immersing the sample into polar liquids (for example by an alcoholic iodine solution [126])
- (ii) Reducing the charge carrier density at the surface by implementation of a doping profile below the silicon surface such as the back surface field (BSF) produced by an aluminium back contact or by field effect passivation due to electrical charges in an overlying insulator, such as silicon nitride.

Both of these methods, and often a combination, are widely employed in the silicon solar cell industry and research, and are referred to as surface passivation. An example where both effects are employed simultaneously is the plasma enhanced chemical vapour deposition (PECVD) of silicon nitride where a field-effect passivation is provided by positive interface charges and at the same time, the number of surface states are reduced [127].

### 6.1.1 Shockley-Read-Hall (SRH) recombination

By far the most important recombination processes in indirect semiconductors are those which involve trap states in the band gap [128], see Figure 25. Dislocations and impurities will in most cases introduce trap states in a semi conductor. This effect was described by Shockley, Read and Hall as early as in 1952 [129], [130].

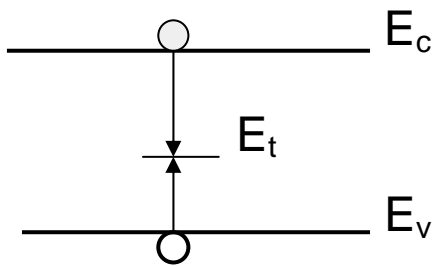


Figure 25: Shockley Read Hall recombination

The net rate of SRH-recombination is given by equation 21.

$$21 \quad U_{SRH} = \frac{np - n_i^2}{\tau_{n,SRH}(p + p_t) + \tau_{p,SRH}(n + n_t)}$$

$n$  and  $p$  is the number of electrons and holes respectively,  $n_t$  and  $p_t$  denotes the electron and hole density in a trap and  $n_i$  is the intrinsic carrier concentration.  $\tau_{n,SRH}$  and  $\tau_{p,SRH}$  are the lifetimes for electrons and holes respectively in a trap and is defined by equations 22 and 23:

$$22 \quad \tau_{n,SRH} = \frac{1}{v_{th,n} \sigma_n N_t}$$

$$23 \quad \tau_{p,SRH} = \frac{1}{v_{th,p} \sigma_p N_t}$$

where  $v_{th,n}$  and  $v_{th,p}$  are the mean thermal velocities for an electron and a hole,  $\sigma_n$  and  $\sigma_p$  are the capture cross sections of the trap for electrons and holes, respectively, and  $N_t$  is the number of traps.

### 6.1.2 Recombination activity of contaminated dislocations in silicon

Dislocations can act as gettering sites for impurities, and dislocations will very often be decorated by impurities. Decorated dislocations are often reported to be considerably more harmful to the minority carrier lifetime than clean dislocations. Kveder et al. (2001) [131] proposed the following model to explain this effect.

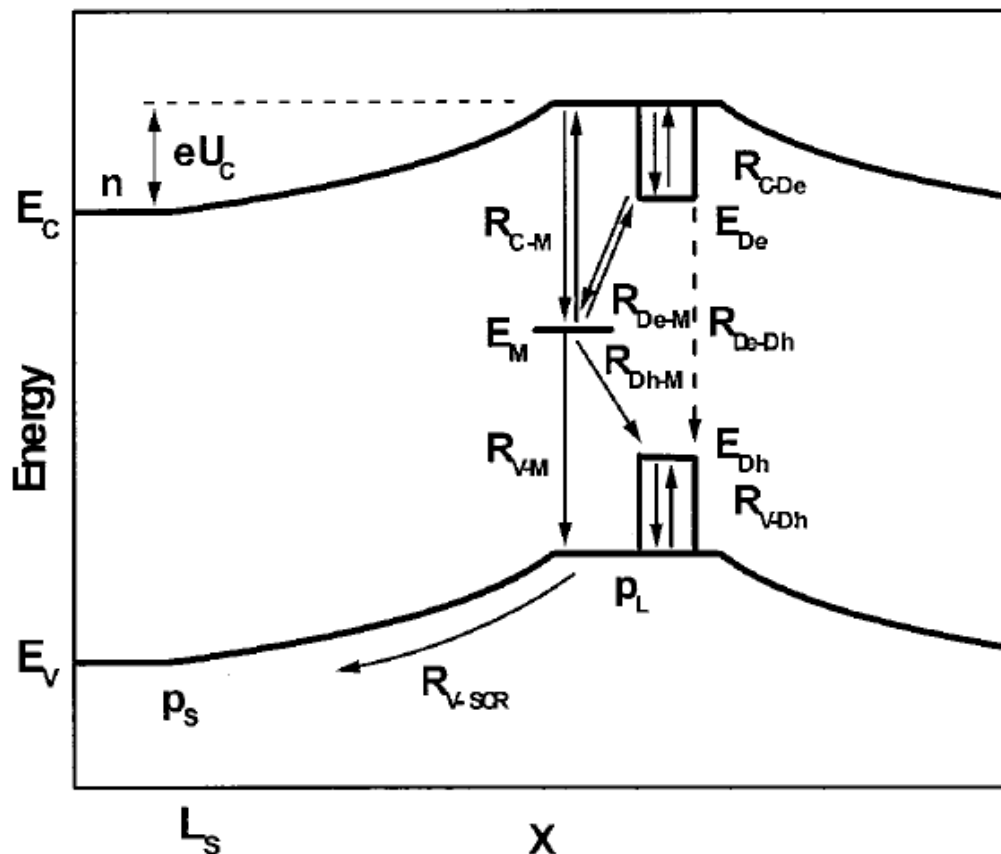


Figure 26: Charge carrier recombination on dislocations. For clean dislocations, the recombination rate is determined by direct recombination of electrons and holes captured by  $E_{De}$  and  $E_{Dh}$  respectively. If a deep energy level,  $E_M$ , is present, the electrons and holes can recombine via this deep level. The figure is taken from [131].

Figure 26 shows a schematic presentation of a negatively charged dislocation containing a metal impurity (like Cu, Fe, Ni etc.) and  $eU_c$  is indicating the Coulomb potential of the dislocation charge. According to theory, relatively shallow one-dimensional energy levels are associated with the strain field surrounding a dislocation. These are shown as  $E_{D_e}$  and  $E_{D_h}$  in the figure. The radii of the wave functions of electrons and holes captured in these shallow traps are larger than the dislocation core. The overlap of the wave function of the deep level and those of the bands  $D_e$  and  $D_h$  initiates a recombination channel.

In this electron-hole recombination process suggested by Kveder, the capture of carriers at the energy bands,  $D_e$  and  $D_h$ , are the first step. According to their experimental data (from Electron Beam Induced Current (EBIC) measurements), the contrast of clean dislocations are very small: less than or about 0.5%. They assumed therefore that direct recombination between  $D_e$  and  $D_h$ ,  $R_{D_e-D_h}$ , is quite small in silicon.

Consider n-type silicon; holes will be minority carriers and dislocations will be negatively charged, as indicated in the figure. The total recombination rate,  $R_T$ , of charge carriers at the dislocation is given by equation 24.

$$24 \quad R_T = R_{D_h-M} + R_{V-M} + R_{D_e-D_h}$$

The transition between the deep levels and conduction or valence band,  $U_{V-M}$ , is equivalent to what is described for SRH-recombination, except for that the Coulomb potential, which is negative for electrons and positive for holes in this case, must be included.

Capture of free electrons and holes by the  $D_e$  and  $D_h$  bands, respectively, and their re-emission are considered as competitive processes to the direct recombination by deep levels, that is, the SRH-recombination.

The recombination step following the capture of carriers in  $D_e$  or  $D_h$  bands can occur either by direct electron transition from  $D_e$  to  $D_h$ , or via deep acceptor states  $M$  at  $E_M$  localised in the extended core region. As mentioned above, the direct recombination rate,  $R_{D_e-D_h}$  is small in silicon, and can in most cases be neglected. The transmission of holes from the  $D_h$  band to negatively charged impurity atoms can be described by equation 25

$$25 \quad R_{D_h-M} = A_h v_{D_h} n_M p_{D_h}$$

Where  $v_{D_h}$  is the thermal velocity of holes in the  $D_h$  band,  $A_h$  is a capture parameter,  $n_M$  is the number of captured electrons in  $M$ , and  $p_{D_h}$  is the number of captured holes in  $D_h$ .

The values of the capture parameter  $A_h$  and its equivalent parameter for transmission between  $D_e$  and  $M$ ,  $A_e$ , are given by the equations 26 and 27, respectively.

$$26 \quad A_h = \frac{\alpha \sigma_h}{\pi r_{D_h}^2}$$

$$27 \quad A_e = \frac{\alpha \sigma_e}{\pi r_{D_e}^2}$$

$\alpha$  is a dimensionless fit parameter,  $\sigma_h$  and  $\sigma_e$  are the respective capture cross-sections for holes and electrons,  $r_{Dh}$  and  $r_{De}$  are radii of the wave functions of holes and electrons in their respective D-bands, for which [131] assumes  $r_{De} \approx r_{Dh} \approx 2$  nm. The fit parameter  $\alpha$  may be considered as a measure of the overlap between the electronic wave function of the deep impurity level with those of  $D_e$  and  $D_h$ .

The effect that metallic impurities have on the recombination rate between the shallow dislocation bands  $D_e$  and  $D_h$  is thus described in this model by the number of deep level states localised in the extended core region,  $N_M$ , and their energy,  $E_M$ , as well as  $\alpha$ ,  $\sigma_h$  and  $\sigma_e$  which are dependent on the type and spatial location of impurity atoms decorating the dislocation.

Experimental data shows that for strongly decorated dislocations with  $N_M = 3 \cdot 10^7 \text{ cm}^{-1}$ , even with small overlap of deep energy states with the shallow dislocation bands ( $\alpha \ll 1$ ) the capture of carriers from the D-bands to the deep impurity level gives a significant contribution to the recombination, see Figure 27.

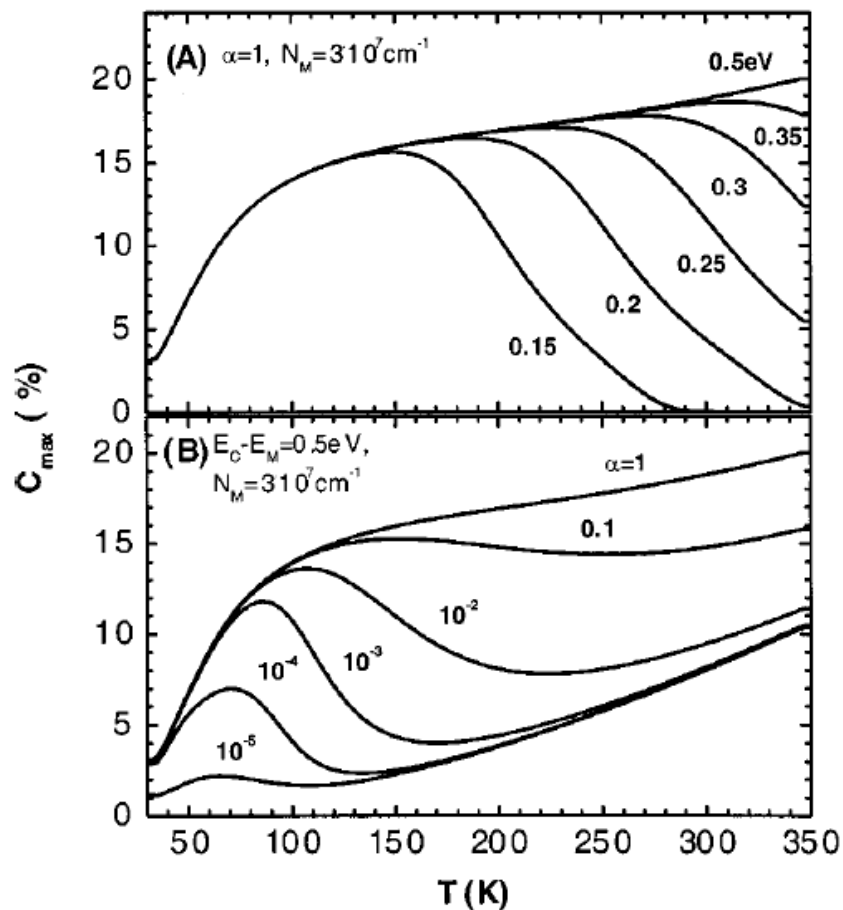


Figure 27: Calculations showing the EBIC-contrast for dislocations as function of temperature. Capture cross sections are  $\sigma_h = 10^{-14}$  and  $\sigma_e = 2 \cdot 10^{-15}$ .  $\sigma_h$  has a higher value than  $\sigma_e$  because it corresponds to the capture of a hole by a negatively charged impurity, while  $\sigma_e$  corresponds to the capture of an electron by a neutral atom. (A) shows  $C_{\max}(T)$  calculated for  $\alpha = 1$ , a doping concentration of donors,  $N_d = 10^{15} \text{ cm}^{-3}$ , free hole concentration (minority carriers),  $p = 10^{13} \text{ cm}^{-3}$ , and with different values of  $E_C - E_M$  written for each curve. (B) shows  $C_{\max}(T)$  calculated for different values of  $\alpha$  (written on each curve) and a fixed value of  $E_C - E_M$  at 0.5 eV. The other parameters are as for (A). The figure is taken from [131].



### 6.1.3 Trapping

Trapping is a non-recombinative process where carriers are trapped in shallow energy levels in the band-gap for a limited time before they are released, as shown in Figure 28.

An undesirable effect of trapping is the apparent increase in minority carrier lifetime during many forms of measurements. The lifetime measurement methods measure the decay of the minority carrier concentration after illumination. The decay can be considerably slower due to trapping, and the measured lifetime will increase correspondingly. While trapped, the carriers will not contribute to the solar cell current, and therefore the measured lifetime must be corrected for trapping. This can be done by calculations [132] or by conducting the measurements under high injection or with bias lighting. During high injection the traps will be saturated with carriers, and the impact on the measurements will be minimal. Since the minority carrier lifetime is dependent on injection level, and since solar cells normally operate under low injection, it is not always desirable to conduct measurements under a high injection level.

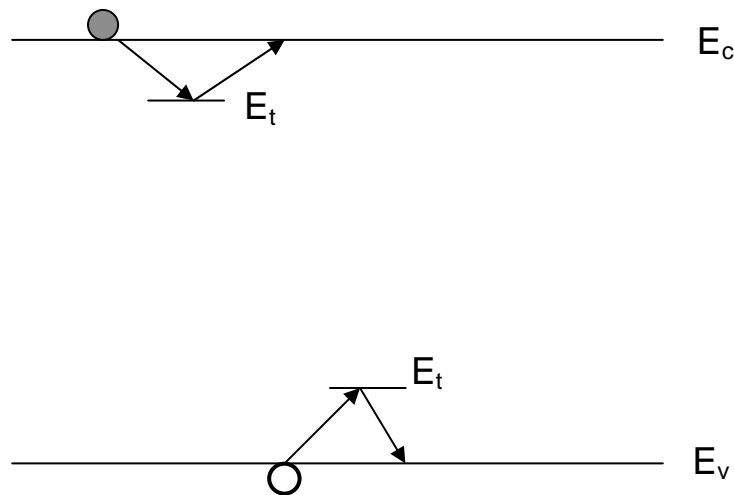


Figure 28: Schematic drawing of the trapping process in a semiconductor, with  $E_c$  denoting the conduction band level,  $E_v$  the valence band level and  $E_t$  is denoting the trap levels.

## 6.2 Measuring minority carrier lifetime

Measuring of the minority carrier lifetime in silicon blocks and wafers is extremely important for process control and material and device-physics research. It is possible to measure the lifetime in steady state or in non-steady state conditions. In non-steady state, the injection level varies with time and a time constant of the variation is measured. In steady state measurements, the generation rate is equal to the recombination rate, and for a known generation level lifetime can be calculated from measurements of the injection level. Three methods that are used in the study included in this thesis are shortly presented in the three following subsections.

### 6.2.1 Quasi Steady State Photo Conductance (QSSPC)

The QSSPC method is perhaps the best option for approaching the steady state conditions, and has been so since it was published by Sinton et al. in 1996 [133]. Today the QSSPC is considered a standard tool for steady state measurement with low spatial resolution. The photo conductance given by equation 28 is as measured by a coil.

$$28 \quad \sigma_{ph} = q\Delta n(\mu_n + \mu_p)W$$

The  $\sigma_{ph}$  is the measured photo conductance,  $\Delta n$  is the excess carrier density,  $W$  is the sample thickness and  $\mu_n$  and  $\mu_p$  are the electron and hole mobility respectively. The mobilities are functions of doping and injection level and can be found in the literature. Microstructures, such as high dislocation density, can also influence the carrier mobility.

The light source is a slowly (compared with the minority carrier lifetime) decaying intensity flash lamp with a decay constant of about 2 ms [132], and the photo conductance is logged as a function of light intensity. This gives the lifetime as a function of excess carrier density which is the injection level, see Figure 29. Since the variation in light intensity, and thus in injection level, is slow compared to the lifetime, every point in the measurement is approaching steady state conditions, and can be considered steady state, thus the name; *quasi steady state*.

Seemingly high lifetime at low injection level can be due to trapping as described earlier. At higher injection levels, all traps are occupied, and the trapping does not effect the lifetime measurements. If a sample contains too many trapping states, bias light can be used to saturate the traps [134].

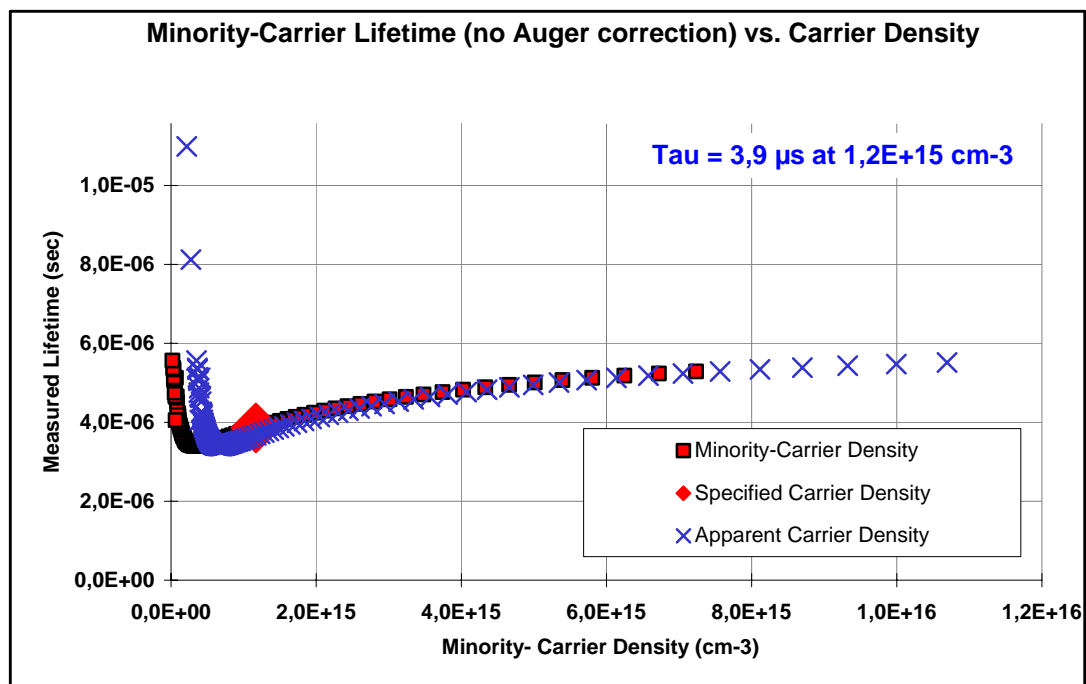


Figure 29: The lifetime as function of excess carrier density as measured by QSSPC

### **6.2.2 Microwave Photo Conductance Decay ( $\mu$ -PCD)**

The  $\mu$ -PCD is a non-steady state method. It measures the time constant of the decay in conductivity after a short, abrupt light pulse. It is often used in scanning mode resulting in lifetime maps. The resolution is limited by the laser used to inject carriers' spot size. The measurements are done by a microwave antenna creating microwave signals that are reflected by the sample and subsequently detected by the same antenna. Microwave reflection is proportional to the conductivity, and the minority carrier lifetime can be calculated from the decay in ion conductivity.  $\mu$ -PCD measurements are mainly performed in high injection since the signal otherwise is very small.

### **6.2.3 Carrier Density Imaging (CDI)**

CDI is a steady state measurement where the wafer is placed on a hot plate and the carriers are induced by homogeneous illumination of the wafer by a pulsed laser. The pulse frequency is so slow that true steady state is achieved during measurement. The infrared (IR) light from the hot plate is transmitted through the wafer and is detected by an IR sensitive digital camera. The IR transmittance in Si is dependent on minority carrier density, and the difference between the images given under illumination and under dark conditions will thus give the minority carrier density. CDI can operate with low injection levels.

## 7 Conclusions of the publications

### 7.1 Casting

- Understanding and controlling the properties of crucible coating and the temperature profile at the point of crystal nucleation is crucial in order to obtain a good material quality in directionally solidified ingots. Differences in cooling rates after solidification have probably a lesser impact.

### 7.2 Characterisation of SoG-Si multicrystalline wafers made from metallurgically refined material

- Small (2-3  $\mu\text{m}$ ) particles containing carbon and dislocation clusters are found unevenly distributed in the ingot made from SoG-Si. The dislocation densities within the clusters as well as particle density are increasing with increasing height in the ingot. The particle density is higher in areas with dislocation clusters than in areas with few dislocations. Finally, the particle density varies in twinned areas and is considerably higher in twinned areas containing dislocations than in twinned areas with no or very few dislocations.
- Metal impurities are found as micrometre size co-precipitates in the top of the ingot.
- The minority carrier lifetime is 10  $\mu\text{s}$  at injection level  $10^{15} \text{ cm}^{-3}$  in wafers from the middle of the ingot made from SoG-Si. This is a typical value for multicrystalline silicon. This is normally considered to be enough to collect minority carriers from the whole cell volume.
- A short comparison of wafers obtained from SoG-Si and commercially available wafers indicates that the microstructure is more influenced by the solidification conditions than by the assumed higher impurity level in the SoG-Si.
- If the Si feedstock is purer than a certain level, the microstructure is more important for the final cell efficiency than the exact impurity level. SoG-Si from Elkem Solar is shown to be of a purity level where the microstructure, rather than the impurities, affects the efficiency the most for the solar cell processing procedure investigated here.

### 7.3 Dislocation clusters

- The dislocation clusters are estimated to cover up to 5–10% of the wafer surfaces investigated.
- The clusters have a dislocation density that varies from  $10^6$ – $10^8 \text{ cm}^{-2}$ .

- The cluster size varies from 100–1000  $\mu\text{m}$ .
- The clusters are found more frequently in the upper parts of an ingot than in the lower parts.
- Dislocations in the clustered areas tend to align and form sub-grains
- A few large (100  $\mu\text{m}$ -size) carbon containing particles have been found in connection with dislocation clusters
- Some large (100  $\mu\text{m}$ -size) nitrogen containing particles have been found, but not in connection with dislocation clusters
- The majority of the dislocations found in multicrystalline silicon ingots are probably nucleated during crystal growth.
- In general it has been observed that samples cut parallel to the solidification direction in a directionally solidified multicrystalline silicon ingot are found to have a lower dislocation density than the wafers which is cut perpendicular to the solidification direction.
- Dislocations are nucleated at grain boundaries. The following mechanism for dislocation cluster growth in directionally solidified multicrystalline silicon is suggested:
  1. Dislocations are nucleated at a grain boundary that has an acute angle to the solidification front
  2. The dislocations can glide in the slip planes under stresses produced during the solidification
  3. Dislocations will be attracted to the solid-liquid interface due to the image forces
  4. In  $\{1\bar{1}0\}$  planes being normal to the solid liquid interface, slip on the  $\{1\bar{1}0\}\langle 110\rangle$  systems must be allowed. The  $\{1\bar{1}0\}$  planes are the only possible slip planes normal to the solid liquid interface, allowing the minimizing of energy according to point 3.
  5. Dislocations moving in slip planes normal to the solid liquid interface may act as Frank-Read sources. These dislocations will be observed as lines of etch pits parallel to the  $\{1\bar{1}0\}$  traces on an etched wafer cut normal to the solidification direction.
    - Slip on the  $\{1\bar{1}0\}\langle 110\rangle$  system and single ended Frank-Read sources explains the dislocation pattern where dislocations are lining up perpendicular to  $\{111\}$  traces.
    - Dislocations seek to minimise its energy by cross-slipping in such a manner that it meets the solid liquid interface at an angle close to  $90^\circ$ . This mechanism explains why samples cut parallel to the growth direction generally shows a lower dislocation density than wafers cut perpendicular to the growth direction, and that grains filled with dislocations in the samples cut parallel to the growth direction is V-shaped.

## 8 Suggestions for further work

### 8.1 *Characterisation of SoG-Si*

To get a better understanding of the limitations given by impurities in silicon feedstock, SoG-Si with known impurity content should be systematically characterised and compared with traditional silicon feedstock, also with known impurity content.

Casting methods with a higher sensitivity for impurities, such as Cz-pulling, could be tested.

A solar cell process with higher demand to material quality (e.g. back contact cell) could be applied.

### 8.2 *Dislocation clusters*

Due to the suggested nucleation and crystal growth mechanisms that can produce ingots that are either dominated by dislocations or twins, efforts should be made to be able to control the nucleation phase of the directional solidification. It is not understood why some ingots experience a higher undercooling before solidification starts, but a correlation with the coating quality is suggested. It is suggested that the coating can be of such character that nucleation is difficult, and hence a high undercooling is obtained. If the coating possesses other characteristics, many nucleation sites might be present, and a random nucleation will occur before a high undercooling is achieved.

Investigations focusing on the nucleation phase should therefore be performed. How  $\text{Si}_3\text{N}_4$  is wetted by the silicon melt is essential. How the particle size, coating thickness and coating homogeneity will influence the wetting properties, and how this will affect the crystal nucleation. Effort should be made to develop a procedure for coating where the desirable coating characteristics are obtained and thus produce only ingots dominated by twins.

It is concluded in this thesis that dislocations will nucleate at grain boundaries, but which nucleation mechanism is the dominant, is not yet known. Search for precipitates at the grain boundaries can be done by Energy dispersive spectroscopy (EDS) and transmission electron microscopy (TEM). Modelling of the strains at different grain boundaries and grain arrangements could also be done.

The suggested slip on the  $\{1\bar{1}0\}\langle 110\rangle$  system should also be more thoroughly investigated, preferably by TEM.



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