Modelling and Quantification of Power Losses Due to Dynamic On-State Resistance of GaN E-mode HEMT

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***Abstract*—This paper investigates a method for quantifying the additional losses in high-voltage GaN enhancement mode HEMTs (eHEMT) employed in converter applications. The additional losses stem from the phenomenon known as current collapse or dynamic on-state resistance. The goal of this work is to investigate how these losses contribute to the total power loss in converter application. Measurement and modelling methods in the literature are reviewed. Changes to the measurement circuit are made to improve measurement accuracy. Measurements of dynamic on-state resistance are made on a commercial GaN eHEMT. The experimental results shows that the resistance depends on both dc-link voltage and blocking time. The resistance waveform and initial attempts at modelling the dynamic on-state resistance indicate that the suggested model is suitable for modelling the losses in LTSPICE software.**

I. Introduction

Due to the high importance of energy efficiency in electric power converters and the increasing maturity of the manufacturing technology, the interest in using GaN transistors in industrial applications is increasing. GaN-on-Si substrate HEMTs are highly attractive to the power electronics industry due its favourable characteristics. Enhancement mode devices (eHEMT) have a design that give them a normally-off behaviour. In addition, they have low on-state resistance and fast switching characteristics. The introduction of new packaging with lower stray inductance allows for further development of compact power conversion systems using these new components. On the other hand, charge trapping phenomenon in the HEMT structure that negatively affects the device performance have been documented [1], [2]. The phenomenon is known as current collapse or dynamic on-state resistance (dynamic $R_{DS,on}$) leading to increased on-state resistance in the GaN HEMT channel. The increase in on-state resistance is highest immediately after the device is turned on and it returns to the rated resistance value after a certain time period. The magnitude and time constant of the increase has been shown to be dependent on both device design and operational parameters [2], [3], [4], [5].

While the mechanism behind current collapse and possible design to minimize the effect are being investigated, a design engineer would need to know what the additional contribution of the effect would be. Previously, the active device loss calculation would consist of conduction losses and switching losses, the latter in the context of hard switched applications. The dynamic $R_{DS,on}$ adds a loss component which currently is not accounted for during the design phase. There are several authors who have investigated the phenomenon with operation parameters close to that in actual application [2], [3], [4], [5], [6], [7], [8]. Examples of operation parameters include bias voltage, device blocking time, current, and temperature variation.

This paper contributes to the ongoing investigations of dynamic on-state resistance of GaN eHEMTs. A state-of-the-art setup is made to measure the dynamic on-state resistance while varying the operational parameters of a commercial GaN eHEMT device. Based on the experimental results, suggestions are made regarding modelling the experimental results in the LTSPICE software. The existing literature is studied and a suitable model is proposed. The final goal is to investigate the loss component caused by dynamic on-state resistance to quantify these losses during converter operation.

The paper is organized as follows. In Section II, models of current collapse at device level from the literature are presented and discussed. Section III describes the experimental setup and the measurement results are shown in Section IV. The suitability of the model is discussed and the conclusion and outlook are presented in Section V.

II. Modelling of Dynamic On-State Resistance

There are several articles that model current collapse in normally-off GaN HEMTs to investigate the switching behaviour. Common for all models is the need for a transistor model that is unaffected by current collapse, i.e. a model based on quasi-static I-V characteristics. Böcker et al [9] use RC models in a detailed device model to accurately model the I-V characteristics of their in-house developed GaN HEMT. Li et al in [8] measure the dynamic on-state resistance of a commercial device and implements a model of the increased resistance by manipulating the gate voltage. In turn, the on-state resistance is changed according to the device transconductance. The model was implemented in a SPICE environment. Although

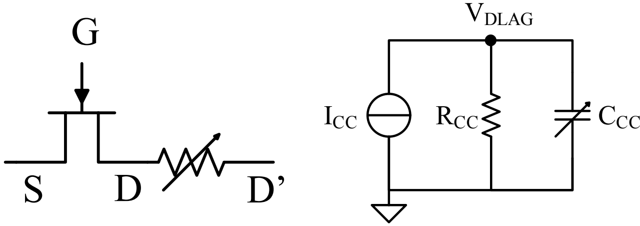

Fig. 1. GaN eHEMT model to model dynamic $R_{DS,on}$. The value of R between D and D' depends on the voltage V_{DLAG}.

changing the gate voltage is a pragmatic approach, it is unclear how well suited multiplying an exponential model with the transconductance of the transistor is to model the trapping effect. An alternative model is presented in [3] where variable resistors are used to model the change in channel resistance. This model assumes that the traps are in the regions affecting gate-source and gate-drain conduction. The model is implemented in Verilog-A. The trapping phenomena at interfaces in the bulk material are modelled as RC-circuits. However, the proposed model does not allow for different time constants for charging and discharging. The experimental results in [8] indicate that such a difference exists.

From the published measurements on dynamic on-state resistance, the resistance appears to have the form of a exponential decay after turn-on. From the three briefly presented models, the model from [3] shows promise in several aspects. The model is based on RC circuits that would be well suited to model the time dependent characteristic of the resistance. Moreover, multiple series-coupled RC elements can be added, each with a variable capacitor to allow for detailed modelling. Implementation of such a model in LTSPICE is achievable. Furthermore, many manufacturer provide SPICE models of their components which are unaffected by trapping behaviour, which is a prerequisite for the model. A simplified version of that model is shown in Fig. 1. The variable part of the on-state resistance between D and D' is dependent on the voltage, V_{DLAG}. The current, I_{CC}, is a function of the drain-source voltage. The use of a variable capacitor is a modification suggested in this paper. By making the capacitor, C_{CC}, variable, influences from operational parameters on the device charge trapping can be included in the model. However, the change in dynamic on-resistance must first be investigated experimentally to establish the dependency on operational parameters. Consideration for test circuit and measurement accuracy to obtain such experimental data is described in the following section.

TABLE I
MEASUREMENT PROBES FOR THE EXPERIMENTAL SETUP.

Measurement	Probe
V_{meas} - LV diff. probe	TDP0500
V_{meas} - HV diff. probe	THDP0200
I_{load}	TCP0030
V_m	TPP1000

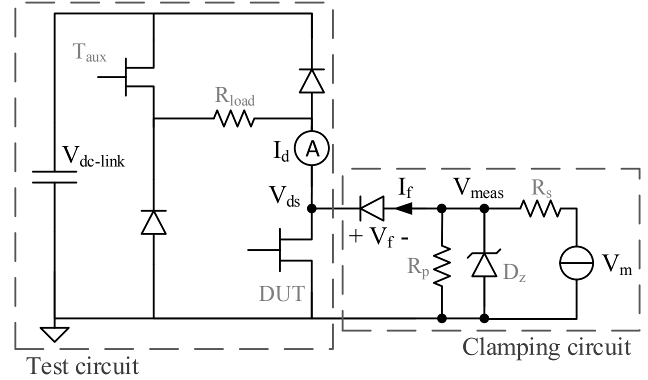

Fig. 2. Schematic diagram of the test and clamping circuit.

III. Experimental Setup

One major challenge in measuring on-state resistance of high voltage switching devices is obtaining a good measurement sensitivity of V_{DS} during the on-state. The voltage difference between on-state and off-state can be several hundred volts. If the oscilloscope is setup to include the signal at hundreds of volts during the off-state, the signal will be noisy during on-state when the voltage is only a few volts or less. If the the oscilloscope is set up to measure only a few volts, the off-state voltage will be clipped. In the worst case the measurement equipment is damaged. Even if no damage is done, the oscilloscope amplifier will be saturated and the measured signal cannot be trusted. Hence, there is a

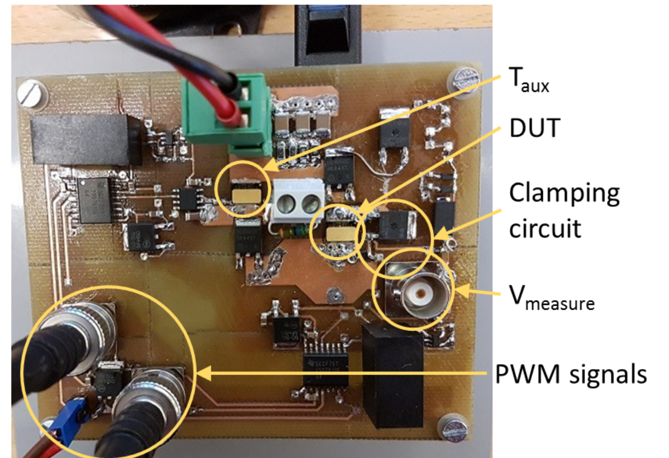

Fig. 3. Photo of the experimental setup for measuring dynamic on-state resistance.

need for a clamping circuit on the device under test (DUT) to precisely measure the on-state voltage. The goal of the clamping circuit is to keep the voltage at approximately the same magnitude during both on and off state while at the same time allow for accurate measurement of the on-state voltage. Several circuits for high accuracy measurement of dynamic on-resistance are suggested in the literature [4], [6], [8], [9], [10]. A comparison of the circuits is presented in [11]. The recommended clamping circuit in [11] was selected and modified for the investigations in this paper. A schematic of the clamping circuit is seen in Fig. 2. The task of the Zener diode in the clamping circuit is to limit the measured voltage during the off-state. If the voltage difference between off and on states is small, the oscilloscope gain is maximized. If the difference is large, a smaller oscilloscope gain must be used to avoid above mentioned problems of clipping and amplifier saturation. With a larger oscilloscope gain, a wider band of the oscilloscope analogue to digital converter range is used which leads to higher resolution and lower noise-to-signal ratio. A resistor is added to the clamping circuit in parallel with the Zener diode (R_p). By using the resistor R_p, the off-state clamping voltage can be finely tuned close to the expected measurement voltage during DUT on-state and the oscilloscope sensitivity is maximized. With the added resistor, the Zener diode operating point is far from its avalanche state. The Zener is kept in the circuit to allow a low impedance path for the discharging of the blocking diode. The value of R_p is chosen so that the voltage difference between on and off state is minimized. The value of R_s is chosen to obtain the desired I_{meas} during DUT on-state.

In addition to the clamping circuit, a suitable test circuit must be chosen for switching the DUT and passing current through it. In test circuits with inductive load, a double pulse testing scheme is employed to test at specific load currents. The load current is established by turning on the DUT and charging the load inductor to the target current. During this time the DUT will experience self-heating. In the following off-period, the current falls according to the resistance in the freewheeling path. Simultaneously, the bias voltage of the dc-link leads to charge trapping in the GaN eHEMT structure. Hence, it is of interest to vary the blocking time when investigating the dynamic on-resistance. If long blocking times are desired, then either a large inductance must be chosen or the inductor current can be overcharged to allow for a longer off time. Either case results in increased self-heating of the DUT. If a resistive load is chosen, long off and on times can be tested without increasing the effect of self-heating. Thus, a resistive load allows for resistance measurements over longer time periods with constant current which in turn allows for detailed investigation of longer trapping time constants in the device. In contrary to inductive loads, the switching losses are lower with a resistive load. This could potentially change the trapping behaviour, as hot electrons during this high power state have been shown to contribute to the increased on-state resistance [12]. Also, inductive load is closer to application for most hard switched applications.

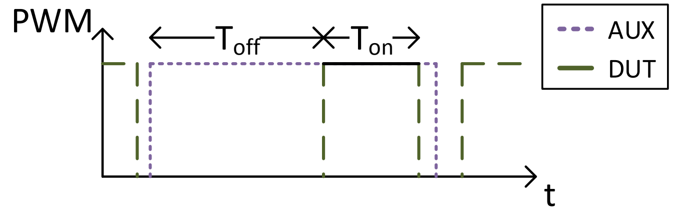

Fig. 4. Timing diagram for switching the auxiliary switch and DUT.

The test circuit in this work was taken from [8] since it allows for precise control of both trapping and detrapping time. The circuit employs a resistive load. The circuit schematic is shown in Fig. 2 and the setup is depicted in Fig. 3. The timing diagram in Fig. 4 shows how the auxiliary switch and DUT are controlled for measuring the dynamic on-resistance. The DUT is kept on before the test starts to discharge any charge in the DUT structure. Then, the DUT is turned-off and a short dead time is introduced between the auxiliary and the DUT before the auxiliary is turned on. The DUT is now subjected to the bias voltage for the controlled time period T_{off}. Then, the DUT is turned on and $R_{DS,on}$ is measured during T_{on}. After both switches are turned off, the DUT is again turned on until the next repetition of the test. For all operating points in this work, each test is repeated and averaged over 20 repetitions. The DUT is a commercial GaN eHEMT rated at 650V and 30 A with a typical on-state resistance of 50 $m\Omega$ at room temperature (GaN Systems GS66508T).

A. Considerations Regarding Measurement Errors

The device on-state resistance is defined as

$$R_{DS,on} = \frac{V_{DS,on}}{I_D} = \frac{V_{meas} - V_f(I_f) - V_{offset}}{I_D} \quad (1)$$

where V_{meas} is the clamped measured voltage, V_f is the forward voltage of the blocking diode, and V_{offset} is any offset voltage introduced by the measurement circuit. The equation shows that the measured voltage in millivolts results in on-resistance in milliohms divided by amperes. Furthermore, measurement error in magnitude of millivolts will potentially influence the resistance measurement. Fig. 5 shows examples of the error introduced by an offset voltage in the measurement. The effect of any fixed voltage offset decreases with increasing current. Hence, it is preferential to increase the load current in order to improve measurement accuracy. However, if the voltage offset scales with the current, the load point has less impact on the measurement error. An example of this would be incorrect estimation of V_f, which is a function of I_f that in turn changes with V_{DS}. This is illustrated in Fig. 5 with a solid line for an erroneous estimation of V_f by 3 mV per ampere.

For circuits where grounding conditions allow the use of passive probes, these are most commonly used. In switching circuits, the falling voltage transient during turn-on results

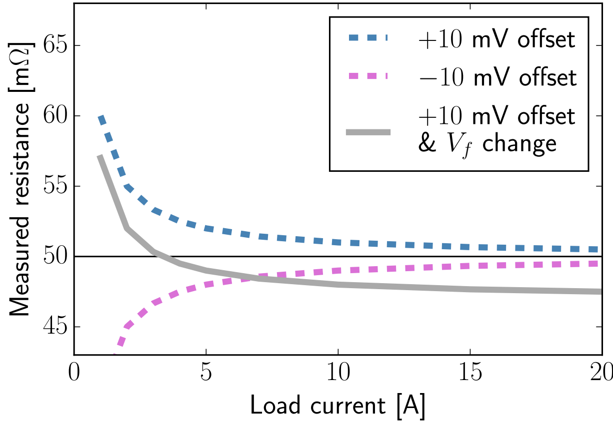

Fig. 5. Effect of measurement offset voltage on measured resistance. Example is with a 50 mΩ resistor.

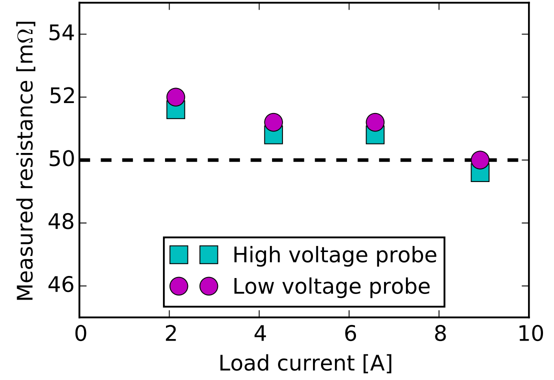

Fig. 6. Measured resistance of a 50 $m\Omega$ resistor as test object for increasing load current.

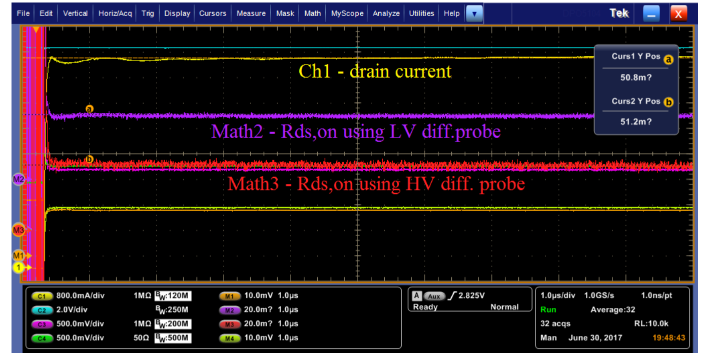

Fig. 7. Measurement of resistance of a 50 $m\Omega$ resistor over 10μs with 6.6A load current. Steady state is obtained within 200 ns.

in a common mode voltage. The probe measurement will inevitably be affected by the common mode voltage. Several actions can be taken to minimize this voltage, but the effect cannot be avoided. While passive probes are effected by common mode voltage, active differential probes provide certain immunity from common mode voltages. The probe's immunity, or common mode rejection ratio, is specified in the probe datasheet. Furthermore, passive probes are affected by the probe compensation made by the measurement setup. While these factors have little impact on measuring for instance rise and fall times, resulting error from common mode voltage and probe compensation will affect the measured resistance value, even for errors in the range of a few millivolts. Hence, using active differential probes is considered preferable while investigating the smallest time constants of the $R_{DS,on}$. Table I shows which probes that were used in the experimental setup of this work. Two different active differential probes were used for comparison. They are named according to their relative maximum voltage rating as the low voltage (LV) probe and the high voltage (HV) probe. The probes differ in several parameters. The LV probe has a bandwidth of 500 MHz, a maximum voltage rating of 42 V, has shorter leads, and has a third connection to a local grounding point. The HV probes has a bandwidth of 200 MHz, a maximum voltage rating of 1500 V, has longer leads, and only two connections for the differential measurement. Higher voltage rated probes come with a higher common mode rejection voltage. There is a concern that the LV probe could be saturated due to the switching voltage up to 400 V. The HV is hence used to verify the LV probe behaviour. The LV probe has lower attenuation, hence the noise level is expected to be lower for this probe and it is the preferred signal for calculating the DUT resistance.

As mentioned above, errors in estimating the forward voltage of the blocking diode will introduce resistance measurement error. The diode current depends on the voltage between V_{DS} and V_{meas}. As V_{DS} increases with the load current, the driving voltage for the blocking diode will decrease. If V_f in Eq. 1 is set as a constant, the mismatch between that constant and the real forward voltage will result in a measurement error. By choosing a high supply voltage for the measurement current, V_m, this effect is minimized. Alternatively, V_f can be characterised for different forward currents and the voltage estimate can be corrected accordingly. For the test results presented in this work, the forward voltage of the blocking diode was characterised with zero load current.

IV. Results

To verify the accuracy of the measurement setup, the setup was tested using a 50 $m\Omega$ resistor as DUT. The calculated resistance for several load currents is shown in Fig. 6. The calculated resistance for the LV and HV probes are separated by a small offset that likely stems from the inherent probe offset values. The results show that the clamping circuit is accurately measuring the resistance. The decrease in resistance with increasing current is due to both minimizing any offset voltage and from incorrect estimation of the blocking diode forward voltage. A screen shot of the oscilloscope image for load current equal to 6.6 A is seen in Fig. 7. The steady state resistance value is obtained within 200 ns. Using either HV or LV differential probe show very little change in measured resistance value. However, the HV probe will provide a noisier signal. The LV probe is used for the following results presented in this work.

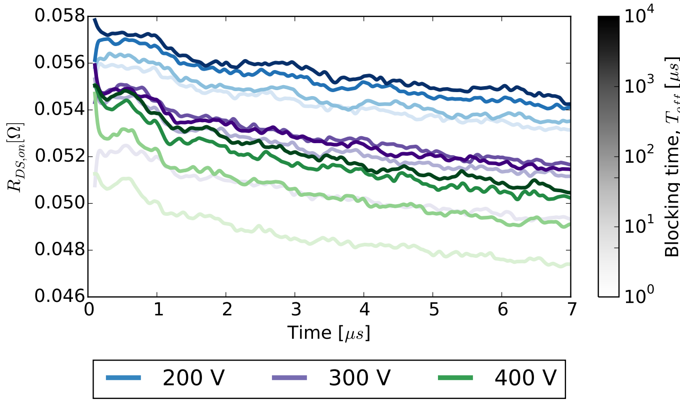

Fig. 8. Measured $R_{DS,on}$ of a commercial GaN eHEMT for 10 A load current, increasing voltage and blocking time

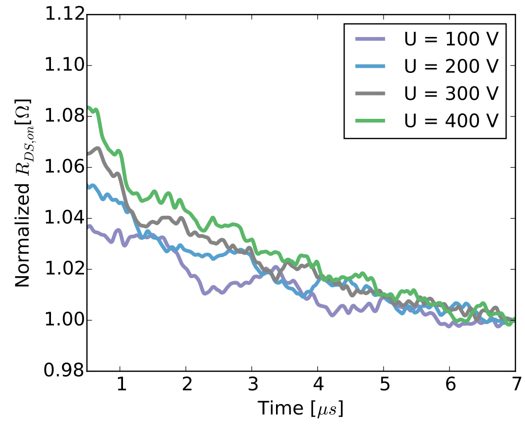

Fig. 9. Normalized resistance values with changing voltage for 10 A load current and 50 μs blocking time.

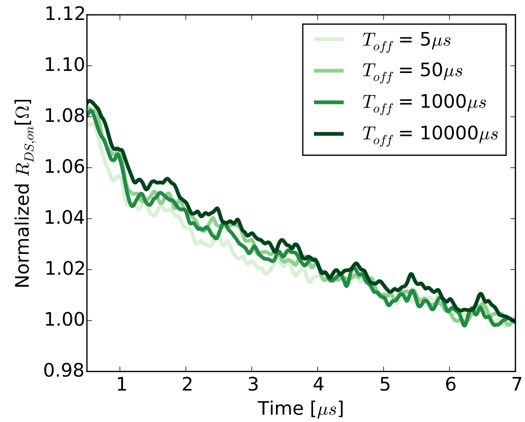

Fig. 10. Normalized resistance values with changing blocking time for 10 A load current and 400 V dc-link.

In Fig. 8 the on-state resistance measurements are shown for varying voltage and blocking time. The blocking time is varied between 5 μs to 10 ms and the dc-link voltage is varied between 200, 300 and 400 V. An increase in blocking time is observed to increase the resistance value. The magnitude of the increase appears to depend on the dc-link voltage. In contrary to other published resistance measurements, increasing dc-link voltage appears to decrease the resistance within the measured time scale of 7 μs. The reason for this shift is unknown at this point. Further testing is necessary to give confidence to the results frin this measurement setup. Future testing should include longer on-time to investigate whether the steady state resistance value decreases with increasing dc-link voltage, or if the steady state on-resistance converges to a single value for different dc-link voltages.

Moreover, a small oscillation can be observed on all of the resistance measurements. This oscillations stems from an oscillation in the load current after turn-on and follows the resistance calculation since the forward voltage of the blocking diode is set as a constant. An improvement in the estimation of the blocking diode forward voltage drop would increase the accuracy of the measurement.

To further investigate the time varying behaviour of the dynamic resistance, select signals from Fig. 8 are plotted normalized to their individual resistance value at the end of the on period. In Fig. 9, the resistance for 50 μs blocking time is plotted for different dc-link voltages. It is observed that, regardless of their absolute value after 7 μs, the difference between the starting and end values increases with increasing dc-link voltage. The shape of the resistance resembles exponential decay, hence the proposed modelling technique appears to be suitable. In Fig. 10, the resistance for 400 V dc-link and increasing blocking time is plotted. For blocking times up to 10 ms, the normalized on-state resistance is almost unchanged. This is in line with other published results on dynamic on-resistance. Hence, the time constant for the trapping phenomenon appears close to unaffected by short blocking times. However, the results in Fig. 8 indicate that the absolute resistance value increases with blocking time, which is the value used to normalize the resistance in Fig. 10. Comparing this result with that in [8], the presence of a second trap with a longer time constant could be present. Thus, the on-state resistance should be investigated for longer on-times to correctly identify the possible time constant, magnitude and sensitivity of this second trap.

The result of an initial attempt at modelling the dynamic on-state resistance in LTSPICE is shown in Fig. 11. The $R_{DS,on}$ value of the GaN eHEMT SPICE model is 55 $m\Omega$ at room temperature. The DUT switches on a resistive load as is done in the experimental setup. The figure shows the DUT resistance when it switched on at the 100 μs time step. The test condition is 10 A load current, 400 V dc-link for an on-time of 7 μs, which is the same as one operating point of the experimental results. The shape and magnitude of the simulated resistance is similar to the measured value. Nonetheless, more extensive experimental data is needed to establish a correct model for the loss modelling of all operating points in a converter application. This will be the focus of future work.

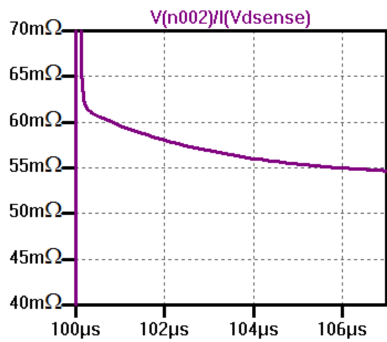

Fig. 11. Graph taken from LTSPICE of the modelled dynamic on-state resistance for 10 A load current and 400 V dc-link for device turn-on at the 100 μs time step.

V. Conclusion and Outlook

An experimental setup for measuring dynamic on-state resistance of GaN eHEMTs has been established using active differential probes. A deeper discussion of error sources for dynamic on-resistance measurement is presented. Validation of the experimental setup was done with a resistive DUT which shows that the circuit is able to quickly measure the resistance within 200 ns with high accuracy. The dynamic on-resistance was measured for a commercial GaN eHEMT. The results show that the resistance is sensitive to both dc-link voltage and blocking time. However, contrary to other published work, the absolute resistance is observed to decrease with increasing dc-link voltage. The measured time dependency of the resistance indicate that the suggested model is suitable for modelling dynamic on-resistance in LTSPICE. With further validation of the measurement circuit, the model of on-resistance will be fitted to the measured time constants and resistance magnitudes. The longer time constants will be added when measurement results are ready. For future work, the losses due to dynamic on-state resistance can be quantified for converter applications.

Acknowledgment

This work has been financed by Norwegian Research Council project no. 246784. The authors would like to thank Kjell Ljøkelsøy and Giuseppe Guidi for fruitful discussions on measurement technique.

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