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Characterization of electrical activity and lifetime in compensated multicrystalline silicon

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Abstract

This master's thesis concerns the electrical activity and lifetime in compensated multicrystalline silicon wafers used for solar cell production.

Resistivity profiles across grain boundaries have been obtained by a Four Point Probe (FPP). Profiles have been investigated in relation to minority carrier lifetime acquired by Microwave Photo Conductance Decay (μW-PCD).

It has been found that a two-step process consisting of pre-annealing at either 600°C or at 900°C followed by phosphorus diffusion (P) gettering will increase the electrical activity of crystalline defects. It has been proposed that a P gettering step should follow directly after annealing for a better dissolution of metallic precipitates.

Introduced defects in the material as a consequence of both pre-annealing at 900°C and of resistivity measurements before gettering, have possibly enhanced the phosphorus diffusion depth in the gettering process. The higher concentration of phosphorus has lead to an augmented lifetime in the material.

Metallic impurity precipitation at defects, affecting the electrical activity and the minority carrier recombination rate, has been observed. A good correlation between grain structure, resistivity- and lifetime profiles has thus been established.

Preface

The work presented in this thesis sums up a semester that has for me been challenging, rewarding and interesting, all at the same time. I have had the honor of working with so many talented people, and I will before all else give a special thanks to my supervisors,
Ursula Gibson and Marisa Di Sabatino.
Thanks for your collaboration, time and support during this semester.

I will give a thanks to PhD student Chiara Modanese for all your helpful guidance and time, knowing my way around the Berg building would not have been too easy without you.

Thanks to Rune Søndenå at IFE for his help with lifetime and gettering, to Hege Knutsen for spending her time helping me in the lab, to Astrid Salvesen for help with the glass amoules, and to Ragnar Fagerberg for resources and for including me in their research group.

Trondheim, 14.06.2011

Karianne Austad

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Chapter 1

Introduction

Solar energy is renewable energy, which does not produce greenhouse gases. Solar cells make use of this energy through the photovoltaic effect.

The photovoltaic effect was reported by A. E. Becquerel in 1939, but it was not until 1954 that the forerunner of the present silicon solar cells was announced. At that time, the solar cell only had an efficiency of 6%, in comparison to today's cells with efficiencies up to 20%. Solar cells were primarily used for satellites in space due to their lower efficiency. More efficient cells were produced in the 1970s, which made the cells interesting for terrestrial use. Today, solar cells are found all over the world, providing important social benefits for rural communities around the world [1].

Several types of solar cells are on the market today, with crystalline silicon cells as the dominating type, being responsible for 91% of the power module market. The module price was in 1978 around $70/W in current US dollars, and has since then had a 20% cost reduction for each doubling of cumulative production [2].

A shortage of silicon has since 2005 influenced the price of silicon solar cells. Historically, manufacturers have focused on other cost elements than efficiency, which resulted in a stagnation of the efficiency at 14% from 1983 to 2002 [2].

Higher efficiency of silicon solar cells will have a positive impact through the entire value chain. Higher efficiency means less silicon, less module materials, and less installation costs for a given power rating [2].

The development of today's commercially available multicrystalline silicon solar cells have been influenced by the goal of increasing the efficiency. Today the efficiency is estimated to be around 14-19% [3].

The need for silicon feedstock has made researchers look away from electronic-grade silicon and shifted the focus on to the less pure up-graded metallurgical grade silicon (UMG-Si). Solar grade silicon used in solar cell production can be produced via a direct metallurgical route from UMG-Si, followed by a purification step and by a final casting step to get multicrystalline wafers. Up-graded metallurgical grade silicon usually contains high amounts of both boron and phosphorus, in addition to transition metals, oxygen and carbon. Phosphorus and boron are difficult elements to eliminate from the feedstock, resulting in silicon ingots having compensated doping.

Compensated doping is poorly understood. Interesting properties to investigate include how compensation influences the carrier lifetime and the carrier mobility of the solar cell [4]. A detailed knowledge of the impurities' impact on the performance of the cell is therefore required.

The efficiency of the solar cell is related to the lifetime of the charge carriers in silicon. Longer lifetimes, and there by lower recombination activities, are important to obtain the required efficiency. Transition metals and their precipitates in silicon are effective recombination centers, thus increasing the recombination activity. In the case of solar grade silicon, the impurities are mainly collected at grain boundaries or at intra-grain defects [5] .

The segregation of impurities towards crystal defects in multicrystalline silicon affects the electrical activity at grain boundaries and dislocations. Investigations of the grain boundary activity are therefore important since a high activity leads to a decrease in the open circuit voltage of the solar cell, and thus decreasing the cell's performance [6].

There is a lot of current research and development in this field. Phosphorus diffusion (P) gettering [7] is a well-known gettering technique used for p-type silicon materials, where impurities are gettered out of the bulk material and finally removed.

Annealing of multicrystalline silicon is an internal gettering technique known to getter impurities at grain boundaries and at defects in the material. The aim of this thesis is to investigate the effect of pre-annealing at 600°C and at 900°C of p-type multicrystalline silicon wafers with different compensation levels, in addition to P gettering.

The goal is to find that a two-step procedure will be more effective in terms of removing impurities from the wafer, hence resulting in lower grain boundary activities and higher minority carrier lifetimes than obtained by using P gettering alone. The theoretical background along with publications by researchers working on the same topic will be presented in the first part of the thesis. Results and discussions are given in relation to earlier research, in addition to a proposed conclusion.

Chapter 2

Theory

This chapter will provide the theoretical background needed to interpret the results obtained in the thesis. It will first encounter the basic principles behind the solar cell concept including the formation of a p-n junction, before looking at different aspects which have a negative impact on the total performance of the solar cell material.

2.1 Semiconductor crystals and solar cells

Solar cell operation is based on the ability of semiconductors to convert sunlight directly into electricity by making use of the photovoltaic effect. The incident light creates mobile charge particles in the semiconductor which are separated by the device structure and produce electrical current.

According to quantum theory, the energy of an electron in a crystal has to fall within well defined bands. The difference between metals, insulators and semiconductors can be described in terms of different electronic band structures. Semiconductors have the same band structure as an insulator, with a completely filled lower band, just with a forbidden energy gap, E_g between the two bands that is narrower. The forbidden energy gap is the region between the upper energy band and the lower energy band where no electron orbitals exist [8]. The lower filled band is called the valence band (VB) and the upper energy band is called the conduction band (CB). Figure 2.1 gives a schematic view of a semiconductor band diagram where excitation of an electron to the VB generates a free electron-hole pair. The electrons

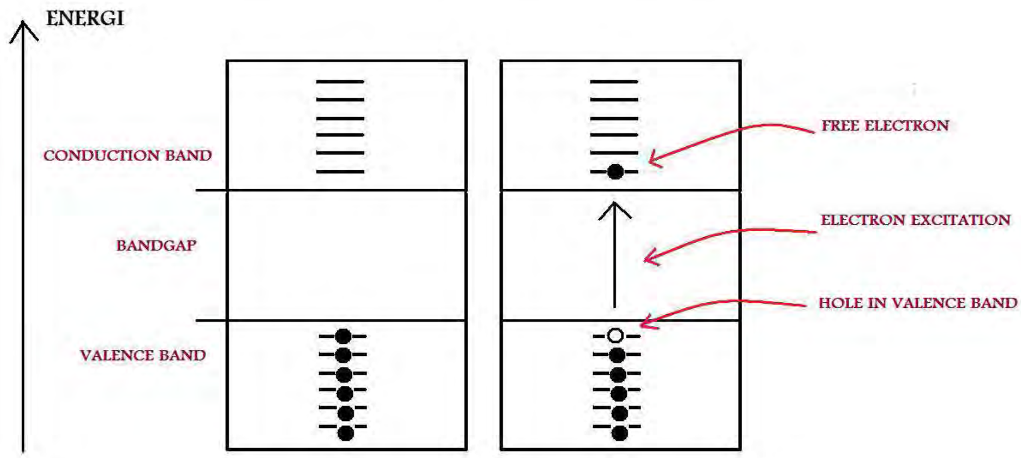


Figure 2.1: For a semiconductor, occupancy of electron states before (left) and after (right) an electron excitation from the valence band into the conduction band, in which both a free electron and a hole are generated. Reconstructed from [9].

in the conduction band, with unoccupied states called holes in the valence band, contribute to a current flow in the semiconductor. This is the principal mechanism in semiconductor materials such as silicon.

Impurities in silicon will have an effect on the electronic properties of the material. Additions of specialized impurities, named donors or acceptors, are a way of controlling these properties. The donor atoms control the relative concentrations of electrons in the conduction band, and acceptors control the relative concentrations of holes in the valence band. Materials doped with donors are commonly called n-type materials, while materials doped with acceptors are called p-type materials [10]. The doping of the semiconductor material influences the Fermi level E_F.

All available states in a crystal up to a certain energy level will be filled by two electrons. This energy level is the Fermi level E_F where the probability of finding the state occupied is 50%. Generally, when the temperature increases, some of the electrons will gain energy in excess of the Fermi level, and might be able to occupy a higher energy level.

The Fermi-Dirac distribution, seen in Equation (2.1), describes the probability of occupation of an allowed electron state of any given energy.

$$f(E) = \frac{1}{e^{[(E-E_F)/kT]} + 1} \tag{2.1}$$

where the quantity E_F is the Fermi energy, k the Boltzmann's constant and T the temperature.

When the temperature increases, states of a higher energy than E_F have a finite probability of being occupied, and states below E_F have a finite probability of being empty [10]. A plot of the Fermi-Dirac distribution for an intrinsic semiconductor can bee seen in Figure 2.2.

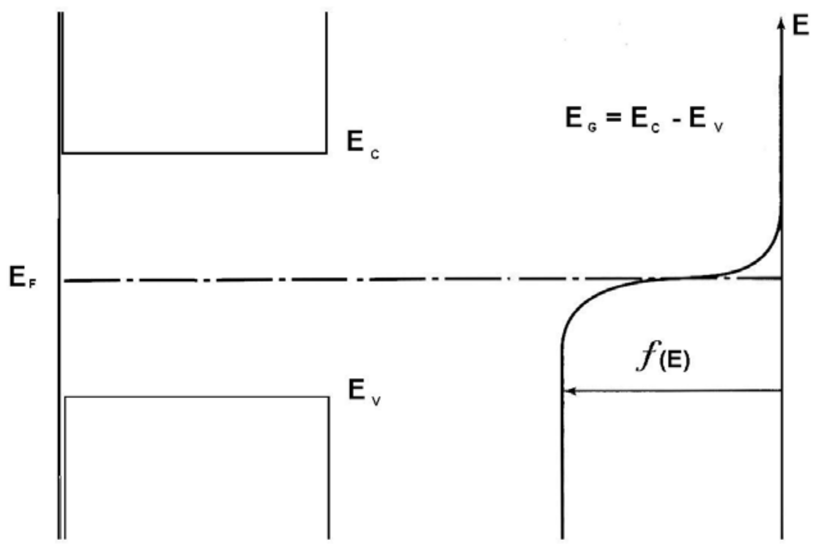


Figure 2.2: Energy scale for statistical calculations. The Fermi distribution is shown on the same scale, for a temperature $kT << E_g$. The Fermi level E_F is taken to lie well within the bandgap, as a function of an intrinsic semiconductor. If $\epsilon = E_F$, then $f = 1/2$. Reconstructed from [8].

The Fermi level will be positioned in the middle of the bandgap E_g for an undoped, intrinsic, semiconductor. However, it will move away from the midgap and approach the conduction band for n-type materials, or the valence band for p-type materials.

In silicon, each atom forms four covalent bonds, one with each of its nearest neighbors in the diamond structure. This corresponds to a chemical valence of four. If an impurity atom of valence five, such as phosphorus is substituted in the lattice instead of a silicon atom, there will be a valence electron left over after the four covalent bonds are established with the nearest neighbors. The impurity atoms that can give up an electron are therefore called donors [8].

Acceptors in silicon can be trivalent impurity atoms such as boron. They accept electrons from the valence band in order to complete the covalent bonds with neighbor atoms, leaving holes in the band [8].

The dominating charge carriers in a given semiconductor are called majority carriers. Examples of majority carriers in a given semiconductor are holes in a p-type semiconductor and electrons in an n-type. The opposite type of carriers whose concentration is generally much lower, are called minority carriers.

Silicon, with a bandgap of 1.11 eV at 300K [8], is one of the most common semiconductor materials used in solar cell production. The wavelength of the incident light on the solar cell will determine the photon energy given in Equation (2.2), which can be though of as energy packets which will excite electrons from the VB to the CB in the material.

$$E_{photon} = \frac{hc}{\lambda} \tag{2.2}$$

where h is the Planck constant, c is the speed of light and λ is the wavelength of the incoming light. Silicon is an indirect band-gap semiconductor where the minimum energy in the CB and the maximum energy in the VB occur at different values of the crystal momentum. Photons with larger energies are therefore required for a direct transition from the VB to the CB.

The threshold energy for an in direct band gap is thus greater than the true band gap. Excitation of an electron to the CB will be possible for lower photon energies, but has to involve a phonon which has a higher crystal momentum than a photon, as seen in Figure 2.3.

A two-step process through introduced impurity energy levels in the bandgap is also a possible absorption process, as seen in Figure 2.16. The position

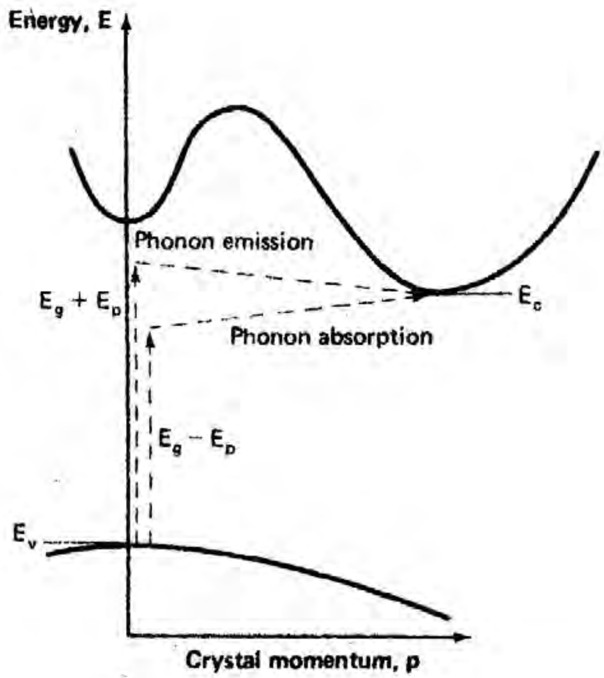


Figure 2.3: Energy-crystal momentum diagram of an indirect-band gap semiconductor such as silicon, showing the absorption of photons by two step process involving a phonon emission or absorption. From [10].

of the impurity energy level, seen in Figure 2.15, determines if it acts as a possible step in the absorption process, or as a recombination center. This will be discussed in detail in Section 4.3.

The total carrier concentration $n + p$ can be reduced in an impure crystal by introducing a small proportion of suitable impurities. Such a reduction is called compensation, and will be discussed in Section 2.1.3.

2.1.1 Multicrystalline silicon

Multicrystalline silicon is composed of a number of smaller crystals, where the small crystals have different orientations. These smaller crystals are termed grains and the boundaries between them are termed grain boundaries (GBs).

The GBs are the most important regions in multicrystalline silicon cells when regarding an electrostatic barrier developing between the grains. This barrier blocks the majority carrier flow inside the material, acting as a large series resistance [10]. This is illustrated in Figure 2.4.

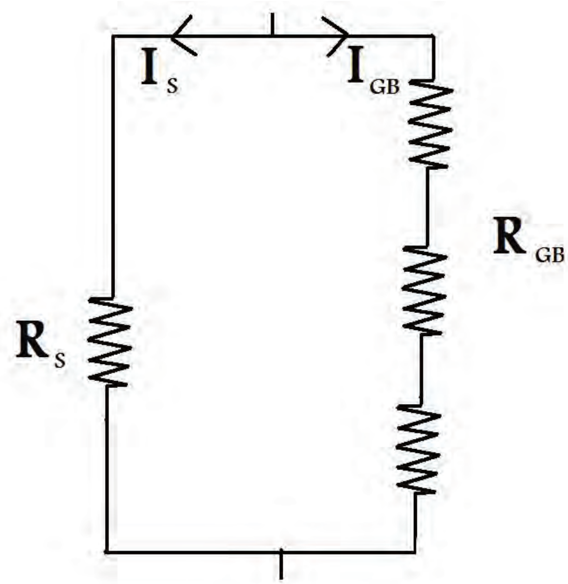


Figure 2.4: Grain boundary acting as a series resistance R_{GB}. The surface current I_s is expected to be much larger than the current through the grain boundary region I_{GB}.

Grain boundaries are defects in the crystal structure causing allowed levels into the forbidden gap of the semiconductor material and acting as very effective recombination centers, thus decreasing the carrier lifetimes. Grain boundaries can be thought of as minority carrier sinks. Therefore, to avoid significant loss in the performance of the solar cell the lateral dimensions of the grains must be large compared to the minority carrier diffusion length in the material, given in Equation (2.3).

$$L_n = \sqrt{D_e \tau_n} \tag{2.3}$$

Minority carrier diffusion length L_n is related to the minority carrier lifetime and the diffusion constant D_e, and is the distance a carrier can diffuse before it is recombined. Here given for p-type materials where electrons are the minority carriers.

Silicon requires large diffusion lengths in the order of 0.1 mm for good photovoltaic performance. This requires that the lateral dimension of the grains should be about a few millimeters [10].

Lifetime mapping of a multicrystalline silicon wafers will typically show inhomogeneous recombination lifetimes, correlated with the grain structure of the wafers. Grains exhibiting a distinctly higher recombination activity than neighboring grains will reduce the total performance of the solar cell [7].

2.1.2 Directional solidification

A common method of producing multicrystalline silicon is by producing ingots through directional solidification, where the solidification front advances towards the top. The aim of the directional solidification step is to refine silicon from metal impurities. Metals generally have a low equilibrium segregation coefficient and hence the distribution profile in the solid silicon reaches a good refinement extent [11].

The equilibrium segregation coefficient in thermodynamic equilibrium gives the relation between the concentration of impurity atoms in the growing crystal and that of the melt. It is usually much lower than 1, which leads to an accumulation of impurities in the un-solidified front during solidification. This can be seen from the liquidus and solidus lines in the phase diagram in Figure 2.5.

Directional solidification leads to an increasing impurity concentration in the crystal towards the upper part of the ingot, according to Scheil Equation (2.4).

$$C_s{}^* = C_0 k_0 (1 - f_s)^{k_0 - 1} \tag{2.4}$$

where $C_s{}^*$ is the concentration of impurities incorporated in the solid, and C_0 the initial impurity concentration in the bulk liquid, the feedstock material. The fraction of solidified material is denoted f_s and k_0 is the equilibrium segregation coefficient.

Scheil Equation assumes no diffusion in the solid state, complete mixing in the liquid state and equilibrium at the solid/liquid phase. If these prerequests are not fulfilled k_0 can be substituted by $k_{eff} = C_s/C_l$, the effective

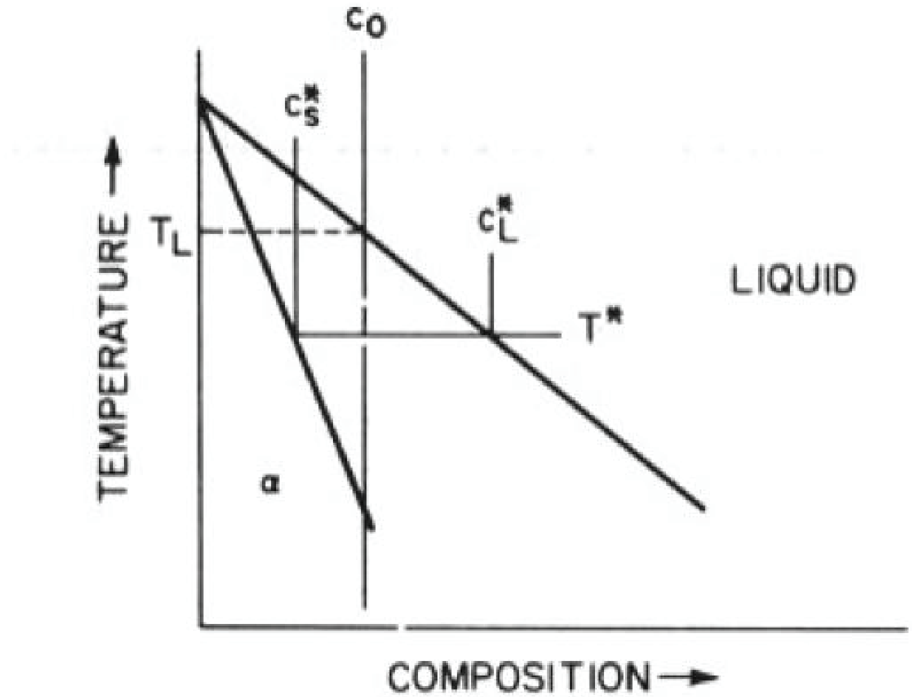


Figure 2.5: An extraction of the phase diagram of alloyed silicon under equilibrium conditions. It is assumed that the liquidus and solidus lines are straight (i.e k_0 is constant) for the range of composition shown here [12].

segregation coefficient between the bulk liquid and the solid phase. The effective segregation coefficient, k_{eff}, is different from the equilibrium segregation coefficient at the solid/liquid interface due to imperfect mixing of impurities in the liquid. The coefficient is therefore dependent of the growth speed, the diffusivity of impurities in the liquid, and the thickness of the convection free layer near the solid/liquid interface [7].

2.1.3 Compensated silicon

Compensated doping is typical for upgraded metallurgical silicon. Silicon usually contains a large amount of impurities, such as metals, carbon and oxygen. Metallic impurities have a detrimental effect on the carrier lifetime in silicon. They can be present in silicon as interstitial or substitutional ions alone or paired with dopant atoms, precipitates of oxides, silicates or silicides [13].

Compensated silicon typically contains high concentrations of boron and phosphorus, p-type and n-type dopants, respectively. Boron and phosphorus are difficult to eliminate through the metallurgical process due to a high equilibrium segregation coefficients k_0.

Phosphorus and Boron will therefore act as natural doping elements. Table 2.1 gives the equilibrium coefficients for some impurities in compensated silicon. The doping concentration will vary depending on ingot height, following Scheil's Equation (2.4).

Table 2.1: Equilibrium segregation coefficient k_0 for some impurity elements in compensated silicon, from [11].

Element	k_0
B	0.80
Al	0.002
P	0.35
Cr	0.000011
Fe	0.000008
Ni	0.00003
Cu	0.000015

Compensated material have higher dopant densities than not compensated materials, and are therefore expected to have lower mobilities, both for majority and minority carriers. A shorter minority carrier diffusion is therefore expected. Surface recombination activities have a greater impact on compensated wafers than on non-compensated wafers of the same resistivity. The effective lifetime will thus be lower in compensated silicon [4].

Earlier experiments [14] have shown that compensation of p-type silicon by phosphorus will result in a reduction of carrier concentration, a shift of the Fermi level, a change of occupation carrier lifetime, an increase in minority carrier lifetime and an increase of the resistivity.

The doping concentration has a further impact on the resistivity value of the material, which will be discussed in Section 2.3.2.

2.1.4 p-n junctions

A solar cell is essentially just a junction between n-type and p-type regions, as seen in Figure 2.6. A p-type region has a large hole density, but a small electron density. The opposite is true for n-type regions. When joining these two regions, electrons leaving the n-type region will leave ionized positive donors created due to a charge imbalance. Holes leaving the p-type region will similarly leave ionized negative charges. These exposed charges will set up an electric field which will oppose the natural diffusion of electrons and holes. An equilibrium situation will finally occur when they continuously recombine and annihilate one another, according to [8]:

electron + hole $\rightarrow$ energy

The equilibrium situation can be found by investigating the Fermi level, since only one Fermi level will exist for a system in thermal equilibrium [10].

The region where electrons and holes have diffused across the junction is called the depletion region because it no longer contains any mobile charge carriers. It is also known as the space charge region [10]. The potential change near the junction is given as ψ_0. When a voltage V_a is applied, the potential across the depletion region will become $(\psi_0 - V_a)$. The voltage measured is equal to the difference in the quasi Fermi levels of the minority carriers, i.e. electrons in the p-type portion and holes in the n-type portion.

A solar cell can be created by connecting the n-type and p-type sides of the junction to an external load. When light is absorbed by the material (the absorber), a transition from the ground state to an excited state occur. Absorber materials are capable of absorption-caused excited states produced by photons with energies in the photon-rich range of the solar spectrum, see Figure 2.7. The resulting excited states must be mobile; i.e., free electron-hole pairs, which can be separated, or excitons, which can be disassociated into free electrons and free holes and separated. The resulting free negative- and free positive- charge carriers will move in different directions, the electrons to the cathode side and electrons to the anode side of the junction. Electrons will then travel through an external path, an electric circuit, losing energy to an electrical load before returning to the anode of the cell. At the anode all

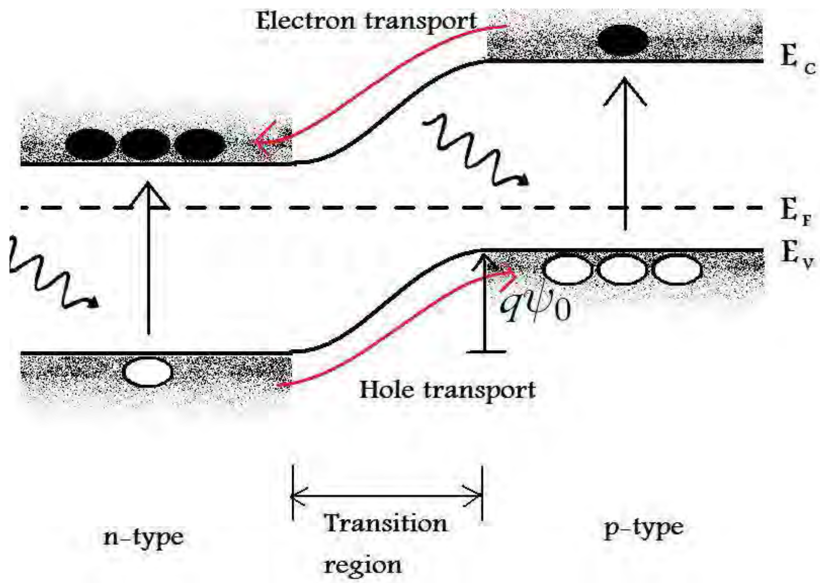


Figure 2.6: Schematic representation of current in a n-p junction under illumination.

the electrons combine with a positive-charge carrier, relaxing the absorber to its ground state [15].

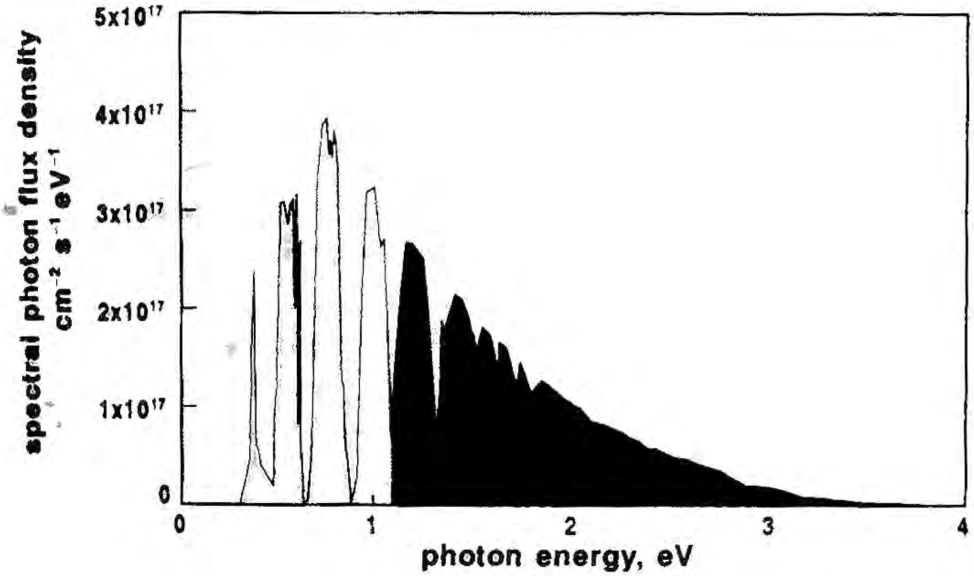


Figure 2.7: Photon flux utilized by a silicon solar cell with a bandgap of 1.11 eV is shaded. The relation between photon energy and wavelength of the absorbed light is given in Equation (2.2). From [1].

2.2 Imperfections in silicon

All solids contain a large number of various defects, or imperfections. A crystalline defect, is a lattice irregularity having one or more of its dimensions on the order of an atomic diameter, where classifications are based on geometry or dimensionality of the defect. This section will give a brief overview of imperfections in silicon, introducing terms which will be used in later discussion of the obtained results in this thesis.

2.2.1 Point defects

Point imperfections in crystals are chemical impurities, vacant lattice sites and extra atoms not in regular lattice positions. An example of a vacancy and an interstitial atom can be seen in Figure 2.8 a) and b), respectively.

Vacancies are the simplest of the point defects, where a site normally occupied is empty. Their presence in the material increase the entropy of the material.

Self-interstitials are atoms from the crystal that are crowded into an interstitial site, a small void space that is usually not occupied.

Interstitial point defects are sites where voids between the host atoms are filled with impurity atoms.

Substitutional point defects are sites where host atoms are replaced or substituted by impurity atoms.

Figure 2.8 shows defects disrupting the perfect arrangement of the surrounding atoms in a crystal lattice such as silicon.

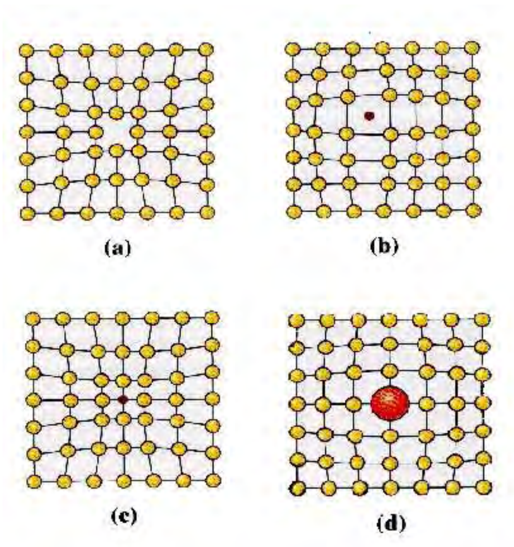


Figure 2.8: Point defects: (a) Vacancy, (b) interstitial atom, (c) small substitutional atom and (d) large substitutional atom [16].

2.2.2 Linear defects

A dislocation is a linear or one-dimensional defect around which some of the atoms are misaligned.

An edge dislocation is a linear defect that centers around the line that is defined along the end of an extra half plane of atoms.

A screw dislocation is another type of dislocation, where the upper front region of a crystal is shifted one atomic distance to the right relative to the bottom position. Edge and screw dislocations are most often found together, and are termed mixed dislocations.

2.2.3 Interfacial defects

Regions having different crystal structures and/or crystallographic orientations are separated by interfacial defects. These defects can be external surfaces, grain boundaries, twin boundaries, stacking faults and phase boundaries. Material containing such regions are termed multicrystalline materials, and are presented in detail in Section 2.1.1.

Grain boundaries A grain boundary is the boundary separating two small grains or crystals having different crystallographic orientations in multicrystalline materials. The degree of crystallographic misalignment between adjacent grains will vary. Small orientation mismatches are termed low angle grain boundaries, and larger orientation mismatches are termed high angle grain boundaries. An illustration of high and low angle grain boundaries can be found in Figure 2.9

A low angle boundary is a tilt boundary or a twist boundary. A tilt boundary undergoes a stronger reaction with impurities than a twist boundary.

A high angle boundary consists of alternatively repeated regions of good and bad matching between neighboring grains. Bad matching regions will typically have a stronger interaction with impurities than good regions [17].

An important fact is that atoms are bounded less regularly along a grain boundary, and thus gives an interfacial energy dependent on the degree of misorientation. This means a larger energy for high angle boundaries. A consequence of this energy, is that the grain boundaries are more chemically active than the grains themselves. This leads to impurity segregation along the boundaries because of their higher energy state.

Twin boundaries A twin boundary is a special type of grain boundary where the atoms on one side of the boundary are located in mirror-image

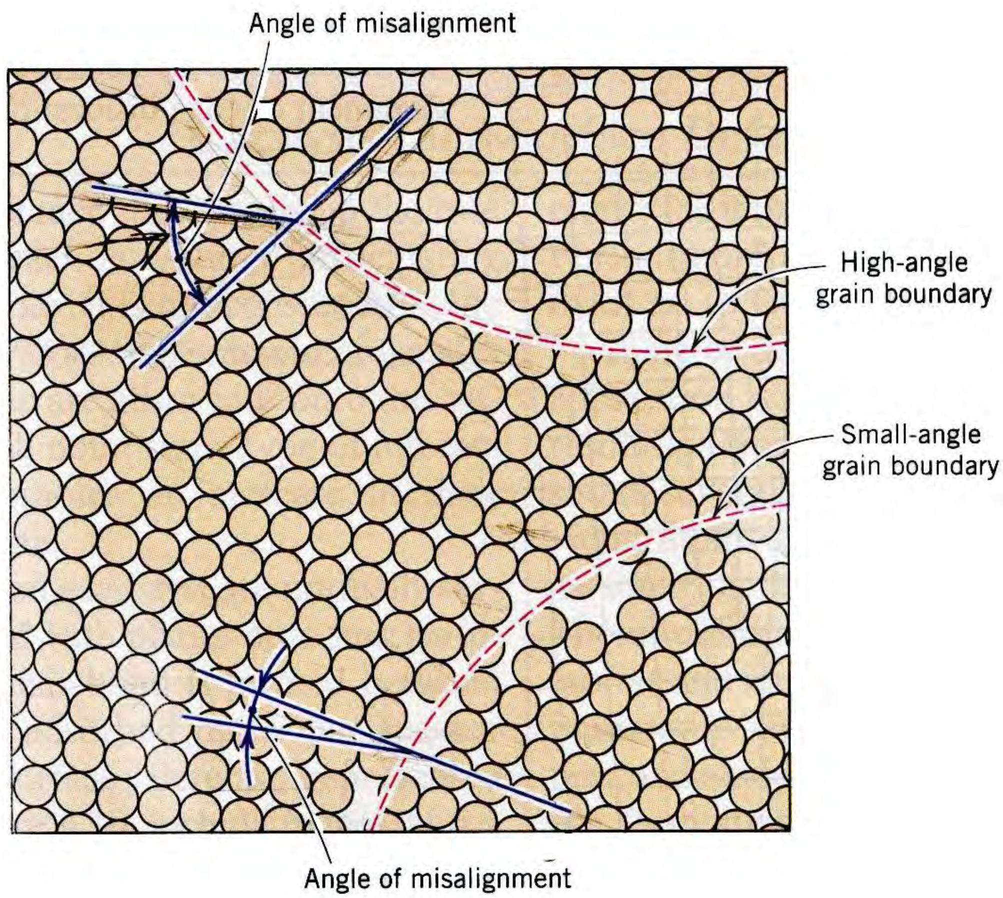


Figure 2.9: Schematic diagram showing small- and high-angle boundaries and the adjacent atom positions. From [9].

positions of the atoms on the other side. A schematic diagram is shown in Figure 2.10.

Precipitates If impurities are present in higher concentrations than their solubility at a given temperature, they may precipitate. Precipitates may form during solidification, during cooling after growth or during heat treatment. The formed precipitates are usually compounds of silicon [18].

Impurities in silicon can be Fe, Cr, Cu, Co, B, P, C and O, which will be

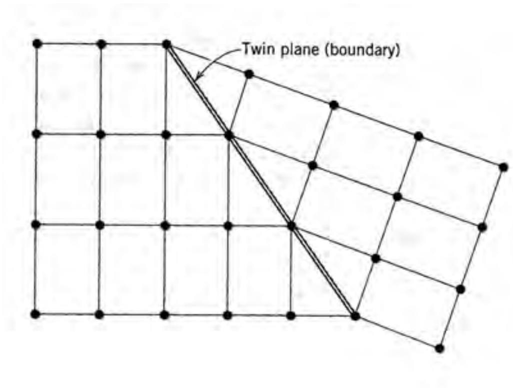


Figure 2.10: Schematic diagram showing a twin plane or boundary and the adjacent atom positions (colored circles). From [9].

discussed in Section 2.4.2 in relation to minority carrier lifetimes.

Precipitates can be found both intra-grain and at the grain boundaries. Grain boundaries have a tendency of being highly contaminated with impurities, which will be discussed more thoroughly in Section 2.6.

2.3 Carrier transport

Carriers in the conduction band and the valence band can flow by drift and/or diffusion when appropriate perturbations are present.

Drift When an electric field is set up inside a crystal structure, freely moving electrons will eventually collide with a lattice atom, an impurity atom, or a defect in the crystal structure. Such a collision will reduce the velocity of the electron. The average time between collisions is called the relaxation time, τ_r. Figure 2.11 show how an electron can be scattered several times due to imperfections in the lattice.

The electron carrier mobility, μ_e, is defined in Equation (2.5)

$$\mu_e = \frac{q\tau_r}{m_e^*} \tag{2.5}$$

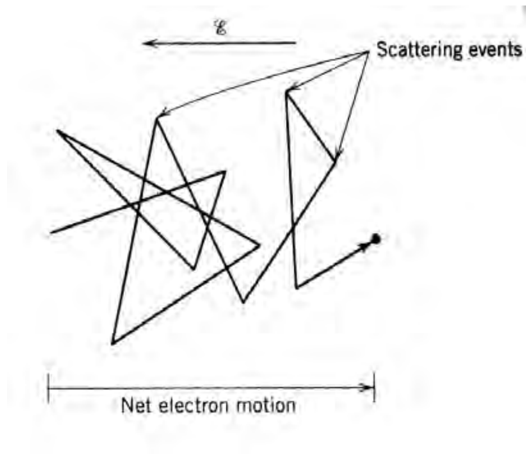


Figure 2.11: Scattering of an electron due to imperfections in the lattice. From [9].

where q is the charge and $m_e^* = 0.2m_0$ is the effective mass of an electron in the silicon lattice [10]. The effective mass of the electron incorporates the effect of the periodic force of the lattice atoms.

An analogous expression is valid for holes, giving the hole mobility μ_h.

The conductivity, σ, of a semiconductor can further be written as

$$\sigma = \frac{1}{\rho} = \frac{J}{\epsilon} = q\mu_e n + q\mu_h p \tag{2.6}$$

where ρ is the resistivity, J is the total current density flow, ϵ the applied electric field, n the density of electrons in the conduction band, and p the density of holes in the valence band.

From Equation (2.6), it is evident that an increase in the strength of the electric field will lead to an increase in the drift velocities of carriers. This will further decrease the time between collisions and the mobility. The carrier mobilities in compensated silicon are dependent on the level of compensation, defined by the ratio R_C.

The compensation ratio R_C can be defined as:

$$R_C = \frac{N_A + N_D}{N_A - N_D} \tag{2.7}$$

where N_A is the density of acceptors and N_D the density of donors in the compensated material.

A decrease in the carrier mobilities with compensation is expected. This is due to more scattering centers introduced in the material. There are various scattering mechanisms contribution to limit the bulk carrier mobility in silicon. These defects are crystal defects, impurities, carrier-carrier scattering, and lattice scattering. Hole-hole scattering and electron-electron scattering can not alter the total momentum, but can increase the momentum transfer rate. Compensated donors are ionized at room temperature and thus acts as additional ionized scattering centers reducing the mobility. For increasing donor concentrations, the acceptor scattering mechanism becomes less effective, due to screening of acceptors by donors. This means that acceptors are more effective scattering centers for very low compensation ratio [19].

Diffusion Carriers in semiconductors can also flow by diffusion, where the excess concentration of particles will tend to dissipate themselves unless constrained. Figure 2.12 shows the three basic mechanics of diffusion of an atom in a periodic lattice.

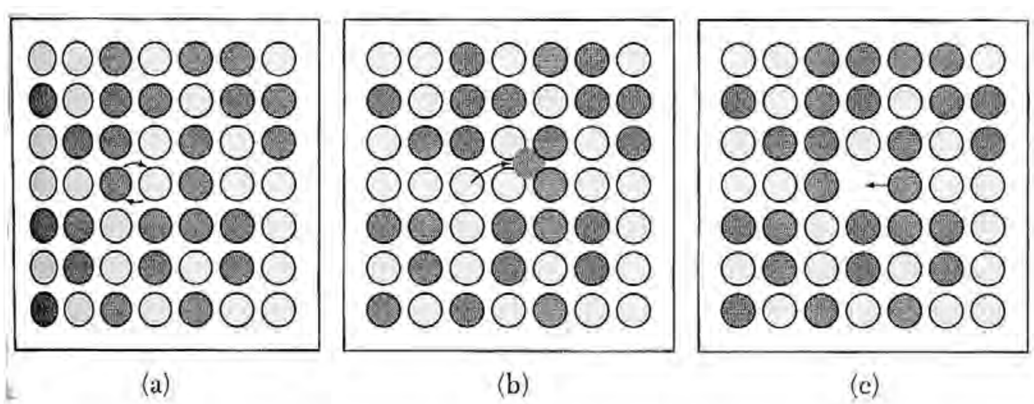


Figure 2.12: Three basic mechanics of diffusion. (a) Interchange by rotation about a midpoint. More than two atoms may rotate together. (b) Migration through interstitial sites. (c) Atoms change positions with the vacant lattice sites. From [8].

Drift and diffusion are fundamentally related, and the mobility and diffusion constants are connected through the Einstein's relations, seen in Equations

(2.8)

$$D_e = \frac{kT}{q}\mu_e \tag{2.8a}$$

$$D_h = \frac{kT}{q}\mu_h \tag{2.8b}$$

where D_e is the diffusion constant here giving the diffusivity for electrons, and D_h is the diffusion constant for holes.

The diffusivity of a specie is dependent on its activation energy for diffusion, and the diffusing temperature. This will be discussed in more detail in Section 2.5.1 in relation to gettering of impurities.

2.3.1 Hall probe measurements

Hall probe measurements are used to measure carrier concentration and/or carrier mobility. When a magnetic field is applied at right angles to current flow, an electric field is generated which is mutually perpendicular to the current and the magnetic field, and is directly proportional to the product of the current density and the magnetic induction. This is shown in Figure 2.13.

The force on an electron resulting from the collective effect of an electric field E and a magnetic field B is given by [20]:

$$f = -e(E + v \times B) \tag{2.9}$$

where v is the electron velocity.

A stationary state is attained when the Lorentz force is canceled as a consequence of the arising electric field in y-direction, as seen in Figure 2.13. This means that:

$$E_y = v_x B_z \tag{2.10}$$

At equilibrium, a voltage appears at the semiconductor edges, and the fundamental relations can be expressed as:

$$V_H = \frac{R_H I B}{W} \tag{2.11}$$

$$E_H = \frac{R_H I B}{A} \tag{2.12}$$

$$R_H = \frac{E_y}{j_x B} = \frac{dV_H}{IB} = -\frac{1}{ne} \tag{2.13}$$

where R_H is the Hall coefficient, I the current through the sample, A the sample cross section, W the thickness, j_x the current density and n the net carrier density.
The sign of the Hall coefficient R_H determines if the material is n- or p-type. The hall coefficient is negative for n-type materials and positive for p-type materials [21].

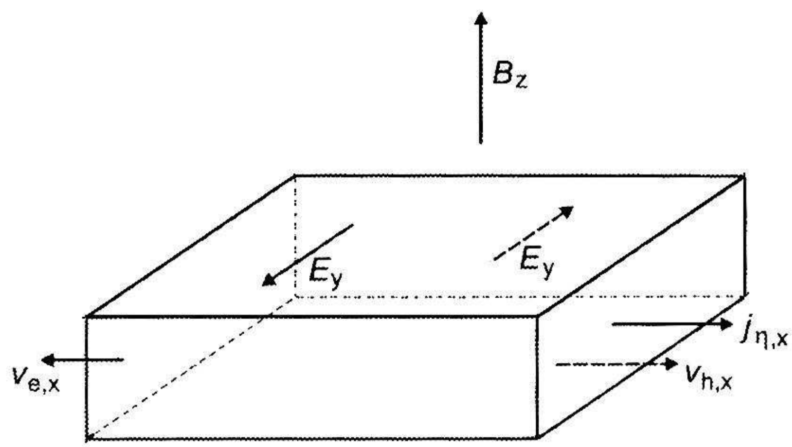


Figure 2.13: Fields and currents associated with measurements of the Hall effect: the charge current density j_n, the velocity of electrons $v_{e,x}$ and the holes $v_{h,x}$ as well as the electric transverse field E_y if the conduction is due to electrons and holes (dashed) respectively. From [20].

Equation (2.13) generally holds when there are just one type of carriers, but for mixed conduction, as in semiconductor materials and in the small-field case, R_H can be expressed as:

$$R_H = \frac{(1/q)(p - b^2 n)}{(bn + p)^2} \tag{2.14}$$

where $b = \mu_e/\mu_h$.

Errors may be due to a large offset voltage caused by non-symmetric contact placement, sample shape, and sometimes nonuniform temperature. The most common way to control this problem is to acquire two sets of Hall measurements, one for positive and one for negative magnetic field direction [22].

The resistivity of the sample can be calculated by using the measured voltage V together with the associated current I through the sample according to:

$$\rho = \frac{2\pi}{\ln 2} \frac{V}{I} W \tag{2.15}$$

2.3.2 Net dopant density

The concentration of dopants in silicon can be calculated from the measured resistivity value of the material.

The net dopant density can be calculated from the average resistivity by using the standard ASTM-F723 [23].
For boron-doped silicon, the dopant density can be calculated as:

$$N = \frac{1.330 \cdot 10^{16}}{\rho} + \frac{1.082 \cdot 10^{17}}{\rho[1 + (54.56\rho)^{1.105}]} \tag{2.16}$$

where the net carrier density N is given in [cm^{-3}] and the resistivity ρ in [cm].

For phosphorus-doped silicon, the net dopant density can be calculated as:

$$N = \frac{6.242 \cdot 10^{18}}{\rho} \cdot 10^{z} \tag{2.17}$$

$$z \approx \frac{-3.11 + (-3.26 \log \rho)}{1 + (1.03 \log \rho)} \tag{2.18}$$

where the net carrier density N is given in [cm^{-3}] and the resistivity ρ in [cm].

Figure 2.14 gives the relation between resistivity, acceptor and donor concentrations for compensated silicon.

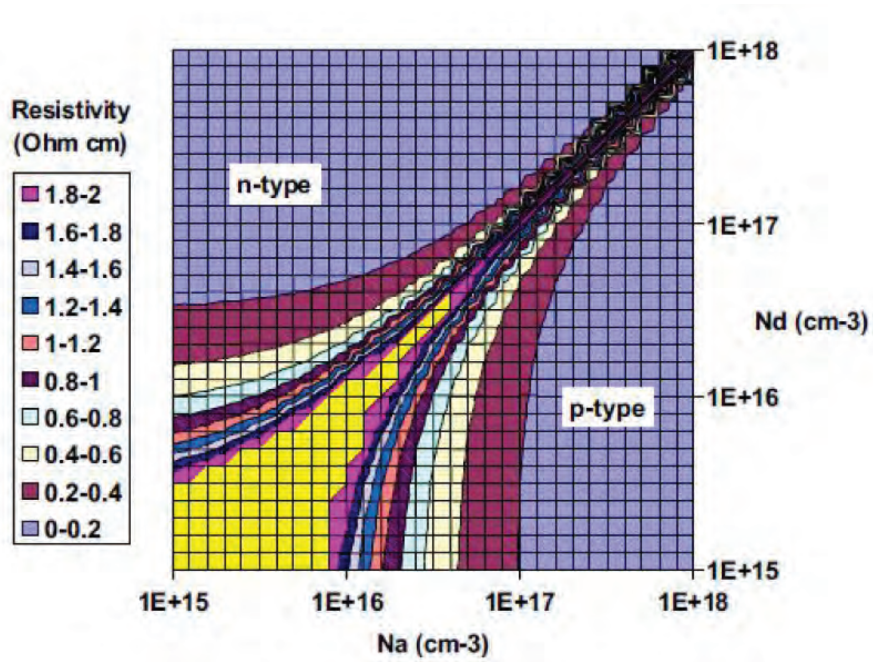


Figure 2.14: Resistivity of compensated silicon as a function of both acceptor and donor concentrations. Curves are only plotted for the resistivity range below 2 Ωcm. From [4].

2.4 Recombination and lifetime

When the equilibrium number of holes and electrons is distributed by introducing additional carriers, the minority carrier lifetime τ is a measure of the time required for the excess carriers to recombine. The lifetime is one of the most important parameters for the characterization of semiconductor wafers such as silicon in the preparation of solar cells, due to its effect on potential cell efficiency.

The lifetime is related to the recombination rate by:

$$\tau_n = \frac{\Delta n}{R} \tag{2.19}$$

where τ_n is the minority carrier lifetime for electrons, Δn is the excess minority carrier concentration for electrons in the CB and R is the corresponding recombination rate.

A similar expression is found for holes:

$$\tau_h = \frac{\Delta p}{R} \tag{2.20}$$

where τ_h is the minority carrier lifetime for holes, Δp is the excess minority carrier concentration for holes in the VB.

When measuring thin wafers, the recombination process will occur both in the bulk material and at the wafer surface. The rate of the recombination process on the surface is denoted as S, the surface recombination velocity. This give the effective lifetime τ_{eff} which is dependent on the bulk lifetime τ_{bulk} and the surface lifetime τ_s. The effective lifetime is given by:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_s} \tag{2.21}$$

A common case is where the two surfaces of the wafer are identical and characterized by a certain surface recombination velocity S. The surface recombination lifetime can then be written as [24]:

$$\tau_s = \frac{W}{2S} \tag{2.22}$$

where W is the thickness of the wafer.

By combining Equation (2.21) and (2.22) the effective lifetime can be expressed as:

$$\tau_{eff} = (\frac{1}{\tau_{bulk}} + \frac{2S}{W})^{-1} \tag{2.23}$$

If the wafer surface is well passivated with a thermal oxide or with SiN, the effect of the surface recombination can be neglected, and the measurement can be used to determine the bulk recombination properties of the wafer.

According to Equation (2.23) the effective lifetime would be zero when the surface recombination velocity is very high. In reality there is a limit on how low the effective lifetime can be because electrons and holes have to travel towards the surfaces by the relatively slow diffusion mechanism in order to recombine. The minimum effective lifetime for a transient Photo Conductive Decay (PCD) measurement is [24]:

$$\tau_{eff}(S \to \infty) = \frac{W^2}{\pi^2 D_e} \tag{2.24}$$

where D_e is the diffusion constant for electrons in silicon.

The bulk recombination lifetime is rather complex, three different recombination effects may occur. The carriers can recombine via traps within the energy gap by either radiative recombination, Auger recombination or by Shockley-Read-Hall (SRH) recombination with respective lifetimes τ_{rad}, τ_A, and τ_{SRH} [24].

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_A} + \frac{1}{\tau_{SRH}} \tag{2.25}$$

2.4.1 Shockley-Read-Hall recombination

The most important recombination processes in indirect semiconductors such as silicon are Shockley-Read-Hall (SRH) recombinations involving traps in the bandgap. Traps occur in crystals containing impurities and defects giving rise to allowed energy levels within the otherwise forbidden bandgap. Typical impurity levels can be seen in Figure 2.15.

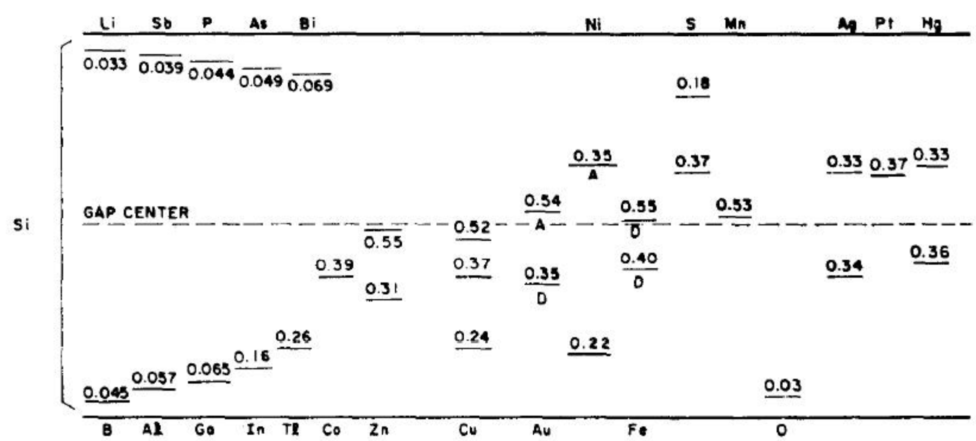


Figure 2.15: Energy levels within the forbidden gap for a range of impurities in silicon at 300K. A indicates an acceptor level, D a donor level. From [25].

Traps create a two-step recombination process where electrons relax from the CB energies to the defect level and then further to the VB, annihilating a hole [10]. This process is shown in Figure 2.16.

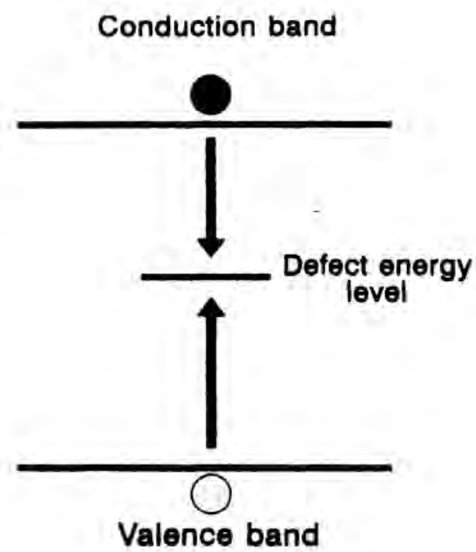


Figure 2.16: Defect assisted recombination of electron-hole pairs. From [1].

When the energy level of a trap is introduced close to either band edge, recombination is less likely to occur since the electron will be re-emitted to the conduction band edge rather than recombined with a hole from the valence band. For this reason, energy levels near mid-gap are very effective for recombination and should be avoided [24].

The net rate of SRH recombination is given as [18]:

$$U_{SRH} = \frac{np - n_i^2}{\tau_{n,SRH}(p + p_t) + \tau_{p,SRH}(n + n_t)} \tag{2.26}$$

where n and p is the number of electrons and holes respectively, n_t and p_t the electron and hole density in a trap and n_i the intrinsic carrier concentration. $\tau_{n,SRH}$ and $\tau_{p,SRH}$ are the lifetimes for electrons and holes respectively in a trap, with lifetimes dependent on the type of trap and the volume density of trapping defects.

If $\tau_{n,SRH}$ and $\tau_{p,SRH}$ are of the same order of magnitude, it is clear that U_{SRH} has its peak value when $n_t = p_t$. This occur when the defect level lies near the middle of the bandgap, thus introducing very effective recombination centers [10].

2.4.2 Recombination activity of contaminated dislocations

Dislocations are often decorated with impurities, acting as gettering sites during thermal treatment. Decorated dislocations can be more harmful to the minority carrier lifetime than clean dislocations [26].

Impurities in silicon form recombination complexes which introduce traps in the bandgap of silicon. Some important complexes are listed in Table 2.2 in addition to their position relative to the valence- or the conduction band.

Table 2.2: Location of the energy levels introduced in the silicon bandgap of both interstitial chromium, iron and aluminum, and their most common complexes.

Complex	Energy level eV
Cr_i	E_C-0.23
CrB	E_V+0.27
Fe_i	E_V+0.38
FeB	E_C-0.29
Al_i	E_V+0.06
AlO	E_V+0.44

Recombination centers in silicon can among others [27] be iron-boron pairs, FeB, chromium-boron pairs, CrB, interstitial iron, Fe_i, or interstitial chromium, Cr_i. These defects introduce traps in the bandgap that functions as very effective recombination centers, which is illustrated in Figure 2.17

Interstitial Aluminum, Al_i, introduce acceptor levels at 0.057 eV above the valence band, and may form complexes with transition elements in the same manner as boron, when oxygen is present in concentrations above 10^{15} cm^{-3} [28]. Aluminum-oxygen complexes have been located to 0.44 eV above the valence band by Rosenits et al. [29].

Not only Al can form complexes with oxygen. Boron is also known to form boron-oxygen pairs, BO, as a results of illumination of the material. Boron-oxygen complexes will annihilate at annealing temperatures above 200°C

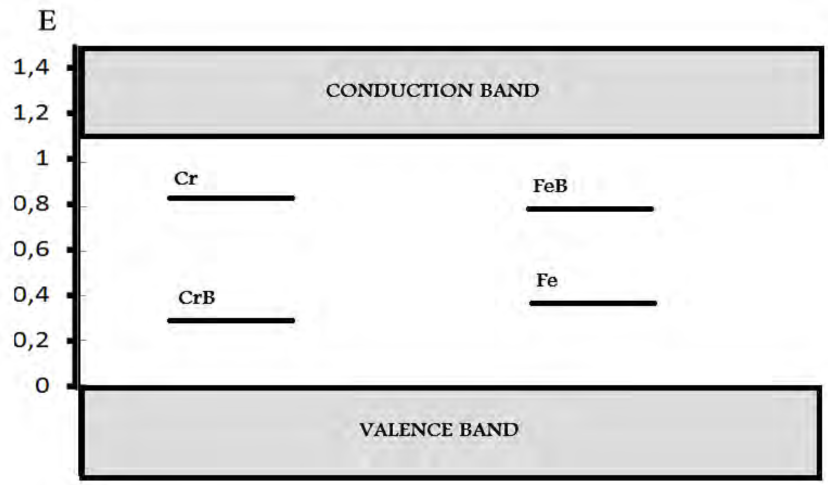


Figure 2.17: The energy levels introduced by interstitial chromium , interstitial iron as well as chromium-boron and iron-boron pairs.

[30]. The effect of BO complexes is mostly important in single crystalline silicon and not that important in multicrystalline silicon, since multicrystalline silicon wafers generally have a lower lifetime due to crystalline defects [31].

Istratov et al. [32] found that precipitated impurities at GB and dislocations in silicon usually show low recombination activities. They stated that the recombination activity can be high enough to dramatically reduce the minority carrier diffusion length if the metal impurities in the silicon lattice are situated at substitutional or interstitial sites, which is the case for Cr, Cu and Fe found in the investigated materials in this thesis. Metal-silicide precipitates are found to introduce deep electronic levels in the band gap, thus increasing the recombination activity. Fe and Cu usually precipitate as silicides, Fe_2Si and Cu_3Si, and will be found at grain boundaries or at dislocations after annealing.

New thermal donors should also me mentioned as possible recombination centers. They are oxygen-related defects formed at temperatures between 600-900°C, and are annihilated at 1100°C [33]. The highest concentration of oxygen is found in the bottom of the ingot, and are thus not expected to be in concentrations high enough to increase a significant amount of recombination centers in the band gap for wafers from 50% ingot height.

2.4.3 Other recombination processes

Auger recombination is the effect where an electron recombine with a hole giving the excess energy to a second electron instead of emitting light. The secondary electron then relaxes back to its original position in the CB by emitting a phonon. Auger recombination is most important in heavily doped or heavily excited materials [34].

Radiative recombination is the process where an electron make a transition from the CB to a lower energy state, without transferring the excess energy to another electron, but emitting the energy as light with corresponding wavelength, as seen in Equation (2.2). Radiative recombination is the dominating mechanism in direct band semiconductor, and can therefore be neglected for silicon being an indirect band gap semiconductor with long radiative lifetimes [24].

2.4.4 Lifetime measurements, μW-PCD

Microwave Photo Conductance Decay (μW-PCD) measures the time constant of decay in conductivity after a short, abrupt light pulse. The lifetime is often presented as lifetime maps where the resolution is dependent on the laser's spot size in the injection moment of carriers [18].

A micro wave antenna measures the difference in the reflected micro wave signal from the sample. Micro wave reflected signals are proportional to the decay in conductivity, from where the minority carrier lifetime can be deduced. To obtain a high enough signal, μW-PCD measurements are usually performed at high injection levels to obtain good signal [18].

2.5 Gettering of impurities

Gettering is a process where unwanted defects and impurities are removed from the active device environment into selected regions in the wafer. It is a technique used to obtain a large minority carrier lifetime and long diffusion lengths in silicon, through minimization of the concentration. The mechanisms for impurity gettering include precipitation of metal-silicides at energetically favorable nucleation sites at the surface or at structural defects within the material such as grain boundaries and dislocations [14].

Gettering processes are described as either internal or external.

External gettering is the process where impurities are attracted to a defect region on the backside of the wafer, removing impurities from the whole bulk material. This is necessary since solar cells use the whole bulk of the wafer as the active device region [35]. Parameters such as the thermal history of the crystal, the temperature at which the gettering takes place, and the rate of the passage through the gettering range characterize external gettering [17].

Phosphorus diffusion gettering (P gettering) is an external gettering technique, where most of the impurities can be diffused to the surface of the wafer. The phosphorus and impurity rich layer on the wafer surface formed after high temperature phosphorus diffusion gettering, typically around 900°C, is in the end removed, leaving a material containing less impurities than before the gettering process. Phosphorus gettering will be explained in more detail in Section 2.5.2.

Internal gettering is the process where impurities are collected inside the bulk, and much closer to the active devices. The internal gettering effect is characterized by the type of structural defect, the type of species and the concentration of the crystal.

Gettering of impurities can be considered as a three step process involving release, transport and capture of the impurity, as illustrated in Figure 2.18. Impurities most be released from substitutional positions or extended defects to enable diffusion to intentional nucleation sites outside the active component volume. This transport will take place during high temperature processing. The release and diffusion mechanics of the impurities are related to the properties of the transition metals in silicon and their interaction with self-interstitials [36].

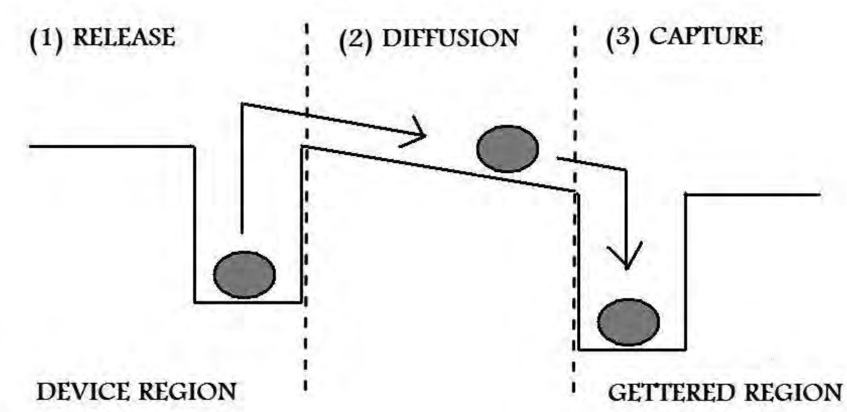


Figure 2.18: Concept of gettering process involving release, diffusion, and capture of defects. Reconstructed from [37].

Impurities should be immobilized and deactivated when captured. This is to avoid transport into the active device volume during later processing steps and render them inactive. For effective gettering, the energy barriers for release of impurities from the original impurity site should be low and the captured impurities should not be released easily.

2.5.1 Diffusion characteristics

The diffusion step in the gettering process is complex, so this section will briefly encounter some basic diffusion theory before looking at the mechanisms behind phosphorus diffusion gettering.

A flux $\mathbf{J}$, the number of atoms crossing unit area in unit time, will arise through the solid where there is a concentration gradient of impurity atoms or vacancies. In equilibrium the impurities or vacancies will be distributed uniformly, and can therefore be described by Fick's law:

$$\mathbf{J} = -D_A \nabla C_A \tag{2.27}$$

where the constant D_A is the diffusion constant, or diffusivity, of the diffusion species, and C_A is the concentration of the diffusing specie.

The following explanation will consider diffusion when donor impurity A^+ interacts with intrinsic point defects of different charge states, X^{-m}. The diffusion constant D_{AX}, where AX denotes the total charge of the diffusion species A^+X^{-m}, is often found to vary with temperature as

$$D^i_{AX} = D^0_{AX} \exp(-\frac{E^a_{AX}}{kT}) \tag{2.28}$$

where i is introduced to indicate the intrinsic conditions meaning that D^i_{AX} is to be understood as the diffusivity of A via interaction with intrinsic point defect X in the form of AX pairs. D^0_{AX} is a temperature independent factor including terms such as crystal geometry, total number of lattice sites and the vibrational frequency of the diffusing species. E^a_{AX} is the activation energy for diffusion. The diffusion follows the so-called Arrhenius behavior [7]. Diffusivities of different impurities in silicon can be found in Figure 2.19.

To diffuse, an atom most overcome the potential energy barrier presented by its neighbors. At a temperature of 700 °C, impurities at a concentration of 1 ppma are effectively trapped at sites where the interaction energy is larger than about 1.5 eV [17]. An increase in temperature is therefore one pre-request for a release to take place.

When looking at diffusion of impurities between interstitial sites, the same argument will apply to the diffusion of vacant lattice sites. If the barrier is of height E^a_{AX}, the atom will have sufficient thermal energy over the barrier a fraction exp (- E_{AX}/kT) of time. Quantum tunneling through the barrier is another possible process, but is usually of most importance for the lightest nuclei.

When the impurity is charged, one may find the ionic mobility μ and the conductivity σ from the diffusivity by rewriting the Einstein's relations given in Equations (2.8).

$$\mu = \frac{qD^0_{AX}}{kT} \exp(-E^a_{AX}/kT) \tag{2.29a}$$

$$\sigma = q\mu C_A = \frac{C_A q^2 D^0_{AX}}{kT} \exp(-E^a_{AX}/kT) \tag{2.29b}$$

where C_A is the concentration of impurity ions of charge q.

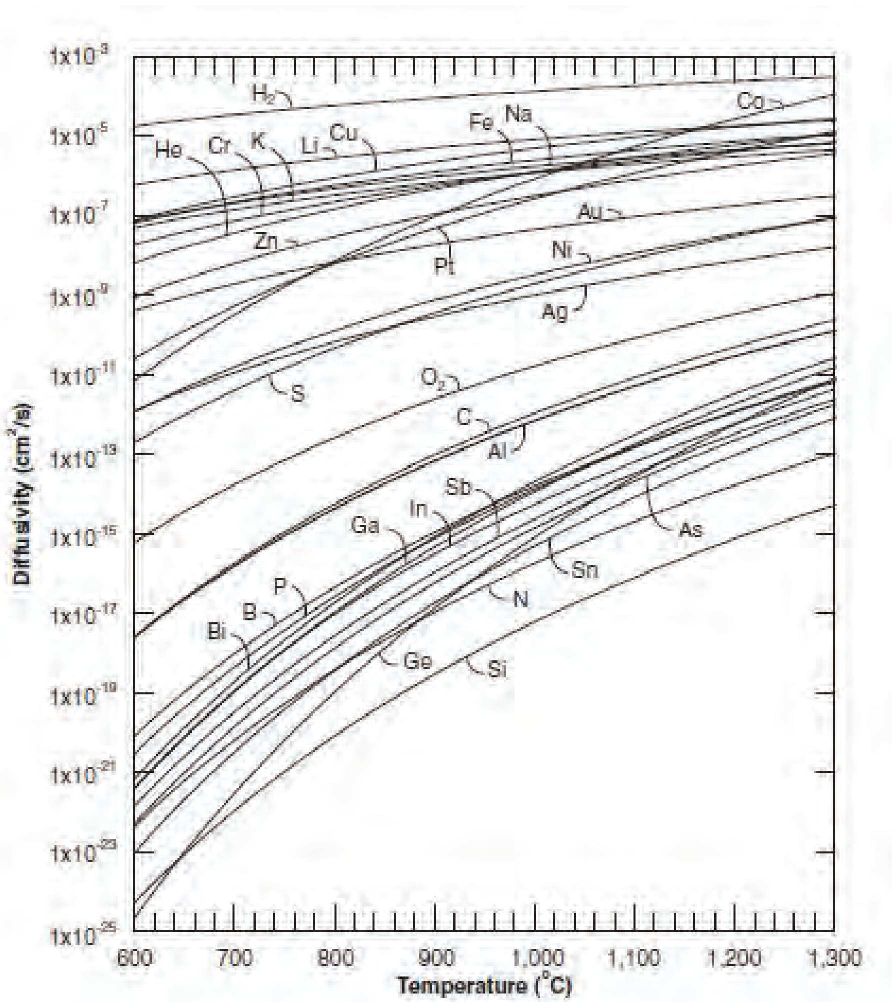


Figure 2.19: Diffusivities of selected impurities in silicon versus temperature. From [38].

2.5.2 Phosphorus Diffusion Gettering

An effective way of gettering is through phosphorus diffusion, which is a method that relies on the transport of released impurities towards a segregation region near the surface of the sample.

This transport is governed by charged dopants such as P^+ diffusing through the silicon lattice. Diffusion of an ionized dopant causes a spatially varying

Fermi level, so the force exerted on the dopants is no longer only determined by the thermodynamics but also by an internal electric field during diffusion. The Fermi level position changes with carrier concentration, and will further determine if the dopant diffusion mechanisms are due to interaction with vacancies and/or self-interstitials or to directly exchange of site with an adjacent crystal atom [7].

The concentration of phosphorus will be highest at the surface and will decrease with depth into the material. P diffusion in Si is typically [39] divided into four regions with varying diffusivity, as seen in Figure 2.20.

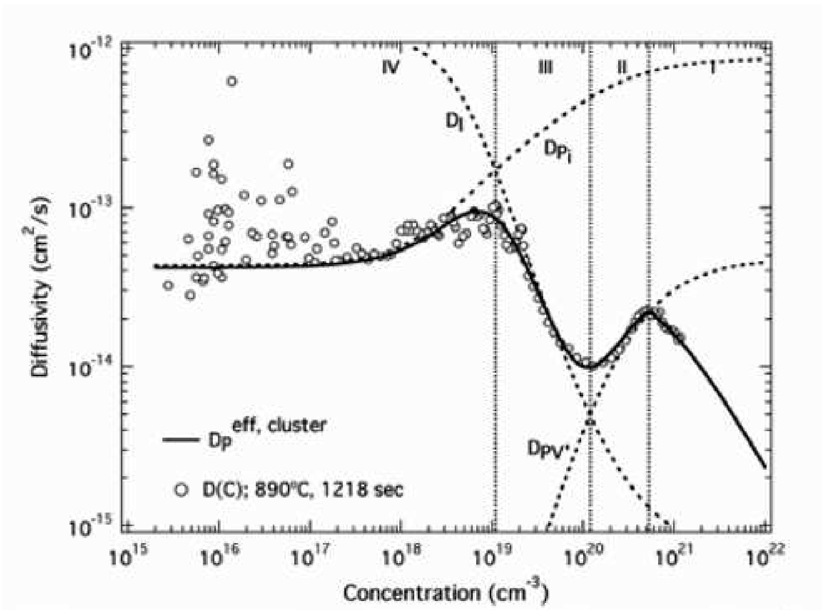


Figure 2.20: Plot from Bentzen et al. [39]. Phosphorus diffusivity as extracted by Boltzmann-Mantano analysis [7](open circles), and modeled (solid line) after in-diffusion at 890°C for 1218 seconds. Region I near the surface, and the border between region III and IV at a depth of approximately 0.2 μm.

Diffusion in region IV in the figure is governed by interaction with self-interstitials, referred to as I-type diffusion. A transition region occurs at the interface to region III, where migration of self-interstitials to restore local point defect equilibrium commences to limit the P diffusion. This self-interstitial limited diffusion prevails in region III. Region IV to III, where the

P concentration is low, is therefore the region where P diffuses in Si through kick-out reactions as described in Equation (2.30).

$$Si_{Si} + P_i \leftrightarrow Si_i + P_{Si}^{+} + e^{-} \tag{2.30}$$

where Si_{Si} denotes a substitutional Si atom, P_{Si} is a substitutional dopant, P_i is an interstitial P atom, e^{-} is an electron, and Si_i is a self-interstitial.

At the interface between region III and II, when the P concentration becomes significantly large, the Fermi level reaches the energy position 0.11 eV below the conduction band edge. This leads to a large increase in doubly negative vacancies which promotes a vacancy mediated diffusion in region II. Note that single vacancy in silicon can have four stable charge states [39]: doubly positive V^{++}, neutral V^{0}, single negative $V^{'}$. and doubly negative $V^{''}$. At the highest P concentration towards the surface, the solubility limit will be exceeded and cause formation of clusters. This finally leads to a P-rich layer near the surface in region I, with a consequent decreasing diffusivity of the clustered atoms [39]. Region III to I have a higher P concentration, and the diffusion will mainly be due to vacancy mediated diffusion, as in Equation (2.31).

$$P_{Si}^{+} + V^{''} \leftrightarrow (P_{Si} - V)^{'} \tag{2.31}$$

where V is a vacancy.

The total diffusivity will typically be result from a dual mechanism, through interaction with both self-interstitials and vacancies. Therefore, the overall effective dopant diffusivity is the sum of the two individual mechanisms [40], plotted as the solid line in Figure 2.20.

MacDonald et al. [13] have observed that the concentration of substitutional elements in silicon did not change upon P diffusion gettering, while the concentration of interstitial elements did. This is due to a difference in diffusivity between the impurity elements in silicon, with interstitial impurities having higher diffusivity, and hence lower activation energies than substitutional impurities.

Elements like O, Ag, Co, Cr, Cu and Fe are located in interstitial positions in silicon and can therefore be more easily gettered than substitutional species like C, As, Sb, Sn and Zn [13].

Experiments by Bentzen [7] have shown that significantly higher lifetimes can be obtained by applying longer duration diffusions at lower temperatures which is needed for deeper gettering into the wafer bulk. Deeper gettering can be possible due to an enhanced solubility segregation at lower temperatures, as well as increased transport lengths for dissolved transition metals and greater ability to dissolve precipitated impurities.

2.6 Grain boundary activities

An effect of thermal heating is that intra-grain impurities moves out to boundaries formed between grains. When impurities are precipitated at the boundary, an increase of the electrical activity is expected. Investigation of the grain boundary activity is therefore important since a high activity leads to a decrease of the open circuit voltage of the solar cell, thus decreasing its performance [6].

The electrical activity can be characterized in terms of the resistivity of the material. Resistivity is defined as the inverse value of the electrical conductivity, and is a measure of the material's resistance to the passage of current [9].

The resistivity will be uniform inside grains if no electrical impurities are present, but will change abruptly over grain boundaries due to a higher concentration of impurities influencing the currents ability to pass through. The abrupt change in the resistance through boundaries leads to a change in the measured potential.

The change is due to a pinning effect of the Fermi level with a band bending near the interface between the two grains. The band bending is due to the presence of a negative space charge region near the boundary surface in p-doped silicon, or due to a positive space charge region in n-doped silicon [6]. A schematic overview of the band-bending behavior can be seen in Figure 2.21. The properties of grain boundary barriers are dependent on doping and on grain size. This implies that the barrier height and widths can be reduced or removed by impurity doping [41].

In Section 2.4.2, the impact of precipitated impurity complexes was discussed. Complexes introduce energy levels in the middle of the bandgap in silicon, resulting in effective recombination centers for minority carriers. These trap levels, with energies E_T, are responsible for the pinning of the Fermi level at the boundary, as seen for n-type materials in Figure 2.6.

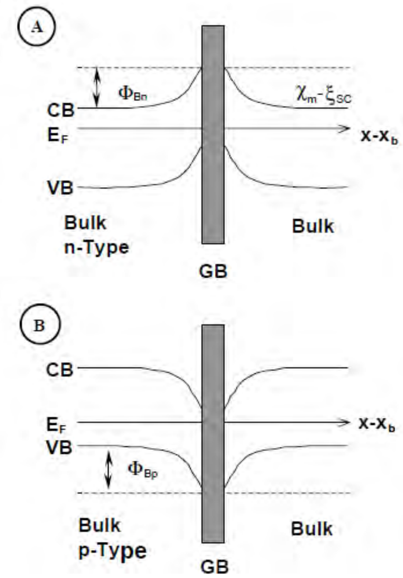


Figure 2.21: Schema of the energy band diagram in the "Two-Diode Model" for grain boundaries. In part (A) for a n-type mc-Si and (B) for a p-type mc-Si. A band bending appears due to the presence of charge in the surface of the grain boundary and the pinning of the Fermi level into the band gap. From Diaz et al. [6]

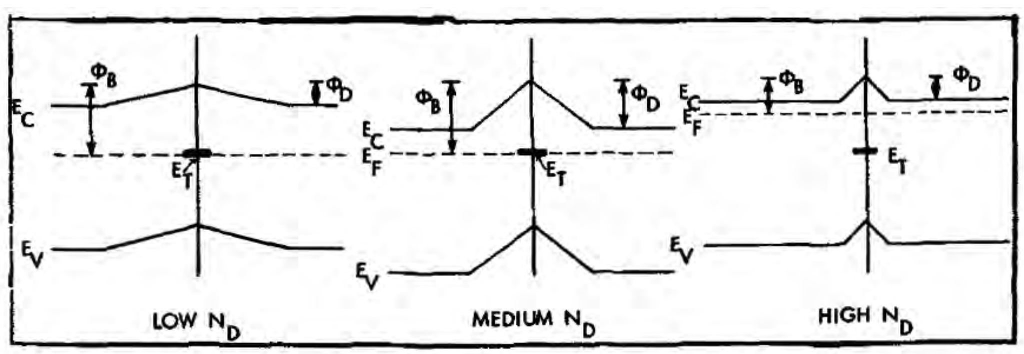


Figure 2.22: Energy level scheme of a grain boundary as a function of doping, Φ_B remains constant at low N_D because the Fermi level is pinned [41].

Ghosh et al. [41] explained the pinning effect of the Fermi level for an n-type material as follows; If there is a density of about 10^{12}cm^{-2} of the trapping specie, the Fermi level can move after the traps are filled. The relationship between E_F and E_T on the magnitude of the grain boundary barrier is indicated in Figure 2.6, in addition to figures showing low and medium doping densities. The Fermi energy is fixed at E_T at the interface between the grains so that the difference between E_F and E_C at the boundary remains constant. The Fermi level is expected to rise above the E_T approaching E_C for high donor densities when the traps become filled. When the donor density increases, the diffusion potential Φ_D through the barrier will increase as E_F approaches E_C, but will decrease when E_F begins to rise above E_T at the boundary. The diffusion potential $\Phi_D$is related to the barrier height Φ_B, and can be found by solving Possion's equation, and is expressed in Equation (2.32) [41].

$$\Phi_D = \frac{(ql)^2 N_D}{2\epsilon} \tag{2.32}$$

where q is the electric charge, l_2 is the width of the barrier region, N_D the doping density and ϵ the dielectric constant of the material ($\epsilon = 11.7$ for intrinsic silicon [8]). The present discussion has been based on n-type materials, but is also applicable to p-type materials.

2.6.1 Resistivity and height of barriers

The relationship between resistance and height of grain boundary barriers will be discussed in the following section. The crystal structure for a particular grain and its associated boundary can be illustrated as a bulk region and a barrier region of width l_2. The total measured resistivity will have two contributions, one from the bulk ρ_1 and one from the barrier ρ_2, as seen in Equation 2.33.

$$\rho = \rho_1 + \rho_2 \tag{2.33}$$

In resistivity measurements, an one-dimensional current density J will flow through the grain and the barrier [41].

$$J = q\frac{A^*T}{k}\exp(-\Phi_B/kT)V \tag{2.34}$$

$$J = q\frac{A^* T N_D}{k N_C}\exp(-\Phi_D/kT)V \tag{2.35}$$

where A^* is the Richardson's constant, N_C the effective density of states in the conduction band, k the Boltzman's constant, T the absolute temperature and V the potential over the barrier.

The resistivity for the barrier region can be expressed in terms of the current density as:

$$\rho_2 = \frac{V}{J l_2} \tag{2.36}$$

Equations (2.34) and (2.35) inserted in (2.36) and differentiation give the relation between Φ_D and Φ_B ($= E_A$), where $E_A$is the activation energy for diffusion [41].

$$E_A = k\frac{\partial \ln \rho}{\partial(1/T)} = \Phi_D - T\frac{\partial \Phi_D}{\partial T} = \Phi_B \tag{2.37}$$

The grain boundary activity has in earlier publications [6] been found to vary with ingot height. It has been shown that wafers taken from the bottom and from approximately 50-60 % ingot height show a larger grain boundary activity than from other heights in the ingot. This leads to a drop in the open circuit voltage for wafers showing high grain boundary activities.

Acceptable resistivity values for solar cells are between 0.1 - 10 Ωcm, and a balance between acceptor and donor species in the material is critical. A drawback is that resistivity control of compensated silicon can be difficult, due to the different segregation coefficients of P and B. This causes a varying resistivity due to the fact that the doping changes from p -type to n-type with ingot height, which again result in a cross-over point from p- to n-type at approximately 90% ingot height [4].

2.6.2 Resistivity measurements, Four Point Probe

A convenient way of measuring the resistivity, ρ, of a material is to use a four point probe (FPP).

FPP measurements can be done by passing a current through two outer probes and measuring the voltage through the inner probes, as illustrated in Figure 2.23. This allows the calculation of the substrate resistivity, ρ.

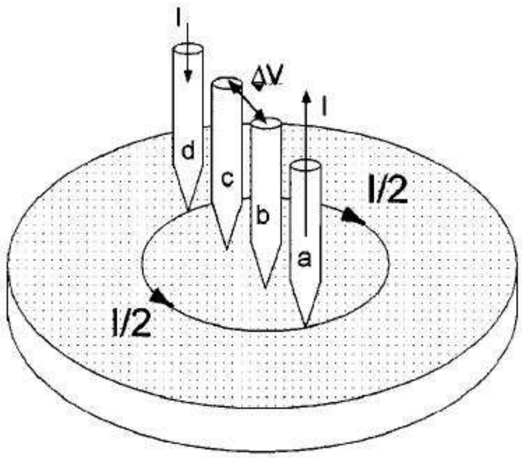


Figure 2.23: Four point probe measurement technique [42].

Resistance R is defined as

$$R = \rho(\frac{dx}{A}) \tag{2.38}$$

where dx denotes the sphere radius where the current will be distributed, and A the area of the sample. With $A = 2\pi xW$,where W is the sample thickness, the resistance becomes

$$R = \int_{s}^{2s} \rho \frac{dx}{2\pi xW} = \frac{\rho}{2\pi W} \ln 2 \tag{2.39}$$

From Figure 2.23 we see that

$$R = \frac{V}{2I} \tag{2.40}$$

which gives

$$\Rightarrow \rho = \frac{\pi}{\ln 2} \frac{V}{I} W \tag{2.41}$$

This generally holds for uniform samples if the probes are more than 2s from the edge of the sample, where s is the probe spacing, and if the thickness, W, of the sample is much less than the probe spacing [21]. FPP measurements are generally sensitive to impurities and defects in the material and a change in the potential will be present when crossing grain boundaries.

Chapter 3

Experimental

This chapter will give the experimental details related to all the results in this thesis. It will give the impurity compositions of the multicrystalline silicon samples and the samples' treatment in the process of obtaining possible better minority carrier lifetimes.

The order of treatments and characterization of the samples were done as follows:

1. Resistivity mapping
2. Organic cleaning
3. Annealing of samples
4. Resistivity mapping
5. CP5 etch, as explained in Table 3.4
6. Lifetime mapping
7. Phosphorus diffusion gettering
8. HF 5% etch to remove Phosphorus layer
9. CP5 etch
10. Lifetime mapping

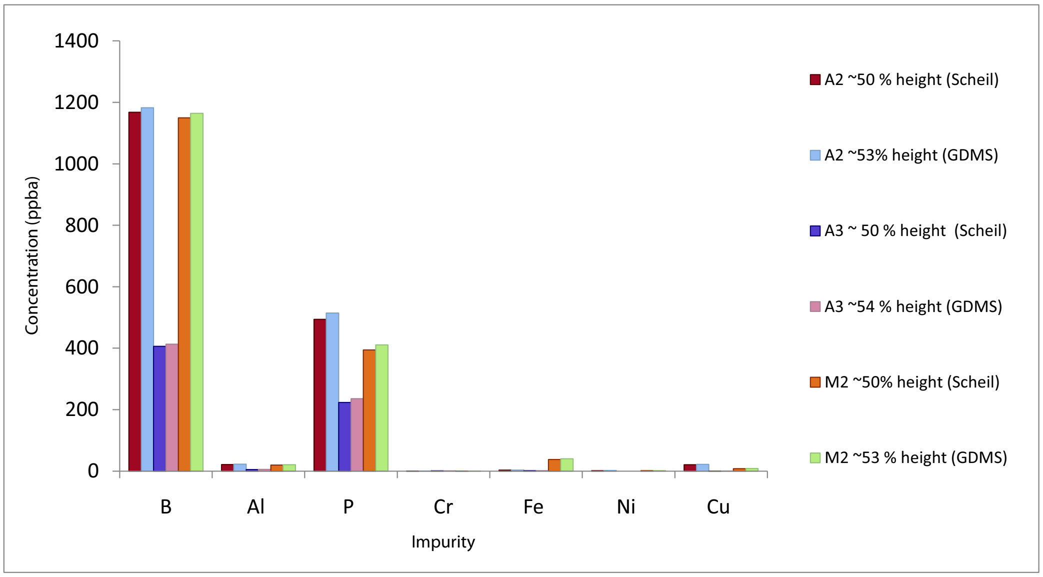
11. Resistivity mapping

Each of the listed points will be described in details in the following sections.

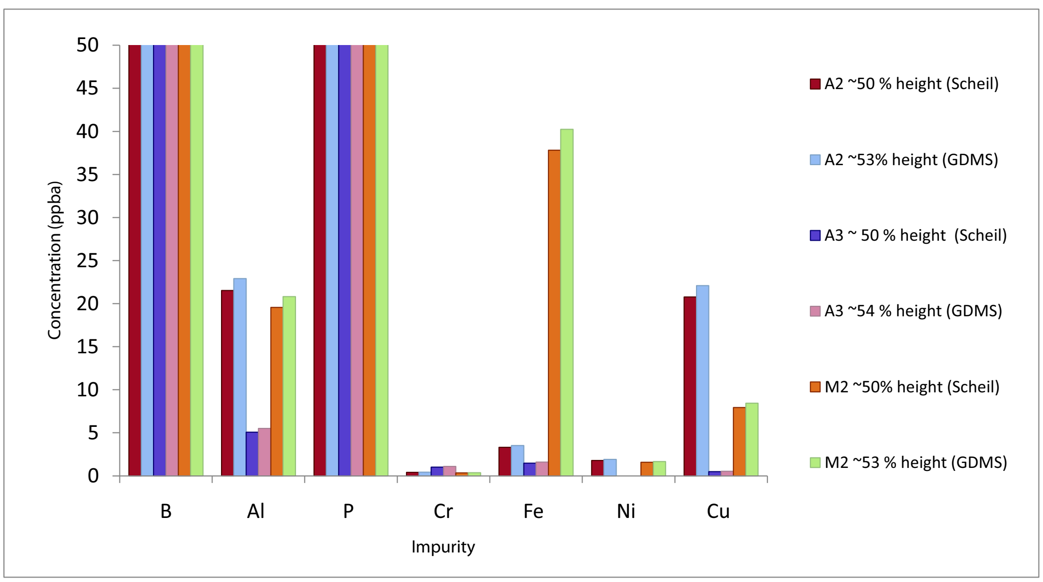
3.1 Impurity composition

Impurity concentrations of the wafers investigated in this thesis are shown in Figure 3.1. The concentrations at 50% ingot height are calculated based on measured impurity concentrations between 40-60% of the ingot height. Concentration values were obtained by Glow-Discharge Mass Spectrometry (GDMS) measurements [43], the lowest values close to the detection limit. Equilibrium segregation coefficients used in the calculation are found in Table 2.1.

Three wafers from three different multicrystalline silicon ingots with compensated doping have been investigated in this thesis. All wafers were initially as-cut and were extracted from about 50% ingot height. Each wafer of size 50x50 mm^2 was cut in four 25x25 mm^2 pieces as illustrated in Figure 3.2, at NTNU nanolab using a DX-III Scriber Breaker from Dynatex International. To obtain a nice cut, the wafer had to be scribed several times with increasing needle force, before applying the break force to the wafer. The wafer pieces will from now on be termed samples due to further treatment which will be explained in the following sections.



(a) Concentration of impurities.



(b) Lower concentration impurities.

Figure 3.1: Concentration of impurity species at approximately 50 % ingot height for ingots A2, A3 and M2. Scheil's Equation (2.4) has been used to calculate concentrations at about 50 % ingot height based on GDMS values between 40-60% ingot height. GDMS values from [44].

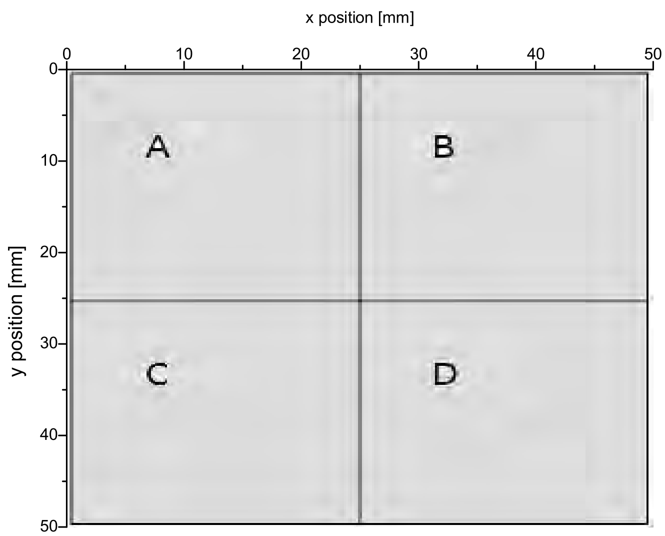


Figure 3.2: Illustration showing the division of one 50 mm x 50 mm wafer into samples A,B,C and D, each of size 25 mm x 25 mm.

3.2 Pre-anneal treatment of samples

This section will explain the relation between the wafers investigated in this thesis and their corresponding sample names. Three wafer have been selected from 50% ingot height, and are named A2-197, A3-141 and M2-118.

Each wafer was cut in four pieces/samples, where each sample was given different thermal treatment before the following procedures. One sample was annealed at 600 °C, one at 900 °C, one was kept in room temperature, and the last one was left untreated as a ”backup piece”.

Table 3.1 gives the sample names used in this thesis and their origin, along with their respective pre-annealed temperature.

Note that two ”sister” wafers, wafer A2-202 and wafer A3-139 have been included in addition to the three wafers originally investigated (A2-197 and A3-141). Only the minority carrier lifetimes before and after both annealing at 900°C and phosphorus gettering have been measured on the ”sister” wafers. A sister wafer is a wafer that has the same resistivity, impurity concentration and grain structure as its ”sister”. Two sister wafers can be seen in Figure A.15 in the Appendix. The addition of two sister wafers was done to investigate if the observed increase in lifetime after gettering of a pre-annealed wafer to 900°C was reproducible. The sister wafers were not cut in four, and have thus a size of 50x50 mm^2.

Table 3.1: List of samples, and their respective pre-annealing temperatures. The numbers in the end of the sample names indicate the annealing temperature of the sample. No number in the end of the sample name means sample without pre-annealing.

Name of wafer	Name of sample	pre-anneal temperature
A2-197-A	A2A6	600°C
A2-197-B	A2B9	900°C
A2-197-C	A2C	none
A2-197-D		
A3-141-A	A3A6	600°C
A3-141-B	A3B9	900°C
A3-141-C	A3C	none
A3-141-D		
M2-118-A (broken)	M2A6 (broken)	600°C
M2-118-B	M2B9	900°C
M2-118-C	M2C6	600°C
M2-118-D	M2D	none
A2-202	A29	900°C
A3-139	A39	900°C

An organic clean, as seen in Table 3.2, was used to remove organic impurities from the sample surface before annealing. This was done to avoid having a too ”dirty” sample surface during the annealing process, thus excluding any unwanted in-diffusion of impurities during the heat treatment.

Table 3.2: Organic clean, RCA-1, to remove organic impurities. First (1) step to 80°C results in formation of a thin silicon dioxide layer (about 10 Å) on the surface along with a certain degree of metallic contaminations (notably Fe) which is removed in the second (2) step.

Step	Composition	Time	Temperature
1	$NH_4OH + H_2O_2 + H_2O$ 1:1:5	10 minutes	80°C
2	5 % HF	2 minutes	25°C

The samples were sealed in small glass ampoules filled with 5.0 Argon gas during the heat treatment. 5.0 indicates that the Argon gas is at least 99.999 % clean of other contaminates. Samples heated to 600°C had an initial pressure inside the ampoule of 0.3 bar, while ampoules heated to 900°C had an initial pressure of 0.2 bar. This was done to avoid a possible collapse of the ampoules.

The ampoules were made at the glass-blowing workshop at NTNU. Figure 3.3 shows the glass ampoule containing a sample.

Figure 3.3: Picture of glass ampoule containing a sample, a 25 x 25 mm^2 piece of a wafer.

Table 3.3: Annealing temperatures for each of the samples. Each ampoule was annealed for 30 minutes. The temperature inside the furnace dropped each time an ampoule was inserted into the furnace. The temperature recovery times were about 2 and 3 minutes, at 600°C and 900°C, respectively. Ampoules heated to 600°C had an initial pressure inside the ampoule of 0.3 bar, while ampoules heated to 900°C had an initial pressure of 0.2 bar.

Annealing temperature	Sample	Temperature drop	Stable annealing temperature
600°C	A2A6	526° C	615° C
900° C	A2B9	810° C	909° C
600°C	A3A6	557° C	627° C
900° C	A3B9	824° C	907° C
600°C	M2C6	556° C	609° C
900° C	M2B9	803° C	907° C
900° C	A29	847° C	909° C
900° C	A39	812° C	907° C

Each of the samples was in turn annealed inside a ”Kanthal Super; Rapid High Temperature Furnace” from Bulten-Kanthal at the Department of Materials Science and Engineering at NTNU. The furnace was pre-heated to the required temperature before a glass ampoule was inserted.

The temperature inside the furnace was measured using a thermocouple of type S, which is suitable for this temperature range. An uniform temperature profile inside the furnace has been assumed. An overview of the furnace temperature during the experiment can be seen in Table 3.3.

3.3 Resistivity mapping

Four point probe (FPP) measurements were performed at the Department of Physics at NTNU using a probe from Signatone, model S-301-4, with a probe spacing of 1.59 mm. The experimental setup is shown in Figure 3.4. In addition to the probe, the setup consisted of a DC voltage source set at 8 V, two voltmeters and a resistance of 1 kΩ. The applied current through the sample was found from Ohm's law.

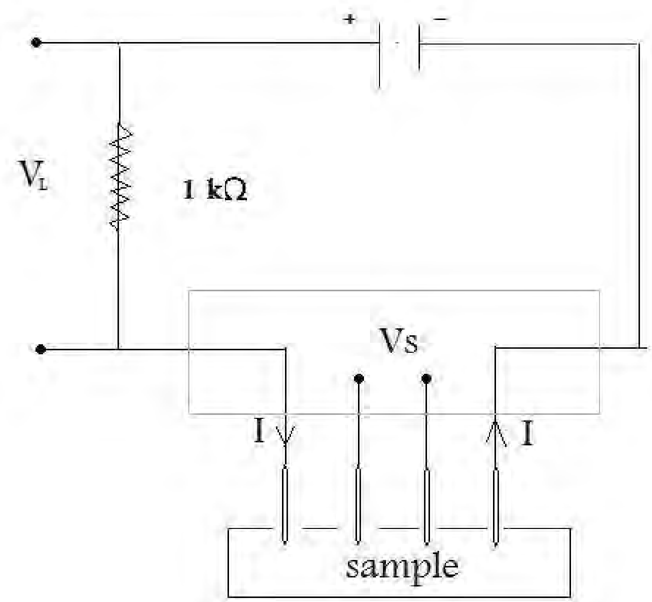


Figure 3.4: Setup used in four point probe measurements. Voltage over sample V_S, voltage over load V_L (1 kΩ), sample and DC voltage supply are indicated.

Each wafer was in turn placed on top of a one-dimensional translation stage which gave accurate positions (error of $\pm 5\mu$m) during the measurement. Lines were measured across each of the samples with the probe pins in parallel with the measured direction. The voltage and current were noted for each point, with a spacing of 25μm. The resistivity was then determined from these values using Equation (2.41) and the respective thickness of each sample, found in Table 4.1. Correction factors due to edge or grain boundary effects are not taken into account in favor of observing the potential drop, or rise, over structural defects.

Resistivity measurements were performed on samples before and after phosphorus diffusion gettering.

Table 3.4: Details of the CP5 etch performed before lifetime measurements at IFE

Step	Composition	Time
1	$HNO_3 : CH_3COOH : HF$ 10:5:2	2 minutes
2	5 % HF	2 minutes

3.4 Etching before lifetime mapping

Etching was performed in the clean room at Institute for Energy Technology (IFE) at Kjeller. The samples were etched using a CP5 etch and a hydrofluoric acid (HF) prior to lifetime measurements. CP5 is a chemical polish used to remove all traces of previously processing while the HF acid serves the role of smoothing the surface before lifetime measurements. Etching details can be seen in Table 3.4

The impact of the etching seemed to have been dependent on which wafer was etched, and the sample's thermal history. The two rounds of etching removed in total 24-85 μm of the wafer thicknesses. The decrease in thickness was measured at NTNU nanolab using the Vecco Dektak 150. The exact values for the thickness before and after etching can be found in Table 4.1 in Section 4.1.

3.5 Lifetime mapping

Mapping of recombination lifetime was performed by microwave photo-conductance decay (μW-PCD) measurements using a SEMILAB WT-2000 instrument at IFE. The measurements were performed at a laser power of 120 E11, with a spot size of 1 mm^2, a wavelength of 904 nm and a penetration depth of about 30 μm. Spatial maps were performed by measurements prior to and immediately after a strong illumination from an Xenon flash lamp. The data was acquired and analyzed using the computer program WINTAU. More details about μW-PCD measurements can be found in Section 2.4.4.

3.6 Phosphorus diffusion gettering

Phosphorus diffusion gettering was performed at IFE. A Phosphorus in-diffusion layer was applied on the surface of the samples before the gettering process. This was done using a spin-on dopant (Filmtronics P509) for wafers A2-197, A3-141 and M2-118, which was applied by pressurized air spraying to both sides of the samples. One side was sprayed, then baked at about 200°C for 15 minutes to evaporate the solvents from the film, before the same procedure was performed on the other side of the samples.

The samples where then placed inside an IR heated RTC LA-309 belt furnace to allow the diffusion process to occur. The furnace was divided into several temperature regions, with the first and highest temperature region at 890°C. The belt was operated at a speed of 4 cm/min for 100 minutes, before the speed was increased and the temperature decreased to allow the samples to cool down.

The two additional wafers, A2-202 and A3-139, were heated inside a $POCl_3$ tube furnace instead of using a spin-on dopant and an IR heated belt furnace. This is due to the sample size requirements of the tube furnace.

Finally, the diffusion source residues were removed by etching in 5% HF. The samples were again etched using a CP5 solution to prepare the surface before new lifetime measurements. Details of the CP5 etch can be found in Table 3.4.

3.7 Hall probe measurements

Hall probe measurements were performed at the Department of Electronics and Telecommunications at NTNU using Lakeshore 7500. The measurements were done for both positive and negative magnetic field up to 5000 Gauss, and the values were noted at the highest applied field, when the steady-state was reached.

The measurement geometry is shown in Figure 3.5.

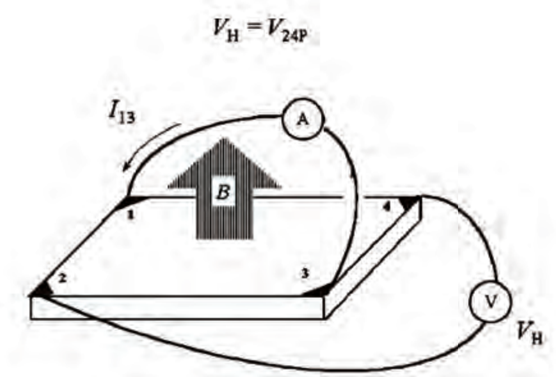


Figure 3.5: Illustration of measurement geometry used in Hall measurements. From [22].

Chapter 4

Results and Discussion

This chapter will first present and discuss the results obtained from resistivity measurements, before looking into how the minority carrier lifetime of each of the samples differs. The analysis is presented as a function of thermal history of the samples.

Resistivity and lifetime measurements have been performed on samples with different thermal history both before and after phosphorus diffusion gettering, also termed P gettering. The list of samples were given in Table 3.1. Phosphorus gettering is used to enhance the lifetime by removing dissolved metallic impurities from the bulk through diffusion to enhanced precipitates in the n-type surface region.

The wafers will from now on be recalled by their pre-fix, ie. A2-197 $\rightarrow$ A2 etc., and samples by their respective sample names, i.e. A2A6 etc.

4.1 Average resistivity

As mentioned earlier, the three wafers were cut in four samples each as illustrated in Figure 3.2, where the fourth sample served as ”backup piece” and as a reference when needed. The samples were given different thermal histories as shown in Table 3.3.

The sample resistivity was measured along a line over each sample using a FPP. The measured resistivity has a contribution from both the bulk and the

Table 4.1: Thickness of wafers before and after two rounds of CP5 and HF etching, as in Table 3.4

Sample	Thickness before μm	Thickness after μm	Difference in thickness μm
A2C	270	241	29
A2A6	270	246	24
A2B9	270	236	34
A3C	229	158	71
A3A6	229	184	45
A3B9	229	144	85
H2D	276	210	66
H2C6	276	221	55
H2B9	276	200	76

surface, in addition to contributions from crystalline defects. Grain boundaries have an impact on the resistivity as mentioned in Section 2.6, which can be seen as a fall or rise in the resistivity profile when crossing grain boundaries.

An electric current will follow the path with the lowest resistance through the sample. The bulk of the material will therefore influence the measured resistivity if the surface is more heavily contaminated with impurities than the bulk.

The average resistivity for each sample, seen in Table 4.2, was obtained by averaging the resistivity values measured along a line over the surface. The average resistivity will thus be influenced by the boundaries as well as by the grains themselves.

Samples are etched before each lifetime measurement, and a decrease in sample thickness is thus expected. Thicknesses before and after gettering can be found in Table 4.1.

The reduction in sample thickness differs for the samples, which has influenced the results. The lifetime and the resistivity values after P gettering may be directly affected if some of the P- and impurity-rich surface layer still is present on the surface. An addition of phosphorus will increase the donor concentration in p-type silicon, hence increasing the resistivity. The impact

Table 4.2: Average resistivity [Ω cm] measured along each sample's respective path before and after phosphorus diffusion gettering. Values are plotted in Figure 4.2.

	Average resistivity *before* gettering		Average resistivity *after* gettering	
Technique	Four point probe	Hall probe	Four point probe	Hall probe
Sample	Ωcm	Ωcm	Ωcm	Ωcm
A2C	0.55 ± 0.02	0.52	0.56 ± 0.11	
A2A6	0.53 ± 0.06		0.55 ± 0.08	
A2B9	0.24 ± 0.10		0.65 ± 0.27	0.52
A3C	1.90 ± 0.21	1.88	2.04 ± 0.37	
A3A6	1.63 ± 0.13		1.71 ± 0.09	
A3B9	1.92 ± 0.34		2.16 ± 0.37	2.01
M2D	0.62 ± 0.04	0.57	0.79 ± 0.11	
M2C6	0.60 ± 0.05		0.66 ± 0.17	
M2B9	0.67 ± 0.12		0.67 ± 0.11	0.49

of a phosphorus layer on the lifetime will be discussed in Section 4.3.

A smaller decrease in thickness is found for samples pre-annealed at 600°C compared with samples pre-annealed at 900°C. A possible explanation can be that the etching responded better to higher densities of surface impurities. Thus more impurities can have out-diffused from the bulk as a result of the pre-annealing at 900°C.

4.2 Dopant density

Hall measurements were carried out to investigate the net dopant density for A2 and A3 before and after the treatments, and to confirm the resistivity values obtained by the FPP. Calculations of the net dopant density from resistivity is possible for both p- and n-type materials, using the standard ASTM F-723 [23].

The ASTM standard is valid for materials where there are no interactions between dopants, meaning that there is assumed any presence of B-P pairs or other B- or P- based precipitates. Earlier investigations on compensated multicrystalline silicon [45] have shown the ASTM standard to be valid for compensated materials as well. Calculated and measured GDMS values for the net dopant density of the samples can be seen in Table 4.4 and in Table 4.5, before and after P gettering, respectively.

Table 4.3: Net doping density of non pre-annealed samples *before* gettering, measured by GDMS. It is assumed that B and P are present as single-charged atoms in the conversion from dopant concentration to carrier density.

Sample	Type	GDMS			
		Acceptor conc. $N_A = [B + Al]$	Donor conc. $N_D = [P]$	Net dopant conc.	Net carrier density
		ppba	ppba	ppba	cm^{-3}
A2C	p	1214	494	720	$3.59 \cdot 10^{16}$
A3C	p	413	223	190	$9.48{\cdot}10^{15}$
M2D	p	1216	395	821	$4.10{\cdot}10^{16}$

Table 4.4: Net doping density *before* P gettering. All samples are p-type. Results from GDMS, Hall measurements, and calculated values using Equation (2.16) have been compared.

Sample	Type	Resistivity Ωcm	Calculated cm^{-3}	Hall probe cm^{-3}	GDMS cm^{-3}
A2C	p	0.55	$2.87{\cdot}10^{16}$	$5.19 \cdot 10^{16}$	$3.59 \cdot 10^{16}$
A2A6	p	0.53	$3.00{\cdot}10^{16}$		
A2B9	p	0.24	$8.03{\cdot}10^{16}$		
A3C	p	1.90	$7.34{\cdot}10^{15}$	$1.68{\cdot}10^{16}$	$9.48 \cdot 10^{15}$
A3A6	p	1.63	$8.62{\cdot}10^{15}$		
A3B9	p	1.92	$7.26{\cdot}10^{15}$		
M2D	p	0.62	$2.49{\cdot}10^{16}$	$2.26{\cdot}10^{16}$	$4.09 \cdot 10^{16}$
M2C6	p	0.60	$2.59{\cdot}10^{16}$		
M2B9	p	0.67	$2.28{\cdot}10^{16}$		

In phosphorus diffusion gettering a thin layer (n-type) is formed on the sample surface. This layer contains impurities as a result of the diffusion gettering process, and has to be removed through etching after the processing. Samples from A2, as seen from Table 4.5, show a change from p- to n-type after gettering due to a lower decrease in thickness which indicate that some of the n-type phosphorus rich layer is still left after the etching process.

Table 4.5: Net doping density *after* P gettering. Note the type of majority carriers, p or n-type. Results from Hall measurements, and density calculated using Equation (2.16) for p-type and Equation (2.17) for n-type, have been compared.

Sample	Type	Resistivity (FPP) Ωcm	Calculated cm^{-3}	Hall probe cm^{-3}
A2C	n	0.56	$9.15 \cdot 10^{15}$	
A2A6	n	0.55	$9.34 \cdot 10^{15}$	
A2B9	n	0.65	$7.76 \cdot 10^{15}$	$1.01 \cdot 10^{17}$
A3C	p	2.04	$6.81 \cdot 10^{15}$	
A3A6	p	1.71	$8.20 \cdot 10^{15}$	
A3B9	p	2.16	$6.41 \cdot 10^{15}$	$1.60{\cdot}10^{16}$
M2D	p	0.79	$1.89 \cdot 10^{16}$	
M2C6	p	0.66	$2.32 \cdot 10^{16}$	
M2B9	p	0.69	$2.28 \cdot 10^{16}$	$5.29{\cdot}10^{16}$

The net dopant density is compared and plotted in Figure 4.1 for all samples. The figure shows an increase in net dopant density (p) at 600°C for all three wafers. Net dopant density for p-type materials is defined as the difference in acceptor and donor densities, which implies that either the density of acceptor species has increased or the density of donor species has decreased.

4.2.1 Mobility

Hall probe measurements were performed to investigate the majority carrier mobility of A2 and A3 before and after treatments (annealing + P gettering). The mobility decreased after a two-step treatment involving both annealing at 900°C and P gettering. The most significant decrease in mobility was found for the wafer A2, which is the wafer that initially contained more impurities than A3 and where all samples changed from p- to n-type after phosphorus gettering. The higher concentration of phosphorus in the samples after gettering has decreased the mobility significantly, as seen in Table 4.6.

Recall how the resistivity was given in Equation (2.6), dependent on the mobility and the density of charge carriers. The resistivity will increase if either/or both the mobility and the density of charge carriers decrease.

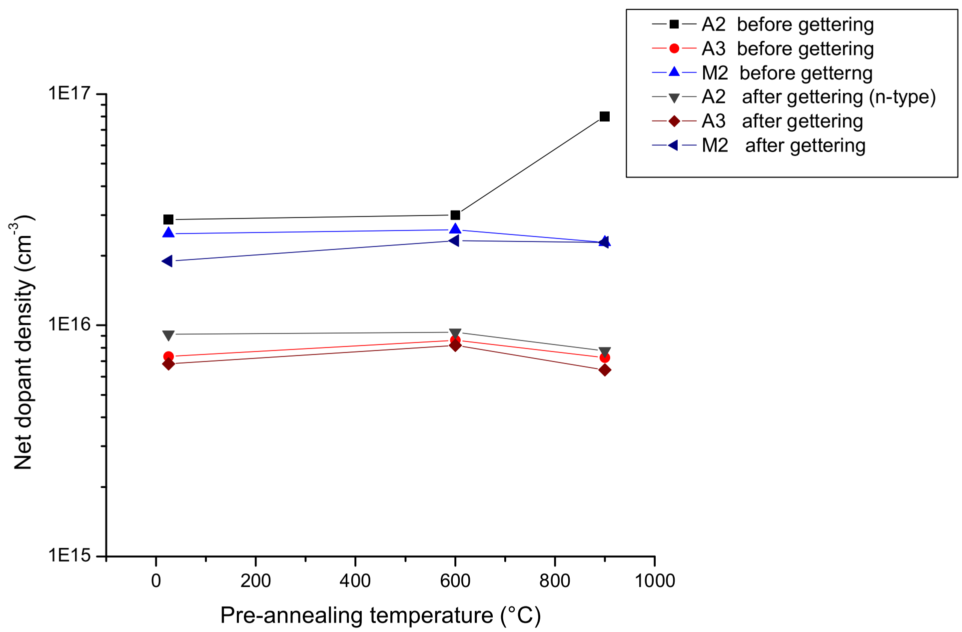


Figure 4.1: Net dopant density calculated by using Equation (2.16) for Boron doped silicon and by using the average resistivity for each sample. Samples from A2 were measured to be n-type after gettering and the net dopant density has been calculated using Equation (2.17). Note that the net dopant density scale is logarithmic.

Also, the Einstein's relations in Equation (2.8) gave that the diffusivity is proportional with the mobility.

Table 4.6 shows the obtained results for the mobility, the net dopant density, the resistivity and the majority carrier diffusivity for wafer A2 and wafer A3, with values in good agreement with the statement above. The decrease in mobility for A2 after treatment is reflected in the higher net dopant density and the lower diffusivity of charge carriers.

Peter et al. [46] found that the hole mobility in p-type wafers decreases with increasing degree of compensation. This is confirmed by Hall probe measurements before treatments, where the mobility of A2 compared to A3 is higher. This further implies that the compensation ratio for both A2 and

Table 4.6: Mobility and net dopant density measured by Hall probe before and after both an annealing at 900°C and P gettering. Resistivity values measured by Hall probe and 4PP are presented.

		Before any treatment		Annealing 900°C + P gettering	
Sample		A2	A3	A2	A3
Compensation ratio R_C		2.4	3.3		
Mobility (Hall)	[cm^2/VS]	231	198	117	192
Net dopant density (Hall)	[cm^{-3}]	$5.2{\cdot}10^{16}$	$1.7{\cdot}10^{16}$	$1.0{\cdot}10^{17}$	$1.6{\cdot}10^{16}$
Resistivity (Hall)	[Ωcm]	0.52	1.88	0.52	2.01
Resistivity (4PP)	[Ωcm]	0.55	1.90	0.65	2.16
Diffusivity D_p	[cm^2/s]	6.0	5.1	3.0	5.0

A3 has increased after treatment.

4.3 Average lifetimes

The minority carrier lifetime has been investigated before and after P gettering, and are compared with resistivity as a function of pre-annealing temperature in Figure 4.2.

The average lifetime was found by averaging over all the spots measured by μW-PCD. The samples were not passivated, hence a high surface recombination activity is expected.

Table 4.7 shows that a pre-annealing treatment at 900°C has had a destructive impact on the samples before P gettering in terms of the lifetime. The same trend is also found after P gettering, except for wafer A2, and in particularly sample A2B9 where the lifetime increased compared to the lifetime of a non-treated sample. Hall measurements showed that samples from wafer A2 changed from p- to n-type after P gettering, which has influenced the minority carrier lifetime.

Table 4.7: Average minority carrier lifetime measured before and after phosphorus gettering using μW-PCD. Pre-annealing temperature of each sample is included in the first column. Resistivity is plotted in Figure 4.2.

Pre-anneal temperature	Sample	Average lifetime before P gettering μs	Average lifetime after P gettering μs
25°C	A2C	2.7 ± 0.5	2.9 ± 0.9
600°C	A2A6	2.5 ± 0.5	3.2 ± 0.7
900°C	A2B9	0.2 ± 0.1	3.6 ± 1.5
25°C	A3C	2.4 ± 0.3	2.6 ± 0.7
600°C	A3A6	2.0 ± 0.6	2.10 ± 0.5
900°C	A3B9	0.3 ± 0.2	1.4 ± 0.4
25°C	M2D	0.4 ± 0.1	3.1 ± 1.0
600°C	M2C6	0.8 ± 0.1	2.9 ± 0.7
900°C	M2B9	0.2 ± 0.1	2.7 ± 0.7
900°C	A29-202	0.2 ± 0.3	2.5 ± 0.5
900°C	A39-139	0.3 ± 0.1	1.9 ± 0.3

According to Bentzen [7], phosphorus is only expected to diffuse about 1μm into the sample depth during the P gettering process. This statement does not seem to hold for the samples from wafer A2 since they became n-type after P gettering.

The wafer A2 has a higher impurity concentration than A3, and the decrease in lifetime with increasing pre-annealing temperature before P gettering implies that more defects are formed as a result of annealing, and thus introducing recombination centers in the bandgap. A recent publication by Xu et al. [47] claims that the electrical properties of multicrystalline silicon wafers decrease with increasing annealing temperature above 1100°C. The same is found for the experiments reported in this thesis before P gettering and for lower temperatures.

An other recent publication by Schön et al. [48] has shown that the lifetime for multicrystalline silicon with iron concentrations of $3.5 \cdot 10^{13}\mathrm{cm}^{-3}$ can be increased by using a short pre-annealing step at 900°C directly before P gettering process. The wafers A2, A3 and M2 investigated in this thesis have iron concentration of $1.6 \cdot 10^{14}\mathrm{cm}^{-3}$, $7.32 \cdot 10^{13}\mathrm{cm}^{-3}$ and $1.8 \cdot 10^{15}\mathrm{cm}^{-3}$, respectively. These are above the equilibrium concentration of iron around large precipitates which is $4 \cdot 10^{13}\mathrm{cm}^{-3}$ at 900°C [49]. A higher iron concentration will lead to a complete dissolution of small and medium sized precipitates during a short 900°C annealing, thus increasing the lifetime [48].

Schön et al. [48] also pointed out that the gain in lifetime after such a procedure is strongly dependent on the level and solubility of the impurities, implying the annealing temperature has to be adapted to the solubility and concentration of impurities.

Sample A3B9 show an increase in the lifetime after P gettering, indicating that a pre-annealing process at 900°C has had a positive influence on the lifetime value. The same procedure was performed one more time, to a sister wafer with the same impurity concentration, initial lifetime and crystalline structure. This wafer did not give the same increase in lifetime after P gettering. The lifetime was now lower than the obtained lifetime for the not pre-annealed sample after P gettering.

Bentzen et al. [50] found that areas adjacent to crystalline defects will have an enhancement of the P diffusion depth due to an increased concentration of silicon self-interstitials around defects. It is therefore possible that the introduced defects through the annealing process have increased the diffusion depth of phosphorus.

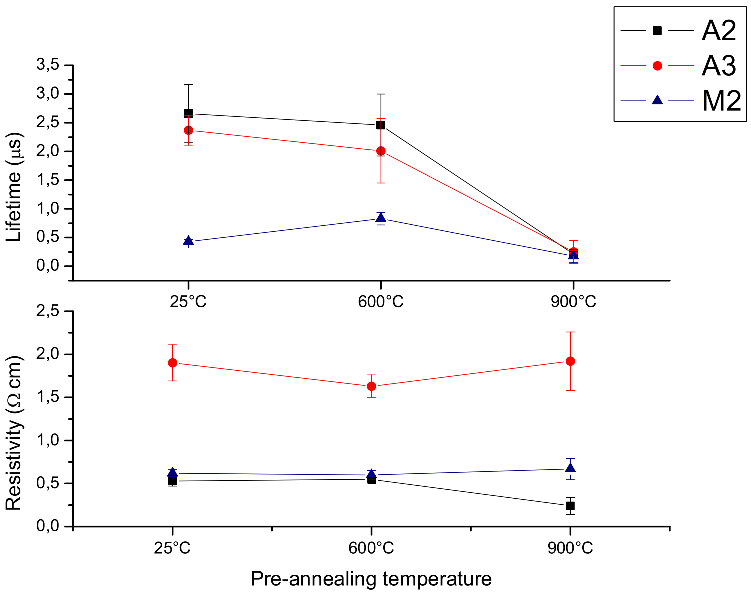
The increased phosphorus depth can also be explained in relation to the FPP measurements performed before the P gettering process. The probe left pin holes in the sample's surface. These "channels" may have increased the penetration depth of the phosphorus in-diffusion process in especially wafer A2-197 where the resistivity had been probed several times, due to the wafers's use in the learning process of setting up the probe and its electrical circuit.

The resistivity of the sister wafer A2-202 was not measured before the P gettering process, and was thus not harmed by the probe pins. The sister wafer had the same lifetime before P gettering, 0.2μs, but with a lifetime of 2.5μs compared to sample A2B9 with a lifetime of 3.6μs after P gettering.

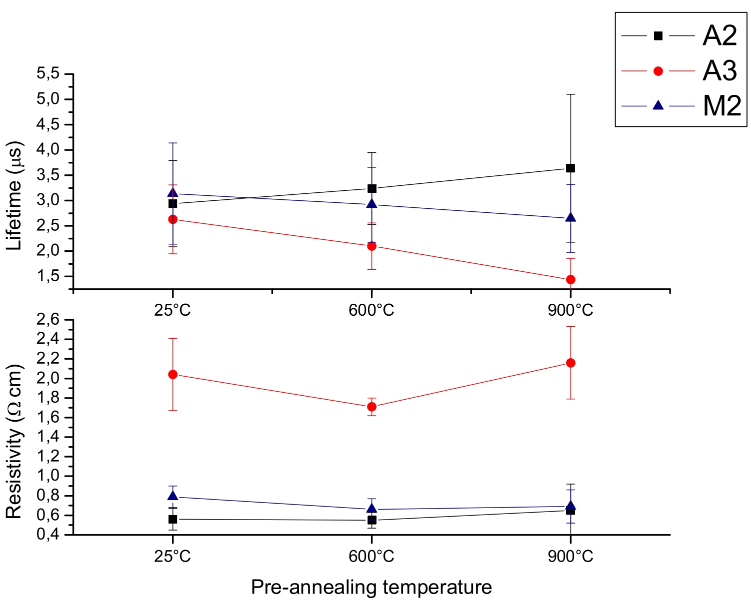
The introduced pin holes in the wafer surface have increased the in-diffusion depth of phosphorus, and thus increased the lifetime more than expected. MacDonald et al. [51] found that the presence of phosphorus can increase the lifetime by a factor of three, compared to control samples with similar concentration of boron, due to a reduction of the net doping. The increased lifetime found for the samples containing higher concentrations of phosphorus has thus been observed before. It would therefore have been interesting to see how the minority electron lifetime increase and mobility reduction combine to change the diffusion length.

This discussion has led to an understanding of the importance of a pre-annealing step at high temperature directly before the P gettering process, instead of weeks before which was the done in this thesis. It has given a better understanding of the effect of introduced defects in the wafer, which have served as diffusion channels for the phosphorus during the gettering process, hence increased the minority carrier lifetime.

Phosphorus gettering and a subsequent etching step should in principle remove most of the out-diffused and gettered impurities accumulated at the GBs, but have in these experiments not been very effective. A longer diffusion time might have been needed for the precipitated impurities at the GBs to be gettered out. According to Plekhanov et al. [35], precipitates have to be completely dissolved for the gettering process connected to annealing to be successful. Precipitates act as sources that slowly release metal atoms into the silicon matrix during the gettering process, and are thus unwanted in the lattice. They found that increased gettering temperature can accelerate the precipitates dissolution process and increase the diffusion coefficient of dissolved atoms. If the gettering time was shorter than the time needed for the completion of the gettering process, the result would, as seen here after pre-annealing, be a decrease in carrier lifetimes.



(a) Resistivity and lifetime *before* P gettering as a function of pre-anneal treatment.



(b) Resistivity and lifetime *after* P gettering as a function of pre-anneal treatment.

Figure 4.2: Resistivity and lifetime as a function of pre-anneal treatment. Figure a) shows before P gettering and b) after P gettering. Note that A2 has a heavily phosphorus doped surface region after gettering.

4.4 Minority carrier diffusion length

The minority carrier diffusivity D_n can be calculated from Equation (2.24) for a non-passivated surface, i. e. a sample with a high surface recombination rate. The minority carrier diffusion length can thus expressed as:

$$L_n = \sqrt{D_n \times \tau_{eff}} \approx \frac{W}{\pi}, \tag{4.1}$$

Table 4.8 gives the minority carrier diffusivity, mobility and diffusion length for the untreated wafers A2 and A3.

Table 4.8: Minority carrier diffusivity, mobility and diffusion length for untreated wafer A2 and A3.

		A2	A3
Compensation ratio R_C		2.4	3.3
Thickness W	[μm]	270	229
Lifetime τ_{eff}	[μs]	2.7	2.4
Diffusivity (min.) D_n	[cm^2/s]	0.3	0.2
Diffusivity (maj.) D_p	[cm^2/s]	0.1	0.07
Diff. length (min.)L_n	[mm]	0.09	0.07

The minority carrier diffusion length is expected to increase with increasing compensation in silicon according to Rougieux et al. [19]. Table 4.8 list the diffusion lengths for A2 and A3, which show a decrease with increasing compensation ratio.

Peter et al. [46] states that the minority carrier diffusivity is about three times as large as the diffusivity of majority carriers. The majority carrier diffusivity based on the mobility found by Hall probe measurements, given in Table 4.6, is much larger than the diffusivity calculated from Equation (2.24), and expressed in Table 4.8.

This indicates that the effective lifetime not only is influenced by surface recombination, as assumed in Equation (2.24), but also by the bulk lifetime. An increasing bulk lifetime, will lead to a higher effective lifetime and thus a higher minority carrier diffusion length, mobility and diffusivity.

Green [10] claims that silicon requires large diffusion lengths of the order of 0.1 mm for good photovoltaic performance. Since bulk recombination effects should be taken into account when calculating the diffusivity, longer diffusion lengths than the lengths listed in Table 4.8 are expected. The diffusion lengths in Table 4.8 for A2 and A3 can thus only be considered as diffusion lengths when the surface recombination dominates over recombinations in the bulk.

4.5 Resistivity, lifetime and crystalline structure

The feedstock composition of M2 had an initial addition of 50 ppmw of Cr, but no significant amount of Cr has been found by GDMS measurements of the wafers from about 50% ingot height. Chromium might still be present since only a small area is measured for each GDMS value. If the measured area contains less Cr than other areas in the same wafer, the measured concentration of Cr will be too low. Even though Cr has a low equilibrium segregation coefficient, some Cr is still expected to be found at 50 % ingot heights.

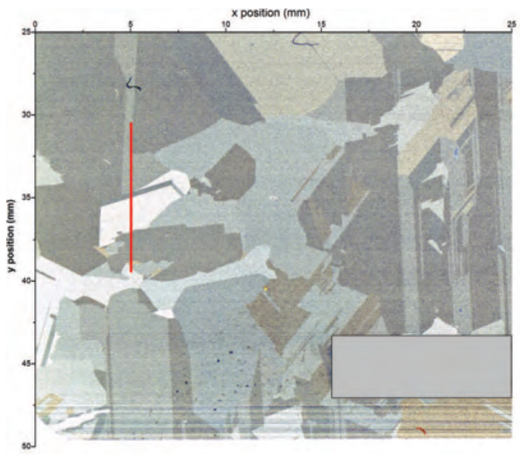
Section 2.4.2 explained that the recombination activity lies in the type of precipitates formed during and after annealing. The present section will compare the lifetime and the resistivity measured in samples A2A6, A3B9, A3C and M2D, showing the crystal symmetry and the effect of crystalline defects.

The electrical activity at the grain boundaries has been investigated by a FPP. A line has been measured twice, once before P gettering and once after P gettering over all nine samples.

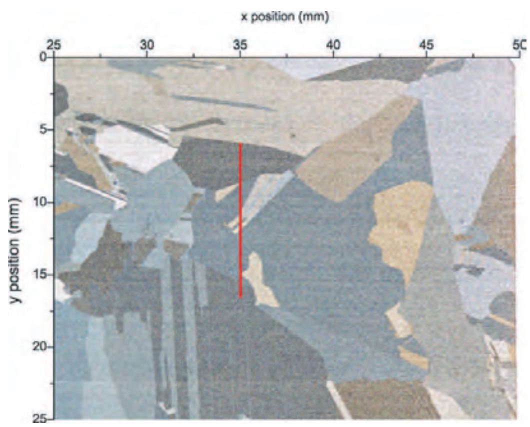
The results will be given as resistivity profiles with corresponding pictures of the measured path above each plot. Impurity accumulation at grain boundaries and at twins will be discussed in terms of the resistivity and the minority carrier lifetime. Four samples will be presented here, the last five are found in Section A in the Appendix.

4.5.1 Grains and grain boundaries

Sample A3C and sample A3B9 shown in Figure 4.3(a) and Figure 4.3(b), respectively, will be discussed in the following section.



(a) Sample A3C.



(b) Sample A3B9.

Figure 4.3: Samples from wafer A3. Red line indicating the path along which the resistivity has been measured.

Sample A3C has a region between 32-36 mm in the y direction (x = 5 mm) where no values for the resistivity could be obtained before gettering. This is shown in Figure 4.4.

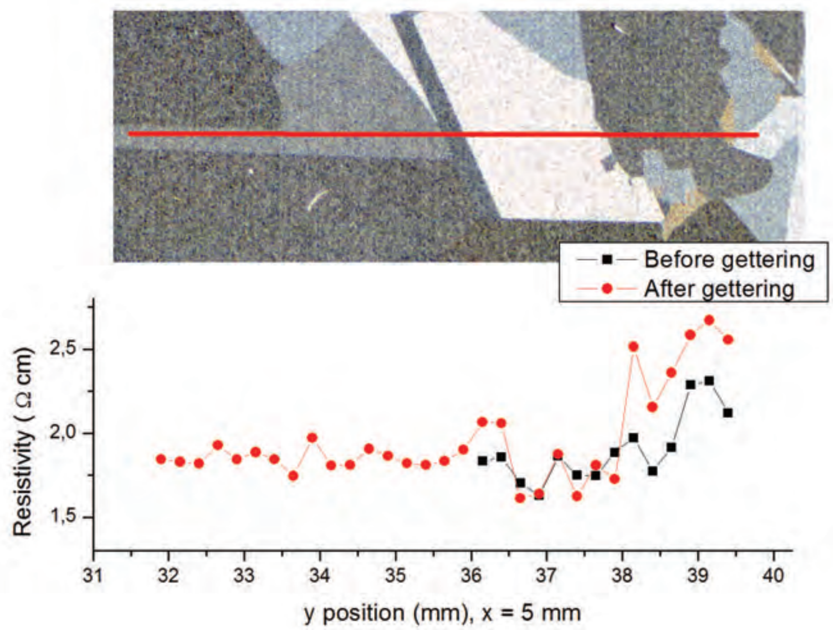


Figure 4.4: Resistivity and the corresponding measured path from Figure 4.3(a) are indicated. The resistivity was measured both before and after gettering of sample A3C.

The resistivity was possibly too high to be measured in this region by the probe before gettering, implying that no current could be passed through the sample. Signal was obtained when the probe crossed over to a neighboring grain at x = 36 mm. The resistivity increased at x = 38 mm when crossing a new boundary. This indicates that there is accumulation of electrical active impurities at the boundaries, and that even more impurities are found at the same spot after gettering.

The lifetime both before and after P gettering is presented in Figure 4.5, where the drawn line represents the measured resistivity path.

It is a clear correspondence between the resistivity in Figure 4.4 and the lifetime in Figure 4.5. An error of ±0.5 mm in positioning the drawn line in the picture relative to the true measured path is reasonable. It is thus reasonable to assume that the lower lifetime found at 37 - 39 mm is in the same region as the resistivity peaked,

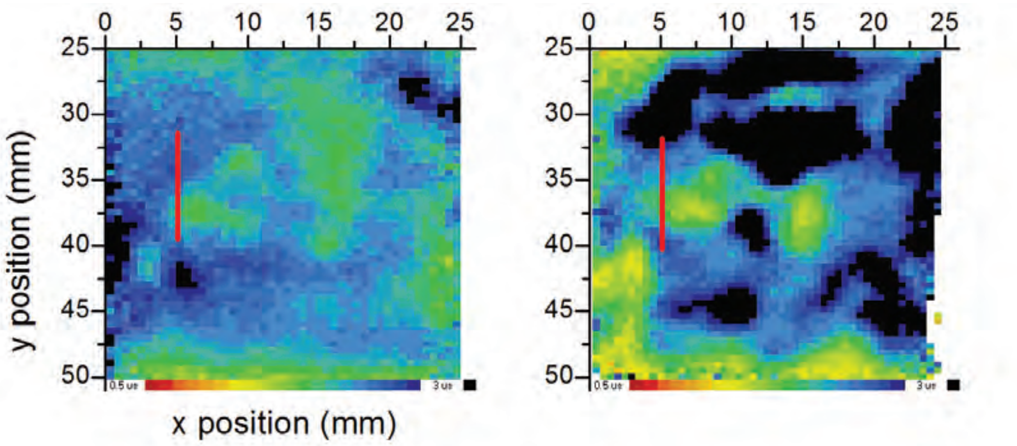


Figure 4.5: Lifetime map before (left) and after (right) P gettering of sample A3C.

Sample A3B9 seen in Figure 4.6, shows the same relation between resistivity and lifetime as sample A3C.

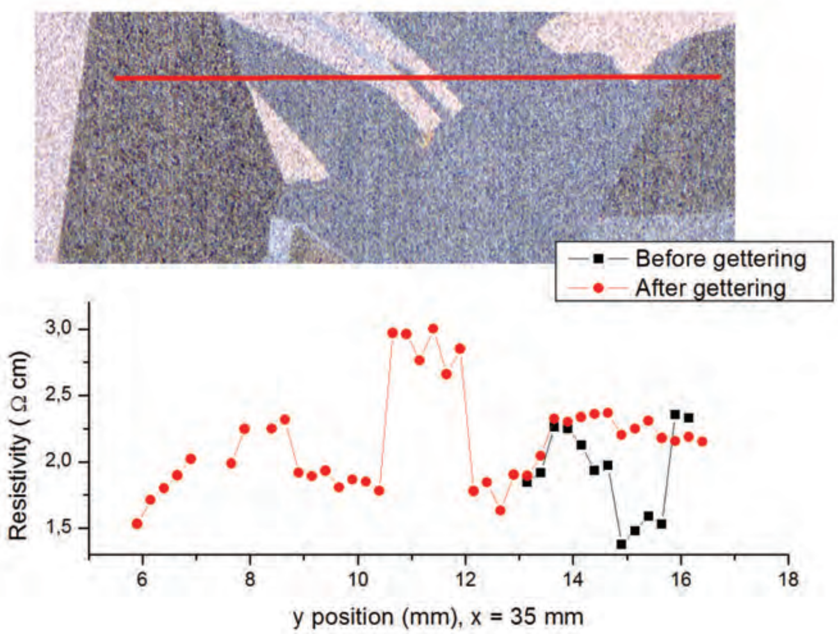


Figure 4.6: Resistivity and the corresponding measured path from Figure 4.3(b) are indicated. The resistivity was measured both before and after gettering of sample A3B9.

A region where no resistivity values could be obtained is present also here. No current was passed through between 6 - 13 mm in the y-direction (x = 35 mm) before P gettering. A peak occurred while crossing a thin grain at about 11 - 12 mm due to a higher impurity concentration.

Buonassisi et al. [52] reports that annealing with following slow cooling may result in widely and homogeneously distributed precipitates at micro defects within grains. They are usually formed as silicides, oxides or as carbides and have higher recombination activity than smaller precipitates located at grain boundaries and dislocations.

This is possibly observed for a grain situated about y = 11 - 12 mm which shows a high increase in resistivity. The accumulation of impurities is a consequence of the orientation of the neighboring grains, potentially forming a high-angle boundary which is a known gettering site for impurities.

The region between 14 - 16 mm shows an increase of about 1 Ωcm after P gettering. This region may be a favorable spot for phosphorus to precipitate, hence increasing the resistivity and the lifetime seen in Figure 4.7. As mentioned earlier, MacDonald et al. [51] found that the lifetime increase in p-type compensated silicon when high phosphorus concentrations are added.

A decrease in lifetime at about y = 11 mm, is the same spot whereas the resistivity peaked after gettering.

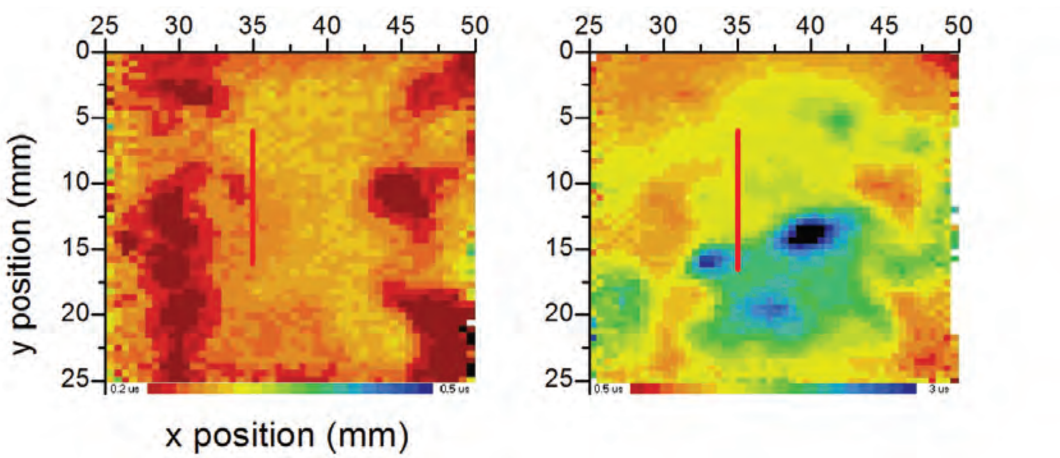


Figure 4.7: Lifetime map before (left) and after (right) P gettering of sample A3B9.

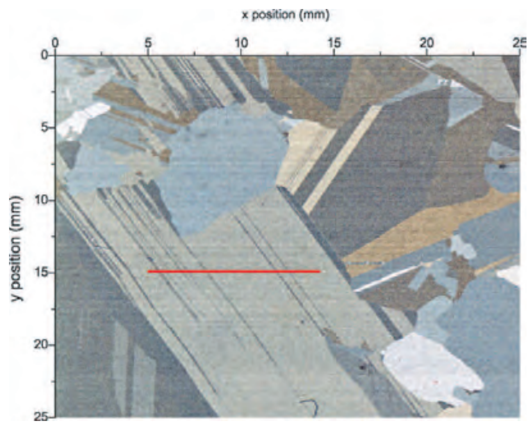
There are thus some grain boundaries which are more effective gettering sites for phosphorus than others.

It has been found that the lifetime generally decrease in areas where high impurity concentrations are present, i.e. areas with higher resistivity.

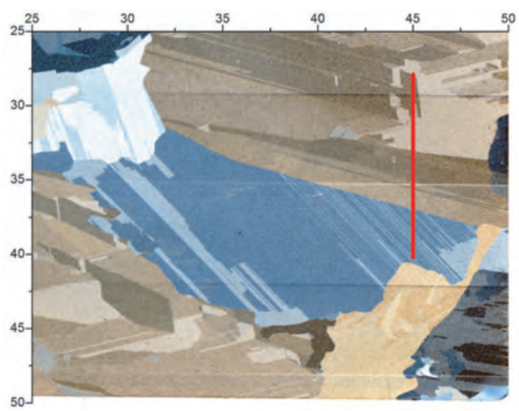
Additional observations are that the grain boundaries in sample A3B9 show a higher tendency of particle accumulation, which is related to the pre-annealing of this sample, where more impurities are expected to have segregated at the boundaries before the P gettering process.

4.5.2 Twins

Sample A3A6 and sample M2D shown in Figure 4.8(a) and Figure 4.8(b), respectively, will be discussed in the following section.



(a) Sample A3A6.



(b) Sample M2D.

Figure 4.8: Samples from wafer A3 and wafer M2. Red line indicating the path along which the resistivity has been measured.

Sample A3A6 has no obtained resistivity values in the region between 5 - 10 mm in the x-direction (y = 15 mm) before P gettering, as seen in Figure 4.9. After gettering, resistivity values were obtained and the region is thus ”cleaner” after gettering.

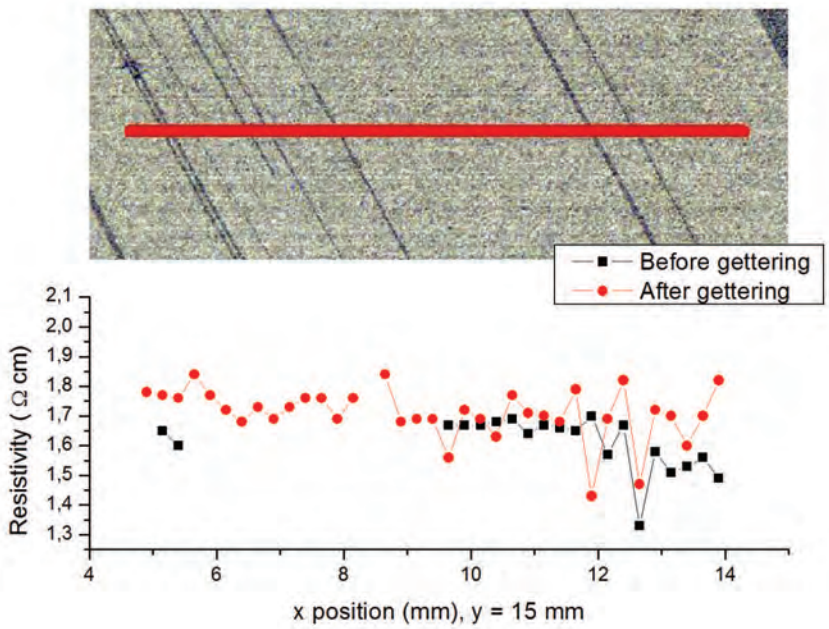


Figure 4.9: Resistivity and the corresponding measured path from Figure 4.8(a) are indicated. The resistivity was measured both before and after gettering of sample A3A6.

The region between 12 - 13 mm contains two twin planes, which is the same spot as where two peaks and two dips occur relative to the resistivity outside the region. Thus, impurities are precipitated at the twin planes and are still present after P gettering.

Lifetime maps of the samples both before and after P gettering are given in Figure 4.10. A relation between the resistivity and the lifetime is also found here. The region where no resistivity values were obtained before gettering, show a lower lifetime relative to neighboring grains. The region between 10 -

12 mm is the region where the resistivity is stable, and where a higher relative lifetime is measured. The lifetime drops when crossing the twin planes at about 12 - 13 mm.

Publications by Buonassisi et al. [53] have shown that twins ($\Sigma 3$ boundaries) are less electrical active than higher order grain boundaries. Twins have the highest degree in symmetry, with every 3rd atom in common. In general, metal precipitate decoration tends to increase with decreasing degree of atomic coincidence in the grain boundary plane (increasing Σ values) [18].

The results discussed above show that the twins in sample A3A6 have a high electrical activity. This is due to the pre-annealing process at 600°C which has gettered more impurities to the twin planes, thus leading to higher electrical activity and lower lifetimes.

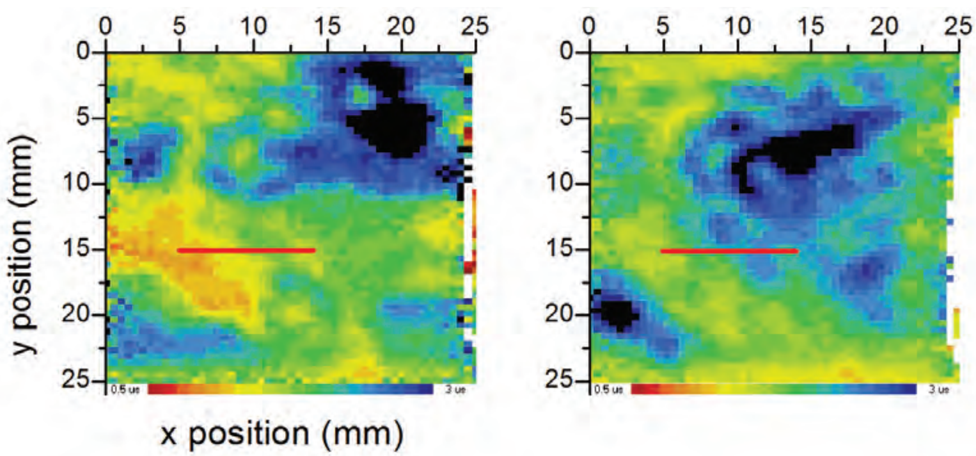


Figure 4.10: Lifetime map before (left) and after (right) P gettering of sample A3A6.

Sample M2D has a twin region at about 34.5 - 37 mm in the y-direction (x = 45 mm). Figure 4.11 shows that this region has a stable resistivity before gettering, with an increased electrical activity after gettering. The region between about 32 - 33 mm show a slight decrease in the resistivity.

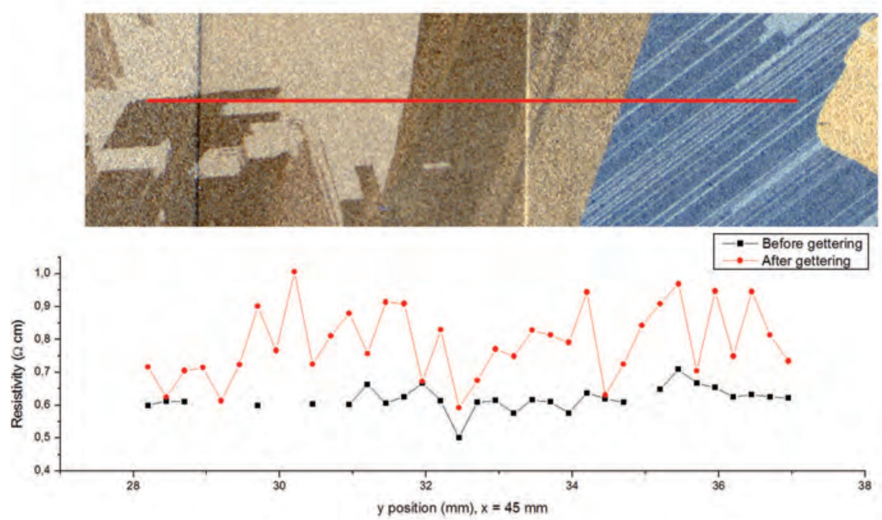


Figure 4.11: Resistivity and the corresponding measured path from Figure 4.8(b) are indicated. The resistivity was measured both before and after gettering of sample M2D.

The same regions are then compared with the lifetime maps in Figure 4.12. The lifetime along the measured path is relatively constant, only the region about 32 - 33 mm shows a higher lifetime. This is the same region where as the resistivity dropped. The twin region at 34.5 - 37 mm does not show any significant increase in the lifetime compared to the other regions.

Wafer M2 contains a higher amount of chromium impurities, which is a faster diffuser than for instance Al, B and P. This leads to a low and uniform lifetime map before gettering, as seen in Figure 4.12. The impurities are thus well distributed, which is seen as a quite constant resistivity profile before gettering.

The electrical activity has increased dramatically after gettering. Chromium

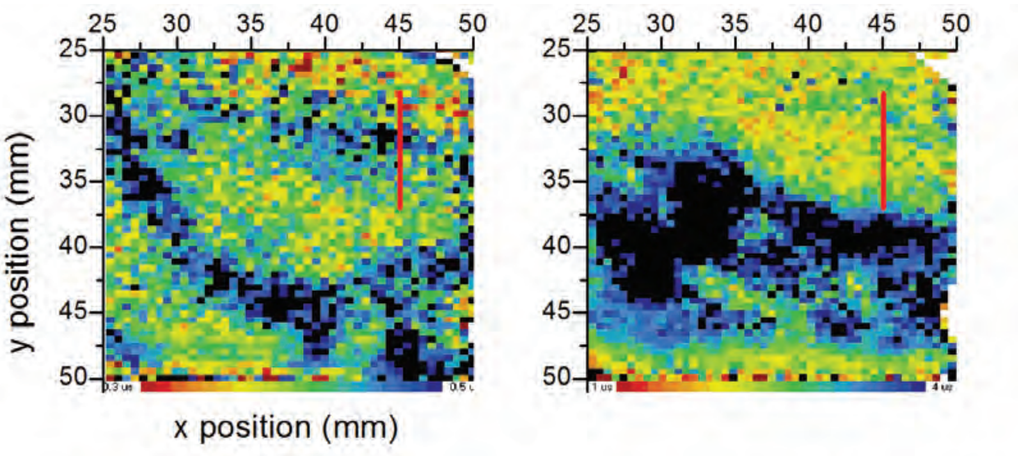


Figure 4.12: Lifetime map before (left) and after (right) P gettering of sample M2D.

impurities have now segregated at twin planes and grain boundaries, thus enhancing other regions in terms of the lifetime. This is seen as more distinct regions in the lifetime map after gettering.

Chapter 5

Conclusion

A new method has been established to study electrical activity and lifetime of multicrystalline silicon samples. Investigations have been done by a simple technique such as resistivity measurement using a Four Point Probe (FPP), with a probe spacing of 1.6 mm, and by lifetime mapping using Microwave Photo Conductance Decay (μW-PCD).

Three types of compensated multicrystalline silicon materials have been investigated (A2, A3 and M2) which all have different level of impurities, where M2 has a higher level of chromium. Generally, a phosphorus diffusion (P) gettering step at 890°C for 100 minutes is very effective at removing fast diffuser impurities (e.g. Fe, Cr) from multicrystalline silicon, hence resulting in higher lifetimes after gettering.

A two-step process has been applied to investigate how a pre-annealing treatment before P gettering would influence the electrical activity and the minority carrier lifetimes of the samples.

Resistivity and minority carrier lifetimes were compared before and after annealing at 600°C and at 900°C, which generally showed an increasing resistivity and decreasing lifetime with increasing annealing temperature due to out-diffusion of impurities.

The resistivity has increased for all pre-annealed samples after P gettering, including for non-annealed samples. This is due to a higher level of phosphorus and to out-diffusion of impurities, hence reducing both the net dopant density and the mobility, and increasing the minority carrier lifetimes. For a better dissolution of metallic precipitates, phosphorus diffusion gettering should be performed directly after annealing.

It has been observed that the enhancement in lifetime after P gettering was highest for non pre-annealed samples.

The in-diffusion depth of phosphorus during the gettering process has been improved by introduced defects as a consequence of resistivity measurements before gettering, and as an effect of pre-annealing at 900°C. The higher concentration of phosphorus lead to augmented lifetime of the specific sample, from $(0.2\pm0.1)\mu$s to $(3.6\pm1.5)\mu$s. The standard deviation in lifetime reflects the spread in high and low lifetime regions in the sample.

The electrical activity at grain- and twin boundaries were studied before and after gettering in relation to annealing temperature.

Accumulation of metallic impurity precipitates at defects in the materials, affecting the electrical activity, has been found from a change in both resistivity and lifetime. A good correlation between grain structure, resistivity- and lifetime profiles has thus been established.

Appendix A

Additional results

This chapter will give additional results which are not included in the Results and Discussion chapter in this thesis. They show the same tendency in terms of particle precipitation at defects, the same relation between resistivity and lifetime, and give thus no new information.

Table A.1 gives full size pictures of the samples that are mentioned in the results and discussion section, but served no use in terms of the discussion.

Additional resistivity results measured with a FPP and lifetime maps of the samples presented in Table A.1 are also included. The uncertainty in the resistivity measurements are presented in form of two resistivity paths, that show a consistency in the resistivity profile. The lifetime maps show a large spread in carrier lifetime, which is presented as histograms.

Two sister wafers are included, which show that two wafers taken from the same ingot height have the same crystalline structure.

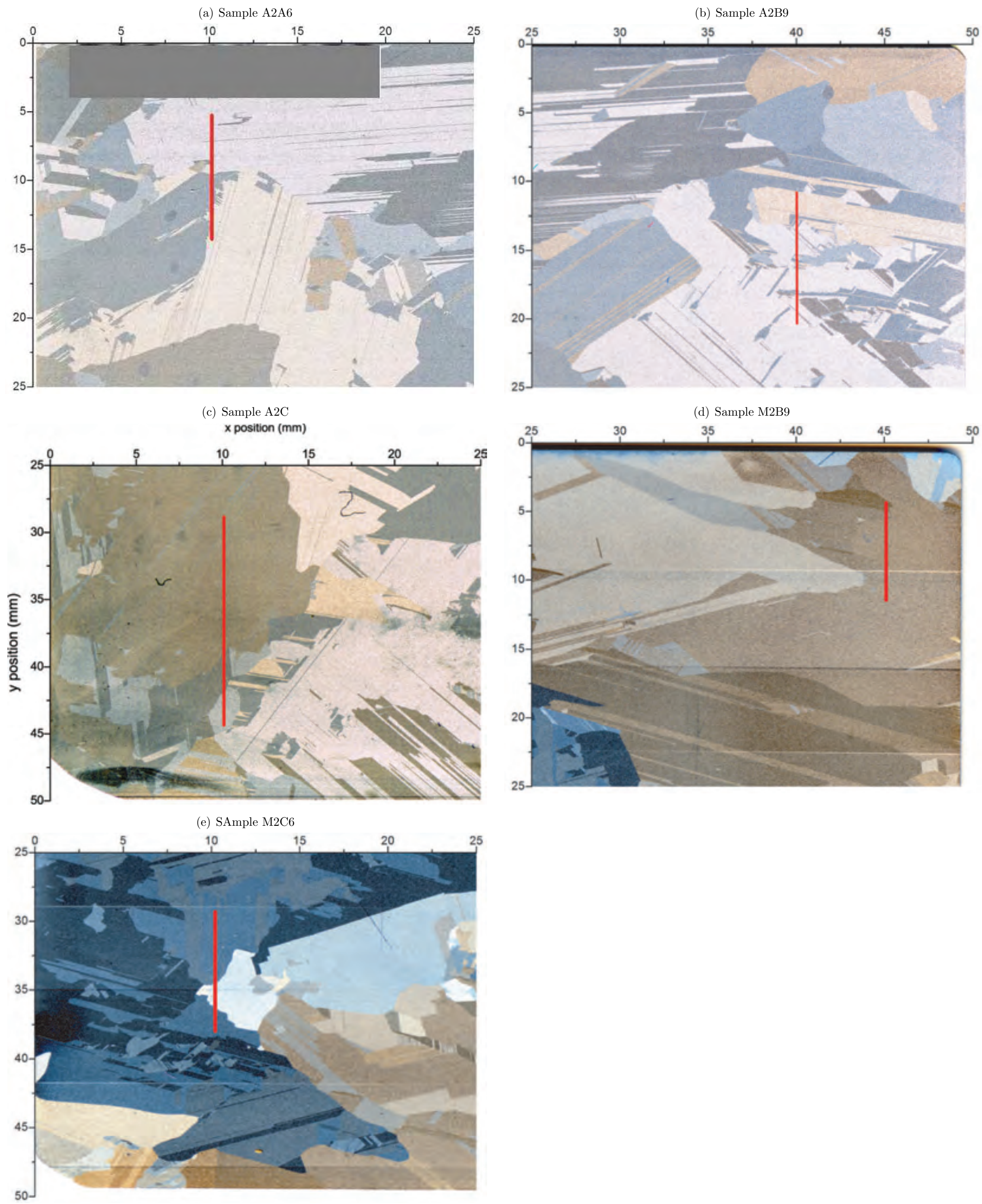


Table A.1: Additional samples. Red lines indicate the measured resistivity paths.

Additional resistivity results (FPP)

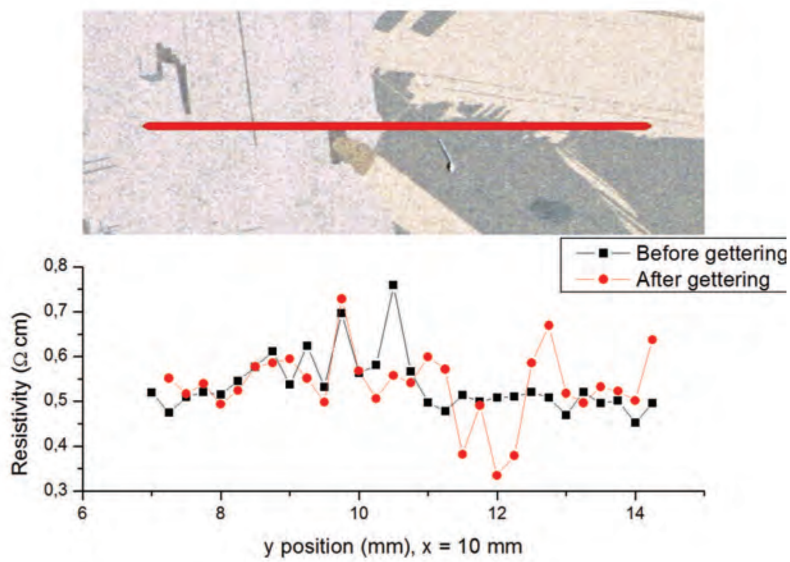


Figure A.1: The resistivity along the path measured across sample A2A6 both before and after gettering.

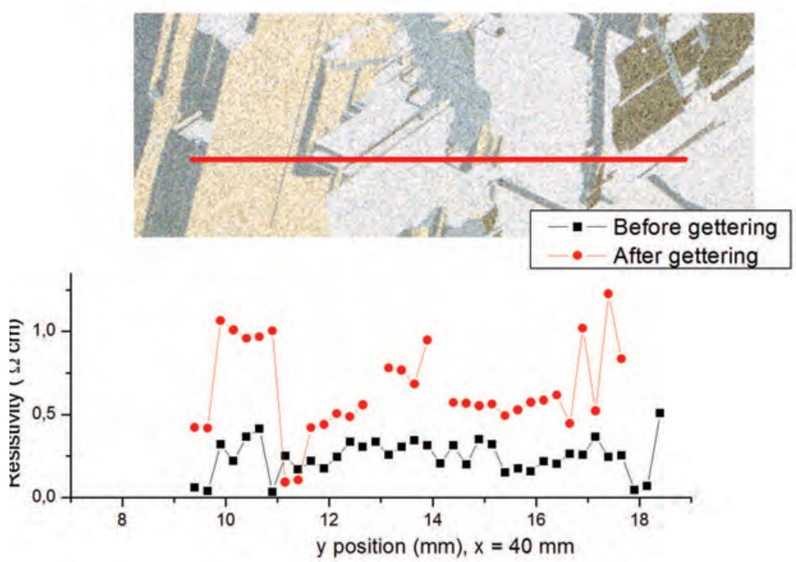


Figure A.2: The resistivity along the path measured across sample A2B9 both before and after gettering.

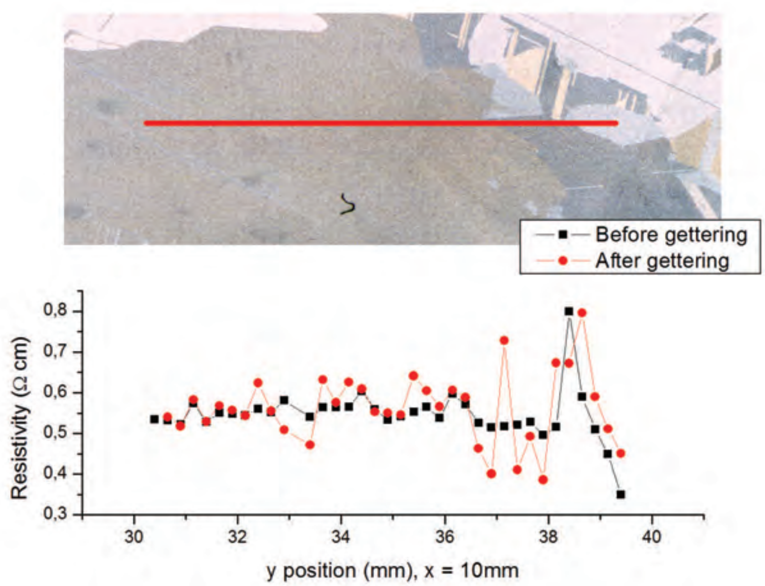


Figure A.3: The resistivity along the path measured across sample A2C both before and after gettering.

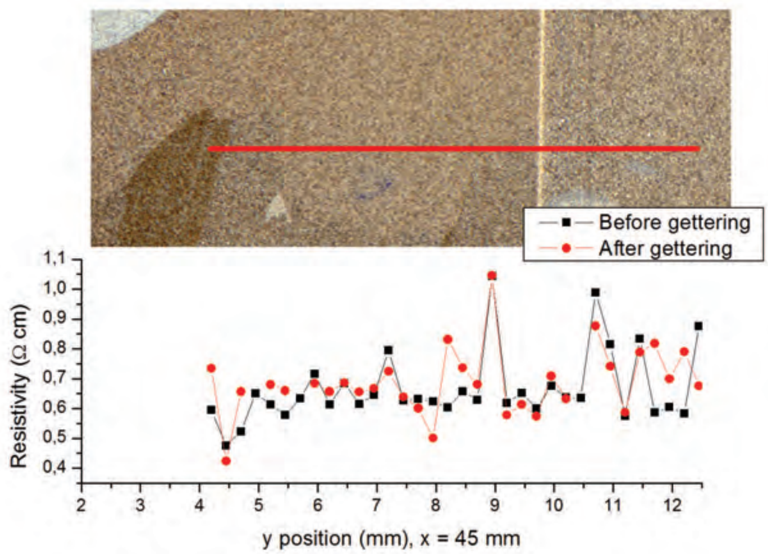


Figure A.4: The resistivity along the path measured across sample M2B9 both before and after gettering.

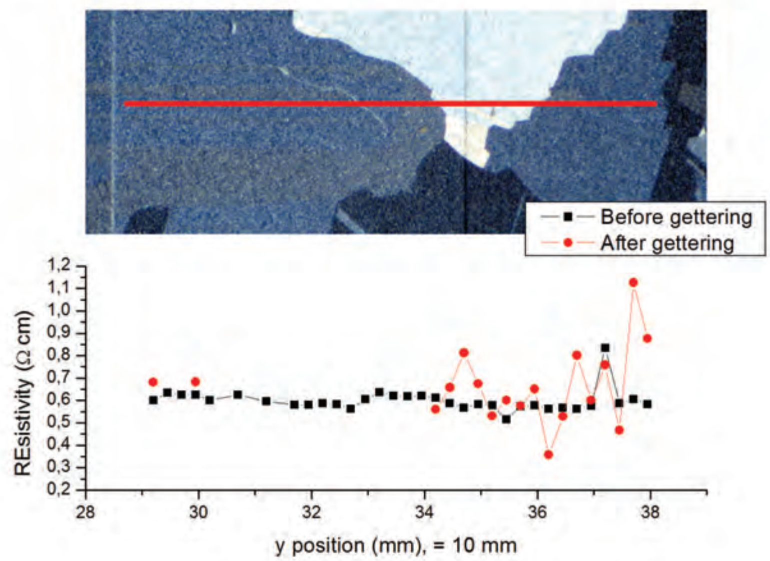
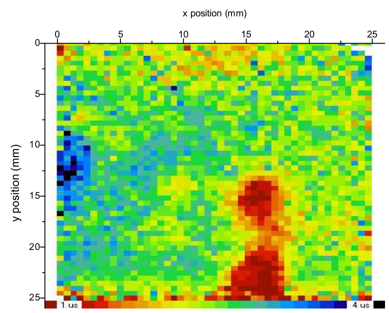
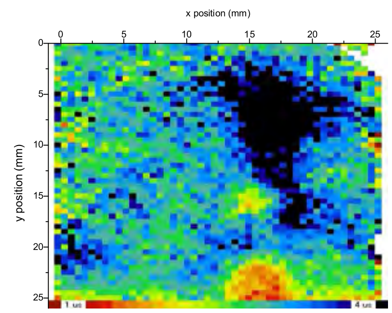


Figure A.5: The resistivity along the path measured across sample M2C6 both before and after gettering.

Additional lifetime results

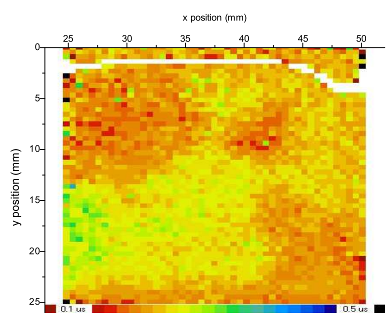


(a) Lifetime map before gettering.

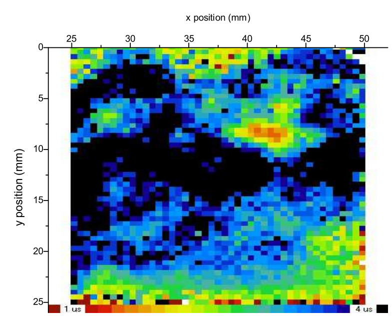


(b) Lifetime map after gettering.

Figure A.6: Figures indicating the spatial lifetime maps of sample A2A6 a) before gettering and b) after gettering.

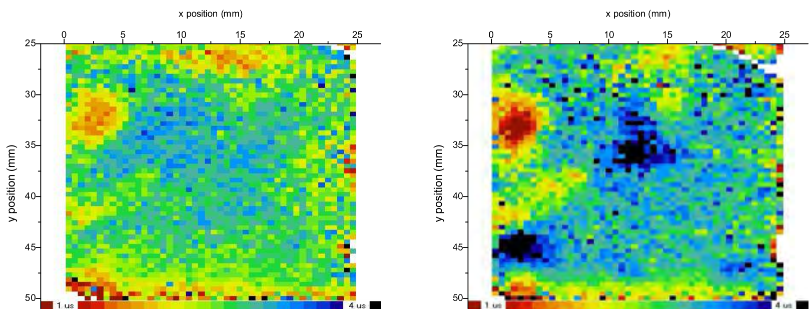


(a) Lifetime map before gettering.



(b) Lifetime map after gettering.

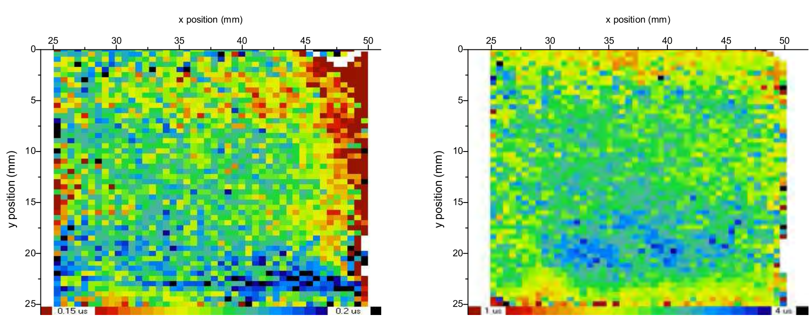
Figure A.7: Figures indicating the spatial lifetime maps of sample A2B9 a) before gettering and b) after gettering.



(a) Lifetime map before gettering.

(b) Lifetime map after gettering.

Figure A.8: Figures indicating the spatial lifetime maps of sample A2C a) before gettering and b) after gettering.



(a) Lifetime map before gettering.

(b) Lifetime map after gettering.

Figure A.9: Figures indicating the spatial lifetime maps of sample M2B9 a) before gettering and b) after gettering.

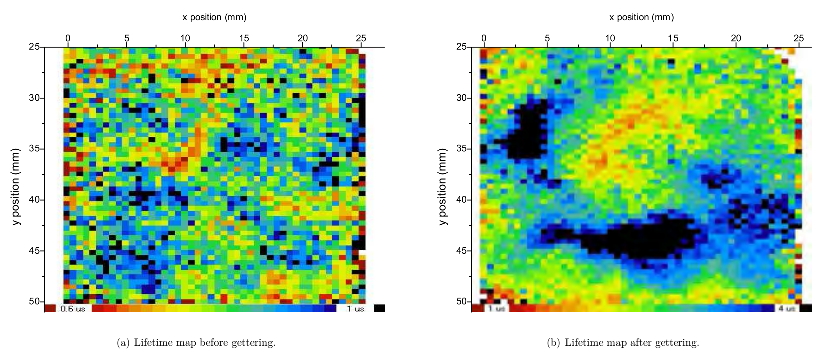
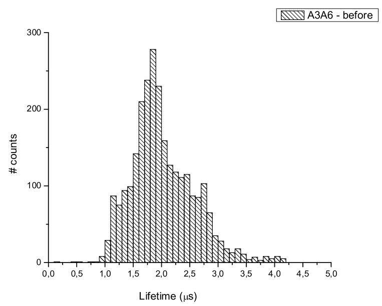


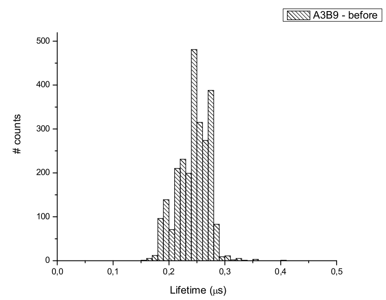
Figure A.10: Figures indicating the spatial lifetime maps of sample M2C6 a) before gettering and b) after gettering.

Uncertainty - Lifetime

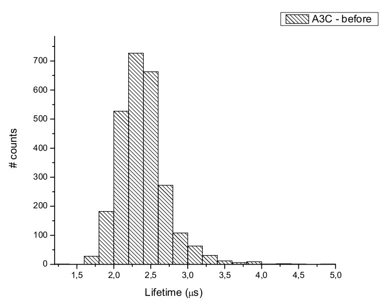
The spread in the lifetime map is shown in Figure A.11 before P gettering, and in Figure A.12 after P gettering.



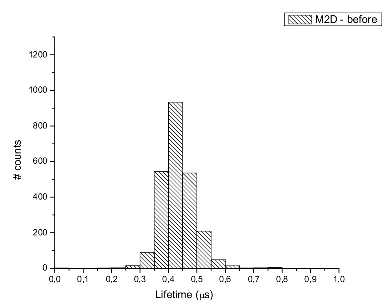
(a) Sample A3A6



(b) Sample A3B9

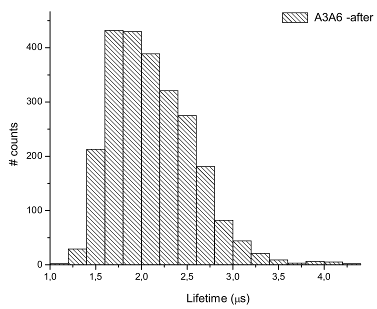


(c) Sample A3C

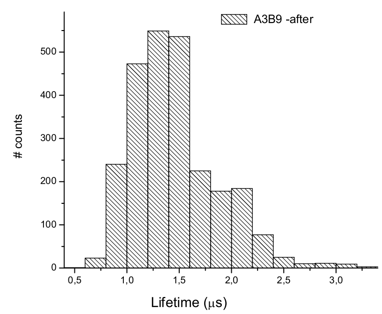


(d) Sample M2D

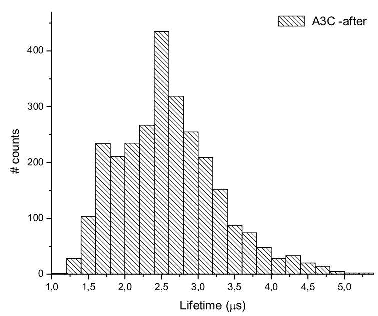
Figure A.11: Histogram showing deviation in lifetime between pixels in the lifetime maps. Here shown for samples *before* P gettering.



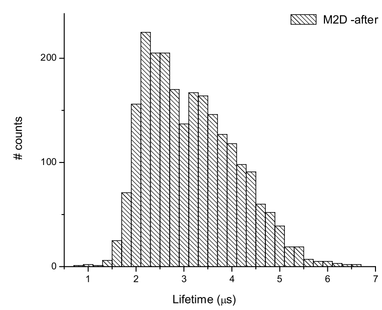
(a) Sample A3A6



(b) Sample A3B9



(c) Sample A3C



(d) Sample M2D

Figure A.12: Histogram showing deviation in lifetime between pixels in the lifetime maps. Here shown for samples *after* P gettering.

Uncertainty - Resistivity (FPP)

Resistivity profiles measured multiple times alon the same line using the FPP is shown in Figure A.13 and in Figure A.14.

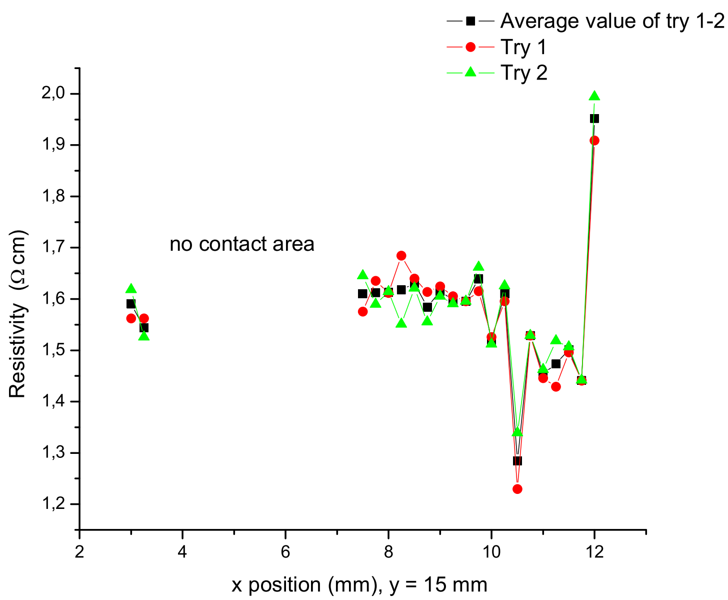


Figure A.13: Graph showing the deviation in resistivity of sample A3A6 along the same path measured two times using a FPP. The average resistivity is the resistivity plotted in Figure 4.9.

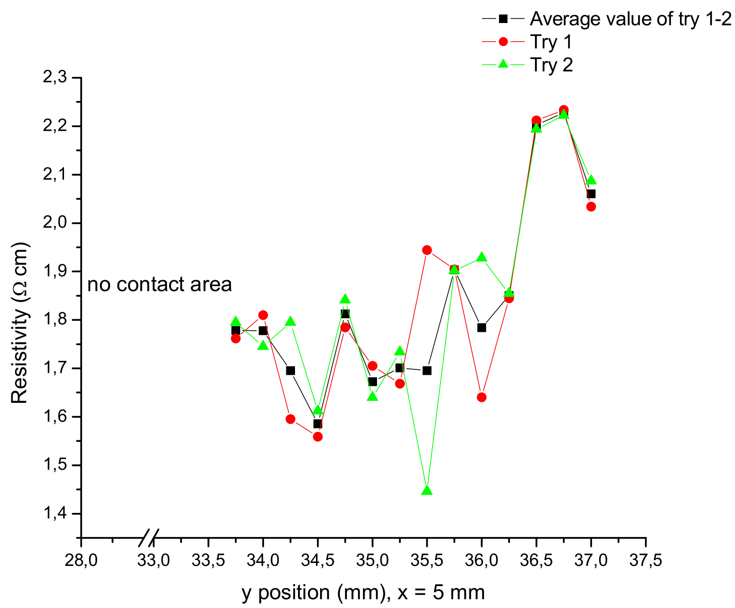


Figure A.14: Graph showing the deviation in resistivity of sample A3C along the same path measured three times using a FPP. The average resistivity is the resistivity plotted in Figure 4.4.

Sister wafer

Two sister wafers are shown in Figure A.15.

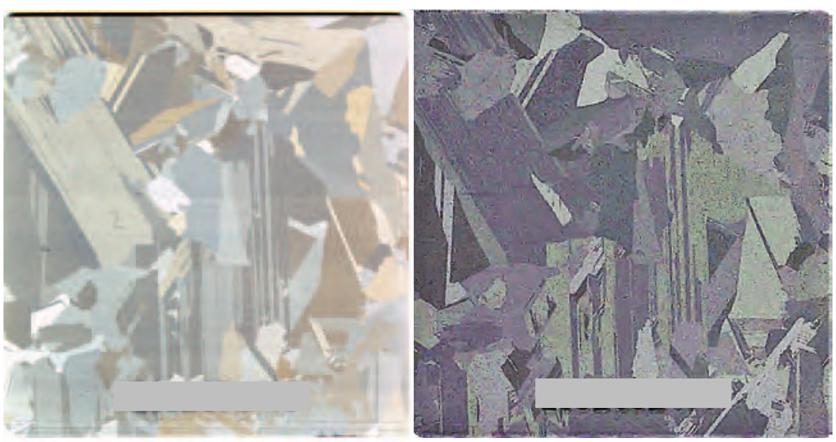


Figure A.15: Sister wafers; A3-140 and A3-141.

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