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Science and Technology

Low Power Electronic Paper Display Driver with Unipolar Driving Waveform

Mattis Spieler Asp

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Supervisor: Per Gunnar Kjeldsberg, IES
Co-supervisor: Snorre Aunet, IES
Øystein Moldesvor, Disruptive Technologies

Norwegian University of Science and Technology
Department of Electronic Systems

NORWEGIAN UNIVERSITY OF SCIENCE AND TECHNOLOGY

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Master thesis

Faculty of MTEL
Department of Electronics and Telecommunications

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Problem Description

New types of displays allow for extremely small power dissipation as long as the image is static. These types are often referred to as "electronic paper displays". Such displays are interesting for IoT applications, as they would allow display of images or messages when little power is available.

.Implementation of a level shifter for an electronic paper display driver.

An important part of the low-power electronic paper display (EPD) driver is the level shifter. The level shifter converts logical input to analog output. This is the analog input for the horizontal (source) and vertical (gate) lines in the electronic paper display. In the case of an EPD, this analog output is discrete. The EPD requires a minimum voltage of 5 volt over the electrodes to drive the pixel between states. A common practice is to attach one electrode on every pixel to a common ground and vary the other electrode above or below ground to change between black and white color. It is the duration of the applied voltage that variates the pixel gray level in any specified voltage domain. The voltage, if above minimum, can be varied to reach a higher level of color intensity/extreme in the black/white domain.

A master thesis carried out in the spring 2016, and a project thesis carried out in the fall the same year, analyzed in depth the feasibility of an alternative unipolar driving waveform for the pixel electrodes. It showed that the unipolar waveform can potentially save 73% power in a 360X480 sized display. The unipolar driving waveform exploits a second compliment level shifter connected to the common electrode, replacing ground. To switch color, the compliment level shifter will be the inverse of the source voltage. With this second level shifter, each level shifter can reduce the output voltage by two, and still keep the minimum voltage required to change pixel state.

The assignment will start with a study of different level shifter concepts. Based on the specific requirements of an EPD, a low power level shifter shall then be designed and simulated in a design environment of choice. The power consumption of the level shifter

shall be estimated and compared with state of the art solutions.

Co-supervisor: Øystein Moldsvor, Disruptive Technologies

Co-supervisor: Professor Snorre Aunet, NTNU

Supervisor: Professor Per Gunnar Kjeldsberg, NTNU

NORWEGIAN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Abstract

Faculty of MTEL
Department of Electronics and Telecommunications

Master thesis

by Mattis Spieler Asp

Electronic paper display (EPD) has reached a position of great maturity. Due to its capability of bistability and great reflectivity it can display an image without any flowing current. Today, sensors and regulators are being placed out to monitor the real world, and are often battery powered without a display. With the introduction of electronic paper displays these units can be given a display without a significant increase in power. There is however still very limited power available, and power reduction is considered increasingly important.

A theoretical and practical analysis of EPD, Thin-Film Transistor, and level shifters have been used to investigate power reduction techniques. The area of interest is the sub circuits where level shifters are adopted. These sub circuits typically carry over 60% of the total power consumption during an electronic paper write cycle. Practical experiments and simulations have been used to find new power saving level shifters for these sub circuits.

The simulations have been successfully used to show different level shifters performing and running at two different frequencies (10MHz and 2Hz) using commercially available 180nm technology. The results from the simulations in Cadence Virtuoso have shown that the proposed circuits perform about 80% - 85% better in terms of power at high frequency (10MHz). The results also show that the proposed circuits perform about 65% - 150% worse in terms of power at low frequency (2Hz).

From the results we have concluded that the proposed circuits are not better in low frequency applications such as electronic paper displays. However storage capacitors can be added to electronic paper pixels which can potentially speed up the scan process, thereby making these results more applicable.

Preface

The presented dissertation is created by Mattis Spieler Asp.

The idea behind the project came from a specialization project in the NTNU subject TFE4520, conducted in the Autumn semester of 2017. In this specialization project, a circuit board capable of driving electronic paper was created. The results showed that it was possible to achieve a remarkable power stringent electronic paper driver saving up to 75% of the previously used power given a worst case image update. In collaboration with professor Per Gunnar Kjeldsberg at NTNU, professor Snorre Aunet at NTNU, and Øystein Moldesvor at Disruptive Technologies AS the idea was further developed. The results were a simulation on chip of the major sub components of the electronic paper driver.

The required software for the simulation was not accessible before one week before deadline. Four trials were conducted with full implementation in the software during the semester, and significant delays where encountered due to software malfunction. The project continued as a literature study, and without any supporting software five new circuits were developed manually. These circuits were closely based on previous articles found during literature study. When the simulation worked, two of the circuits showed excessive power usage and malfunction in the specific process environment, however three remained successful and the results where presented.

Trondheim, 2016-06-28

Mattis Spieler Asp

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I would first like to offer my special thanks to my supervisor Per Gunnar Kjeldsberg for taking the time to guide the project in this period. Per Gunnar has contributed by giving me guidance on the overall report structure, as well as reviewing my progress through the semester.

I am particularly grateful for the extra support given by my co-supervisor Snorre Aunet on circuit advice and motivating me throughout this project. Snorre Aunet has been available for questions, and helped me concerning circuit problems.

My special thanks goes to Øystein Moldesvor, and his team of engineers at Disruptive Technologies AS for their advisory in this project. Øystein has helped me with architectural design, as well as supported me with a workplace during the last part of the semester.

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Abbreviations

OLED	**O**rganic **L**ight **E**mitting **D**isplay
LDO	**L**ow **D**ropout
MCU	**M**icrocontroller **U**nit.
PARC	**P**alo **A**lto **R**esearch **C**enter
PCB	**P**rinted **C**ircuit **B**oard.
SOC	**S**ystem **O**n **C**hip.
SOP	**S**ystem **O**n **P**anel.
PM	**P**assive **M**atrix
RAM	**R**andom **A**ccess **M**emory.
TFT	**T**hin **F**ilm **T**ransistor.
SPI	**S**erial **P**eripheral **I**nterface.
IoT	**I**nternet **o**f **T**hings.
RTL	**R**esistor **T**ransistor **L**ogic.
CCLS	**C**apacitor **C**oupled **L**evel **S**hifter.
IC	**I**ntegrated **C**ircuit.
I/O	**I**nput / **O**utput
DC	**D**irect **C**urrent
AM	**A**ctive **M**atrix **PM**
Passive **M**atrix	
VCOM	**V**oltage **C**ommon
GND	**G**round

Chapter 1

Introduction

Today computers are the backbone of society, largely due to the display which gives a straightforward way of operating a wide spread of tasks on the computer. The reason for the display popularity is that it can completely rearrange colors, text, and figures to fit the task the operator requires. Lately there has been a steady increase of low power computer chips which operate tasks such as sensors, motors, and communication. The frequency of the interactions with computer chips are low, ranging from hourly to monthly which is why they often run on battery and are placed remotely often without display to save power.

The dominating display on the market is the Liquid Crystal Display (LCD) [10, P.14]. This type of display generally needs high refresh rates and backlighting, which makes them unsuitable for low power devices. An alternative that dates back to the early 1970s is called the Electrophoric Paper Display (EPD). This display uses the reflectiveness of the particles in the pixels to display the image. The EPD is completely independent of an external power source once the image is formed which is known as bistable behaviour. Because of the low power properties of EPD, it would be interesting to integrate it with low power computer chips.

This chapter will give an introduction to the topic area for this thesis. The project motivation is first presented, which explains the reason why this work is important for designing a low power display driver. The project goal is then presented to set the expectations or aim for this thesis. The chapter outline will go through the chapters, and should help the reader navigate through this thesis. Lastly the main contributions has been added from the work done by the author.

1.1 Problem Description

Adding a display to small sensors and controllers powered by computer chips have been desired in Internet of Things (IoT) applications for several reasons. These devices operate remotely, and may fail, be reconfigured, and should be inspected. Adding a display will give these devices an opportunity to be identified, and can display messages and figures that helps the operator. A tradeoff between lifetime and operational convenience will usually end up prioritizing the lifetime because the intended lifetime is several years. For this reason the display will rarely be implemented because of its significant power increase.

1.2 Motivation

A new type of display called the Electrophoric Display (EPD) has reached a remarkable state of maturity. The image quality is high and operating voltage has reached a low of 5V. The larges benefit of the Electrophoric display is known as the bistable property, and allows images to be contained with no flowing current. Because the electrophoric display is already considered very low power, most publications are leaned to higher refresh rate, and better image quality [11] [12] [13] [14] [15]. This thesis will investigate the use of unipolar driving waveform to achieve lower power consumption. Unipolar voltage means that voltage over a load, drop from a positive voltage v_1 to an equal but negative voltage v_2. Such that $\|\mathrm{v}_1\| = \|v_2\|$ but $v_1 \neq v_2$. Unipolar waveform means that the polarity over the load can change in a waveform, such that v_1 changes to negative and v_2 changes to positive voltage. The design focus is to achieve a new architecture capable of unipolar output, that occupies small area and use low power.

1.3 Project Goals

Before the display driver may be implemented on chip the submodules of the driver should be investigated. With consideration of the new driving waveform (unipolar), various requirements and limitations of the display driver will be reviewed. The overall project goal is to prepare a unipolar display driver for integration on chip. The level shifter which holds an integral part of the display driver should be considered for power optimization. The tasks listed below highlight the areas of interest:

- Investigate and define the operation of a display driver.

- Use the information to describe the most power consuming parts of the display driver.
- Investigate level shifters that can replace conventional level shifters with less power consumption.
- Consider how a unipolar architecture will affect the gate driver.
- Model the subcircuits in Cadence Virtuoso to find the improvements.

1.4 Chapter Outline

The first **Chapters 2 to 3** is based on a literature study, where the background and working principles of EPD are described. **Chapter 4 and 5** is a collection of new low power sub circuits that will support unipolar driving waveform.

Chapter 2 introduces the principles of the electrophoric display and how it is electrically driven.

Chapter 3 will assess papers and books that has covered the electrophoric display and related issues. The electronic paper display has been around for several decades [16], and there has been many contributions over the years in this field. This chapter covers many topics which form a basis for the thesis. The contributions help define which part of the driver should be subject to optimization.

Chapter 4 is considered the main topic of this thesis. A low power source driver is obtained by reducing power consumption in level shifters. Three level shifters have been described in this chapter.

Chapter 5 investigate the gate driver in the circuit, which is affected by the change to a unipolar driving waveform. The gate driver is responsible for allowing or stopping current from entering the pixel, which is closely connected with the source driver.

Chapter 6 will present and discuss the results of a simulation of five level shifters. This is done in three steps, (1) steady state, (2) transition from steady state to transient, and (3) transient. The last part of this chapter will present the gate driver.

Chapter 7 The project goals are concluded. Further Work is presented.

1.5 Main Contributions

The main contributions made by the author is listed below.

- Negative Capacitor Coupled Level Shifter(CCLS) (Chapter 4.1)
- Optimizing the level shifter for CMOS technology (Chapter 4.2)
- Discovered gate driver properties which is optimized for unipolar driving waveform (Chapter 5.3)
- Current Properties in Electrophoric Display (Chapter 5.2)
- A new gate driver for Electrophoric Display (Chapter 5.3)
- Modeling sub circuits and presentation of results 6

Chapter 2

Introducing the Electrophoric Display

The electrophoric display (EPD) was introduced firstly to mimic the need for ordinary ink on paper. It has the benefit of good reflectivity, wide viewing angle, being thin, lightweight and having high power efficiency [12]. This chapter will present some general information of the electronic display.

2.1 History of Electrophoric Paper Display

The 'electronic paper display' is dated back to 1970s [16], first created in Xerox's Paolo Alto Research Center (PARC). The paper display was patented by Nick Sheridon, and the technology was called Gyricon. The Gyricon uses the principle of rotating beads encapsulated in an oil-filed cavity.

In the late 1980s, the personal computer and printer started to hit the marked. A consequence of this was an increase in the total paper consumption, and researchers began to see the need for electric paper. The Gyricon was thought of as a good candidate to replace ordinary ink on paper. In 1997, E-Ink Corporation was founded and they introduced the worlds first active matrix EPD display in 2001, this was later named E-Ink Vizplex [17]. Where Gyricon relied on rotating beads, the E-ink technology was based on the movement of electrically charged particles. This was considered an upgrade. Today we can see e-paper technology in many consumer products such as smart watch, e-readers, and shelf-labels.

2.2 Operating Principle

The electronic ink consist of small microcapsules bound together with a material such as silicon resin [12]. Figure 2.1 shows a schematic cross-section of the electronic ink known as the electrophoric display.

The microcapsules in the figure contain tiny charged particles suspended in a solvent. Currently, they are using dodecylbenzene dyed with anthoraquinon blue for the solvent. There are two types of particles in the solvent, positive[white] and negative[black], with opposite charge. The particles may rearrange when an electric field is applied [1, P.17]. This is what forms the image. One of the properties of EPD is its zero field stability, also known as bistability behaviour. This means that after the image is formed, even if the electric field is removed, the particles will remain at their current position. This behaviour can be traced back to the particles internal charge. The particle placement

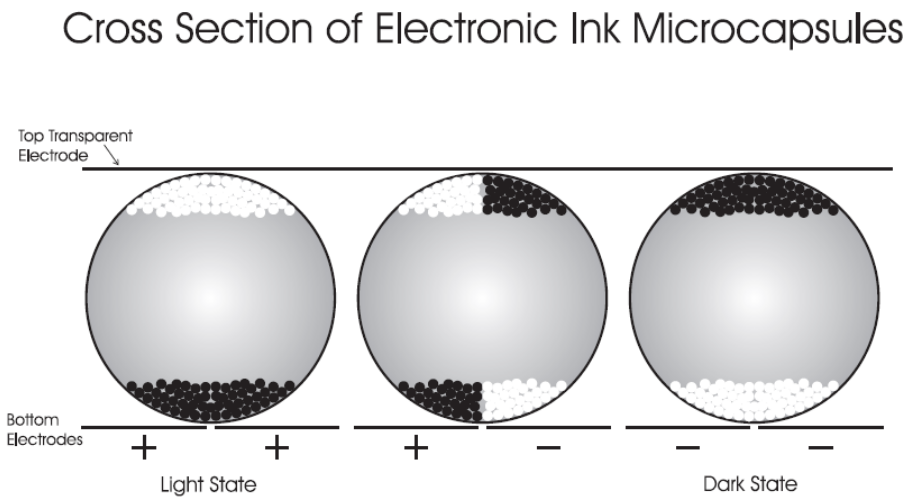


FIGURE 2.1: Principle of electronic inc [1]

is dependent on two factors, the electric field strength and the duration of the applied electric field. Because the system inside the electronic paper is complex, models are based on the chemical and physical process **??**. As a first approximation, it is assumed that charged particles follow a normal(Gaussian) model. This is in good accordance with reality [11]. Moving the particles are given by Stokes' theorem (Equation 2.1) [5] [18].

$$v(t) = qE(t)/(6\pi\eta a) \tag{2.1}$$

where q is the charge of the particle, $E(t)$ is the effective electrical field at time t , η is the viscosity of the solvent, a is the particle radius. Based on this equation the moving

distance D, is given by $D = v(t) \cdot w$. where w is the response time of the system. The distance D between two plates are usually about 100μm appart [11]. Even with voltages over 10V, it can take up to 500ms to reach a full optical contrast [2].

2.3 EPD Driving Circuitry

The EPD driving circuit can be created with five main elements, the control unit, the voltage converter, gate driver, source driver, and the electrophoric display [6]. Figure 2.2 show a schematic overview of a simple EPD driving circuit.

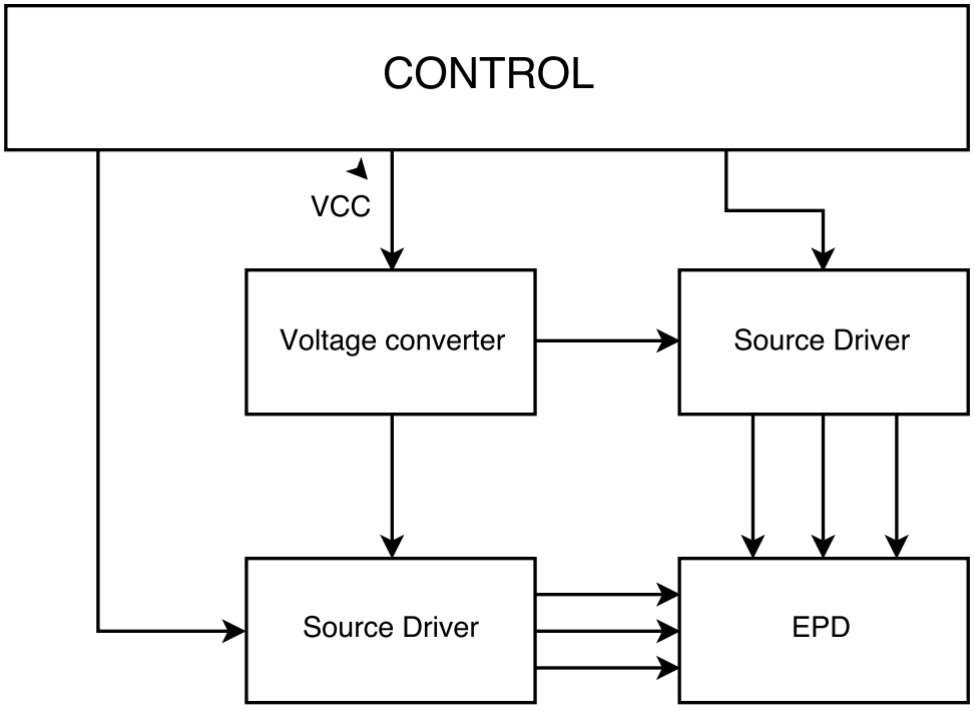


FIGURE 2.2: Simple driving circuit for the EPD

2.3.1 Control Unit

The control unit initializes the image write, it keeps track of the previous image, and ensures correct behaviour of the voltage converter, gate driver and source driver. It may include a timer to prevent race conditions between the gate driver and source driver. The EPD is largely dependent on temperature [19], so it may also include a temperature sensor.

2.3.2 Voltage Converter

If the display run on a different voltage domain then the rest of the system, the voltage converter can supply a separate voltage for those parts of the system. The voltage converter supply the gate and source driver with the driving voltage for the EPD. Voltage converters can convert up, down, and invert.

2.3.3 Source Driver

The source driver is responsible for setting all pixels in the EPD. It applies a voltage for a certain duration to every pixel, which forces the pixel reflectivity (black to white or white to black) to change.

2.3.4 Gate Driver

The gate driver works as a gatekeeper, and can "open and close" the gate. The gate is a transistor, when in an "open" state it allows the source lines to write the pixel. The use of a gate is common in many displays, and the technique is referred to as active addressing. The use of a gate driver is however not required i.e. passive addressing. E-Ink, which is the largest distributor of electronic paper displays, delivers one type of segmented display without gates. These have low resolution and require extensive wiring to passively address all the pixels. A very low resolution display of 30 x 30 pixels would need to escape 900 wires to passively address all the pixels. For this reason this thesis will present active addressing technique which requires less wiring.

2.3.5 Electrophoric Display Structure

The material of the EPD is discussed in Section 2.2. To form a display, newer electrophoric material is coated on a thin film transistor (TFT) backplane [20]. The TFT is the gate driven by the gate driver. The use of TFT allows the gate and source driver to perform addressing.

The electronic paper pixel is usually modeled by a very large resistor in the range of giga ohms [2, P.47] [21, P.3], this is visualized in Figure 2.3. A storage capacitor may optionally be added. With a storage capacitor, the display driver can quickly write a pixel by charging up the capacitor, and then move on while the pixel will be driven by the capacitor. The system inside an electronic paper pixel has a very high electrochemical complexity [11, P.1]. This paper will not try to model the electronic pixel, but simple

current characteristics are of interest. The current is given by the total number of charged particles, that is present inside the pixel, weighted with their velocity [11, P.54].

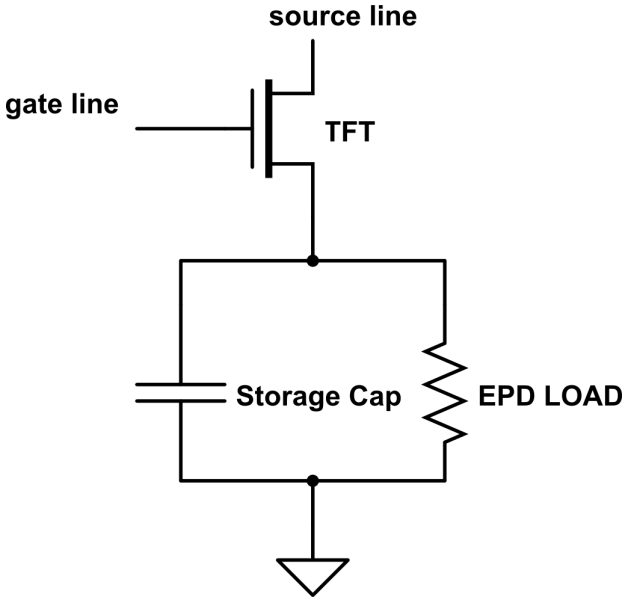


FIGURE 2.3: EPD pixel modeled with a TFT-gate and storage capacitor

2.4 Principles Of The Electrophoric Display Addressing

The electophoric display share many similarities with other displays like Liquid Crystal Display(LCD), and the Organic Light-Emitting Diode(OLED) to name a few. For an m x n sized LCD/OLED display, containing m rows times n columns of pixels, every row would be connected to a gate line, and every column is connected to a source line. A common way of driving LCD/OLED display is by utilizing an active matrix driving scheme. Although there exists other ways of driving a display, such as the passive and direct addressing schemes, the mobile marked and computer display has embraced the active matrix addressing as its standard. This is mainly due to the stability of threshold-voltage [19] and the scalability in the active matrix addressing. Figure 2.4 shows an overview of an TFT (a-Si type) display connected to the source and gate driver. This is similarly true for the electrophoric display, and the EPD driving circuit could for this reason be based on the same LCD/OLED driving circuit.

Active Matrix Addressing

In active matrix addressing each pixel has its own dedicated TFT, allowing the column lines to access the pixel. The gate drive will scan each row sequentially so that the source driver only write to the current activated row. In Figure 2.5 a LCD pixel C_{LC}

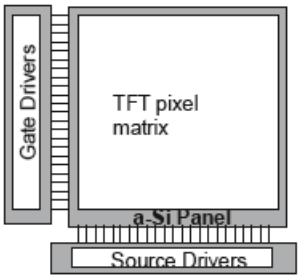


FIGURE 2.4: a-Si display connected to source and gate driver

is modeled by a capacitor and a resistor connected to an address TFT. The optional storage capacitor is also included in the figure.

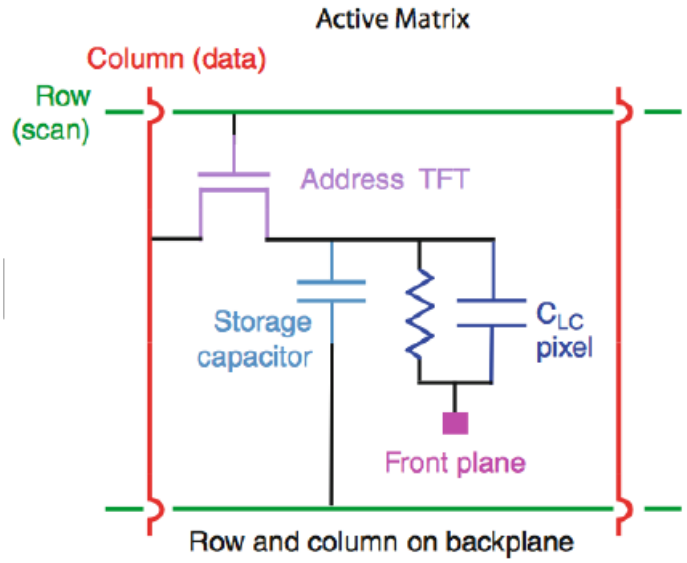


FIGURE 2.5: A pixel connected to a thin-film transistor [2]

Top to Bottom Topology

The gate driver scans each row sequentially from top to bottom, during the scan time the source lines can write the pixel. Figure 2.6, shows a gate drive activating one row while the source lines write that row. In order to ensure correct behaviour, a timer can be integrated to monitor and control to the gate and source driver. This will avoid any potential race conditions.

EPD Addressing

The active matrix addressing display driver is well suited for driving the EPD. The difference from an active matrix LCD is that the source lines now also carry negative voltage while LCD source lines only carry positive voltage. To adjust for this, the gate driver must also support resultant voltages which are negative, and the voltage on the TFT gate must follow. If a row is originally turned OFF when the source driver is positive, it might turn ON if the source lines suddenly turn negative. This will typically

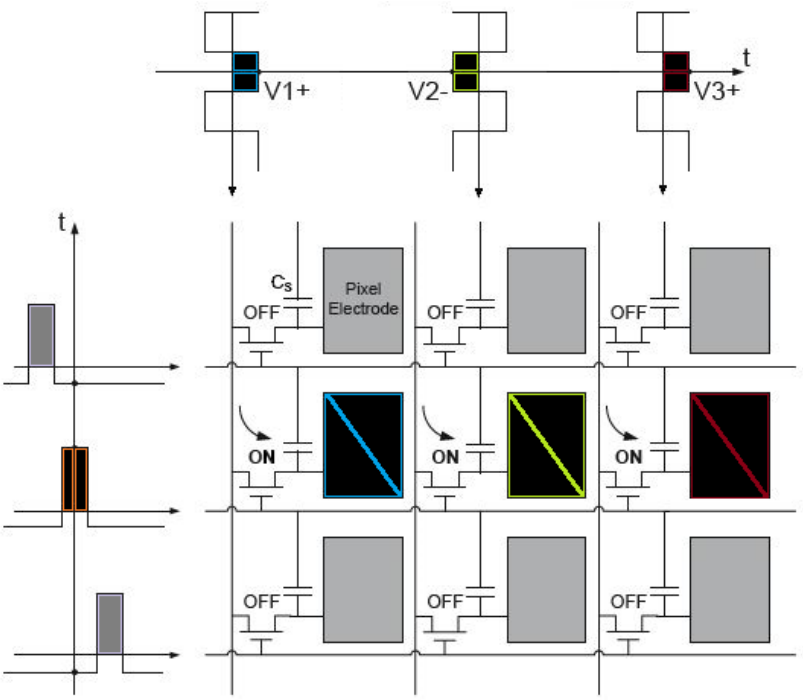
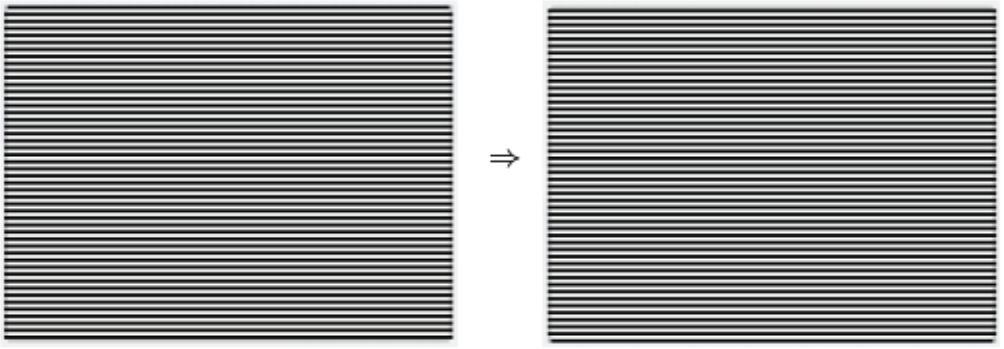


FIGURE 2.6: Sequential addressing of TFT display

happen in images with many vertical transitions. Vertical transitions is known as an image pattern with alternating black and white horizontal lines as seen in Figure 2.7.



(A) Test image 1 (B) Test image 1 inverted

FIGURE 2.7: Vertical transitions in an image [2]

2.5 EPD Driver Architectural Topology

Building a basic TFT-EPD driver involves the sub components found in Figure 2.8. It shows the same setup as the simple driving circuit for the EPD, as well as revealing the internal components in the display driver.

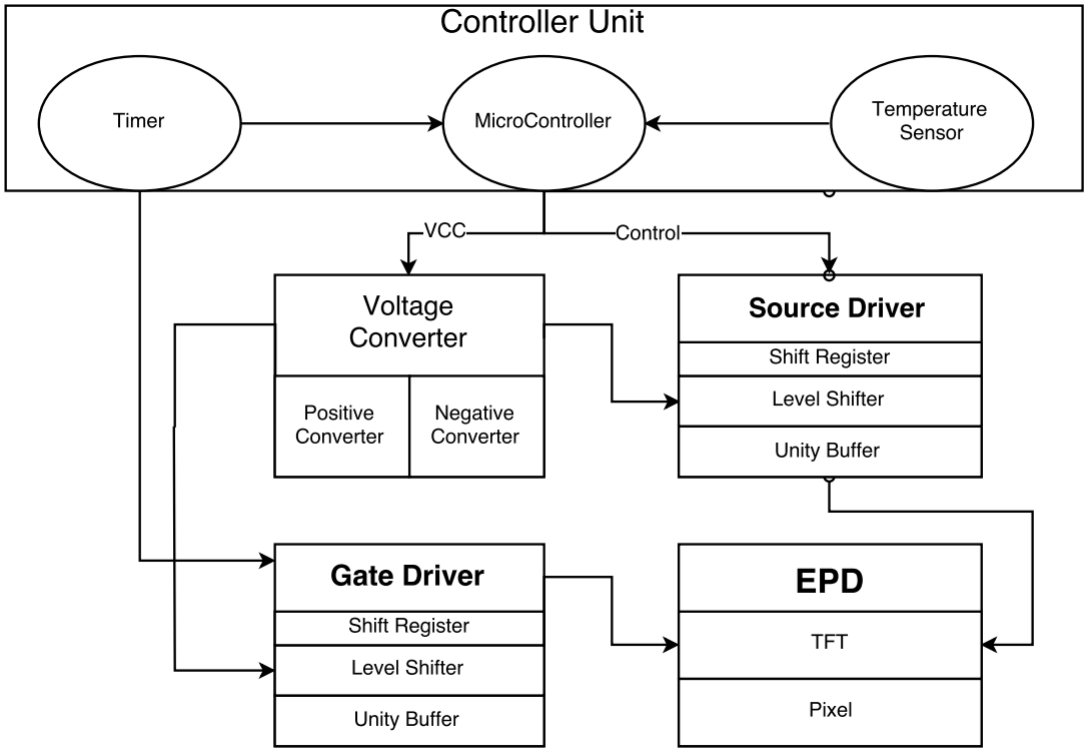


FIGURE 2.8: Internal components of the EPD driver

Voltage Converter

A lot of development has already been put into creating voltage converters, many companies such as Texas Instruments, and Linear Technology deliver complete DC/DC chip solutions. Key design qualities to look for with voltage-converters are, degree of voltage-setting accuracy, load-current delivering capability, stability of the output voltage, power consumed by the converter itself, and cost of implementation. It is encouraged to use complete chip solutions for embedded systems. There exist no EPD specific voltage converters, for this reason it is considered beyond the scope of this thesis, and is left to the designer.

Source Driver Topology

The source driver consists of a shift-register(serial to parallel) as seen in Figure 2.9, connected to a latch to hold off the output until all the bits are set. Figure 2.10 shows a block diagram of the shift register connected to a latch. The output from the latch is then sent to the level shifter. This is where the voltage rises from the low control voltage to the high voltage required by the EPD. Not to be confused with a digital convention for LOW and HIGH voltage meaning zero or one. The last function in the source driver is the unity buffer also known as digital buffer. This is an electrical component where the input is isolated from the output. It draws very low current from the input because

of the very high impedance, but can apply the output with higher current options from a different source. It is also called a unity input buffer because the gain is 1.

Gate Driver Topology

The process is similar for the gate driver, however instead of parallel output, the gate driver utilizes a shift register to scan the rows sequentially. The gate driver will use the shift register without a latch, this output is seen forming a walking 1 waveform as in Figure 2.11. The output of the shift-register is inserted into the level-shifter, again raising the voltage level, this time to the appropriate gate voltage, which may be different from source voltage. It is then asserted into the unity buffer before turning *ON* the thin-film transistor If the timing is correctly performed for the source and gate driver, an image will form on the TFT-EPD.

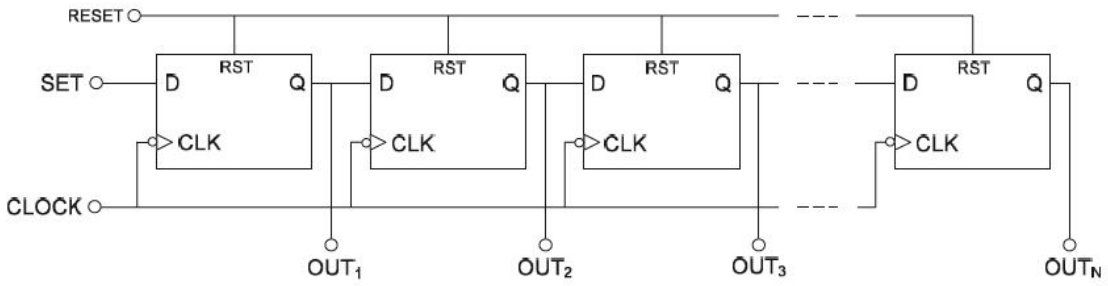


FIGURE 2.9: Shift register circuit [3, P.223]

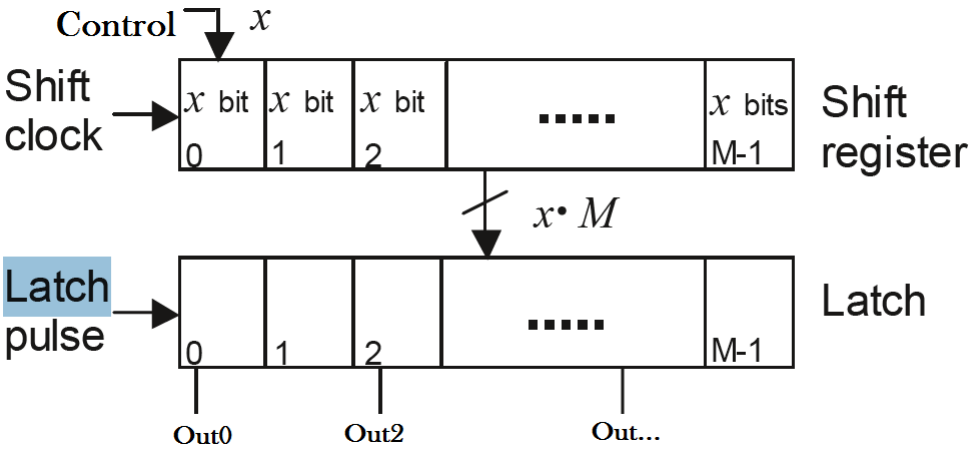


FIGURE 2.10: Block Diagram of a shift register connected to a latch [3, P.131]

2.6 The Voltage Domain

In any high voltage system where the input is not in the same voltage domain, a level shifter is required before communication can continue. If the general system is powered by VDDL and VSSL, then the source lines would be powered by VDDH and VSSH.

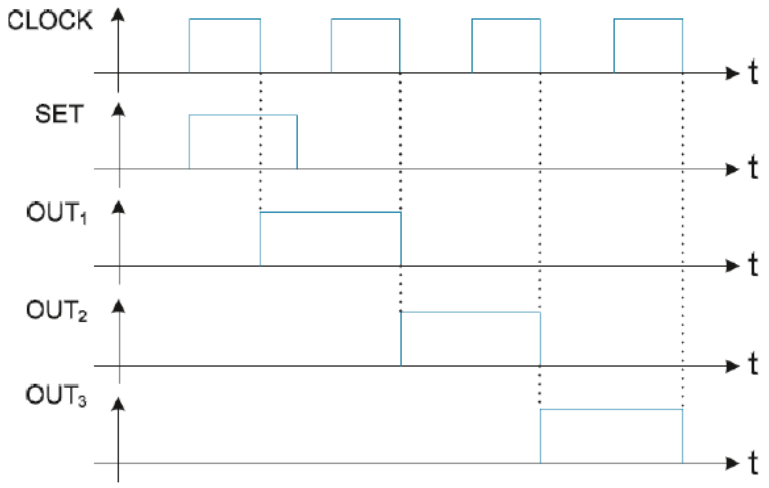


FIGURE 2.11: Shift register; walking one [3, P.223]

Figure 2.12 show how the source-driver will convert a logical pulse signal to an appropriate driving voltage level for the pixel. The pixel is usually driven by voltages between $\pm(5-15)V$, but this could vary dependent on the response time of the pixel, and the driving waveform.

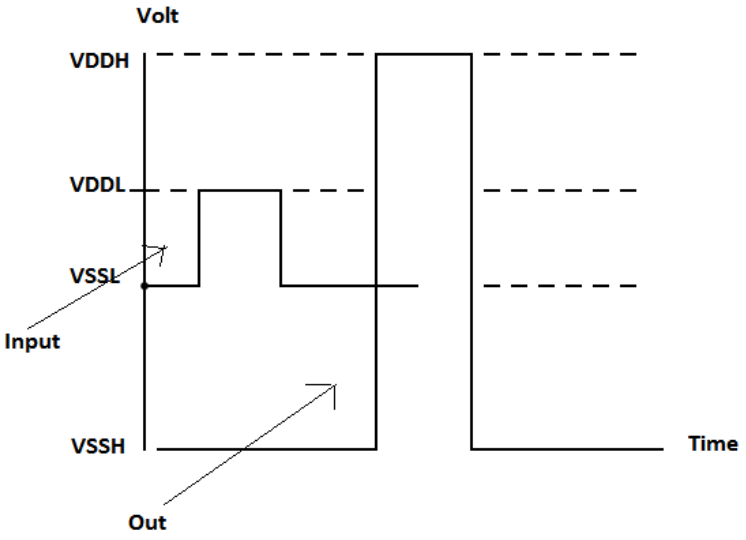


FIGURE 2.12: level-converting logical input voltage to pixel driving voltage

2.7 TFT-properties

The thin-film-transistor (TFT) was introduced as a switch for active matrix addressing. It exhibits poorer properties than the MOSFET in terms of switching speed and

conductance, but has the advantage of being transparent. The TFT is implemented on an insulating substrate, such as glass og polymer substrate, and therefore lack the body or bulk found in conventional MOSFET [3, P.146]. It has the three terminals named *Drain* (D), *Gate* (G), and *Source* (S). The gate-source voltage, v_{gs}, determines the TFT ON/OFF condition. The n-channel TFT operates similarly as the n-channel MOSFET. A cross-section of the TFT is presented in figure 2.13,

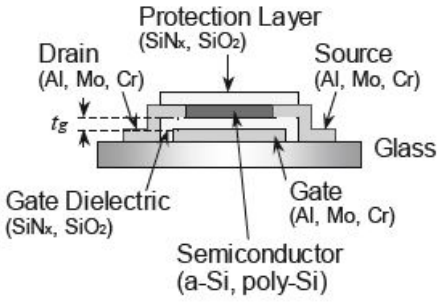


FIGURE 2.13: Cross-section of a basic tft [3, P. 147]

2.7.1 a-Si:H TFT

The most common layer used in the integration of TFT on glass is with a-Si:H **amorphous silicon**. The fabrication is easier due to low-temperature process. The main difference between a-Si:H TFT and the Si MOSFET is the electron mobility. $0.2 - 1.5cm^2/Vs$ while the crystalline Si has more then $1800cm^2/Vs$. For this reason the a-Si:H TFTs are unfit for use in analog and high-speed digital processing, however they are usefull as a switch (ON/OFF) with frequencies around 60HZ. A problem that arises because of this low mobility is the very large aspect ratio needed. This will reduce the aperture-ration, i.e. only a portion of the pixel's area will be visible through the TFT. To adjust for this problem, it is shown that the transconductance is also dependent on the gate-source overdrive, so the TFT can be driven by a high voltage, typically 20V. The a-Si:H TFT shows poor stability and can be modified by strong illumination and charge carrier injections, therefore it must be covered from light. Another issue with the a-Si:H TFT is its temperature dependence, where V_{th} is dependent on two temperature parameters. The shift is not a problem for ON/OFF operations, but becomes impairing when static noise margin decreases in digital circuits. The shift has different polarities at ON/OFF state, at zero volts, a partial cancellation occurs as in Figure 2.14.

Transistor OFF region lies in negative [5 to 7]V and ON state is found at positive [5 to 10]V. In each case, a practical design must take into account a threshold tolerance level.

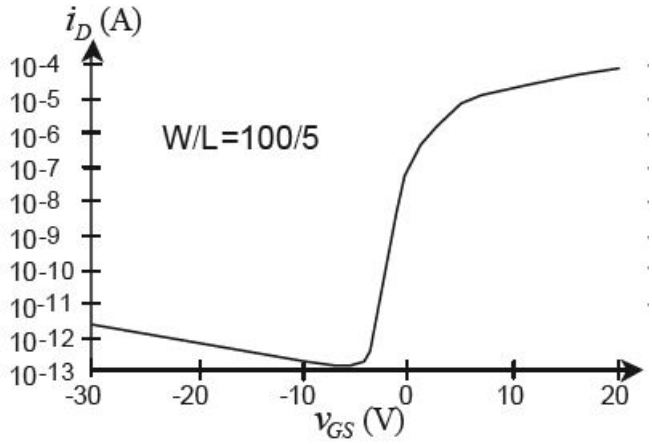


FIGURE 2.14: Drain current versus gate-source voltage for an n-channel a-Si TFT with W/L=100 μm/5 μm [3, P. 151]

2.7.2 poly-Si:H TFT

Polycrystaline Silicon is an alternative material used to realize the TFT. The advantage is the ability to make both p-type and n-type devices as well as higher carrier mobility (up to two orders of magnitude). The high carrier mobility, means smaller TFT-area (1/10 of its a:Si counterpart), which makes them suitable for CMOS-like systems, rising the idea of system on glass (SOG). The preparation of Polysilicon is more complicated then a-Si TFT, in turn adding an extra cost to the end product [3]. The additional cost is one reason why a-Si TFT is more popular the Poly-Si:H. Figure 2.15 shows the Drain current for Polysilicon versus the gate-source voltage. It can be seen that OFF leakage currents are higher the a-Si TFT.

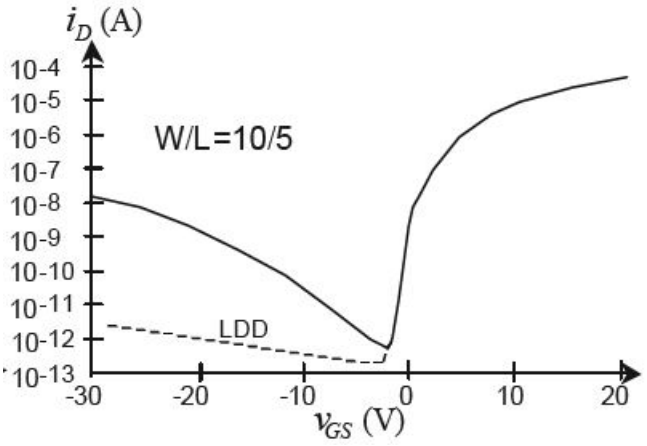


FIGURE 2.15: Drain current versus gate-source voltage for an n-channel Poly-Si TFT with W/L=10 μm/5 μm [3, P. 151]

Comparing both Poly-Si and a-Si TFT shows that displays with high pixel density is best addressed with Polysilicon. Currently E-INK together with Epson is experimenting on Polysilicon in their EPD [22], and may have used this with their product. This detail

is not available throught E-Ink's own datasheet, however the datasheet of E-Ink Carta is indicating that this is optional [23].

Chapter 3

Previous Work

There has been several contributions in recent years to improve the EPD, in terms of efficiency [24], quality, speed [19], and removal of unwanted effects such as the ghosting effect [25]. Modifications in updating sequence, software modifications and hardware are all possible techniques to save energy. Although all the properties listed above will be reflected in the total power consumption, this thesis focus on the hardware based approach to gain a power efficient electronic paper.

This chapter covers previous work in six major topics which will be described in the following order.

- **Power Consumption Investigation** Breaking down the parts of the EPD which use power is considered important if the solution should become low power.
- **Low Power Electrophoric Display Module** The unipolar driving waveform is presented and the source driver is broken into two categories that will help the low power discussion in later chapters.
- **Configurable timing controller for AM EPD** describes a more detailed view of the unipolar driving waveform.
- **Low Power Electrophoric Display** gives an overview of the possible power savings using unipolar driving waveform.
- **Power Reduction in D-RAM Technology** shows how leakage currents can be handled to acheive better performance in transistor technology.
- **Capacitor Coupled Level Shifter** describe a new level shifter with very low power consumption. Note: Article description is inconsistent with results, the section is described as the article presents it.

3.1 Power consumption investigation

In 2002, Pitt [4] published a detailed investigation of power in the electrophoric display, together with Philips Mobile Display Systems and E-Ink Corporation. Under a constantly switching worst case situation of the updating sequence, and using ±15V to update the image, it was found that the largest part of the power consumption comes from driving the source lines. A breakdown chart of the power consumption is shown in Figure 3.1.

To understand the power consumption, consider driving the column signals (source lines) for electronic ink. Energy is **only** consumed by the capacitive components when the source voltage changes. With the additional high voltage used for driving the display, the power usage is considered highest in the level shifter and buffer, both of which are regulating high voltage.

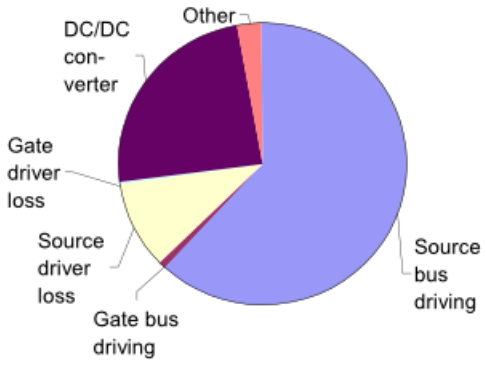


FIGURE 3.1: Breakdown chart for power usage [4]

To determine typical power consumption during continuous operation, a sample of different text images was analysed. Figure 3.2 shows the results. In normal text mode, approximately 10% of the pixels are black, this proportion increases somewhat for larger fonts, up to 20%. There is interestingly not an increase in power because of this, because it is dependent on the number of vertical transitions.

In cases of graphic data, the power consumption will be dependent on the type of image displayed. Images having a large portion of horizontal lines or dotted lines will have a much larger power level then images with same color tone. To simulate this, an image consisting of random placement of black and white pixels was created. The power as a function of black pixel density is shown in Figure 3.3. The simulation assumes that the number of black pixels are the same for the old and new image. The highest power level

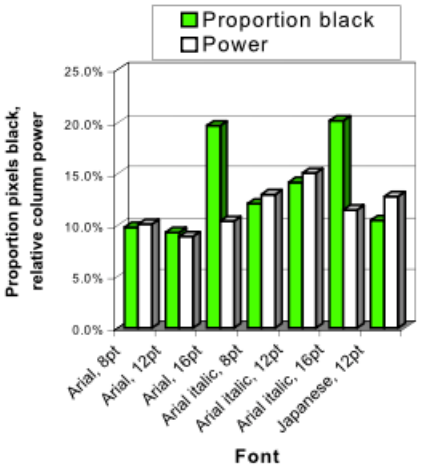


FIGURE 3.2: Power as function of font type [4]

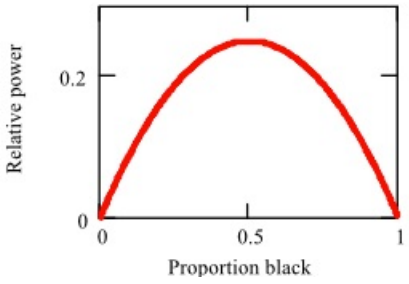


FIGURE 3.3: Power as function of black pixels for image transition [4]

is found when the portion of black pixels are at 50%, in this case the power consumption is at 25% of the maximum value of the power level.

3.2 Low Power Electrophoretic Display Module

A Low Power Electrophoretic Display Module was developed by S. Gunnerød, as a master thesis in 2016 [2]. Based on an analysis of the sub modules in the electrophoric display driving circuit, Gunnerød presented a method for power reduction. Given a pixel such as in Figure 3.4, the common electrode in the EPD is traditionally fixed at 0V, while the pixel electrodes are switched between +15V and -15V called bipolar driving waveform.

If the common electrode instead is set at the opposite polarity as the pixel electrode then the total voltage span will be 30V. This is called a unipolar driving waveform.

For e-reader applications and large size EPDs, the biggest gain in using a unipolar waveform is to reduce image updating time, ghosting effect and flicker. An explanation

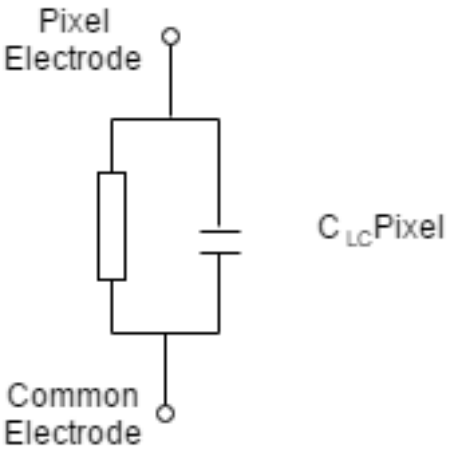


FIGURE 3.4: Modeling a Pixel

of ghosting effect and flickering is available in appendix A. Because the focus for small EPD and low power consumption is of priority, a second compelling aspect can be exploited. The voltage can potentially be reduced to half of what is used in bipolar driving waveform. In cases where the display is only updated on occasional basis, a 5V over the pixel electrode can be used, and the driving voltage can be reduced to ±2.5V. Because the voltage has a quadratic relationship to power then this will have a substantial effect over the power consumption.

3.2.1 Source Driver Power - Digital Part

The digital part of the source driver consists of latches and shift registers. The architecture of a shift register is area consuming, and increases for larger displays. The typical data flip-flop is twice the size of a latch because of the additional clock signal. Since N flip-flops are required for a display with n columns, there will typically be N flip-flops and 2N latches in a traditional source driver. The power dissipation is proportional to the clock scan frequency and its total capacitance. The power dissipation can be reduced by sampling bits on both edges of the clock [3][P. 225]. The total power consumption can thereby be reduced by a factor of two. For a typical LCD source driver, the digital part's power dissipation is close to 10% of the total [3][P. 218]. An EPD source driver is expected to have similar properties.

3.2.2 Source Driver Power - Analog Part

This is the part of the source driver related to high voltage, and accounts for the remaining 90% of the total power dissipation [3][P. 218]. There are two main reasons for power dissipation in the analog part, static power related to leakage, and dynamic power.

Static power dissipation occurs all the time, as transistors are always leaking current through Gate, Drain and Source, and also by short circuiting. When transistors are changing state, a short circuiting may occur because both transistors are partly active. However dynamic power dissipation is considered most significant. Dynamic current draw occurs when the parasitic capacitance in the transistors is charged up and down due to state changes.

3.3 Configurable timing controller for AM EPD

A configurable timing controller provides an easy way to modify waveforms under different design requirements [5]. To facilitate design changes, an EPD timing controller should be configurable. The article describes important design considerations: (a) The activation sequence of charged particles. (b) The movement of charged particles for displaying desired gray level, and (c) the bistable properties and the image erase sequence. The driving waveform is difficult to correctly produce, since timing is set by driving the pixel to a state and measuring the reflectance.

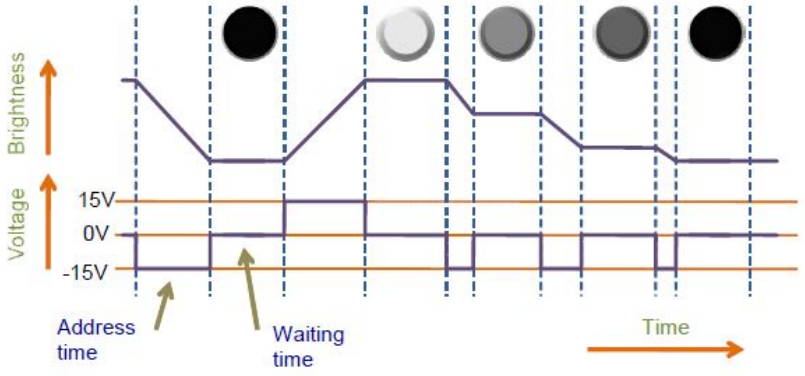


FIGURE 3.5: Bipolar driving scheme [5]

There exist no good models for accurately predicting the movement of particles. Figure 3.5 show a waveform called bipolar driving in this paper. The common electrode is set at 0V and the pixel electrode is set at ±15V. The voltage difference is 15V and the gray level is controlled by giving different voltage pulses.

An alternative approach is called unipolar driving waveform, this utilizes the common electrode to hold the opposite polarity as the pixel electrode. Because the voltage difference becomes 30V, this will speed up the particle state transition as seen in Figure 3.6.

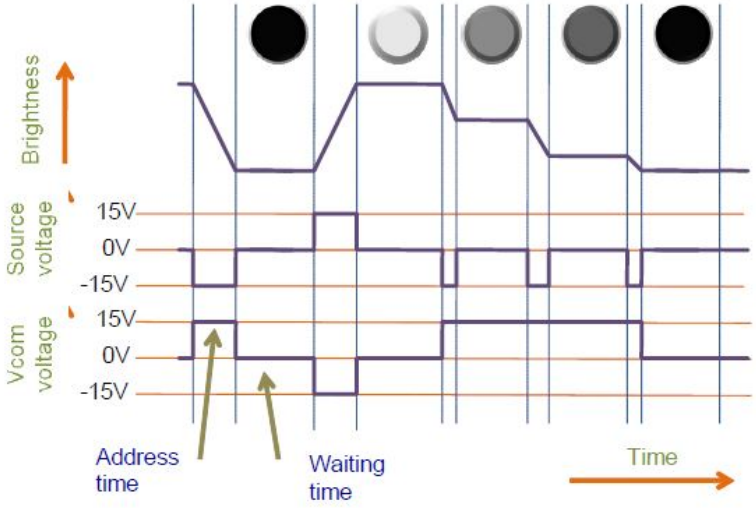
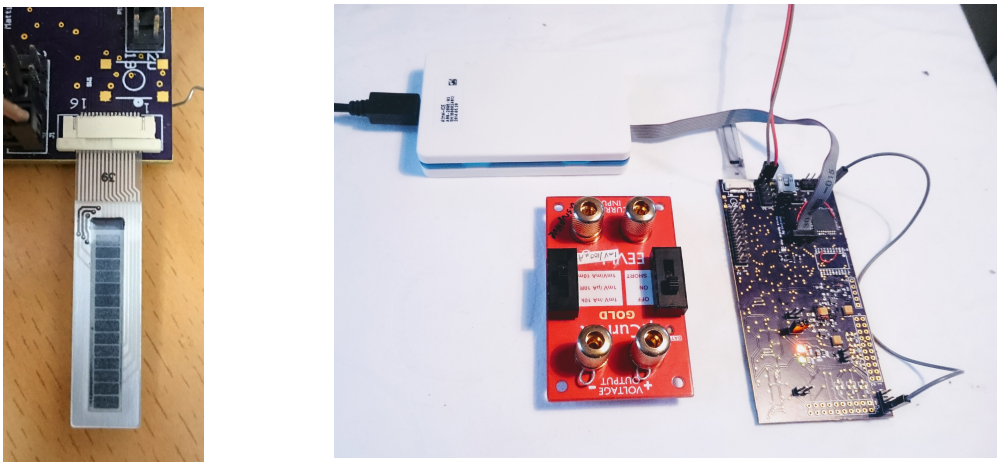


FIGURE 3.6: Unipolar driving scheme [5]

3.4 Low power Electrophoric Display - Specialization project



(A) Segmented display showing black segments [6]

(B) Circuit board (purple), programmer (white), and μcurrent tool (red) [6]

FIGURE 3.7: Specialization Project

A specialization project was carried out in the fall of 2016 by Mattis Spieler Asp [6]. The main purpose was to evaluate and give a working example of unipolar driving in a real EPD. A segmented display bought from E-INK seen in Figure 3.7(A) was used together with a self designed unipolar display driver seen in Figure 3.7(B) as the purple PCB. The display was running on 5V, and using unipolar drivers of $\pm$2.5V. Calculations based on the results show that for a regular 7" display, given the worst case update scenario, power can be reduced by almost 75% using this technique. Measurements also show that a segmented display consumes about 0.6μW /cm^2 in a state change (black to white/white to black). Figure 3.8 shows the impulse response of the current going into

the EPD when alternating the unipolar voltage, this is the same as switching between black and white color. The current swing can reach up to 420nA per segmented display. Which is 30nA per segment.

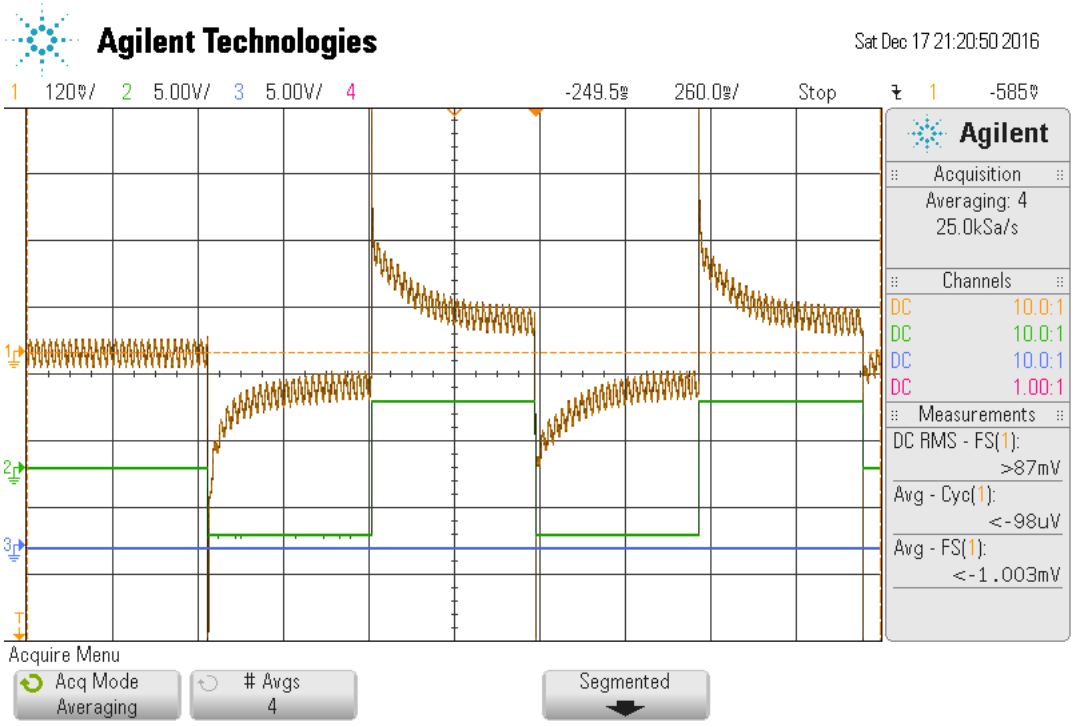


FIGURE 3.8: Oscilloscope measurements at the Electrophoric Display, showing an avg current draw of 86.9nA [6]

3.5 Power Reduction in D-RAM Technology

Level shifters have been used in the past together with D-RAM to adjust resultant voltage levels, ensure stable operation, and retention characteristics [7]. The voltage level shifter is a required part of D-RAM and flash memories. For this reason many power reduction schemes has been developed for D-RAM level shifters.

To realize low-voltage RAMs, subthreshold leakage of both RAM cells and peripheral circuits must be reduced. Through various reverse bias schemes one can achieve higher threshold value for the transistor, thus minimizing leakage current. [7, P.151].

3.5.1 Reverse Bias Leakage Reduction

The leakage current of MOSFET (i.e subthreshold current) can be expressed by [7, P.152]

$$i \propto e^{\pm\frac{V_{GS}-V_t-K(\sqrt{\pm V_{BS}+2\Psi}-\sqrt{2\Psi})+\lambda V_{DS}}{S/ln10}} \cdot (1-e^{\pm\frac{qV_{DS}}{kT}}) \tag{3.1}$$

where the upper sign refers to the NMOS and lower sign refers to the PMOS transistor. V_t is the actual threshold value, S is the subthreshold swing, K is the body effect coefficient, q is the electronic charge, k is the Boltzmann constant and T is the absolute temperature. Leakage is usually decreased with a factor of 10 with a V_t increment of 0.1 volt for a bulk MOSFET with $S \cong 100\text{mV/decade}$ at 100°C. The best way to reduce leakage current is to increase V_t. There are categorically two ways of getting high V_t from a low V_t. The first is enhancing the *actual* V_t by increasing the doping level of the substrate, the second to raise the *effective* V_t by applying reverse-biasing schemes. The basic concepts for reverse-biasing can be viewed in Table 3.9.

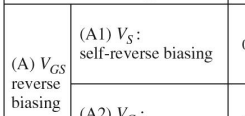
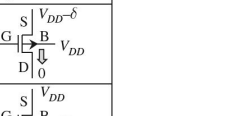
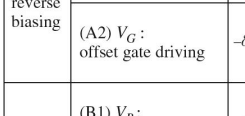
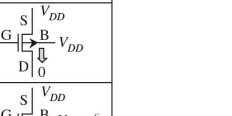
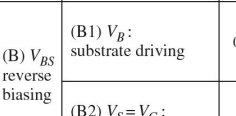
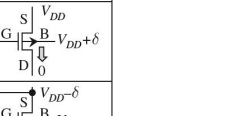
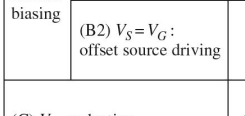
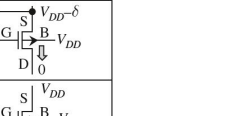
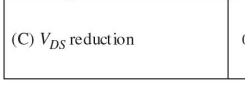
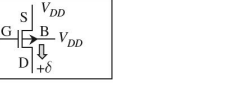
Modified voltage(s)		nMOST	pMOST
(A) V_{GS} reverse biasing	(A1) V_S: self-reverse biasing		
	(A2) V_G: offset gate driving		
(B) V_{BS} reverse biasing	(B1) V_B: substrate driving		
	(B2) $V_S = V_G$: offset source driving		
(C) V_{DS} reduction			

TABLE. 3.9: Concepts for creating high V_t [7, P.153]

The table represents (A) V_{GS} reverse-biasing, (B) V_{BS} substrate-driving, and (C) V_{DS} reduction.

They can be split into basically two categories; static or dynamic with relation to threshold values of the transistor. The selective use of high V_t MOSFET in a low V_t circuit decreases the leakage current of the circuit. The static high V_t, also known as dual-V_t, is used to combine high and low V_t together in circuits. The CMOS dual-V_t in which the low V_t is only used for the critical path will effectively lower the leakage-current, while simultaneously achieving the high speed requirements. It should be noted that extensive reverse biasing may lead to race-conditions in the circuit.

3.5.2 Refresh operation

After a cell is written in D-RAM the high voltage decays over time, charge losses are due to leakage currents, α-particles or cosmic-ray neutron irradiation. At some time before the voltage falls below the high-voltage read-limit, voltage must be restored by a refresh operation. This is done by reading the word on the cell and reinstating the same voltage.

3.6 Conventional Level Shifter

The conventional level shifter is regularly used for generating waveforms such as the one suggested in Figure 2.12 [3]. A conventional level shifter can be seen in Figure 3.10. The circuit consists of a CMOS inverter, M1 - M2, supplied from VSSL and VDDL and two latches. The latch, M3 - M6, supplies the negative supply, and M7-M10 supplies the positive latch.

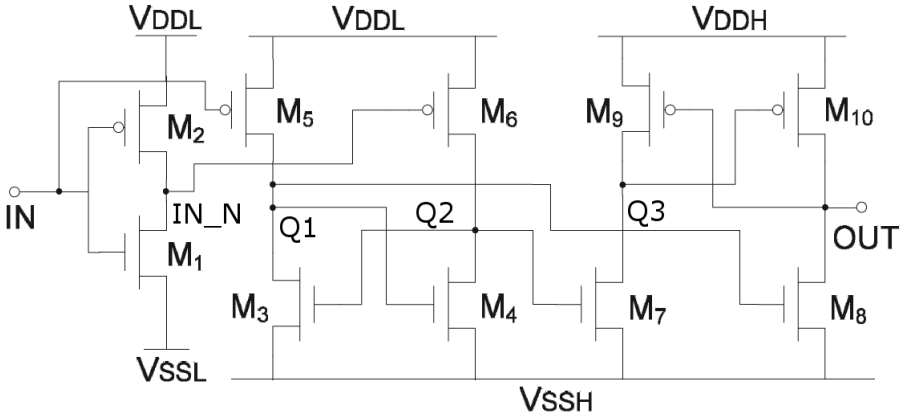


FIGURE 3.10: Conventional level shifter [3]

The conventional level shifter is considered fast, and uses little area [3] [26]. An undesired limitation with this circuit occurs when the circuit is switching, the **cross-conduction** current (flowing from positive supply rail to negative) occurs because the transistors change their logical state and are momentarily *ON* due to a delay in their signal [3]. Although it occurs at a brief moment, the actual current may be significant because only the **ON resistance** of the transistor is limiting the magnitude. The biggest disadvantage with the conventional level shifter is related to the feedback loop. Every transition in IN will require that stored energy in the circuit is fully committed to ground [6]. This is a result of a former charge buildup in the internal capacitance of the transistor.

3.7 Capacitor Coupled Level Shifter

The capacitor coupled level shifter (CCLS)[8] can produce a positive drive output. It was introduced to limit the number of transistors sourcing ground on transitions between VDDH and VSSH in the feedback loop. The CCLS is composed of two coupling capacitors, three diode-connected transistors, two switches and a load. Transistor N4 pulls down to the voltage of INPUT, whereas P1 pulls the voltage of the node OUT up to the voltage of node Q1. N4 has low voltag logic inputs, whereas P1 has high voltage nodes connected. The design in Figure 3.11 is motivated by an offset voltage formed by

two capacitors C1, C2, and the identical diode-connected transistors N1, N2 and N3.

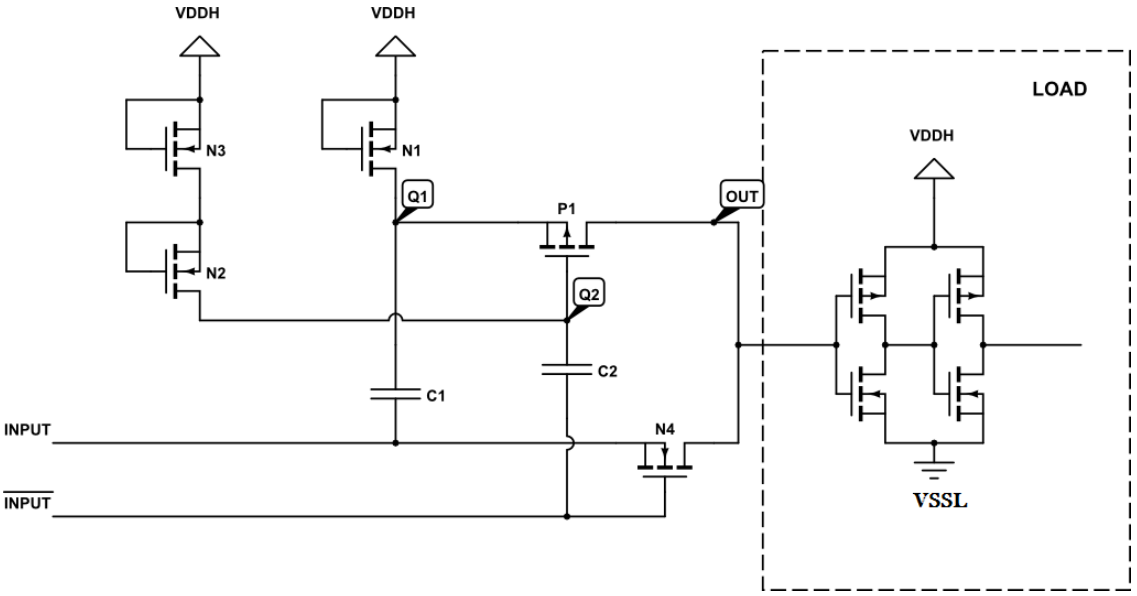


FIGURE 3.11: Capacitor Coupled Level Shifter [8]

3.7.1 Transient Response

Assuming INPUT toggle as in Figure 3.12.

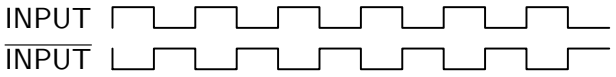


FIGURE 3.12: INPUT and $\overline{\text{INPUT}}$ toggle.

Initially when INPUT is LOW(VSSL) and hence $\overline{\text{INPUT}}$ is HIGH(VDDL), C1 is charged to the voltage VDDH-V_{th} by the diode connected transistor (N1) where V_{th} is the threshold voltage of the N-channel transistor. When INPUT is HIGH(VDDL), C2 charged to the voltage of VDDH-2V_{th} by the diode connected transistor (N2 and N3). A falling *LOW* INPUT and hence OUT rise to (VDDL), would pull the voltage on Q2 down because a capacitor voltage cannot change instantly. When INPUT rise, it would drive the voltage on Q1 with it. The following properties exist after each transition.

- When INPUT = $VDDL$
  - Q1 = $VDDH - V_{th}$+$VDDL$
  - Q2 = $VDDH - 2{\cdot}V_{th}$

- ◇ OUT = $VDDH - V_{th} + INPUT$

- When INPUT = $VSSL$
  - ◇ Q1 = $VDDH - V_{th}$
  - ◇ Q2 = $VDDH - 2{\cdot}V_{th}{+}VDDL$
  - ◇ OUT = $VSSL$

Power Consumption

The simulated results showed that the power consumption of the proposed and the conventional level shifters were 29μW and 86μW, respectively. The power consumption of the proposed level shifter could be reduced by about 66% compared to that of the conventional one for an 3.3V input and 10V output operating at 25KHz frequency.

3.8 Positive and Negative Level shifter

The output waveform in Figure 2.12 shows that both VDDH and VSSH are positioned *higher* and *lower* then the input VDDL and VSSL, respectively.

A possible architecture for achieving both the positive and negative output levels is presented in Figure 3.13 [3]. The schematic combined the two level shifters with the half-bridge stage M1-M2, which drives the output lines with proper current capability. The transfer gate-section M3-M6 has the function of precharging (discharging) the output lines to the intermediate voltage level VSSL when rising (falling) output transitions, this has the purpose of saving power consumption.

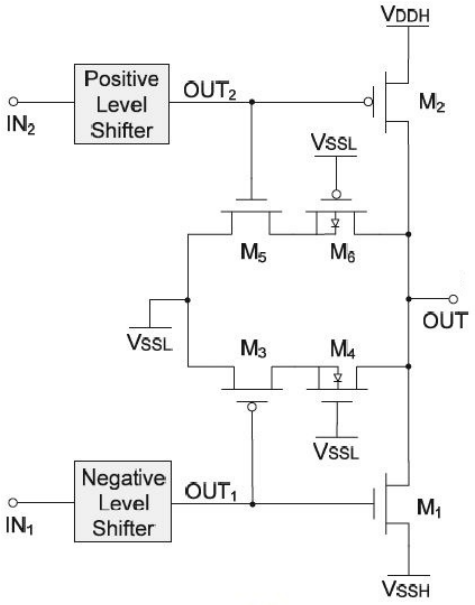


FIGURE 3.13: A digital buffer, which combines two level-shifters of opposite polarity [3]

Chapter 4

New Architectural Level Shifter

This chapter presents the largest contributions by the author. Three architectural designs are created by the author in the effort of supplying a unipolar driving waveform. The power characterization is included and based on performed simulation and information from previous papers where applicable.

The architectural design is focused on the level shifter, which is a major contributor to achieve unipolar output voltage.

4.1 Proposed Negative Capacitor Coupled Level Shifter

Since the capacitor coupled level shifter presented in Chapter 3.7 does not support negative level output values, the author propose the solution presented in Figure 4.1. The new circuit is based on the same principles as the CCLS. To verify the circuit the design is described in two parts, first the steady state will be described, followed by a desciption of transient state.

4.1.1 Steady State

INPUT = VSSL
When INPUT is *LOW* (VSSL) then $\overline{\text{INPUT}}$ will be *HIGH* (VDDL). Leakage current through transistor P1 and N4 will drive the node Q1, Q2 and Q3 *low*. When Q1 is higher than VSSH+V_{th} the transistor N1 will turn ON and Q1 charges down to VSSH+V_{th}. Transistors N2 and N3 work on the same principle as N1, Q2 will reach the voltage VSSH+V_{th} and Q3 will not be higher then V_{th}. Since Q3 already is VSSL which

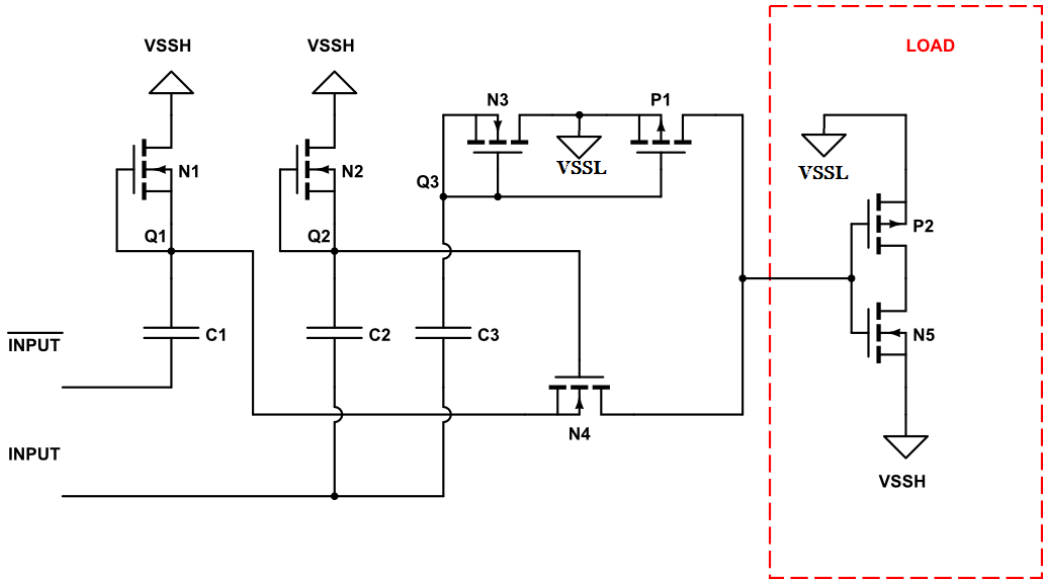


FIGURE 4.1: The Author proposes this level shifter to achieve negative levels in the capacitor coupled level shifter.

is lower then V_{th}, it will be stable at that voltage. The voltage drop of $V_{GS}(P1)$ is $Q2 - Q1 = V_{th}$. The two transistors P1 and N4 display the following properties:

- Transistor P1
  - $V_{GS} \geq V_{th}$
  - P1 stay OFF
- Transistor N4
  - $V_{GS} \leq V_{th}$
  - N4 stay OFF

Because both transistors are OFF the OUTPUT will be floating. To solve this a pull-up resistor could be added to achieve a desired stable state.

4.1.2 Transient State

This circuit will charge the capacitor C1, C2 and C3 with the diode-connected transistors N1, N2, and N3 respectively. INPUT is directly connected to capacitor C2 and C3, while C1 is connected to $\overline{\text{INPUT}}$. IF INPUT starts at *low*, the nodes Q1 and Q2 will be charged to $VSSH + V_{th}$. Q3 is unaffected by INPUT until INPUT *rises*, then the diode-connected transistor N3 will partake to re-stabilize Q3 at $+V_{th}$. During the rise event, Q1 will fall down to $VSSH + V_{th} - VDDL$, and the voltage is trapped in

node Q1 because N1 will block current in that direction. Simultaneously Q2 will rise to $VSSH + V_{th} + VDDL$, N2 will quickly counteract the sudden rise and re-stabilize Q2 back to $VSSH + V_{th}$. The voltage difference on N4's gate-source is $VDDL$ and OUTPUT will become Q1.

Controlling P1

When the INPUT **falls** once again this will force Q3 down to $-VDDL+V_{th}$ because the transistor C3 cannot change instantly. The diode connected transistor N3 will block current from ground into the node Q3, and thus Q3 will be pumped down to -$\|VDDL\|$+V_{th}. Q3 is applied to the gate of P1, and will control ON/OFF states. When INPUT is **high** (**low**) P1 will turn OFF (ON).

Controlling N4

Q1 and Q2 behave similarly, but because C1 is attached to $\overline{\text{INPUT}}$ and C2 is attached to INPUT, they will always have opposite states during a period. Q2 is applied to the gate of N4 and will control ON/OFF states. Q1 is applied to the source of N4 and will be connected to the load when INPUT is **high**. When INPUT is **high** (**low**) N4 will turn ON (OFF).

Requirements

There are some requirements for this circuit to function correctly.
(1) INPUT or VDDL must be equal to or higher than $2V_{th}$, this can be seen from node Q3 where P1 will not turn completely ON if the threshold voltage is unreached.
(2) The capacitances of C1, C2, and C3 are responsible for holding the potential on Q1, Q2 and Q3. Eventually the nodes will fall back to steady state because leakage current is always discharging the capacitor. The size of the capacitors will be responsible for the duration a single state can exist.

4.1.3 Power Characterization

The actual power characterization depends upon the process-technology used, switching frequency, speed of the transition, and size of capacitors. Because the newly proposed circuit is based largely on the CCLS described in Chapter 3.7 it should exhibit power characterization similar to that circuit. Firstly three capacitors C1, C2, and C3 charge up, therefore an initial large charge current should be expected. Leakage will be expected in all nodes connected to a transistor. A large current will be drawn when INPUT is transitioning and diode connected capacitors charge up.

A full power consumption disclosure will be presented in Chapter 6.

4.2 Optimizing for CMOS technology

Looking at Figure 3.11 (CCLS) and Figure 4.1 (Negative CCLS) it is important to know that they are designed for Poly-Si TFT-transistors, described in Chapter 2.7, largely popular because of integration on panel. However the transistors used for the source driver could arguably be any other technology if integrated on a chip. With regards to other technologies, it is possible to *omit* the **Q1 node** including **C1**, and the **inverted** signal.

One solution seen in Figure 4.2 would move N1 to be connected in series with N2. The resulting circuit would double the gate-source voltage upon N4, and thereby guarantee a voltage buffer to securely control N4. This subsequently solves two problems. (1) less components occupy less area, (2) when input stays long in one logic state, the voltage over C1 would drop due to leakage, eventually leading to circuit error. This is solved by attaching VSSH directly to the source of N4.

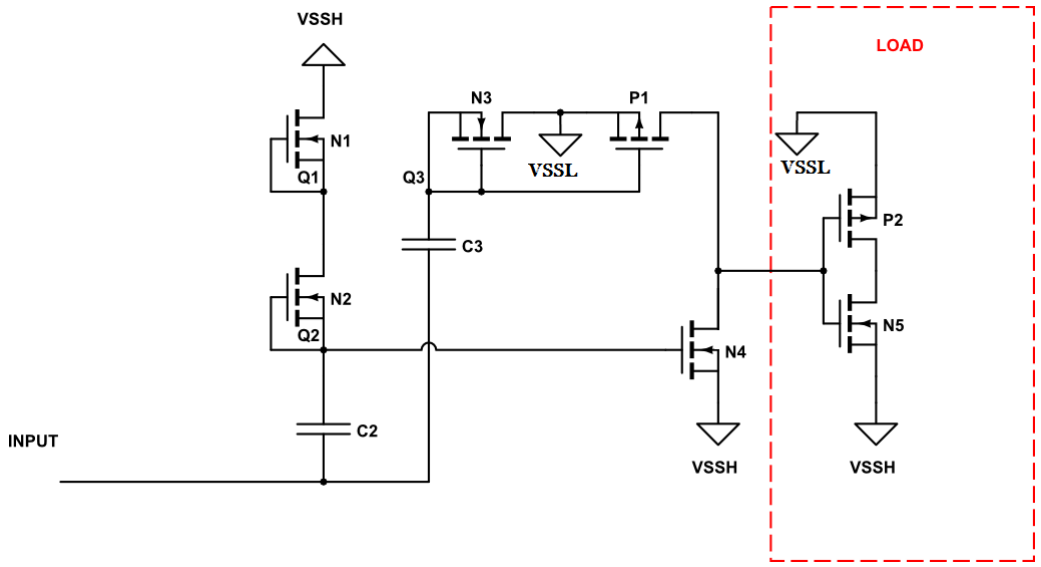


FIGURE 4.2: Optimized negative level-shifter with two capacitors instead of three, and no $\overline{\text{INPUT}}$.

4.3 Refresh Operation

The CCLS, NCCLS and the optimized NCCLS can not stay in a certain state forever, as the voltage on each capacitor eventually will fall back to their steady state. The length of their lifetime is proportional to capacitor capacitance and leakage current, after which the voltage must be reinstated.

Capacitance requirements

The power characterization and leakage is dependent on the process-technology. Figure 4.3 presents an optimized capacitor coupled level shifter (P1 source directly connected to VDDH). From node Q2 current can travel in three directions when Q2 is VDDH-2 $\cdot V_{th}$+VDDL.

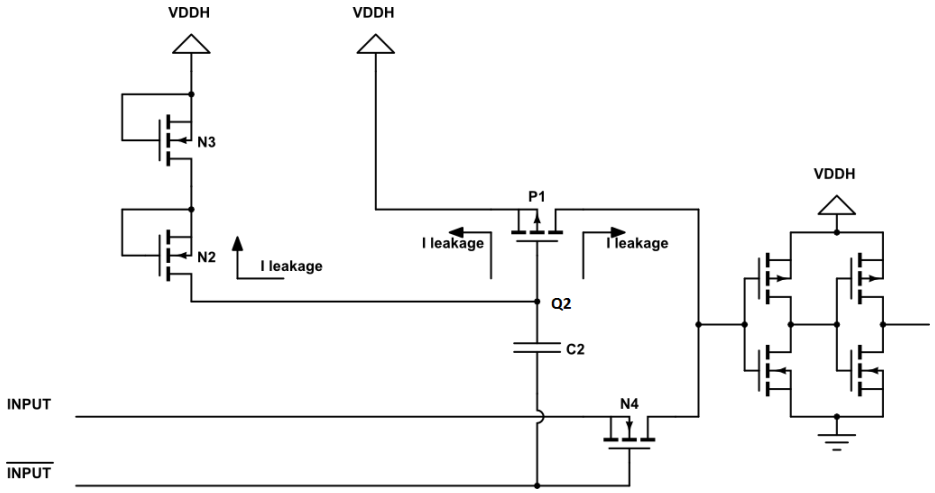


FIGURE 4.3: The possible leakage currents from node Q2 in CCLS

Adding a high capacitor would solve this timing issue, but design considerations will constrict that solution in many integrated circuits. This issue is however not limited to this particular circuit and has already been discussed in Chapter 3.5.2 as DRAM refresh operation. It is possible to implement a timer both in software and in hardware, which will reinstate the voltage of Q2.

To reinstate the voltage, output must be turned *low*, but the short time required to do this operation will not affect the pixel in any particular way. The actual time required to recharge should be less than 1ns if the time-constant is a few pico seconds. This was calculated using 20pF capacitor and modeling the transistor N2, and N3 as 0.1 Ω resistor. Equation 4.1 [27] [page 246] was used to evaluate the charge up time from 5V to 10V.

$$v_c = I_s R + (V_0 - I_s R)e^{-t/RC} \tag{4.1}$$

Similar considerations must be taken when adding capacitors for the negative capacitor coupled level shifter. Calculating the correct capacitor and refresh rate should be possible with the discussion above.

4.4 Use of reverse biasing

The reverse biasing scheme has been described in Chapter 3.5.1, and can be implemented to achieve less leakage. Figure 4.4 describes such a solution implemented on the circuit to limit the leakage current from high potential rail to low potential rail. Gate current was reportedly decreased when a large positive voltage was applied to the substrate [28].

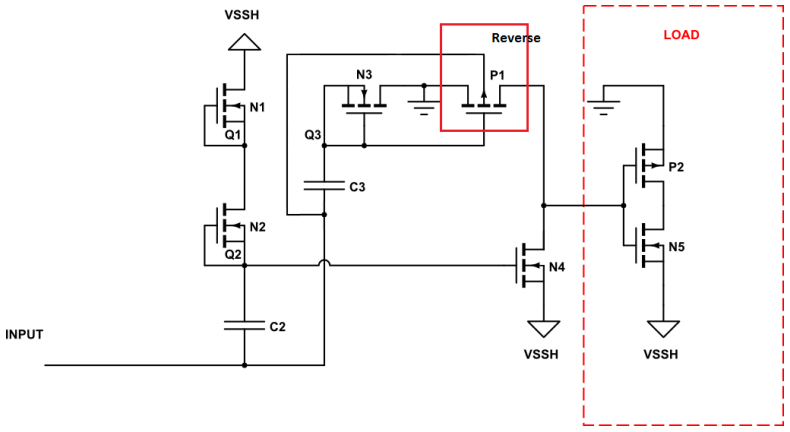


FIGURE 4.4: Reverse Bias P1 to limit leakage from source to drain

Chapter 5

Gate-driver

This chapter includes the second large contribution by the author. It was stated in Section 2.7 that the thin film transistor only produce a partial cancellation when the gate-source voltage is 0V. This chapter will consider how this will affect the gate-driver and what the counteractions can be. This chapter will first consider the voltage that the gate of the TFT must be driven to. A research into the current consumption when driving the display at different voltages is then presented. Lastly two new circuits capable of producing the correct gate-voltages are presented.

5.1 TFT threshold voltage

The desired TFT gate voltage, depends on how much current it should deliver to the pixel. From Section 3.4, the segmented display had a current swing or I_{MAX} of 30nA through one segment, this was under a 5V applied voltage. From the graph in Figure 2.14 a current of $3 * 10^{-7}$ should be sufficient to drive the display. Reading from the graph (of a-SI-TFT), a TFT's V_{GS} of approximately 0V or higher should be sufficient to deliver enough current for the pixel. Chapter 2.4 explained how the pixel current is proportional to the amount of particles weighted with the speed of the particles. Since the electric field is proportional with the speed of the particle, the current should increase with a higher voltage.

5.2 A Research Into I-V Characteristics of Electrophoric Paper

It was shown in Section 5.1 that current through the pixel is proportional to voltage applied. Because Section 3.4 only considered one instance where the voltage is 5V, a better current measurement should be investigated which shows the maximum current for an increasing voltage. To find the desired TFT gate voltage, the maximum current during a pixel write should be found. Figure 5.1 provides the current response to a single pixel write. The actual current is highly irregular starting with a short rise after which it is quickly falling.

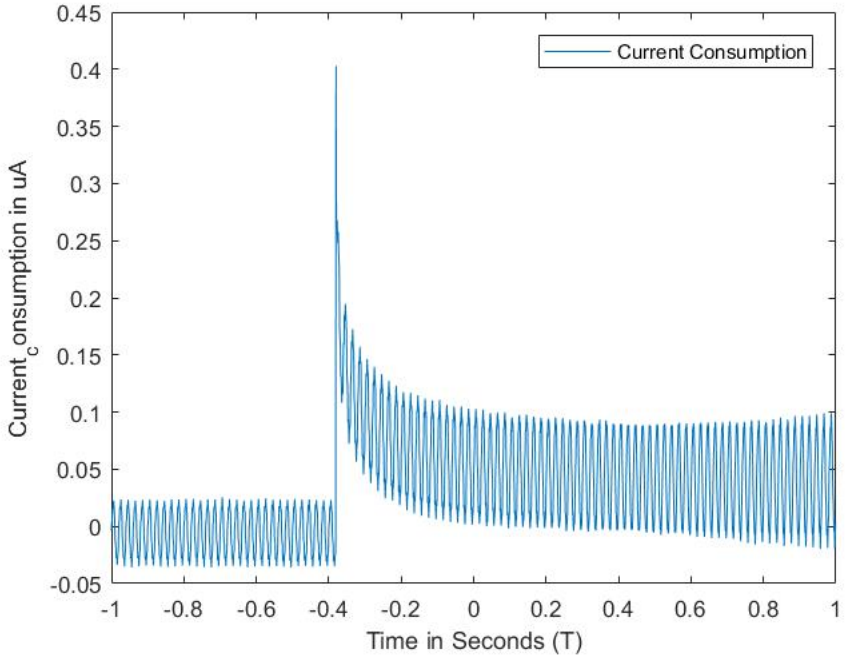


FIGURE 5.1: Current measurements provided by a single experiment

An I-V characteristics curve is not obtainable at E-INK's website and is therefore experimentally obtained.

Test Setup

The experiment consists of the segmented display in Figure 3.7(A) attached to a voltage supply. With a time interval the voltage over the pixel would switch polarity and the segmented display would switch color (Black to White and White to Black). Voltages ranging from 5V to 10V were tested with an increment of 0.5V. The μCurrent tool seen in Figure 3.7(B) as the red colored circuit board was used to measure current in nA. The output of μCurrent was in mV and has the ratio 1mV per nA current measured. Five tests per voltage level were conducted using an oscilloscope and stored to a USB

with comma separated values. The files were then imported to Matlab where a script was used to find the highest current point in the curve.

Adding all the highest current values together with their respective voltage in a matrix and then plotting these values resulted in Figure 5.2

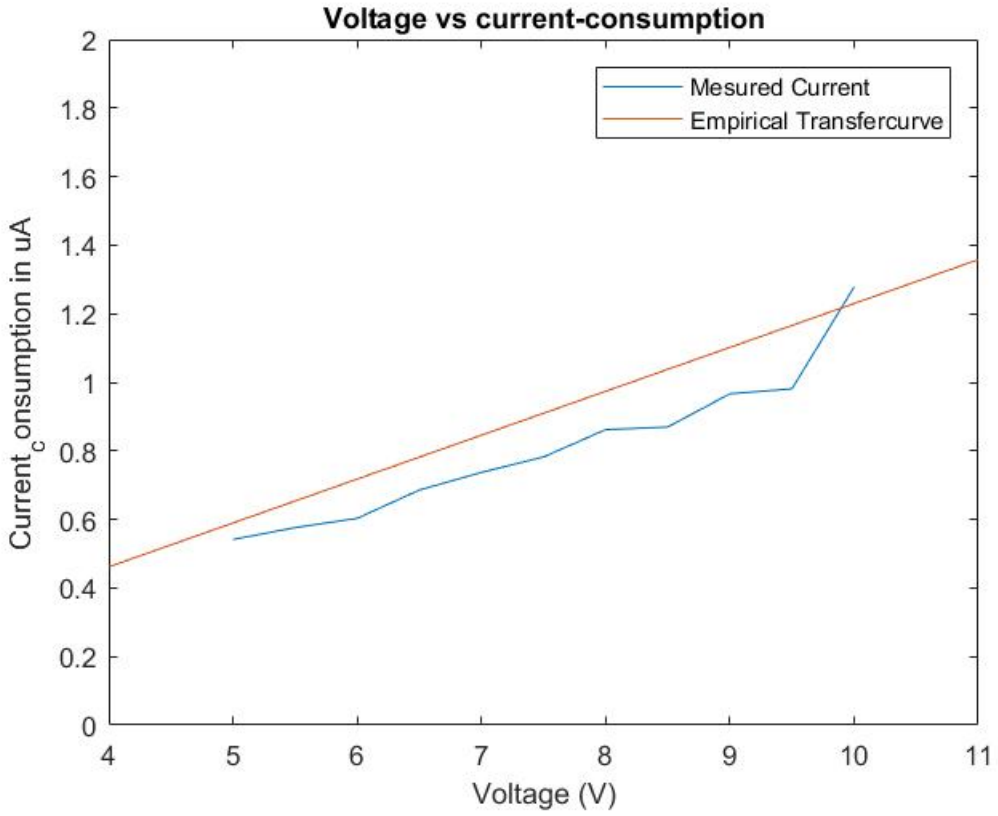


FIGURE 5.2: V-I Curve through 13 segments in a segmented display. Voltage measured at maximum value.

The voltage is limited to 10V, because the measurement was done with μCurrent and the tool starts to clip when output current reaches over 1μA. The empirical evidence shows an almost linear transfer curve across the measurements. The measurements were done with 13 segments in the display and should for this reason be divided by the same number to find avrage current through each segment. The size of the segment is 3mm x 1.67mm [29]. If a different display is chosen, different I-V characteristics will apply.

5.3 Designing a Gate Driver for Unipolar Driving Waveform

Now that the current in one such electrophoric display is known it is possible to read directly off Figure 2.14 or Figure 2.15 and find the TFT gate-source voltage. Two

questions must be decided by the designer:

- What technology process will be used on the TFT (a:Si or Poly:Si)?
- What voltage will the display run on?

It is the designers task to answer the questions above before a good gate driver can be designed.

This section will provide a general discussion to the topic of designing a gate driver for unipolar driving waveform. In a unipolar gate driver the common electrode is an active participant in writing the pixel. In fact it decides what color can be written, during that time the source lines can either write or not write that color, it can not choose to write a different color. This is how the gate driver can correctly decide the gate voltage to scan only one row at the time. Two states exist, (1) write black, and (2) write white. If writing black is VDDH on the source lines, then writing white color is VSSH on the source lines. Different gate voltages apply for black and white, this can be seen in Figure 5.3. A full gate cancellation (no current) in the upper level can be a partial or no cancelation (max current) when the common electrode switch from black to white configuration.

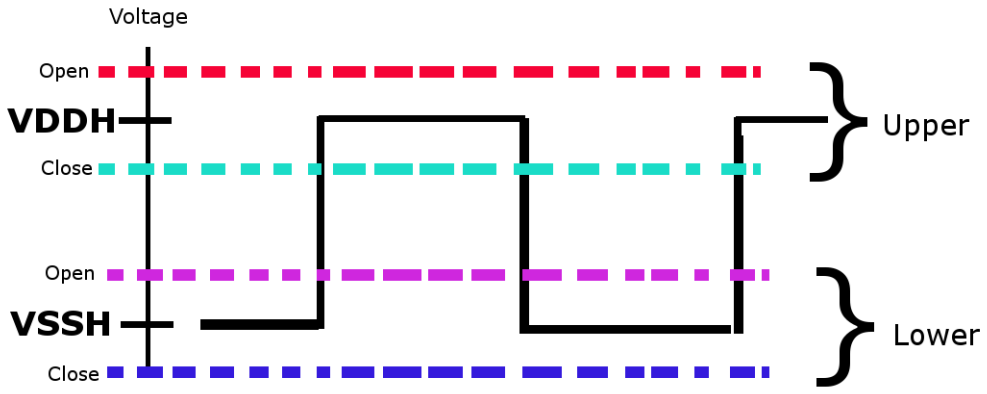


FIGURE 5.3: The two states of the gate driver

This is normally solved by driving the gate to the extremes in Figure 5.3. Depending on the chosen TFT a-Si or Poly-Si this setup can be problematic. A Poly-Si TFT seen in Figure 2.15 has a minimum at -2V, and the TFT turns partially ON if gate-source reaches -15V to -20V. There is no minimum threshold voltage for current through an EPD. The EPD pigments respond to every applied voltage [11], therefore all pixels that are OFF will be affected. The same problem exist for a-Si, but in such a low scope that it is negligible.

Topology

If the a-Si TFT is used, a simple dual level shifter as presented in Chapter 4 can supply the gate-voltage. If the Poly-Si TFT is used, a quad level shifter is a better approach. Figure 5.4 present a block diagram for that given solution.

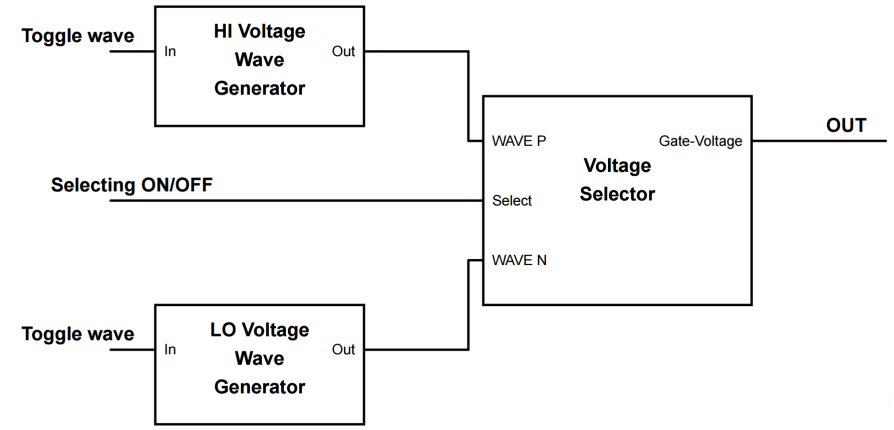


FIGURE 5.4: A quad level shifter block diagram

Design of waveform generator

The waveform generator can be designed similarly as the source driver level shifter presented in Chapter 4. The advantage of using the optimized "Negative" capacitor coupled level shifter is that it can be used to produce both positive and negative output values. It was originally designed to produce only negative output, but because both Q1 and Q2 is separated with a capacitor from INPUT, OUT is found to be fully independent from INPUT. The direction of the diode-connected transistors will also stay the same, because they are referenced to P1 and N4 *not* INPUT, and P1 and N4 is attached to HIGH and LOW voltages. For this reason the level shifter can be used to create the output voltages for the gate-driver

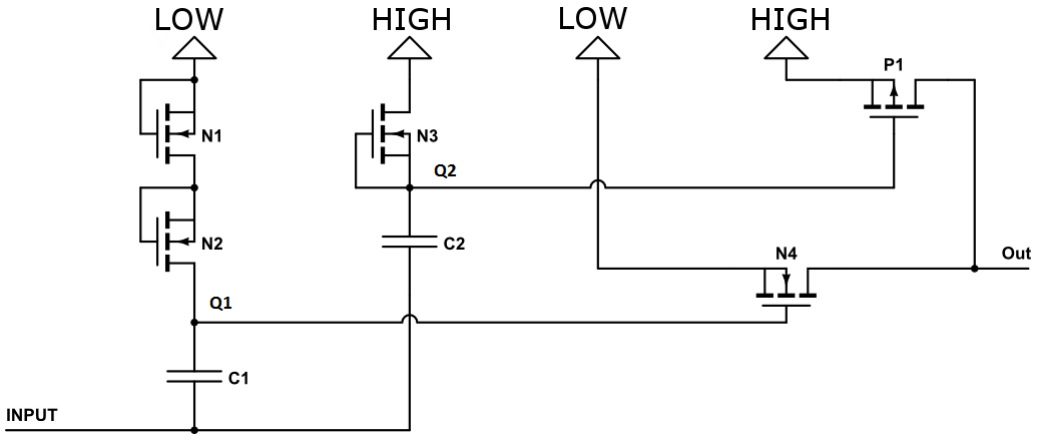


FIGURE 5.5: Using the ONCCLS as a waveform generator

The **selector** can be composed such the digital buffer in Section 3.8, described in Figure 3.13, however for a four-level output this buffer will not work since it only support two levels.

An optional selector is created by the author but requires an updated block diagram topology as seen in Figure 5.6. The two diode-connected transistors N1, and N2 can be seen as two separate half wave rectifiers, where the LOW (HIGH) voltage will be available in Q1 (Q2). Now that the voltage is split into two channels Q1 and Q2, the capacitor C1 and C2 is charge pumped when INPUT change. INPUT is then used as the selector which will navigate the voltage of Q1 (Q2) below or above the threshold voltage of N3 (P1). The transistor N3 and P1 can also be seen as a buffer which either selects the input waveform or the output is floating.

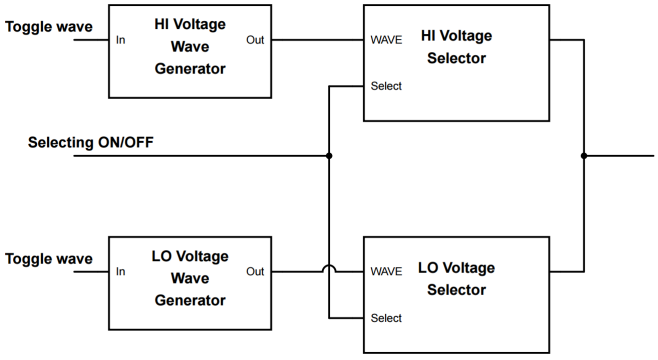


FIGURE 5.6: A quad level shifter block diagram

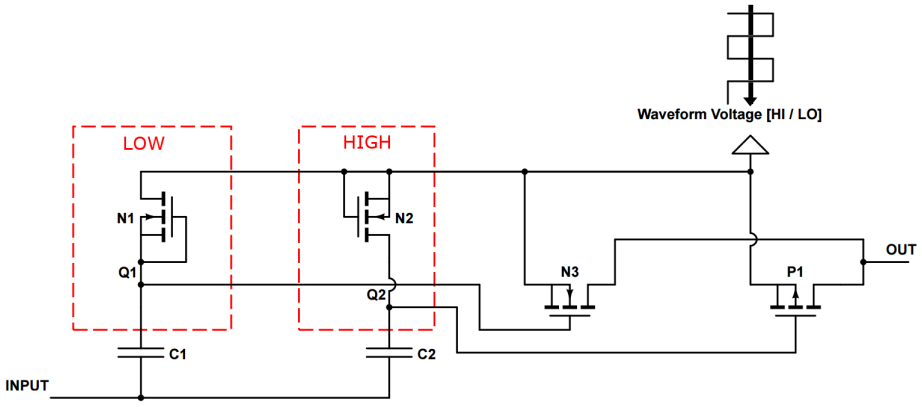


FIGURE 5.7: Selecting output depending on Source Driver output Voltage

Chapter 6

Results and Discussion

This chapter will present results from design and simulation in Cadence Virtuoso.

The results of simulating level shifters are presented in Section 6.2 through Section 6.5. The analysis in each section is done in three steps. First the steady state is presented. The second step presents the transition between steady state and transient. The last step presents the circuit running at 10MHz. All steps will show signal waveforms and accompanying power consumption waveforms. After all the circuits have been presented with their respective power consumption and waveform diagram, a full comparison table of each circuit is described in Section 6.7.

After a discussion of level shifters, the results from the gate driver analysis will be presented. The analysis will follow the same three steps as before.

6.1 Simulation Analysis

A design and simulations was conducted with Cadence Virtuoso in 180nm process technology. Throughout this chapter the following parameters was used.

- VSSL = 0V
- VDDL = 3V
- VSSH = -5V
- VDDH = 5V
- INPUT [VSSL/VDDL]

6.2 Conventional Level Shifter

As described in Chapter 3.6, the conventional level shifter can be used to gain positive output shift.

The conventional level shifter is described and used for reference in several papers, [8] [3], and will for this reason be analyzed and used for reference when describing other proposed level shifters.

The transition from steady state to transient is skipped because the circuit behaves as if it is in steady state between transition.

6.2.1 Steady State

In steady state the circuit uses very little current, the conventional level shifter draws a limited power of a few hundred femto watt seen in Figure 6.2. The signals are presented in in Figure 6.1.

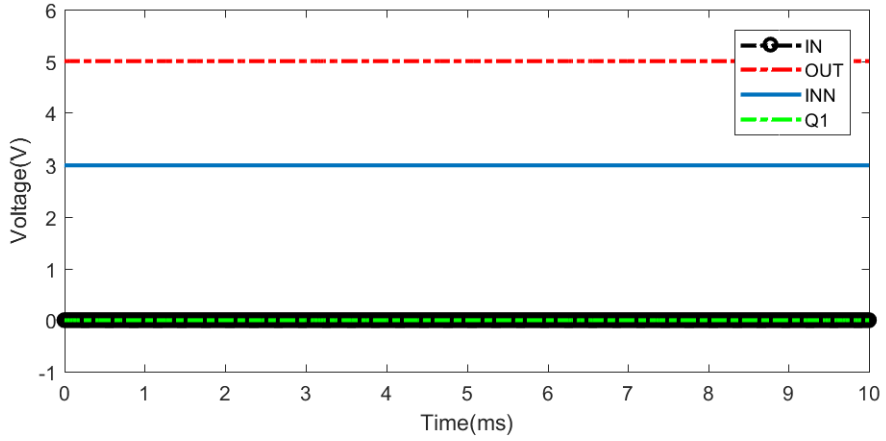


FIGURE 6.1: Steady State INPUT voltage in the conventional level shifter for 10ms

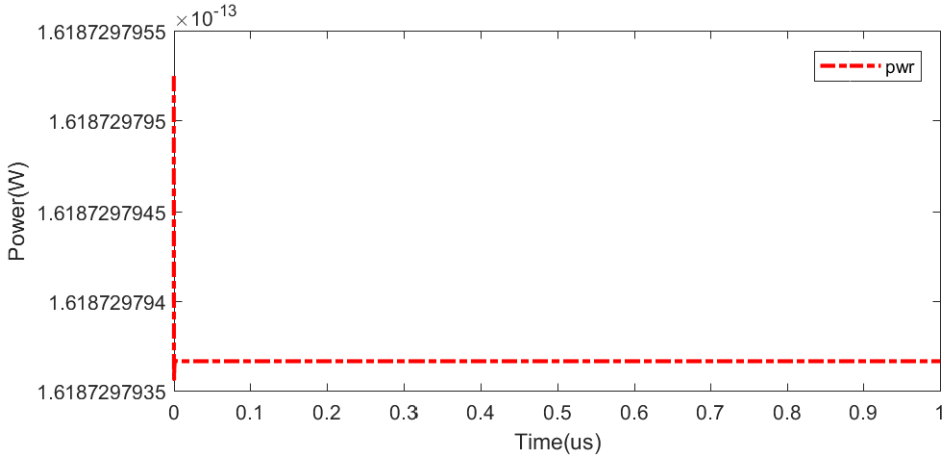


FIGURE 6.2: Power usage during steady state for a conventional level shifter.

6.2.2 Transient

The conventional level shifter has very low power consumption between transitions. The high power consumption is related to the switching activity where it can reach very high switching current. Figures 6.3 - 6.7 show the signals in the conventional level shifter during an applied 10MHz INPUT.

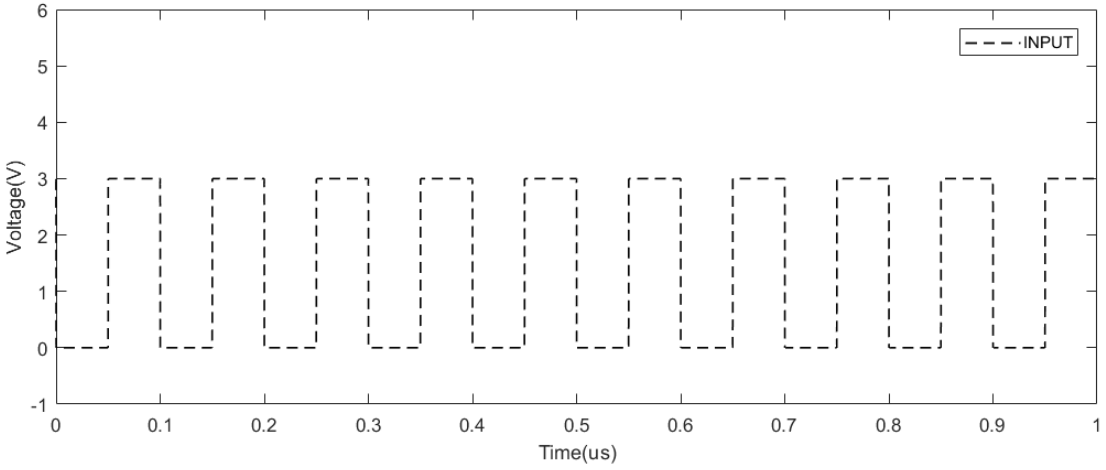


FIGURE 6.3: INPUT signal in a conventional level shifter running at 10MHz

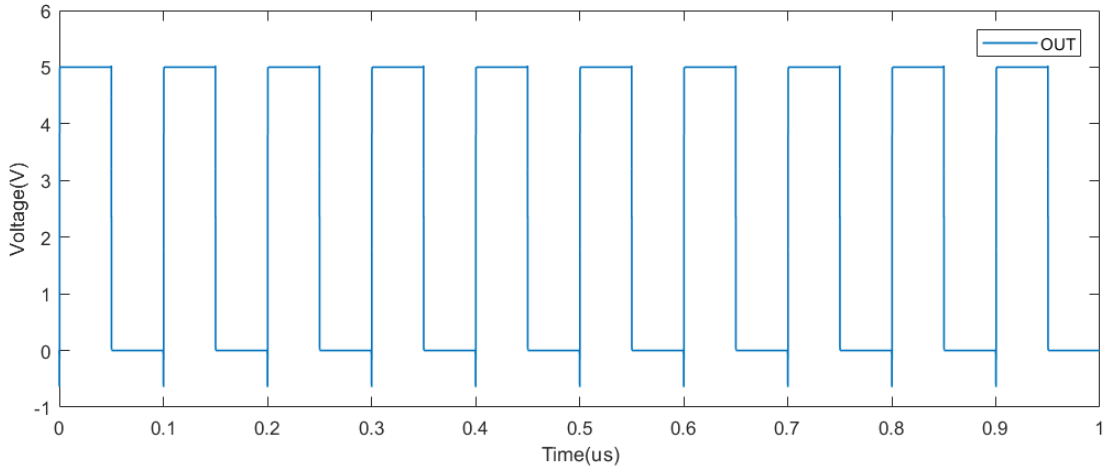


FIGURE 6.4: OUTPUT signal in a conventional level shifter running at 10MHz

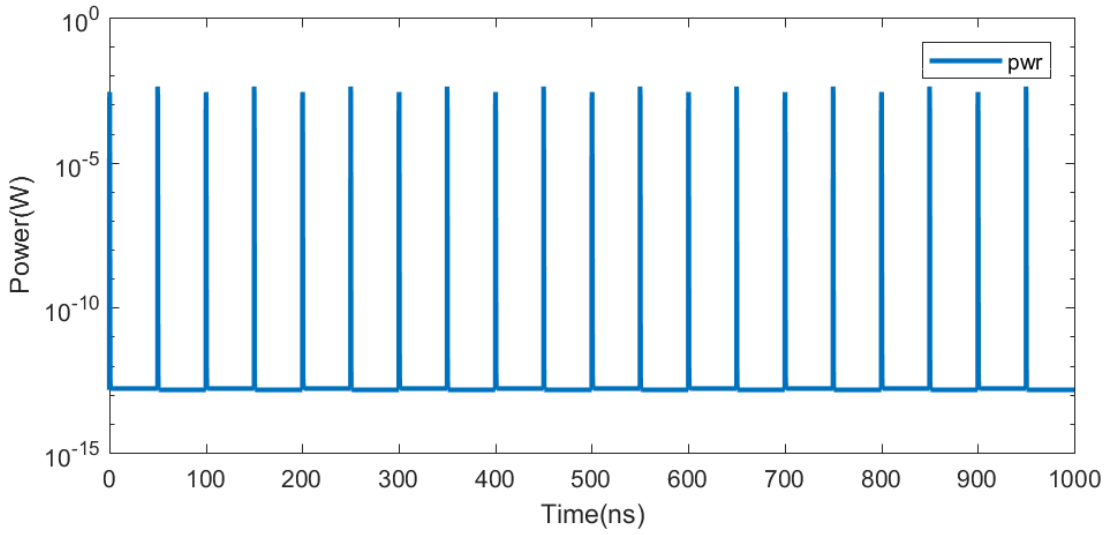


FIGURE 6.5: Power consumption during a transition in the conventional level shifter

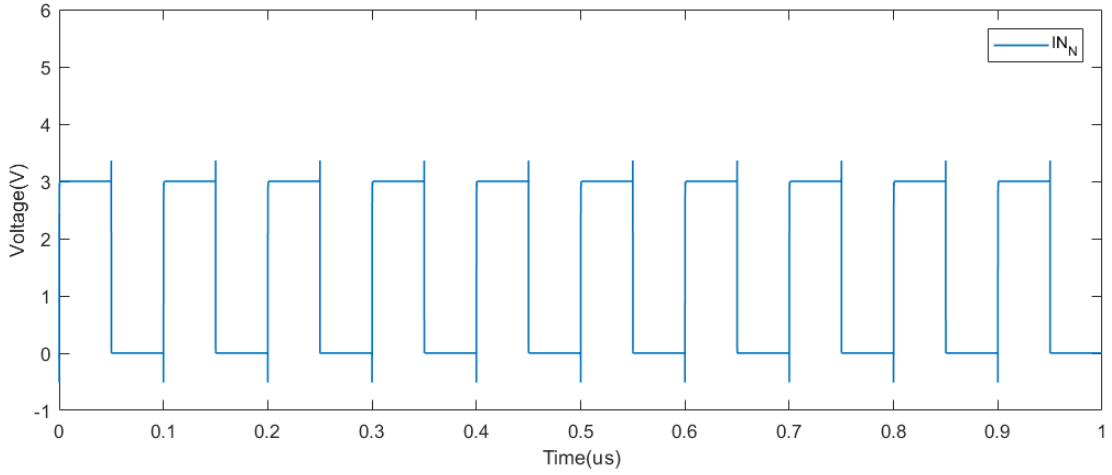


FIGURE 6.6: INPUT INVERTED signal in a conventional level shifter running at 10MHz

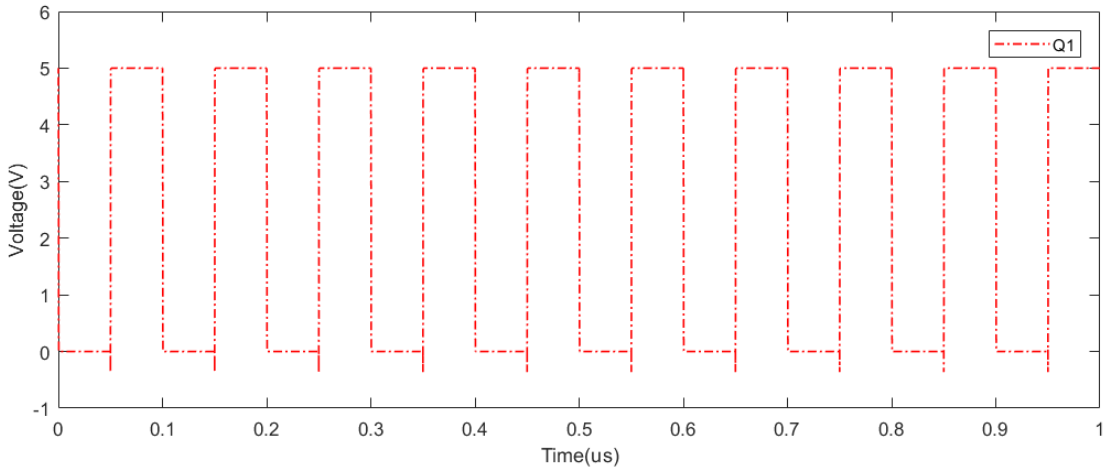


FIGURE 6.7: Q1 signal in a conventional level shifter running at 10MHz

6.3 CCLS

The capacitor coupled level shifter was described in Chapter 3.7 and is reprinted in Figure 6.8. According to [8], the diode-connected transistor N1 and N2 will charge node Q1 (Q2) to VDDH -V_{TH} (VDDH -2V_{TH}). However results of a simulation shown in Figure 6.10-6.13 indicate that this is wrong. This section will describe the CCLS with results from an analysis done with Cadence Virtuoso.

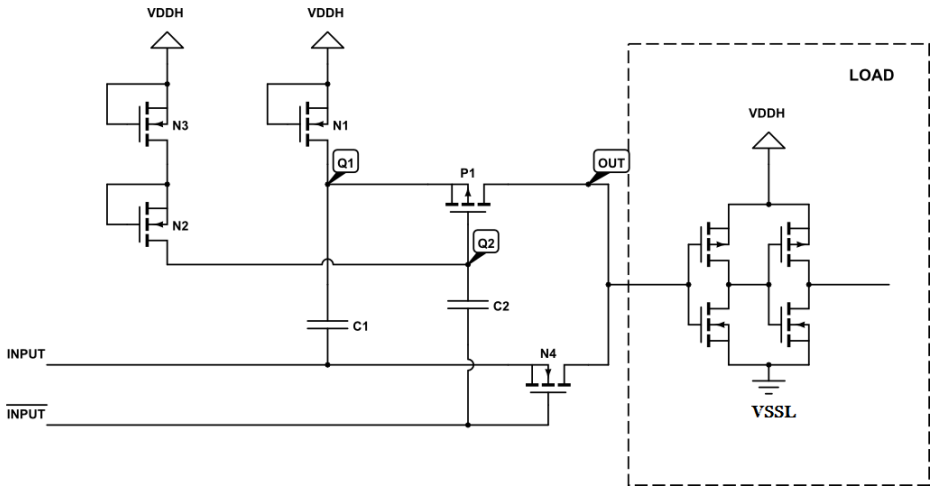


FIGURE 6.8: Capacitor Coupled Level Shifter [8]

6.3.1 Steady State

Two INPUT signals are shown in Figure 6.10, and 6.12, one when INPUT is VDDL and one when input is VSSL. The response signals (INVERTED IN), (OUT), (Q1) and (Q2) show the behaviour on the circuit. It is seen from the waveform that Q1 and Q2 does

not behave as predicted, Q1 is VDDH-v_u and Q2 is VDDH, where V_u is an unknown voltage drop seen in Figure 6.10, and 6.12. Consider the power shown in Figure 6.11 and 6.13, where the power draw is a few femtowatt to picowatt. Therefore the actual current through the diode-connected transistor N1, N2, and N3 must be at its highest some hundred femto amps. V-I characteristics of a silicon diode given in Figure 6.9, show that the diode will not block at the known threshold voltage (V_{th}) unless there is a constant saturation current [9]. For silicon that current is typically 10^{-12} amps.

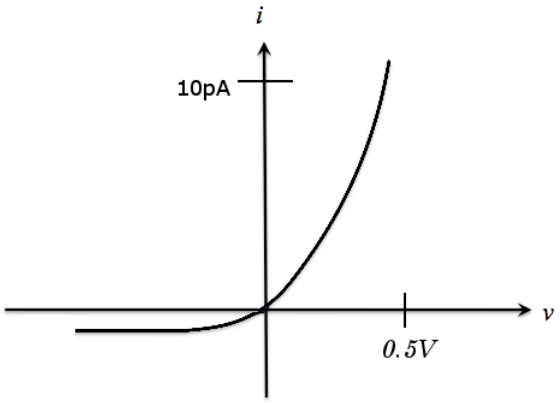


FIGURE 6.9: V-I characteristics of a silicon diode [9]

P1's V_{GS} is set by Q1 and Q2, which is slightly negative and unable to reach the required V_{th} to turn the transistor ON. The Transistor P1 is therefore OFF. INPUT is also OFF because the Inverted INPUT is *VSSL* and INPUT is *VDDL*. The OUT voltage is 3.9V in Figure 6.10, but is actually floating because both transistors N4 and P1 are OFF. A solution would be to put a pullup-resistor on the OUT signal. A floating signal is dangerous if the signal is applied to an inverter. In some cases this can force both transistors in the inverter ON and short circuit.

In Figure 6.12 the INPUT is VSSL and $\overline{\text{INPUT}}$ is VDDL. Transistor P1 will be OFF, but N1 is ON and OUT is connected to negative supply rail (VSSL) through INPUT. The power consumption is higher, this can come from higher leakage current when OUT is *not* floating but is connected to VSSL. In this state the OPEN state inverter on the LOAD is avoided, thus INPUT being VSSL is the only option to avoid floating OUT signal.

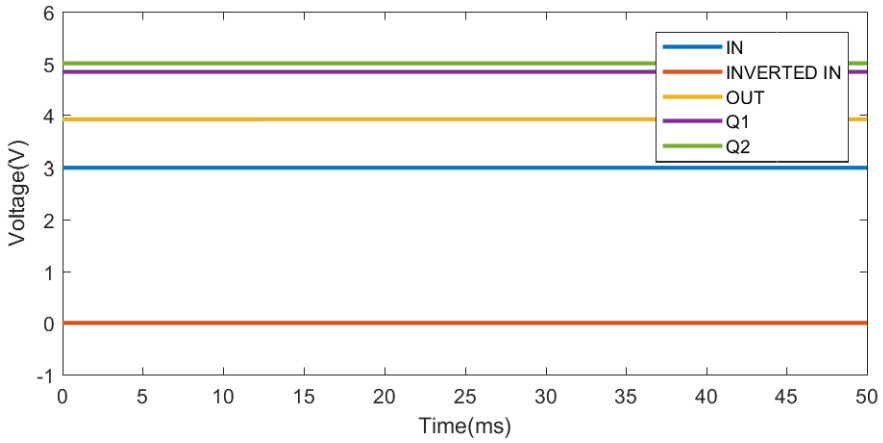


FIGURE 6.10: Merged plot of all signals in CCLS during HIGH INPUT DC voltage for 50ms

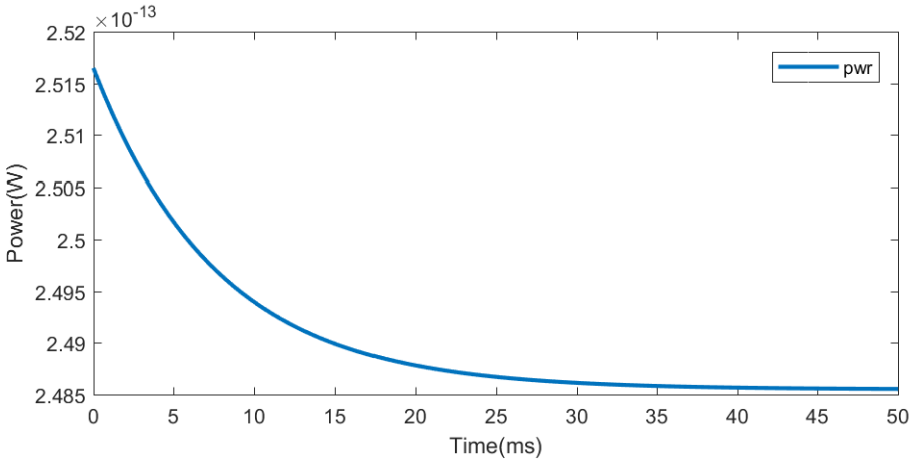


FIGURE 6.11: Power plot in CCLS during HIGH INPUT DC voltage for 50ms

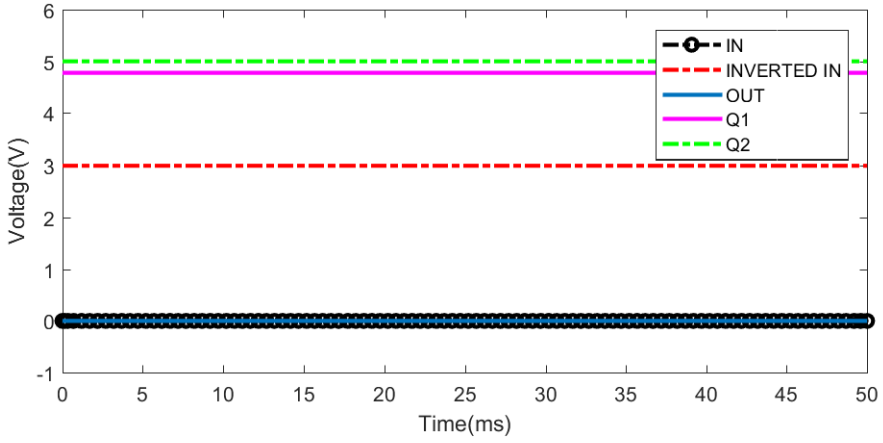


FIGURE 6.12: Merged plot of all signals in CCLS during LOW INPUT DC voltage for 50ms

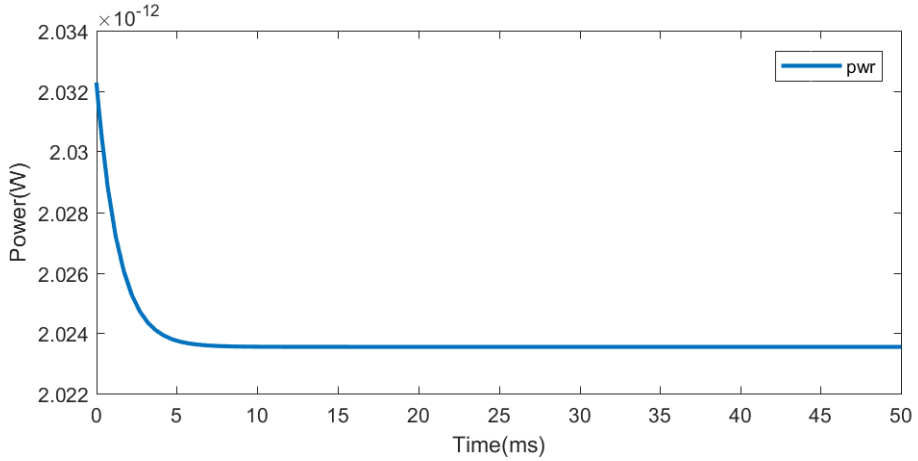


FIGURE 6.13: Power plot in CCLS during LOW INPUT DC voltage for 50ms

6.3.2 Steady State to Transient

Figure 6.14 - 6.15 is a plot of the transition between a steady state and transient state in the CCLS. There is much power drawn in the short interval of almost twenty pico-seconds during the transition. part of this power comes from the fact that there is a short-circuit in the time-interval when P1 and N4 is ON simultaniously (500ns - 500.05ns). When N4 shuts off at (500.005ns) the power consumption is still rising and is likely due to capacitor on Q2 is charging up.

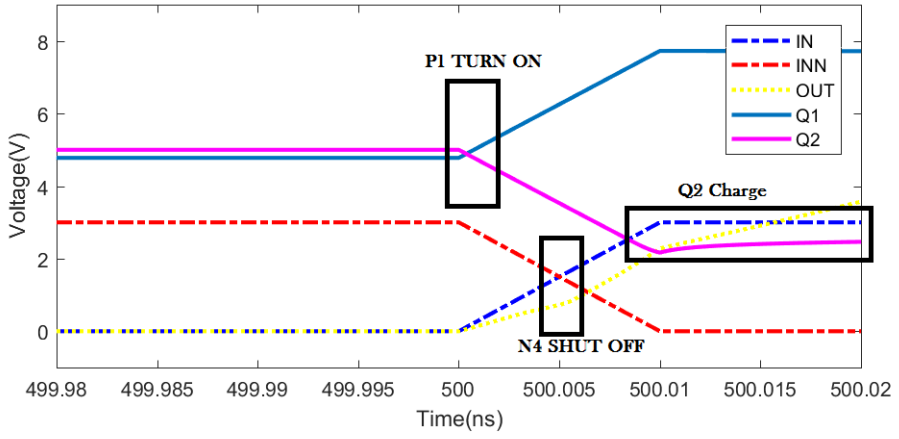


FIGURE 6.14: Merged plot of all signals in CCLS during LOW INPUT Steady State to Transient

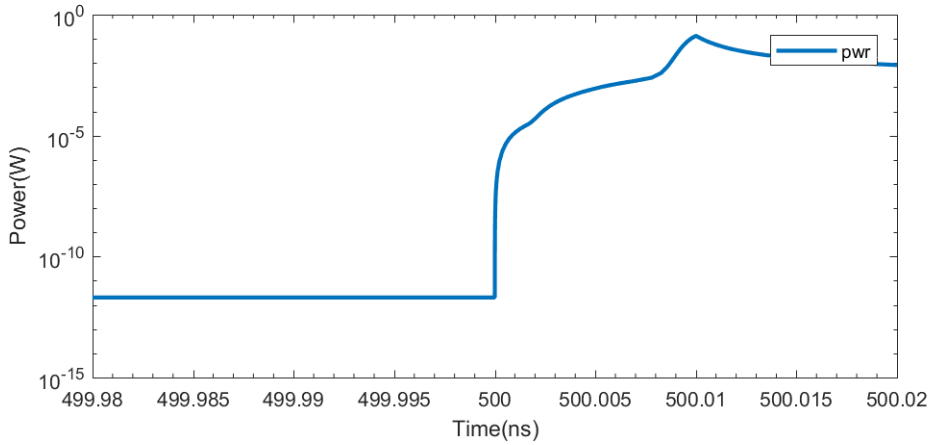


FIGURE 6.15: Logarithmic power plot in CCLS during LOW INPUT Steady State to Transient

6.3.3 Transient

Figures 6.16 - 6.18 show the signal and power consumption when the circuit is running at 10MHz. Q2 charges up in the first period after which the circuit stabilizes. The OUT signal is difficult to see in the first figure and is therefore shown as a single signal in Figure 6.17. OUT is switching between VSSL and Q1, which is much higher than required VDDH. The powerplot is given in Figure 6.18, and shows a falling power consumption as the node Q1 and Q2 is stabilizing. The floor is steadily rising. and the roof is closely stable after the first instance of change.

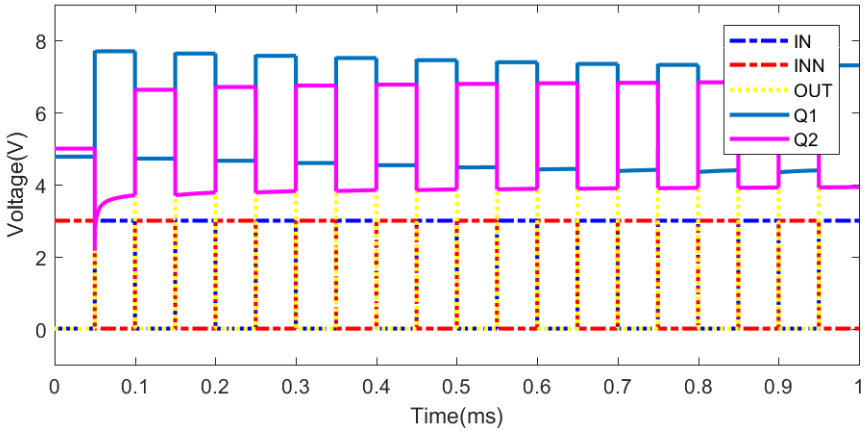


FIGURE 6.16: Merged plot of all signals in CCLS during transient

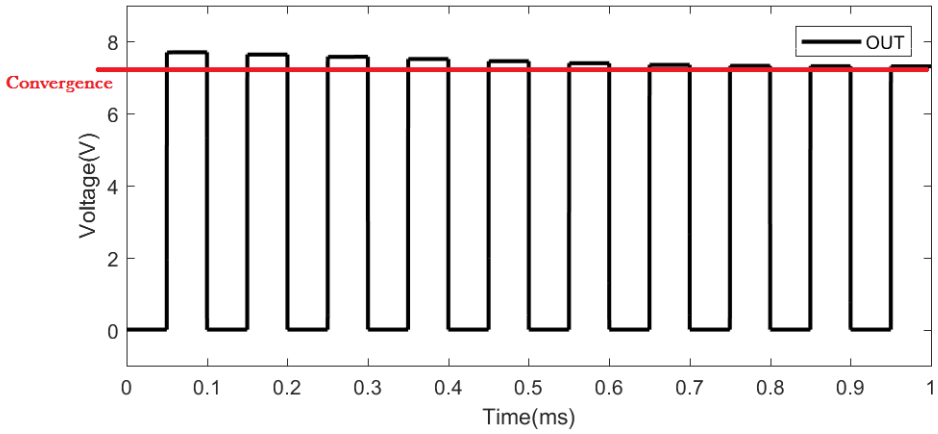


FIGURE 6.17: Plot of OUT signal in CCLS during transient

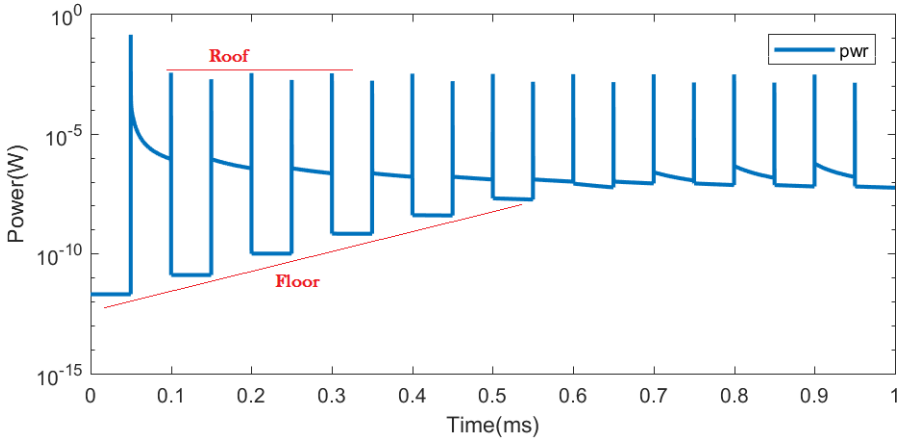


FIGURE 6.18: Logarithmic power plot in CCLS during transient

6.4 Negative CCLS

The negative capacitor coupled level shifter was presented in Chapter 4.1 and is reprinted in Figure 6.19.

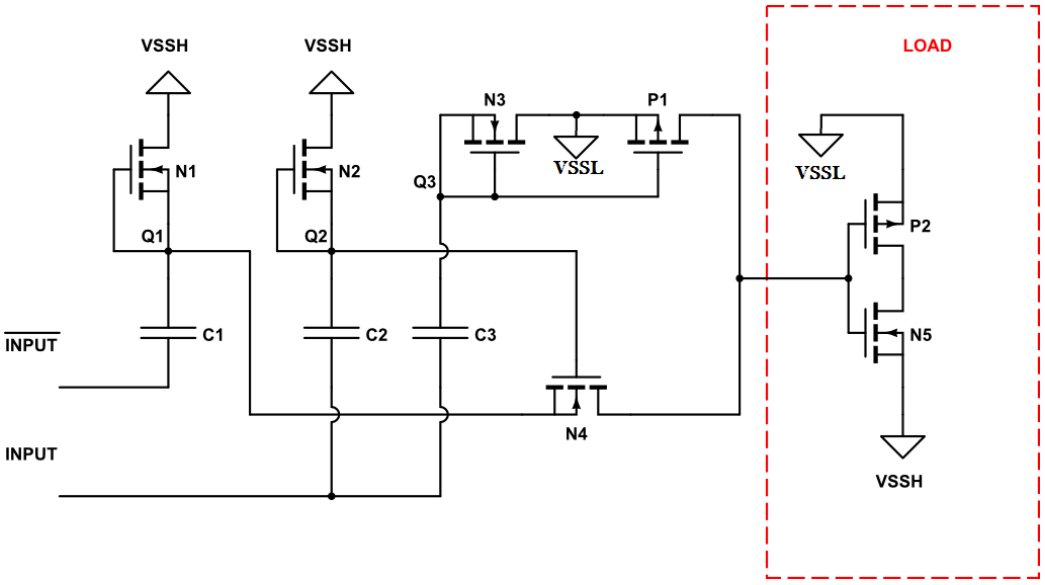


FIGURE 6.19: The Author proposes this level shifter to achieve negative levels in the capacitor coupled level shifter.

6.4.1 Steady State

A steady state signal waveform and powerplot is given in Figure 6.20 through 6.23. The diode-connected transistors will experience the same issue with the low current through the diode as seen in Figure 6.9. Hence the actual voltage on Q1 and Q2 is seen in Figure 6.20 and Fig. 6.22. Because the voltages on Q2 and Q3 do not satisfy the required threshold voltage of P1 and N4 both transistors will turn OFF. Signal OUT will therefore be floating which is unwanted. A solution would again be to attach a pull-up resistor to the floating OUT signal.

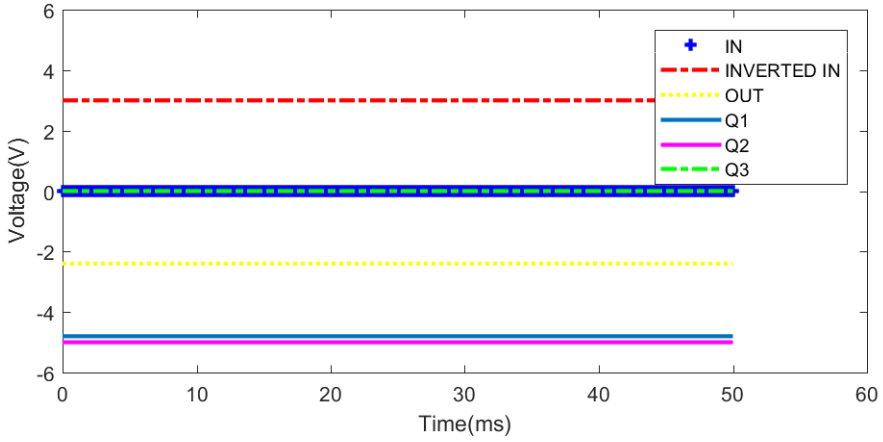


FIGURE 6.20: Merged plot of all signals in Negative CCLS during LOW INPUT DC voltage for 50ms

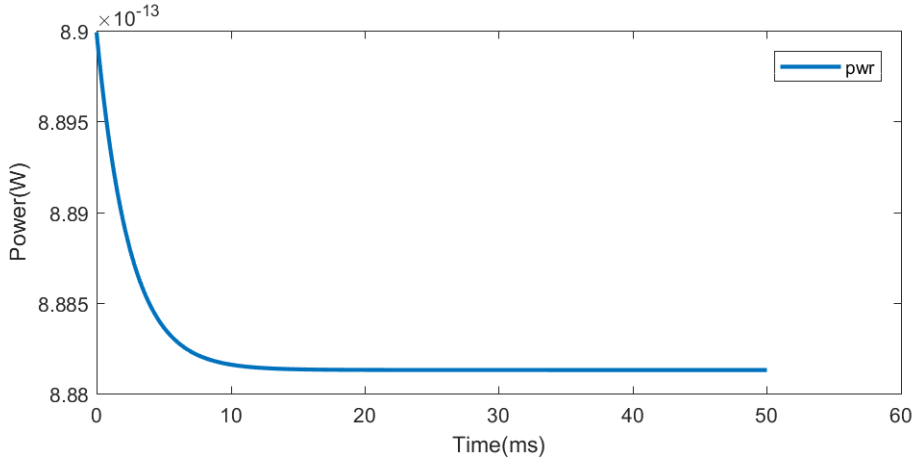


FIGURE 6.21: Power plot in Negative CCLS during LOW INPUT DC voltage for 50ms

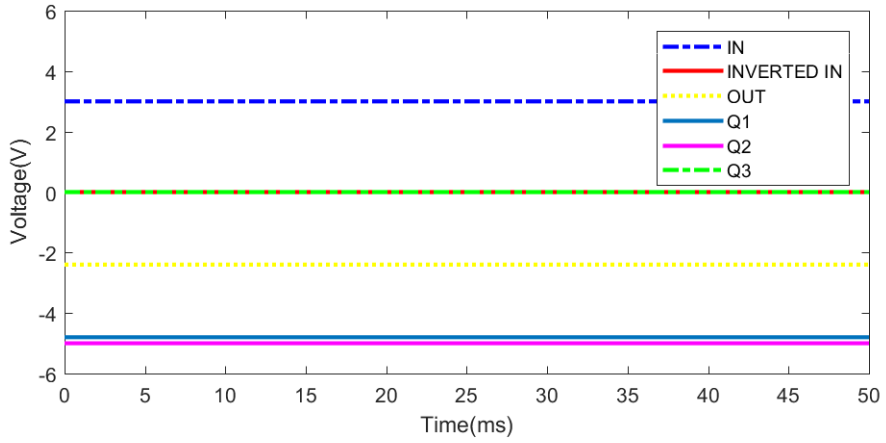


FIGURE 6.22: Merged plot of all signals in Negative CCLS during HIGH INPUT DC voltage for 50ms

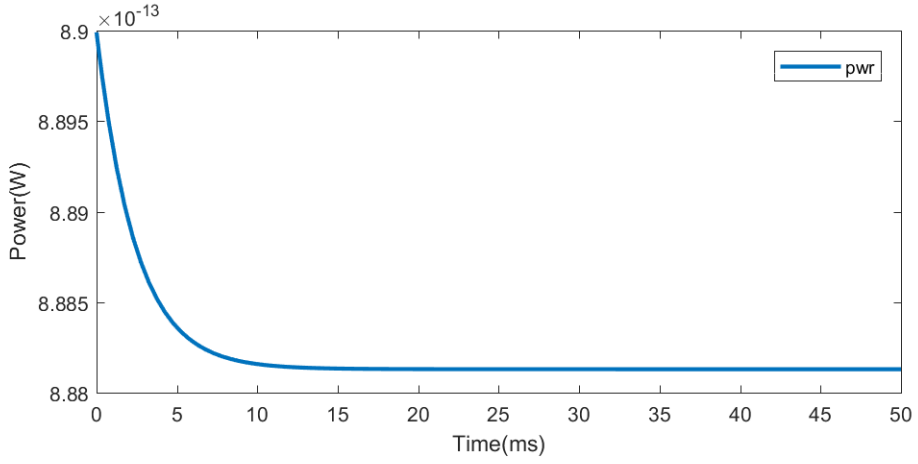


FIGURE 6.23: Power plot in Negative CCLS during HIGH INPUT DC voltage for 50ms

6.4.2 Steady State to Transient

A steady state transition to Transient signal waveform and powerplot is given in Figure 6.24 through 6.27. Figure 6.24 shows a rising input. When the input rises, Q3 will also rise but this *does not* turn P1 ON. However Q2 and Q3 will split up in two directions and the required threshold voltage on N1 is achieved, resulting in the OUT signal rising to the values of Q1. The power consumption seen in Figure 6.25 is high but should not be related to any short circuit, but rather a charge current because the capacitors connected to node Q1, Q2 and Q3 charge up. Figure 6.26 shows a falling input. Q3 will therefore also fall and this *does* turn P1 ON. Q2 and Q3 split in two directions as before but do not cross, thus keeping N4 OFF. As Q3 drops, OUT will rise to VSSL. The power consumption seen in Figure 6.27 is similar to Figure 6.25. Again, there is no short-circuit so the charge current related to charging Q1, Q2 and Q3 is a likely reason for the high power consumption.

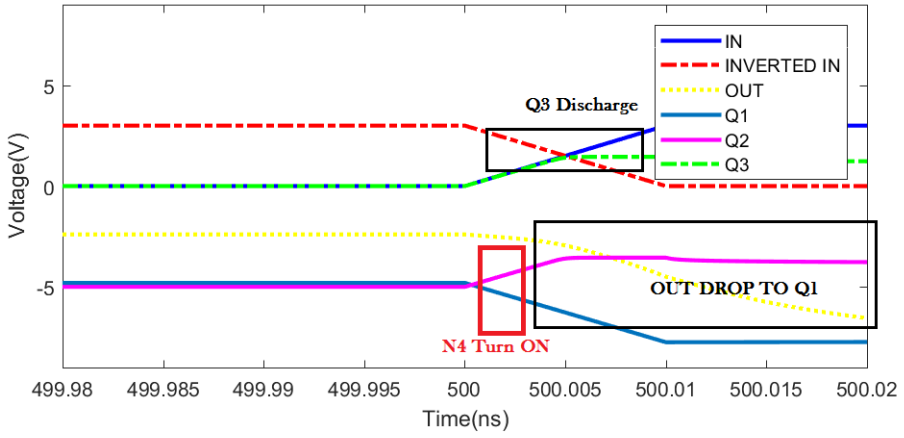


FIGURE 6.24: Transition Mergeplot

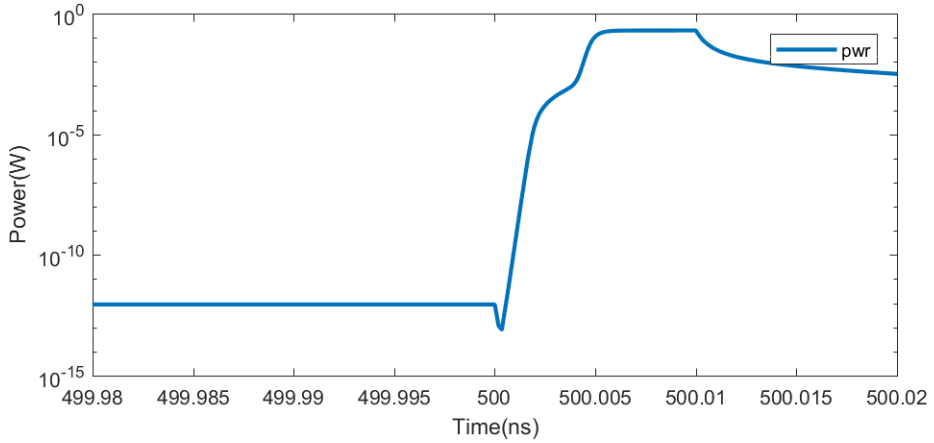


FIGURE 6.25: Power plot Transition

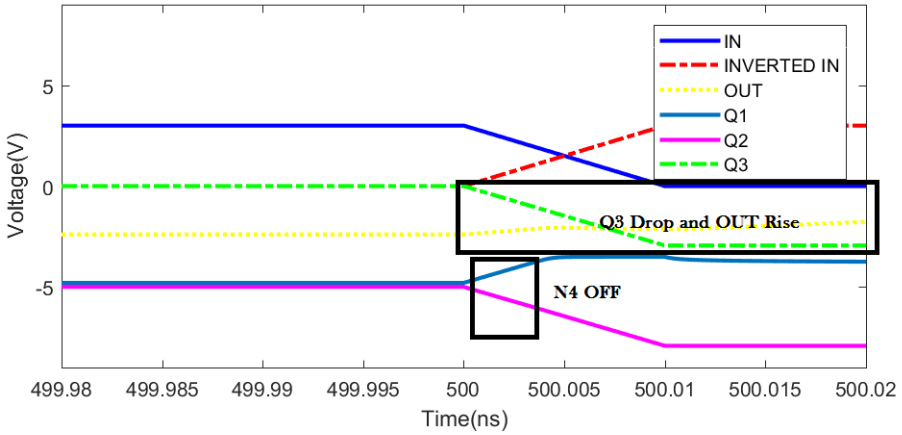


FIGURE 6.26: Mergeplot Transient

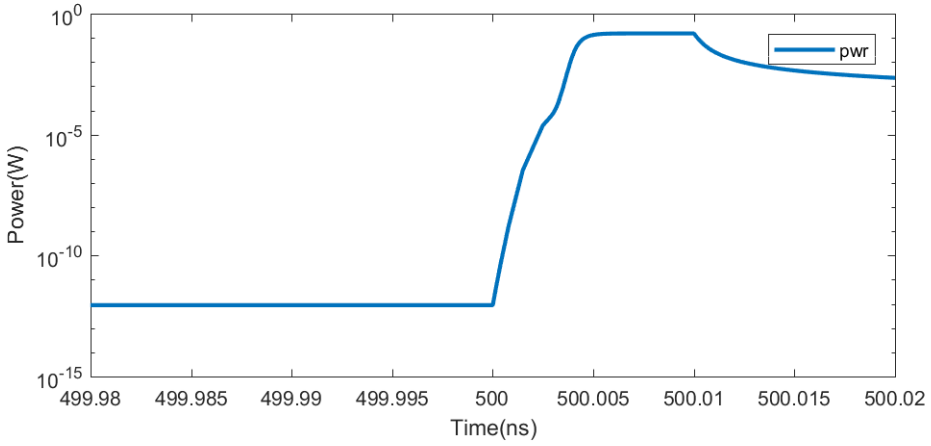


FIGURE 6.27: Power plot Transient

6.4.3 Transient

A transient signal waveform and powerplot is shown in Figure 6.28 through Figure 6.30. Because OUT signal is difficult to see in the first figure, it has been explicitly added in Figure 6.29. It is seen from Figure 6.28 that the signals are stable. Q2 and Q3 charge in the first period of INPUT, after which the signals are stable during the second period. They eventually reach a higher power consumption in third period. Similarly as with CCLS, the NCCLS has a powerconsumtion where the floor is rising as the capacitors are charging up. The roof is stable after the first period.

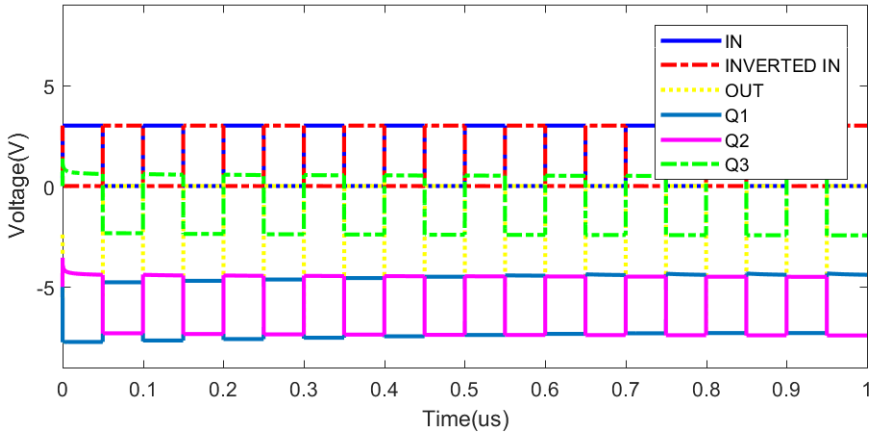


FIGURE 6.28: Transition Mergeplot

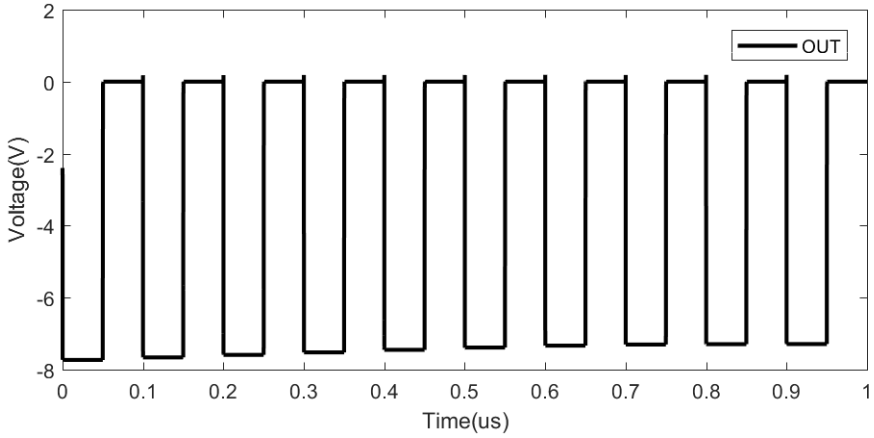


FIGURE 6.29: OUTPUT signal in a transient waveform

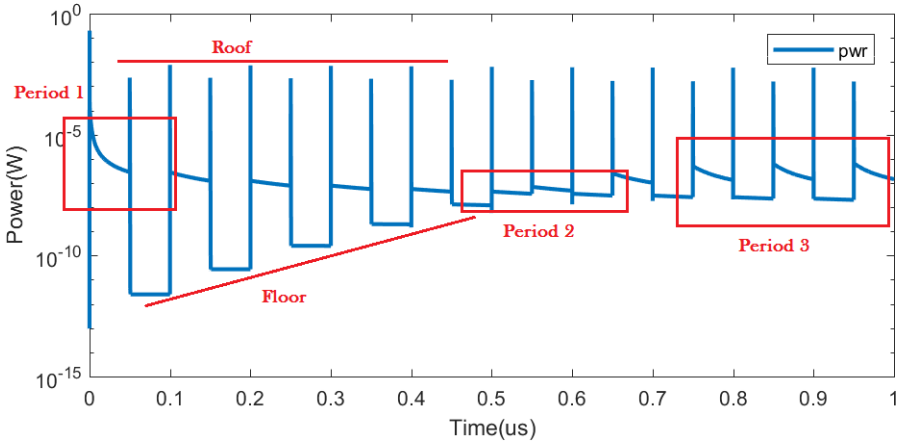


FIGURE 6.30: Power plot Transition

6.5 Optimized Negative Capacitor Coupled Level Shifter (ONCCLS)

The optimized negative capacitor coupled level shifter was presented in Chapter 4.2 and is reprinted in Figure 6.31.

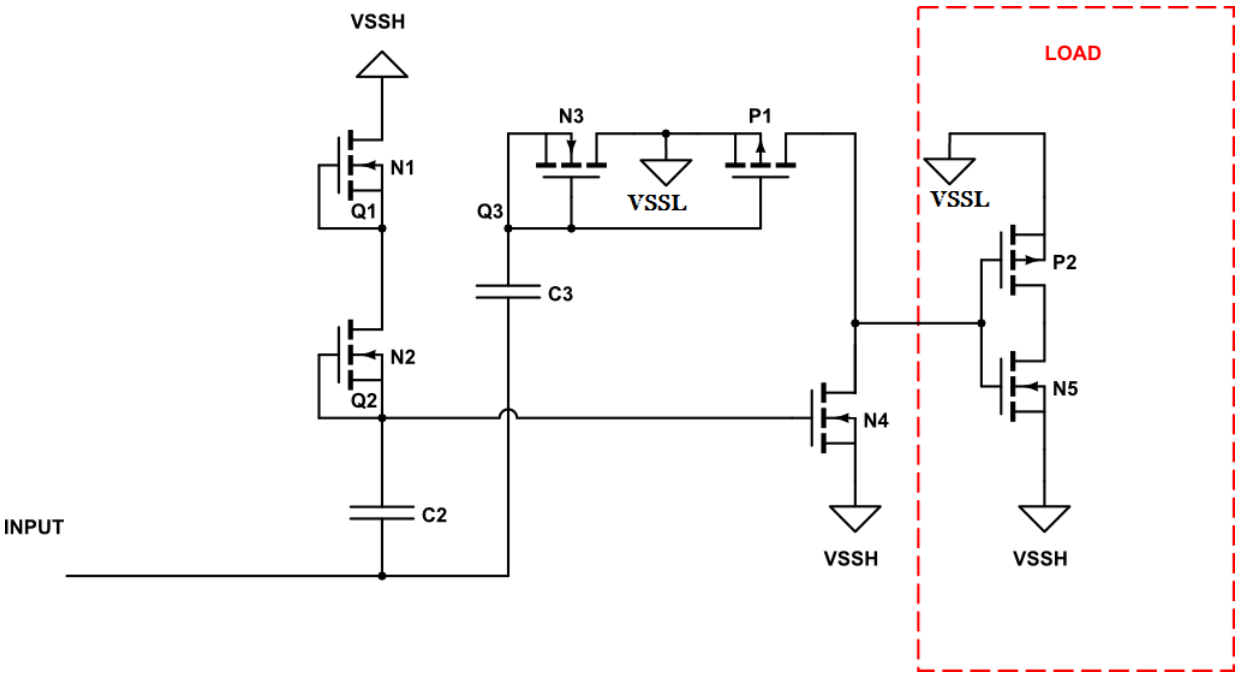


FIGURE 6.31: Optimized negative level-shifter with two capacitors instead of three, and no $\overline{\text{INPUT}}$.

6.5.1 Steady State

A steady state signal waveform and powerplot is shown in Figure 6.32 through 6.35. The low current consumption ensures that Q2 and Q3 hold the voltage seen in Figure 6.32 and Figure 6.34. Both P1 and N4 will be OFF during steady state, and OUT signal is floating shown in Figure 6.32 as -2.5V. This can be solved with a pull-up resistor on OUT to secure a stable *known* output voltage. The power consumption is steadily decreasing over 500ms. It is about 35 femto watt, which is the lowest steady state power-consumption so far in this chapter.

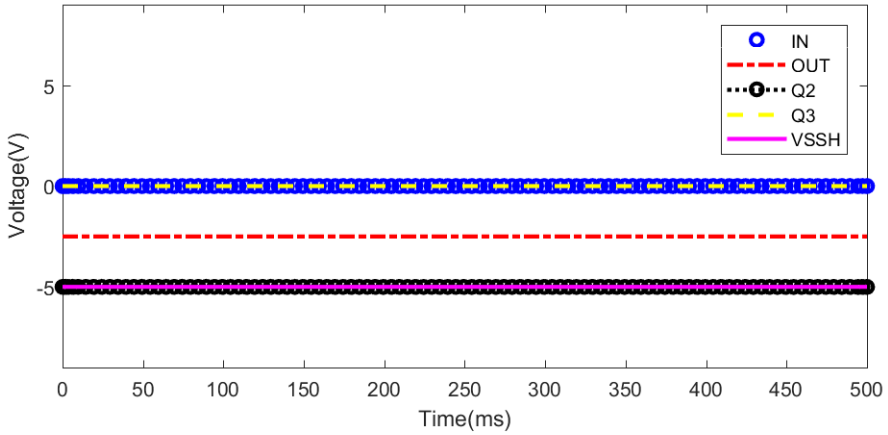


FIGURE 6.32: Merge Plot in Steady State of NCCLS

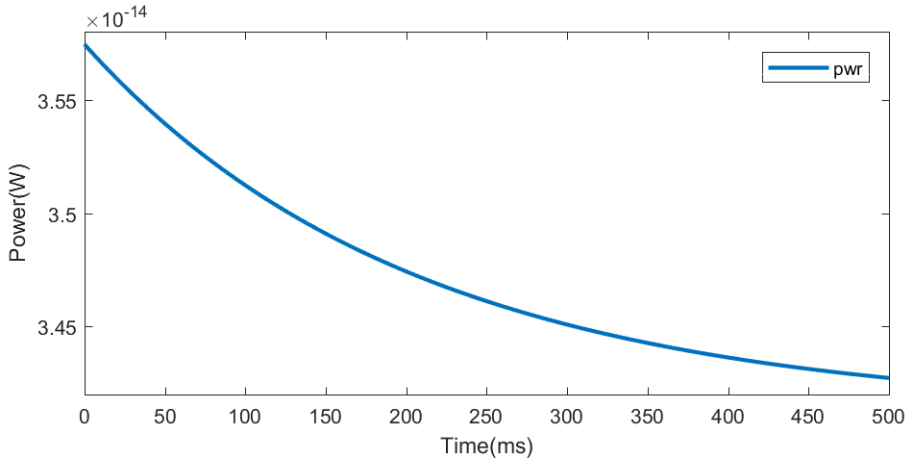


FIGURE 6.33: Power Plot in Steady State of NCCLS

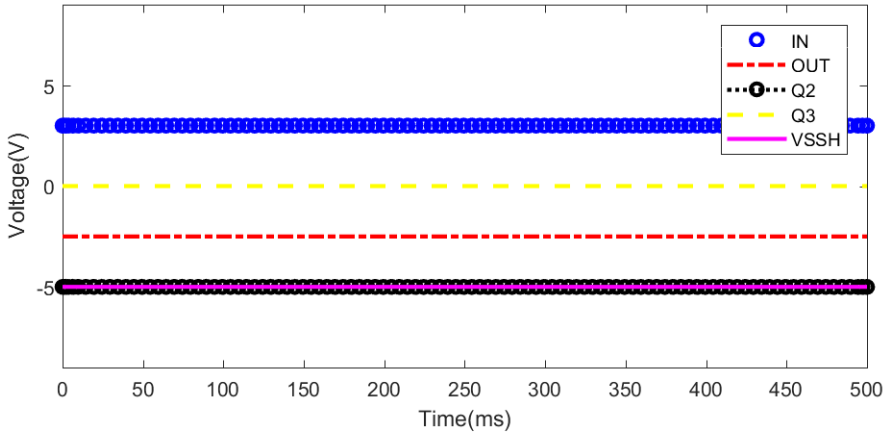


FIGURE 6.34: Merge Plot in Steady State of NCCLS

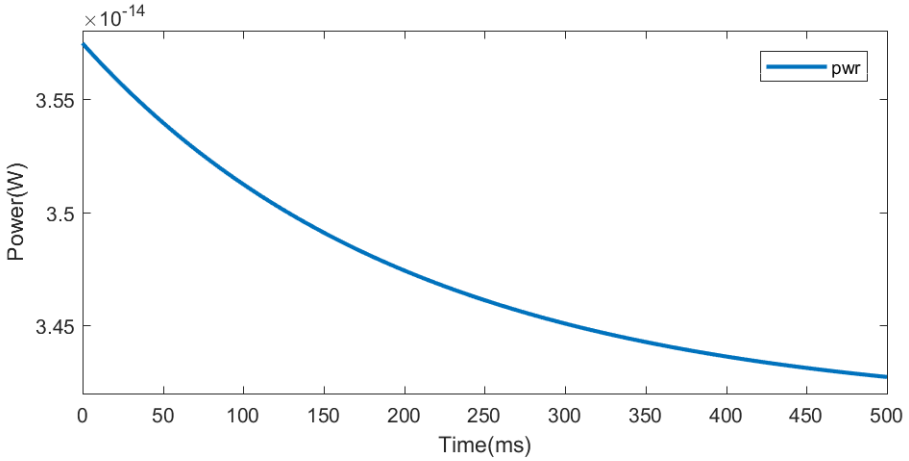


FIGURE 6.35: Power Plot in Steady State of NCCLS

6.5.2 Steady State to Transient

A steady state transition to transient signal waveform and powerplot is shown in Figure 6.38 through 6.39. A rising INPUT is seen in Figure 6.36. Since Q2 and Q3 are connected to INPUT through a capacitor they will rise as well. At approximately 500.005 ns the threshold value of N4 is reached and N4 turns ON. Subsequently, OUT starts to fall. Q3 which is rising at the same time will force transistor N3 ON and discharge. This can be seen from the curved yellow Q3 line that smoothly separates from the INPUT's rising voltage in Figure 6.36. Power consumption is given in Figure 6.37 where it steadily increases from the first switching INPUT until N4 turns ON, after which it will reach a high when Q2 is at its highest. The flattening curve of Q2 looks similar to the logarithmic power plot, a spike can be seen at 500.01 ns in both, and the curve follows the same shape.

If INPUT has been high for a long time and fall, both Q2 and Q3 will fall proportionally. As Q3 reaches the threshold voltage of P1, OUT will rise. The power consumption is shown in 6.39. It shows a much smoother power curve.

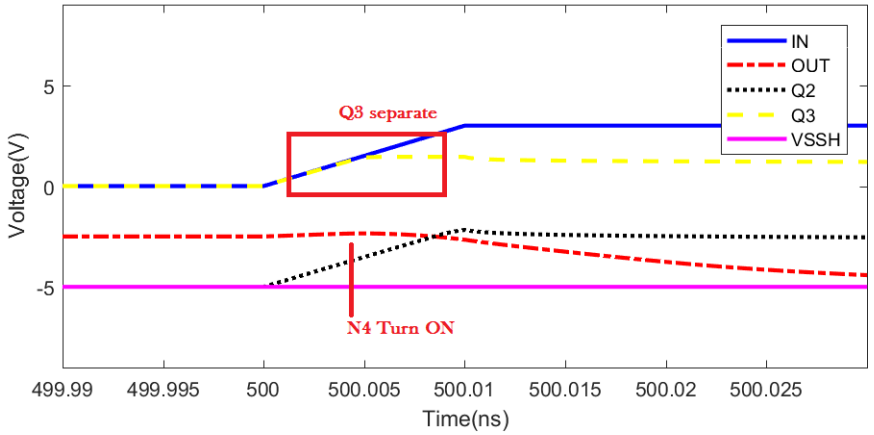


FIGURE 6.36: Merge Plot in Steady State to Transient of NCCLS

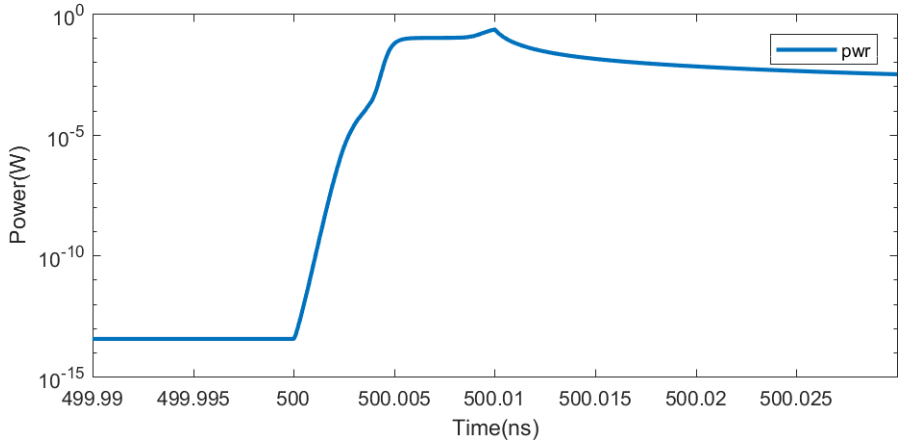


FIGURE 6.37: Power Plot in Steady State to Transient of NCCLS

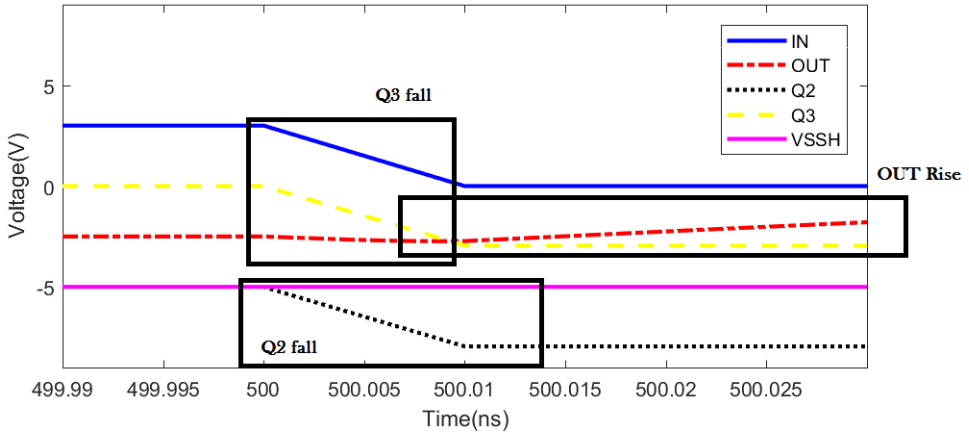


FIGURE 6.38: Merge Plot in Steady State to Transient of NCCLS

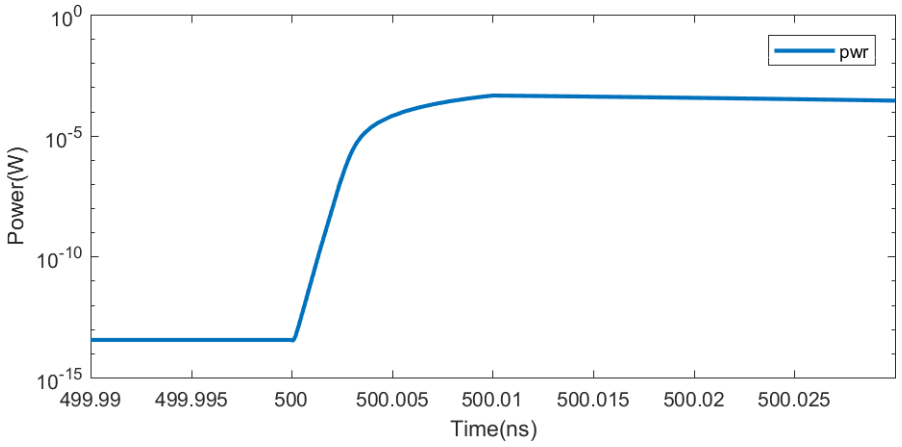


FIGURE 6.39: Power Plot in Steady State to Transient of NCCLS

6.5.3 Transient

A transient signal waveform and powerplot is shown in Figure 6.40 through Figure 6.43. The first two figures show signals and power from a rising INPUT, the second two figures show signals and power from a falling input. There are two very interesting aspects to notice in these figures. Power is steadily falling as Q2 settles, and the power consumption almost transitions to steady state power consumption when input is low. This may be a result of the capacitor difference between C2 and C3 where C2 is much larger the C2.

The second two figures show a falling input where OUTPUT signal is broken. This has to do with the Q2 node, which is is very slowly leaking and cannot reach the required threshold voltage to turn N4 on.

Fixing the broken OUTPUT signal

The broken OUTPUT signal is so because Q2 behaves similarly as Q3 when boosted *down* from its original state, to a lower negative state. Q3 will very slowly fall back to its original state, where a higher capacitance C2 increases time used and power consumed. A few thousand nano seconds is just not enough. The circuit is based on a original statement of the diode-connected transistor by [8] which does not hold with such low currents. However this slow falling behaviour would be very interesting if it were in the opposite direction. It would be interesting if the node Q2 would be pulled towards higher voltage when INPUT is high, and with that same slow speed fall down to its steady state VSSH.

By removing both N1 and N2 and replacing N2 with a single PMOS with the same wirecoupling, this would give those requested properties to Q2. The results are shown in Figure 6.44, running at very low frequency of 2Hz. It should be noted that the two capacitors C2 and C3 are the same. The Q2 node is stable at 5 volt. Q2 is pulled

towards positive when INPUT pulls up. The leakage current is far lower in this case and the voltage is pulled further up, giving it much more time before the voltage on Q2 reaches the threshold voltage of N4 and turns OFF. The required capacitance on C2 and C3 is approximately 500fF to keep the circuit stable for 500ms. A power plot is shown in Figure 6.45 for reference. Adding this property to previously presented circuits, would make them better in terms of power, stability, speed, and capacitance sizes. This is because more stable circuits require less capacitance to work, increasing speed and therefore decreasing power.

Additional notes

The circuit can also be used for positive output voltages. To acheive this, replace VSSL with VDDH in Figure 6.31, and the circuit will produce positive OUTPUT signal when INPUT is *high*.

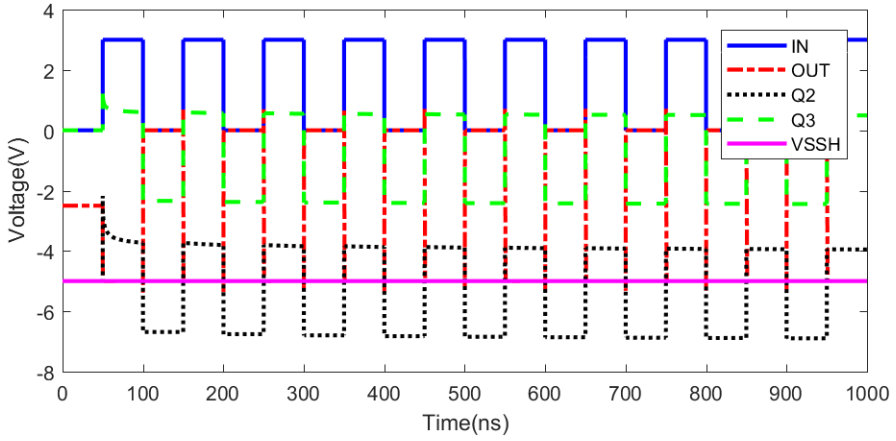


FIGURE 6.40: Merge Plot in Transient of NCCLS

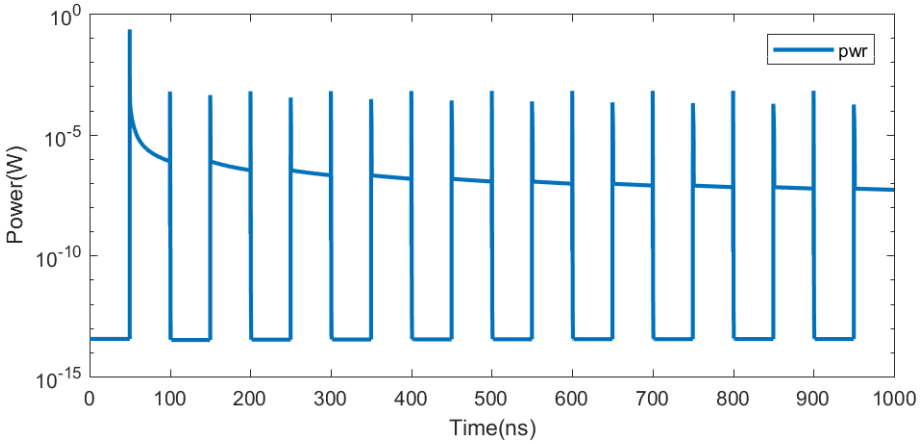


FIGURE 6.41: Power Plot in Transient of NCCLS

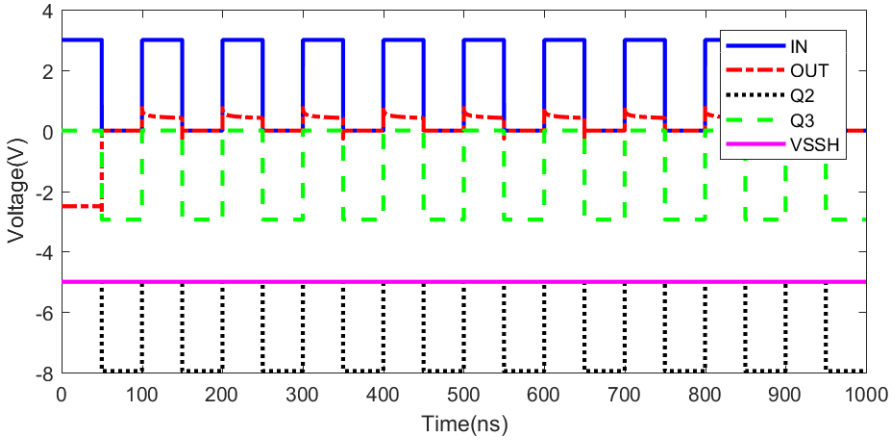


FIGURE 6.42: Merge Plot in Transient of NCCLS

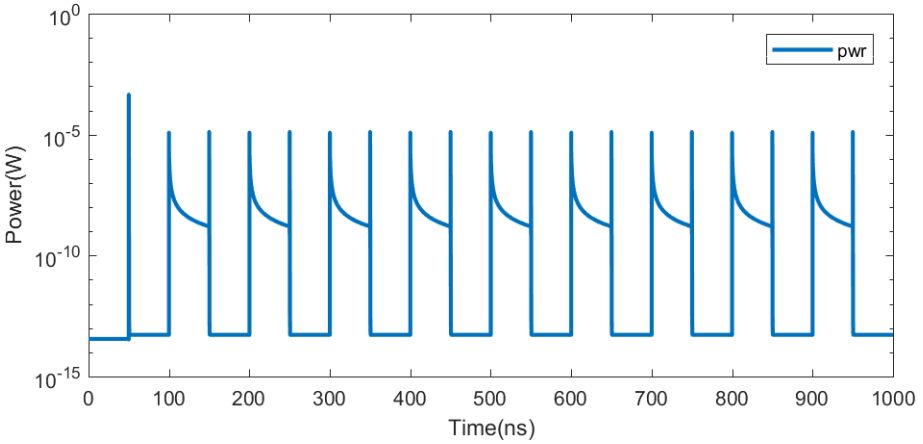


FIGURE 6.43: Power Plot in Transient of NCCLS

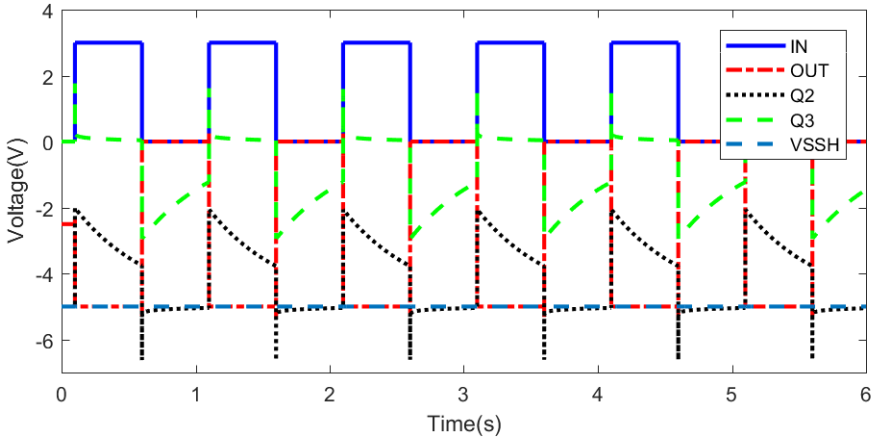


FIGURE 6.44: Merge plot of signals in transient, where NMOS transistor N1 and N2 is replaced with a single PMOS, running for 6seconds and a period of 1 second.

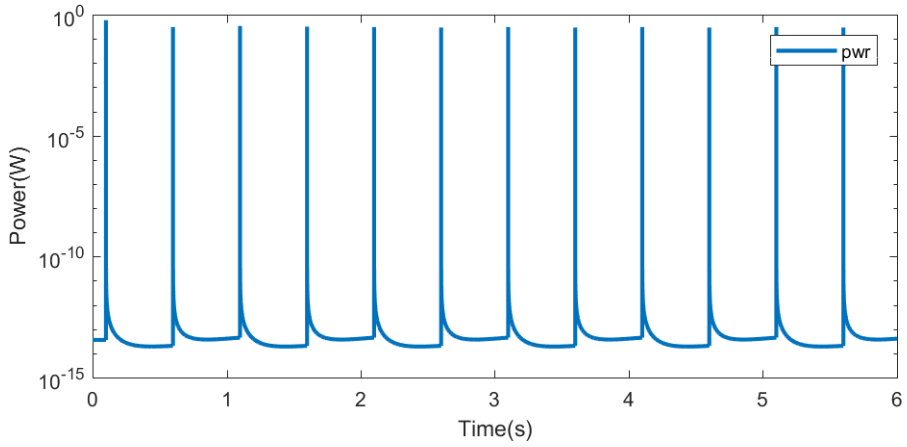


FIGURE 6.45: Power plot in transient, where NMOS transistor N1 and N2 is replaced with a single PMOS, running for 6seconds and a period of 1 second.

6.6 Gate Driver Selector

The selector was presented in Chapter 5.3 and is reprinted in Figure 6.46.

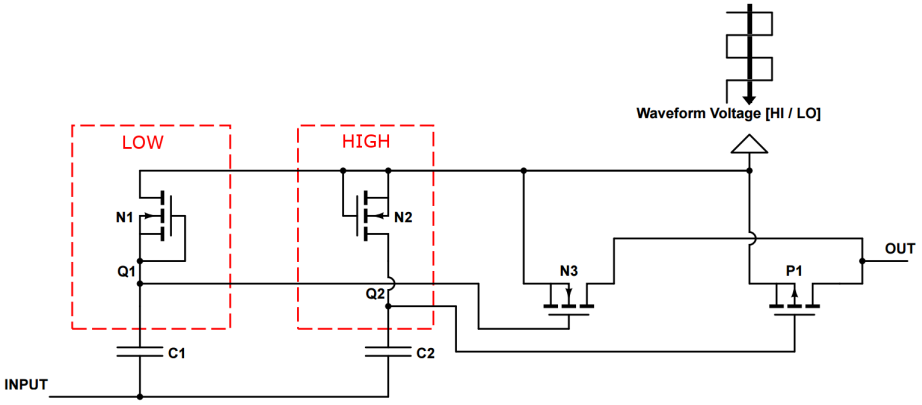


FIGURE 6.46: Selecting output depending on Source Driver output Voltage

Steady State

A steady state signal waveform and power plot is shown in Figure 6.47 and 6.48. The figure represents a steady state when INPUT is high and SRC (waveform) is -6V. The OUTPUT is driven to -6 volts because N3 turns ON when Q1 is higher then -6V+V_{th}. P1 will simultaneously turn OFF because Q2 is much higher then -6V. The Power consumption can be seen in Figure 6.48 where the power consumption is gradually falling while Q1 is charging.

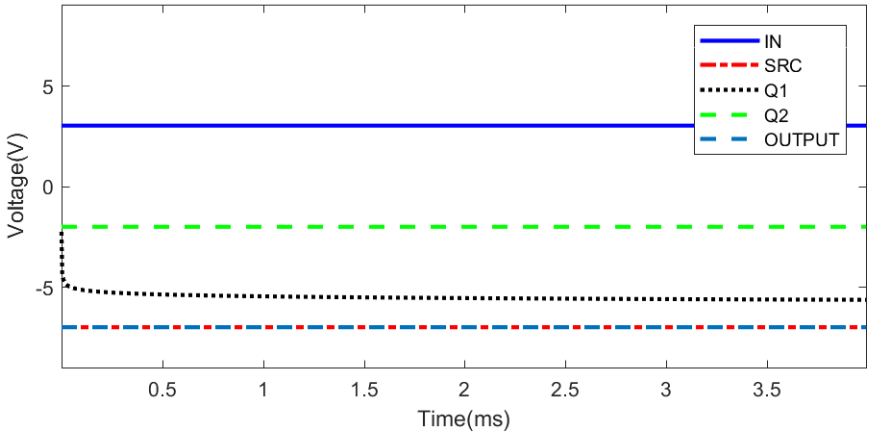


FIGURE 6.47: Merge plot of signals in steady state,

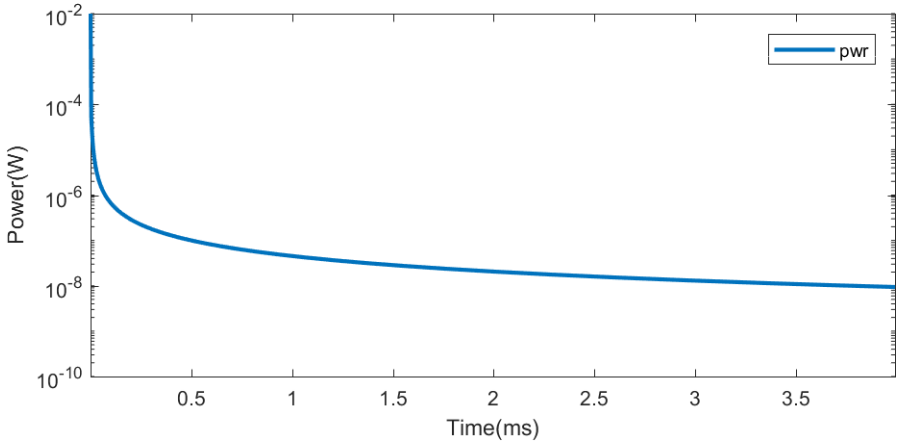


FIGURE 6.48: Power plot in steady state,

Steady State to Transient

A steady state transition to transient signal waveform and power plot is shown in Figure 6.49 and 6.50. When INPUT fall, Q1 and Q2 follow. Because the SRC is at a constant -6V, both transistors N3 and P1 will turn OFF. OUT is now floating, which is seen by the blue dotted line in Figure 6.49, at 10ms starts drifting OFF. This is the desired behaviour, because the output is also connected to a seperate equal selector (not seen here), wich should not have a floating output. When the circuit deselect the SRC the power consumption fall down to a few hundred femto watt.

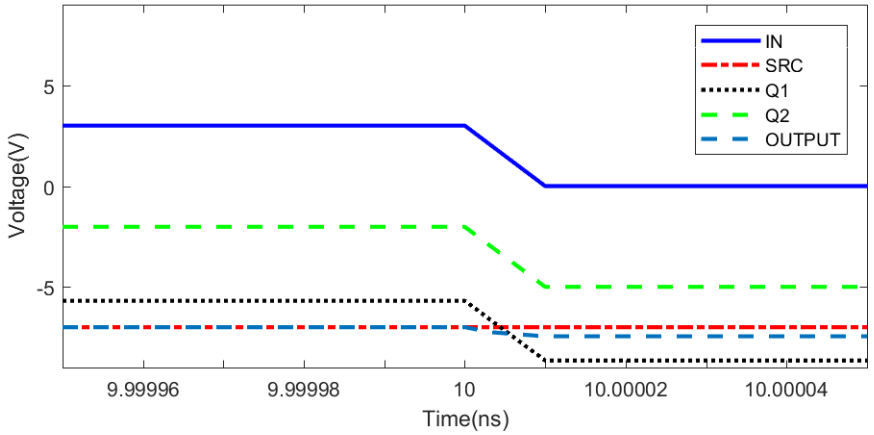


FIGURE 6.49: Merge plot of signals in steady state transition to transient

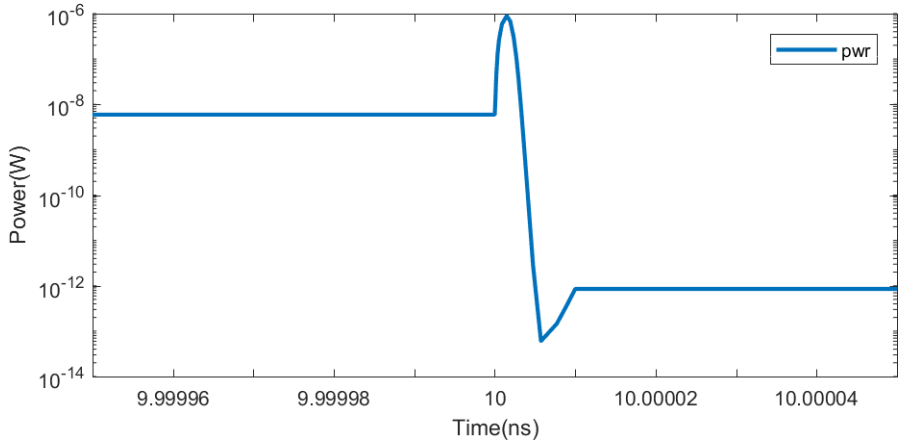


FIGURE 6.50: Power plot in steady state transition to transient

Steady State to Transient

A transient signal waveform and power plot is shown in Figure 6.51 and Figure 6.52. Because both SRC and INPUT can change independently the selector has four states. (1) When SRC is HIGH voltage, INPUT selects on *VSSL* and deselects on *VDDL*. (2) When SRC is LOW voltage, INPUT selects on *VDDL* and deselects on *VSSL*. During the deselect, it can be seen in Figure 6.53 that OUTPUT will drift OFF.

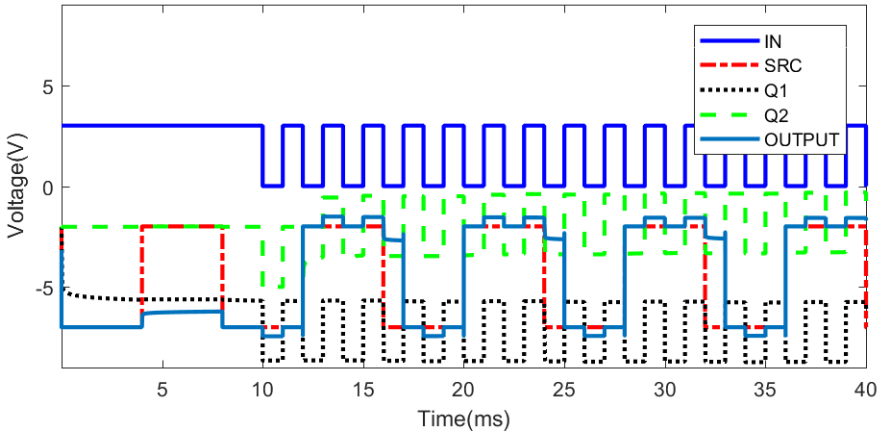


FIGURE 6.51: Merge plot of signals in transient

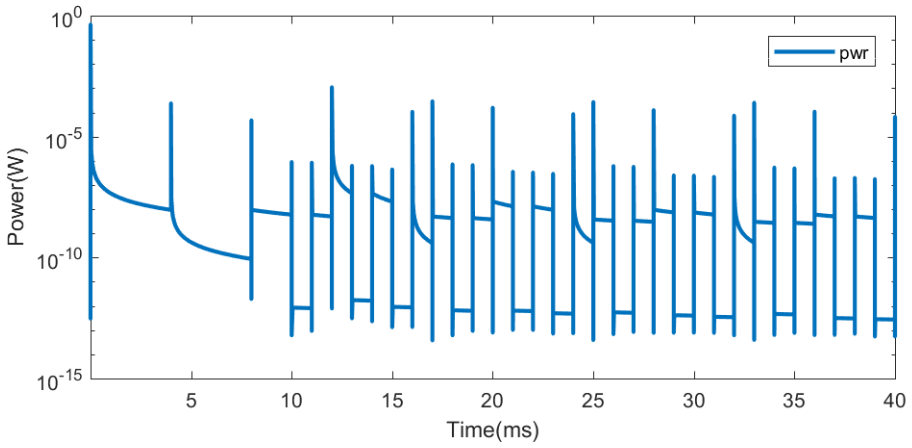


FIGURE 6.52: Power plot in transient

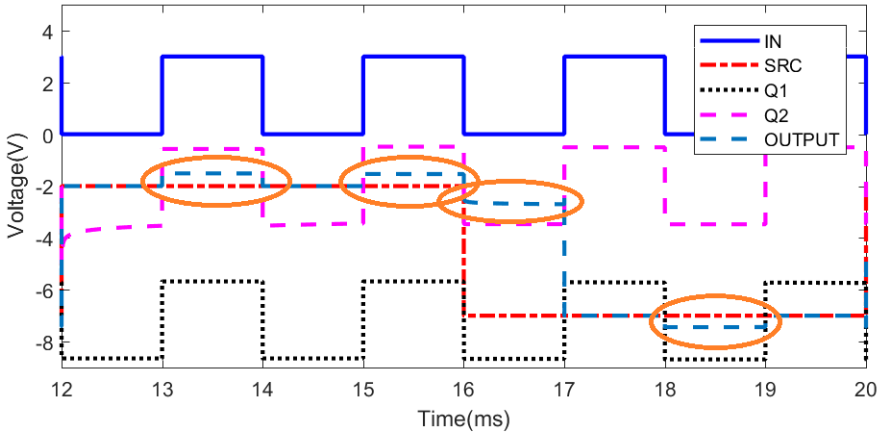


FIGURE 6.53: Merge plot of signals in transient

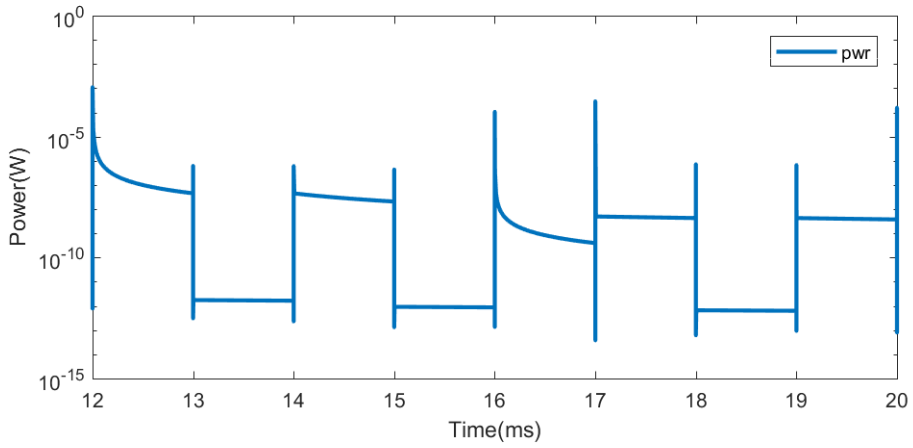


FIGURE 6.54: Power plot in transient

6.7 Discussion

Five circuits have now been described, a few alterations have been added in some circuits while presenting the results for better performance. Table 6.1 and Table 6.2 is given in an effort to compare total power consumption in each level shifter. The first table present details on level shifters that are running at 10MHz. Because the E-paper may be running at much slower speed (up to 500ms) the second table present details for level shifters running at 2Hz. The two tables represents two extremes, and the circuit is presumed to run at a speed between the two extremes. The EPD scan-process can be faster by adding the optional storage capacitor.

The two tables show that for high frequencies given in Table 6.1, the new level shifters are superior to the conventional. For a circuit running at a low frequency given in Table 6.2, the high capacitors needed will draw more power in the proposed level shifters than for the conventional level shifter. If gate tunneling (leakage through gate) is reduced, this can lead to lower capacitance which will bring down the power-consumption in the proposed level shifters.

For a low power system, pull-up resistors should be avoided. An optional solution is to attach the pull-up resistors to a switch, only to be used during critical start up and shut down intervals.

Two tables are included. **Conventional level shifter** refers to Figure 3.10. **CCLS** refers to Figure 3.11. **Negative CCLS** refers to Figure 4.1. **Negative CCLS Optimized** refers to Figure 4.2 used for negative level shift. **Negative CCLS Full Span** refers to Figure 4.2 used for a full voltage span [-5V, +5V]. **Negative CCLS Optimized (pos)** refers to Figure 4.2 used for a positive level shift.

Level Shifter	**Conventional**	**CCLS**	**NEG CCLS**	**NEG CCLS OPTIMIZED**	**Neg CCLS FULL SPAN**	**NEG CCLS OPTIMIZED (pos)**
Frequency (Hz)	10MHz	10MHz	10MHz	10MHZ	10MHZ	10MHZ
VDDL [V]	3.000	3.000	3.000	3.000	3.000	3.000
VDDH [V]	5.000	5.000	NA	NA	5.000	5.000
VSSL [V]	0.000	0.000	0.000	0.000	0.000	0.000
VSSH [V]	NA	NA	-5.000	-5.000	-5.000	NA
Rise delay [s]	4.9713e-08	13.07e-12	5.01e-08	5.46e-12	5.00e-08	4.96e-12
Fall delay [s]	5.0118e-08	67.47e-12	5.00e-08	4.99e-08	4.99e-08	4.99e-08
Rise time [s] 10% - 90%	1.0270e-10	45.00e-12	1.95e-11	2.78e-10	3.96e-11	1.57e-10
Fall time [s] 10% - 90%	1.8021e-10	63.70e-12	1.95e-11	1.26e-11	1.42e-10	1.57e-10
Power (W)	11.66e-06	1.65e-06	2.02e-06	1.47e-06	3.38e-06	1.47e-06

TABLE 6.1: Results From design analysis with Cadence Virtuoso

TABLE 6.2: Results From design analysis with Cadence Virtuoso Running at 2Hz

Type ref. [Figure]	Power (w)
Conventional [3.10]	2.6p
CCLS [3.11]	5.0p
NCCLS [4.1]	6.5p
NCCLS OPT [4.2]	4.3p

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The major work in this thesis has been to develop low power level shifters capable of delivering high voltage to vertical and horizontal lines in the display. The solutions presented is based on the capacitor coupled level shifter and the conventional level shifter. A theoretical analysis and practical measurements of the EPD, the TFT, and the level shifters have been used to investigate the solutions. The project goals will be revisited to conclude this thesis.

- Investigate and define the operation of a display driver.

  This was presented in Chapters 2 to 3.

- Use the information to describe the most power consuming parts of the display driver.

  The high number of source lines and the analog part of the source driver account for more than 60% of the power consumption in the driving circuitry.

- Investigate level shifters that can replace conventional level shifters with less power consumption.

  Two level shifters where considered and analyzed. The CCLS given in Fig. 3.11 shows impressing results compared to the conventional level shifter given in Fig. 3.10 and was further developed to support positive and negative level shift.

- Consider how a unipolar architecture will affect the gate driver.

  The gate driver can either be driven to an extreme voltage as seen in Fig. 5.3, or carefully maneuvered while the source driver shifts between black and white color. The downside of only using the extreme values is because it can lead to a partial cancellation in the TFT. The result being that all TFTs are ON simultaneously. The alternative will require a quad level shifter, which adds more circuitry. A tradeoff between power consumption and area is unavoidable.

- Model the sub circuits in Cadence Virtuoso to find the improvements.

  Although the new level shifters shows promising results at 10MHz it becomes apparent that large capacitors are required to drive the circuit at slower speed. The additional capacitors slow down the circuit, and drive up the power consumption compared to the conventional level shifter. Because the conventional level shifter is quick, and uses very low steady state power, the resultant power is less for the conventional level shifter at slower speed.

7.2 Future Work

During this work it was found that the power consumption is not linear with the frequency. A next step to analyze this circuit should be to plot the frequency versus power consumption to find the crossing point between conventional level-shifters and proposed level shifters. By adding storage capacitors the scan frequency can be increased, and the proposed level shifters would perform better at higher frequencies. Considering reverse-biasing schemes to achieve lower leakage current through gate will decrease capacitance and thereby decrease power.

Appendix A

Ghosting effect

After the old image has been replaced with a new image on the EPD, ghosting effect or sticking effect means that the old image will appear slightly on the new image as shown in Figure A.1. This is due to a remnant of the internal electric field from the previous image formed by a specific distribution of the charges substance along with its charged ions and also by the specific amount of dipoles induced in the ceiling layer. A conventional method of removing ghosting effect is by applying voltage pulses with constantly shifting polarity [25]. Switching polarity to remove ghosting is shown in Figure A.2.

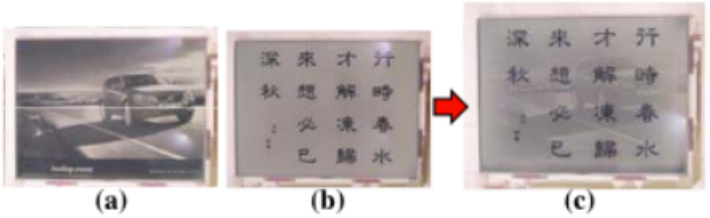


FIGURE A.1: Ghosting Effect [**?**]DTP:SDTP6057

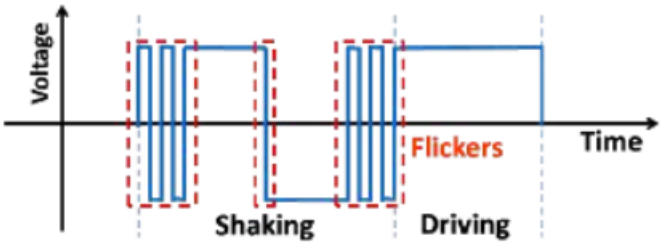


FIGURE A.2: Switching polarity to remove ghosting effect [25]

The consequence of creating flickering, is the introduction of dynamic power dissipation. It is common practise to update the EPD in four stages, as shown in Figure A.3. Clearing the display between each transition is done by inverting the previous image. The total stage time will be multiplied by four because of this.

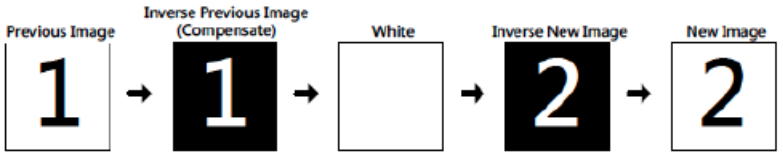


FIGURE A.3: A common practise is to use the four stage image update to remove ghosting effect [2]

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