NTNU

Norwegian University of
Science and Technology

Active Filter Capability of a Voltage Source Inverter in Marine Applications

Vegard Moritsgård Flatjord

Master of Energy and Environmental Engineering
Submission date: June 2017
Supervisor: Elisabetta Tedeschi, IEL
Co-supervisor: Hanne Rygg, Siemens

Norwegian University of Science and Technology
Department of Electric Power Engineering

Active Filter Capability of a Voltage Source Inverter in Marine Applications

Vegard Moritsgård Flatjord

June 2017

Preface

This thesis contains the work of my final semester as a master student in the Department of Electrical Power Engineering at the Norwegian University of Science and Technology (NTNU). The thesis is a continuation of a preliminary specialization project carried out in cooperation with Siemens AS in the fall of 2016.

The past year has brought insight into the life as a researcher. Being able to concentrate all my efforts on one project has been very educational to me. I am privileged to have had so many accommodating and talented people around, and I would like to thank each and every one that have contributed to the work.

Special gratitude goes to my supervisor at NTNU, Prof. Elisabetta Tedeschi. Her experience and knowledge has been a great resource throughout the year. Her availability, especially concerning the response time on e-mails, has been highly appreciated.

Secondly, I would like to thank my co-supervisor M.Sc. Hanne Rygg at Siemens, who initiated the cooperation leading to the specialization project and the final master thesis. A well defined and highly interesting problem has contributed to a rewarding year. She has closely followed the progression, and offered her much appreciated expertise within the field of power electronics.

Phd. student Atle Rygg has, with his pedagogical and educational way of explaining, contributed to the progression this last semester. His ability to quickly understand the problem and follow up with good advice is deeply valued. He has spent a significant amount of time following this project and directed me all the way.

Having support in a loving family and girlfriend has, during these five years of study, been invaluable to me. Kudos to my girlfriend keeping up with my lost brain these last weeks, i forgot it on school.

Trondheim, 22. June 2017

Vegard Moritsgård Flatjord

Abstract

This thesis is centered around the possibilities of utilizing the active filter capability of a Voltage Source Inverter (VSI) to mitigate harmonic distortion in a marine power system.

Hotel loads in marine vessels constitute an increasing part of the installed power onboard, as ships are increasingly electrified. Hotel loads represent the loads that do not contribute to the propulsion of the vessel, e.g. lighting or cranes. The system studied in this thesis is presented in figure 1. The system consists of a power supply supplying hotel loads in the MW range. The power supply, which is connected to the internal DC-grids of the ship, consists of a VSI and a LCL-filter. The problem is related to the highly distorting hotel loads propagating harmonic distortion into the system. The harmonic distortion is mainly produced from the diode rectifier stages in Variable Frequency Drives (VFDs). The VFDs are used to control AC-motor torque and speed by varying frequency and voltage at the motor terminals.

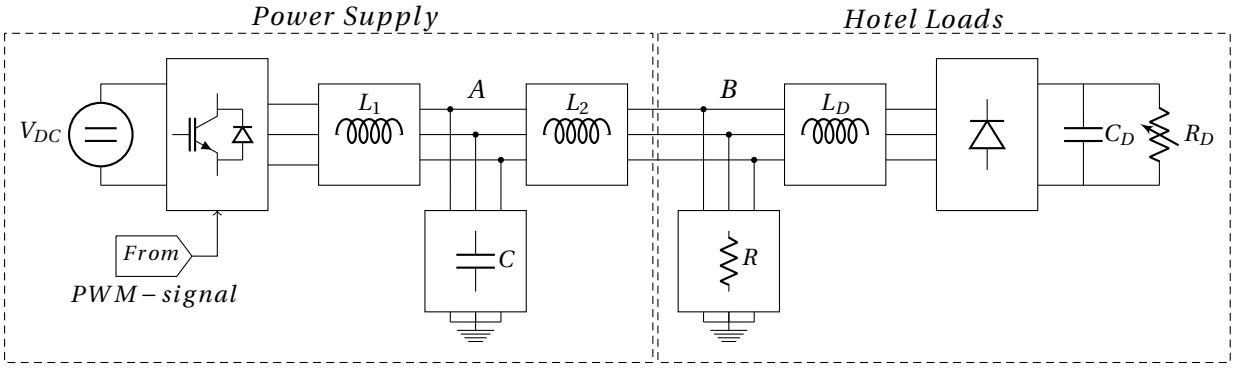


Figure 1: The system studied in this thesis.

The main objective of this thesis is to ensure a voltage waveform at point B, see figure 1, within the requirements on Total Harmonic Distortion (THD) set by Det Norske Veritas (DNV). The worst-case THD obtained in the system exceeds the requirements. Measures must be taken in order to lower the harmonic content at point B and fulfill the requirements.

An active harmonic filter integrated to the control of the VSI was developed in order to mitigate the harmonic distortion. Three cases have been simulated, with different degrees of harmonic filtering. The applied active filter features great performance and obtains a low THD well within the demands. However, it comes with a price in terms of increased power losses and the current rating of the components. Efforts were therefore made to decreasing the power losses and the system currents. Case 2 was devoted to finding the minimum power losses when still operating within the THD requirements. In the last case, a proposed degree of harmonic mitigation was simulated. This case yielded a worst-case THD well within the requirements, while still keeping both power losses and system currents within acceptable limits.

It was concluded that the active filter capability of the Voltage Source Inverter is sufficient to mitigate the harmonic distortion in the system. However, the results are strongly dependent on the parameter data; further research should therefore put more efforts into gaining more precise estimations of these data.

Samandrag

Denne masteroppgåva ser på moglegheita for å nytte spenningsstyrte vekselrettarar (VSI-ar) til å filtrere eit marint kraftsystem for harmonisk støy.

Hotell-laster ombord i marine fartøy utgjer ein aukande del av den totale installerte effekten. Dette er fordi fleire og meir kraftkrevjande installasjonar ombord krev elektrisk kraft. Hotell-laster representera dei lastene som ikkje bidreg til framdrifta av fartøyet, f.eks. belysning eller lastekranar. Systemet som er studert i denne masteren er presentert i figur 2. Systemet består av ei kraftforsyning som forsyner hotell-laster i MW storleik. Kraftforsyninga, som er kobla til DC-distribusjonsnettet ombord, består av ein VSI og eit LCL-filter. Problemet er knytt til dei harmonisk produserande hotell-lastene som forsyner kraftsystemet med harmonisk støy. Dette harmoniske støyet er hovudsakleg forårsaka av diodelikerettarane som befinn seg i variabel frekvens motordrifter. Slike motordrifter blir brukt til å kontrollere moment og fart i AC-motorar ved å kontrollere spenninga og frekvensen forsynt til motor-terminalane.

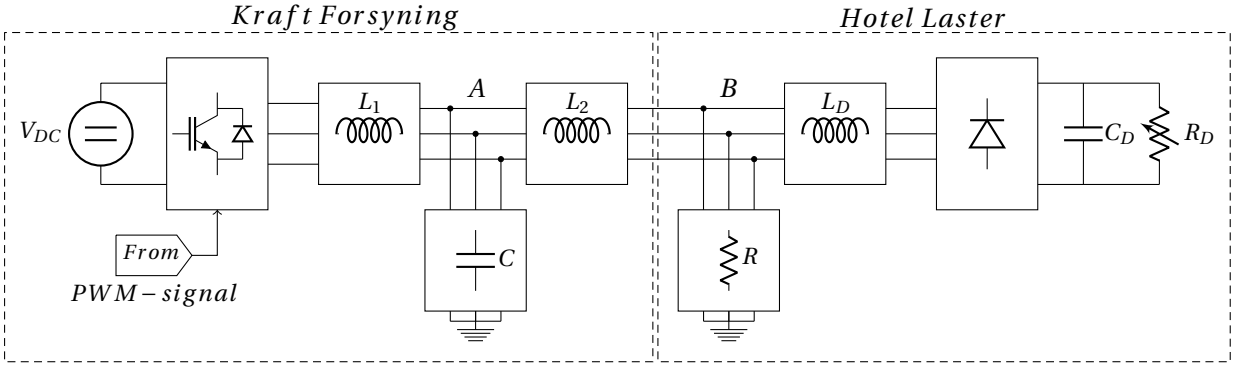


Figure 2: Systemet som vert studert i denne oppgåva.

Hovudformålet med denne masteroppgåva er å forsikre seg om at spenningssignalet i punkt B, sjå figur 2, held seg etter forskriftene rundt Total Harmonis Forvrenging (THD) gitt frå Det Norske Veritas (DNV). I dei gitte operasjonstilfella vil den maksimale THD-en overskride krava. Tiltak må difor iverksettast for å håndtere og senke dei harmoniske i punkt B til godkjente verdiar.

Eit aktivt filter integrert i kontrollen til den allereie eksisterande VSI-en, har vorte utvikla med det formål å håndtere den harmoniske forvrenginga. Tre forskjellige opperasjonstilfeller har vorte studert med forskjellig grad av aktive harmonisk filtrering. Det utviklede aktive filteret viser til gode eigenskapar angåande harmonisk filtrering, men det har ein kostnad i form av auka effekttap og aukande system-straumar. Tiltak blei satt i verk for å minske effekttapa og system-straumane. I tilfelle 2 vart eit minst mogeleg effekttap, medan ein på same tid opprettheld THD krava, utforska. I det siste tilfellet vart det foreslått ei løysing som både sikrar gode verdiar av THD samt reduserte effekttap og system-straumar. Det vart konkludert med at VSI-en i det gitte systemet er tilstrekkelig til å håndtere det harmoniske støyet som oppstår i systemet. Men resultata oppnådd er svært avhengig av parameterar brukte under simuleringane, det vert difor oppmoda til å finne meir nøyaktige systemverdiar for å sikre stabilitet og gode ytingar.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background and Motivation

A changing climate, caused by emission of greenhouse gasses, threatens future generations of the world. The combination of a growing world population and an overall higher standard of living causes the ship industry to constantly evolve. The International Maritime Organization predicts an increase of emissions caused by marine transport of 50% to 250% by 2050 [1]. Maritime transport emits around 2.5% of the global greenhouse gas emissions today. In order to reach the internationally agreed upon goal of a temperature increase below 2°C, the emissions should drastically be reduced from the values of today. Reducing the green house emissions calls for more efficient ships. Several studies have shown that an extensive electrification of ships using electric propulsion could lead to fuel savings [2–4].

In the marine and offshore business, there is an ongoing revolution thanks to energy storage systems. This is mainly due to the fast evolving battery technology, with lithium-ion proven to be capable of both high power and high energy densities. In addition, the power electronics needed to store and supply energy are getting steadily both cheaper and better. With the possibility to store energy, many opportunities for smarter power generation, distribution and consumption open up [5, 6]. Peak shaving, dynamic performance, strategic loading and pure battery drive are examples of ways to even out the operation pattern of the gensets and lower the operation time. In modern marine vessels, both propulsion systems and hotel loads are electrically powered. An electric power distribution system capable of high power transfer is therefore needed. The DC-distribution system is a novel concept which a lot of research is pointed towards [6–9]. The energy storage revolution causes a trend shift within power distribution systems towards the DC-distribution. The DC-distribution system makes the implementation of energy storage easier. It also has benefits when it comes to supplying loads through Variable Frequency Drives (VFD). These, among others, are two aspects that in the end will initiate fuel savings. The first ships with DC-grids have already been produced, and fuel savings up to 27% have been reported for certain operation modes [6].

A typical VFD is composed by a front-end diode rectifier extracting a characteristic current with a substantial amount of harmonics [10]. It is therefore important to be able to cope with those harmonics and prevent harmonic propagation to the rest of the system. In diesel-electric ship power systems, the main contributor to harmonic distortion are the diode rectifier stages in VFDs [11].

Problem Formulation

A general ship integrated power system is presented in Figure 1.1 [6, 9, 12]. The system contains diesel generators supplying a DC-busbar. In order to sustain mobility during fault, the system is divided in two by a fast DC-breaker [12, 13]. The half containing the fault is disconnected; since each half has at least one electric propulsion unit, the ship maintains its mobility. Optionally, a battery bank capable of utilizing different kinds of services, depending on battery size and system controllability and flexibility, is connected to the DC-busbar [5, 6]. This thesis directs its focus towards the power supply of hotel loads. This power supply is directly connected to the DC-busbar, see the focus area in Figure 1.1. The power supply consists of a Voltage Source Inverter (VSI) and a LCL-filter. The system of focus is presented more in detail in Figure 1.2. The hotel loads are composed of an ohmic load R and a non-linear load. The non-linear load consists of a diode rectifier supplying an adjustable resistance R_D. Attached to the diode rectifier is an AC-side smoothing inductor L_D and a DC-side smoothing capacitor C_D. The non-linear load represents the loads driven by VFDs onboard marine vessels.

In modern marine vessels, hotel loads often amounts to 10% - 20%, and sometimes more than 20%, of the installed power onboard [14]. It is important to design, both in terms of components and control, a power supply capable of supplying the hotel loads present onboard the ship. The main challenge is related to the non-linear hotel load, which causes harmonic distortion in the system. The considered test case, provided by Siemens in Trondheim, has a non-linear power consumption P_D in the range of 30% to 70% of the nominal apparent power (Sn = 1.8MW). The ohmic hotel load operates with a power consumption P_R from 0% to 20% of Sn. The aim is to be able to control the voltage at point B, see Figure 1.2, in such a way that the ohmic load represented by R is exposed to a voltage waveform within certain requirements. The offshore standard regarding electrical installations sets an upper limit of 8% Total Harmonic Distortion (THD), with a maximum contribution per harmonic order of 5% [15]. The systems components are given and fixed, with the exception of the LCL-filter capacitor. This capacitor should be chosen for the best possible performance with regard to power losses and the capability for harmonic mitigation. To sum up, the main task is to overcome the THD requirements by using the active filter capability of the already existing VSI. The active harmonic filter integrated in the control of the VSI is called the Integrated Active Filter (IAF). There are also some constrains upon available measurements. One is only allowed to measure the voltage at point A, the capacitor current i_C and the inverter current i_1, see Figure 1.2. Measuring the voltage at point B, as well as the hotel load currents i_{L_D} and i_R, is not allowed.

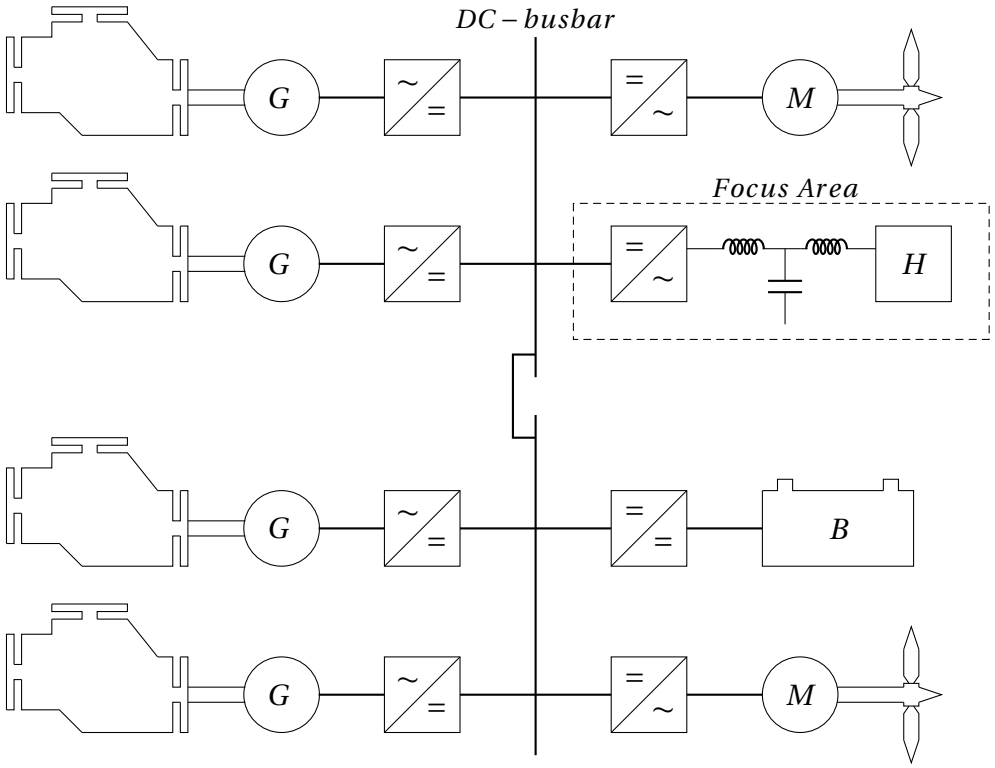


Figure 1.1: Ship integrated power system with DC-distribution.

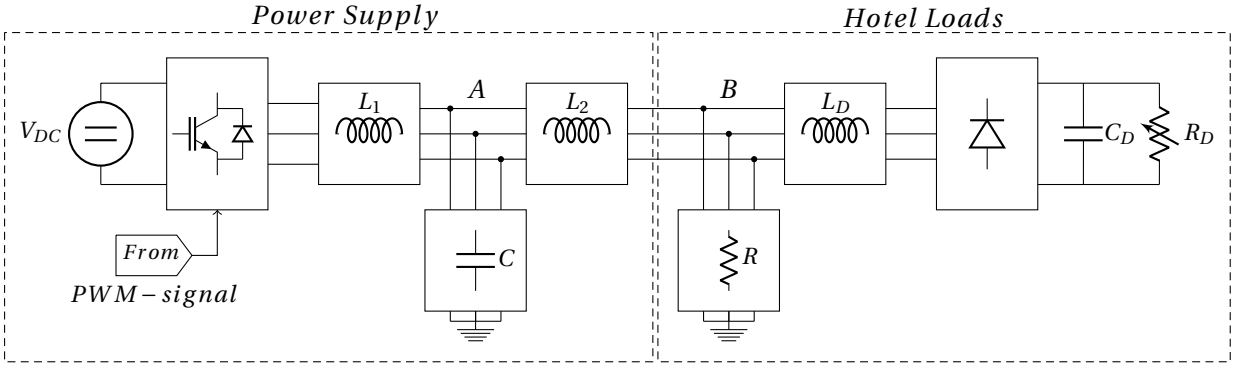


Figure 1.2: The system investigated in this thesis.

1.2 Objectives

The main objectives of this thesis are listed in the following:

1. Investigate system properties with consideration of harmonic frequencies and LCL-filter capacitor sizes.
2. Develop a cascaded control of the VSI capable of controlling the fundamental voltage component at point B.
3. Investigate the Total Harmonic Distortion at point B for representative power consumptions.
4. Develop an original VSI Integrated Active Filter with the purpose of reducing the harmonics at point B to magnitudes fulfilling the requirements.
5. Develop an original Matlab Simulink model to perform case studies; highlighting the possible IAF operation modes and identify the most suitable active filter control strategy.
6. Investigate the effects of harmonic mitigation in terms of increased power losses and component current ratings.

1.3 Outline of Master Thesis

The following section explains the sequence of the contents and how the chapters are connected together.

The thesis starts off with a detailed description of the system investigated in chapter 2. This chapter contains information about the nominal operation of the systems, as well as information of the given components. Chapter 3 concerns mainly the modelling and control of the VSI. Since we are dealing with harmonics in the system, the VSIs switching-induced harmonics are investigated. Characteristics of the passive LCL-filter, mainly used to cancel the switching induced harmonics, are also looked into. In chapter 4, a state-space representation of the system is developed with the purpose of investigating system properties. The input-to-output sensitivity is investigated in terms of frequency and the LCL-filter capacitor size.

In chapter 5, the harmonic distortion at point B is investigated in terms of ohmic power consumption P_R and distorted power consumption P_D. chapter 6 discloses various types of Active Power Filters (APF) able to mitigate the harmonic distortion previously investigated. The idea behind the applied IAF is discussed in the end of this chapter.

In chapter 7, the VSI integrated active filter based on the selective harmonic mitigation method [16] is developed. Finally, in chapter 8, three different cases are simulated utilizing the developed IAF. This chapter includes a proposal for an original trade-off active filtering solution. A discussion in the end sums up the main findings.

1.4 Relation to Specialization Project

The author wrote a specialization project report the fall of 2016 [5]. It was titled "Investigation of Harmonic Distortion in Marine Power Systems". Some material in this thesis is based on the work done in the spec. project. This includes the following sections:

* Section 3.3: VSC-attached Passive Fillters.
* Section 3.4: Control of the VSC.
* Section 5.2: Investigation of Harmonic Distortion.

Note that the contents of the above mentioned sections are strongly rewritten and shortened. The experience brought from the spec. project has however been vital to the progression of this thesis.

Chapter 2

Detailed Description of the System

A thorough description of the investigated system is given in this chapter. The Per Unit (pu) system will be introduced, and the system quantities are transferred into the pu-system. A figure of the power supply connected to the hotel loads was shown in the introduction, see Figure 1.2.

2.1 System Values

Siemens AS in Trondheim has provided the system values used in this thesis, see Table 2.1. The subscript n denotes nominal values. It is important to notice that the size of the capacitor is fully selectable, but finding the best capacitor size is a rather complex task. The determination of the capacitance is a compromise between the ability of the power supply to compensate for harmonics and the cancellation of switching induced harmonics from the inverter. This is further discussed in the sections 3.3 and 4.3. The DC-side adjustable resistance R_D and the capacitance C_D are also not given; they are further discussed in chapter 5.1.

Inverter Switching Frequency	f_{sw}	$2000Hz$
DC-link Voltage	v_{DC}	$1350V$
AC-side nominal Line to Line Voltage	v_n	$690V$
AC-side nominal Phase Current	i_n	$1500A$
AC-side Frequency	f	$60Hz$
Filter Inductances	L_1, L_2	$49.3\mu H$
Commutation Inductance	L_D	$14.1\mu H$
Internal Resistance in L_1,L_2,L_D,C	R_{L1},R_{L2},R_C,R_{L_D}	$2.66m\Omega$

Table 2.1: System values.

Using the given values from Table 2.1, the nominal apparent power (S_n) becomes:

$$S_n = \sqrt{3} v_n i_n = 1.793MVA \tag{2.1}$$

2.1.1 The Per Unit System

To get a more general control system, the control is developed in the pu system. The pu system is defined with the following base quantities:

$$V_b = \frac{\sqrt{2}}{\sqrt{3}} v_n,\ I_b = \sqrt{2} i_n,\ Z_b = \frac{V_b}{I_b},\ S_b = \frac{3}{2} V_b I_b. \tag{2.2}$$

Here v_n is the AC-side line-to-line voltage and i_n is the line current. Further, Z_b can also be written as:

$$Z_b = \omega_b L_b, \longrightarrow L_b = \frac{Z_b}{\omega_b} \tag{2.3a}$$

$$Z_b = \frac{1}{\omega_b C_b}, \longrightarrow C_b = \frac{1}{Z_b \omega_b} \tag{2.3b}$$

The base values can now be calculated, see Table 2.2. These values are further used in the development of the VSI control.

V_b	$563.4 \frac{V}{pu}$
I_b	$2121.3 \frac{A}{pu}$
Z_b	$0.2656 \frac{\Omega}{pu}$
ω_b	$377.0 \frac{rad}{s \times pu}$
L_b	$7.04 \times 10^{-4} \frac{H}{pu}$
C_b	$0.010 \frac{F}{pu}$

Table 2.2: System base values.

2.1.2 Per Unit System Values

Transferring system values into the pu system results in the following values:

$L_{1_{pu}}, L_{2_{pu}}$	7%
$L_{D_{pu}}$	2%
$R_{L1_{pu}}, R_{L2_{pu}}, R_{C_{pu}}, R_{L_{D_{pu}}}$	1%
ω_{pu}	100%

Table 2.3: System values in pu.

Chapter 3

Modelling and Control of the VSC

3.1 Modelling

A diagram of a two-level Voltage Source Converter (VSC) is shown in Figure 3.1. The voltages v^a, v^b and v^c are the AC-side phase voltages and v_{DC} is the DC-side voltage. The semiconductor switches, in this case IGBTs, are connected with anti-parallel diodes. The most common configuration of the VSC is the two-level converter, where the magnitude of the output voltage is either zero or v_{DC}. The optional multilevel converter builds up the voltage in smaller steps than the two-level VSC and thus decreases the harmonics of the output waveform. This is however not of interest, since we are using the two level converter in our system.

The VSC can be modelled in detail with blanking time, snubber circuits and semiconductors switches, or in a simplified way using an average model, see Figure 3.2. The characteristics of the semiconductor switches are of great importance in this master thesis, as we are dealing with harmonics in the system, hence, the detailed model is used. The VSCs in general will produce harmonics around its switching frequency; this is further investigated in section 3.2. A passive filter connected to the terminals is therefore necessary to be able to cancel the switching-induced harmonics; this is looked into in section 3.3.

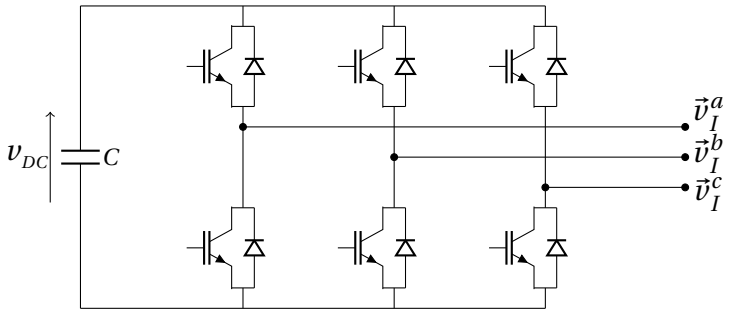


Figure 3.1: Voltage Source Converter.

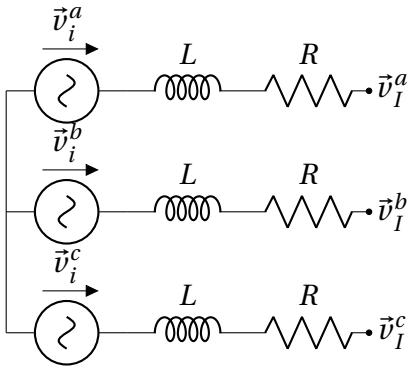


Figure 3.2: Average model.

3.2 Pulse Width Modulation

There are different methods to modulate the signal to the semiconductor switches. Here, pulse width modulation (PWM) is used, which is a carrier-based modulation technique where each phase voltage is controlled independently [17]. Figure 3.3 shows the PWM of a sinusoidal waveform at a switching frequency of 2kHz. With a DC-voltage of 1pu, the typical AC-voltage modulated has a peak value of 0.8pu. The triangular waveform is used in the PWM to modulate the signal. If the value of the triangular waveform is higher than the sinusoidal waveform, the PWM output is set to zero. If it is lower, the PWM output is set to one.

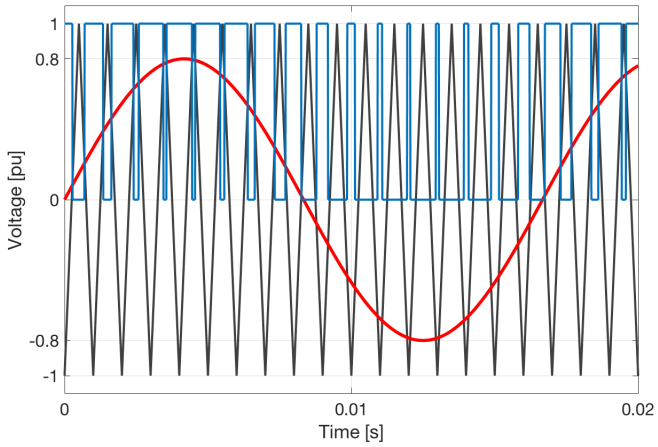


Figure 3.3: PWM of a sinusoidal waveform.

As previously mentioned, the harmonics caused by the PWM is of importance, and the line-to-line voltage v_{LL} should contain a minimum of harmonics. Figure 3.4 shows the inverter output line-to-line voltage when a sinusoidal waveform is produced. The sinusoidal waveform is then extracted from the PWM voltage by the use of filters. The characteristic PWM voltage before filtering gives the

frequency spectrum presented in Figure 3.5. From the figure, it can be seen that the harmonic content around the switching frequency is the main concern. The switching frequency is around the 33th order but, as seen from the FFT plot, the harmonics start to build up around the 30th order, i.e. 1.8kHz. A filter is necessary to get rid of these higher-order harmonics.

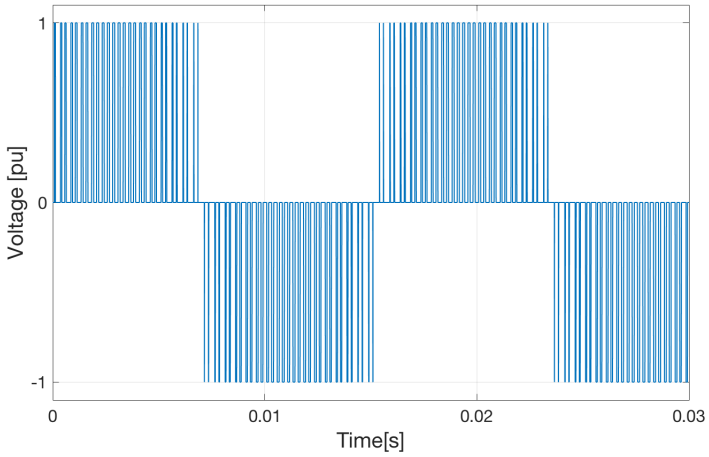


Figure 3.4: Inverter output, line to line sinusoidal waveform.

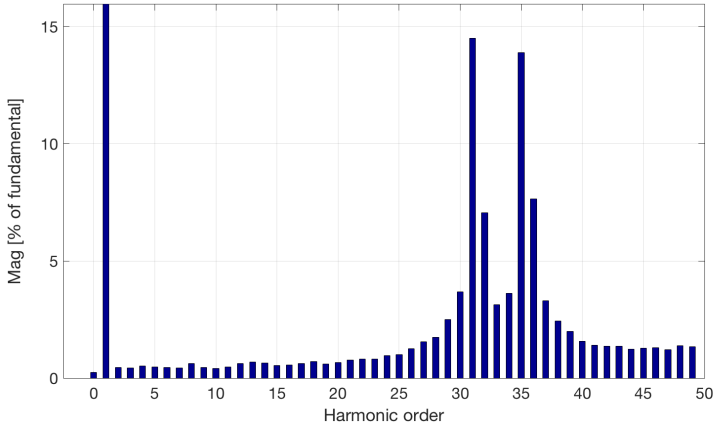


Figure 3.5: FFT of inverter output.

3.3 VSC-attached Passive Filters

Producing an AC waveform with a VSC induces harmonics in the system. Usually, a capacitor is put on the DC-side of the VSC to keep the voltage stable and within certain limitations. The AC-side of the VSC usually has a higher-order filter. The classical LCL-filter is commonly used in such applications. This is a low-pass filter which cancels out the higher-order harmonics. The LC-filter,

the LCLCL-filter and the C-type-filter are other examples of filters which could have been used in this application.

3.3.1 The LCL-filter

As mentioned in the introduction, the inductors L_1 and L_2, together with the capacitor C, form a LCL-filter, see Figure 1.2. The equivalent single phase diagram of the LCL-filter is shown in Figure 3.6. The resistances R_{L1}, R_{L2} and R_C are the internal resistances in the inductors L_1 and L_2, and the capacitor C.

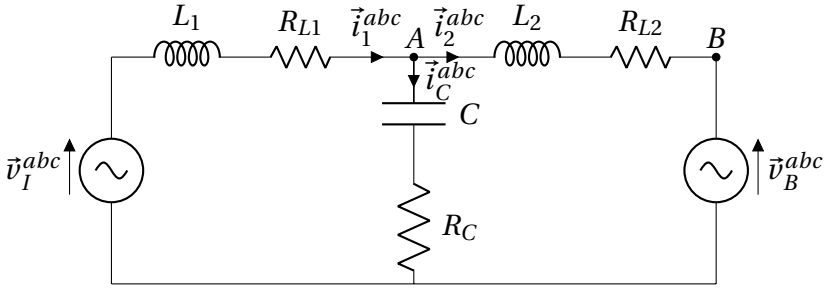


Figure 3.6: LCL-filter.

From the equivalent circuit, the transfer function $Y_{LCL}(s)$ can be found:

$$Y_{LCL}(s) = \frac{\vec{i}_2^{abc}(s)}{\vec{v}_I^{abc}(s)} = \frac{sR_CC+1}{sL_1L_2C\left(s^2+s\left(\frac{1}{L_1}(R_1+R_C)+\frac{1}{L_2}(R_2+R_C)\right)+\omega_{res}^2\right)+R_1+R_2} \tag{3.1}$$

$$\omega_{res} = \sqrt{\frac{1}{L_1C}+\frac{1}{L_2C}+\frac{1}{L_1L_2}\left(R_1R_2+R_1R_C+R_2R_C\right)} \tag{3.2}$$

The capacitor value is chosen such that the noise caused by the inverter around its switching frequency (f_{sw}) is cancelled. It is therefore important that the resonance frequency of the LCL-filter (f_{res}) is lower than the switching frequency of the inverter. The rule of thumb, when dealing with a relatively low switching frequency of 2kHz, is to set $f_{res} = \frac{1}{5}f_{sw}$. From the transfer function $Y_{LCL}(s)$, given in equation 3.1, the capacitance can be calculated as:

$$C = \left(\frac{1}{L_1}+\frac{1}{L_2}\right)\left(\frac{1}{\omega_{res}^2-\frac{1}{L_1L_2}\left(R_1R_2+R_1R_C+R_2R_C\right)}\right) \tag{3.3}$$

Calculating $f_{res} = \frac{1}{5}f_{sw}$ and inserting it into equation 3.3, the capacitance is found:

$$C = 6.4mF = 0.643pu \tag{3.4}$$

The bode plot of $Y_{LCL}(s)$ with the calculated capacitance is shown in Figure 3.7. The bode plot

shows that any disturbances caused by the inverter around f_{sw} = 2kHz are highly damped. The characteristics of the LCL-filter are more thoroughly explained in [5].

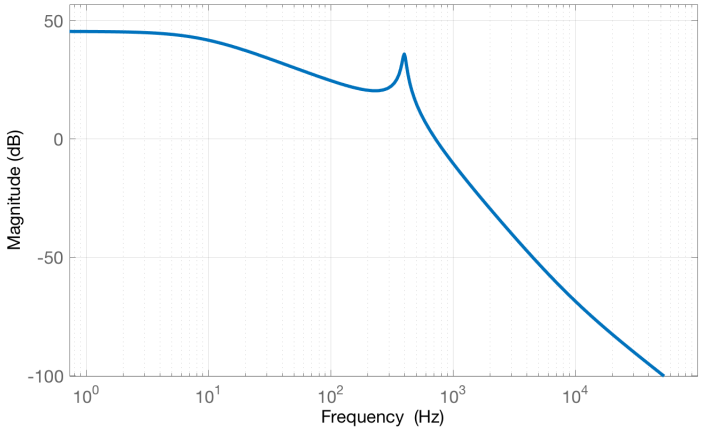


Figure 3.7: The LCL-filter bode plot.

3.4 Control of the VSC

A cascaded control based on Proportional-Integral (PI) regulators is used to control the voltage in the system. In order to make these regulators work properly, the control needs to be done with stationary values. By use of the Park transformation, one is able to transform the time-varying sinusoidal currents and voltages into stationary values. The amplitude-invariant Park transform is used for the transformation; it can be viewed in appendix B. The cascaded control structure of the VSI consists of an Inner Current Control (ICC) and an Outer Voltage Control (OVC).

3.4.1 Inner Current Control

The purpose of the ICC is to be able to control the current through the inductor L_1, known as the inverter current i_1. The equations for the ICC can be found by looking at the equivalent circuit shown in Figure 3.8. Here $\vec{v}_I^{abc}$ is the voltage supplied from the inverter, R_{L_1} is the internal resistance of L_1 and $\vec{v}_A^{abc}$ is the voltage at point A.

From Figure 3.8, the following equation can be drawn:

$$\vec{v}_I^{abc} - \vec{v}_A^{abc} = L_1 \frac{d\vec{i}_1^{abc}}{dt} + R_{L_1} \vec{i}_1^{abc} \tag{3.5}$$

By use of the Park transformation, equation 3.5 is transformed into the rotating reference frame, also known as dq-coordinates. In addition, for a more general control, the equation is transformed

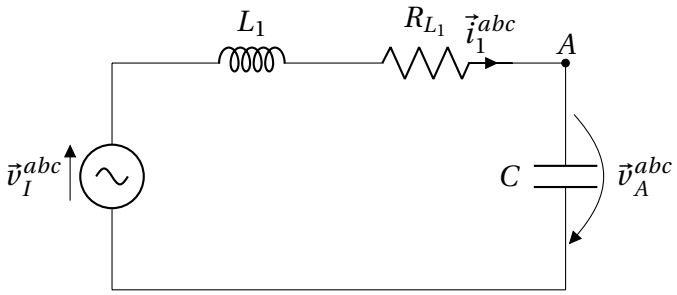


Figure 3.8: Inner Current Control equivalent circuit.

into the pu-system, see the equations 3.6. For a better explanation of the procedure see [5].

$$\frac{L_{1_{pu}}}{\omega_b}\frac{d\vec{i}^{\,d}_{1_{pu}}}{dt} = -R_{L_{1_{pu}}}\vec{i}^{\,d}_{1_{pu}} + \vec{v}^{\,d}_{I_{pu}} - \vec{v}^{\,d}_{A_{pu}} + \omega_{pu}L_{1_{pu}}\vec{i}^{\,q}_{1_{pu}} \tag{3.6a}$$

$$\frac{L_{1_{pu}}}{\omega_b}\frac{d\vec{i}^{\,q}_{1_{pu}}}{dt} = -R_{L_{1_{pu}}}\vec{i}^{\,q}_{1_{pu}} + \vec{v}^{\,q}_{I_{pu}} - \vec{v}^{\,q}_{A_{pu}} - \omega_{pu}L_{1_{pu}}\vec{i}^{\,d}_{1_{pu}} \tag{3.6b}$$

From these equations the ICC block diagram is developed, see Figure 3.9. In order to make the d- and q-components in the equations 3.6 independent of each other, the parts $\omega L_1 \vec{i}_1^{\,q}$ and $\omega L_1 \vec{i}_1^{\,d}$ are decoupled. $\vec{v}_M^{\,dq}$ is the signal going to the inverter modulator, the inverter then produces the inverter voltage $\vec{v}_I^{\,dq}$. The time delay T_e represents the delay occurring from the modulator and the inverter.

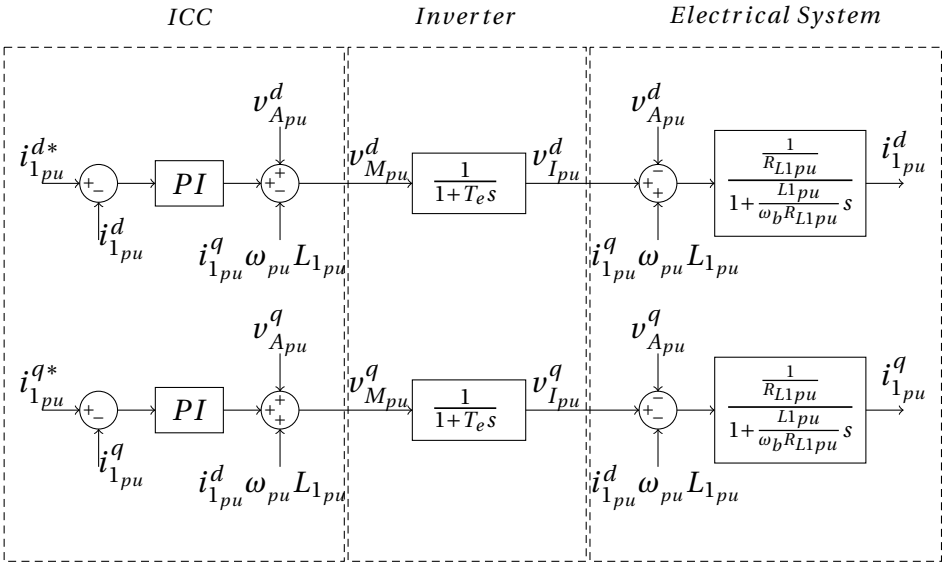


Figure 3.9: Block diagram of the Inner Current Control.

3.4.2 Outer Voltage Control

By including the nature of the capacitor, the OVC can be developed. The new equivalent circuit becomes:

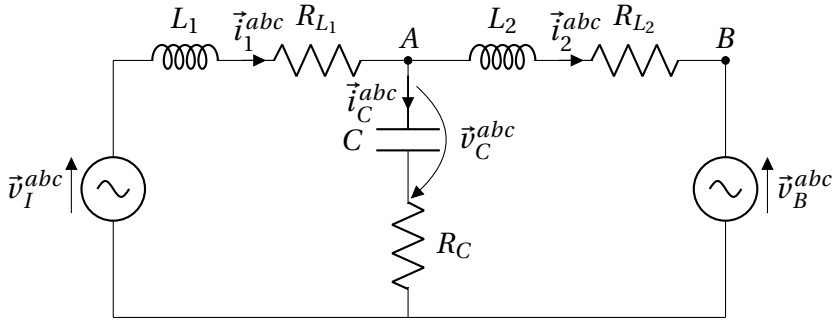


Figure 3.10: Outer voltage control equivalent circuit.

From the equivalent circuit, the following equations can be drawn:

$$\vec{v}_I^{abc} = L\frac{d\vec{i}_1^{abc}}{dt} + R_{L_1}\vec{i}_1^{abc} + \vec{v}_C^{abc} + R_C\vec{i}_C^{abc} \tag{3.7a}$$

$$\vec{i}_1^{abc} = \vec{i}_2^{abc} + \vec{i}_C^{abc} \tag{3.7b}$$

$$\vec{i}_C^{abc} = C\frac{d\vec{v}_C^{abc}}{dt} \tag{3.7c}$$

Ignoring the resistances R_{L_1} and R_C results in $\vec{v}_C^{abc} = \vec{v}_A^{abc}$. By transforming the equations 3.7 into dq-coordinates and into pu-values, the equations 3.8 are obtained. See reference [5] for a more thorough explanation of the procedure.

$$\frac{L_{1_{pu}}}{\omega_b}\frac{d\vec{i}_{1_{pu}}^{dq}}{dt} = \vec{v}_{I_{pu}}^{dq} - \vec{v}_{A_{pu}}^{dq} - j\omega_{pu}L\vec{i}_{1_{pu}}^{dq} \tag{3.8a}$$

$$\vec{i}_{C_{pu}}^{dq} = \vec{i}_{1_{pu}}^{dq} - \vec{i}_{2_{pu}}^{dq} \tag{3.8b}$$

$$\frac{C_{pu}}{\omega_b}\frac{d\vec{v}_{A_{pu}}^{dq}}{dt} = \vec{i}_{C_{pu}}^{dq} - j\omega_{pu}C_{pu}\vec{v}_{A_{pu}}^{dq} \tag{3.8c}$$

From these equations the block diagram of the OVC can be drawn, see Figure 3.11. As for the ICC, the d- and q-components are decoupled in the block diagram. T_{eq} represents the equivalent time delay for the ICC and the converter presented in Figure 3.9.

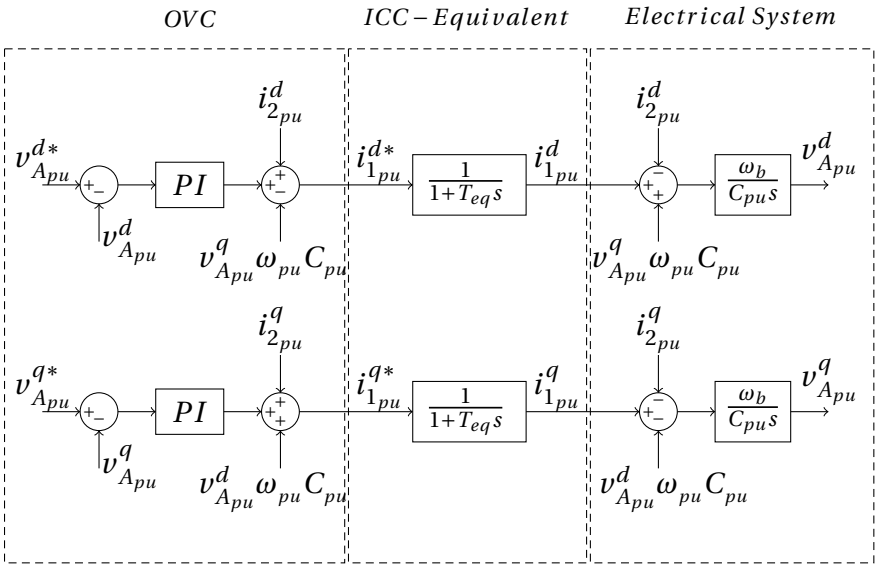


Figure 3.11: Block diagram of the Outer Voltage Control.

Chapter 4

Using a State Space Representation to investigate System Properties

In this chapter the state space representation is developed and verified. The state space representation is a mathematical model of the physical system, where inputs and outputs as well as state variables are related by first-order differential equations. The aim of the model development is to be able to analyze the system, looking at how the different frequencies penetrate the system. The model will be of particular use when investigating how the capacitor size influences the sensitivity of the system. This is investigated and discussed in section 4.3. As the diode rectifier has shown itself to be very difficult to model mathematically, the state-space representation has its limitations.

4.1 Model Development

The equivalent single-phase scheme of the system is shown in Figure 4.1.

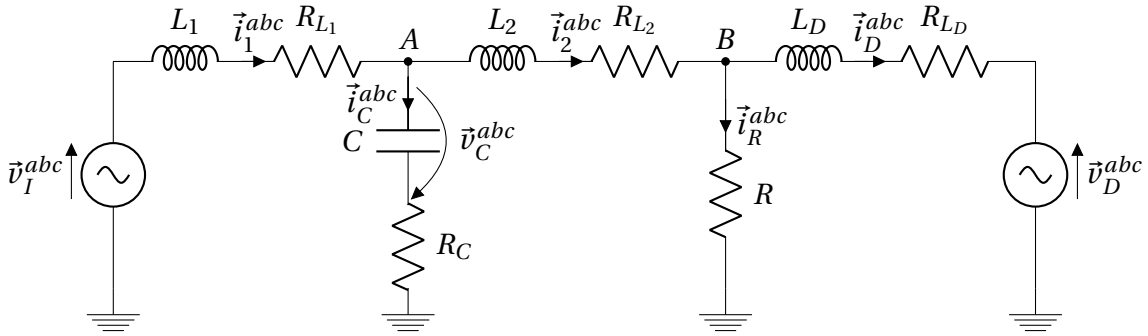


Figure 4.1: Equivalent single-phase scheme of the system.

Here $\vec{v}_I^{abc}$ is the voltage delivered from the VSI. The input $\vec{v}_D^{abc}$ is the voltage at the AC-terminals of the diode rectifier. L_D represents the smoothing reactor connected to the diode rectifier with an

internal resistance R_{L_D}. R is the ohmic load connected in parallel to the diode rectifier. The components L_1, L_2 and C, together with their corresponding internal resistances constitute the LCL-filter. The equivalent circuit contains four components capable of storing energy; L_1,C,L_2 and L_D. These components have a certain state at all times, therefore four state equations are developed for the state-space representation. It is worth mentioning that the system is modelled as a linear time-invariant system. Hence, the equations to be solved can be represented by a linear combination of the functions and variables represented in them. The fact that the system is time independent means that the components within it are ideal and not influenced by wear and tear, mode of operation or external conditions like temperature and humidity.

From the equivalent circuit, the equations for the state-space representation can be found. By use of Kirchhoff's laws, the following four equations are obtained:

$$L_1 \frac{d\vec{i}_1^{abc}(t)}{dt} = \vec{v}_I^{abc}(t) - R_{L_1}\vec{i}_1^{abc} - \vec{v}_C^{abc}(t) - R_C\big(\vec{i}_1^{abc}(t) - \vec{i}_2^{abc}(t)\big) \tag{4.1a}$$

$$C\frac{d\vec{v}_C^{abc}(t)}{dt} = \vec{i}_1^{abc}(t) - \vec{i}_2^{abc}(t) \tag{4.1b}$$

$$L_2 \frac{d\vec{i}_2(t)}{dt} = \vec{v}_C^{abc}(t) + R_C(\vec{i}_1(t) - \vec{i}_2(t)) - R_{L_2}\vec{i}_2(t) - R\big(\vec{i}_2(t) - \vec{i}_D(t)\big) \tag{4.1c}$$

$$L_D \frac{d\vec{i}_D(t)}{dt} = R\big(\vec{i}_2(t) - \vec{i}_D(t)\big) - R_{L_D}\vec{i}_D(t) - \vec{v}_D^{abc}(t) \tag{4.1d}$$

By use of the Park transformation, see appendix B, the state equations are transferred into a rotating reference frame. In addition, by letting the different states be denoted as $x_1(t) = \vec{i}_1(t)$, $x_2(t) = \vec{v}_C(t)$, $x_3(t) = \vec{i}_2(t)$ and $x_4(t) = \vec{i}_D(t)$, the following eight equations are obtained:

$$\dot{x}_1^d(t) = -\frac{R_{L_1}+R_C}{L_1}x_1^d(t) + \omega x_1^q(t) - \frac{1}{L_1}x_2^d(t) + \frac{R_C}{L_1}x_3^d(t) + \frac{1}{L_1}v_I^d(t) \tag{4.2a}$$

$$\dot{x}_1^q(t) = -\omega x_1^d(t) - \frac{R_{L_1}+R_C}{L_1}x_1^q(t) - \frac{1}{L_1}x_2^q(t) + \frac{R_C}{L_1}x_3^q(t) + \frac{1}{L_1}v_I^q(t) \tag{4.2b}$$

$$\dot{x}_2^d(t) = \frac{1}{C}x_1^d(t) + \omega x_2^q(t) - \frac{1}{C}x_3^d(t) \tag{4.2c}$$

$$\dot{x}_2^q(t) = \frac{1}{C}x_1^q(t) - \omega x_2^d(t) - \frac{1}{C}x_3^q(t) \tag{4.2d}$$

$$\dot{x}_3^d(t) = \frac{R_C}{L_2}x_1^d(t) + \frac{1}{L_2}x_2^d(t) - \frac{R_C+R_{L_2}+R}{L_2}x_3^d(t) + \omega x_3^q(t) + \frac{R}{L_2}x_4^d(t) \tag{4.2e}$$

$$\dot{x}_3^q(t) = \frac{R_C}{L_2}x_1^q(t) + \frac{1}{L_2}x_2^q(t) - \omega x_3^d(t) - \frac{R_C+R_{L_2}+R}{L_2}x_3^q(t) + \frac{R}{L_2}x_4^q(t) \tag{4.2f}$$

$$\dot{x}_4^d(t) = \frac{R}{L_D}x_3^d(t) - \frac{R+R_D}{L_D}x_4^d(t) + \omega x_4^q(t) - \frac{1}{L_D}v_D^d(t) \tag{4.2g}$$

$$\dot{x}_4^q(t) = \frac{R}{L_D} x_3^q(t) - \omega x_4^d(t) - \frac{R+R_D}{L_D} x_4^q(t) - \frac{1}{L_D} v_D^q(t) \tag{4.2h}$$

The equations 4.2 can be put into the general state space representation for linear systems. The general representation is on the following form [18]:

$$\dot{\vec{x}}(t) = A\vec{x}(t) + B\big(\vec{u}(t) + \vec{\omega}(t)\big) \tag{4.3a}$$

$$\vec{y}(t) = C\vec{x}(t) + D\vec{u}(t) \tag{4.3b}$$

Here A is the system matrix, B is the input matrix, C is the output matrix and D is the feedforward matrix. In this case, the D matrix is non-existent, since no feed forward takes place in the system. The vector $\vec{y}(t)$ is the output vector, $\vec{u}(t)$ is the control vector and $\vec{\omega}(t)$ is the disturbance vector. The control vector will consist of v_I^d and v_I^q, which are the controllable inverter voltages. The disturbance vector $\vec{\omega}(t)$ contains the diode rectifier voltages v_D^d and v_D^q, which are uncontrollable. From the equations 4.2, the following matrices are obtained:

$$A\vec{x}(t) = \begin{bmatrix} -\frac{R_C+R_{L_1}}{L_1} & \omega & -\frac{1}{L_1} & 0 & \frac{R_C}{L_1} & 0 & 0 & 0 \\ -\omega & -\frac{R_C+R_{L_1}}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{R_C}{L_1} & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \omega & -\frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & -\omega & 0 & 0 & -\frac{1}{C} & 0 & 0 \\ \frac{R_C}{L_2} & 0 & \frac{1}{L_2} & 0 & -\frac{R_C+R_{L_2}+R}{L_2} & \omega & \frac{R}{L_2} & 0 \\ 0 & \frac{R_C}{L_2} & 0 & \frac{1}{L_2} & -\omega & -\frac{R_C+R_{L_2}+R}{L_2} & 0 & \frac{R}{L_2} \\ 0 & 0 & 0 & 0 & \frac{R}{L_D} & 0 & -\frac{R+R_{L_D}}{L_D} & \omega \\ 0 & 0 & 0 & 0 & 0 & \frac{R}{L_D} & -\omega & -\frac{R+R_{L_D}}{L_D} \end{bmatrix} * \begin{bmatrix} x_1^d(t) \\ x_1^q(t) \\ x_2^d(t) \\ x_2^q(t) \\ x_3^d(t) \\ x_3^q(t) \\ x_4^d(t) \\ x_4^q(t) \end{bmatrix}$$

$$B\big(u(t)+\omega(t)\big) = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_D} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_D} \end{bmatrix} * \left(\begin{bmatrix} v_I^d(t) \\ v_I^q(t) \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ v_D^d(t) \\ v_D^q(t) \end{bmatrix} \right)$$

$$\vec{y}(t) = C\vec{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 \end{bmatrix} \vec{x}(t)$$

4.2 Model Verification

A simulation of the state-space representation was built in Matlab Simulink to verify the state-space model. By running the simulation of the system and inserting the voltage from the inverter $\vec{v}_I$ and the diode rectifier $\vec{v}_D$ into the mathematical state-space model, one can examine whether the different states are equal in both the physical and the mathematical model. If that is indeed the case, the mathematical model is correct and can be used to analyze the physical model. To be clear, the physical model is referred to as the model with actual components developed in Simulink, see Figure 4.2. The content of the mathematical state-space model block in Figure 4.2 is depicted in Figure 4.3. A screenshot of the Simulink model used to verify the state-space model can be viewed in appendix E.

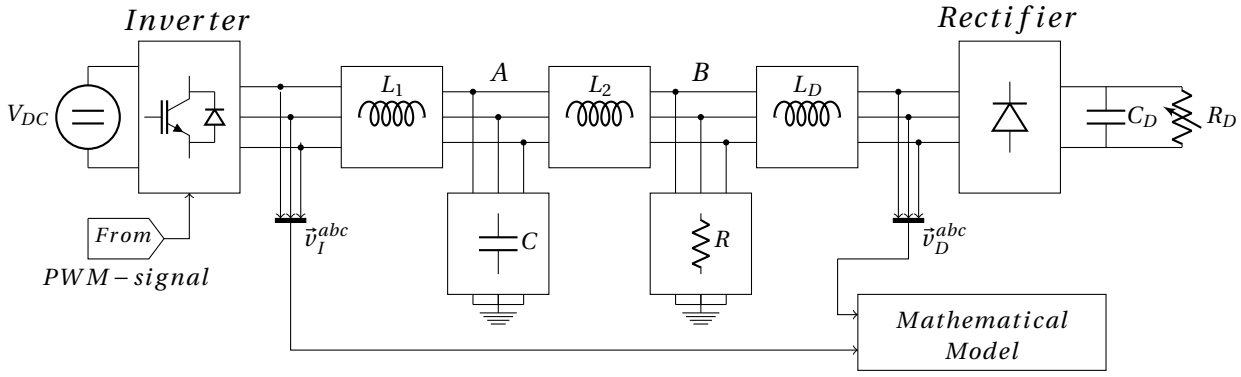


Figure 4.2: Model verification scheme.

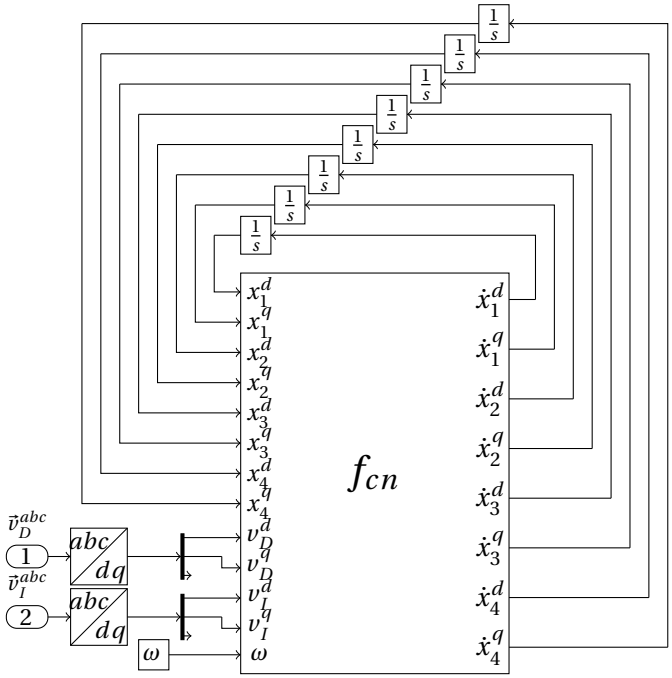


Figure 4.3: Mathematical model.

By measuring and comparing the different states in the mathematical and the physical model, the accuracy of the mathematical model is verified. Figure 4.4 shows the d-component of the capacitor voltage v_C^d with an extract in Figure 4.5. Figure 4.6 with an extract in Figure 4.6 compares the mathematical and the physical d-component of the inductor current i_2. Negligible differences are found when comparing the different models, which leads to the conclusion that the state-space model is correct.

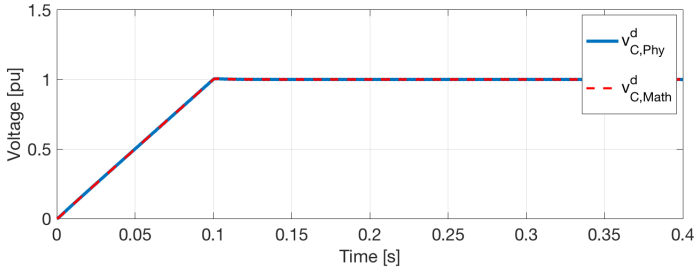


Figure 4.4: Comparing the physical and the mathematical capacitor voltage, $v^d_{C,Phy}$ vs $v^d_{C,Math}$.

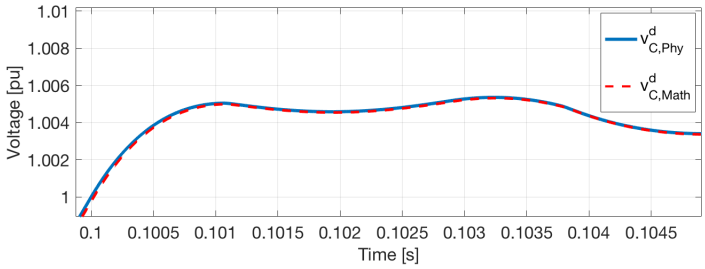


Figure 4.5: Extract from Figure 4.4.

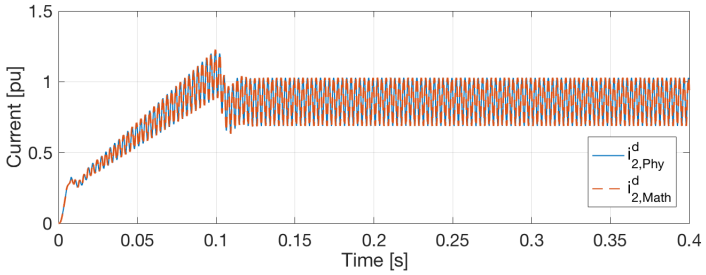


Figure 4.6: Comparing the physical and the mathematical inductor current, $i^d_{2,Phy}$ vs $i^d_{2,Math}$.

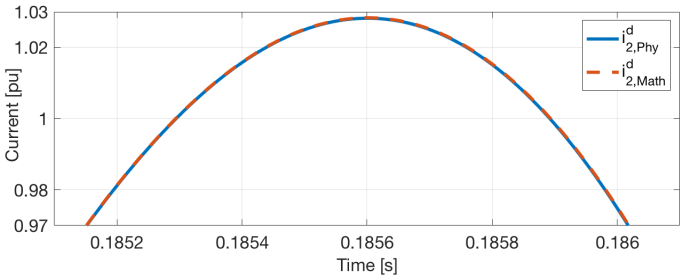


Figure 4.7: Extract from Figure 4.6.

4.2.1 Model limitations

The diode rectifier voltage $\vec{v}_D^{abc}$ is modelled as a disturbance. This is due to the comprehensive difficulties inherent in modelling the highly non-linear diode rectifier mathematically. In systems containing such components, one might need to linearize around an operation point, and the validity of the results is limited to the conditions close to that point. The state-space model and its benefits when it comes to investigating the system would have been more valuable if it was possible to model the diode rectifier properly. A more comprehensive system analysis could have been performed this way. If a suitable mathematical model could be found, the eigenvalues of the system

could have been readily found. Then, by use of pole placement, a stable system could be obtained while trying to cancel the different harmonics.

With the obtained state-space model one is, regardless of the model limitations, able to perform a sufficient sensitivity analysis of the system. The three-phase diode rectifier could be considered as single-phase, with conducting diodes or non-conducting diodes. When conducting diodes are present, the power supply sees a resistance R_D in parallel to the capacitance C_D. If one neglects the capacitance C_D, the system behaves like the resistance R_D is in series with the resistance R_{L_D}. By adding the resistance R_D to R_{L_D} in the state-space representation, a sufficient model of the conducting diode rectifier is obtained. When the diodes are non-conducting, the single- phase approximation looks like an open circuit after L_D. The input-to-output sensitivity will in this case be higher than with conducting diodes. For this reason, only the sensitivity with conducting diodes is investigated in the following.

4.3 Capacitor Influence on Stability and Sensitivity

In this section the system is investigated in terms of the capacitor size. Since the state-space model is found to be equal to the physical model within the above-mentioned limitations, it can be used to gather more information about the system and evaluate the system characteristics. An overview of how the voltage penetrates the system in terms of frequency is important when designing a control of an active filter. Evaluating the transfer function from the input vector $\vec{u}(t)$ to the output vector $\vec{y}(t)$ in a bode plot will show how the input effects the output.

The capacitor is the only component which we are allowed to design. The capacitor size will significantly influence the input-to-output sensitivity. How sensitive the system is to inputs is crucial to the performance of the active filter, which is implemented later. Because of the location of the capacitor in the system, the disturbance-to-output sensitivity is not considerably influenced by the relevant capacitor sizes. This sensitivity will not be considered when choosing the capacitor size, hence, a further investigation here is not of interest.

The AC-side capacitor design is of major importance when developing both the fundamental and the active filter control. In general, there are three aspects to consider when choosing the capacitor size. These are the capacitor current ratings, inverter switching frequency and resonance issues within the circuit. The LCL-filter was designed in chapter 3 based on the inverter switching frequency. As mentioned, the resonance frequency of the LCL-filter cannot be too close to the inverter switching frequency, as it will allow PWM switching noise to propagate through the system. The resonance frequency moves closer when decreasing the capacitor size and vice versa. See the bode plot of the LCL-filter 4.8 with varying capacitor values. In the Figure, it can be seen that a capacitor of 10mF gives a resonance frequency around 1kHz, which is half the switching frequency.

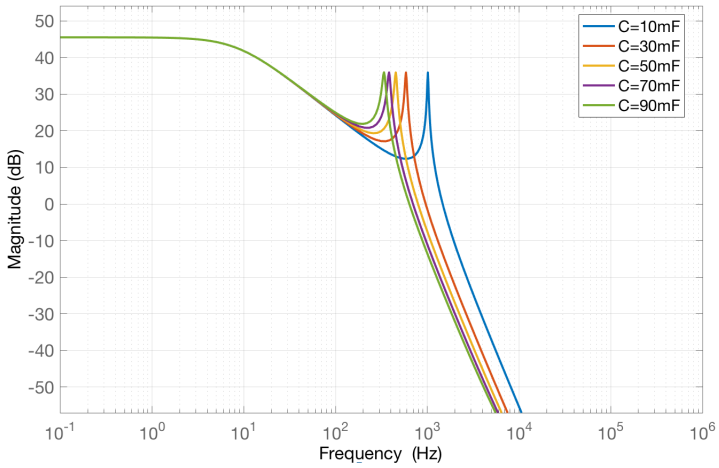


Figure 4.8: The LCL-filter bode plot for different capacitor sizes.

It is important to choose a capacitor that does not cause resonance in the system. Since the inverter will produce harmonic voltages to cope with harmonics in the system, the power supply should be able to handle the frequencies of the harmonics dealt with. The resonance phenomena will be discussed in chapter 6 when talking about passive filters. High harmonic currents are no problem for capacitors to handle, but inductors will develop high losses, and the possibility of component breakdown is present. The capacitor size also has a huge influence on the capacitor current, which can be seen by the classical relation: $i_C = C\frac{dv_C}{dt}$. Increasing the capacitor size will, in general, increase the current through the capacitor. With this in mind, a small capacitor is preferable, as the losses in the capacitor are proportional to the current squared. In general, an increased current in the capacitor also causes the current i_1 to increase.

4.3.1 Sensitivity Analysis

From the state space model, the transfer function is found by use of the following equation [18]:

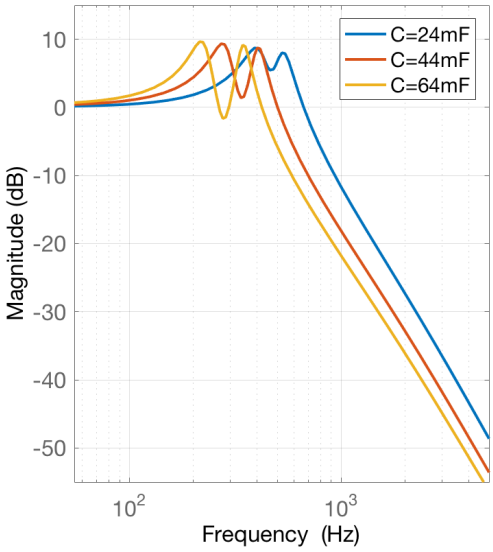
$$H(s) = C(sI - A)^{-1}B + D. \tag{4.4}$$

In Matlab, the calculations needed to find the transfer function from input to output are easily performed. The input is here referred to as the inverter voltage $\vec{v}_I$, and the output is the voltage $\vec{v}_B$, which yields $H(s) = \frac{\vec{v}_B}{\vec{v}_I}$. The plotted bode diagrams of the transfer function are shown in the Figures 4.9 and 4.10. Figure 4.9 represents the case with maximum power consumption and Figure 4.10 represents the minimum. These two different cases are obtained by including the resistance R_D. In the state-space model we let the resistance R_{L_D} be the sum of both R_{L_D} and R_D. As mentioned, the power consumption of the load is adjusted by the resistances R and R_D. By adjusting the resistances so that we represent the minimum and maximum power consumption, the presented bode diagrams are obtained. The different cases of power consumption display limited inequalities in

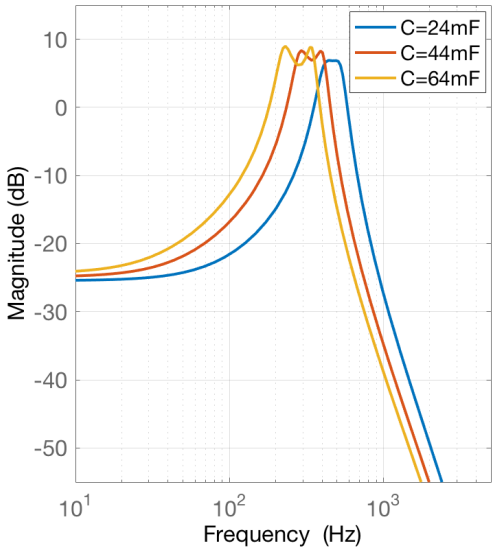
their bode plot. The inequalities are biggest around the resonance peaks, showing a higher resonant peak in the case of minimum power consumption.

Handling Harmonic Orders

Since the 5th harmonic is a negative sequence voltage, it will be transformed into a 6th harmonic, with the positive sequence park transformation at the fundamental frequency. The positive sequence 7th harmonic will also be transformed into the 6th harmonic in the same Park transformation. This is also the case with the 11th and the 13th order, where they both become the 12th harmonic. The bode diagrams are plotted for three different capacitances to show the sensitivity in relation to the capacitor size. From the figures, the same is observed as for the LCL-filter bode diagram, see Figure 4.8. The curves move to the right for smaller capacitances and vice versa. Moving the frequency response curve to the right makes it easier to filter higher- order harmonics, but the harmonics from the inverter switching at 2kHz start to become problematically close already at a capacitance of less than 50mF. Remembering that a switching frequency of 2kHz produces a substantial amount of noise with a frequency as low as 1.8kHz, see the frequency spectrum in Figure 3.5. In addition, a Park transformation is performed at the fundamental frequency, subtracting $60Hz$ from the 1.8kHz. The 17th and 19th order harmonics both become the 18th in dq-coordinates, which is 1080Hz. These harmonics, and even higher-order harmonics are notably hard to filter, as their frequency is too close to the inverter switching frequency. Hence, the active filter performing harmonic cancellation will be limited to the 5th,7th, 11th and the 13th order.

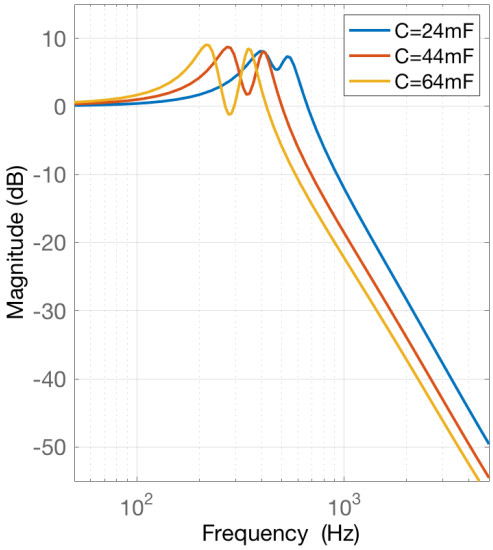


(a) d-component.

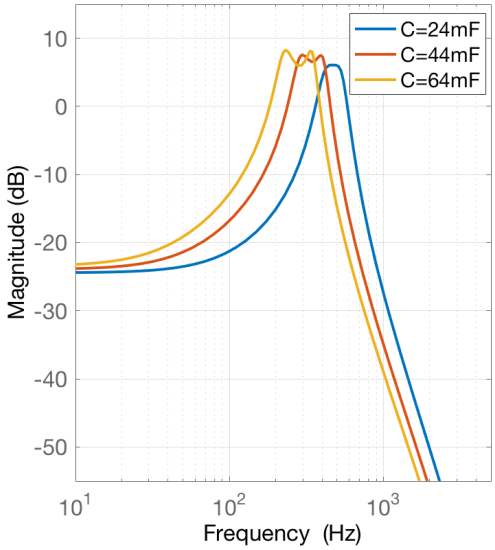


(b) q-component.

Figure 4.9: Bode diagram of $H(s) = \frac{\vec{v}_B}{\vec{v}_I}$ for maximum power consumption.



(a) d-component.



(b) q-component.

Figure 4.10: Bode diagram of $H(s) = \frac{\vec{v}_B}{\vec{v}_I}$ for minimum power consumption.

Chapter 5

Harmonic Distortion in the System

The voltage components causing harmonic distortion in the system are mainly caused by the non-linear and time-variant hotel load. This chapter begins with an introduction of the components within the hotel load. An investigation of the harmonic distortion at point *B* with regard to the Total Harmonic Distortion (THD) is performed in section 5.2. The concept of THD is further discussed in appendix F.1.

5.1 The Hotel Load

As mentioned in the introduction, hotel loads are loads that are not related to the propulsion system onboard ships, e.g. winches, lights or cranes. Here, both an ohmic load and a power electronic load are supplied, see Figure 1.2. The content of this section will mainly involve the distorting power electronic load.

In VFDs, the trend is to transfer power from AC to DC in an uncontrolled manner by use of cheap diode rectifiers [11, 17, 19]. A typical VFD is shown in Figure 5.1. The VFD consists of a smoothing reactor L_D, a diode rectifier, a smoothing capacitor C_D and a PWM-modulated inverter. The power consumption is controlled by the inverter in the VFD. In our case, the characteristics of the VFD inverter is not of importance and can therefore be simplified with an adjustable resistance R_D, as seen in Figure 5.2. This will decrease the simulation time and allows for an easier control of the power consumption.

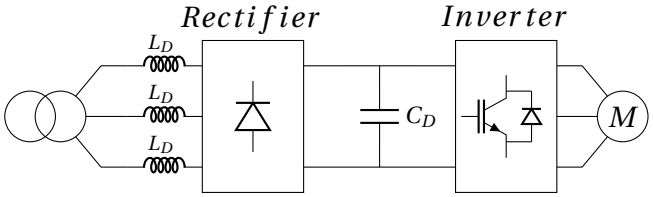


Figure 5.1: VFD.

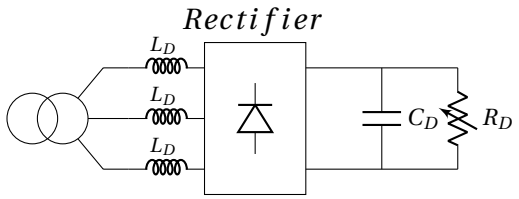


Figure 5.2: VFD equivalent circuit.

5.1.1 Three Phase Diode Rectifier Characteristics

The most common diode rectifiers are the 6- and the 12-pulse rectifiers. The 6-pulse rectifier produces harmonics of the following orders: 5th, 7th, 11th, 13th, 17th etc. It is important to mention that the 5th, 11th, 17th etc. are negative-sequence harmonics, which means that the b-phase voltage comes after the c-phase voltage. This phenomenon is important to have in mind when performing harmonic mitigation. The better performing 12-pulse rectifier produces only the 11th, 13th, 23th, 25th etc., cancelling out the side-bands of any odd multiple of 6 (5th, 7th, 17th, 19th etc.) [19]. The 6-pulse rectifier is both cheaper, lighter and less space-consuming than the 12-pulse rectifier, as it contains only half of the diodes. The 12-pulse rectifier also needs a special transformer with a secondary winding connected in delta-wye to get the harmonic cancellation as mentioned. These are all big disadvantages, considering that it will be located onboard marine vessels and not onshore. The topology of the 6-pulse rectifier compared to an example of the 12-pulse rectifier is shown in Figure 5.3 and 5.4.

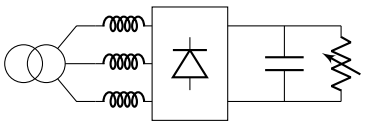


Figure 5.3: VFD equivalent based on the 6-pulse rectifier.

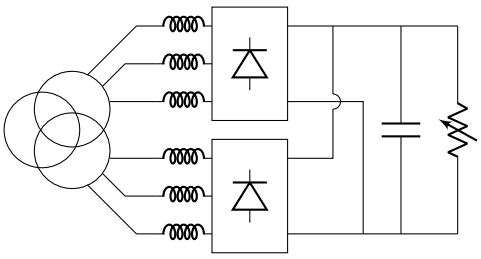


Figure 5.4: VFD equivalent based on the 12-pulse rectifier.

5.2 Investigation of Harmonic Distortion

To get a better understanding of the problem that we are dealing with, an investigation of the harmonic distortion is necessary. The control developed in chapter 3 is used to keep a sinusoidal voltage at point A with a magnitude of 1pu. Using the equivalent setup, shown in Figure 5.5, one can measure the harmonic distortion caused by the diode rectifier at point B.

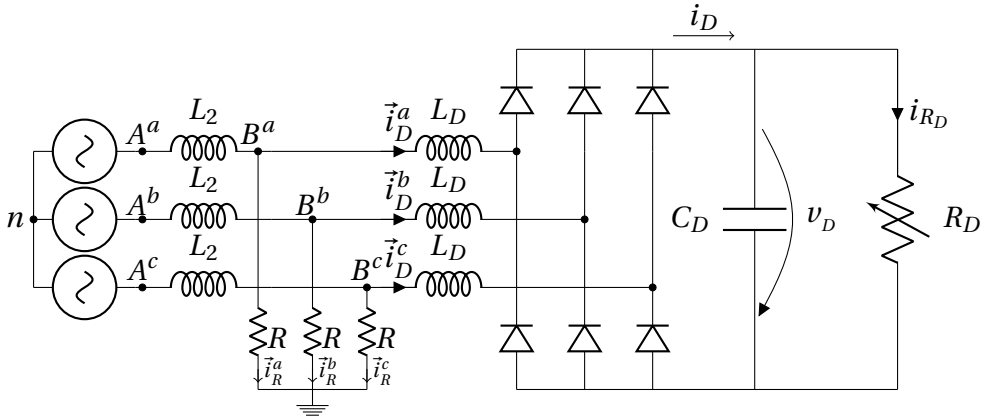


Figure 5.5: VFD equivalent circuit including L_2 and R.

The harmonic distortion varies with the power consumption. The distorted power consumption P_D is in the range of 30% to 70% of the nominal apparent power. Also, the ohmic power consumption P_R varies at point B, and it operates in the range from 0% to 20% of nominal apparent power. These power ratings are provided by Siemens in Trondheim. The value of the DC-side smoothing capacitance is found by simulation; setting a 2% DC-side voltage ripple results in $C_D = 17.5mF$. This capacitor size will be chosen differently when performing active filtering in the system; this is explained further in detail in chapter 8. The THD-levels for different power consumptions are presented in Table 5.1.

P_D [%ofS_n]	P_R [%ofS_n]				
	20%	15%	10%	5%	0%
70%	9.38%	9.45%	9.52%	9.60%	9.70%
60%	8.55%	8.62%	8.69%	8.76%	8.83%
50%	7.69%	7.75%	7.82%	7.88%	7.95%
40%	6.80%	6.85%	6.91%	6.96%	7.02%
30%	5.85%	5.90%	5.94%	5.99%	6.09%

Table 5.1: THD at point B with respect to P_D & P_R.

From the tabular 5.1, it can be seen that the highest THD level is present when the diode rectifier has its maximum power consumption P_D at 70% of Sn, and the ohmic load has its lowest power con-

sumption where P_R is zero. This condition, with a THD of 9.70%, gives the voltage waveform shown in Figure 5.6, with the corresponding frequency spectrum shown in Figure 5.7. As the maximum THD allowed by the DNV-standard [15] is 8% with a single harmonic contribution of maximum 5%, the THD is not within the requirements. The 5th harmonic contributes with roughly 7.5% in itself, and needs to be attenuated to fulfill the requirements.

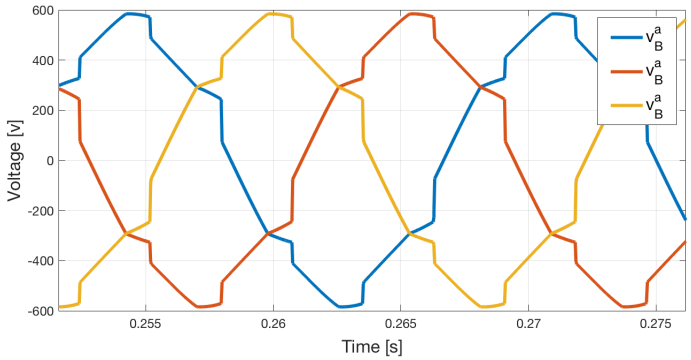


Figure 5.6: Voltage waveform of $\vec{v}_B^{abc}$ with $P_D = 70\%$ and $P_R = 0\%$ of Sn (THD=9.70%).

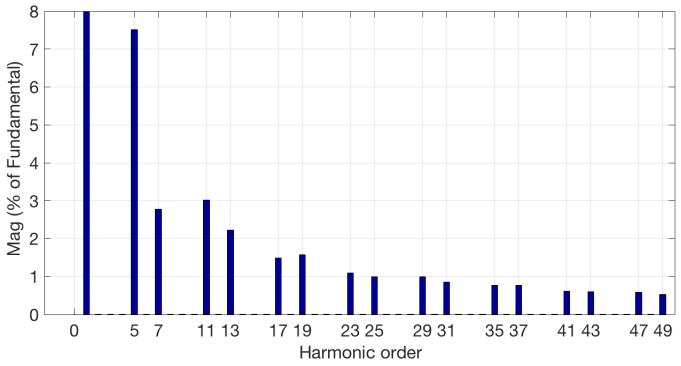


Figure 5.7: Frequency spectrum of $\vec{v}_B^{abc}$ at $P_D = 70\%$ and $P_R = 0\%$ of Sn (THD=9.70%).

The smallest THD-level appears when having a minimum distorted power consumption where $P_D = 30\%$, and a maximum ohmic power consumption where $P_R = 20\%$. The THD level is then 5.85%, as shown in Table 5.1. The resulting voltage waveform is shown in Figure 5.8, with its frequency spectrum shown in Figure 5.9. As the load R is purely ohmic, the current i_R has a waveform with the same characteristic look as the voltage waveform.

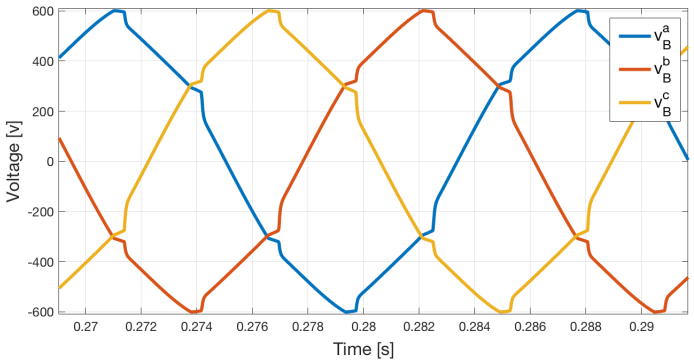


Figure 5.8: Voltage waveform of $\vec{v}_B^{abc}$ with $P_D = 30\%$ and $P_R = 20\%$ of Sn (THD=5.85%).

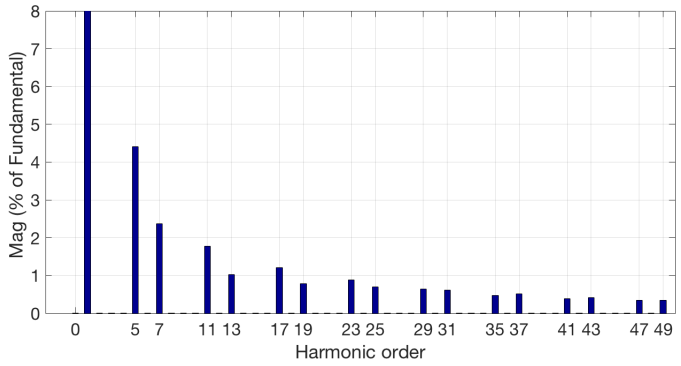


Figure 5.9: Frequency spectrum of $\vec{v}_B^{abc}$ at $P_D = 30\%$ and $P_R = 20\%$ of Sn (THD=5.85%).

Chapter 6

Mitigation Of Harmonic Distortion

The most widespread approach when mitigating harmonic distortion is to use passive filters [10]. Passive filters are usually tuned to absorb a given set of harmonics. If the harmonic spectrum changes, the passive filters have to be replaced or modified. Single-tuned filters are often installed to absorb the 5th, 7th, 11th and the 13th harmonic orders produced by the standard 6-pulse diode rectifier. It is wort mentioning that a single-tuned filter, by its nature, cannot ensure an equally good cancellation of the mentioned harmonics at the same time. However, single-tuned filters together with the 6-pulse diode rectifier is a cost-efficient solution in many applications. But passive filters have a tendency to interfere with the grid and can cause serious harmonic amplifications. This is due to the resonance phenomena which occurs when the resonance frequency is near a harmonic order [20]. Resonance can occur both in series with, or in parallel to the grid. It can come from changing system properties when inserting passive filters, see Figure 6.1. In the Figure, a standard series LC-filter, also known as a band-pass filter, is utilized. The resonance frequencies f_{series} and $f_{parallel}$ are given by the equations 6.1. Another drawback with passive filters is that, in order to get proper filtering, they should be connected at the point where the filtering is needed. This is not the case with Active Power Filters (APF), discussed in the following section. Although the passive filters only perform properly at the point of connection, they need to be oversized, as harmonics produced distant in the system will propagate and can find their way through the filter.

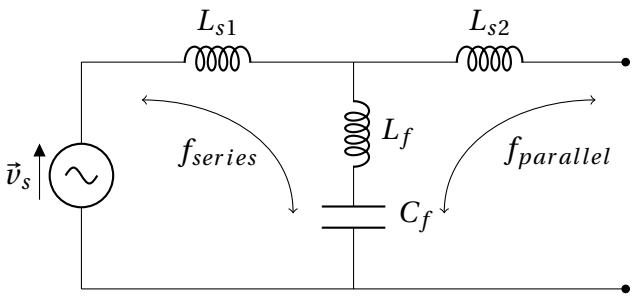


Figure 6.1: Series and parallel resonance.

$$f_{series} = \frac{1}{2\pi\sqrt{C_f(L_{s1}+L_f)}} \tag{6.1a}$$

$$f_{parallel} = \frac{1}{2\pi\sqrt{C_f(L_{s2}+L_f)}} \tag{6.1b}$$

6.1 Active Power Filters

Active Power Filters are a high-bandwidth switched power converter often based on pulse width modulated current injection [10, 19]. In this context is high bandwidth referred to as a combination of a low measurement sampling time and a quick response. APFs are most commonly used to cope with harmonics in low- to medium-voltage networks, and in high-voltage networks, they are utilized to perform voltage control and reactive compensation [21]. The voltage and current ratings of an APF are determined by the physical components within. The voltage rating is dependent on the available DC-voltage, and the current rating is dependent on the semiconductor devices, usually IGBTs with antiparallel diodes. The APFs can be connected both in series to or in parallel with the grid. Combinations of an active and a passive filter in different configurations are known as hybrid filters [22]. Investing in a APF is rather costly compared to the passive harmonic filters. On the other hand, the APFs can provide both harmonic and reactive compensation. It performs a faster regulation than the passive filters, and it avoids interactions with the grid. The fast regulation makes it more suitable for handling time variant loads compared to the passive filter solutions. Active filters can by control strategies be divided into broadband filters [23, 24] or selective harmonic filters [16]. The broadband type of filters handles a wide range of harmonic frequencies through the same controller. Selective harmonic filters on the other hand filter different harmonics through different controllers designed for a particular frequency.

6.1.1 Shunt Connected APF

Connecting an APF in parallel to the system, also known as a shunt connected filter, is the most common way of implementing an APF. The APF is normally connected to the bus where a filtered waveform is wanted. However, it is possible to connect a filter to a certain bus and decrease the harmonic content in the system as a whole, see [11]. Another way is to connect the APF at a certain point and try to filter a waveform somewhere distant. This can be beneficial if that distant point is undesirable for an APF connection. The shunt connected APFs are based on the harmonic current cancellation concept [25]. The harmonic current is measured, and from this measured current an opposing harmonic current is injected to wipe out the harmonics. The shunt connected filter topologies can be built from both VSIs and Current Source Inverters (CSIs), see Figure 6.2. VSIs are the preferred choice, as they are smaller in size, lower in cost, and additionally they can utilize a higher switching frequency with lower losses [21, 25]. APFs based on multilevel VSIs are also applicable in high power applications.

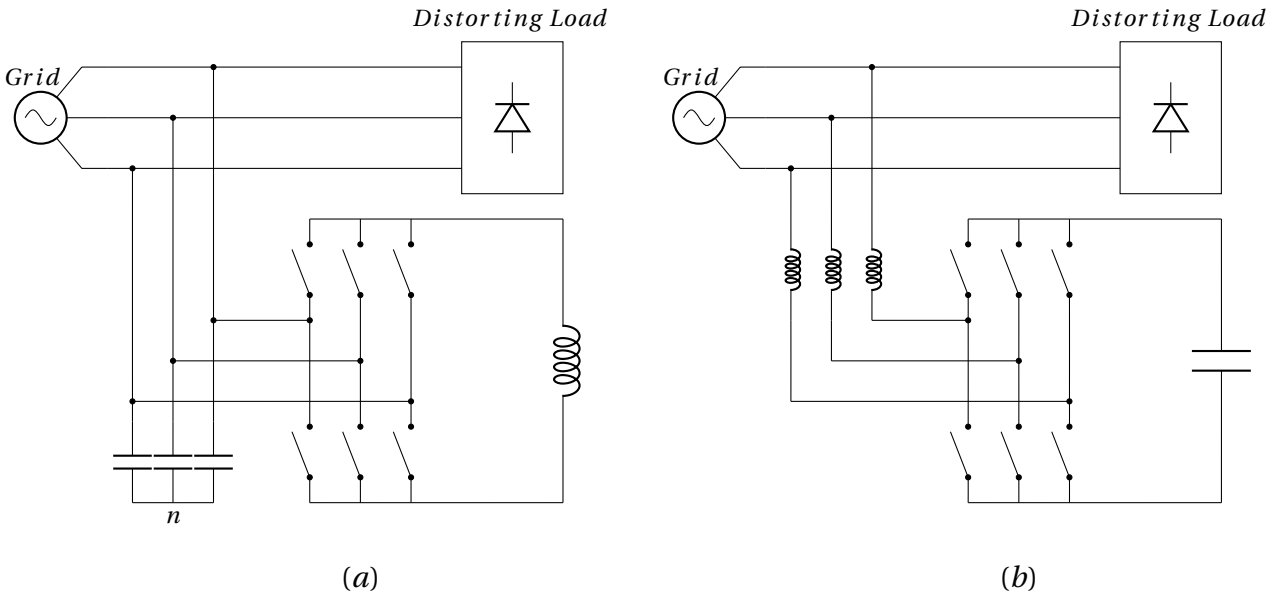


Figure 6.2: Shunt connected APFs, (a) is a CSI, (b) is a VSI.

6.1.2 Series Connected APF

Series connected APFs are based on the harmonic voltage cancellation concept [21, 25]. The series APFs produces a PWM voltage waveform, which is added or subtracted to ideally obtain a pure sinusoidal waveform in the grid. Series active filters are most often connected to the grid by a connection transformer [26], see Figure 6.3. Because of the previously mentioned drawbacks compared to the parallel connected APFs, the series connected APFs are less common in industry. The series APFs have to handle high load currents; this increases the current rating compared to the parallel connected APFs, which again increases losses and the physical size of the filter. It now seems like the series connected APFs only has drawbacks compared to the parallel ones. In fact, there are some benefits with series- connected filters. A series APF has advantages when it comes to eliminating the voltage-waveform harmonics and balancing three-phase voltages. This is beneficial when supplying voltage-sensitive equipment and devices.

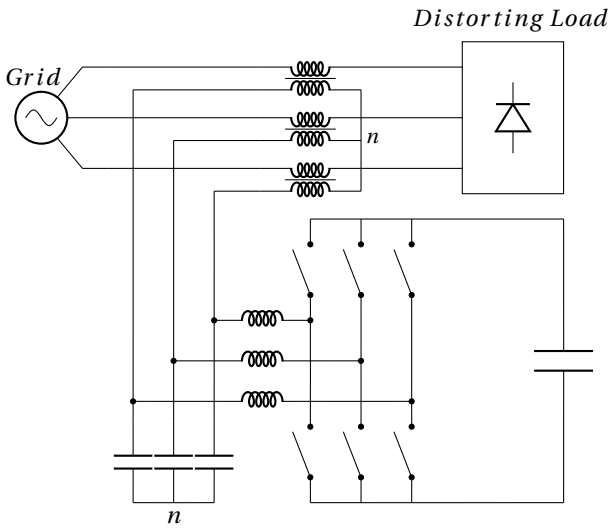


Figure 6.3: Series connected APF.

6.2 Integrated Active Filters

In systems where a self-commutated inverter already exists, which is the case here, control strategies which try to cope with the harmonics in the system can be implemented. This is in the following referred to as an Integrated Active Filter (IAF). In this thesis, the already existing power supply inverter, see Figure 1.2, is used to perform active filtering in the system.

The increase in costs is limited, as the components already exist. An increase in costs will mainly be related to the possibly increased inverter current, since the system currents might increase as a consequence of performing active filtering. The development of the control is usually more complex, as the harmonic cancellation could be desired at a point distant from the inverter, which happens to be the case in our system. When using the inverter in the power supply to perform the active filtering, the switching frequency is normally low. Since the total load current flows through the inverter, the switching frequency should be low to reduce switching induced losses. This influences the properties of the passive terminal filters, and also limits the possibilities of coping with higher-order harmonics.

Chapter 7

Voltage Controlled Harmonic Mitigation

In this chapter, an IAF is developed, with the aim of decreasing the harmonic distortion in the system. The chapter starts off by discussing the utilized general IAF control method named *selective harmonic mitigation*. Further, the availability of system measurements is discussed. The availability of measurements is vital to the choice of approach for harmonic mitigation. The section 7.1 concerns the modification and tuning of the original cascaded voltage controller, hereafter called the *fundamental voltage control*, as it is used to control the fundamental voltage component in the system. In section 7.2, the theory behind the voltage controlled IAF is presented. The schematics of the control structure are shown and discussed. In order to be able to properly control the power consumption of the distorted load when performing active power filtering, a new way of modelling and controlling the power consumption is utilized. This is presented in section 7.3, together with an investigation of how modelling and control of the distorted load affects the harmonics in the system. In the end, the concept of anti-windup in PI-regulators is presented.

Selective Harmonic Mitigation

As mentioned in chapter 6, the control strategies implemented to active filters can be divided into broadband and selective harmonic mitigation. Here, the selective harmonic mitigation, which was developed by the researcher Prof. P. Mattavelli [16], is applied. This method handles each harmonic individually by having different controllers locked to each harmonic frequency; this is also known as closed-loop synchronous frame controllers.

Availability of Measurements and how it Influences the Control Strategy

Since this thesis concerns the power supply for hotel loads, the currents $\vec{i}_R^{abc}$ and $\vec{i}_D^{abc}$ are often difficult and expensive to measure. Hotel loads consist of many small loads at different locations onboard the ship. Measuring the different currents to either all the non-linear or the linear loads requires a huge effort, and brings about an increase in expenses. This is mainly due to the high number of required ampere meters and the increased length of signal wiring. Measuring the voltage

at point B, on the other hand, is rather straightforward. The voltage $\vec{v}_B^{abc}$ can be measured at the transformer, which is part of the power supply, usually located near the inverter. The signal wiring needed is therefore short, and only one three-phase voltmeter is required. Despite the ease of access to $\vec{v}_B^{abc}$, Siemens do not allow measuring this voltage.

If the power supply were to supply the main propulsion system, the number of different loads would have to be decreased, and measuring the currents $\vec{i}_D^{abc}$ and $\vec{i}_R^{abc}$ would be an easier task. This is not the case, and it is therefore assumed that the diode rectifier current $\vec{i}_D^{abc}$ and the ohmic load current $\vec{i}_R^{abc}$ are unavailable. It is notably difficult to make a mathematical model of the current $\vec{i}_D^{abc}$ which depends on the voltage $\vec{v}_A^{abc}$. There was no success in finding an existing mathematical model of the diode rectifier. The fact that the resistance R is unknown and a mathematical model of the diode rectifier is unavailable, makes it impossible to estimate $\vec{i}_D^{abc}$ and $\vec{i}_R^{abc}$ accurately. Due to the reasons mentioned above, it is not feasible to compensate for harmonics by use of current control. Hence, a voltage-controlled harmonic mitigation approach was chosen.

7.1 Modification of Fundamental Voltage Control

The IAF control is built in parallel to the original cascaded voltage control, which was discussed in chapter 3. The original cascaded voltage control, called the fundamental control, produces the fundamental modulator voltage signal $\vec{v}_{M_F}^{abc}$. From the original control, it is possible to control the fundamental voltage at point A, which is the voltage over the capacitor in the passive LCL-filter. Since the loads are connected at point B, it is more convenient to have a stable voltage at point B than at point A. Therefore, the fundamental voltage control is modified to control the voltage at point B. This is achieved by subtracting the fundamental voltage loss over the inductor L_2 and its inner resistance R_{L_2} from the feedback voltage, see Figure 7.1. The band-pass filter is tuned to the fundamental frequency; this tuning is further explained in appendix F.2. The fundamental modulator signal $\vec{v}_{M_F}^{abc}$ and the harmonic modulator signal $\vec{v}_{M_H}^{abc}$ are added together in the end, forming the final modulator signal $\vec{v}_M^{abc}$. The harmonic modulator signal is produced in the voltage controlled IAF, which is developed in the following section.

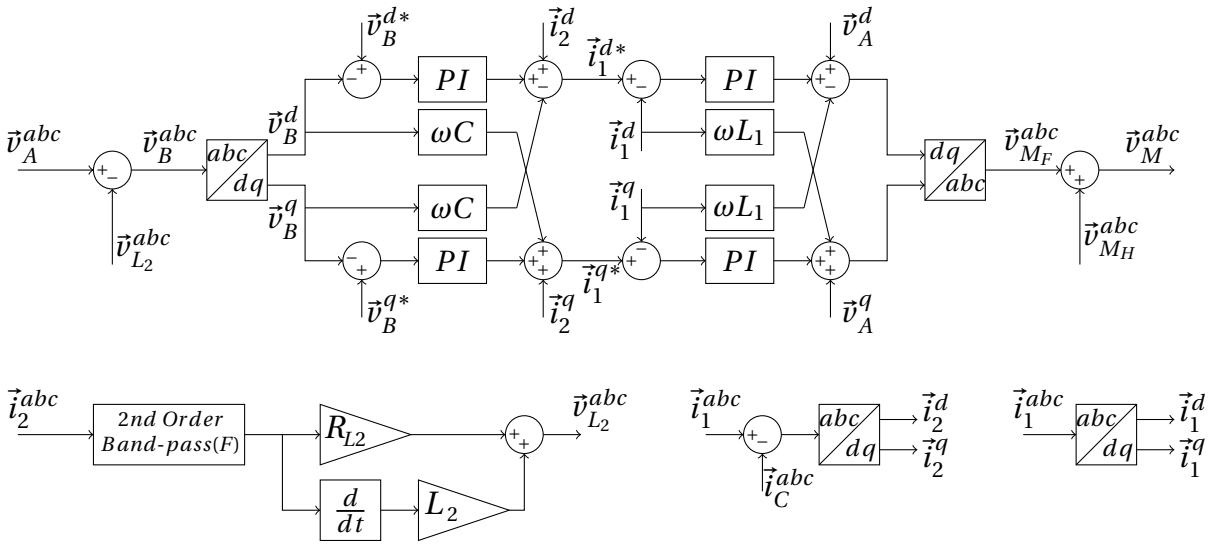


Figure 7.1: Modified fundamental voltage control.

7.1.1 Fundamental Regulator Tuning

The tuning of the fundamental voltage control is based on both pole placement and simulations. The same tuning is used for all of the cases which are investigated. The pole-zero plot of the closed loop OVC and ICC transfer function is depicted in Figure 7.2. The pole-zero diagram is plotted for increasing values of the OVC PI-regulator gains. In the Figure we see that the system becomes unstable when the regulator gains are increased such that poles are placed in the right-half plane. When increasing the ICC PI-regulator gains, the poles move away from the horizontal center line. And by increasing the OVC PI-regulator gains, the poles move to the right in the pole-zero plot. The big red crosses in the pole-zero diagram represent the chosen poles. These poles have shown satisfactory performance during simulations. The PI-regulator gains yielding these poles are presented in Table 7.1. These fundamental regulator gains are used in the continuation of this thesis.

$Gain$	$Value$
$K_{p_{ICC}}$	61.89
$K_{i_{ICC}}$	3333
$K_{p_{OVC}}$	2.358
$K_{i_{OVC}}$	269.7

Table 7.1: Fundamental voltage control regulator tuning.

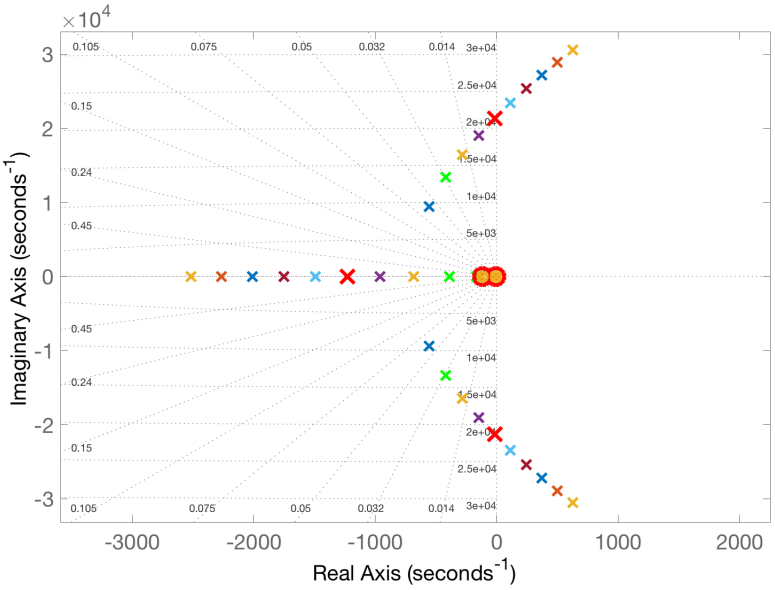


Figure 7.2: Pole-zero plot of the closed loop fundamental control transfer function.

7.2 The Voltage Controlled IAF

The idea behind the voltage controlled IAF is to add a compensating harmonic voltage signal $\vec{v}_{M_H}^{abc}$ to the fundamental voltage modulator signal $\vec{v}_{M_F}^{abc}$, which comes from the cascaded control developed in chapter 3. The selective harmonic control structure can be viewed in Figure 7.3. As can be seen from the figure, the harmonic components of each order are controlled independently. After the different compensating harmonic voltages have been calculated, they are added together, forming the harmonic modulator signal $\vec{v}_{M_H}^{abc}$. As mentioned in the previous section, the voltage $\vec{v}_{M_H}^{abc}$ and $\vec{v}_{M_F}^{abc}$ are added together in the end, forming the final modulator signal $\vec{v}_{M}^{abc}$. The reasons for only handling the first four orders were discussed in chapter 4.

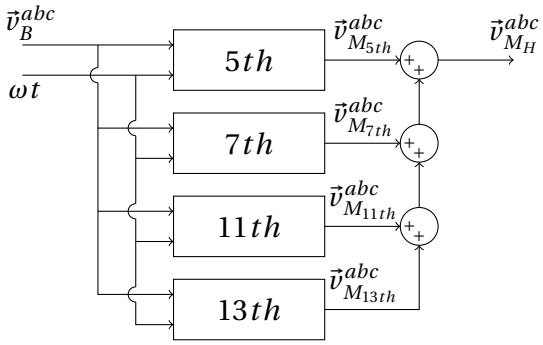


Figure 7.3: Harmonic filter voltage control approach.

The different boxes, named after the different harmonics in Figure 7.3, contain the control viewed in Figure 7.4. The capital letter N represents the harmonic order being dealt with. If the

fifth order is filtered, N has to be changed to five. As the N in parenthesis suggests, the band-pass filter and the PI-regulators also have to be tuned based on which harmonic order is being dealt with. No common tuning method was used for the harmonic control tuning, as these PI-regulator gains were adjusted based on the simulation performance. The tuning of the harmonic controllers is different for each case investigated. Therefore, the tuning is given for each case in chapter 8.

From the control input voltage $\vec{v}_B^{abc}$, a single harmonic component is extracted in order to obtain $\vec{v}_{B_n}^{abc}$. This is done with the use of band-pass filters. The tuning of the different band-pass filters is explained in appendix F.2. The harmonic component is further transformed into dq-coordinates. Since a cancellation of the harmonic content in the voltage $\vec{v}_B^{abc}$ is desired, the d- and q-references are set to zero. The PI-regulators will then try to cope with the different harmonic components and force them to their reference values.

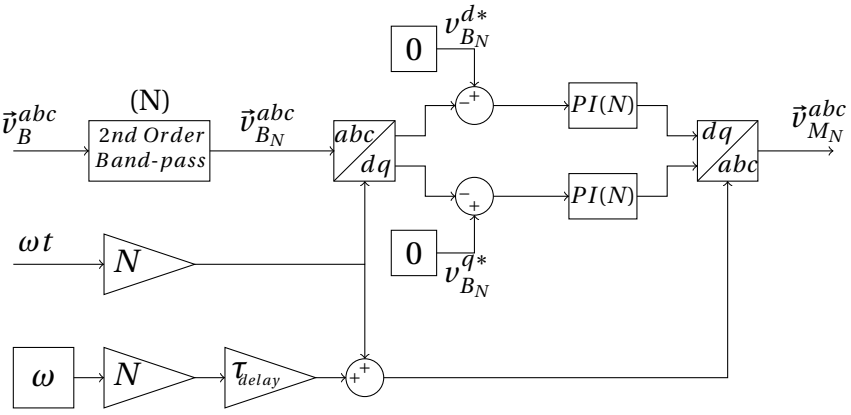


Figure 7.4: The voltage controlled IAF with $\vec{v}_B^{abc}$ measured.

As mentioned in the introduction, measurements of the voltage $\vec{v}_B^{abc}$ and the currents $\vec{i}_2^{abc}$ and $\vec{i}_R^{abc}$ are unavailable. When the inductance L_2 and its inner resistance R_{L2} are known, the voltage $\vec{v}_B^{abc}$ can be calculated from the voltage $\vec{v}_A^{abc}$, the inverter current $\vec{i}_1^{abc}$ and the capacitor current $\vec{i}_C^{abc}$. This gives the following two equations:

$$\vec{i}_2^{abc} = \vec{i}_1^{abc} - \vec{i}_C^{abc} \tag{7.1a}$$

$$\vec{v}_B^{abc} = \vec{v}_A^{abc} - L_2 \frac{d\vec{i}_2^{abc}}{dt} - R_{L2}\vec{i}_2^{abc} \tag{7.1b}$$

From these equations, the control in Figure 7.4 becomes like shown in Figure 7.5. Since the exact characteristics of the component L_2 are known, the voltage at point B can be calculated with high precision in the simulation. However, this is not the case in the real world, and a voltage measurement at point B is therefore strongly recommended in order to obtain a more accurate result.

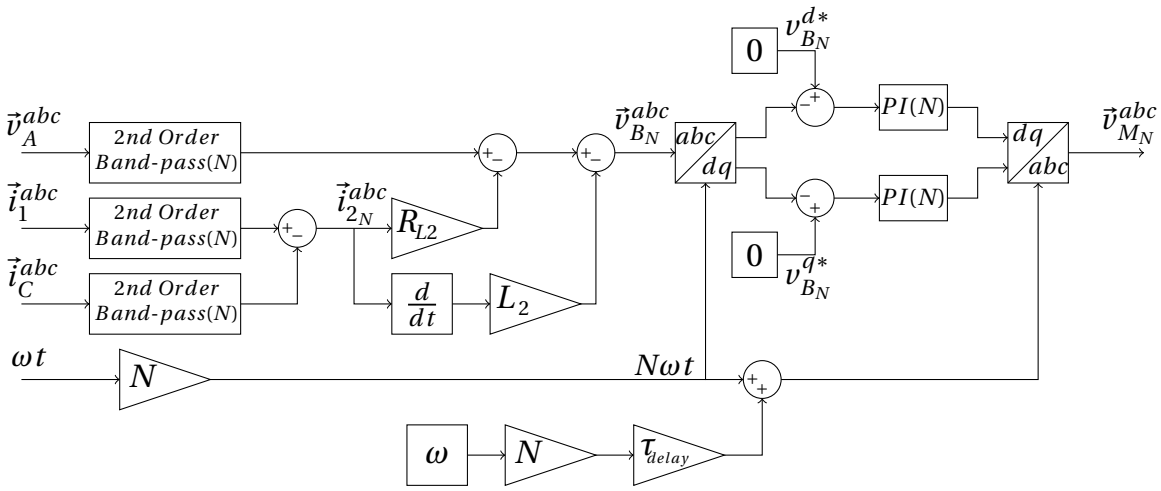


Figure 7.5: The voltage controlled IAF without $\vec{v}_B^{abc}$ measured.

7.2.1 Utilisation of different Park transformations

The amplitude-invariant Park transformation and the inverse amplitude-invariant Park transformation used to transform positive-sequence harmonics into dq-coordinates can be viewed in appendix B. As mentioned in section 5.1.1, the 5th, 11th, 17th, etc. harmonics produced by a 6-pulse diode rectifier are in negative sequence. Using a negative-sequence Park transformation is therefore necessary to be able to transform these harmonics into dq-coordinates. The applied negative-sequence amplitude-invariant Park transform and its inverse can also be viewed in appendix B.

7.2.2 Time delay compensation

There is a time delay in the active harmonic filter from the current is measured until it is processed and fed to the modulator as the voltage signal $\vec{v}_{M_H}^{abc}$. In the Integrated Active Harmonic filter, see Figure 7.4, an angle is added to the second Park transformation in order to compensate for the time delay. By adding an angle, the Park transform inserts the harmonic compensating voltage from the PI-regulators ahead of time. The compensating angle is calculated with the equation $\theta_{comp} = \omega N \tau_{delay}$, which is dependent on the order of the harmonic component the active filter is dealing with. The time delay τ_{delay} has been estimated to 0.38ms through simulations. When dealing with the fifth harmonic, an angle of approximately 41° is added to the second Park transformation relative to the first. This angle is proportional to the harmonic order, and will increase as the harmonic order increases. For this reason, the time delay compensation is very important for higher-order harmonics. The delay angle could then be such that the compensation voltage is inserted around half a period later than it should, which will worsen the problem significantly, and likely make the system unstable.

Another way to tackle the time delay issue is to insert a time delay box in the simulations; delaying the compensating voltage signal with a magnitude of one period minus the actual time delay. This method has been tested, and it has been shown to function properly. However, the signal delay method is not preferred, as it is slower than the angle compensation method previously discussed. The difference in performance will be especially noticeable during transients. This is due to the later insertion of the compensating voltage compared to the angle compensation method. The major practical drawback with the signal delay method, however, is the need for data storage capability. The signal which is to be inserted in the next period needs to be stored pending the transmission to the inverter modulator.

7.3 Control of Distorted Power Consumption

The distorted power consumption has, when adding different amounts of harmonic compensation, shown itself to be difficult to control by calculating the resistor R_D. In order to get a more precise estimation of the distorted power consumption, a controlled current source is inserted into the model, replacing the adjustable resistance R_D, see Figure 7.6. The current reference $i^*_{R_D}$ fed to the controllable current source is obtained by dividing the difference between the desired distorted power consumption P^*_D and the ohmic losses P_{L_D} on the measured voltage v_D. The measured DC-side voltage v_D is filtered through a first order low-pass filter to get rid of the capacitor voltage ripple, thereby obtaining a more even power consumption. The power losses in L_D are also low-pass filtered to get a smaller ripple.

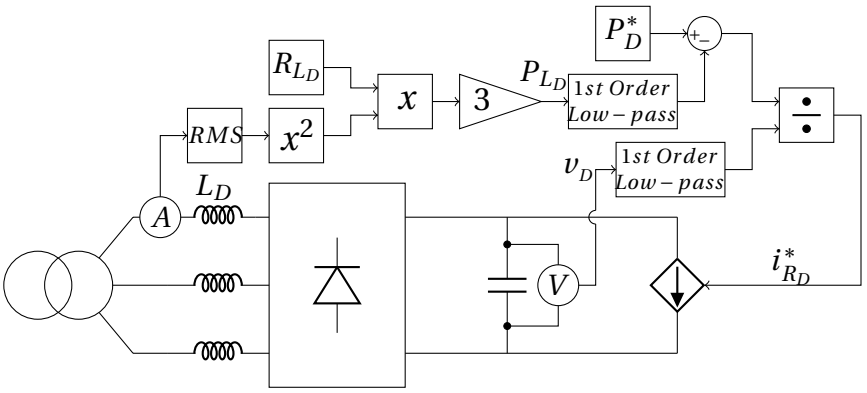


Figure 7.6: Control of the distorted power consumption when using a controllable current source.

7.3.1 Load Modelling - Influence on Harmonic Distortion

Having a controlled current source instead of a variable resistance R_D yields negligible differences in the THD level. Table 7.2a shows the THD levels at different operation modes with the resistance R_D, and Table 7.2b shows the THD levels for the controllable current source. From the tables it

can be seen that the maximum deviation of the THD is 0.05%. Decreasing the simulation time step would make the differences even smaller.

When inserting the IAF, the DC-side capacitor C_D needs to be increased in order to limit the DC-side voltage ripple to 2%. The capacitor is increased from 17.5mF to 55mF in the maximum harmonic mitigation case. For the minimum and proposed harmonic mitigation cases, C_D is changed to 45mF and 49mF, respectively. An increase in the capacitor size has been shown to slightly reduce the harmonic content in the circuit, and this is the main reason for the slightly different results in Table 7.2a and Table 7.2b, compared to Table 5.1 in chapter 5. The C_D with a capacitance of $55mF$ was used to obtain these THD levels. Because of the modification of the fundamental control, there is also a small increase of the voltage at point B, especially during high power consumption. This will slightly influence the THD level in the system.

P_D [$\%ofS_n$]	P_R [$\%ofS_n$]		
	20%	10%	0%
70%	9.02%	9.15%	9.34%
50%	7.43%	7.55%	7.68%
30%	5.67%	5.77%	5.85%

(a) Variable Resistor.

P_D [$\%ofS_n$]	P_R [$\%ofS_n$]		
	20%	10%	0%
70%	9.01%	9.19%	9.33%
50%	7.41%	7.55%	7.73%
30%	5.64%	5.75%	5.90%

(b) Controlled Current Source.

Table 7.2: THD with different modelling of the distorted load.

7.4 Anti-Windup

Anti-windup limits the control output signal from PI-regulators. When a deviation from the reference signal exists, the integral sum starts to accumulate. When the integral control output signal continues to increase in magnitude due to a persisting control error, a phenomena called integral windup [27] occurs. Anti-windup could be used in several applications; for example, it could be used to decrease the control overshoot during transients. If a significant step in the control reference occurs, a big control error follows. Anti-windup limits the integral windup, which gives better control performance.

It could happen that the controller is unable to fully cancel the control error due to system constraints, which means that it is not physically possible to cancel the error under the given circumstances. The integral part of the PI-regulator will then build up over time. This is a result of a constant error between the measured values and the desired reference values in the control system. This accumulation effect has been shown to cause over-modulation in the inverter and a slower response during transients. The slowness of the response is determined by the time duration of the wind-up. In Figure 7.7, the regulator response is shown with and without anti-windup. From the figure, we see that when stepping up, both PI-regulators have the same response. The problem becomes clear when stepping down again. The control acts slowly when stepping down without

the anti-windup. The wound up regulator must then first be wound down again before the control starts to take action. Note that the areas A_1 and A_2 are equal without the use of anti-windup. The result when using a properly tuned anti-windup is shown on the right-hand side in Figure 7.7. The control acts immediately after the reference is stepped down.

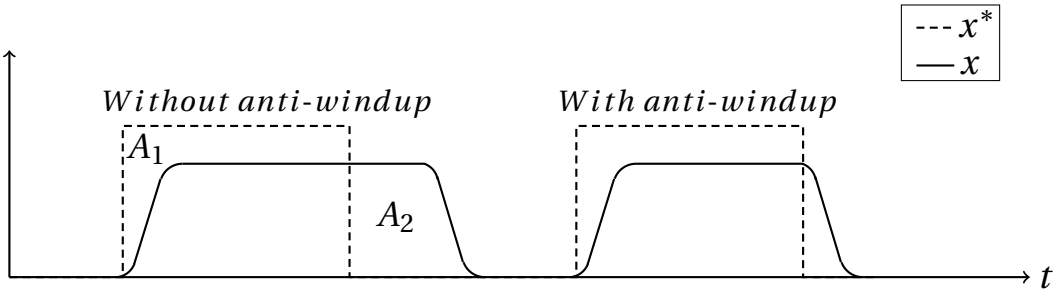


Figure 7.7: Example of control response with and without anti-windup.

Anti-windup can also be utilized when a small control error is preferred, rather than a perfect error elimination. Reasons for this could be that a total cancellation of the error is expensive in terms of system power-losses and that it places higher requirements on the components.

The anti-windup method used here is the back-calculation method. The block diagram of the back-calculation anti-windup method is presented in Figure 7.8. In order to ensure that an integral windup is prevented, a negative feedback loop and a saturation block are added to the original PI-regulator. The saturation block limits the output to a certain maximum level. The feedback loop consists of the saturated signal subtracted from the control output signal. The signal is fed to the integral branch of the PI-regulator, and this prevents an integral windup.

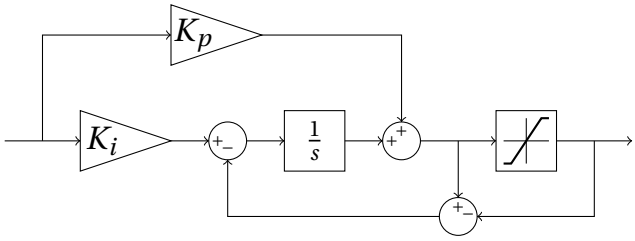


Figure 7.8: Anti-windup using back-calculation.

Chapter 8

Case Studies

This chapter contains simulations of the three different cases investigated. As discussed and concluded in chapter 4, efforts should be concentrated around mitigating the 5th, 7th, 11th and the 13th harmonic orders. The first section, section 8.1, concerns the case of maximum harmonic mitigation with no limitations on system current magnitudes. In section 8.2, the case of minimum harmonic mitigation is investigated. This case shows small current magnitudes, while at the same time keeping the THD within the limitations set by DNV. In the third and final simulation case, see section 8.3, simulations of the proposed solution of harmonic mitigation is presented. This case will ensure limited currents and a harmonic cancellation well within the requirements set by DNV.

A challenge with the implementation of capacitors is their aging characteristics. The capacitance of a capacitor will decrease over time [28]. It is common to define a capacitors end of life when its capacitance has decreased by 20% from its original value [29, 30]. The proposed case is therefore divided into two, representing the system with a new and an old capacitor.

General Simulation Setup

All cases are simulated with a varying distorted power consumption, in order to see the behaviour during transients and start-ups. This gives an understanding of how well and how fast the active filter performs. The time duration of the simulation is set to 27 seconds, with the diode rectifier power consumption varying over time. At first the power supply is initialized, and the voltage at point B rises to 1 pu over one second and stabilizes. After two seconds the distorted power consumption (P_D) steps from zero to 70% of Sn. After eleven seconds the power consumption drops from 70% to 50%, and after nineteen seconds it drops from 50% to 30%. The reference distorted power consumption P_D^* is shown in Figure 8.1.

As discussed in chapter 5 and presented in Table 5.1, the harmonic distortion increases when reducing the ohmic power consumption (P_R). Each case is therefore simulated for a P_R of 0% and 20% of Sn. This ensures that the IAF works properly in every mode of operation. In order to get a better picture of the IAFs performance during transients and start-ups, two different simulations were

run, one with the IAFs constantly switched on, and one where the IAFs are periodically switched on and off. When the IAFs are periodically switched, the filter is switched on and off again at the times shown in Figure 8.2. Before the IAF is switched on, the PI-regulators are reset, in order to investigate their start-up performance. Notice that the IAF is switched off at the same time as P_D is changed, and switched on again one second later.

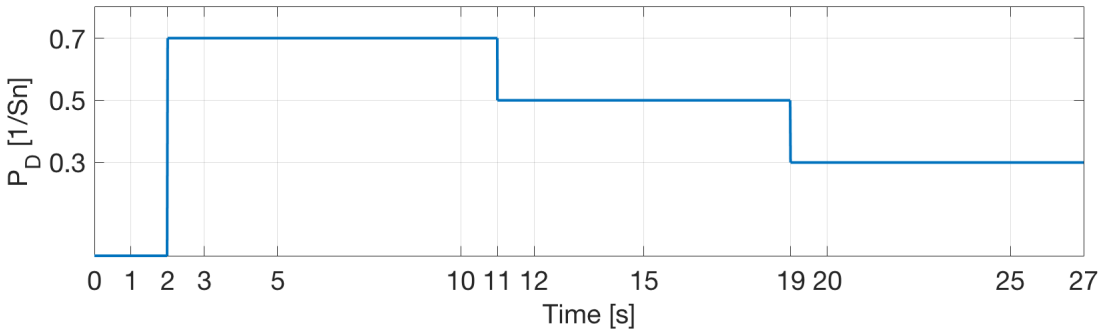


Figure 8.1: Diode rectifier reference power consumption P_D^*.

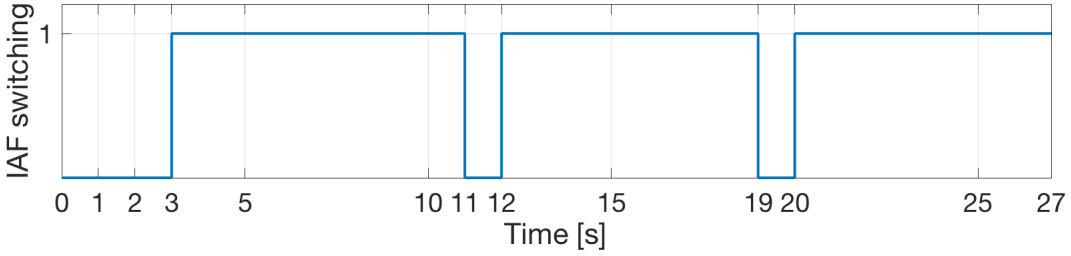


Figure 8.2: Switching of IAF when periodically connected (1 = on and 0 = off).

The sample time used in all simulations is:

$$T_{sample} = 5 \cdot 10^{-6} s. \tag{8.1}$$

The change in the LCL-filter currents while filtering is of major importance, as it generates power losses due to the internal resistances of the components. The RMS capacitor current $i_{C_{RMS}}$ and the RMS inverter current $i_{1_{RMS}}$ are therefore compared before and after the IAF is switched on. The magnitude of the currents is also investigated in each of the three different cases. The THD at point B and the total LCL-filter power losses are presented for every mode of operation in each case. This allows for a thorough overall comparison of the different cases, which makes the choice of mitigation strategy easier. In order to get a proper overview of the cases, the currents $i_{C_{RMS}}$ and $i_{1_{RMS}}$, the THD, and the LCL-filter power losses are presented in bar graphs. The Simulink model used for the simulations can be viewed in appendix E.

8.1 CASE 1: Maximum Harmonic Mitigation

This case investigates the abilities of the developed IAF, with no limitations on system currents. The aim is to fully cancel the four harmonic orders being dealt with. The individual numerical parameters applied in the simulations of this case are displayed in Table 8.1. The LCL-filter capacitor size was calculated based on the inverter switching frequency when discussing the LCL-filter, see section 3.3.1. The tuning of the harmonic PI-regulators is the same for all harmonics in this case. The tuning is found by trial and error.

$Parameter$	$Value$
C	$6.4mF$
C_D	$55mF$
K_{p_N}	247.6
K_{i_N}	13333

Table 8.1: Maximum harmonic mitigation parameters.

8.1.1 Mitigation of Harmonic Orders

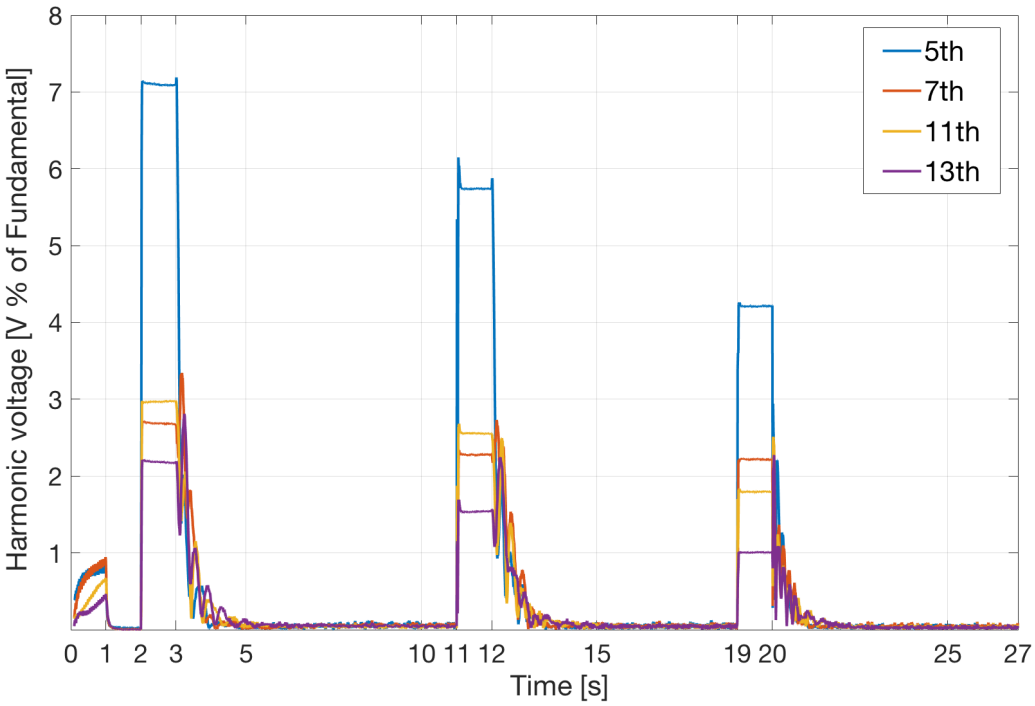
The performance of the IAF is best seen when investigating how the different harmonics are cancelled when varying the power consumption. First, the IAF performance is considered when P_R = 0% of Sn. Figure 8.3a represents the case with the IAF turned on and off periodically, and Figure 8.3b represents the case where the filter is constantly turned on. Secondly, we are looking at the IAF performance when P_R = 20% of Sn. Figure 8.4a and Figure 8.4b represent the cases when the IAF is periodically and constantly turned on, respectively.

The above-mentioned graphs are obtained with Fourier analysis. The magnitude of the four relevant harmonics are found for each frequency. Every magnitude is represented by a point in the relevant graph, and lines are drawn between the points, which yields the presented graphs. The THD analysis is only valid in stationary conditions. However, the frequency spectrum is still correct for the single wavelength, regardless of the validity of the THD analysis. In other terms, the graphs show the voltage feedback to the different orders of harmonic controllers during transients and steady state.

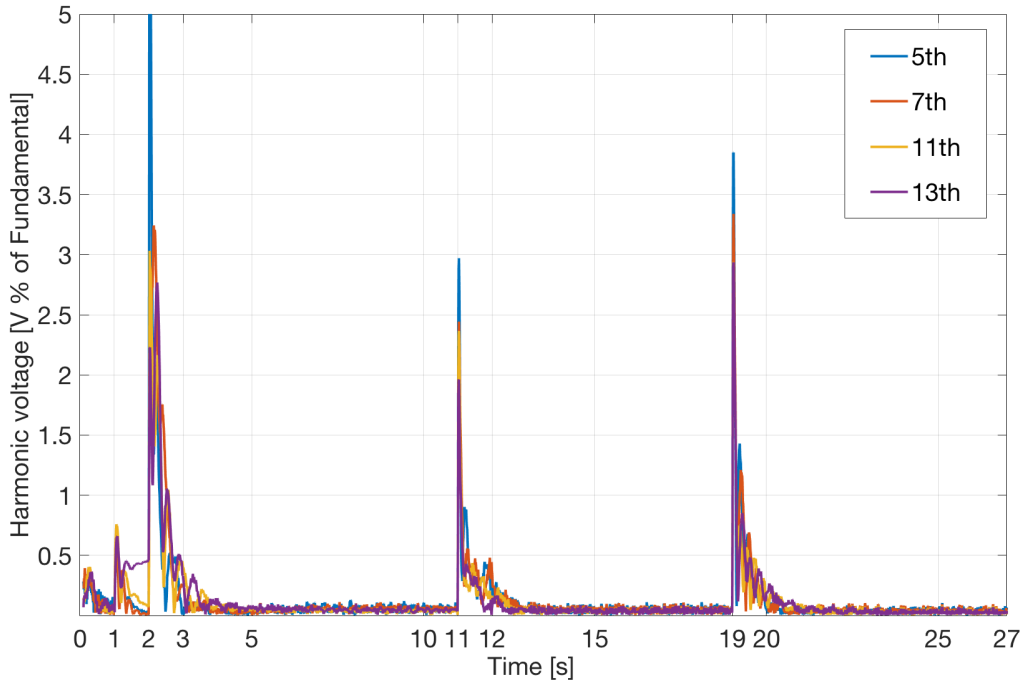
From Figure 8.3a and Figure 8.3b, it can be seen that the harmonic orders in question are forced to approach zero when P_R = 0%. In Figure 8.3a it can be seen that, before turning on the IAF, the 5th harmonic order is the main contributor to the harmonic distortion. The 5th order is at P_D = 70%, which is the worst-case scenario, slightly above 7% of the fundamental voltage. The 7th order is lower than the 13th order at P_D = 70%. The 7th order is less influenced by a decreasing P_D, and becomes the second-most contributing component at P_D = 30%. When turning on the IAF, the 5th order rapidly starts to decrease. The other three harmonic components are not decreasing in the

same manner, and they start to fluctuate. Since the 5th-order component is the largest contributor to the harmonic distortion, the feedback to the 5th order harmonic controller is the largest. This causes the proportional gain in the PI-regulators to rapidly insert a compensating 5th-order harmonic voltage in the system. Exposing a diode rectifier to a 5th harmonic leads to an increase of the other harmonics. With a diode rectifier it is difficult to predict which harmonics are to be expected in return when a certain harmonic is inserted. This is why it is so difficult to make a mathematical model of the diode rectifier, as was mentioned in the previous chapter. When the 5th harmonic reaches the same order of magnitude as the other harmonics, they descend to zero in a joint manner. The system is stable, both during IAF turn-on and turn-off. With $P_R = 0\%$, and the IAF constantly connected, the graph in Figure 8.3b is obtained. During the step changes of P_D at two, eleven and nineteen seconds, the harmonic voltages show an increase in magnitude. The IAF rapidly mitigates the harmonics, and they descend towards zero.

When $P_R = 20\%$, the graphs in Figure 8.4a and Figure 8.4b are obtained. The differences when $P_R = 0\%$ and $P_R = 20\%$ are minor, making the above-mentioned remarks valid in both cases. Hence, Figure 8.4a and Figure 8.4b are not further discussed.

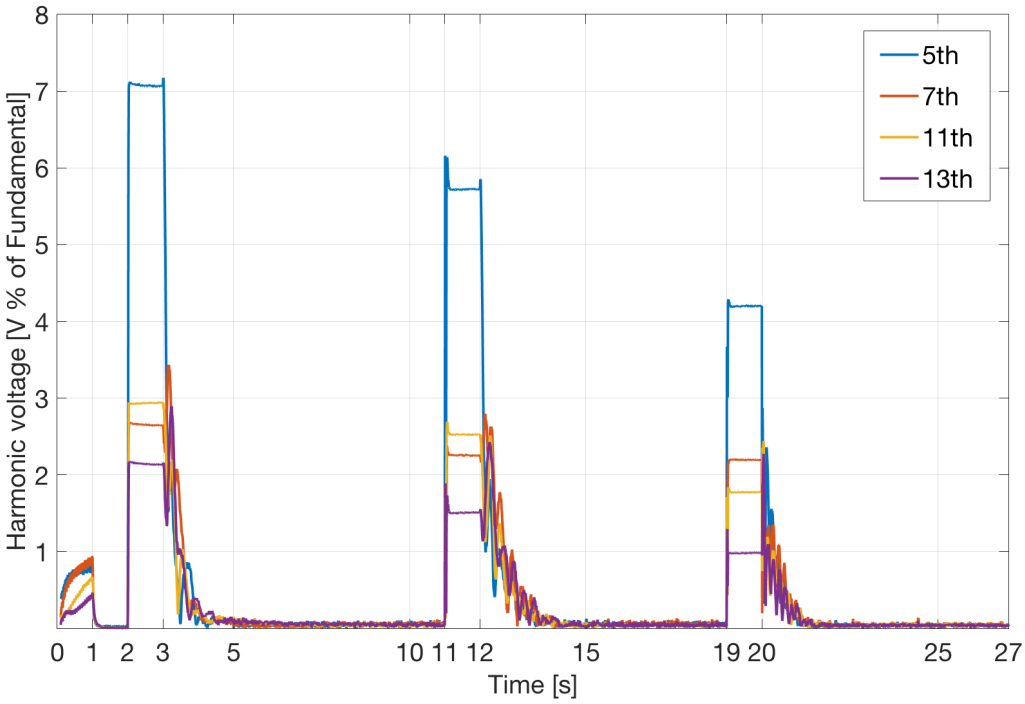


(a) Periodically turned on IAF. See Figure 8.2 for the turning on scheme.

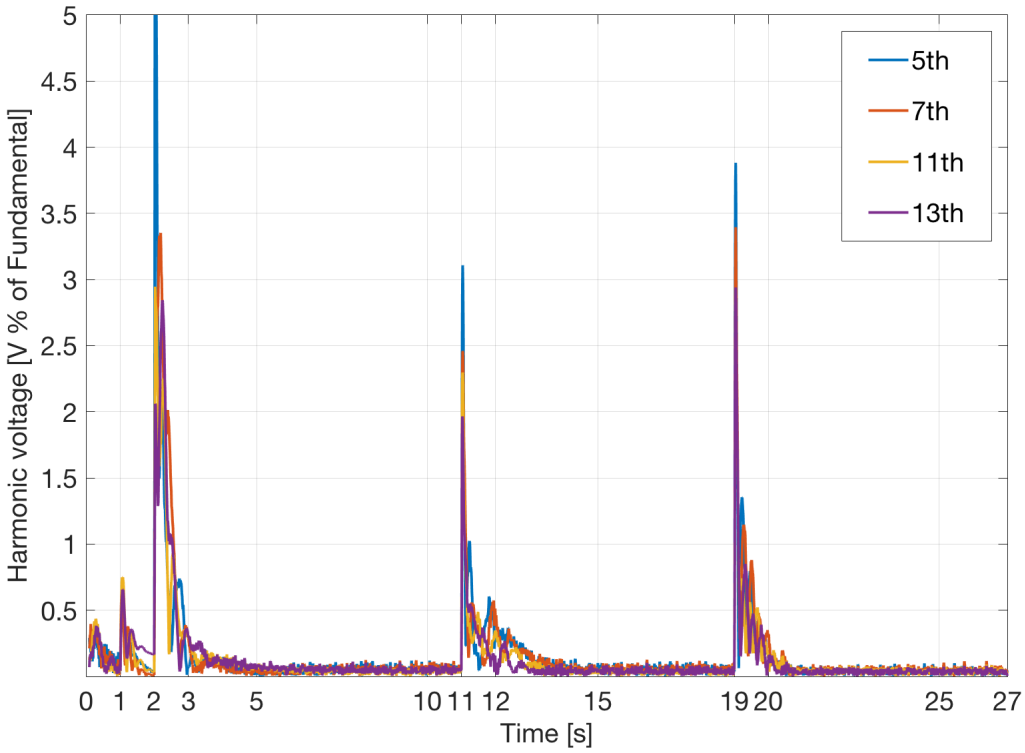


(b) Constantly turned on IAF.

Figure 8.3: Harmonic voltages at maximum harmonic mitigation when $P_R^* = 0\%$ and P_D^* like shown in Figure 8.1.



(a) Periodically turned on IAF. See Figure 8.2 for the turning on scheme.

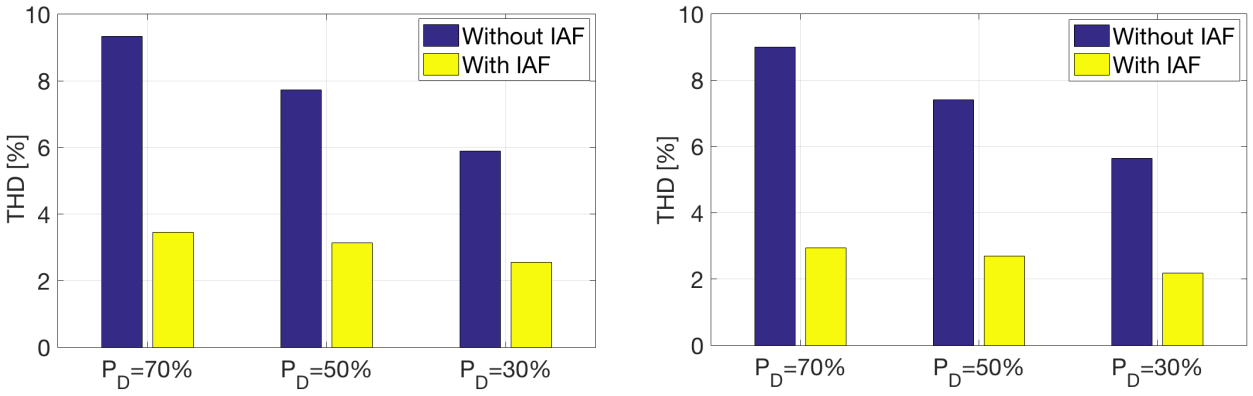


(b) Constantly turned on IAF.

Figure 8.4: Harmonic voltages at maximum harmonic mitigation when $P_R^* = 20\%$ of Sn and P_D^* like shown in Figure 8.1.

8.1.2 THD

The THD levels obtained in this case are presented in Figure 8.5a (P_R = 0% of Sn) and Figure 8.5b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.1, in Table C.1a and Table C.1b. From the bar graph it becomes clear how effective the IAF is. With the IAF turned on, the THD never exceeds 3.44% in any steady state mode of operation. The THD decreases when P_D decreases and when P_R increases.



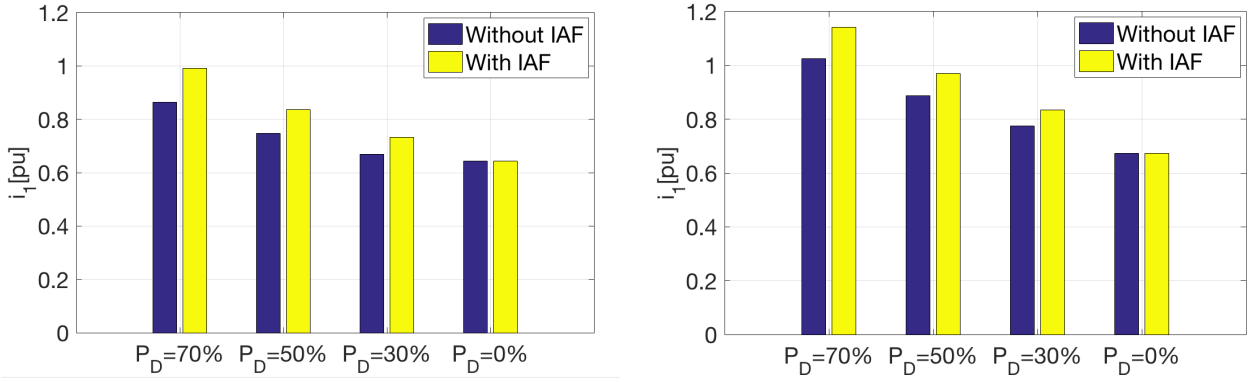
(a) THD at P_R = 0% of Sn

(b) THD at P_R = 20% of Sn

Figure 8.5: THD at maximum harmonic mitigation.

8.1.3 Inverter Current

The inverter current i_1 is given in Figure 8.6a (P_R = 0% of Sn) and Figure 8.6b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.1 in Table C.2a and Table C.2b. From the bar graphs, it can be seen that i_1 strongly depends on both P_R and P_D. The current increases when the IAF is switched on, making the current dependent on the state of filtering. In the worst-case scenario, i_1 is as high as 1.142pu with the IAF switched on. The inverter design should allow for this increase.



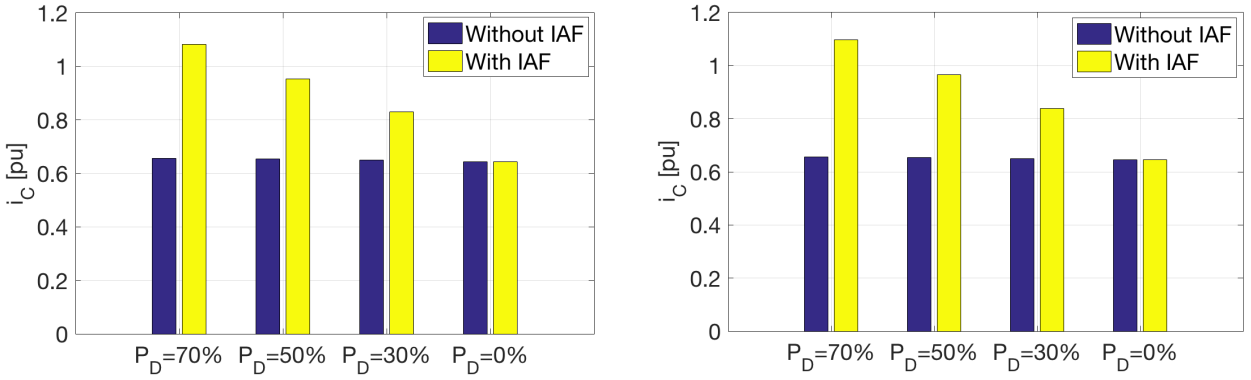
(a) i_1 at P_R = 0% of Sn

(b) i_1 at P_R = 20% of Sn

Figure 8.6: Inverter current at maximum harmonic mitigation.

8.1.4 Capacitor Current

The capacitor current i_C is given in Figure 8.7a (P_R = 0% of Sn) and Figure 8.7b (P_R = 20% of Sn). The data behind these graphs can be viewed in appendix C.1 in Table C.3a and Table C.3b. As can be seen from the graphs, the capacitor current exceeds 1pu at P_D = 70% when the IAF is turned on. With the IAF turned off, i_C is almost independent of both P_D and P_R. In general, the capacitor current is independent of P_R, regardless of whether the IAF is turned on or off.



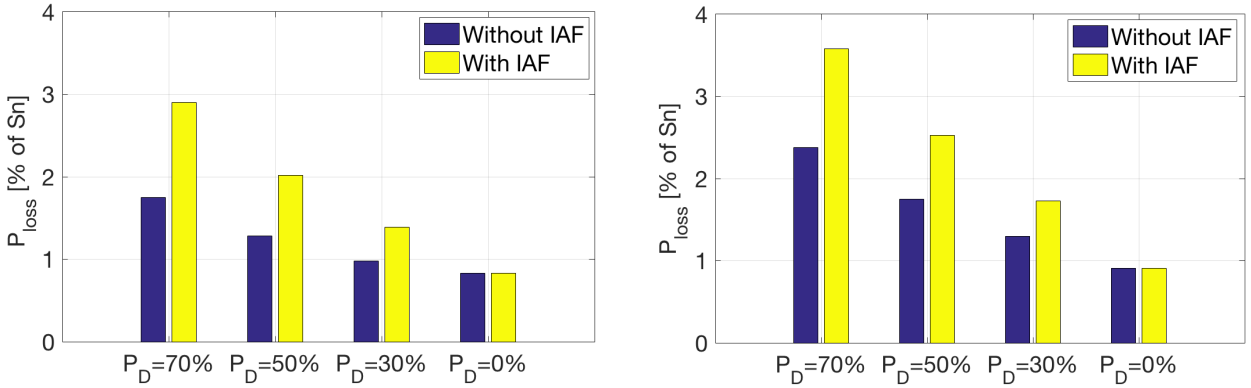
(a) i_C at P_R = 0% of Sn

(b) i_C at P_R = 20% of Sn

Figure 8.7: LCL-filter capacitor current at maximum harmonic mitigation

8.1.5 Power Losses

The LCL-filter power losses are given in Figure 8.8a (P_R = 0% of Sn) and Figure 8.8b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.1, in Table C.4a and Table C.4b. As can be seen from the bar graphs, the power losses depend significantly on both P_D and P_R. Naturally, the power losses are higher when P_R = 20%, compared to the case where P_R = 0%. Switching the IAF on leads to a substantial increase in the power losses. In the worst-case scenario, the power losses will increase with 1.2%, from 2.38% to 3.58% of Sn. The no-load losses are 0.83%.



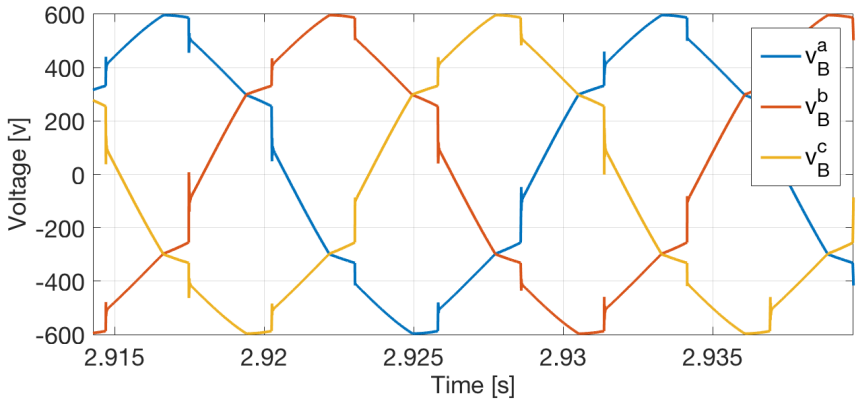
(a) P_{loss} at P_R = 0% of Sn

(b) P_{loss} at P_R = 20% of Sn

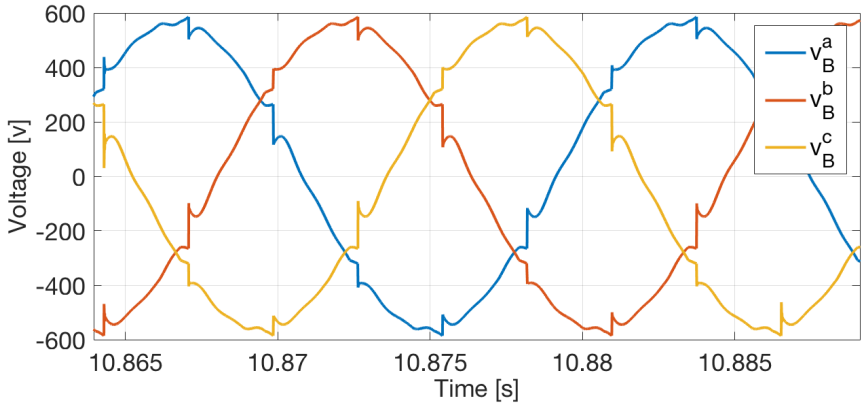
Figure 8.8: Power loss at maximum harmonic mitigation

8.1.6 Worst Case Voltage Waveform and Frequency Spectrums

The worst-case voltage waveform, i.e. with $P_D = 70\%$ and $P_R = 0\%$ of Sn, is presented with and without the IAF in Figure 8.9a (THD = 9.33%) and Figure 8.9b (THD = 3.44%). The corresponding frequency spectrums for the above-mentioned waveforms are shown in Figure 8.10a and Figure 8.10b. The harmonics in these frequency spectrums matches the harmonic found in the Figures 8.3 and Figures 8.4.

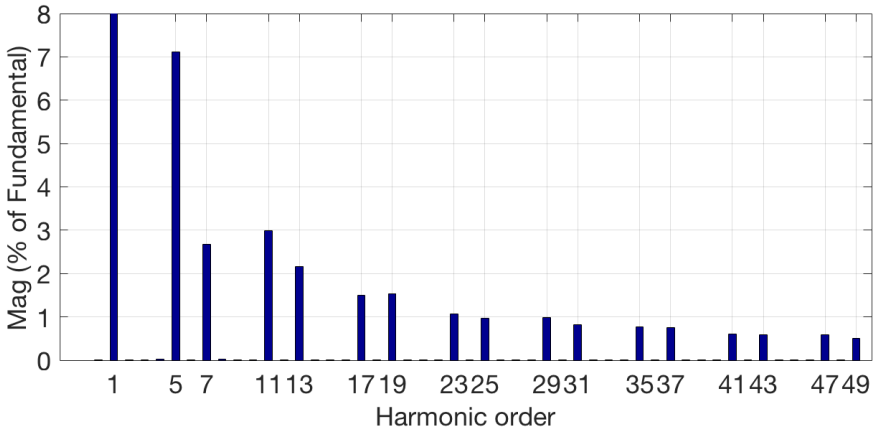


(a) IAF turned off resulting in a THD of 9.33%.

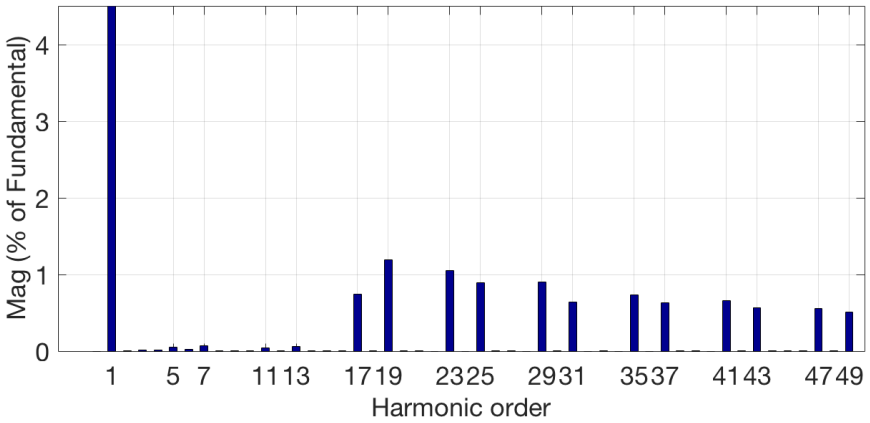


(b) IAF turned on resulting in a THD of 3.44%.

Figure 8.9: Voltage waveforms at maximum harmonic mitigation when $P_D = 70\%$ and $P_R = 0\%$.



(a) IAF turned off resulting in a THD of 9.33%. See corresponding waveform in Figure 8.9a.



(b) IAF turned on resulting in a THD of 3.44%. See corresponding waveform in Figure 8.9b.

Figure 8.10: Frequency spectrums at maximum harmonic mitigation when $P_D = 70\%$ and $P_R = 0\%$.

8.2 CASE 2: Minimum Harmonic Mitigation

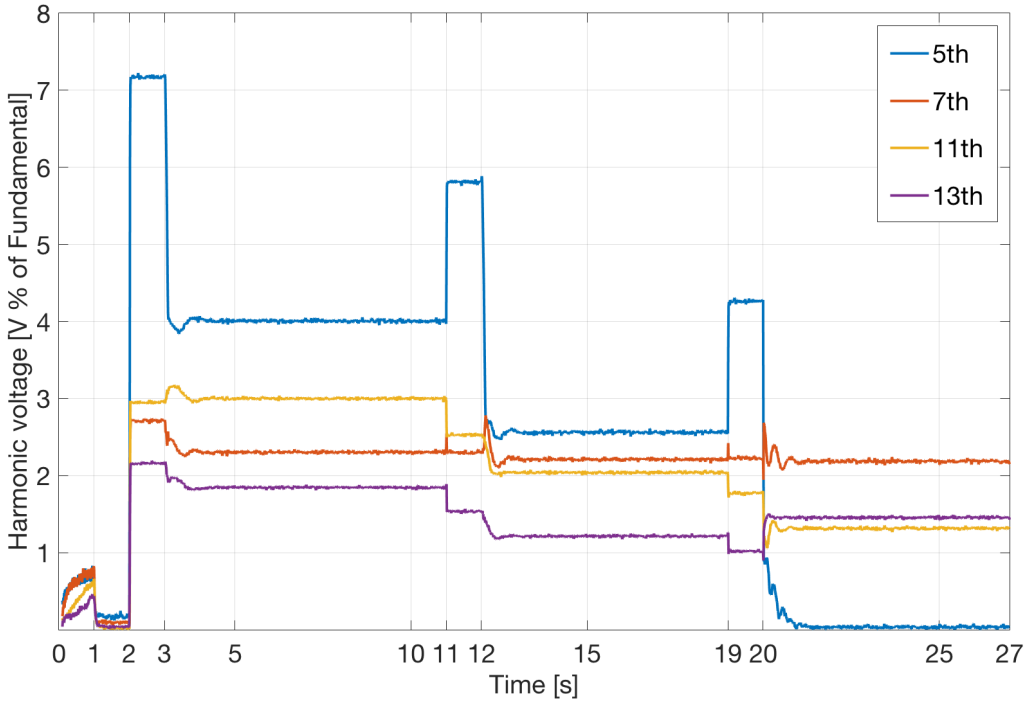
The power losses in the power supply depend on the magnitude of the current flowing through the LCL-filter. Filtering the harmonics increases the current in the LCL-filter. This case is therefore based on finding the minimum currents when still operating within the THD requirements. By using anti-windup it is possible to attenuate the harmonics slightly, instead of trying to fully cancel them, like in the previous case. In order to operate within the requirements, it is only necessary to deal with the 5th and the 7th harmonic components. These components are only attenuated to such a degree that the requirements from DNV are met, in order to limit the currents flowing in the system.The numerical parameters applied in the simulations of this case are displayed in Table 8.2. The LCL-filter capacitor was chosen to be 3.8mF, since this is close to the lower limit of what is physically achievable. This capacitor has also, through simulations, proven itself to contribute to a well behaving system. In this case, each PI-regulator is tuned individually, see Table 8.2. The DC-side capacitor C_D has been reduced from 55mF to 45mF.

$Parameter$	$Value$
C	$3.8mF$
C_D	$45mF$
$K_{p_{5th}}$	123.8
$K_{i_{5th}}$	6667
$K_{p_{7th}}$	61.89
$K_{i_{7th}}$	3333

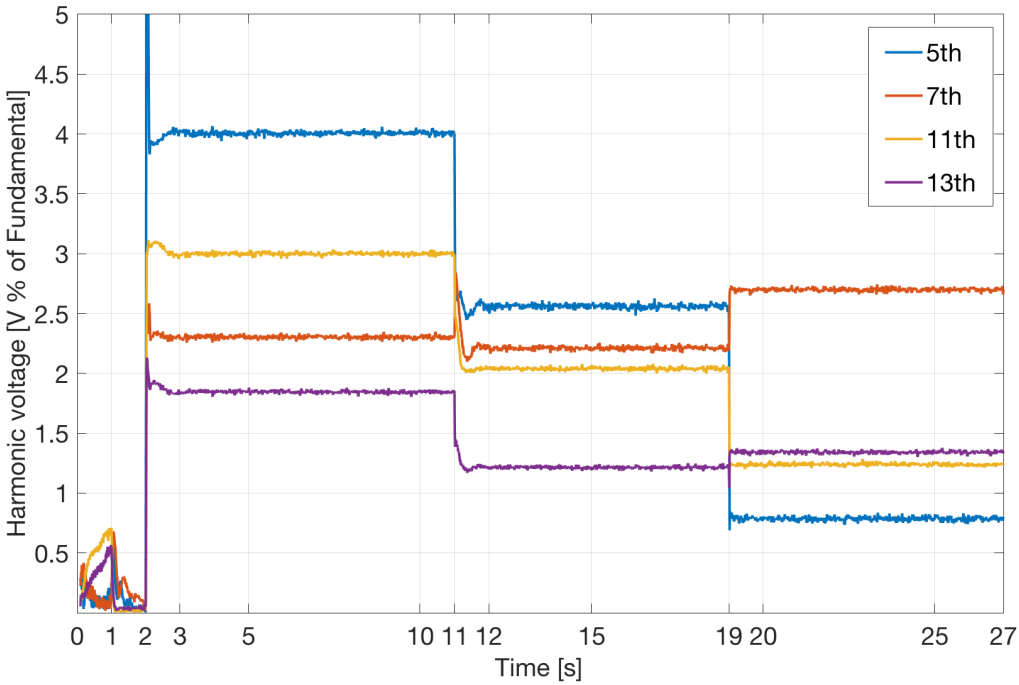
Table 8.2: Minimum harmonic mitigation parameters.

8.2.1 Mitigation of Harmonic Voltages

The Figures 8.11a and Figure 8.11b represents the cases with a periodically switched and a constantly switched on IAF, respectively. The above-mentioned figures are obtained with $P_R = 0\%$. Due to the small/negligible differences, the two graphs representing the operation mode with $P_R = 20\%$ are placed in appendix D. From Figure 8.11a and Figure 8.11b, it can be seen that none of the harmonic voltages exceed the demand of maximum 5% of the fundamental voltage when the IAF is turned on. The 5th harmonic component is controlled from roughly 7% to 4% when $P_D = 70\%$. It is interesting to see that, when dropping from $P_D = 50\%$ to $P_D = 30\%$, the harmonics obtained are dependent on whether the IAF is constantly on or periodically switched. This means that the IAF is dependent on memory when utilizing anti-windup in the PI-regulators. When decreasing P_D from 50% to 30%, the 7th harmonic increases when the IAF is constantly turned on. This is the reason for choosing to reduce the 7th harmonic, instead of the 11th harmonic, despite the 11th harmonic being larger at $P_D = 70\%$.



(a) Periodically turned on IAF. See figure 8.2 for the turning on scheme.

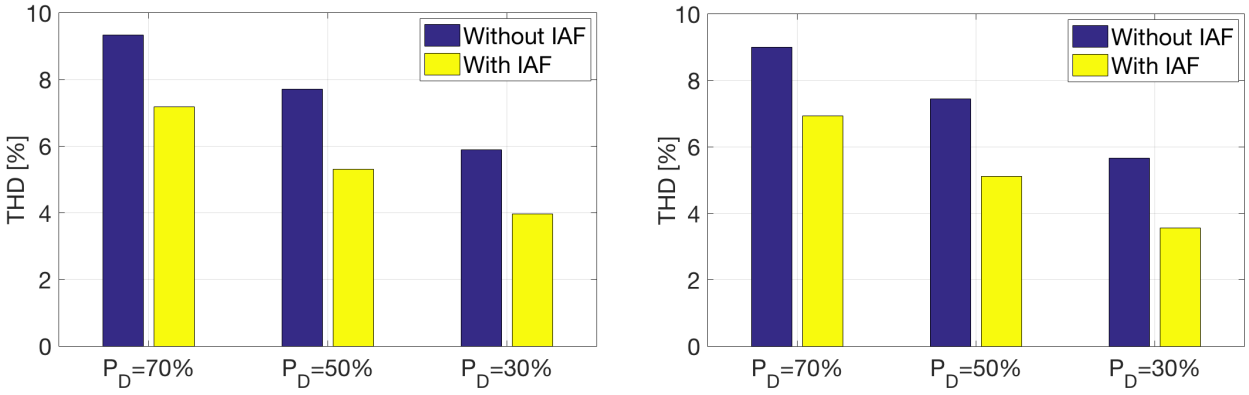


(b) Constantly turned on IAF.

Figure 8.11: Harmonic voltages at minimum harmonic mitigation when $P_R^* = 0\%$ and P_D^* like shown in Figure 8.1. The IAF is only acting on the 5th and the 7th harmonic orders.

8.2.2 THD

The THD levels obtained in this case are presented in Figure 8.12a ($P_R = 0\%$ of Sn) and 8.12b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.2, in Table C.5a and Table C.5b. With the IAF turned on, the THD never exceeds 7.18% in any steady state mode of operation. This is below the maximum allowed THD of 8%.



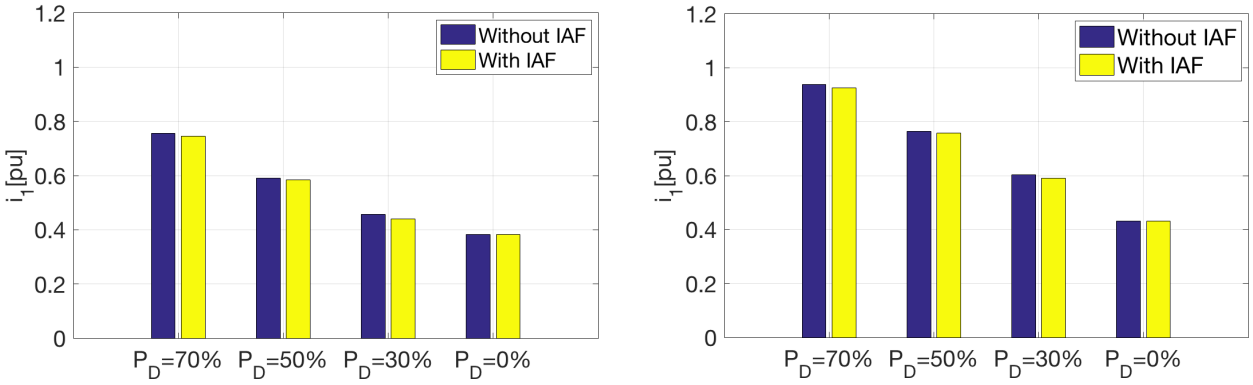
(a) THD at $P_R = 0\%$ of Sn

(b) THD at $P_R = 20\%$ of Sn

Figure 8.12: THD at minimum harmonic mitigation.

8.2.3 Inverter Current

The inverter current i_1 is given in Figure 8.13a ($P_R = 0\%$ of Sn) and 8.13b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.2, in Table C.6a and Table C.6b. From the bar graphs it can be seen that i_1 strongly depends on both P_R and P_D. It is worth noting that the current decreases slightly when the IAF is switched on and P_D is bigger than zero. In the worst-case scenario, i_1 is only 0.939pu with the IAF switched on.



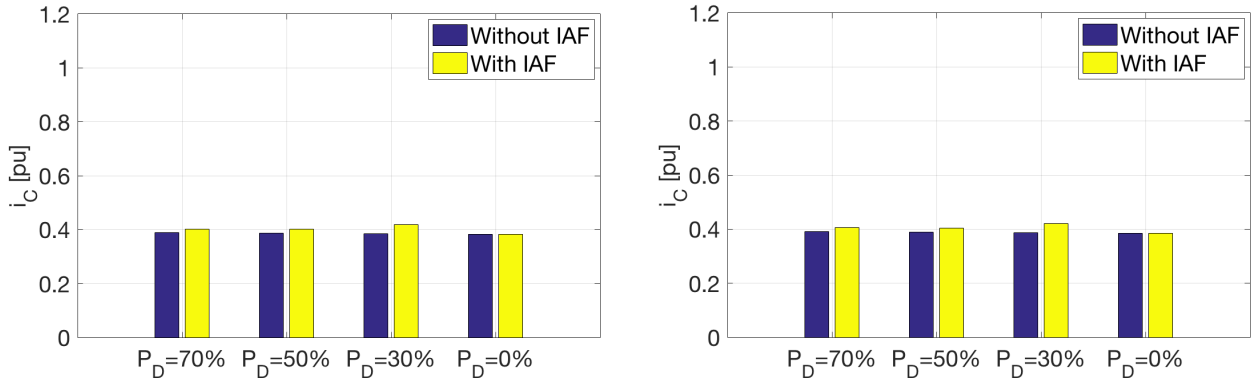
(a) i_1 at $P_R = 0\%$ of Sn

(b) i_1 at $P_R = 20\%$ of Sn

Figure 8.13: Inverter current at minimum harmonic mitigation.

8.2.4 Capacitor Current

The capacitor current i_C is given in Figure 8.14a ($P_R = 0\%$ of Sn) and 8.14b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.2, in Table C.7a and Table C.7b. As seen from the graphs, i_C is almost independent of both P_D and P_R. This is the case regardless of whether the IAF is turned on or off. In general, the capacitor current is very low, with a maximum value of 0.421pu at $P_D = 30\%$ and $P_R = 20\%$.



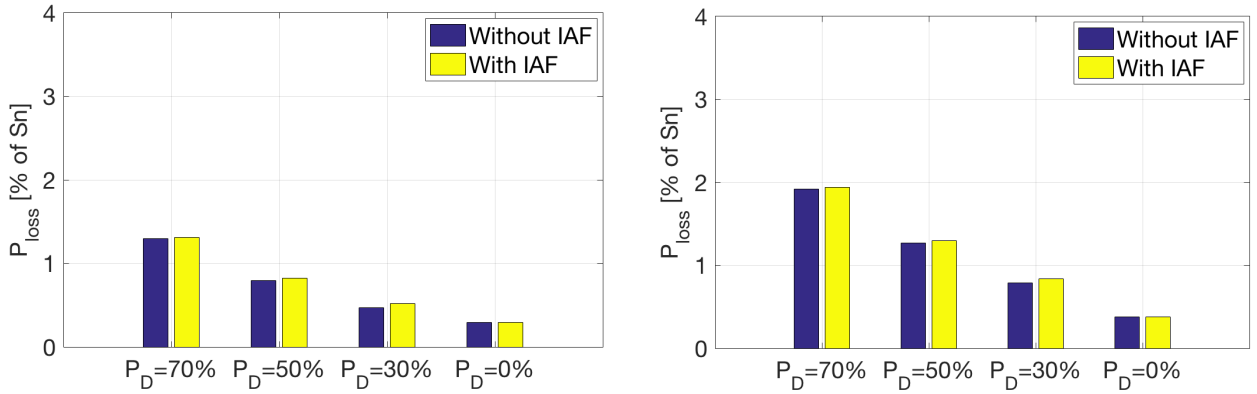
(a) i_C at $P_R = 0\%$ of Sn

(b) i_C at $P_R = 20\%$ of Sn

Figure 8.14: LCL-filter capacitor currents at minimum harmonic mitigation.

8.2.5 Power Losses

The LCL-filter power losses are given in Figure 8.15a ($P_R = 0\%$ of Sn) and 8.15b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.2, in Table C.8a and Table C.8b. As can be seen from the bar graphs, the power losses are strongly dependent on both P_D and P_R. Switching the IAF on has almost no effect on the total power losses. In the worst-case scenario, the power losses increase with 0.05% when operating at $P_D = 30\%$. The worst-case power losses are 1.94%, obtained when P_D and P_R are at their maximum. The no-load losses are 0.29% of Sn.



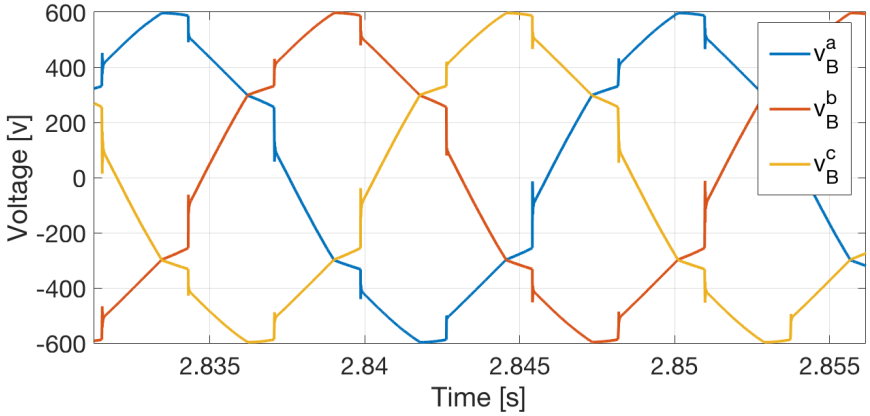
(a) P_{loss} at $P_R = 0\%$ of Sn

(b) P_{loss} at $P_R = 20\%$ of Sn

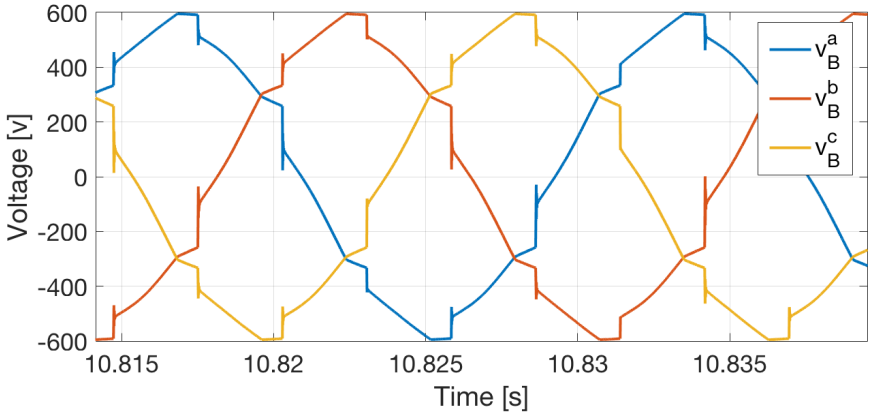
Figure 8.15: Power losses at minimum harmonic mitigation.

8.2.6 Worst Case Voltage Waveform and Frequency Spectrums

The worst-case voltage waveforms, i.e. $P_D = 70\%$ and $P_R = 0\%$ of Sn, are presented with and without the IAF in Figure 8.16a (THD = 9.34%) and Figure 8.16b (THD = 7.18%). The corresponding frequency spectrums for the above-mentioned waveforms are shown in Figure 8.17a and Figure 8.17b. The harmonics in these frequency spectrums matches the harmonic found in the Figures 8.11 .

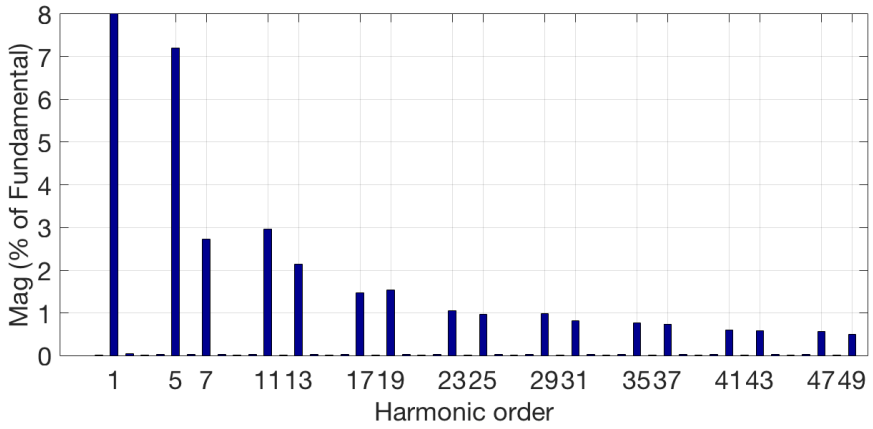


(a) IAF turned off resulting in a THD of 9.34%.

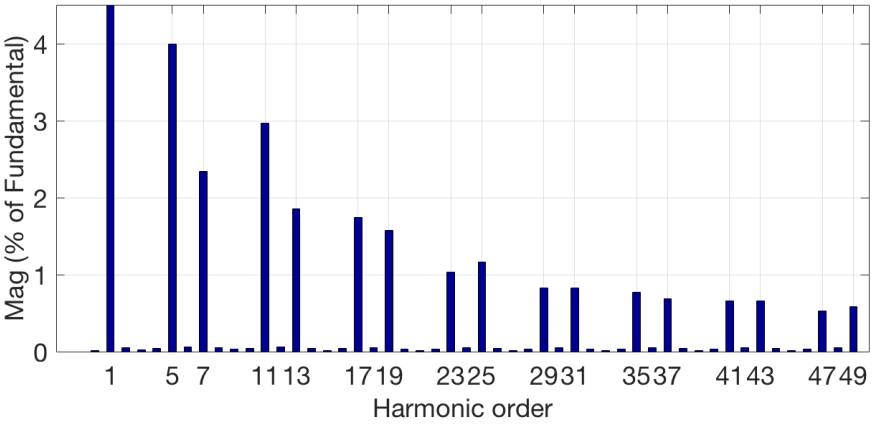


(b) IAF turned on resulting in a THD of 7.18%.

Figure 8.16: Voltage waveforms at minimum harmonic mitigation when $P_D = 70\%$ and $P_R = 0\%$.



(a) IAF turned off resulting in a THD of 9.34%. See corresponding waveform in Figure 8.16a.



(b) IAF turned on resulting in a THD of 7.18%. See corresponding waveform in Figure 8.16b.

Figure 8.17: Frequency spectrums at minimum harmonic mitigation when $P_D = 70\%$ and $P_R = 0\%$.

8.3 CASE 3: Proposed Harmonic Mitigation

Here, the proposed case of harmonic compensation is based on a maximum allowed RMS steady state capacitor phase current of 900A, which equals 0.6pu. The statement becomes:

$$i_{C,Max,RMS} \leq 900A = 0.6pu. \tag{8.2}$$

The numerical parameters applied in the simulations in this case are displayed in Table 8.3. The PI-regulator gains are equal for the different harmonic orders, except for the 5th order, where they are doubled. The DC-side capacitance C_D is increased from 45mF (in case 2) to 49mF. This case is divided into two parts; the case with a new capacitor (case 3a) and with an old capacitor (case 3b). The old capacitor has 80% of the capacitance of the new capacitor, and represents the end of life capacitance of the new capacitor. In the previous case, a LCL-filter capacitor of 3.8mF was chosen. This is just about in the middle of the new and old capacitances, making it easier to compare case 2 and 3 in terms of power losses and current magnitudes.

$Parameter$	$Value$
C_{new}	$4.25mF$
C_{old}	$3.4mF$
C_D	$49mF$
$K_{p_{5th}}$	127.8
$K_{i_{5th}}$	6666
$K_{p_{7th,11th,13th}}$	61.9
$K_{i_{7th,11th,13th}}$	3333

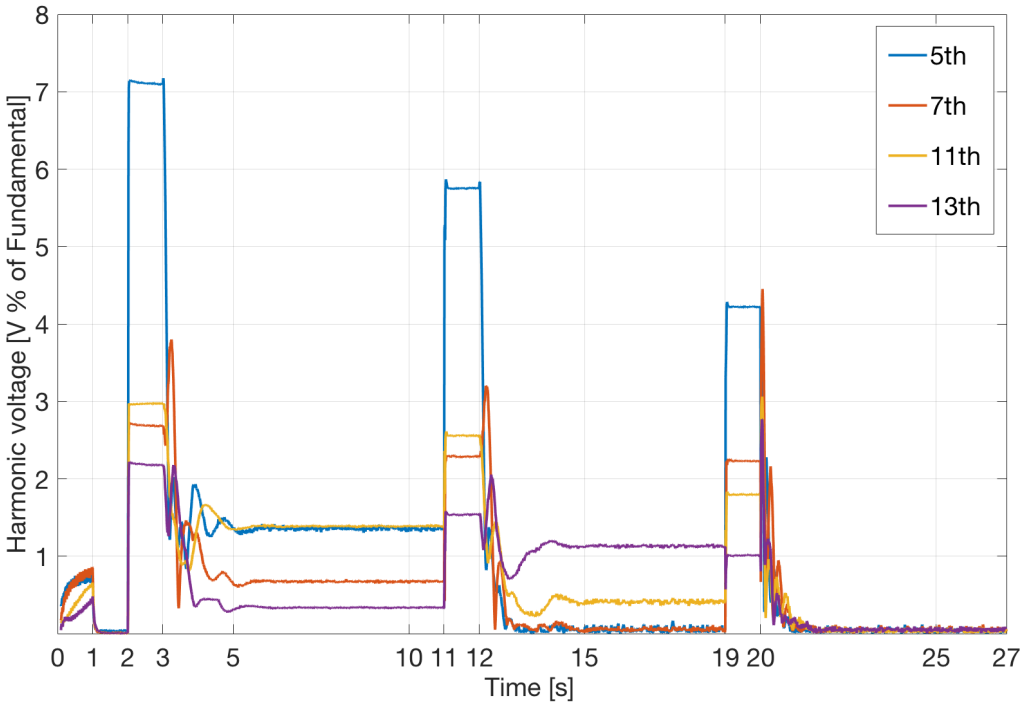
Table 8.3: Proposed harmonic mitigation parameters

With the new capacitor, a series resonance frequency of roughly 350Hz is obtained between the inductance (L_1) and the capacitor in the LCL-filter. The old capacitor gives a resonance frequency of approximately 390Hz. Since the 5th harmonic has a frequency of 300Hz and the 7th one of 420Hz, there is not much room for changing the capacitance of the new capacitor while avoiding resonance with the 5th or the 7th harmonics. Changing the capacitor so that the series resonance is higher than the 7th harmonic frequency of 420Hz has shown to be too close to the switching frequency. One is not able to sustain a stable system with a capacitance smaller than 3.4mF.

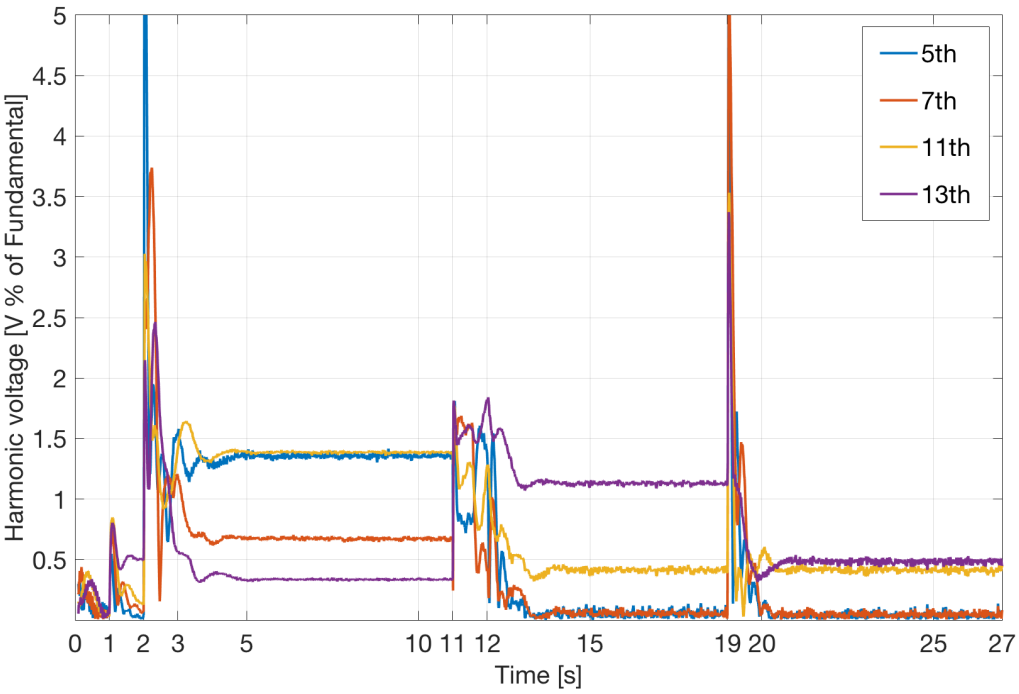
8.3.1 CASE 3a: New Capacitor

Mitigation of Harmonic Voltages

The capacitor is now brand new with a capacitance of 4.25mF. When it comes to the previous cases, the IAF performance is considered when P_R = 0% of Sn. Figure 8.18a represents the case where the IAF is periodically turned on, and Figure 8.18b represents the case where the filter is constantly turned on. The IAF performance when P_R = 20% of Sn shows negligible differences compared to the case where P_R = 0%. Therefore, the two graphs representing the case where P_R = 20% are placed in appendix D. From Figure 8.18a and 8.18b, it can be seen that none of the harmonic voltages exceed the magnitude of maximum 5% of the fundamental voltage when the IAF is turned on. In steady state, the four different harmonic voltages being dealt with are forced below 1.5% of the fundamental voltage in every mode of operation. When P_D = 50%, the 13th harmonic component is the largest contributor to the THD. Similar to case 2, the harmonic mitigation is dependent on memory when P_D = 30%. When the IAF is turned off, reset, and turned on again, like in Figure 8.18a, the filter is able to fully cancel all harmonics at P_D = 30%. When the IAF is constantly on, there are harmonic voltage components of orders 11th and 13th remaining. Otherwise, with P_D = 70% and P_D = 50%, the harmonic voltages are mitigated in a similar manner, regardless of the memory effect.



(a) Periodically turned on IAF. See Figure 8.2 for the turning on scheme.

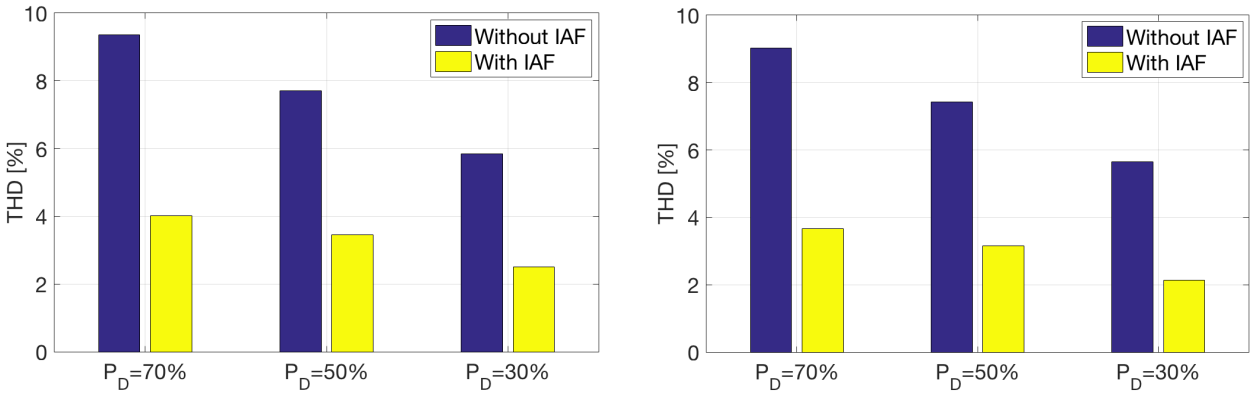


(b) Constantly turned on IAF.

Figure 8.18: Harmonic voltages at proposed harmonic mitigation with a new capacitor, $P_R^* = 0\%$ of Sn and P_D^* like shown in Figure 8.1.

THD

The THD levels obtained in this case are presented in Figure 8.19a ($P_R = 0\%$ of Sn) and 8.19b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.3.1, in Table C.9a and Table C.9b. With the IAF turned on, the THD never exceeds 4.02% in any steady state mode of operation. This is well below the maximum allowed THD.



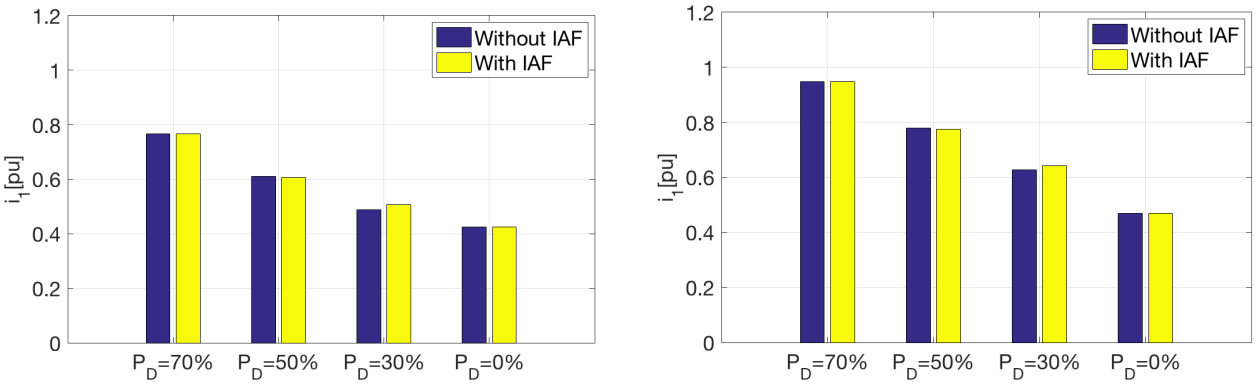
(a) THD at $P_R = 0\%$ of Sn

(b) THD at $P_R = 20\%$ of Sn

Figure 8.19: THD at proposed harmonic mitigation with a new capacitor.

Inverter Current

The inverter current i_1 is given in Figure 8.20a ($P_R = 0\%$ of Sn) and 8.20b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.3.1, in Table C.10a and Table C.10b. From the bar graphs, it can be seen that i_1 strongly depends on both P_D and P_R. The current i_1 shows little correlation with switching scheme of the IAF. At most, i_1 is approximately 0.95pu with the IAF switched on.



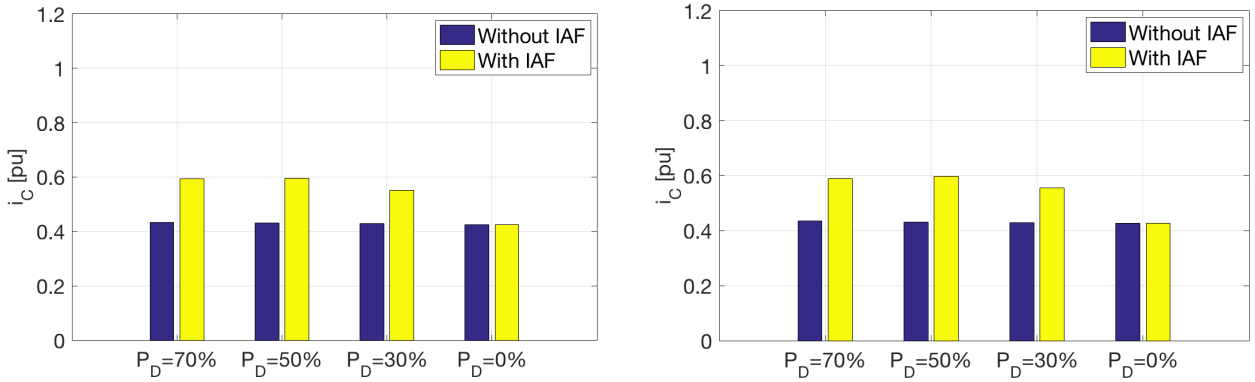
(a) i_1 at $P_R = 0\%$ of Sn

(b) i_1 at $P_R = 20\%$ of Sn

Figure 8.20: Inverter current at proposed harmonic mitigation with a new capacitor.

Capacitor Current

The capacitor current i_C is given in Figure 8.21a (P_R = 0% of Sn) and 8.21b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.3.1, in Table C.11a and Table C.11b. As can be seen from the graphs, i_C is almost independent of both P_D and P_R when the IAF is turned off. When the IAF is turned on, i_C is only dependent on P_D. The capacitor current has a maximum magnitude of 0.6pu, which was the limit in this case,see equation 8.2.



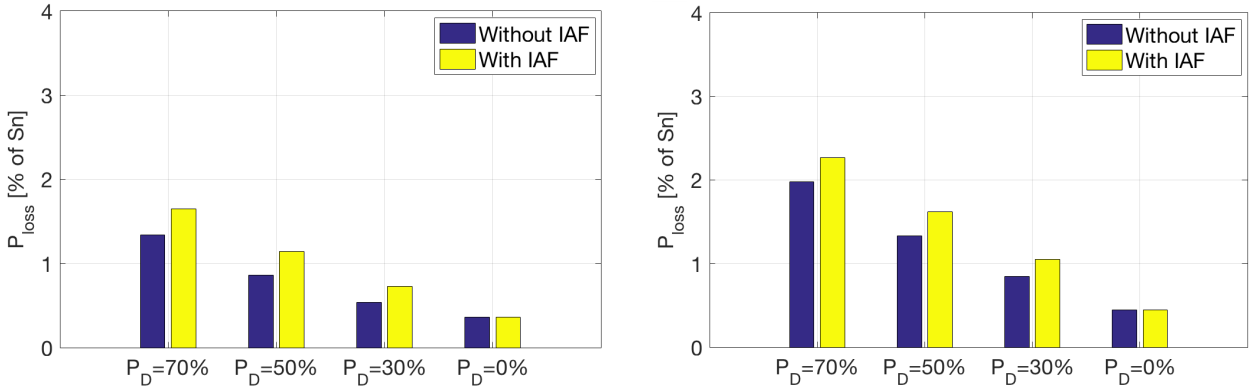
(a) i_C at P_R = 0% of Sn

(b) i_C at P_R = 20% of Sn

Figure 8.21: LCL-filter capacitor current at proposed harmonic mitigation with a new capacitor.

Power Losses

The LCL-filter power losses are given in Figure 8.22a (P_R = 0% of Sn) and 8.22b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.3.1, in Table C.12a and Table C.12b. As seen from the bar graphs, the power losses depend strongly on both P_D and P_R. Switching the IAF on increases the power losses with just about 0.3%. The worst-case power losses are 2.27%, obtained when P_D and P_R are at their maximum. The no-load losses are 0.36% of Sn.



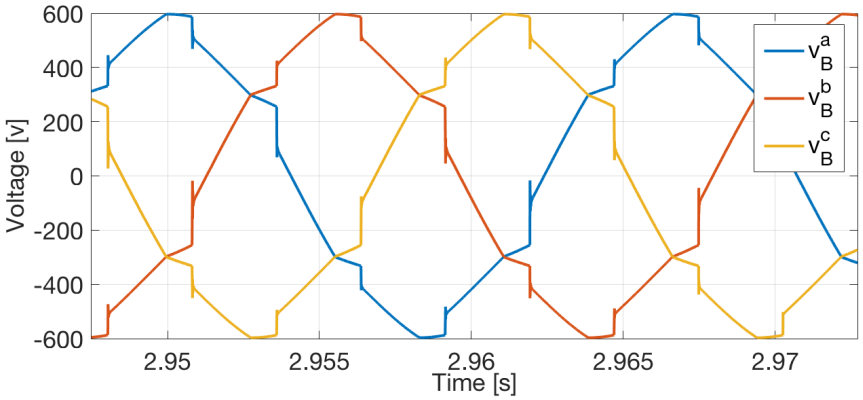
(a) P_{loss} at P_R = 0% of Sn

(b) P_{loss} at P_R = 20% of Sn

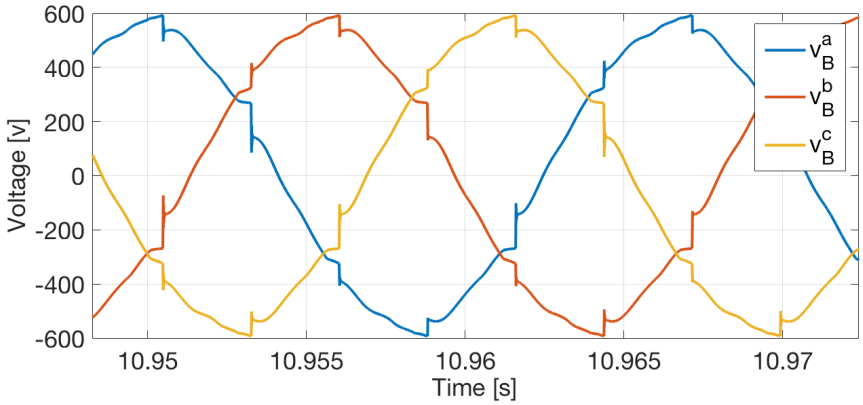
Figure 8.22: Power loss at proposed harmonic mitigation with a new capacitor.

Worst Case Voltage Waveform and Frequency Spectrums

The worst-case voltage waveform is presented with and without the IAF in Figure 8.23a (THD = 9.35%) and Figure 8.23b (THD = 4.02%). The corresponding frequency spectrums for the above-mentioned waveforms are shown in Figure 8.24a and Figure 8.24b. All harmonics in the filtered frequency spectrum are below 1.5% of the fundamental voltage and matches the Figures 8.18.

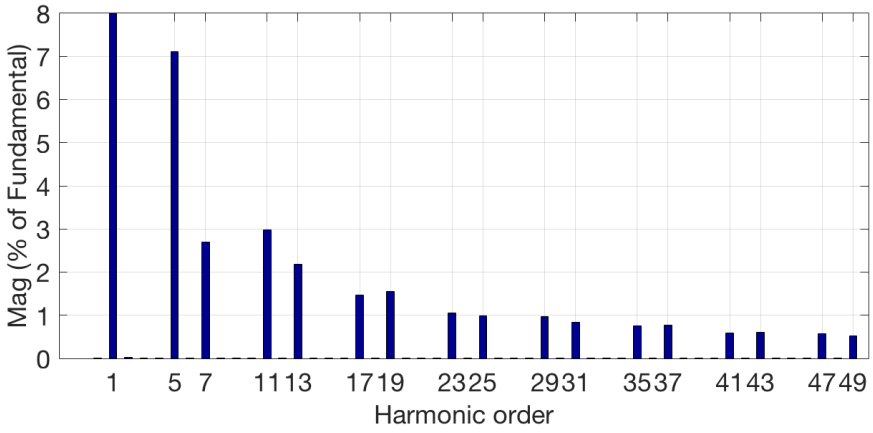


(a) IAF turned off resulting in a THD of 9.35%.

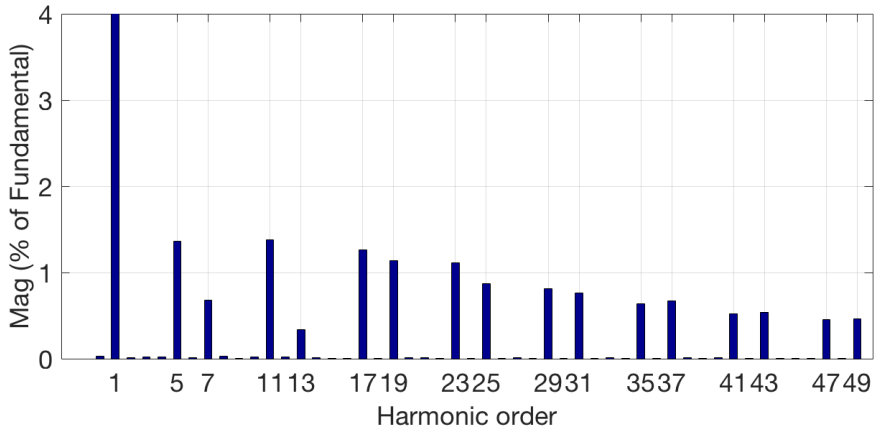


(b) IAF turned on resulting in a THD of 4.02%.

Figure 8.23: Voltage waveforms at proposed harmonic mitigation with a new capacitor, P_D = 70% and P_R = 0%.



(a) IAF turned off resulting in a THD of 9.35%. See corresponding waveform in Figure 8.23a.



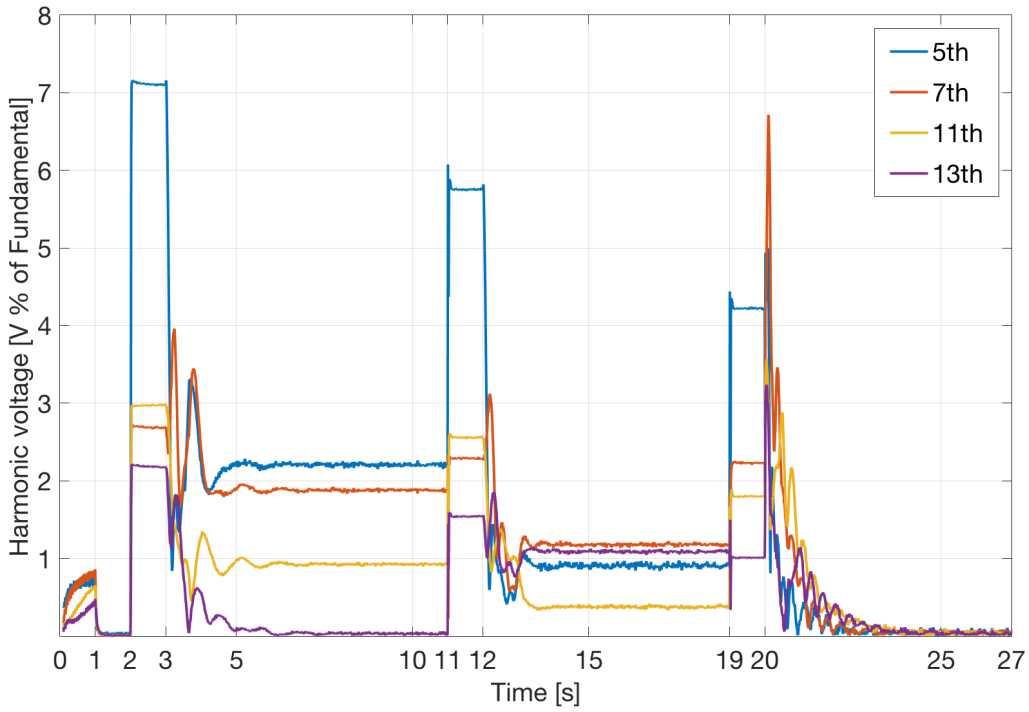
(b) IAF turned on resulting in a THD of 4.02%. See corresponding waveform in Figure 8.23b.

Figure 8.24: Frequency spectrums at proposed harmonic mitigation with a new capacitor, $P_D = 70\%$ and $P_R = 0\%$.

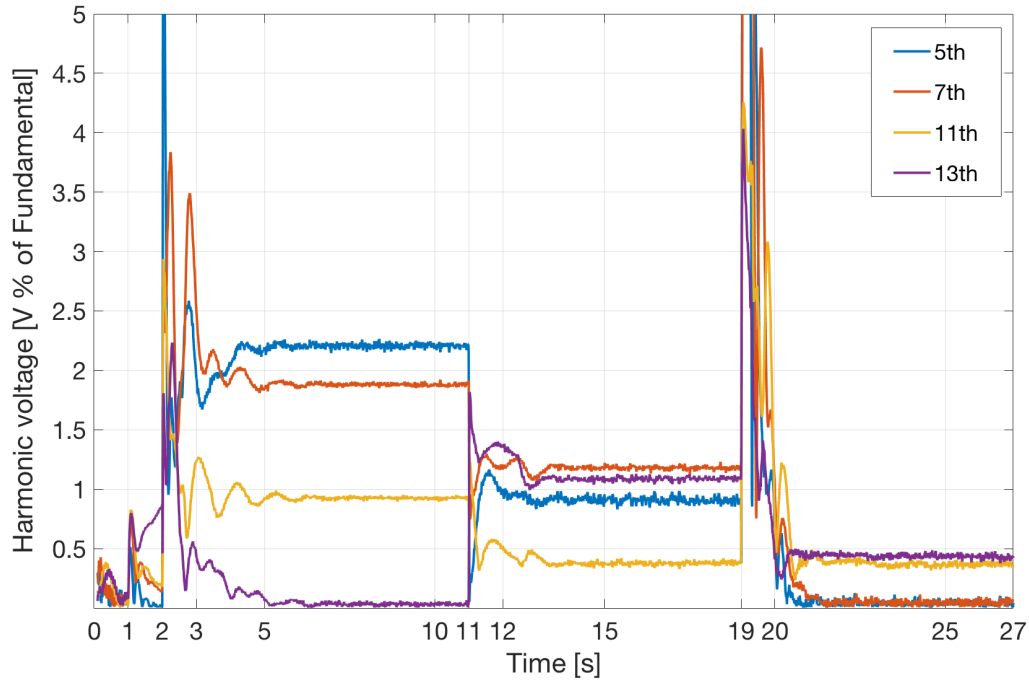
8.3.2 CASE 3b: Old Capacitor

In this case the capacitor is aged, with a capacitance of 3.4mF. As for the previous cases, the IAF performance is considered when $P_R = 0\%$ of Sn. Figure 8.25a represents the case with the IAF periodically turned on, and Figure 8.25b represents the case where the filter is constantly turned on. Like in the previous cases, the case where $P_R = 20\%$ of Sn shows negligible differences, compared to the case where $P_R = 0\%$. The two graphs representing the case where $P_R = 20\%$ are therefore placed in appendix D. From Figure 8.25a and Figure 8.25b, it can be seen that none of the harmonic voltages exceed the demand of maximum 5% of the fundamental voltage when the IAF is turned on. Compared to case 3a, when the new capacitor is present, the harmonic content has increased. In steady state, the four different harmonic voltages are forced below 2.5% in every mode of operation. Comparing this with a new capacitor, where the harmonics are forced below 1.5%, the difference is substantial. As in cases 2 and 3a, the harmonic mitigation depends on memory when $P_D = 30\%$. When the IAF is turned off, reset, and turned on again, like in Figure 8.25a, the filter is able to fully cancel all harmonics when $P_D = 30\%$. As for case 3a, when the IAF is constantly on, there are harmonic voltage components remaining of the 11th and 13th order. Otherwise, with $P_D = 70\%$ and $P_D = 50\%$, the harmonic voltages are similarly mitigated, regardless of the memory.

When the distorted power consumption is changed, the harmonic voltages start to fluctuate. Especially when stepping from $P_D = 50\%$ to $P_D = 30\%$, the IAF performs rather slow, with considerable fluctuations. It takes just about two seconds to properly stabilize the system after a 20% step in P_D. The harmonics are mitigated to acceptable magnitudes in roughly one second.



(a) Periodically turned on IAF. See figure 8.2 for the turning on scheme.

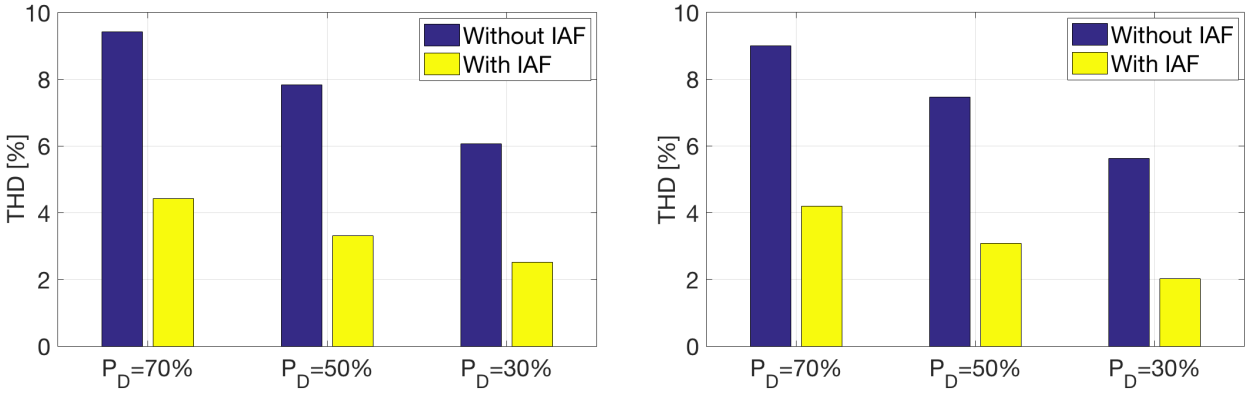


(b) Constantly turned on IAF.

Figure 8.25: Harmonic voltages at proposed harmonic mitigation with an old capacitor, $P_R^* = 0\%$ of Sn and P_D^* like shown in Figure 8.1.

THD

The THD levels obtained in this case are presented in Figure 8.26a (P_R = 0% of Sn) and Figure 8.26b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.3.2, in Table C.13a and Table C.13b. With the IAF, the THD will never exceed 4.43% in any steady state mode of operation. This is much lower than the maximum allowed THD, but higher than the 4.02% obtained with a new capacitor.



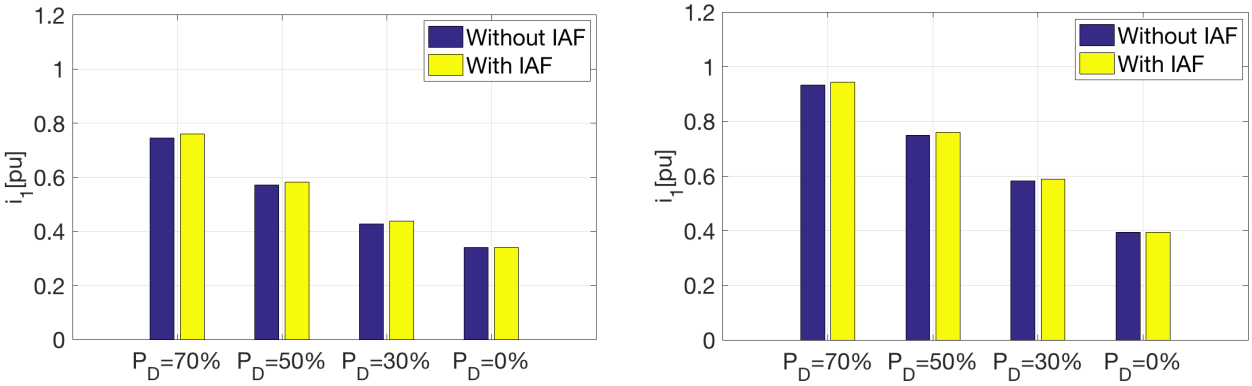
(a) THD at P_R = 0% of Sn

(b) THD at P_R = 20% of Sn

Figure 8.26: THD at proposed harmonic mitigation with an old capacitor.

Inverter Current

The inverter current i_1 is given in Figure 8.27a (P_R = 0% of Sn) and Figure 8.27b (P_R = 20% of Sn). The data behind these bar graphs can be viewed in appendix C.3.2, in Table C.14a and Table C.14b. From the bar graphs, it can be seen that i_1 strongly depends on both P_D and P_R. The current i_1 is not significantly dependent on whether the IAF is on or off. At most, i_1 is circa 0.94pu with the IAF switched on.



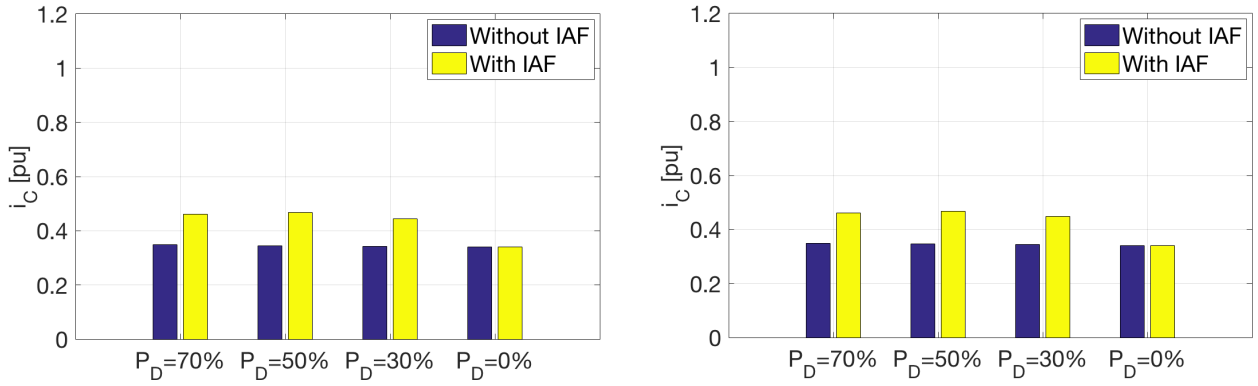
(a) i_1 at P_R = 0% of Sn

(b) i_1 at P_R = 20% of Sn

Figure 8.27: Inverter current at proposed harmonic mitigation with an old capacitor.

Capacitor Current

The capacitor current i_C is given in Figure 8.28a ($P_R = 0\%$ of Sn) and Figure 8.28b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.3.2, in Table C.15a and Table C.15b. As seen from the graphs, i_C is almost independent of both P_D and P_R when the IAF is turned off. When the IAF is turned on, i_C is only dependent on P_D. However, the current i_C is almost the same when $P_D = 70\%$ and $P_D = 50\%$. The capacitor current is maximum of 0.47pu in this case.



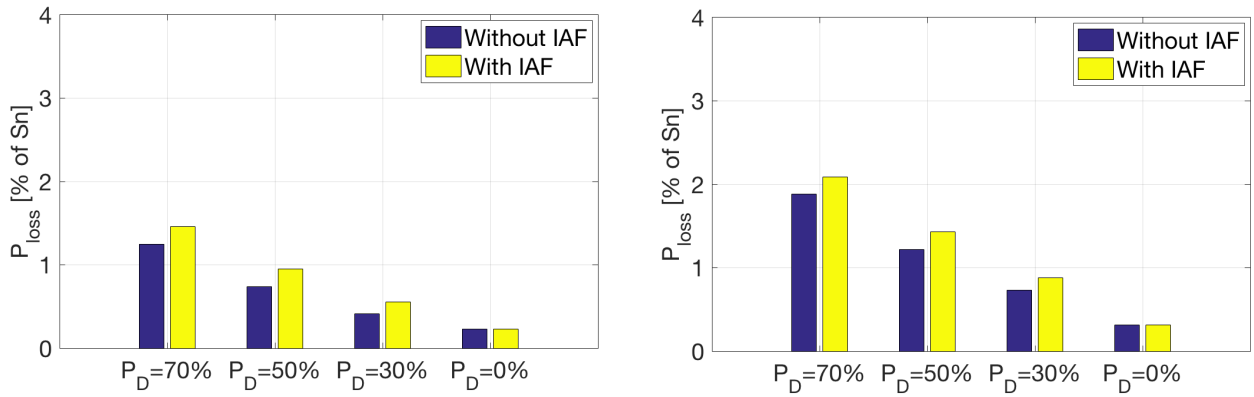
(a) i_C at $P_R = 0\%$ of Sn

(b) i_C at $P_R = 20\%$ of Sn

Figure 8.28: LCL-filter capacitor currents at proposed harmonic mitigation with an old capacitor.

Power Losses

The LCL-filter power losses are given in Figure 8.29a ($P_R = 0\%$ of Sn) and Figure 8.29b ($P_R = 20\%$ of Sn). The data behind these bar graphs can be viewed in appendix C.3.2, in Table C.16a and Table C.16b. As can be seen from the bar graphs, the power losses are strongly dependent on both P_D and P_R. Switching the IAF on increases the power losses with roughly 0.2% in the worst cases. The worst-case power losses are 2.09%, obtained when P_D and P_R are at their maximum. The no-load losses are 0.23% of Sn.



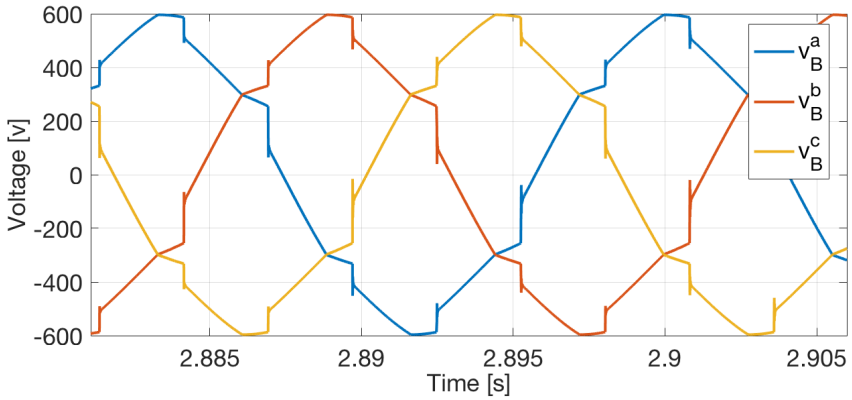
(a) P_{loss} at $P_R = 0\%$ of Sn

(b) P_{loss} at $P_R = 20\%$ of Sn

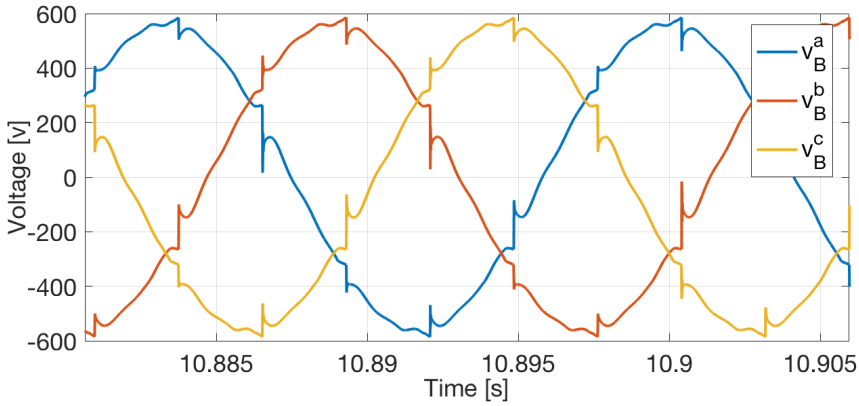
Figure 8.29: Power losses at proposed harmonic mitigation with an old capacitor.

Worst Case Voltage Waveform and Frequency Spectrums

The worst-case voltage waveform is presented with and without the IAF in Figure 8.30a (THD = 9.43%) and Figure 8.30b (THD = 4.43%). The corresponding frequency spectrums for the above-mentioned waveforms are shown in Figure 8.31a and 8.31b. All harmonics in the filtered frequency spectrum are below 2.3% of the fundamental voltage and match Figure 8.25.

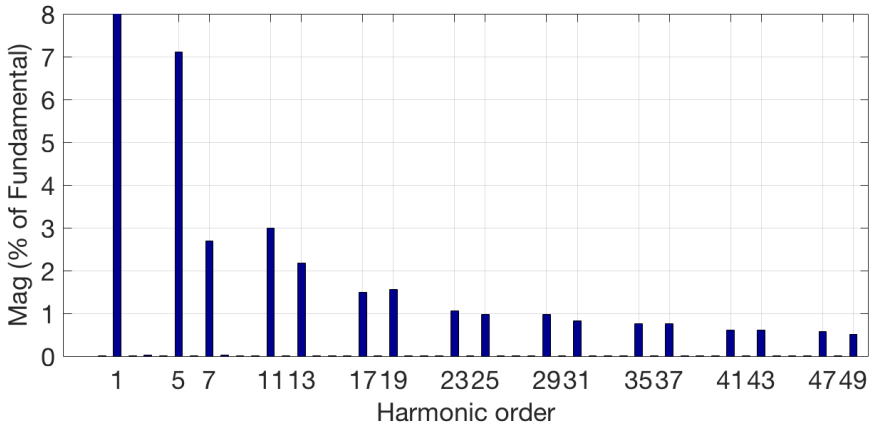


(a) IAF turned off resulting in a THD of 9.43%.

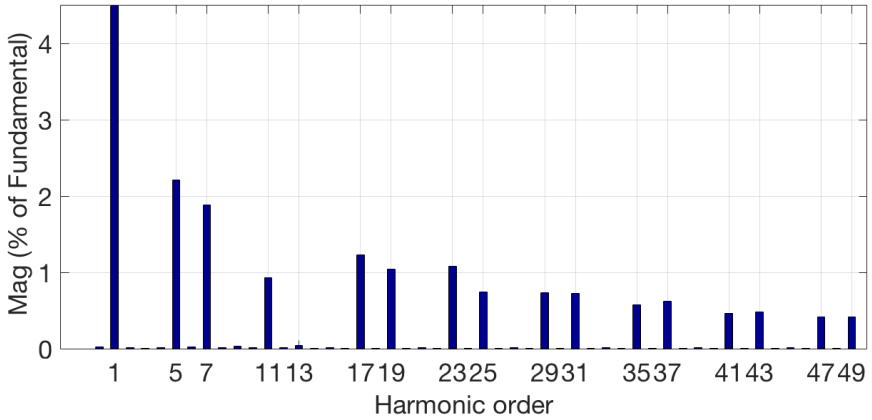


(b) IAF turned on resulting in a THD of 4.43%.

Figure 8.30: Voltage waveforms at proposed harmonic mitigation with an old capacitor, $P_D = 70\%$ and $P_R = 0\%$.



(a) IAF turned off resulting in a THD of 9.43%. See corresponding waveform in figure 8.30a.



(b) IAF turned on resulting in a THD of 4.43%. See corresponding waveform in Figure 8.30b.

Figure 8.31: Frequency spectrums at proposed harmonic mitigation with an old capacitor, P_D = 70% and P_R = 0%.

8.4 Discussion

A collection of the main findings in this thesis is shown in Table 8.4. The table contains the maximum quantities of THD, i_1, i_C and P_{loss} obtained for the cases investigated. In the maximum harmonic mitigation case, the harmonics of the 5th, 7th, 11th and 13th order are mitigated to negligible magnitudes, resulting in a worst-case THD of 3.44% at point B. However, this comes with a price, since currents and power losses are increased. In the worst case, the LCL-filter power losses reach 3.58%, with the no-load losses being 0.83%. This is considered to be too high, and measures should be taken to force these power losses down to acceptable levels. Both the currents i_1 and i_C are more than 1pu with the IAF turned on, operating in the worst-case scenario. Having a big inverter current places higher demands on the design of the inverter, and it leads to higher internal losses. As was discussed in section 4.3, decreasing the LCL-filter capacitance will decrease the magnitude of the LCL-filter currents. Nevertheless, a decrease of the capacitor size without the use of anti-windup makes the system unstable. The harmonic PI-regulators build up their modulator voltage signal, trying to completely cancel the harmonics. Fully cancelling the harmonics, with a slightly smaller capacitor than used in case 1, has shown itself to be physically impossible with the given system properties. Anti-windup in the PI-regulators is therefore needed in order to decrease the LCL-filter currents and power losses.

The minimum harmonic mitigation case shows the minimum power losses obtained in this thesis, see Table 8.4. The THD is 7.18% at worst, which is significantly higher than the 3.45% obtained in case 1. But the THD levels are still within the requirements from DNV. The power losses show a slight increase when switching on the IAF, resulting in a modest 1.94% at worst. The power losses in case 2 with the IAF turned on are significantly smaller than in case 1, both with and without the IAF turned on. This is because of the decreased LCL-filter capacitance, resulting in i_1 being lower than 1pu, and i_C being roughly 0.4pu in all situations. This also causes the no-load losses to be only 0.29%, which is low compared to the 0.83% in case 1. In general, the IAF in case 2 acts very fast, with minor fluctuations after transients.

The proposed harmonic mitigation case operates in the middle of case 1 and 2 in terms of mitigating harmonics. This case shows the importance of taking capacitor aging into consideration. Case 3 operates in the same area as case 2 considering the sizing of the filter capacitor. The IAF in case 3 is able to obtain a THD of 4.02% with a new capacitor, and 4.43% with an old one, using the same anti-windup settings. In general, we see that the THD increases as the capacitor ages. However, this case reaches even higher standards with a maximum THD of 5% and a single order contribution of maximum 3%. This standard is mostly used in systems operating with a voltage above 1kV [15]. The power losses are higher with a new capacitor compared to an old. The worst-case power losses are 2.27% with the new capacitor and 2.09% with the old capacitor, yielding an average of 2.18%. Comparing these losses with the 1.94% obtained in case 2, the increase is minimal. The increased losses mainly come from the increased capacitor current when turning the IAF

on. Seen from the Table 8.4, the capacitor current decreases from 0.600pu to 0.467pu when the capacitor ages. The inverter current is almost not effected by the capacitor aging and decreases from 0.947pu to 0.944pu. In case 3a we see, despite what one would expect, a minor decrease in the current i_1 for $P_D = 50\%$ and $P_D = 70\%$ when turning on the IAF.

	THD	i_1	i_C	P_{loss}
$CASE\,1$	3.44%	$1.142pu$	$1.097pu$	3.58%
$CASE\,2$	7.18%	$0.926pu$	$0.421pu$	1.94%
$CASE\,3a$	4.02%	$0.947pu$	$0.600pu$	2.27%
$CASE\,3b$	4.43%	$0.944pu$	$0.467pu$	2.09%

Table 8.4: Main findings.

Chapter 9

Conclusion

A power supply in a marine power system has been investigated in this thesis. The power supply supplies highly distorting hotel loads onboard a marine vessel. The focus has been pointed towards the active filter capability of the power supply integrated Voltage Source Inverter. This section contains the most important conclusions that have been drawn.

The distorting hotel load, representing components driven by VFDs, was modelled in two different ways, both having a diode rectifier supplying a DC-load being either an ohmic resistance or a controllable current source. There were found negligible differences between the two models in terms of the THD. Therefore, it was concluded that the modelling of hotel loads is representative of the actual hotel loads located onboard marine vessels.

A mathematical model of the system was built in order to investigate system properties in terms of harmonic frequency and LCL-filter capacitor sizes. Due to the system properties found, it was decided only to focus on cancelling the 5th, 7th, 11th and the 13th harmonic orders. An Integrated Active Filter based on the selective harmonic mitigation method was developed in order to mitigate the harmonics dealt with. Three different cases were simulated, with various degree of harmonic mitigation.

Case 1 was simulated with the aim of totally cancelling the four harmonics dealt with. The IAF showed great performance with the ability to mitigate the relevant harmonics to negligible magnitudes. A satisfying worst-case THD of 3.44% was obtained, which is far better than the requirement of 8%. The worst-case power losses were at 3.58%, caused by increased system currents, which in this case were concluded to be too high.

Case 2 was simulated with the aim of fulfilling the THD requirements with a limited margin. Only the 5th and the 7th harmonics were dealt with in this case. Anti-windup of the PI-regulators made it possible to partly mitigate the harmonics dealt with and to reduce the size of the LCL-filter capacitor. This case shows small worst-case power losses of 1.94% caused by small system currents, which again are caused by the smaller capacitor and the limited degree of harmonic mitigation. Due to the limited harmonic mitigation, a worst-case THD of 7.18% was obtained.

Case 3 proposes a harmonic mitigation well within the THD requirements while still obtaining

small power losses. This case is divided into two, simulating the system with a new and an old LCL-filter capacitor. When the the LCL-filter capacitor ages, the capacitance decreases. During aging, the THD increases and the power losses decrease. The decrease in power losses is brought on by a decreasing current when the capacitance gets smaller. An overall worst-case THD of 4.43% is obtained, with worst-case power losses of 2.27% of Sn.

The active filter capability of the Voltage Source Inverter is sufficient to mitigate the systems harmonic distortion to magnitudes well within the requirements. If one is willing to increase the power losses by maximum 0.3% of Sn, the worst-case THD drops from 9.33% to 4.43% using the IAF setup in case 3.

9.1 Recommendation for Further Work

The results are strongly dependent on the parameter data, further research should therefore put more efforts into obtaining more precise estimations of the system parameters. An investigation of the AC-side capacitors available in the market should be made. New simulations based on the chosen capacitor are encouraged in order to make sure that the system is stable and that the wanted degree of harmonic mitigation is obtained. It is important to know the state of the capacitor, and a control routine is recommended in order to prevent the capacitance of reaching devastating values.

The worst-case VSI power losses should be investigated in order to find the total power losses in the power supply. These power losses, and how they are affected by the rate of harmonic mitigation, should be taken into account when deciding the desired degree of harmonic mitigation in the system. The total power losses are also needed in order to design a suitable cooling system onboard the vessel.

All cases have been simulated with a sample time of $5 \cdot 10^{-6} s$. The digital signal controllers offering control-oriented peripherals like PWM are not able to operate with a sample time as low as simulated. Therefore, the control systems applied should, in the simulations, be separated from the system with rate transition blocks. This enables for a lower sampling time in the control system while still obtaining the high simulation sampling time accuracy of the simulation. A lower sampling time in the control system could influence the harmonics in the system. An investigation should be performed to address this matter. This can also be an interesting step in view of a lab scale validation, for example with a Hardware in the loop approach.

It is encouraged to consider the possibilities for using other VSI attached passive filters, such as the C-type and the LCLCL-filter.

Appendix A

Acronyms

AC Alternating Current.

APF Active Power Filters.

CSI Current Source Inverter.

DC Direct Current.

DNV Det Norske Veritas.

IAF Integrated Active Filter.

ICC Inner Current Control.

OVC Outer Voltage Control.

PI Proportional Integral.

pu Per Unit.

RMS Root Mean Square.

THD Total Harmonic Distortion.

VFD Variable Frequency Drive.

VSC Voltage Source Converter

VSI Voltage Source Inverter.

Appendix B

Park Transform

The amplitude invariant Park transform [31]:

$$\vec{x}^{dq} = P\vec{x}^{abc} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} x^a \\ x^b \\ x^c \end{bmatrix} \tag{B.1}$$

Figure B.1: The amplitude invariant Park transformation matrix

The inverse amplitude invariant Park transform [31]:

$$\vec{x}^{abc} = P^{-1}\vec{x}^{dq} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \times \begin{bmatrix} x^d \\ x^q \\ x^0 \end{bmatrix} \tag{B.2}$$

Figure B.2: The inverse amplitude invariant Park transformation matrix

The amplitude invariant negative sequence Park transform:

$$\vec{x}^{dq} = P_{neg}\vec{x}^{abc} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\cos\left(\theta - \frac{2\pi}{3}\right) & -\cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} x^a \\ x^b \\ x^c \end{bmatrix} \tag{B.3}$$

Figure B.3: The amplitude invariant negative sequence Park transformation matrix

The inverse amplitude invariant negative sequence Park transform:

$$\vec{x}^{abc} = P_{neg}^{-1}\vec{x}^{dq} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ -\cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ -\cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \times \begin{bmatrix} x^d \\ x^q \\ x^0 \end{bmatrix} \tag{B.4}$$

Figure B.4: The inverse amplitude invariant negative sequence Park transformation matrix

Appendix C

DATA

The bar graphs in chapter 8 are made based on the data presented in the following four pages. The data is presented in the order as follows:

1. CASE 1.
2. CASE 2.
3. CASE 3a (New capacitor).
4. CASE 3b (Old capacitor).

C.1 Case 1: Maximum Harmonic Mitigation

IAF	P_D [$\%ofS_n$]		
	70%	50%	30%
Off	9.33%	7.73%	5.90%
On	3.44%	3.08%	2.55%

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]		
	70%	50%	30%
Off	9.01%	7.41%	5.64%
On	2.94%	2.69%	2.18%

(b) $P_R = 20\%$.

Table C.1: THD [% of fundamental].

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.864	0.747	0.668	0.644
On	0.991	0.837	0.733	0.644

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	1.026	0.888	0.775	0.674
On	1.142	0.970	0.835	0.674

(b) $P_R = 20\%$.

Table C.2: Inverter current i_1 [pu].

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.655	0.653	0.649	0.644
On	1.080	0.953	0.831	0.644

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.657	0.654	0.651	0.645
On	1.097	0.966	0.838	0.645

(b) $P_R = 20\%$.

Table C.3: LCL-filter capacitor current i_C [pu].

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	1.75%	1.28%	0.98%	0.83%
On	2.90%	2.02%	1.39%	0.83%

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	2.38%	1.75%	1.30%	0.91%
On	3.58%	2.53%	1.73%	0.91%

(b) $P_R = 20\%$.

Table C.4: LCL-filter power losses [% of Sn].

C.2 Case 2: Minimum Harmonic Mitigation

IAF	P_D [$\%ofS_n$]		
	70%	50%	30%
Off	9.34%	7.71%	5.89%
On	7.18%	5.31%	3.96%

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]		
	70%	50%	30%
Off	9.01%	7.44%	5.66%
On	6.94%	5.11%	3.56%

(b) $P_R = 20\%$.

Table C.5: THD [% of fundamental].

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.756	0.591	0.456	0.382
On	0.745	0.585	0.441	0.382

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.939	0.763	0.604	0.432
On	0.926	0.757	0.591	0.432

(b) $P_R = 20\%$.

Table C.6: Inverter current i_1 [pu].

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.389	0.387	0.385	0.382
On	0.401	0.403	0.419	0.382

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	0.391	0.389	0.387	0.385
On	0.406	0.404	0.421	0.385

(b) $P_R = 20\%$.

Table C.7: LCL-filter capacitor current i_C [pu].

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	1.30%	0.79%	0.47%	0.29%
On	1.31%	0.82%	0.52%	0.29%

(a) $P_R = 0\%$.

IAF	P_D [$\%ofS_n$]			
	70%	50%	30%	0%
Off	1.92%	1.27%	0.79%	0.38%
On	1.94%	1.30%	0.84%	0.38%

(b) $P_R = 20\%$.

Table C.8: LCL-filter power losses [% of Sn].

C.3 Case 3: Proposed Harmonic Mitigation

C.3.1 New Capacitor

IAF	P_D [%ofS_n]		
	70%	50%	30%
Off	9.35%	7.70%	5.85%
On	4.02%	3.45%	2.50%

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]		
	70%	50%	30%
Off	9.03%	7.42%	5.65%
On	3.67%	3.16%	2.13%

(b) $P_R = 20\%$.

Table C.9: THD [% of fundamental].

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.767	0.611	0.488	0.426
On	0.767	0.607	0.507	0.426

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.948	0.779	0.627	0.469
On	0.947	0.775	0.643	0.469

(b) $P_R = 20\%$.

Table C.10: Inverter current i_1 [pu].

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.433	0.431	0.429	0.426
On	0.593	0.595	0.551	0.426

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.435	0.432	0.429	0.427
On	0.590	0.600	0.556	0.427

(b) $P_R = 20\%$.

Table C.11: LCL-filter capacitor current i_C [pu].

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	1.34%	0.86%	0.54%	0.36%
On	1.65%	1.14%	0.73%	0.36%

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	1.98%	1.33%	0.85%	0.44%
On	2.27%	1.62%	1.05%	0.44%

(b) $P_R = 20\%$.

Table C.12: LCL-filter power losses [% of Sn].

C.3.2 Old Capacitor

IAF	P_D [%ofS_n]		
	70%	50%	30%
Off	9.43%	7.89%	6.07%
On	4.43%	3.31%	2.52%

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]		
	70%	50%	30%
Off	9.01%	7.47%	5.63%
On	4.20%	3.08%	2.03%

(b) $P_R = 20\%$.

Table C.13: THD [% of fundamental].

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.745	0.572	0.428	0.341
On	0.761	0.582	0.438	0.341

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.931	0.749	0.583	0.394
On	0.944	0.759	0.589	0.394

(b) $P_R = 20\%$.

Table C.14: Inverter current i_1 [pu].

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.348	0.345	0.343	0.341
On	0.462	0.467	0.443	0.341

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	0.348	0.346	0.344	0.341
On	0.461	0.467	0.448	0.341

(b) $P_R = 20\%$.

Table C.15: LCL-filter capacitor current i_C [pu].

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	1.25%	0.74%	0.41%	0.23%
On	1.46%	0.95%	0.56%	0.23%

(a) $P_R = 0\%$.

IAF	P_D [%ofS_n]			
	70%	50%	30%	0%
Off	1.88%	1.22%	0.73%	0.31%
On	2.09%	1.43%	0.88%	0.31%

(b) $P_R = 20\%$.

Table C.16: LCL-filter power losses [% of Sn].

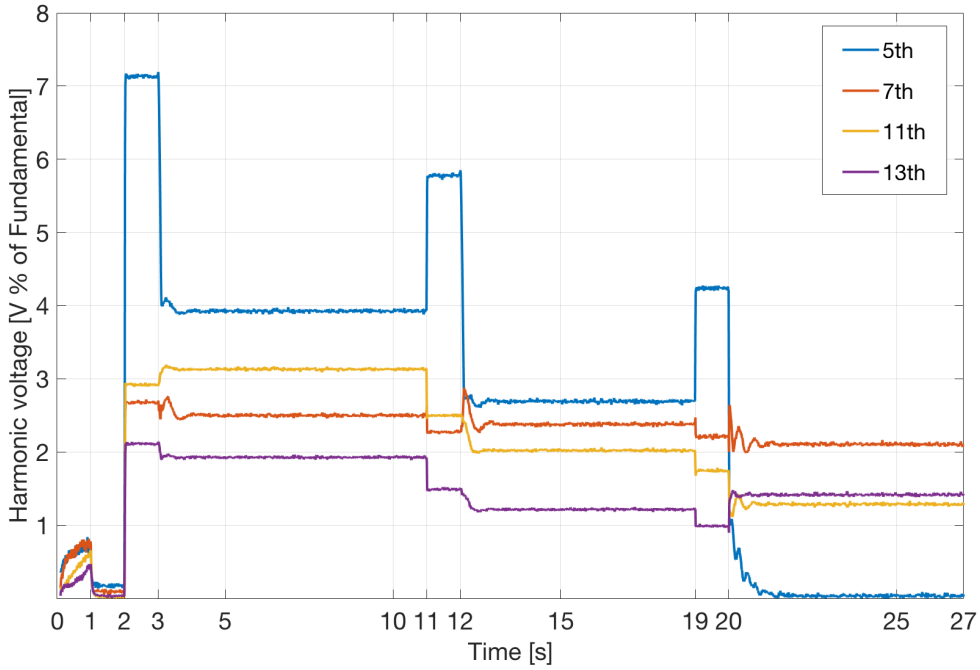
Appendix D

Additional Figures

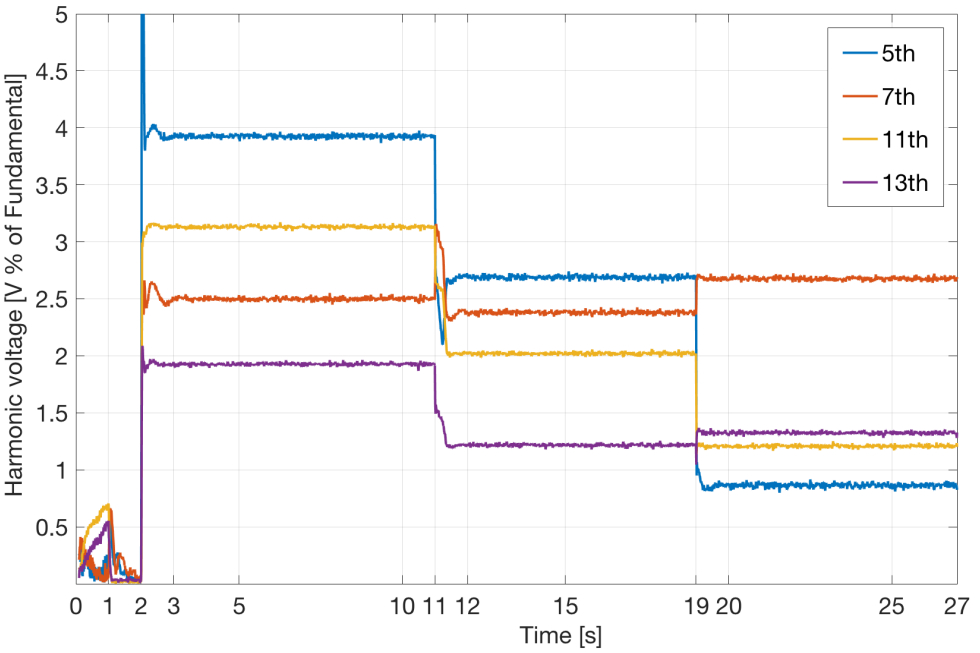
The following three phages contains additional figures for cases two and three. They are presented in the order as listed:

1. CASE 2: Minimum Harmonic Mitigation.
2. CASE 3a: Proposed Harmonic Mitigation with New Capacitor.
3. CASE 3b: Proposed Harmonic Mitigation with Old Capacitor.

D.1 CASE 2: Minimum Harmonic Mitigation.



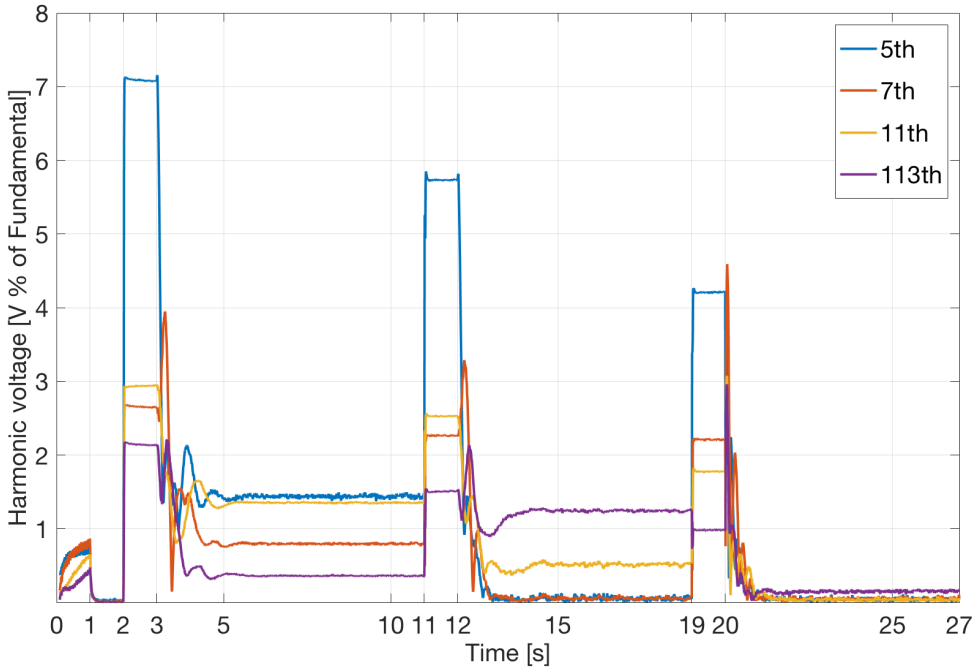
(a) Periodically turned on IAF. See Figure 8.2 for the turning on scheme.



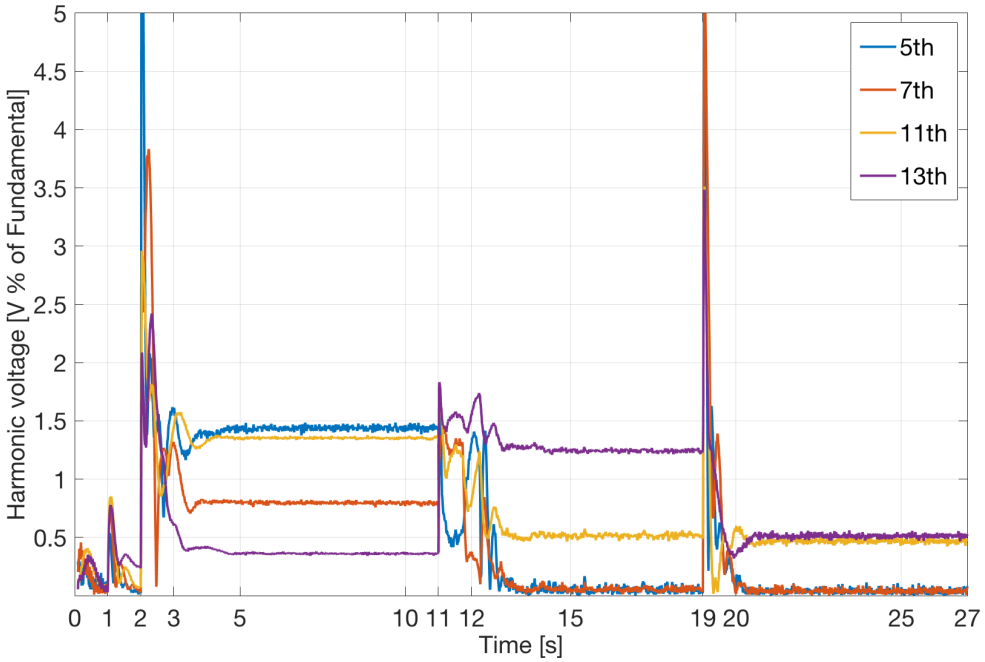
(b) Constantly turned on IAF.

Figure D.1: Harmonic voltages at minimum harmonic mitigation when $P_R^* = 20\%$ and P_D^* like shown in Figure 8.1. The IAF is only acting on the 5th and the 7th harmonic orders.

D.2 CASE 3a: Proposed Harmonic Mitigation with New Capacitor.



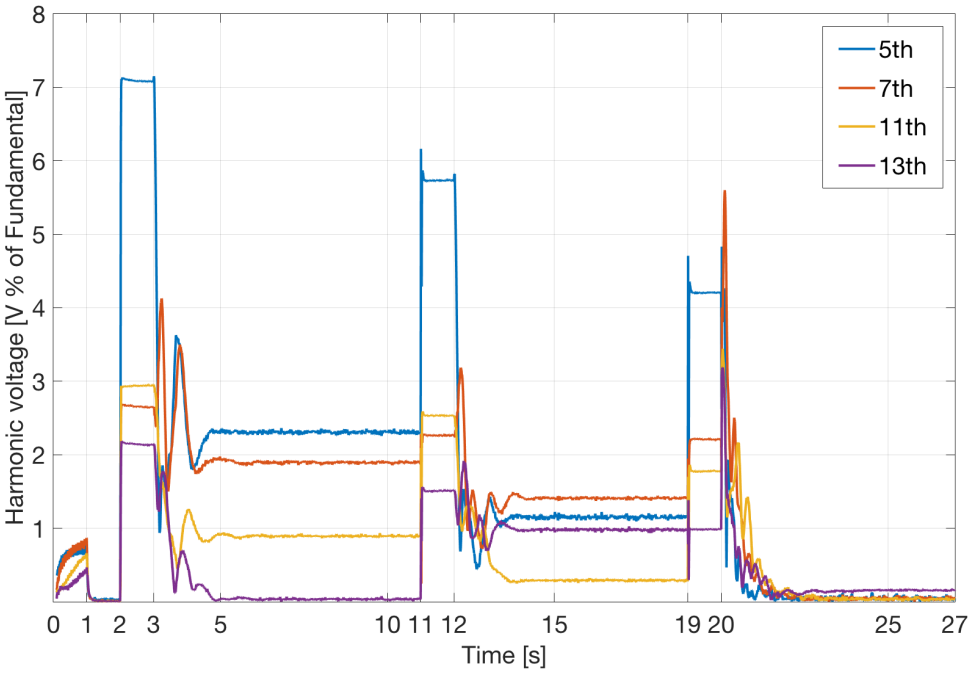
(a) Periodically turned on IAF. See Figure 8.2 for the turning on scheme.



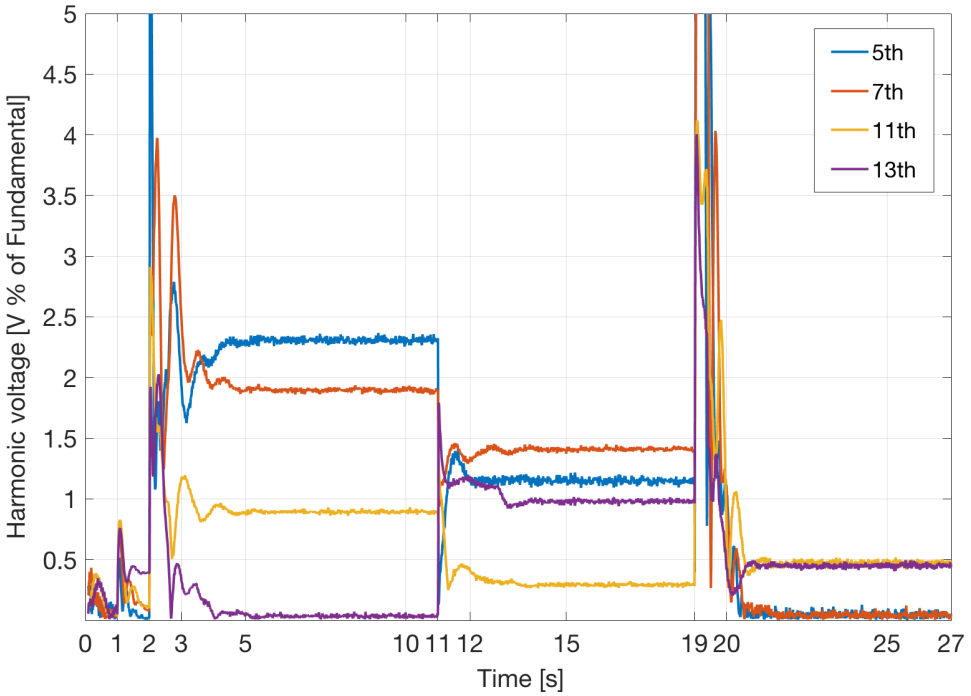
(b) Constantly turned on IAF.

Figure D.2: Harmonic voltages at proposed harmonic mitigation with a new capacitor, $P_R^* = 20\%$ of Sn and P_D^* like shown in Figure 8.1.

D.3 CASE 3b: Proposed Harmonic Mitigation with Old Capacitor.



(a) Periodically turned on IAF. See Figure 8.2 for the turning on scheme.



(b) Constantly turned on IAF.

Figure D.3: Harmonic voltages at proposed harmonic mitigation with an old capacitor, $P_R^* = 20\%$ of Sn and P_D^* like shown in Figure 8.1.

Appendix E

Simulink Models

Screenshots of the most important simulink models are presented in the following pages, in the order as listed:

1. Verification of state space model.
2. Voltage controlled harmonic mitigation.
3. Selective harmonic voltage controller.
4. Distorting load.

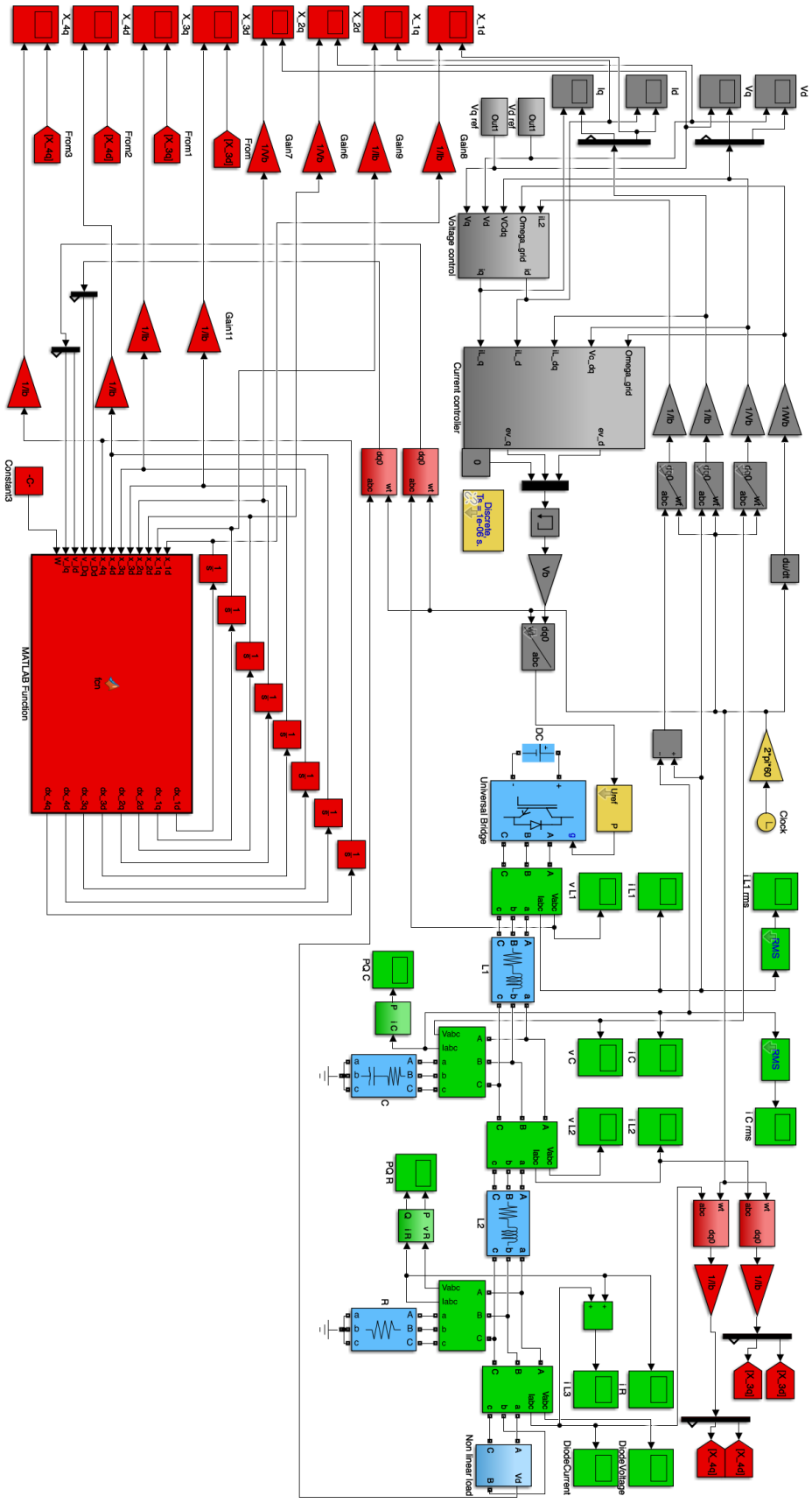


Figure E.1: Simulink model used to verify the state space model.

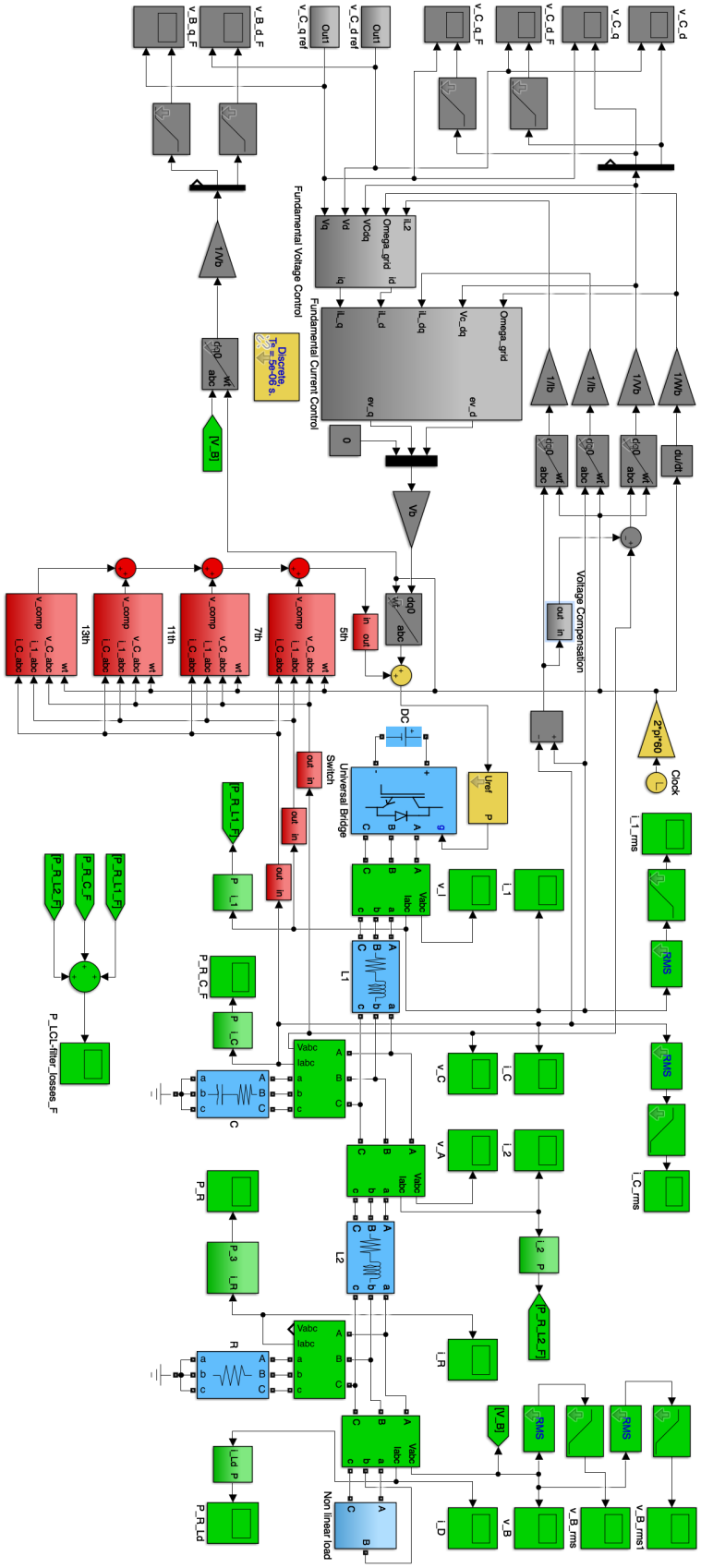


Figure E.2: Voltage controlled harmonic mitigation.

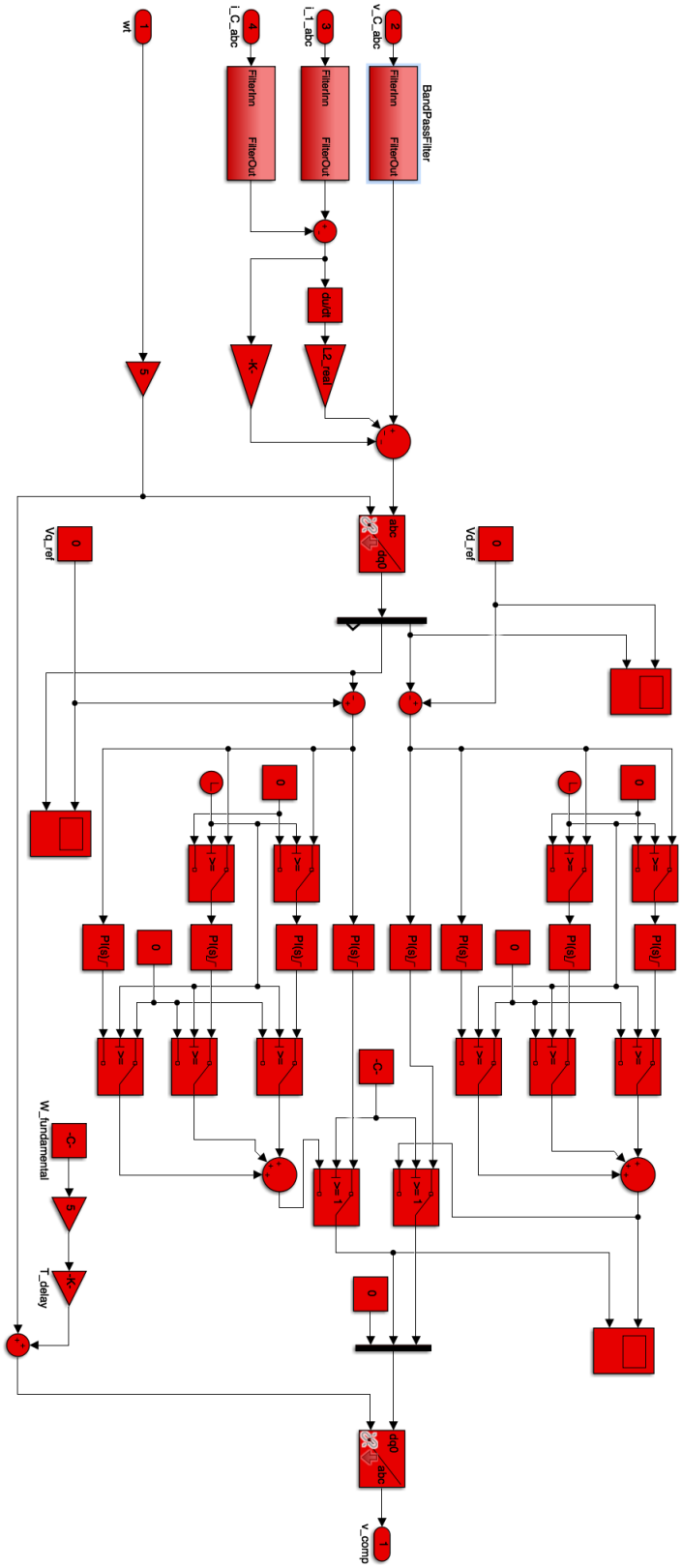


Figure E.3: Selective harmonic voltage controller.

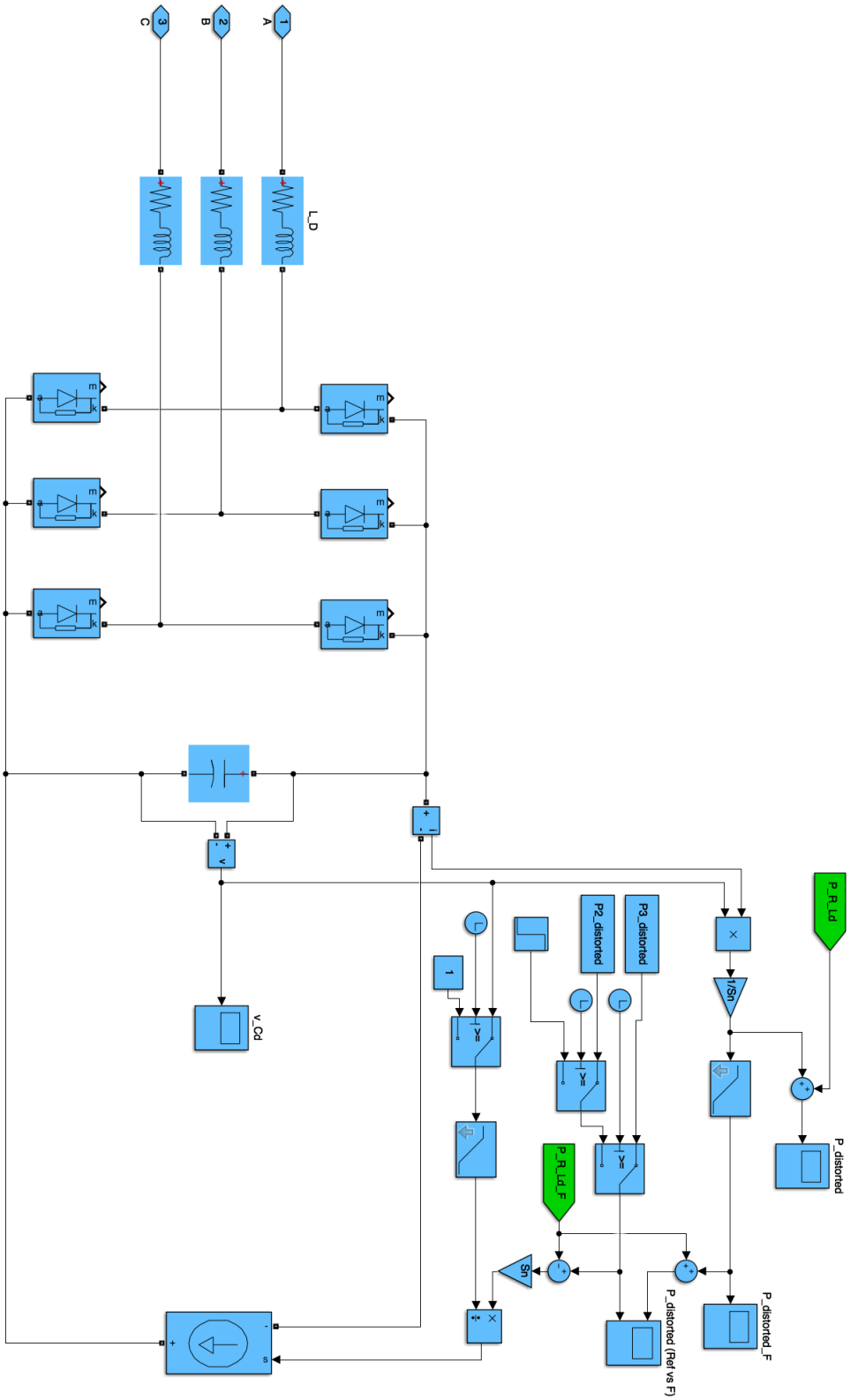


Figure E.4: Distorted load.

Appendix F

Supplementary

F.1 Total Harmonic Distortion

The total harmonic distortion THD is found from the following formula [32]:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} X_h^2}}{X_1} \tag{F.1}$$

The THD describes the amount of harmonic distortion in a signal. All the harmonics are summarized and compared to the amount of the fundamental frequency.

F.2 Second Order Band-pass

Since we are using the selective harmonic cancellation method we need filters that are able to filter out a single harmonic order. For each harmonic order we want a specific bandpass filter to let one harmonic order through. The tuning frequencies of the different band-pass filters should therefore be chosen as the harmonic frequency we want to pass through. The band-pass filters damping coefficients are chosen by locking at the frequency response of all the bans-pass filters at once. The obtained 5th, 7th, 11th and 13th band-pass filter frequency responses is shown in Figure F.1. Seen from the figure, the different frequency responses has a very limited impact on each other. The 5th harmonic band-pass filter shows a frequency response of less then -40dB on the 7th harmonic. The cancellation of the neighbouring harmonic orders shows all a frequency response of less then -40dB. The different damping coefficients are listed in Tabule F.1. For the band-pass filter transfer function, see equation F.2.

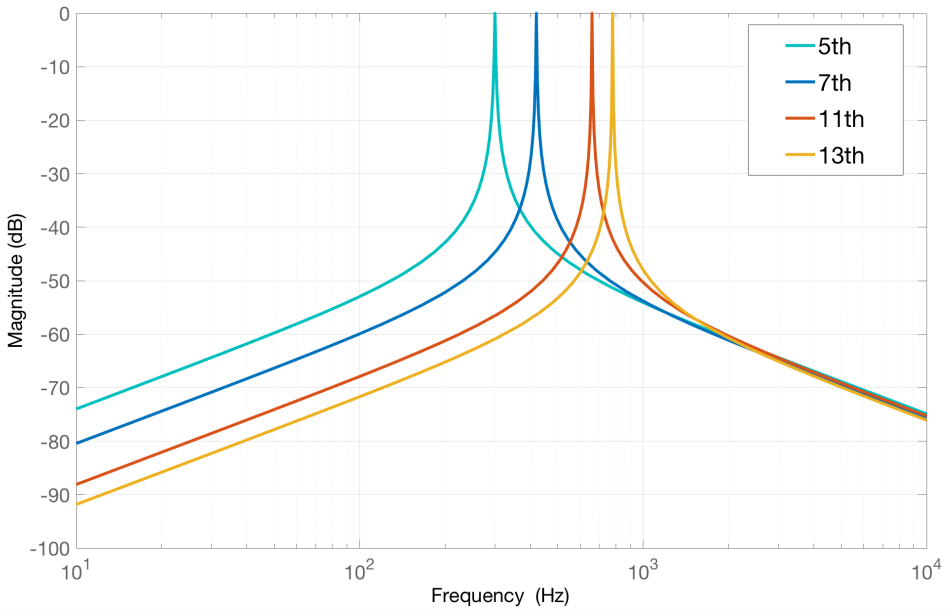


Figure F.1: Bode diagram of second order band-pass filters

ζ_{5th}	0.003
ζ_{7th}	0.002
ζ_{11th}	0.0013
ζ_{13th}	0.001

Table F.1: Band-pass filter damping coefficients

$$H(s) = \frac{2\zeta\omega_c s}{s^2 + 2\zeta\omega_c s + \omega_c^2} \tag{F.2}$$

Bibliography

[1] J. P.; Anderson B. A.; Corbett J. J.; Faber J.; Hanayama S.; O'Keeffe E.; Parker S.; Johansson L.; Aldous L.; Raucci C.; Traut M.; Ettinger S.; Nelissen D.; Lee D. S.; Ng S.; Agrawal A.; Winebrake J. J.; Hoen M.; Chesworth S.; Pandey A Smith, T. W. P.; Jalkanen. Third imo ghg study 2014; international maritime organization (imo). Technical report, IMO.

[2] S. D. Sudhoff. Currents of change. *IEEE Power and Energy Magazine*, 9(4):30–37, July 2011. ISSN 1540-7977. doi: 10.1109/MPE.2011.941319.

[3] J. M. Prousalidis, G. J. Tsekouras, and F. Kanellos. New challenges emerged from the development of more efficient electric energy generation units. In *2011 IEEE Electric Ship Technologies Symposium*, pages 374–381, April 2011. doi: 10.1109/ESTS.2011.5770901.

[4] J. S. Thongam, M. Tarbouchi, A. F. Okou, D. Bouchard, and R. Beguenane. All-electric ships x2014;a review of the present state of the art. In *2013 Eighth International Conference and Exhibition on Ecological Vehicles and Renewable Energies (EVER)*, pages 1–8, March 2013. doi: 10.1109/EVER.2013.6521626.

[5] Vegard Flatjord. Investigation of harmonic distortion in marine power systems. Specialisation project, NTNU, Trondheim, December 2016.

[6] J. F. Hansen and F. Wendt. History and state of the art in commercial electric ship propulsion, integrated power systems, and future trends. *Proceedings of the IEEE*, 103(12):2229–2242, Dec 2015. ISSN 0018-9219. doi: 10.1109/JPROC.2015.2458990.

[7] Jan F. Hansen, John O. Lindtjørn, Tor-Arne. Myklebust, and Vänskä Klaus. Onboard dc grid, the newest design for marine power and propulsion systems. 2011.

[8] H. Lotfi and A. Khodaei. Ac versus dc microgrid planning. *IEEE Transactions on Smart Grid*, 8 (1):296–304, Jan 2017. ISSN 1949-3053. doi: 10.1109/TSG.2015.2457910.

[9] F. D. Kanellos, G. J. Tsekouras, and J. Prousalidis. Onboard dc grid employing smart grid technology: challenges, state of the art and future prospects. *IET Electrical Systems in Transportation*, 5(1):1–11, 2015. ISSN 2042-9738. doi: 10.1049/iet-est.2013.0056.

[10] E. Skjong, M. Ochoa-Gimenez, M. Molinas, and T. A. Johansen. Management of harmonic propagation in a marine vessel by use of optimization. In *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–8, June 2015. doi: 10.1109/ITEC.2015.7165797.

[11] E. Skjong, J. A. Suul, A. Rygg, T. A. Johansen, and M. Molinas. System-wide harmonic mitigation in a diesel-electric ship by model predictive control. *IEEE Transactions on Industrial Electronics*, 63(7):4008–4019, July 2016. ISSN 0278-0046. doi: 10.1109/TIE.2016.2532845.

[12] Siemens. BlueDrive PlusC make vessles safer, more profitable and environmentally friendly, 2017. URL `https://w3.siemens.no/home/no/no/sector/industry/marine/Documents/Orig.BDPC_16pages.pdf`.

[13] V. Staudt, R. Bartelt, and C. Heising. Fault scenarios in dc ship grids: The advantages and disadvantages of modular multilevel converters. *IEEE Electrification Magazine*, 3(2):40–48, June 2015. ISSN 2325-5897. doi: 10.1109/MELE.2015.2413436.

[14] T. J. McCoy. Trends in ship electric propulsion. In *Power Engineering Society Summer Meeting, 2002 IEEE*, volume 1, pages 343–346 vol.1, July 2002. doi: 10.1109/PESS.2002.1043247.

[15] DNV. Offshore standard, electrical installations, April 2011.

[16] P. Mattavelli. A closed-loop selective harmonic compensation for active filters. *IEEE Transactions on Industry Applications*, 37(1):81–89, Jan 2001. ISSN 0093-9994. doi: 10.1109/28.903130.

[17] Ned Mohan, Tore M Undeland, and William P. Robbins. *Power Electronics Converters, Applications and Design*. John Wiley Sons, Inc., 111 River Street, Hoboken, NJ070300, 5th edition, 2003.

[18] Sigurd Skogestad and Ian Postlethwaite. *Multivariable Feedback, Analysis and design*. John Wiley Sons, Chichester, New York, Brisbane, Toronto, Singapore, 2nd edition, 2001.

[19] A. R. Årdal, E. Skjong, and M. Molinas. Handling system harmonic propagation in a diesel-electric ship with an active filter. In *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, pages 1–6, March 2015. doi: 10.1109/ESARS.2015.7101524.

[20] Chi-Jui Wu, Jung-Chen Chiang, Shih-Song Yen, Ching-Jung Liao, Jin-Shyr Yang, and Tzong-Yih Guo. Investigation and mitigation of harmonic amplification problems caused by single-tuned filters. *IEEE Transactions on Power Delivery*, 13(3):800–806, Jul 1998. ISSN 0885-8977. doi: 10.1109/61.686977.

[21] M. El-Habrouk, M. K. Darwish, and P. Mehta. Active power filters: a review. *IEE Proceedings - Electric Power Applications*, 147(5):403–413, Sep 2000. ISSN 1350-2352. doi: 10.1049/ip-epa:20000522.

[22] F. Z. Peng and D. J. Adams. Harmonic sources and filtering approaches-series/parallel, active/passive, and their combined power filters. In *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370)*, volume 1, pages 448–455 vol.1, 1999. doi: 10.1109/IAS.1999.799993.

[23] Zhiling Qiu, Jie Kong, and Guozhu Chen. A novel control approach for lcl-based shunt active power filter with high dynamic and steady-state performance. In *2008 IEEE Power Electronics Specialists Conference*, pages 3306–3310, June 2008. doi: 10.1109/PESC.2008.4592464.

[24] Wenqiang Zhao, Yuling Li, and G. Chen. A double-loop current control strategy for shunt active power filter with lcl filter. In *2009 IEEE International Symposium on Industrial Electronics*, pages 1841–1845, July 2009. doi: 10.1109/ISIE.2009.5222606.

[25] H. Akagi. Active harmonic filters. *Proceedings of the IEEE*, 93(12):2128–2141, Dec 2005. ISSN 0018-9219. doi: 10.1109/JPROC.2005.859603.

[26] S. Rahmani, A. Hamadi, and K. Al-Haddad. A comprehensive analysis of hybrid active power filter for power quality enhancement. In *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pages 6258–6267, Oct 2012. doi: 10.1109/IECON.2012.6389025.

[27] Tim Bucella. *Servo Control of a DC-Brush Motor*. Microchip Technology, 1997.

[28] T. Kamel, Y. Biletskiy, C. P. Diduh, and L. Chang. Failure detection of the capacitor bank of the three phase diode rectifier. In *2012 25th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, pages 1–4, April 2012. doi: 10.1109/CCECE.2012.6334967.

[29] A. M. R. Amaral and A. J. M. Cardoso. Using input current and output voltage ripple to estimate the output filter condition of switch mode dc/dc converters. In *2009 IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives*, pages 1–6, Aug 2009. doi: 10.1109/DEMPED.2009.5292791.

[30] A. Lahyani, P. Venet, G. Grellet, and P. Viverge. *Failure prediction of electrolytic capacitors during operation of a switchmode power supply*. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 13, NO. 6, NOVEMBER 1998, 1984.

[31] Temesgen Haileselassie. Control of multiterminal vsc-hvdc (mtdc) systems. Master thesis, NTNU, Trondheim, 2008.

[32] Rik De Doncker. *Power Electronics Control, Synthesis, Application*. Institut für Stromrichtertechnik und Elektriche Antriebe (ISEA), Jägerstrasse 17-19, 52066 Aachen, 5th edition, 2016.