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Short Circuit Current Contribution from Converters

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Master of Energy and Environmental Engineering
Submission date: June 2017
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Problem Description

This master's thesis is part of the joint research project, ProSmart, at NTNU departments of Electrical Engineering and Telecommunication. The research project addresses relay protection solutions in a smart grid perspective where communication of data becomes possible over a wide area.

The implementation of distributed generation in the distribution grid, leads to new challenges regarding operation of the grid. One challenge, being changes in the short circuit current level. While there is existing research on the short circuit current contribution from directly connected distributed generation, the research available on converter connected units, are limited.

Therefore, the goal of this master's thesis is to investigate the short circuit current contribution from converter connected distributed generation. The thesis, can be divided in to three parts. In the first part, a literature review will be conducted. In the second part, simulations in Simulink will be performed. In the third part, short circuit tests at the Smart Grid Laboratory, will be conducted.

Preface

This report is my master's thesis for the course "Electric Power Engineering and Smart Grids". This is the final step for achieving the degree Master of Science in Energy and Environmental Engineering, at the Norwegian University of Science and Technology. The thesis, is based on, and a continuation of, the specialization project "Converter Contribution During Faults" performed by the same author, in the fall of 2016.

The motivation for choosing this topic is a burning interest for the power system of the future. This is a field of rapid change, and the introduction of distributed generation is an essential part of the transformation. It has been especially exciting to investigate the impact of converters by performing short circuit tests in the Smart Grid Laboratory at NTNU.

The completion of this master's thesis would not have been possible without the help of the people around me, and in the following I would like to pay special attention to some of these people. First, I will like to thank my supervisor, Professor Hans Kristian Høidalen, for the continuous guidance and help which have led to the finalization of this thesis.

I would also like to thank Post-Doc, Santiago Sanchez Acevedo, for helping with the creation of a Simulink model representative of the laboratory setup. Furthermore, I would like to thank Research Scientist at Sintef, Kjell Ljøkelsøy, for suggesting the laboratory set-up and explaining the limitations as well as the possibilities of testing in the Smart Grid Laboratory. I would also like to thank the guys at the Service Lab at NTNU, for acquiring the necessary parts and helping with constructing the setup in the laboratory. Furthermore, I would like to thank Research Scientist at Sintef, Jon Are Suul for helping me understand the fundamentals of converter control and providing me with relevant literature. I would also like to thank Research Scientist at Sintef, Jorun Irene Marvik, for guidance regarding limitation of the scope.

Finally, I would like to thank my family and friends for the encouragement and kindness they have shown throughout this process. An extra thanks to Frida Berg for being my sparring partner with respect to ideas and laboratory preparations. Finally, a special thanks to my sister, Eirin Garnås for proofreading this thesis.

My interest in this topic and the power system of the future, has not been diminished throughout the completion of this thesis. In the future, I hope to be able to continue working in the field of smart grids.

Trondheim, June 2017

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Abstract

The implementation of converter connected distributed generation in the grid is increasing. The converter enables control of the renewable resources' intermittent nature, which leads to regulation of voltage, frequency, and power output characteristics. This makes converters a preferable interface for renewable resources. The implementation of these units introduces new challenges in the distribution grid. One being a bi-directional power flow. This could be problematic for the traditional protection scheme, because it is based on an one-directional flow. Another challenge, is that the units can impact the short circuit level.

The scope of this master's thesis is investigating the short circuit current contribution from converters. Common practice today, is to operate with a rule of thumb saying that the short circuit current is one to two times the rated current. Therefore, the purpose of this thesis is to gain a deeper understanding of the converter short circuit behaviour, beyond the rule of thumb.

The hypothesis of this thesis, is that the short circuit current contribution from a converter is negligible. To investigate this hypothesis thoroughly, this thesis consists of a literature review, Simulink simulations and tests in the Smart Grid Laboratory.

The literature review corroborates the hypothesis to some extent. The review illustrates that the short circuit current contribution from a converter, is small. Some papers went as far as stating that the converter short circuit current contribution, is negligible. The results from the Simulink simulations showed that the short circuit contribution from one converter is small. However, this result is only accurate for the simplified control scheme implemented in the simulation model.

Some of the laboratory results also corroborate the hypothesis. Two different control schemes were tested in the laboratory. Control scheme 1 was directly controlling the reactive and active current, while control scheme 2 supplied AC voltage support to the grid. Different external factors and internal control settings were changed, to investigate the impact on the converter short circuit contribution. Results showed that the current contribution was largest with control scheme 2 implemented. However, even with this control scheme, the largest measured current was only 1.61 pu.

The findings in this Master's thesis, are not enough to make a general conclusion regarding the short circuit current contribution from a converter. To make such a conclusion, more research is needed. However, the findings have corroborated the hypothesis.

Sammendrag

Stadig flere omformer-tilknyttede produksjonsenheter blir implementert i distribusjonsnettet, og omformere seiler opp som soleklar favoritt for nettilknytning av fornybare energikilder. En av årsakene, er at kontrollsystemet kan tilpasse seg den kontinuerlige endring relatert til fornybare energikilder. På denne måten kan spenningen, frekvensen og den injiserte effekten reguleres. Samtidig bringer disse produksjonsenhetene også med seg nye utfordringer til driften av distribusjonsnettet. En utfordring, er at disse enhetene gjør effektflyten i nettet to-dimensjonal. Siden de tradisjonelle beskyttelsesmekanismene er basert på en en-dimensjonal effektflyt, kan denne endringen være problematisk. En annen utfordring, er at det totale kortslutningsnivået kan bli endret.

Denne masteroppgaven utforsker hva kortslutningsbidraget fra en omformer-tilknyttet produksjonsenhet er. I litteraturen bruker man ofte en tommelfingerregel som sier at kortslutningsbidraget fra en omformer er en til to ganger nominell verdi. Målet med denne masteroppgaven er å utforske kortslutningsbidraget utover denne tommelfingerregelen.

Denne masteroppgavens hypotese er at kortslutningsbidraget fra en omformer er neglisjerbart. Hypotesen har blitt undersøkt ved et litteraturstudium, simuleringer i Simulink og tester i Smart Grid Laboratoriet på NTNU.

Litteraturstudiet forsterker hypotesen til en viss grad. Det illustrerte at kortslutningsbidraget fra omformere er liten. Noen av artiklene tok det et skritt lenger, ved å konkludere at kortslutningsbidraget fra omformere er neglisjerbart. Resultatene fra simuleringene forsterker også hypotesen. Det må dog bemerkes at et forenklet kontrolldesign ble brukt i denne modellen.

Hypotesen forsterkes også av noen av resultatene fra laboratorieforsøkene. To forskjellige kontrolldesign ble testet. Med kontrolldesign 1, ble den reaktive og den aktive strømmen kontrollert direkte, mens kontrolldesign 2 bisto nettet med spenningssupport. Videre ble eksterne faktorer og kontrollinnstillinger endret for å undersøke effekten de har på kortslutningsbidraget fra omformerne. Kortslutningsbidraget var størst med implementering av kontrolldesign 2.

Hovedfunnene i denne masteroppgaven forsterker hypotesen om at kortslutningsbidraget er neglisjerbart. De er dog ikke tilstrekkelig grunnlag for en generell konklusjon angående kortslutningsbidraget fra en omformer. For å kunne trekke en slik konklusjon, er det nødvendig med mere forskning på området.

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Abbreviations

BDEW	Bundesverband der Energie- und Wasserwirtschaft
DG	Distributed Generation
DER	Distributed Energy Resources
FRT	Fault Ride-Through
FPGA	Field-Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistors
LVRT	Low Voltage Ride-Through
MV	Medium Voltage
PLL	Phase-Locked Loop
PV	Photovoltaic
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
ROCOF	Rate-of-Change of Frequency
VSC	Voltage Source Converter

Chapter 1

Introduction

Section 1.1 describes the background and motivation for this thesis. Section 1.2 presents the scope of the thesis and the hypothesis. This section also summarizes the main research questions. Section 1.3 presents the limitations of this thesis, and in Section 1.4 the approach of the thesis is described. Finally, Section 1.5 presents the outline of the thesis.

1.1 Background and Motivation

The modern society is dependent on electricity, and a well-functioning electrical power system is therefore crucial for day-to-day life. A well-functioning system includes the transport of high-quality, safe, and reliable power to every consumer alike [1]. In the traditional power system, the power flow was one-directional, meaning the power was produced at a high voltage level and transported to the consumer at a low voltage level. These factors made the operation of the power system straightforward.

In recent years, the traditional power system has been subjected to changes. One reason, being an increasing world population combined with a larger consumption per capita. These factors lead to a desire for more energy sources with higher efficiency. At the same time, there is an emerging desire for increasing sustainability [2]. The increasing focus on sustainability can be illustrated with help of the "20/20/20" climate and energy targets created by the European Commission. These targets state that by 2020, 20% of all energy shall come from renewable sources, the energy efficiency shall increase by 20% and the emission of greenhouse gasses shall be 20% lower than the 1990 level [3].

One way of meeting the goal of more renewable energy is by implementing renewable sources in the distribution grid. The impact these sources have on the grid will depend on several factors, including their location, type, maximum production, the voltage level of connection, the stiffness of the grid and the total number of these units present in the grid [4].

These units also introduce new challenges in the distribution grid. One being a bi-directional power flow. This could be problematic for the protection scheme, because the traditional protection scheme is based on an one-directional power flow. Another challenge, is that the units can impact the short circuit level. Available literature addressing the impact of directly connected DG, is increasing rapidly. However, there is limited literature addressing the short circuit current contribution from converters.

1.2 Scope of the Thesis

The scope of this master's thesis is investigating the short circuit current contribution from converters. Common practice today, is to operate with a rule of thumb saying that the short circuit current is one to two times the rated current. Therefore, the purpose of this thesis is to gain a deeper understanding of the converter short circuit behaviour, beyond the rule of thumb.

The hypothesis is that the short circuit current contribution from a converter is negligible. To investigate this hypothesis, a literature review, Simulink simulations and laboratory tests have been conducted. The main research questions for this thesis are:

1. Is there some form of consistency in the converter behaviour during short circuits?
2. How does the implemented control scheme, impact the converter short circuit current contribution?
3. How does the control settings in a specific control scheme, impact the converter short circuit current contribution?
4. How does external factors, with a specific control scheme, impact the converter short circuit current contribution?
5. What is the difference between the short circuit current contribution from the main supply and the converter?

1.3 Limitations

As mentioned, tests were performed on voltage source converters in the Smart Grid Laboratory at NTNU. The laboratory setup limits the scope of this thesis, to be about the short circuit current contribution from one converter. However, the penetration of converter connected DG, increases. Therefore, investigation of the aggregated short circuit current contribution from several converters, is of interests. This was not possible with the laboratory setup.

The complex converter control system used in the laboratory tests, opens for numerous possibilities. Compared to the possibilities the control system facilitates, the tests performed in this thesis are limited. The time constrain was a natural limiter of the number of tests. However, the final decision regarding the tested parameter settings was taken by the author. This decision was based on findings from the literature and the authors Simulink simulations. Still, it can be argued that more settings should have been varied, and one can only hope that this will be subject for future work.

The laboratory tests are not performed for the worst-case scenario. With respect to the scope of this thesis, the parameter settings resulting in the largest short circuit current, is the worst-case scenario. One reason the short circuit contribution is being limited, is to protect laboratory equipment. Short circuit tests on the converter connected to the main supply, have not been performed in the laboratory before. Therefore, inductors are implemented to restrain the short circuit contribution.

1.4 Approach

To investigate the hypothesis thoroughly, this thesis is divided into three parts. These parts are summarized in the following.

The first part, consists of a literature review. This review has two main goals: find research papers that have tested the short circuit contribution from converters either by simulations or by laboratory tests and to elaborated on the reasoning behind the rule of thumb.

The second part, consists of simulations in Simulink. The purpose of these simulations, can

be divided into two. Firstly, to predict the converter short circuit behaviour in the Smart Grid Laboratory. Secondly, to test aspects beyond the possibilities in the laboratory.

The third part, includes laboratory tests. Short circuit tests will be performed on a voltage source converter in the Smart Grid Laboratory at NTNU. The results from these laboratory tests, are the most important elements of this thesis.

1.5 Thesis Outline

Chapter 2 presents background information necessary for understanding the scope of this thesis. The focus is on the implementation of distributed generation and the challenges these units introduce. This section is based on the specialization project "Converter Contributions During Faults" conducted by the same author during the fall of 2016 [5].

Chapter 3 presents the main findings of the literature review. In this review, literature found in conjunction with the specialization project is used [5]. However, the literature in question have been investigated more comprehensively. This literature combined with new additional literature, shape this chapter.

Chapter 4 presents the short circuit simulations performed in Simulink.

Chapter 5 presents the laboratory setup and the approach for the tests performed in the Smart Grid Laboratory at NTNU.

Chapter 6 presents the results from the Smart Grid Laboratory tests.

Chapter 7 summarizes and compares the findings from Chapter 3 to Chapter 6. This chapter also include suggestions for further work.

Chapter 2

Background: Implementation of DG

This chapter presents background information necessary for understanding the scope of this thesis. Section 2.1 discusses the increasing penetration of converter connected DG. In Section 2.2 the technical guidelines associated with grid-connection of this technology are presented. Section 2.3 briefly describes the power electronic needed for making the implementation possible. Finally, in Section 2.4, the behaviour of DG-units during short circuits are briefly described, alongside problems the different short circuit level can cause.

In [6] DG is defined as "an electric power source connected directly to the distribution network or on the customer site of the meter". The term DG, usually refers to units with power ratings up to 10 MW [7]. Examples of DG-units are synchronous generators, induction generators and converter connected generators. The first two are directly connected to the grid. Hereafter, the term traditional DG will be used to refer to these units. Converter connected DG is interfaced with power electronics to the grid.

2.1 Increasing Penetration

Converter connected DG is emerging as the preferred DG technology today. This category of DG-units includes both non-renewable and renewable resources. Example of non-renewable resources are internal combustion engines, microturbines and fuel cells, while renewable resources include photovoltaic systems, wind power generation and small hydro-power systems. The converter enables control of the renewable resources' intermittent nature, which leads to regulation of voltage, frequency, and power output characteristics. This

makes converters a preferable interface for these resources. [8]

Small Hydro-Power Units

Hydro-power is the largest source of power in Norway, with a market share of 95% of the total power production. As of 2014, a total of 1500 hydro-power units, within a large power range, were installed in Norway. Nearly all DG-units, are small hydro-power units. Small hydro-power units can be divided into micro-hydro units, which have power ratings lower than 100 kW, mini-hydro units, which have ratings between 100 kW and 1 MW and small-hydro units, which are units with ratings of 1 MW to 10 MW. [4, 9]

Photovoltaic Systems

In 2015, PV systems with a combined capacity of 2,45 MW were installed in Norway, which made the total installed capacity 15 MW [10]. 2016 saw a rapid increase in installed PV capacity, as 11 MW were installed during this period [11]. According to statistics from 2016 [10], the installed PV systems in Norway are primarily off-grid installations, and are mainly associated with small cabins, infrastructure or lighthouses. However, a new trend is emerging: during 2016, 10 MW of the installed capacity were grid connected [11].

The application of PV systems can be categorized in the following categories, small systems with power rating of 400 W or less, residential systems with power rating between 0.4 kW and 6 kW, commercial systems with power rating above 6 kW and commercial/PV plants from 100 kW and above [12]. A trend is that larger PV systems are being installed in storage houses, like at Asko in Vestby and Unils in Våler [13]. The installed capacity of 2016 reflects this, with 7.37 MW of the total capacity being related to commercial buildings [11].

Wind Energy

Another important renewable energy resource experiencing an increase in installed capacity, is wind energy. These units are often installed in groups of tens or hundreds of similar turbines, and they therefore need to be connected with converters to a high voltage level, like the 35 kV level. [8]

2.2 Technical Guidelines

This section gives an overview of the technical guidelines used in the Norwegian distribution grid. The main focus is on requirements regarding grid connection of converter connected DG. This also includes protection mechanisms related to the implementation of these units.

SINTEF has developed a set of technical guidelines [4], for the connection of production units with ratings up to 10 MV. While these guidelines mainly focus on hydro-power units in the MV grid, they can be used as an indication for other types of DG-units. The guidelines were developed as part of the "Distribusjonsnett 2020" project and includes requirements for quality of supply, DG-units equipment, protection, measuring, communication and remote control, as well as general requirements for aspects that influence the distribution grid, and implementation, testing, operation and maintenance of DG. [4]

Another set of guidelines [14], is developed by REN AS and has some similarities with the one from SINTEF. The purpose of these guidelines is to recommend the protection necessary in a distribution grid with DG [7, 14]. In [15] it is stated that these guidelines are the recommended guidelines for the Norwegian distribution grid.

In the following, typical relay settings and other relevant protection settings based on guidelines [4, 14], are presented.

2.2.1 Protection of DG

In Norway, the DG-units usually have over- and under-voltage protection (U/t), over- and under-frequency (f/t) protection, over-current protection, and other internal protection [15]. In some situations, both the feeder and the DG have an over-current protection mechanism, which are coordinated [15].

U/t and f/t protection requirements recommend different disconnection times for the DG-units, depending on the severity of the change. The disconnection time for U/t and f/t protection are summarized in Table 2.2.1. The maximum disconnection time, includes the fault detection time and the breaker operations. The breaker operations are normally estimated to take 100 ms. [4, 14]

Table 2.2.1: Disconnection times for U/t and f/t protection.

Voltage range in % of nominal voltage	**Maximum Disconnection Time [ms]**
U <U_{lower}	200
U <85	1500
U >110	1500
U >115	200
Frequency [Hz]	
f <48	200
f >51	200

DG protection is often used to detect an unintentional islanding in the grid. Methods for detecting an islanded operation can be divided into active and passive methods [16].

In passive detection methods, the device reacts to natural occurring abnormal voltage situations [17]. U/t protection, f/t protection, ROCOF and voltage vector shift are examples of passive methods [17]. In active methods, the device actively participates by creating an abnormal voltage in PCC, with the goal of making a detectable change [17]. According to [16], no islanding detection method is superior in terms of their performance, their cost, and their operation regardless of the implemented DG technology. Still [7], argues that U/t and f/t protection are the preferred methods.

2.2.2 Outgoing Feeder Protection

In Norway, there are typically three alternatives for short circuit protection of an outgoing feeder, these are over-current protection, directional over-current protection, and distance protection with impedance pick-up [14]. The following section, focus on the recommenced relay settings, but the different type of relays will also be briefly described. For detailed explanations of the principle of these relays, the reader is referred to [18].

Over-Current Relays

Over-current relays are constructed based on the principle that a high level of current will be fed to the fault location. There are two important settings in an inverse over-current relay,

that needs to be set for it to operate optimal. The first is the pick-up setting, which sets the maximum level of allowed short circuit current. To choose an optimal pick-up setting that detects all faults, the value needs to be between the normal operating current and the minimum fault current level. This value further depends on the application and the relay specifics. The second important setting, is the time delay setting. The appropriate value of the time delay depends on the design of the relay, and the number and placement of other relays. [18, 19]

In an over-current relay the time delay is often set to 300 ms and the pick-up current is typically set to 120% of the nominal transformer current, in Norway [14]. In [15], two other methods are suggested. In the first method, a pick-up value equal to the component with the lowest rated current value, is used. In the second method, a pick-up value lower than 30% of the short circuit current from a fault located at the end of the line, is used [15].

Directional Over-Current Relays

Directional over-current relays have settings for the trip direction and the nontrip direction. The trip direction is often set to be from the bus-bar and towards the feeder. The direction is determined with voltage measurement, and the angle between the fault current and the voltage. There are various methods of achieving this and the appropriate method depends on the type of relay. These methods will not be explained in detail here, but [20] can be used to gain in-depth knowledge. [14, 18, 20]

The current pick-up setting for directional over-current relay, is usually like the non-directional over-current relay setting [14].

Distance Relays

Distance relays estimate the distance from the fault, by calculating the impedance between the fault location and the relay, by comparing the fault current and the voltage at the relay location [19]. One advantage, being that distance relays can detect short circuit currents lower than the nominal value [7]. This also makes the relay well suited in grids with low short circuit capacity [7].

One disadvantage of distance relays, is that every line segment needs a relay, which can

be quite expensive. This combined with the increasing complexity related to coordination of relays with several zones with different reach, leads to a desire for new solutions. One solution, is a relay with zones composed of several line segments. [14, 15]

The lines protected by distance relays, are divided into two zones. In Norway, the first zone usually has a reach of 80% and a time delay of 200 ms, while the second zone has a 120% reach and a time delay between 400 ms and 500 ms [15].

2.2.3 Fault Ride Through Requirements

The implementation of DG introduces new challenges and an emerging need for new protection mechanisms. The following section, focus on a new protection trend, which is fault ride through requirements.

The recommended practice for DG during faults, is changing. The requirements, have changed from recommending automatic disconnection of DG during faults, to demanding continuous support.

There are disadvantages associated with the disconnection of DG, one being stability issues. Another problem occurs when voltage dips arise in the transmission lines. This can lead to stability issues and voltage dips in the distribution grid. When the DG penetration level increases, the severity of the issues also increases. A high penetration level of DG also introduces the dilemma of staying connected during temporary faults and disconnection during permanent faults. These are some of the reasons, why the recommended practice is changing. [1, 7]

One type of FRT requirement is LVRT requirement. This requirement gives guidelines to a lower voltage limit as a function of time, during which the DG must stay connected to support the grid [1]. While the guidelines in [4] do not include specific LVRT curves, they do provide some relevant restrictions. For example, if a production unit over 250 kW experiences a voltage variation larger than 4%, they should continue to stay connected and maintain synchronized to the grid [4].

Examples of LVRT curves can be found in the BDEW technical guidelines [21]. Here DG is categorized into two categories, type-1 and type-2 units. The type-1 category is directly connected synchronous generators and the type-2 category is all other versions. Figure 2.2.1

illustrates the LVRT curve for converter connected DG-units. If the voltage drops below boundary 2 the DG is allowed to disconnect from the grid, if not it has to stay connected to support the grid. [7, 21]

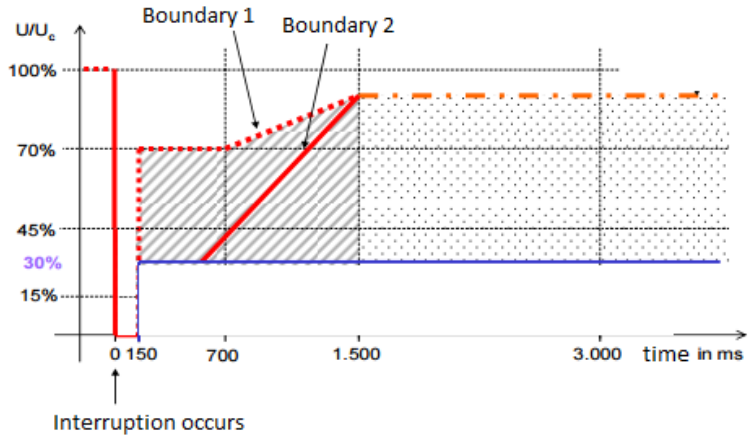


Figure 2.2.1: The LVRT curve for type-2 generator connected to medium voltage grid [21].

To provide the required voltage support the DG-unit needs to inject an increasingly higher current, which could result in an unwanted disconnection of DG, due to over-current [22]. This indicates that the common implemented current control can lead to a behaviour contradictory to the LVRT requirements. This contributes to a desire for changes in the converter control. One new control strategy is suggested in [22], and guarantees a low output current during voltage sags.

While LVRT requirements are being implemented, an even newer trend is the requirement of reactive power injections from the DG-units [23]. This is done to support the grid voltage, and at the same time reduce the risk of voltage collapse [23].

2.3 Power Electronic Interface

The interest in power electronic interface to the grid, is increasing. One reason, is the intermittent nature of renewable resources, which makes power electronics crucial for voltage, frequency, and power output characteristics regulation [8].

Converters are the power electronics most commonly used to interface DG with the grid. The expression includes every stage of power conversion in a power electronic system. A

converter is referred to as an inverter when the average power flow is from the DC- to the AC-side. When the power flow is in the opposite direction, the term rectifier is used. [24]

An important aspect of converters, is the implemented switching mechanism. The switching can be performed by different power electronics, like thyristors or IGBTs. IGBTs are becoming increasingly more favored. One advantage, is that they only require a small amount of energy, because of the high impedance gate. Other advantages, are that they have a small on-state voltage and they can block negative voltages. Compared with thyristors, IGBTs have higher controllability, because they can be switched on and off. They are also capable of having a bi-directional power flow, a characteristic predicted to be increasingly important. IGBTs with ratings up to 1700V and 1200A are in operation today. [1, 24, 25]

2.3.1 Converter Topology

The VSC is often applied for power ratings below 5 MW. However, the introduction of multilevel VSC increases the operation range, and makes power ratings up to 50 MW, possible. VSC is predicted to become the most widespread converter used for grid-connected DC power in the future, and that is why this section focus on VSC. [26, 27]

Still, a vast number of converter topologies exist. For theory about other two-level converter topologies, the reader is referred to [25, 28, 29]. While theory about multilevel topologies can be found in [8, 30–34].

A two-level VSC can operate both in a rectifier- and an inverter-mode. The following explanation is with respect to the inverter-mode of the VSC. Figure 2.3.1, illustrates a topology of a high-power two-level VSC.

The two-level VSC is constructed of three legs, and each leg is connected to one phase. One leg, is composed of two groups of switches. A switch can be constructed of two or more series-connected IGBT-valves. An IGBT-valve is used to refer to an IGBT in anti-parallel with a diode. The number of IGBT-valves reflects the converter DC voltage. To increase the voltage endurance, the IGBT-valves are connected in series. In the topology in Figure 2.3.1, each group consist of three IGBT-valves. Since the IGBT-valves in one group are controlled by the same gating signal, the valves will operate as one switch. [31, 35]

The VSC creates an output AC voltage by performing switching actions. When the upper

switch is turned on, the inverter output voltage is equal to half of the DC-input voltage. When the lower switch is conducting, the output voltage has the same magnitude, but with a negative sign. In other words, the output voltage varies between two voltage levels, which is why it is called a two-level VSC. How to control the converter to achieve this in the most efficient way, is explained in Section 2.3.2. The two switches in one leg, can never be on at the same time, because this makes a short circuit. The operation of the other legs is the same, but with a phase shift. [31, 35]

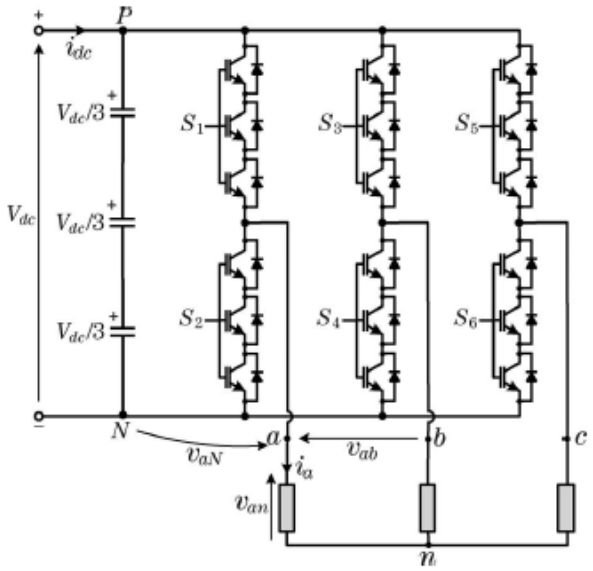


Figure 2.3.1: Illustration of the two-level VSC [35].

2.3.2 Converter Control

The control mechanism applied to a converter is dependent on the topology of the converter. Still, there are three basic functions that the control needs to fulfill. These are current control, DC voltage control and grid synchronization [12]. Further, the control strategies usually consist of two cascaded loops, where the inner loop is faster than the outer loop [36]. In the following different control mechanisms for a VSC are presented.

Reference Frame

The synchronous reference frame (dq-frame), the stationary reference frame ($\alpha\beta$-frame) and the natural reference frame (abc-frame) are often used in the converter control mechanisms. The transformation of the grid currents and voltages into the $\alpha\beta$-frame is also called Clark

transformation. In this transformation, the grid currents are transformed to stationary and sinusoidal values. [32, 36]

In comparison, in the *dq*-frame the grid voltages and currents are transformed in to values that rotates synchronously with the grid voltage. In this transformation, the control variables are decoupled DC values. One advantage, being that the decoupling facilitates independent control of the reactive and the active power. In other words, a direct connection between the direct current component, i_d, and the active power, as well as a direct relationship between the quadrature current component, i_q, and the reactive power, exists. [36, 37]

The *dq*-frame and the $\alpha\beta$-frame are preferred over the *abc*-frame. One advantage, is that they make the control structure easier and thereby also the analysis of the converters. These reference frames are facilitators for a rapid control of the amplitude and/or frequency on the grid side of the converter. [38]

Switching Signals

As briefly described Section 2.3.1, the switches usually consist of IGBT-valves, controlled by a voltage signal. This is accomplished by the generation of a voltage reference which then is used to determine the switching signals [39]. Here, the PWM scheme will be explained. Information about other switching techniques, like vector-based methods and pseudo-modulation method, can be found in [39].

The on and off mechanisms of the switches in the converter are an essential aspect of the control strategy. In this technique, a high-frequency carrier is compared to the voltage reference. This carrier can have different shapes, but the triangular waveform is often preferred. For this case, the upper group of switches in each converter leg will be turned on when the voltage reference is higher than the triangular waveform, while the switches in the lower group will be turned on when it is lower. The PWM scheme is considered to be the most established technique for VSC. Some advantages, are that the PWM reduces harmonics and limits current distortion. [24, 27, 32, 39]

Grid Synchronization

When a converter is grid connected, it is essential that it remains synchronized with the grid frequency and phase. There are different ways of achieving this, but [32] states that the PLL gives the best performance compared to other algorithms proposed in the literature. A common feature for different synchronization techniques, are that most of them uses voltage measurements [27]. With the help of a phase detector, a loop filter, and a voltage-controlled oscillator, the PLL extracts the grid phase angle [32, 36].

A common PLL technique, is the PLL that operates in the *dq*-frame. One disadvantage, is that the technique is not able to react fast or with high enough precision during faults. To solve this problem a decoupled double synchronous reference frame PLL can be implemented instead. [12]

Cascaded Control Loops

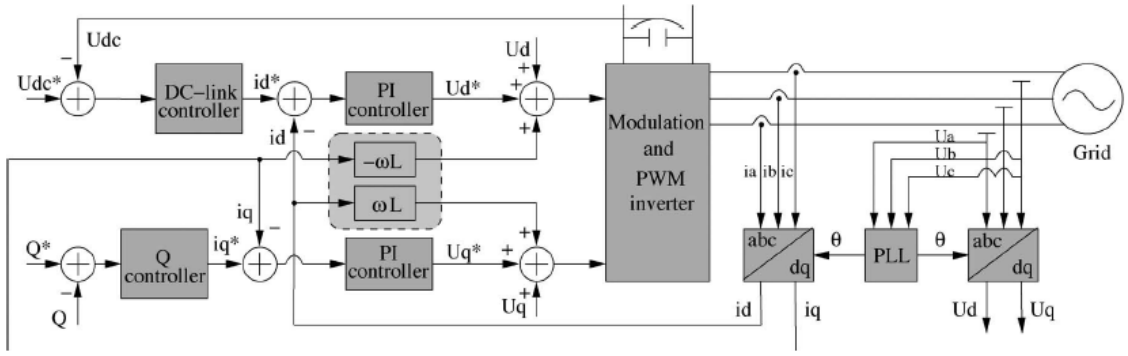
The control scheme is normally constructed of two loops. The inner and outer control loop depends on the application of the VSC [40]. Still, in common for the different possibilities, the outer loop generates a reference signal that the inner loop uses. The following section includes a brief description of some configurations.

One options is to have an outer loop that regulates active and reactive power. In this control scheme, the reference signals to the inner loop influences the active and reactive power flow. The control can either be done by multi-variable optimal controller or two decoupled PI controllers. One problem associated with traditional PI-controller, occurs during unbalanced situations. One solution, is implementing controllers operating with sinusoidal reference signals, which can lead to negligible steady state errors. [27, 41]

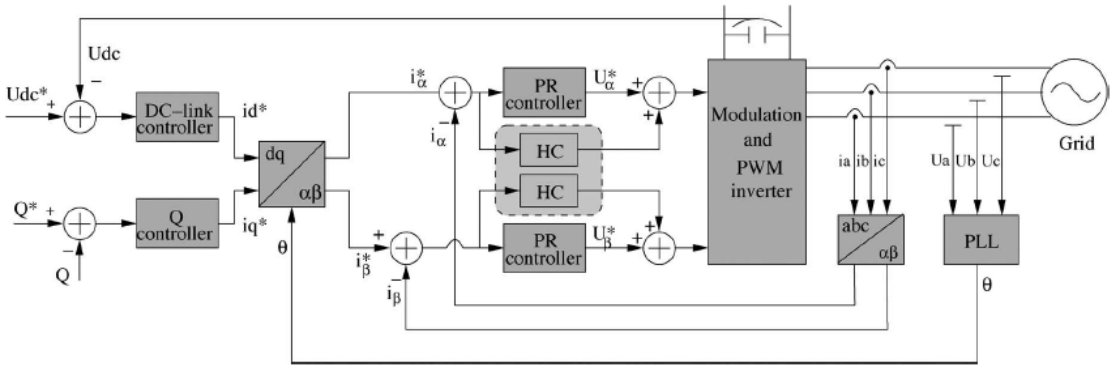
If the inner loop directly controls the current, the scheme is called a current control scheme. Common practice, is to have an inner loop that controls the current through the grid-connected filter inductor. Similarly, if the inner loop regulates the voltage magnitude, it is called a voltage control-based scheme. In this scheme, the output AC voltage is regulated to correspond to the utility grid voltage. [27, 42, 43]

It should be noted, that a current controlled DG is dependent on terminal voltage support supplied by another source, because it is not capable of maintaining the voltage on their

own. The source for this support, can either be the main supply or a voltage controlled DG in the power system. Problems associated with the loss of this support could be exposure to effects of under-voltage faults. [42]



(a) *dq*-frame.



(b) $\alpha\beta$-frame.

Figure 2.3.2: Control strategy with outer DC-link control and inner current loop in different reference-frames [36].

Another option is to have an outer control loop that consists of both a DC-link voltage regulator and a reactive power regulator. To have these decoupled regulators, the control scheme needs to be implemented in either the *dq*-frame or the $\alpha\beta$-frame. Common for the two schemes, is having an inner current loop. Control schemes with an outer loop consisting of both DC-link voltage and a reactive power regulator are illustrated in Figure 2.3.2 (a) and Figure 2.3.2 (b). [36]

In Figure 2.3.2 (a), the inner current control is implemented in the *dq*-frame, and is called a voltage-oriented synchronous reference frame based on proportional-integral controllers. This scheme, controls the DC-link so the desired power level is achieved at the converter output terminals. Figure 2.3.2 (a), clarifies how the grid synchronization and the switching

signal are adapted in a control scheme. In this scheme, the extracted phase angle is used together with the measured three-phase currents to calculate the *dq*-currents. The switching signals is provided by the inner current loop and delivered to the PWM. [32, 36]

In Figure 2.3.2 (b) the inner current control is implemented in the $\alpha\beta$-frame and the scheme is called the stationary reference frame method based on resonant controllers. This scheme is similar to the one in Figure 2.3.2 (a). Therefore, this scheme will not be further explained here. For more information, the reader is referred to [36].

Another option, is to have a outer loop controlling the DC-link, with an inner power loop. In this scheme, the current will be controlled indirectly, and is referred to as a direct power control space vector modulated scheme. [36, 44]

2.4 Short Circuit Level

In [45], a short circuit is defined to "the accidental or intentional conductive connection through a relatively low resistance or impedance between two or more points of a circuit which are normally at different potentials". This definition is based on the IEC 60 909 [45].

Short circuits can be a result of insulation failures due to lightning and switching surges, contamination of insulation or other mechanical causes [46]. Short circuits can cause significant amount of energy, arcing and burning at the fault location [47]. All components along the short circuit current path can also be exposed to high thermal and mechanical stress, which ultimately can cause damaged to the equipment [47].

There are four types of short circuits: single-line to ground, phase-to-phase, double-line to ground and three-phase short circuits. The short circuits can further be dived into symmetrical and unsymmetrical faults. The reader is referred to [46], for in-depth knowledge about the different type of short circuits.

2.4.1 Short Circuit Behaviour

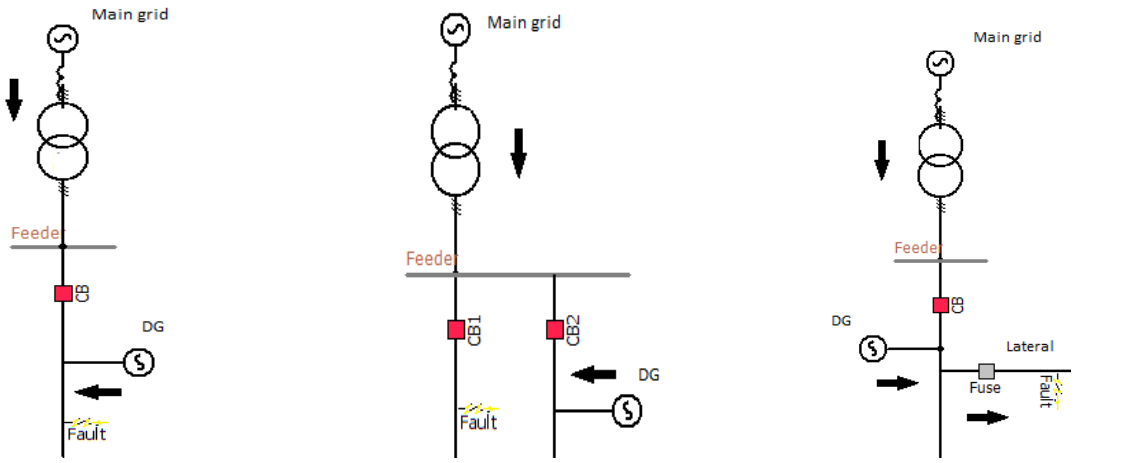
The traditional DG-units can either be induction or synchronous machines. When a short circuit arise in the grid, the rotating machines injects a large current to the fault location. This is freed energy from the energy stored in the inertia of the machine. For a synchronous

machine and an induction machine the initial fault current are approximately five to ten times the rated current. The synchronous machine oscillates to a value equal to two to four times the rated value, and then further down to steady-state. Since the field excitation is not being preserved in an induction machine, the fault current will decay to zero. [1, 48, 49]

The behaviour of converter connected DG is different than the traditional DG behaviour. In the literature, a rule of thumb states that the short circuit current contribution from a converter connected DG is one to two times the rated current [1, 15, 48, 50–53]. This rule of thumb is discussed in Chapter 3.

2.4.2 Associated Problems

The protection mechanism in the traditional power system is based on the contribution of a high magnitude, one-directional current flow from the main supply during faults. The introduction of DG in the grid leads to a bidirectional power flow that introduces new challenges in the power system. Some of these are described in this section.



(a) Blinding. **(b)** Sympathetic tripping. **(c)** Fuse saving scheme.

Figure 2.4.1: Challenges associated with implementation of DG.

Blinding

Blinding is used to describe a situation where the implementation of DG leads to the relay not tripping as intended. This occurs when a DG-unit is connected to a feeder with an over-current relay, and with a fault arising further down on the feeder, as illustrated in Figure 2.4.1 (a). The problem, is that the fault current seen by the relay will be smaller,

while the actual current at fault location will be larger, leading to the relay not tripping [54]. Evidently, this leads to more stress on the equipment, which ultimately can be destroyed [7].

Sympathetic Tripping

Usually a bus-bar in the distribution grid has several feeders connected to it. If a fault occurs in one of them, a relay in a different feeder with a DG-unit connected can trip. This situation, where a DG feeds a fault occurring at another feeder, is called sympathetic tripping, and is illustrated in Figure 2.4.1 (b). This behaviour is unwanted, because an important aspect of protection is selectivity. Selectivity in this situation, would be tripping only the feeder where the fault occurred. [7, 19]

Fuse Saving Scheme

Fuse saving scheme is used to refer to a situation where the interaction between the re-closer and a fuse on a lateral, is disturbed by the connection of DG. This is illustrated in Figure 2.4.1 (c). In a grid with no DG, the re-closer will disconnect the circuit before the fuse reacts to a temporary fault. The current contribution of the DG on the other hand, will make the fuse see a larger fault current than the re-closer, which might blow the fuse before the re-closer is able to react. [41, 55]

Chapter 3

Literature Review

To limit the extent of the literature review, it focuses on finding papers elaborating the main research questions described in Section 1.2. In the following the findings are presented.

The findings can be divided into three parts. Section 3.1 investigates the rule of thumb found in the literature. The rule of thumb states, that the short circuit current contribution from a converter connected DG is one to two times the rated value [1, 15, 48, 50–53].

The purpose of Section 3.2 and Section 3.3, is to present papers describing the converter short circuit behaviour beyond the rule of thumb. Therefore, Section 3.2 consists of research papers where laboratory tests or real-application tests, have been performed. Section 3.3 focus on research papers with simulation tests. In Section 3.4 the findings are discussed and summarized.

3.1 Elaboration of the Rule of Thumb

One reason for the small short circuit contribution from the converter, is limitations in the power electronic switches. In [54], the potential breakdown of the switches is mentioned as one of the technical limitations of the converter current. The same reasoning is used in [50], where the low thermal overload capability of the switches is said to limit the maximum allowed output current. If the current is not restrained, the switching devices can experience overheating [51]. Other papers, supporting the reasoning in this paragraph, are [15,48,56,57].

The limitations in the power electronic switches impact the short circuit level, because these

limitations require the implementation of a protection mechanism. This protection mechanism needs to disconnect the converter, when the maximum current limit is reached [43]. The protection mechanism is also called instantaneous over-current shutdown protection [53]. The limit is set to prevent large overshoots in response to rapid transients occurring in the grid [53]. [51] explains how the converter current can be limited in three ways, instantaneous hard limits in the *abc*-frame or in the *dq*-frame, and pre-defined inductor fault current in the *dq*-frame.

The rule of thumb do not elaborat on the shape of the converter current, or whether the current behaviour is the same throughout the short circuit. Still, literature describing the converter short circuit current behaviour can be found. According to [41], the short circuit current behaviour of converters can be divided into two periods, the transient period and the steady-state period. This division is also supported by [43].

In the transient period of the short circuit, an initial peak occurs. The magnitude of the peak depends to some extent on the hardware over-current protection. The over-current protection will stop the increase and force the current to the pre-set maximum limit. The magnitude of the initial peak depends further on the location and severity of the fault, and the implemented converter control. However, the magnitude of the short circuit current will never exceed the hardware over-current protection. This control-based protection can be performed by the inner loop of the control system. [41]

In the steady-state period of the short circuit, the converter current oscillates with constant magnitude. According to [41], a current controlled converter will reach the steady state operation faster than a voltage controlled converter. Still, most controllers do not use more than a few cycles to reach the steady state. If the short circuit is present after several seconds, either the control system or an external protection device will trip the DG. The magnitude of this current depends on the specific converter settings. A commercially available converter can usually withstand 10% to 30% current overload, for a time duration of a few seconds. [41]

As previously mentioned, the short circuit current is affected by the implemented converter control scheme. According to [51], the short circuit current largely depends on the implemented control mechanism, which again depends on the application of the converter.

To illustrate, according to [53], a control system with a inner current loop will regulate the converter to a behaviour resembling a constant current source, except during transients.

This operation is a result of a current control bandwidth that is order of magnitudes higher than the frequency in the grid. In other words, the converter current behaviour with this control system can be divided into a transient and a steady-state period. [53]

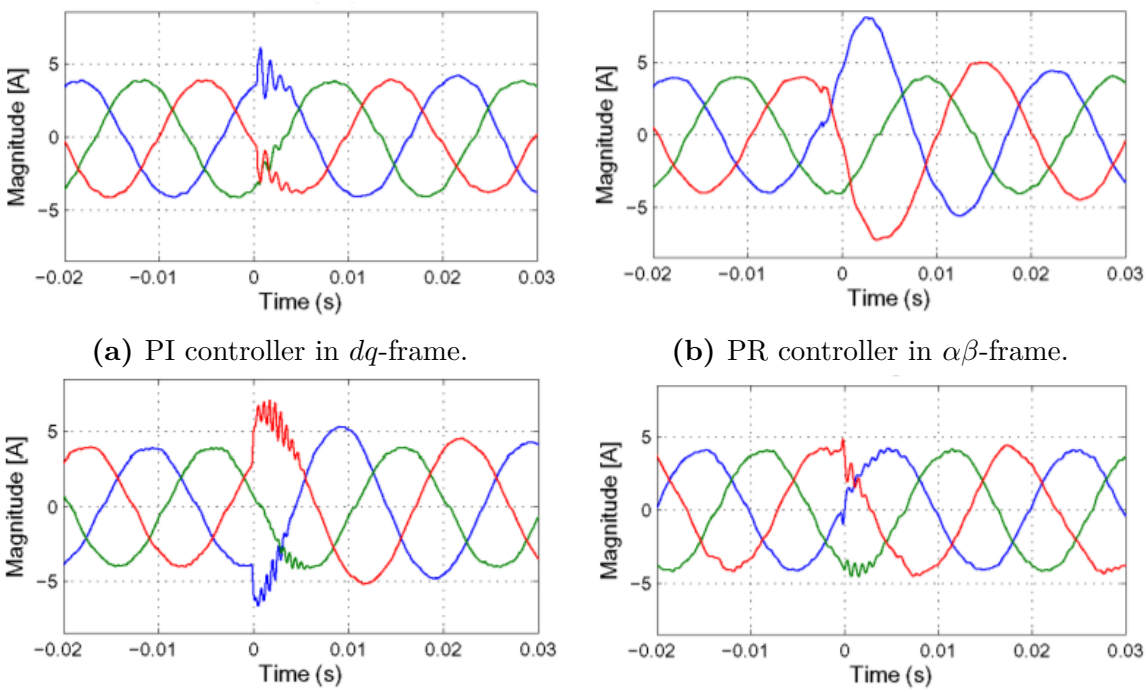
As mentioned, the implemented converter control, depends on the converter topology and intended converter application. However, according to [41] the implemented control scheme also depends on the personal preferences of the designer and the operator of the converter.

[41] further explains how other nonlinearities in the control system and hardware also can constrain the short circuit current. These nonlinearities include "certain control functions hitting their limits, state machine changing its state, and etc." [41].

Another important facilitator for the short circuit behaviour is the DC-link capacitor connected between the power source and the converter. The DC-link decouples the power source from the grid, so the impact of the power source on the fault current can be neglected [42]. The DC-link keeps the DC voltage constant during short transients, which makes the voltage at the input converter terminals constant [43].

3.2 Laboratory Tests

In [58] different control systems have been tested through an experimental setup. The test circuit consist of a DC-source, a PWM VSC, a restive load and a grid simulator. The PWM VSC is from the Danfoss VLT 5000 series, with a rated voltage of 400 V and a rated current of 5 A. The four control systems tested, are PI controller in *dq*-frame, PR controller in $\alpha\beta$-frame, PI controller in *abc*-frame and DB controller in *abc*-frame. Figure 3.2.1 illustrates the results from a single-line to ground fault with these control systems. In Figure 3.2.1 (a) the control is able to regain normal operation fast, after the initial peak. This is because of the imposed current reference. In Figure 3.2.1 (b) the implemented control leads to an overshoot in the current, but the current is controlled back within one fundamental period. With the control in Figure 3.2.1 (c), the behaviour is similar only with a smaller overshoot and with more disturbance. The test results show that the control system in Figure 3.2.1 (d), is the superior control system, with only a small transient and with no overshoot in the current. [58]



(a) PI controller in *dq*-frame.

(b) PR controller in $\alpha\beta$-frame.

(c) PI controller in *abc*-frame.

(d) DB controller in *abc*-frame.

Figure 3.2.1: Converter current contribution during a single-line to ground fault with different current controllers [58].

In [54] one test is performed on a feeder with a converter connected DG-unit, with a rating equal to 5% of the short circuit power seen by the bus-bar. In this test, the current is limited to the rated current value during short circuit. It is further pointed out, that the implemented control system restrains the current, and therefore another control system would give a different result.

In [57], both PSCAD simulations and hardware benchmark tests are performed. The benchmark test was used for validation of the results obtain in the PSCAD simulations. The circuit consists of a grid simulator, a load, a short circuit emulator and a three-phase converter. The controller was set to give an output current equal to unity power factor, and the maximum limit was set to one times the rated value. When a single-line to ground short circuit occurred, the measured converter current was like normal operation. When a three-phase short circuit to ground occurred, the converter current also resembled normal operation. The reason, is the control setting. During normal operation, the converter is controlled to injected rated value. Since the maximum current limit is set to one times the rated value, the magnitude of the converter current will be the same during short circuit and normal operation. The PSCAD results illustrated the same behaviour as the benchmark measurements. [57]

In [59] results from tests performed on a 13.8 kV feeder, with 30 single-phase converter connected DG-units, with a power rating of 2kW, are presented. The main conclusion, was that the short circuit contribution from the converters, are negligible. The maximum registered converter current was two times the rated value. [59]

In [1] tests are conducted at National Renewable Energy Laboratory, in the USA. A single-phase converter is connected to a 15 kW grid simulator. The converter is current controlled. When the converter was short circuited, the maximum peak in the converter current was five times the rated peak current. Tests were also performed on a three-phase 500 kVA converter. Three different types of phase-to-phase short circuits were tested. For each short circuit type, four tests were conducted, where the time instance of the short circuit occurrence, varied. This impacts the value of the maximum peak occurring during the short circuit. The tests showed that the maximum converter current varied between two to three times the rated peak value. [1]

3.3 Simulation Tests

In [60] simulations are performed on a feeder with one load and one 5 MVA converter connected DG. The converter is current controlled, with unity power factor. When a three-phase short circuit to ground occurred, the converter current was like normal operation except from a short transient at the start and end of the short circuit. The converter short circuit contribution compared to the current injected by the main supply, was small. When a single-line to ground short circuit occurred, the converter current contribution increased. The cause of this was the delta-wye transformer between the converter and the grid, which creates a zero-sequence current path. However, the current level was small compared to the total short circuit current. The conclusion was that the implemented current control causes the small short circuit contribution. [60]

[61] presents the main results from a study that focuses on determining the short circuit characteristics of some commercially available PV converters. The PSCAD simulation models were based on detailed device descriptions from the manufactures, and six converter models were created. There were conducted several fault simulations for each converter. When a three-phase short circuit occurred, within the first half cycle, four of the converters

experienced an initial peak in the current, with a magnitude above two times the rated value. After the first half cycle the current contribution from the six converters were below 1.5 times the rated value. [61]

An interesting finding from these simulations was that the converters operate with different trip-levels. The range of the current trip-levels varied from 1 to 1.8 times the rated value. This illustrates, that the trip-level depend on the manufacturer and the implemented power electronics. The number of cycles between the short circuit occurrence and the converter tripping also varied. [61]

Based on the excessive testing, it was concluded that the converter types could be divided into two groups. In the first group, the converters disconnect within one cycle, if the PCC voltage decreases below 0.5 pu. In the second group, the converters remain connected up to 10 cycles, regardless of the voltage level. With simulation models of these two types, more than 840 simulations were performed on a benchmark system. The conclusion was that the maximum converter current occurs within the first cycle, but not at the same instance in time. Another main finding was that the short circuit current contribution depends on the design of the converter and the control. However, the parameter settings affecting the different behaviours are not specified. [61]

In [41] hardware-in-the-loop simulations are used to investigate the short circuit behaviour of a real PV converter using a real-time digital simulator. In the case system, a DG is connected next to the feeder re-closer, and the fault occurs further along on the feeder. The converter is controlled with a current control scheme, and the control system is a commercially available solar controller. When a three-phase fault occurred five miles from the converter, the converter current experienced a high peak. This was caused by the voltage drop in the feeder. After the peak, the PLL used around 2 cycles to re-synchronize with the system. Then the current oscillated with a magnitude equal to 1.2 pu. When the short circuit occurred further away from the DG, the DG injected less reactive current.

In [37] simulations are performed on a case-study model, based on a real network. This model consists of three MV feeders with PWM VSC. In these simulations, the converters are controlled with active and reactive power control scheme. An initial peak occurred in the converter current, when a 0.5 pu voltage dip was applied in the circuit. Still, with a value of 1.3 pu this was significantly lower than when traditional DG was connected. When

a three-phase short circuit occurred, the converter control regained normal operation after one cycle. The magnitude of the initial peak in this situation was 3 pu. The conclusion was that the impact of converter connected DG is negligible. [37]

In [62] simulations are performed on a feeder model with converter connected DG-unit implemented. The converter is controlled with a PI controller. When a short circuit occurred the controllers regained the active and reactive power settings after 110 ms. This led to transients in the current. Still, the conclusion was that the initial 100 ms can be neglected. This means that the injected power stays the same before and right after the short circuit occurs. [62]

In [63] PSCAD simulations are conducted on a model of a typical feeder used in Ontario, Canada. The PWM VSC is implemented at the end of the feeder, and the DG-unit is rated at 7.5 MW. When a three-phase to ground short circuit occurred at the substation, the converter current experienced an initial peak in the value, which was caused by the discharge of the inverter output capacitors. After the peak, the converter injected a current of 1.4 times the rated value. This current level depends on the manufacturer of the converter. When a three-phase to ground short circuit occurred at the feeder-end, the initial peak in the current was smaller, but the behaviour during the rest of the short circuit was similar. The conclusion was that converters contributes with a short circuit current in the range of 1.1 to 1.5 times their nominal current. It was further stated that in the worst-case scenario the current will never exceed a value higher than 1.5 pu. [63]

In [64] simulations are performed on a test system with 27 buses, 15 loads and four DG-units connected. The penetration level is 7% compared to the total load. The converter connected DG-units are controlled to deliver a constant active power. The conclusion was that the current contribution from a converter connected DG-unit is too low to impact the relay. [64]

In [65] simulations are performed in SIMULINK. The PWM converters are controlled with PI controllers in the *dq*-frame and the current loop references are generated by active and reactive power control loops. Four different cases have been tested. The conclusion was that the short circuit current contribution from a converter, is small. The converter current was programmed to be 1.5 times the rated current during the short circuit simulations. Therefore, these simulations do not investigate the actual impact of the controller. Similar assumptions are done in [66]. In these PSCAD simulations, the converter current was pre-set

to contribute with a current equal to two times the rated value. [65, 66]

In [43] two simulations on a feeder are conducted. One converter connected DG is connected to the feeder, and a three-phase fault is applied at the feeder-end. When a current control scheme was implemented, the converter current during fault slowly increased, before it slowly decreased back to normal operation. The slow response, was caused by the outer control loop. The outer loop was set to control power, and it has a slow response time. On the other hand, when a voltage control scheme was implemented, the converter current experienced an overshoot. This control scheme is faster than the current control scheme, and after a few cycles it regulates the current back to normal operation. The converter current never reached the maximum limit in these tests. The maximum limit is often set to two times the rated value. The conclusion was that a voltage control scheme contributes to a higher short circuit contribution compared to a current control scheme. [43]

Fault simulations in PSCAD are performed in [67]. The PSCAD model is a 27.6 kV feeder with one converter connected PV plant. When a three-phase short circuit and a penetration level of 30% of 70MVA were applied, the corresponding converter current was below 2 pu of the rated value. An initial peak occurred, with a magnitude larger than 2 pu. In the second simulation, the penetration level was increased to 45% and the location of the fault was moved. The converter current contribution became higher than in the previous simulation and the magnitude during steady state was two times the rated value. The shape of the current was similar in the two tests.

In [68] laboratory tests are performed on a 3 kW converter, which is available on the market. The results illustrate that the converter current during fault is affected by the magnitude of the fault impedance. The maximum short circuit registered was 1.08 pu. The authors, do not have access to the software controlling the converter. Still, they argue that the low short circuit contribution can be caused by the nature of the converter application. Further, they argue that the converters usually used in research, have switches that are oversized compared to to their application. Because this was not the case in this paper, the short circuit contribution was below two times the rated value. The over-current limit was set to 1.2 pu by the manufacturer of the converter. Simulations in PSCAD with a converter model created based laboratory tests, were also performed. The results are similar, and will not be included here. [68]

3.4 Discussion

The literature review illustrates that the short circuit current contribution from a converter, is small. Some papers, [37, 58–60, 64, 65], goes as far as stating that the converter short circuit current contribution, is negligible. In the following, aspects that impact the resulting short circuit converter current will be discussed. This discussion revolves around the main research questions mentioned in Section 1.2.

Shape of the Converter Current

Both [41, 43] states that the short circuit current contribution can be divided into two periods, the transient period and the steady-state period. They also state that an initial peak will occur in the transient period [41, 43]. This is supported by the test results from [37, 41, 60, 62, 63, 67]. They further state that the converter current will resemble normal operation during the steady state period [41, 43]. This is supported by the test results from [37, 41, 54, 57–60, 62–68].

Impact of Implemented Control Scheme

No papers describe the implemented control scheme in detail. Therefore, it is impossible to draw conclusions on the impact of a specific control scheme. Still, some observations and trends can be observed.

A general observation is that the type of control scheme implemented impacts the converter short circuit behaviour. This can be illustrated with the results from [43]. When a voltage control scheme was implemented, the short circuit current experienced an initial overshoot. On the other hand, when the current control scheme was used, the short circuit current increased slowly, before it decreased back to normal operation.

A trend in the papers, [37, 41, 54, 57, 60, 63], is that the control scheme is programmed to rapidly control the short circuit behaviour to resemble normal operation. The magnitude of the oscillations depends on the maximum output current limit. This limit differs in the different papers. For example, [54, 57] have set the maximum limit equal to the rated value, while [41] has set the limit to 1.2 times the rated value. According to [43], the maximum

current level often is set to two times the rated value. This illustrates that the control parameter settings also affect the short circuit current contribution.

Impact of Control Parameters

The following includes a presentation of other examples illustrating how the control parameters affect the short circuit behaviour. The experimental tests in [58] illustrate that the type of inner current controller affects the converter current at the beginning of the short circuit. The largest overshoot occurred with the PR controller in $\alpha\beta$-frame, but the magnitude was too small to trip the over-current protection in the system. In comparison, when the DB controller in *abc*-frame was implemented, the converter current only experienced small transients with negligible magnitudes. According to [58] the controller behaves more optimally when exposed to voltage variations, if it has a voltage feed-forward term. This can be illustrated with the result from the PR controller in $\alpha\beta$-frame. This controller has no voltage feed-forward term and it created the largest current overshoot out of the four controllers. [58]

An important aspect from [61], is that some converters have been designed to be disconnected. This can be illustrated with the simulation results from the paper. The trip-levels of the six converters ranged from 1 to 1.8 times the rated value. The over-current protection limit is set to protect the power electronics, and therefore these results show that short circuit behaviour to some extent depends on the manufacturer.

Another example of internal factors impacting the short circuit behaviour can be found in [63]. According to [63], the initial current peak is caused by the discharge of the converter output capacitors. Still, the initial peak is also caused by external factors. In [41] it is stated that the initial peak is caused by the voltage drop in the feeder. This illustrates, that it is the combined impact of internal and external factors that results in the converter short circuit behaviour.

Impact of External Factors

In [61] it is illustrated how the converter current behaviour depends on external factors. Based on several simulations, the converters were divided into two categories. The division was based on the converter reaction to a voltage drop. The first category, disconnects within

one cycle if the voltage drops below 0.5 pu. The second category, stays connected for ten cycles even if the voltage drops below 0.5 pu. The reason some are disconnected, while others are not, is also assigned to the internal protection mechanism implemented in the converters.

Other examples of external factors impacting the short circuit behaviour can be found in [68] and in [63]. According to the results from [68], the fault impedance impacts the converter short circuit contribution. Similar, the results from [63] illustrates that the distance between the converter and the fault location impacts the short circuit current injected by the converter.

Elaboration of the Rule of Thumb

As mentioned in Section 3.1, the short circuit current can never exceed the hardware over-current protection. Therefore, the low thermal overload capability of power electronics is a restraining factor with respect to the magnitude of the converter short circuit current. Within the range set by this restriction, the implemented converter control determines the short circuit behaviour.

However, some tests contradict the rule of thumb. One example, in [1], the maximum peak during short circuit varied from two to five times the rated peak value. According to [68] the power electronic switches tested in research papers are often oversized, which gives them a higher over-current endurance. This can be questioned, based on the discussion in this section. Several research papers have been presented, where the results of the tests have given a short circuit contribution of one to two times the rated current. Either way, before making a general conclusion regarding the short circuit current contribution from converters, more research is needed.

Chapter 4

Simulink Simulation

This chapter presents the Simulink simulation results. The purpose of these simulations, can be divided into two. Firstly, to predict the converter short circuit behaviour in the Smart Grid Laboratory. Secondly, to test aspects beyond the possibilities in the laboratory.

Section 4.1 describes the Simulink model, and includes an elaboration of the parameter values. In general, the parameter values are set equal to the VSC and the other equipment used in the laboratory tests. Section 4.2 describes the approach, and includes assumptions and simplifications deemed necessary. Section 4.3 presents the results of the simulations, according to the main research questions in Section 1.2. Finally, Section 4.4 discusses and summarize these results.

4.1 Model

Figure 4.1.1 illustrates the simulation model. This Simulink model approximates the laboratory setup shown in Figure 5.1.1.

In the model a constant DC-source is connected to a small resistance, which again is connected to the DC-side of the VSC. The AC-side of the VSC is connected to a three-phase source, which represents the main supply. The fault simulation block is connected between the VSC and the main supply block.

Current and voltage measurements are performed at the locations denoted with M1, M2 and M3. At M1, the converter current, $I_{converter}$, is measured, with positive direction defined out

of the VSC. At M2, the current injected by the main supply, I_{main_supply}, is measured, with positive direction defined into the main supply. The total fault current, I_{fault}, is measured at M3, and positive current direction is defined into the fault location.

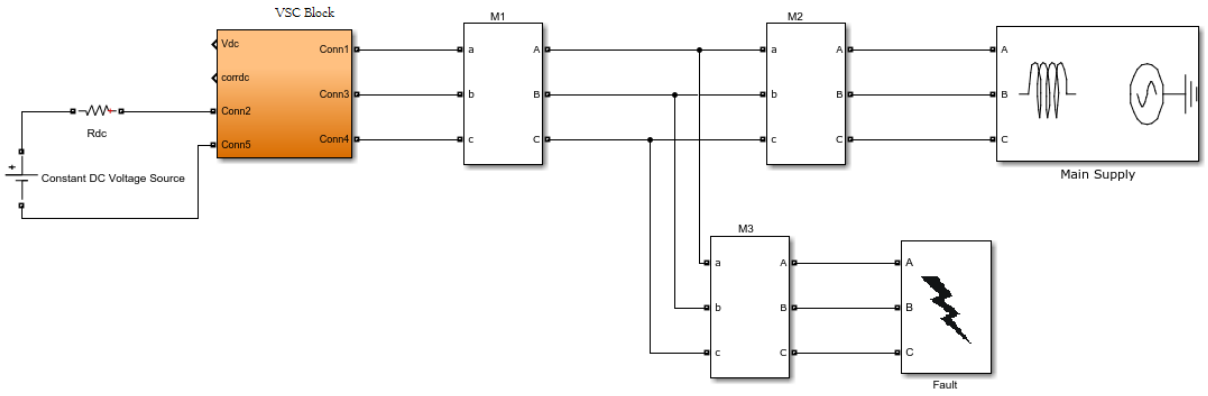


Figure 4.1.1: The Simulink model used for short circuit simulations.

4.1.1 Main Supply and DC-Source

The main supply is simulated with a three-phase source in series with a RL-branch. The line-to-line base voltage of this source is set to 400 V. This is the same voltage level as the supply grid in the Smart Grid Laboratory. The resistance of the RL-branch is set to zero, while the inductance is set to 1 mH. This is the value of the inductance between the supply grid and the model grid in the laboratory tests.

The constant DC-source has a voltage level equal to 600 V, which equals the DC voltage used in the laboratory tests. The source is connected in series with a resistance equal to 2 mΩ. The constant DC-source and the VSC block cannot be directly connected. Therefore this resistance is a necessity. The value of the resistance is based on test simulations.

4.1.2 Voltage Source Converter Block

The VSC block consist of a LCL-filter, a DC-capacitor link and an average-model based VSC. The reference signal of this average-model is the average three-phase voltage at the bridge. Figure A.1.1 in Appendix A.1, illustrates this VSC grid interface.

The parameter values for the LCL-filter and DC-capacitor link are given in Table 4.1.1, and are initialized in the Simulink model with the MATLAB script in Appendix A.2. The values

in Table 4.1.1 are taken from the VSC in the laboratory.

Table 4.1.1: Parameters for the LCL-filter and the capacitor link.

Parameter	Value
C_{vsc_dc}	4.0000 [mF]
C_{vsc}	0.0497 [mF]
L_{vsc_con}	0.5093 [mH]
L_{vsc_grid}	0.2037 [mH]
R_{vsc}	0.0320 [Ω]

The VSC averaged-model is controlled by a PLL and a current controller, which together create the reference signal. Voltage control is omitted from the Simulink model, because the DC-source delivers a constant DC voltage.

Both control mechanisms, have PI controllers, and their values are given in Table 4.1.2. The parameters from the laboratory had discrete values, and they are transformed to continuous values with the MATLAB script in Appendix A.2.

Table 4.1.2: PI parameters for the PLL and the current control.

Parameter	Discrete Value	Continuous Value
k_{ppll}	5.3052	5.3111
k_{ipll}	58.9463	58.9463
k_{pvsc}	0.5000	0.5065
k_{ivsc}	65.0000	65.0000

PLL

The PLL mechanism used in the simulation, is based on the PLL implemented in the built-in control of the VSC in the Smart Grid Laboratory. The PLL implemented in the built-in control is described in Section 5.1.3. Some simplifications have been made, and the resulting loop is illustrated in Figure A.1.2 in Appendix A.1. The PLL consists of an arc-tangent function, a PI controller and an integrator. The parameter values of the PI controller, k_{ppll} and k_{ipll} are given in Table 4.1.2.

Current Control Loop

The current control implemented in the built-in control system is like a normal PI current controller. Therefore, an already existing current control loop has been used in the Simulink simulations. The current controller is created by Santiago Sanchez Acevedo. An illustration of the implemented current control can be found in Figure A.1.3 in Appendix A.1. The PI controller parameters, k_{pvsc} and k_{ivsc} are given in Table 4.1.2.

4.1.3 Fault Simulation Block

To simulate faults, a three-phase fault block is implemented in the circuit, as illustrated in Figure 4.1.1. This block consists of a three-phase circuit breaker. The interval between the circuit breaker switching-operations, corresponds to the duration of the short circuit.

The fault resistance and ground resistance cannot be zero, and therefore both are set to 1 mΩ. The three-phase fault block is modeled as a current source, and cannot be connected in series with the inductive element of the VSC block. Therefore, a snubber resistance is needed. The snubber resistance is set equal to 1 MΩ. The snubbers are made purely resistive by setting the snubber capacitance equal to infinite.

4.2 Approach

This section describes the simulation approach. First the different simulation cases, are presented. An important part of understanding the approach, is to understand the simplifications and assumptions made when the Simulink model was created. Therefore, Section 4.2.2 describes these simplifications and assumptions.

4.2.1 Simulation Cases

The simulations can be divided into two cases. In case A, simulations are performed to get an impression of what will happen in the laboratory tests. In case B, simulations are performed to tests aspects beyond possibilities available in the laboratory.

To limit the contents of this chapter, case A focuses on two aspects. First, how $I_{d\_reference}$ impacts the converter current contribution. Second, how the time instance of the short circuit occurrence impacts the contribution. This is tested by changing the time of fault occurrence, T_{start}. A three-phase short circuit is applied, in all simulations in case A. The simulations in case A, can be summarized as follows:

Case A.1 $I_{d\_reference}$ is changed

Case A.2 T_{start} is changed

In case B, different short circuit types are simulated in order to investigate the impact on the converter current contribution. The short circuit emulator used in the laboratory, can only test three-phase short circuits and phase-to-phase short circuits. Therefore, simulations of short circuit types beyond these two, are of interest. The simulations in case B, can be summarized as follows:

Case B.1 Three-Phase Short Circuit

Case B.2 Three-Phase to Ground Short Circuit

Case B.3 Single-Line to Ground Short Circuit

Case B.4 Double-Line to Ground Short Circuit

Case B.5 Phase-to-Phase Short Circuit

4.2.2 Simplifications and Assumptions

The Simulink model is a simplified version of the circuit used in the Smart Grid Laboratory. Therefore, the laboratory results will be more reliable, than the simulation results. For this reason, the number of simulations included in this chapter are sparse. The simulation results are considered to be supplements to the laboratory results.

The VSC control is simplified, compared to the built-in control in the VSC in the Smart Grid Laboratory. At the same time, the VSC is approximated with an average-model in the Simulink model. This should be kept in mind, when the simulation results are used to predict the converter behaviour in the laboratory tests.

A disadvantage with the simplified control system, is that the control uses a long time to regain normal operation after a short circuit. The converter control struggles to regain

normal operation after three-phase short circuits are cleared. The poor behaviour at the end of the short circuit is assigned to the simplified control system.

The time the short circuit is cleared, also affect the resulting converter current. This is illustrated in Section 4.3.3. The duration of the short circuit is set to 100 ms, which is the short circuit duration used in the laboratory tests.

With regard to the hypothesis of this thesis, parameter settings resulting in a large current injection by the converter, are of interest. Therefore, some parameter settings have been set based on this.

The converter will be controlled to inject maximum active power. Some might argue, that the d-axis current control reference, $I_{d\_reference}$ can be set to a value larger than the rated value. However, tests simulations show that the converter current becomes unstable when, $I_{d\_reference}$ exceeds 5 pu. Even worse, the converter current after the short circuit becomes unstable for an $I_{d\_reference}$ exceeding 4 pu. For values below this, the impact of varying $I_{d\_reference}$ is significant when the short circuit is cleared. The impact of varying $I_{d\_reference}$ is elaborated further in Section 4.3.2.

Still, in the rest of the short circuit tests $I_{d\_reference}$ will be set to 1 pu, and $I_{q\_reference}$ to 0 pu. The reason for this, is that the simplified control scheme is not able to handle an increasing $I_{d\_reference}$ in a proper manner.

The fault resistance and the ground resistance are set to 1 mΩ. These values are chosen, because low resistances give a large fault current. Simulation tests show that smaller resistances, have negligible impact. In the laboratory tests, the short circuit impedance was set to 2 mH. The reason, being to limit the short circuit current injected by the main supply. This is discussed in Section 5.2.

The magnitude of the initial peak, depends on the location on the sine wave-form at the instance the short circuit arise. Therefore, the time of fault occurrence, T_{start}, is set to 1.977 s. This is the time instance just before the peak-value in phase C occurs. The effect of varying T_{start}, is explained further in Section 4.3.3.

4.3 Results

This section presents the simulation results. These results are presented according to the research questions listed in Section 1.2. The research question regarding the impact of the implemented control scheme, has been omitted, because only one has been tested.

4.3.1 Shape of the Converter Current

Figure 4.3.1 illustrates $I_{converter}$ for a 100 ms three-phase short circuit with $I_{d\_reference}$ equal to 1.00 pu. This figure illustrates that the converter short circuit current behaviour can be divided into three periods.

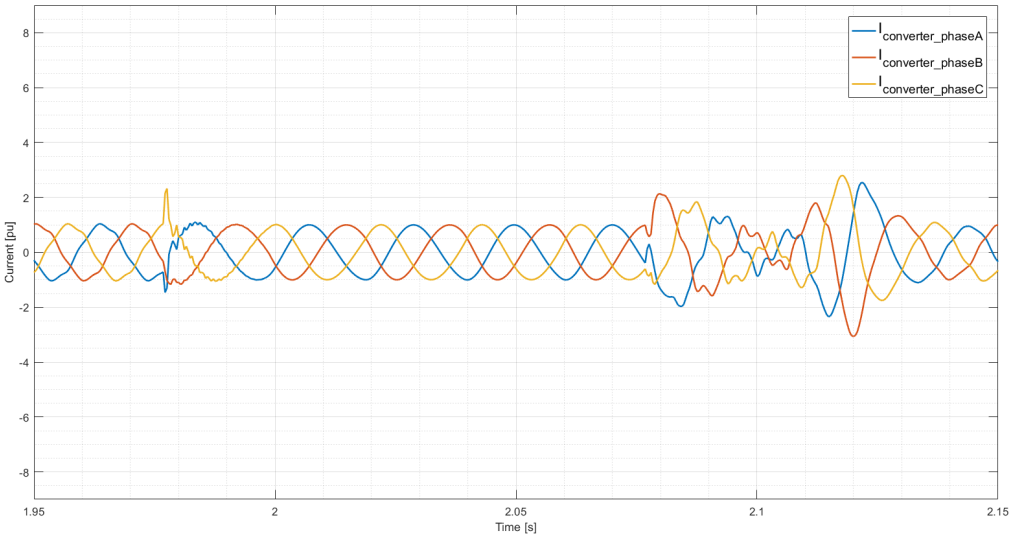


Figure 4.3.1: $I_{converter}$ for a 100 ms three-phase short circuit with $I_{d\_reference}$ equal to 1.00 pu.

The first period refers to the start of the short circuit. In this period a positive peak, $I_{initial\_peak\_positive}$, and a negative peak, $I_{initial\_peak\_negative}$, occurs in $I_{converter}$. This was referred to as the transient period in Chapter 3. In this simulation, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$, are 2.33 pu and -1.47 pu, respectively. The magnitude of $I_{initial\_peak\_negative}$ is smaller compared to phase C. The reason for this is that phase A is further from the time instance where it reaches its negative peak value.

In the second period, the converter control regulates the current to resemble the behaviour during normal operation. This was referred to as the steady state period in Chapter 3.

However, the magnitude of the oscillations, is different than during normal operation. For a three-phase short circuit, the magnitude is 0.02 pu smaller, and therefore negligible. The magnitude of the oscillations in each phase, depends on the type of short circuit. This is explained in Section 4.3.3. The occurrence of a short circuit also introduces a phase shift in the converter current in the second period. The control uses time to make the time period of each phase equal to 20 ms again. At the same time, the converter current is not synchronized with the current injected by the main supply. The rapidness of the phase shift regulation, depends on the implemented control and especially the PLL. Still, these factors have a negligible impact on the magnitude of the short circuit current. Therefore, these aspects will not be investigated further in this thesis.

The third period, starts when the short circuit is cleared and ends when normal operation is reached. When the short circuit clears, the converter control struggles to regulate the converter back to normal operation. The behaviour of this period depends on the short circuit type. This is described further in Section 4.3.3.

4.3.2 Impact of Control Parameters

This section investigates the impact of $I_{d\_reference}$. Figure 4.3.2 illustrates $I_{converter}$ for a 100 ms three-phase short circuit with $I_{d\_reference}$ equal to 1.25 pu.

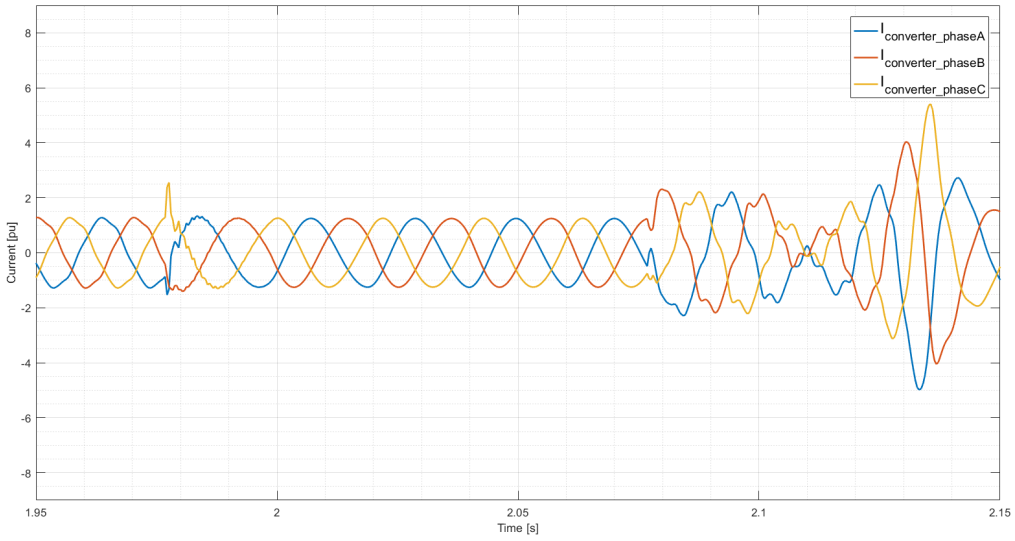


Figure 4.3.2: $I_{converter}$ for a 100 ms three-phase short circuit with $I_{d\_reference}$ equal to 1.25 pu.

In the first period, the $I_{converter}$ has increased compared to when $I_{d\_reference}$ was 1.00 pu. To illustrate, when $I_{d\_reference}$ was increased from 1.00 pu to 1.25 pu, $I_{initial\_peak\_positive}$ increased from 2.33 pu to 2.56 pu. For the same increase of $I_{d\_reference}$, $I_{initial\_peak\_negative}$ changed from, -1.47 pu to 1.54 pu.

In the second period, the control mechanism regains normal operation. The shape of $I_{converter}$ is similar compared to when $I_{d\_reference}$ was 1.00 pu. However, the magnitude of the oscillations differs. The magnitude increases when $I_{d\_reference}$ increases. This is expected, because the converter is regulated to injected more power.

To illustrate the impact of having $I_{d\_reference}$ larger than the rated value, $I_{d\_reference}$ was set to 1.25 pu. The reason for this is elaborated in the following.

In the tests in the laboratory, the rated RMS current is set to 90 A in the built-in control. In Simulink, the rated peak value is set to 102.1 A. Therefore, $I_{d\_reference}$ must be set to 1.25 pu to imitate the rated power from the laboratory VSC. The results from this section show that the impact of increasing $I_{d\_reference}$ in the first and second period is small, while the impact in the third period is significant.

When $I_{d\_reference}$ was 1.00 pu, the largest peak in the third period, was 2.80 pu. However, when $I_{d\_reference}$ was set to 1.25 pu, the largest peak was 5.42 pu. Other test simulations illustrated that the difference increased even more for a higher value of $I_{d\_reference}$. The cause is assigned to the simplified control system, and therefore higher values of $I_{d\_reference}$ is not included in this chapter.

4.3.3 Impact of External Factors

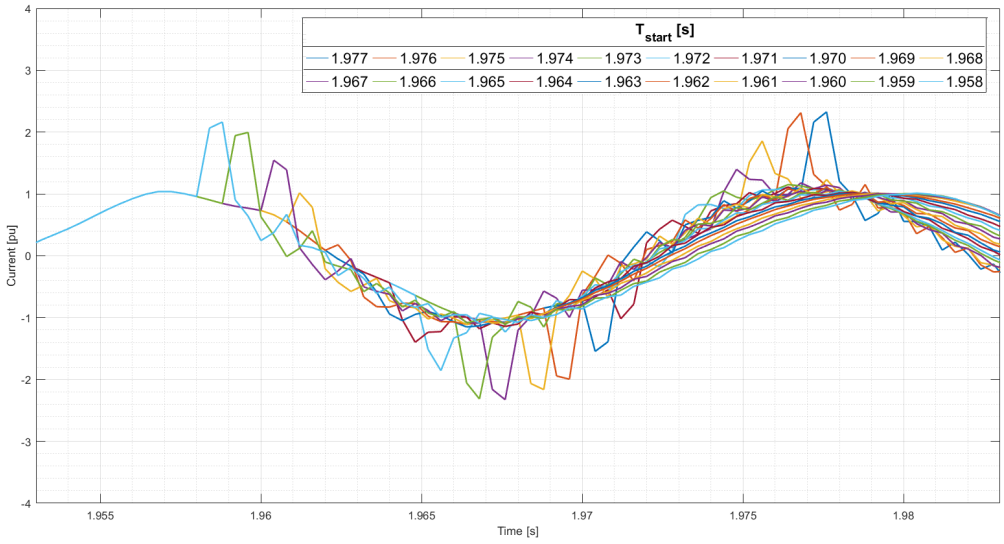
The impact of external factors is investigated with T_{start} and the short circuit type. T_{start} will also be tested in the laboratory. The short circuit type will only partially be tested in the laboratory, because of the limitation of the short circuit emulator.

T_{start} is Changed

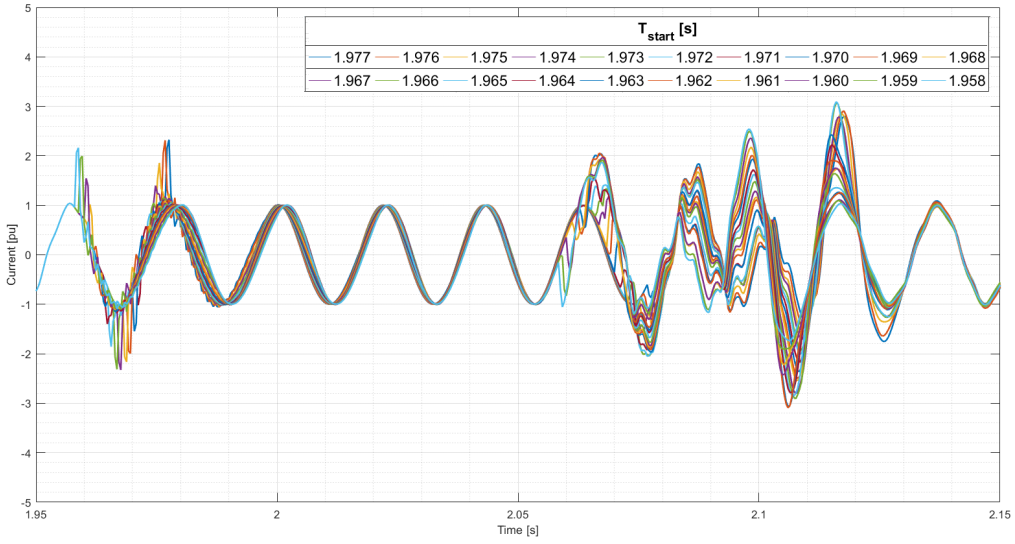
T_{start} has been changed from 1.958 s to 1.977 s, with an increment equal to 0.001 s. The reason being to illustrate one period of one phase. In all simulations, a 100 ms three-phase

short circuit has been applied. Except from T_{start}, the parameter settings are the same in every simulation.

It has been assumed adequate, to illustrate the impact of varying T_{start}, with phase C of the converter current, $I_{converter\_phaseC}$. For comparison, $I_{converter\_phaseC}$ from the different simulations are illustrated in the same graph. The resulting $I_{converter\_phaseC}$ behaviour are illustrated in Figure 4.3.3 (a) and in Figure 4.3.3 (b).



(a) Time interval from 1.953 s to 1.983 s.



(b) Time interval from 1.95 s to 2.15 s.

Figure 4.3.3: $I_{converter\_phaseC}$ during a 100 ms three-phase short circuit for different values of T_{start}.

Figure 4.3.3 (a) and Figure 4.3.3 (b) illustrate the first period and the whole duration of the short circuit, respectively. It should be noted, that Figure 4.3.3 (a) and Figure 4.3.3 (b) have a y-axis from -4.00 pu to 4.00 pu, and 5.00 pu to 5.00 pu, respectively.

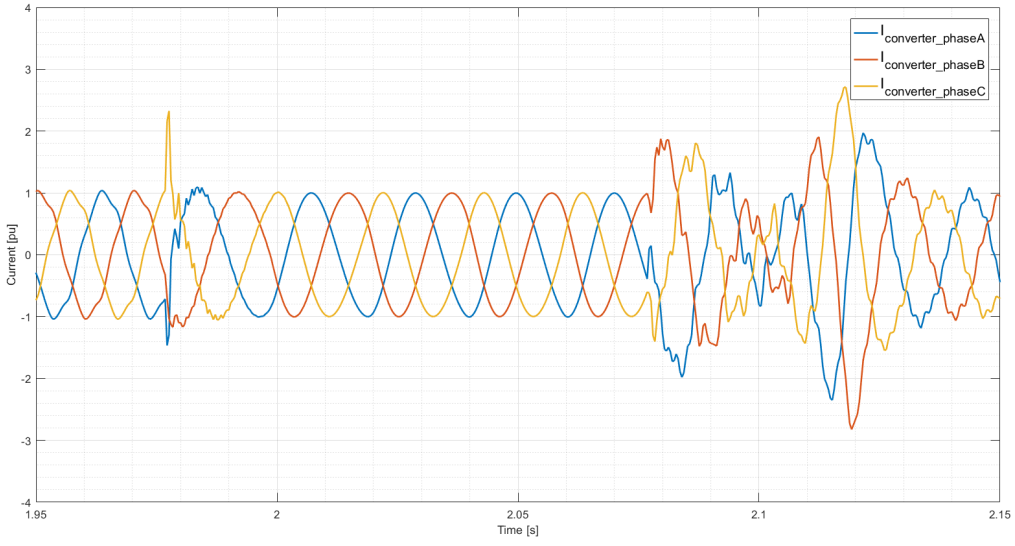
Figure 4.3.3 (a) illustrates how the magnitude of the initial peak in $I_{converter\_phaseC}$ varies as T_{start} changes. During one time period, the magnitude varies between -2.32 pu and 2.32 pu. As $I_{converter\_phaseC}$ approaches the zero-crossing, the magnitude decreases. To exemplify, when T_{start} is set to 1.962 s, $I_{initial\_peak\_positive}$ is 0.06 pu.

The second period of the short circuit is similar for the different values of T_{start}.
However, $I_{converter\_phaseC}$ from the different simulations are phase shifted from each other. This illustrates that T_{start} affects the phase shift.

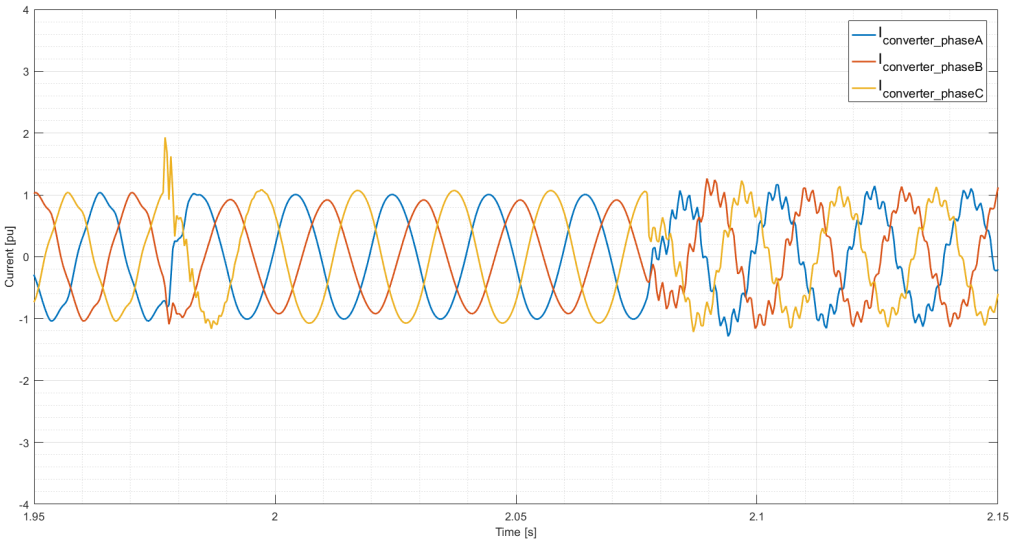
In the third period $I_{converter\_phaseC}$ behaviour differ with T_{start}. Figure 4.3.3 (b) illustrates, that the time the short circuit is cleared impact the current behaviour. The large oscillations in this period, is largely assigned to the simplified control scheme. Therefore, this will not be elaborated any further.

Type of Short Circuit

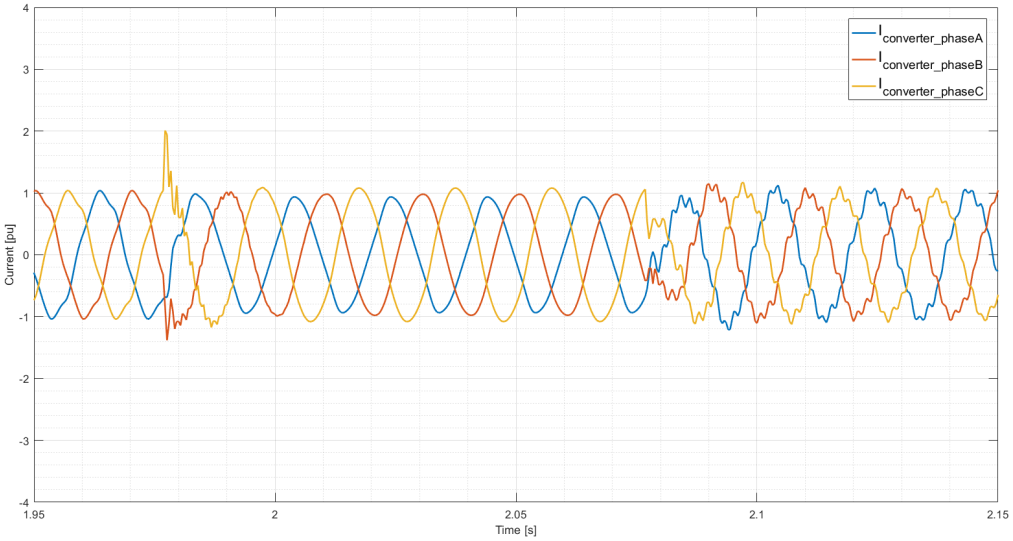
In this section, the impact of the type of short circuit is illustrated. Five different short circuits were simulated, four of these are illustrated in Figure 4.3.4.



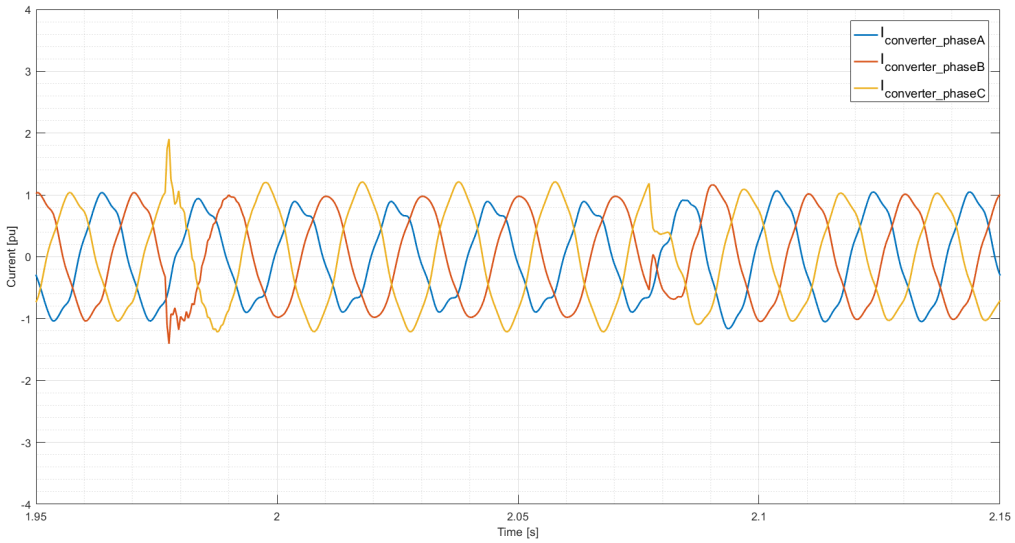
(a) Three-phase to ground short circuit.



(b) Phase C to ground short circuit.



(c) Phase B and phase C to ground short circuit.



(d) Phase B to phase C short circuit.

Figure 4.3.4: $I_{converter}$ during different types of 100 ms short circuits.

Figure 4.3.4 (a) to (d) illustrate $I_{converter}$ for a three-phase to ground short circuit, a phase C to ground short circuit, a phase B and phase C to ground short circuit, and a phase B to phase C short circuit, respectively. $I_{converter}$ for a 100 ms three-phase short circuit was illustrated in Figure 4.3.1.

When different short circuits are simulated, the behaviour of $I_{converter}$ is similar during the first period. However, the magnitude of $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ varies. When a three-phase short circuit is simulated, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$, are 2.33 pu and -1.47, respectively. $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ have the same values when a three-phase to ground short circuit is simulated.

On the other hand, the magnitude is not the same for a phase-to-phase and double-line to ground short circuit. When a 100 ms phase B and phase C to ground short circuit is simulated, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$, are 2.01 pu and -1.38 pu, respectively. The magnitude of $I_{initial\_peak\_positive}$ becomes 0.01 pu smaller when the phase B and phase C are not short circuited to ground. The magnitude of the total fault current also decreases.

When a 100 ms phase C to ground short circuit is simulated, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$, are 1.93 pu and -1.09 pu, respectively.

In the second period, the magnitude of $I_{converter}$ varies for the different short circuit types. For a phase C to ground short circuit, phase C oscillates with a magnitude that is 0.05 pu

larger than during normal operation. The current in phase A and phase B experiences a small decrease in magnitude in this period.

The behaviour during the second period is similar for a phase C and phase B to ground, and phase C to ground short circuit. In both simulations phase C oscillates with a magnitude that is higher than rated value. The largest magnitude oscillations in phase C, occurs when a phase B to phase C short circuit arise. Still, the increase is 0.16 pu, which is negligible.

The behaviour during the third period of the short circuit differs for the different short circuit types. The disturbance in the current is the largest when a three-phase to ground short circuit is applied. The converter control scheme creates more disturbance in the current signals when the phase or phases are short circuited to ground. However, the magnitude is approximately the same, regardless of the fault being short circuited or not, to ground. The impact on the current magnitude is the smallest for a phase C to ground short circuit.

4.3.4 Current Contribution from the Converter versus the Main Supply

Figure 4.3.5 illustrates I_{main_supply} for the same simulation as illustrated in Figure 4.3.1. This figure is included to illustrate the magnitude of the current injected by the main supply.

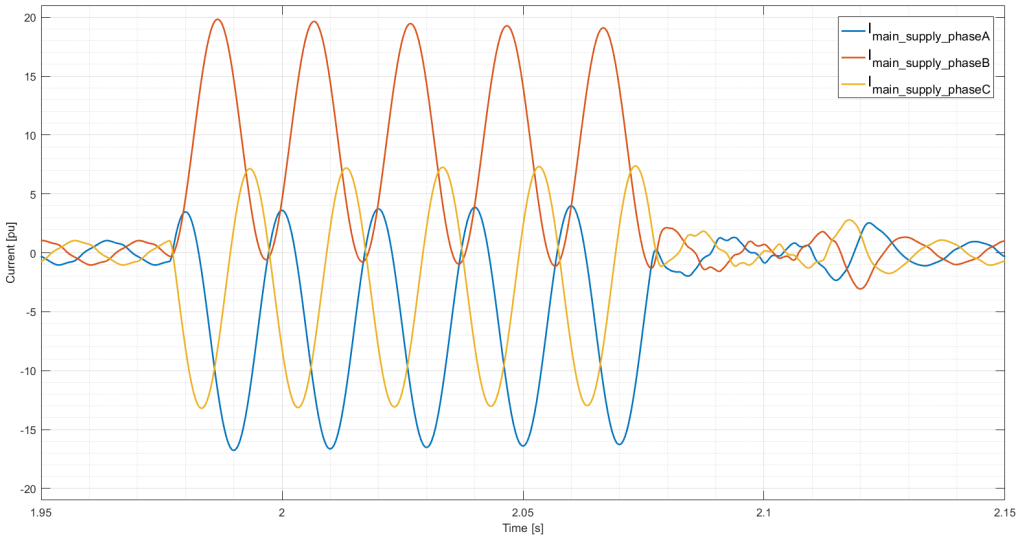


Figure 4.3.5: I_{main_supply} for a 100 ms three-phase short circuit with $I_{d\_reference}$ equal to 1.00 pu.

Opposite to $I_{converter}$, the magnitude of the different phases differs in I_{main_supply}. The largest magnitude can be observed in the first cycle in $I_{main\_supply\_phaseB}$. This magnitude is 19.81 pu. The magnitude decrease throughout the short circuit. Still, in the last cycle of the short circuit the magnitude is 19.10 pu. This is 19 times larger than the peak of $I_{converter}$.

This illustration of the magnitude difference is deemed adequate. The reason is that the magnitude of I_{main_supply} do not exceed this magnitude, in the other simulations. The magnitude of the oscillations in each phase of I_{main_supply}, depends on the time instance the short circuit arises.

4.4 Summary and Conclusion

The main finding from the Simulink simulations, can be summarized in the following statement:

(i) The short circuit current contribution from the converter, is negligible.

The reasoning behind this statement is elaborated in the following.

The short circuit converter current can be divided into three periods. In the first period, the converter current experienced initial peaks. In the second period, the converter current resembled normal operation, but with small magnitude variations. In the third period, the converter current experienced oscillations with various peaks.

The magnitude of the peaks in the first period, depends on T_{start}, $I_{d\_reference}$ and the type of short circuit. The largest initial peak occurred during a three-phase short circuit with $I_{d\_reference}$ equal to 1.25 pu. In this simulation, the $I_{initial\_peak\_positive}$ became 2.56 pu. $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ from the simulations are summarized in Table 4.4.1.

With respect to the normal pick-up setting in over-current protection, this short circuit contribution is small. At the same time, the duration of these peaks is much shorter than the usual time delay in the protection devices. Based on this, an assumption can be made that the impact of these initial peaks is negligible.

The control scheme struggles to regain normal operation, when the short circuit clears. The extent of this struggle, depends on the type of short circuit. The largest impact happens for

three-phase and three-phase to ground short circuits. Compared to the beginning of the short circuit, these oscillations have a magnitude and an occurrence-rate, that are larger. This, combined with the fact that this period is longer, increases the possibility of effecting the trip settings in a relay. However, this poor behaviour is assigned to the simplified converter control scheme. Therefore, the struggle to regain normal operation, is not expected to occur in a real-life application. This illustrates the importance of having a control system constructed to handle irregular system behaviour.

The converter current during the second period, is similar to normal operation. For three-phase and three-phase to the ground short circuits, the magnitude is smaller. When one or two phases are involved, some of the phases have a magnitude that is larger than during normal operation. Still, the increase is small, and thus negligible.

As discussed in Section 4.3.4, the magnitude difference between the injected current from the converter and the main supply, is large. The over-current devices are configured based on this large current injection from the main supply.

For these reasons, the converter short circuit current contribution is negligible in these simulations.

Table 4.4.1: A summary of $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ from the Simulink simulations.

Type of Short Circuit	$\mathbf{I}_{initial\_peak\_positive}$[pu]	$\mathbf{I}_{initial\_peak\_negative}$[pu]
Three-phase$^{(1)}$	2.33 (phase C)	-1.47 (phase A)
Three-phase$^{(2)}$	2.56 (phase C)	-1.54 (phase A)
Three-phase to ground	2.33 (phase C)	-1.47 (phase A)
Phase C to ground	1.93 (phase C)	-1.09 (phase B)
Phase C and phase B to ground	2.01 (phase C)	-1.38 (phase B)
Phase C to phase B	1.91 (phase C)	-1.41 (phase B)

(1): $I_{d\_reference} = 1.00$ pu. (2): $I_{d\_reference} = 1.25$ pu.

Chapter 5

Laboratory Setup and Approach

This chapter presents the laboratory setup and the approach for the tests performed in the Smart Grid Laboratory at NTNU. The purpose of the laboratory tests, is to investigate factors affecting the converter short circuit current contribution. Section 5.1 describes the laboratory setup, and includes descriptions of the required instruments. Section 5.2 summarizes the parameter settings. Section 5.3 describes the approach taken in the laboratory. The results are presented in Chapter 6.

5.1 Laboratory Setup

Figure 5.1.1 illustrates the laboratory setup used when testing.

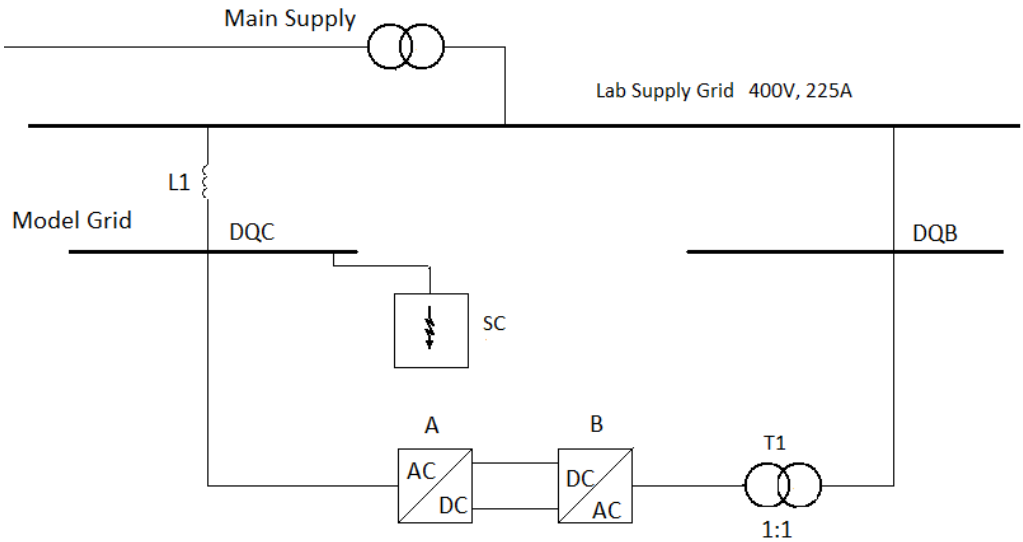


Figure 5.1.1: Sketch of the laboratory setup.

Table 5.1.1 summarizes the instrument-list, and shows the location of these instruments in the sketch in Figure 5.1.1.

In the following, the different instruments are briefly described. Some additional information, can be found in Appendix B.

Table 5.1.1: Laboratory instrument-list.

Instrument Type	**Marked in Figure 5.1.1 with:**	**Lab Number**
Converter	A	B03-0432
Converter	B	B03-0431
Inductor	L1	K01-0135
Transformer	T1	B01-0992
Short Circuit Emulator	SC	R04-0126
Series Inductor	SC	K02-0134
Short Circuit Inductor	SC	K02-0133
Oscilloscope	-	G04-0363

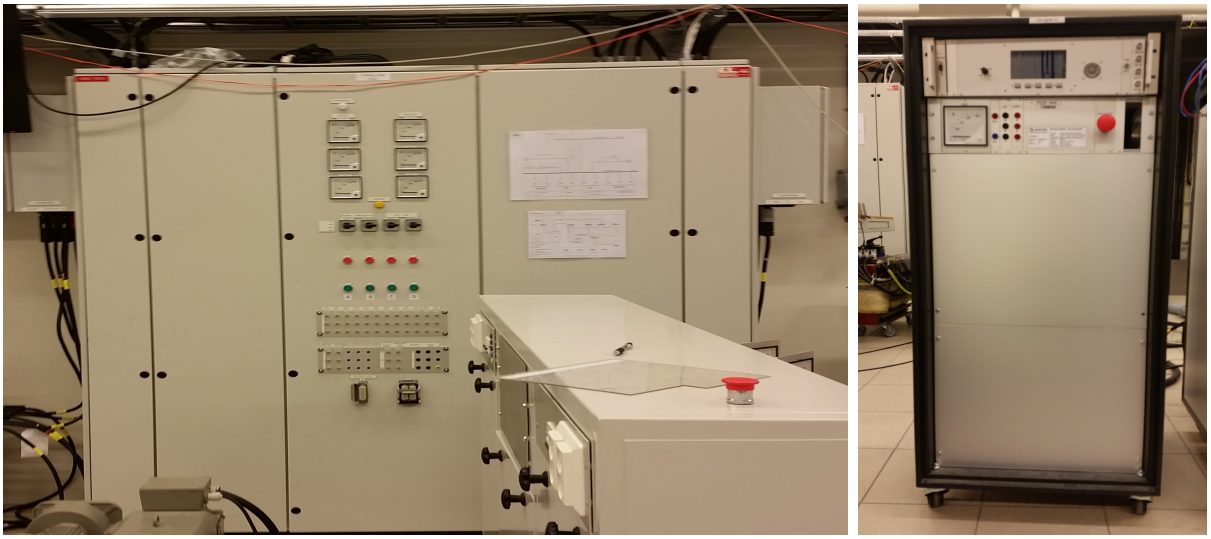
5.1.1 Supply Grid and Model Grid

In the Smart Grid Laboratory, there is a supply grid with an AC voltage level equal to 400 V, and a maximum current rating of 225 A. This grid can be connected to several bus-bars, referred to as the model grid. The AC voltage level at the model grid is 400 V, with a maximum current rating of 125 A. [69]

The bus-bars of interest for the tests, are the DQB and DQC. DQB will be connected directly to the supply grid, while DQC will be connected through an inductor, as illustrated in Figure 5.1.1. Figure 5.1.2 (a) is a picture of the DQC bus-bar in the Smart Grid Laboratory.

5.1.2 Converter Interface

Figure 5.1.2 (b) shows a picture of the box containing the 60 kVA converter used in the tests. This box includes more than just a converter core module, and the integrated grid interface is illustrated in Figure B.1.1 in Appendix B.1.



(a) DQC bus-bar. **(b)** VSC.

Figure 5.1.2: Pictures of the DQC bus-bar and the VSC used in the laboratory tests.

The box consists of a converter core module, a LCL-filter and switchgear. The converter core module is based on a Semikron SEMIKUBE inverter module, and it consists of IGBT-bridges, a DC-link capacitor, drivers, a heatsink and a diode rectifier. In the tests, the active rectifier configuration of the VSC is used. Therefore, the converter is like the VSC described in 2.3.1. [70]

Each inverter module leg consists of two IGBTs of the type SKM 400GB126D. These IGBTs have a maximum voltage tolerance of 1200 V and a maximum switching frequency of 6 kHz. The LCL-filter components can be divided into the converter-side filter inductor, L_{filter_1}, the capacitor, C_{filter}, and the grid-side filter inductor, L_{filter_2}. The converter-side filter is a foil winding transformer. [70]

5.1.3 Converter Control

There are two different options for controlling the converter, either by the built-in control or by using OPAL-RT. In these tests only the built-in control was used, thus only this system will be elaborated on. The built-in control system is integrated in the upper part of the converter, as shown in Figure 5.1.2 (b).

As explained in Chapter 3, the implemented control system is an important factor for the behaviour of the converter connected DG during short circuits. Because of this, the explanation of the built-in control system is described with more detail than the other

aspects of the laboratory setup. For a more comprehensive description, the reader is referred to [71].

The control system can be divided into two systems, the parts implemented as FPGA blocks and the parts implemented as processor software routines. The first system contains the time critical parts of the control system, while the second involves all other parts. Figure 5.1.3 illustrates the signal flow of the control system. The control system has three main signal paths, these are active control, reactive control, and angle reference. In the following, the active and reactive control, current regulator and PLL in the control mechanism will be explained. Both PU-values and real-units are used. In the control, 100% is defined to equal l000 pu. [71]

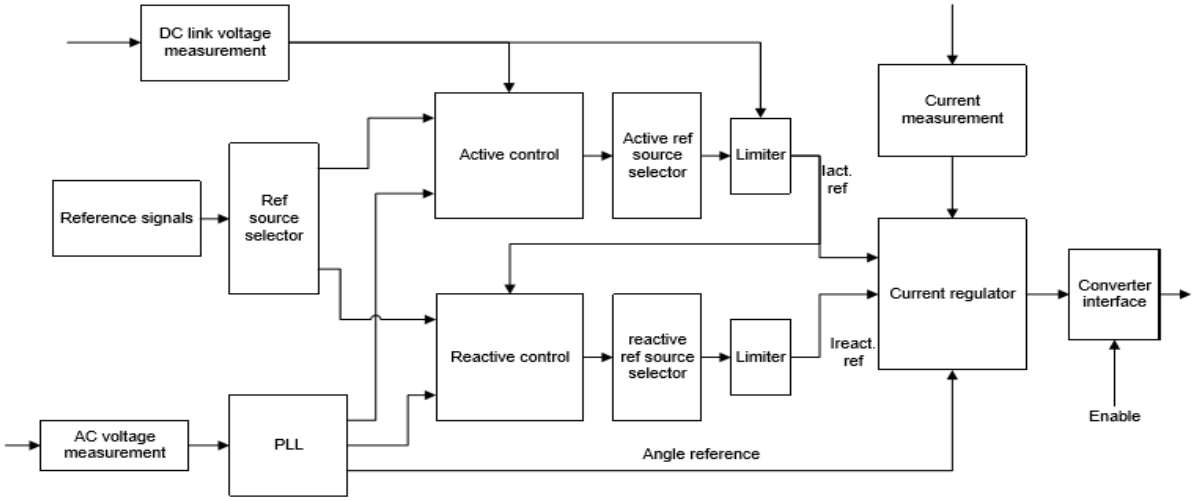


Figure 5.1.3: Schematic drawing of the signal flow in the converter control system [71].

Active and Reactive Control

There are three different ways the active current reference can be generated. The first is by using direct current control, where the active current is controlled directly. The second involves the DC-link voltage regulator. In this setting, the converter controls the DC-link voltage, and leaves the control of the AC-side to another device. The third method is by frequency control. This method requires that there are rotating machines present in the grid, and that the active power flow controls the grid frequency. In this situation, the DC-link voltage needs to be controlled by another unit. [71]

There are three different ways of obtaining the reactive current control reference. The first is by direct current control. The second is through a reference that is proportional to the active

current reference, which gives a constant phase angle operation. The third option is through the AC voltage regulator. This leads to the converter operating as a static compensator, by trying to keep the AC voltage stable. This mode operates on the assumption that the system is symmetric, and therefore it only controls the positive sequence voltage. [71]

Current Regulation

The inner loop of the control system controls the current. Unlike traditional analog current controllers, a large part of the control system is implemented as FPGA IP modules. Due to a high sampling rate, the regulator output signal will vary instantaneously with the current error. There are three different regulators available, these are phase current PI regulator, DQ current regulator, and DQ hysteresis regulator. [71]

The current control scheme is illustrated Figure 5.1.4. It should be noted, that all three regulator options are included in this illustration.

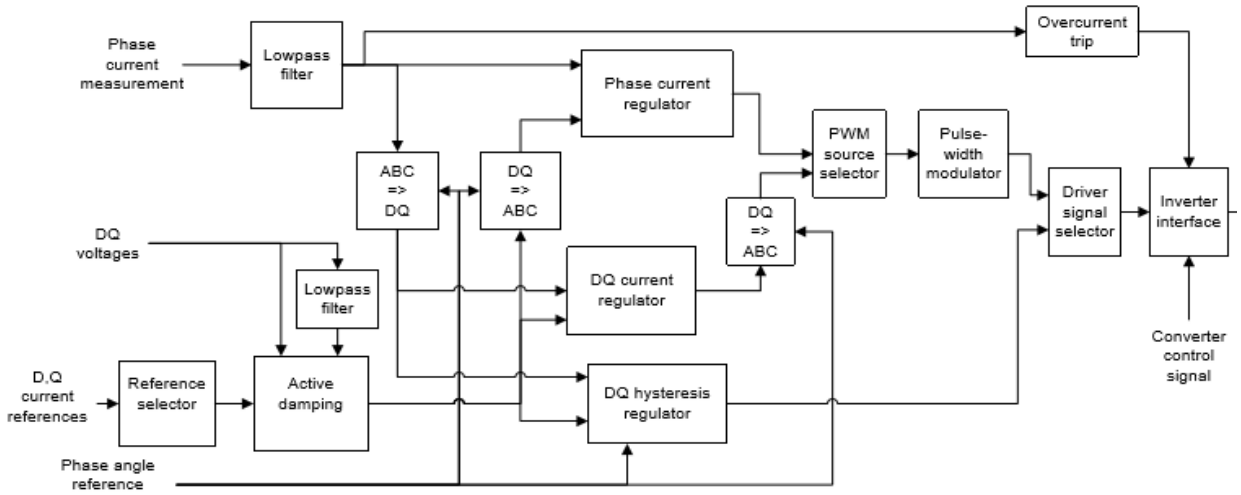


Figure 5.1.4: The current control scheme [71].

The signals to the current regulators are sent through an active damping regulator to handle the poorly damped resonance circuit introduced by the LCL-filter, mentioned in Section 5.1.2. Problems associated with resonance circuit, can occur in situations with transient events or signal components at resonance frequency, which can lead to severe oscillations. [71]

The phase current PI regulator is constructed of three individual PI regulators, one for each phase. The input signals are then in the *abc*-frame. In the DQ current regulator the input signals are in the *dq*-frame. Similar for the two regulators, is that they both deliver voltage

output signals in the *abc*-frame to the PWM. The DQ hysteresis regulator is a valid option, for situations where the PWM is not fast enough. One example of such situations being the rapid response to transients. This regulator is connected directly to the driver signal selector. [71]

Phase Locked Loop

The PLL structure implemented in the control mechanism is illustrated in Figure 5.1.5. This PLL is complex and contains features that are not common in a standard PLL. It should be noted that the shaded area is implemented in FPGA. The measured grid voltages are transformed to the *dq*-frame and then filtered in the FPGA. The filters contribute with removal of high frequency components and harmonics from the PLL output signal. [71]

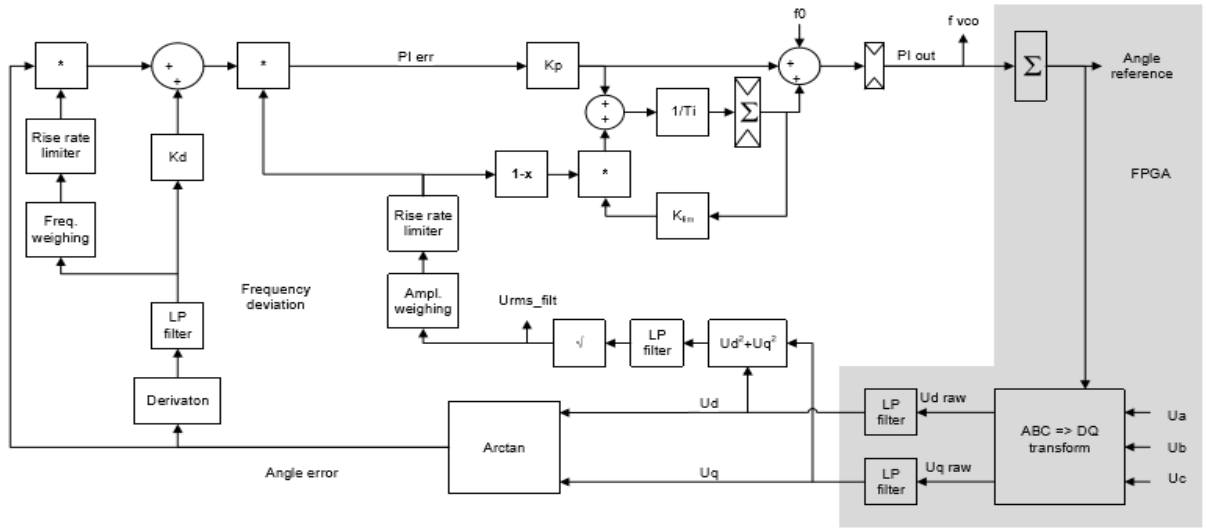


Figure 5.1.5: Built-in phase-locked-loop structure [71].

The PLL can be transformed into a frequency looked loop. This transformation occurs when the weighted factor signal, multiplied with the phase error signal, is reduced. The benefit appears in situations where the frequency error is large, and a PLL that tries to catch the phase angle is unwanted. [71]

User Interface

The user interface is a LCD display with a corresponding set of control buttons, as shown in Figure 5.1.6. Through this user interface, one can set parameter values and control signals, and analyze state and measurement values. [71].

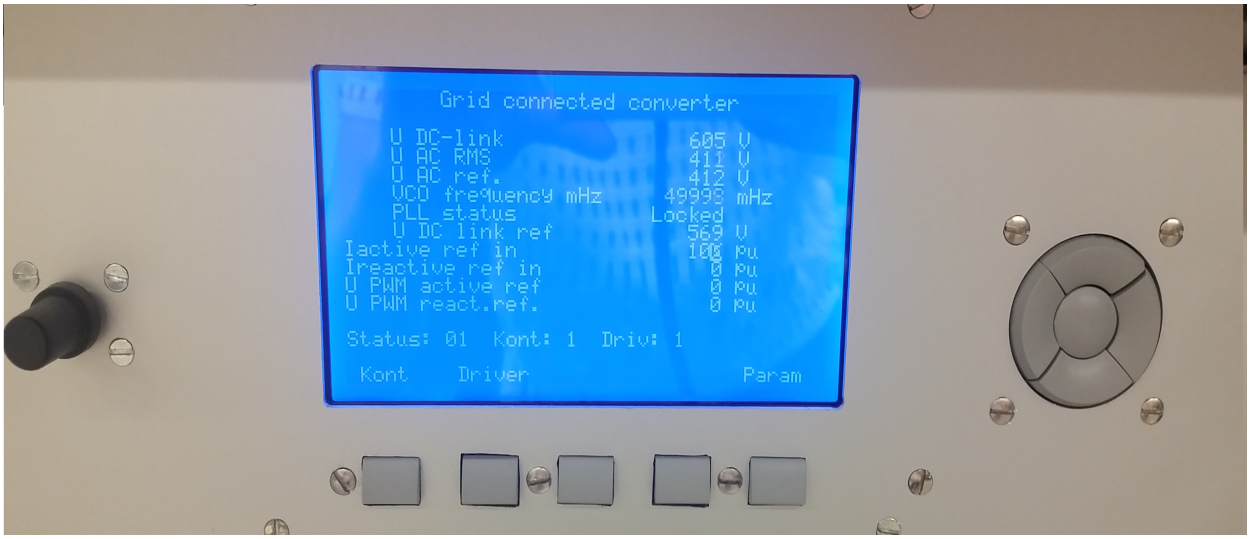


Figure 5.1.6: The user interface of the VSC control system.

While the converter is in operation, the display shows an actual value list and an input list, as well as status code, contactor code and driver code. Before start of operation, the user can configure which values the actual value list should entail. [71]

The input list depends on the source chosen to be the signal source. There are four reference signal source options, these are the fixed parameter values option, the menu option, the from PC via debugger option and the remote control via CAN bus option. For the tests in this thesis, only the first two options are of interest. If the control signal source is selected to be the menu option, then the input list consists of the active control signals of this configuration mode. If the fixed parameter value option is selected, no values can be changed during the operation. [71]

There are a total of 22 parameter values and control signal lists available, which indicate the wide range of operational possibilities and the flexibility in this control system. Some important options in these lists will briefly be mentioned here. For a complete overview of the available parameter value lists and the control signal lists, the reader is referred to Appendix B.1.

The reference signal source can be set in the Signal Parameter list. Another important list is the Operation Mode Parameters, where the active and reactive control mode is set. Choosing between the current regulators is done in the Current Regulator Parameters list. The rated DC voltage will be set in the U DC link Regulator Parameters list.

5.1.4 Short Circuit Emulator

The short circuit is simulated with a short circuit emulator connected as illustrated in Figure 5.1.1. Figure 5.1.7 (a) shows a sketch of how the short circuit emulator is constructed, while 5.1.7 (b) is a picture of it.

The short circuit emulator is built up of a triac connected thyristor bridge connected in series with a supply inductor, $L_{SCemulator\_supply}$, and a short circuit inductor, $L_{SCemulator\_SC}$. The bypass contactor is in parallel with the supply inductor, to ensure a low impedance path when no fault is present. While the thyristor bridge is inside the unit, the two inductors are external units. This makes it easy to change them, which is important as these inductors affect the short circuit level. By changing the supply inductor, the current drawn by the supply grid under fault, can be controlled. [72]

(a) Circuit diagram [72]. **(b)** Design.

Figure 5.1.7: Short circuit emulator used in the laboratory tests.

The short circuit emulator can create three-phase and phase-to-phase short circuits. The parameter settings can be changed through a display with a corresponding set of control buttons. Other parameter settings are T_{short}, T_{pre}, T_{post} and T_{sync}. T_{short} is the time interval of the short circuit. T_{pre} set the time between when the bypass contactor is out and the synchronization starts. T_{post} is the time from the short circuit is finished until the bypass contactor is reconnected. T_{sync} is the time between the zero-voltage crossing of the auxiliary supply and the start of the short circuit. [72]

5.1.5 Measurements

The current and voltage measurements are made with an oscilloscope of the model type MSO3014. The scope can measure four different signals at the same time. To be able to document the rapid change in the converter current during short circuits, the record length is set to 1M. This means that the recorded data will contain 1 million measuring points. At the same time, the acquisition mode is set to Hi res, to remove some of the signal noise.

There are three different three-phase currents measured in the laboratory tests. These are I_{main_supply}, I_{fault} and $I_{converter}$. I_{main_supply} and $I_{converter}$ is measured at the measuring outtakes, MATENETT and UE218, respectively. I_{fault} is measured with pliers ammeter at the output cables of the short circuit emulator. The positive direction of I_{main_supply} and I_{fault}, are defined into the DQC bus-bar and out of the DQC bus-bar, respectively. This is the same direction as their measured current signals. The positive direction of $I_{converter}$, is defined into the DQC bus-bar. The UE218 outtake measures the current in the opposite direction, and therefore this current measurement is given the opposite sign, afterwards in MATLAB. This is done to make the following equation valid:

$$I_{fault} = I_{main\_supply} + I_{converter}$$

5.2 Parameter Settings

This section presents a summary of the parameter settings used in the laboratory tests. Table 5.2.1 summarizes the rated parameter values of the converters. These can be varied, and therefore these values are taken from the actual settings in the built-in converter control.

In Table 5.2.2 the different impedance parameters used in the circuit are summarized. The short circuit impedance, Z_{sc}, consists of $L_{SCemulator\_supply}$ ans $L_{SCemulator\_SC}$.

Table 5.2.3 summarizes the settings of T_{short}, T_{pre}, T_{sync} and T_{post}. For T_{short} and T_{sync} intervals are given, since these values will be changed during the tests. This will be specified clearly in each situation. These values could be changed to values exceeding the intervals defined here.

Table 5.2.1: The rated value settings in the converters.

Parameter	Value
V_{DC_rated}	600 [V]
$V_{AC\_rated\_rms}$	400 [V]
I_{rated_rms}	90 [A]

Table 5.2.2: The inductor and capacitor impedance settings.

Impedance	Value
L_{filter_1}	500 [μH]
L_{filter_2}	200 [μH]
C_{filter}	50 [μF]
L_1	1 [mH]
$L_{SCemulator\_supply}$	1 [mH]
$L_{SCemulator\_SC}$	1 [mH]
Z_{sc}	2 [mH]

Table 5.2.3: The short circuit emulator settings.

Parameter	Value
T_{short}	100-500 [ms]
T_{pre}	50 [ms]
T_{post}	20 [s]
T_{sync}	6.6-20.0 [ms]

5.3 Approach

The control scheme for converter B will be the same throughout the tests. Converter B is controlled to imitate a constant DC-source with a voltage level of 600 V. The reason for this is that it will cause converter A to imitate the grid interface between a DG and the grid.

Converter A will be controlled with two different control schemes. The main difference between these, is the Reactive Control Mode. The difference between the control scheme in

scenario 1 and the control scheme in scenario 2, is summarized in Table 5.3.1.

In both control schemes, the current regulation is performed by PI regulators in the *dq*-frame. Additional parameter settings and control signal settings can be found in Table B.1.1 in Appendix B.1.

Table 5.3.1: Converter control scheme configurations.

Control Scheme Scenario 1	**Converter A**	**Converter B**
Active Control Mode	I active	U DC regulation
Reactive Control Mode	I reactive	Proportional with I active
Control Scheme Scenario 2	**Converter A**	**Converter B**
Active Control Mode	I active	U DC regulation
Reactive Control Mode	U AC regulation	Proportional with I active

In the converter control system some parameters are specified in PU-values. An important remark is that the PU-values in the control system are created based on a definition where 100% equals 1000 pu. This is different from the norm, where 100% usually equals 1 pu. For clarity: the PU-values from the built-in control will be transformed to the preferred PU definition. In other words, in the following 1 pu equals 100% of the base value.

5.3.1 Control Scheme in Scenario 1

In the control scheme scenario 1, the active and reactive current are directly controlled in converter A. This control scheme is common for converter connected DG. To investigate the impact of control parameters and external factors, tests with different short circuit types and parameters will be conducted. The approach can be divided into several cases, where one setting is varied in each case.

Three-Phase Short Circuits

Firstly, three-phase short circuits will be tested. For this type of short circuit, I_{active_ref}, T_{sync}, T_{short} and Z_{sc} will be varied one at the time. Therefore, four cases will be tested, and these are summarized in Table 5.3.2. While one setting is varied, the other three are kept constant. The constant values are given in the original settings column in Table 5.3.2.

T_{short}, T_{sync} and Z_{sc} are parameters related to the short circuit emulator. These are included to see how external parameters effect the converter behaviour during short circuit. The active reference signal of the current control, I_{active_ref}, illustrates how simple changes in the control scheme effects the behaviour during short circuits. It also illustrates how important the converter settings are.

Table 5.3.2: Parameter changes in the control scheme in scenario 1, for three-phase short circuits.

Case	Varying Parameter	Original Settings	Values				
1.1	$\mathbf{I}_{active\_ref}$ [pu]	0.10	0.20	0.30	0.40	1.00	-
1.2	$\mathbf{T}_{synch}$ [ms]	9.8	6.6	13.3	16.6	18.3	20.0
1.3	$\mathbf{T}_{short}$ [ms]	100	200	300	500	-	-
1.4	$\mathbf{Z}_{sc}$ [mH]	2	1	-	-	-	-

Phase-to-Phase Short Circuit

Secondly, phase-to-phase short circuits will be performed. Two type of phase-to-phase short circuits will be tested. To limit the number of tests, a different approach has been chosen for phase-to-phase short circuits. In the following the reasoning behind this decision, is explained.

The parameters that will be changed are I_{active_ref} and T_{synch}. T_{synch} impacts the instance of the short circuit occurrence, and is therefore an important parameter. I_{active_ref} is changed, to illustrate the impact of the control parameters.

T_{short} and Z_{sc} will be held constant at 100 ms and 2 mH, respectively. The impact of T_{short} is small. Therefore, the tests performed with T_{short} in case 1.3, are deemed adequate. Z_{sc} impacts the total current contribution, not only the converter current. This is an interesting aspect, but the tests in case 1.4 are an acceptable coverage of this field.

Fewer parameter changes have been made when phase A to phase C short circuits have been tested. This is because the results will be similar to the ones achieved through testing of phase A to phase B short circuits.

Therefore, three different cases will be tested, and these are summarized in Table 5.3.3.

Table 5.3.3: Parameter changes in the control scheme in scenario 1, for phase-to-phase short circuits.

Case	Varying Parameter	Type of Fault	Values				
1.5	$\mathbf{I}_{active\_ref}$ [pu]	A-B	0.10	0.40	-	-	-
1.6	$\mathbf{T}_{synch}$ [ms]	A-B	6.6	8.3	9.8	9.9	13.3
1.7	$\mathbf{I}_{active\_ref}$ [pu]	A-C	0.10	0.40		-	-

5.3.2 Control Scheme in Scenario 2

In the control scheme in scenario 2, the Reactive Control Mode of converter A is changed to the U AC reference mode. As described in Section 5.1.3, in this reactive control mode the converter will try to keep the AC voltage stable. As the penetration level of converter connected DG increases, requirements regarding voltage support could emerge. Therefore, this control scheme might be used more in the future.

To limit the number of tests, only three-phase short circuits will be tested here. This decision is also based on the fact that reactive control achieved through AC voltage regulation, is constructed based on the system being symmetric. This was mentioned in Section 5.1.3. With the two converters being controlled with the control scheme in scenario 1, V_{AC} became 411 V. Therefore, the AC voltage level, V_{AC} is set to 411 V in the control scheme in scenario 2.

As for the control scheme in scenario 1, one test will be performed with parameter settings at the original settings. These settings are I_{active_ref} equal to 0.10 pu, T_{synch} equal to 9.9 ms and T_{short} equal to 100 ms. The rest of the parameters have values equal to the ones given Section 5.2. In each case one parameter will be changed, while the rest are held constant. In case 2.1, I_{active_ref} will be changed to 0.40 pu. In case 2.2, T_{synch} will be changed from 6.6 ms to 20.0 ms. Finally, in case 2.3, T_{short} will be changed to 50 ms and 300 ms. Table 5.3.4 gives a summary of the three cases tested.

Table 5.3.4: Parameter changes in the control scheme in scenario 2, for three-phase short circuits.

Case	**Varying Parameter**	**Original Settings**	**Values**		
2.1	$\mathbf{I}_{active\_ref}$ [pu]	0.10	0.40	-	-
2.2	$\mathbf{T}_{synch}$ [ms]	9.8	6.6	13.3	20.0
2.3	$\mathbf{T}_{short}$ [ms]	100	50	300	-

Chapter 6

Laboratory Results

This chapter presents important findings from the laboratory tests. Several tests were performed, and have resulted in a substantial amount of data. While this chapter focus on the important findings, additional results can be found in Appendix C. The results will not be presented in a chronological order with respect to the approach described in Section 5.3. Instead, the presentation will be according to the research questions listed in Section 1.2. Two control schemes have been tested, and the difference between these schemes have been described in Table 5.3.1. In the following, the control schemes will be referred to as control scheme 1 and control scheme 2.

Section 6.1 describes the shape of the converter current during short circuits. Section 6.2 describes the impact of the control parameters on the converter current contribution, while Section 6.3 describes the impact of external factors. In Section 6.4 the impact of the two types of control schemes are further elaborated and compared. Section 6.5 discusses the ratio between the short circuit current injected by the converter and the main supply. The results will be discussed throughout this chapter, and in Section 6.6 a summary of the results is presented.

Before presenting the results, the following should be noted:

- The positive direction of $I_{converter}$, is defined out of converter A. The positive flow direction of I_{main_supply} and I_{fault}, are defined into the DQC bus-bar and out of the DQC bus-bar, respectively. The reason for this is mentioned in Section 5.1.5.
- The current and voltage measurements are given in PU-values. The current base and

the voltage base value, are 90 A and 400 V, respectively. These values are RMS values, and are the base values used in the built-in control of converter A.

- To be able to compare the results more easily, a set of parameters is used. The set of parameters differs from control scheme 1 and control scheme 2. The set of parameters for each control scheme, are explained in Table 6.0.1. The reasons for choosing these parameters, are given in Appendix C.1.
- There are noise in the converter current signals. This makes it difficult to precisely determine the current magnitude. Therefore, all measurements should be regarded as indication of the actual values. The cause of the noise will be discussed in Section 6.6.4.

Table 6.0.1: Parameter set for presenting the laboratory results.

Control Scheme 1	**Explanation**(1)
$I_{initial\_peak\_positive}$	The positive initial peak occurring at the start of the short circuit.
$I_{initial\_peak\_negative}$	The negative initial peak occurring at the start of the short circuit.
$R_{\frac{SC}{normal}}$	Ratio between the initial peak and the peak during normal operation.
Control Scheme 2	
I_{sc_max}	The maximum peak current during the short circuit.
$R_{\frac{SC\_max}{normal}}$	The ratio between I_{sc_max} and the peak during normal operation.

(1) Detailed explanations can be found in Appendix C.1.

6.1 Shape of the Converter Current

This section investigates the shape of the converter short circuit current. The current behaviour will be described separately for the two control schemes.

Control Scheme 1

The shape of $I_{converter}$ turned out to be similar, throughout the tests with control scheme 1. Figure 6.1.1 illustrates $I_{converter}$ for a 100 ms three-phase short circuit, with this control scheme. The parameter settings are equal to the original settings in Table 5.3.2.

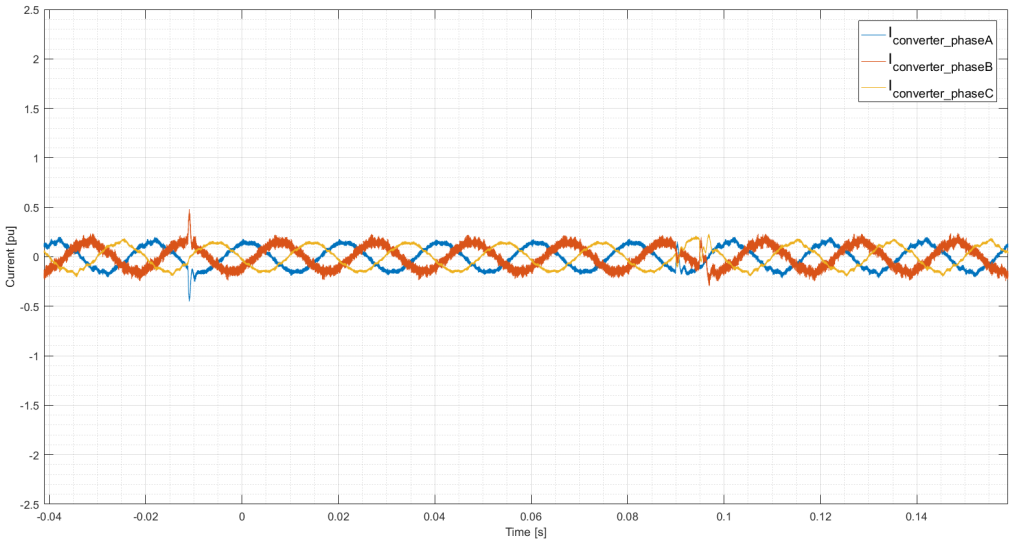


Figure 6.1.1: $I_{converter}$ for a 100 ms three-phase short circuit with I_{active_ref} equal to 0.1 pu, T_{sync} equal to 9.8 ms and Z_{sc} equal to 2 mH, with control scheme 1.

Figure 6.1.1 and Figure 6.1.2 have the same y-axis. This is to clearly illustrate the magnitude difference between these two control schemes. This will be further elaborated in Section 6.4. However, in the following the graphs illustrating the converter current with control scheme 1, will have more appropriate y-axes.

In order to describe the behaviour more easily and to facilitate comparison between the tests, the short circuit duration is divided into three periods. This division is based on the varying converter current behaviour during these periods.

The first period refers to the beginning of the short circuit. During this period, a positive and a negative peak occurs in $I_{converter}$. For the test in Figure 6.1.1, $I_{initial\_peak\_positive}$ is equal to 0.48 pu, while $I_{initial\_peak\_negative}$ is equal to -0.45 pu. $R_{\frac{\_sc\_}{normal}}$ is equal to 2.8 in phase B and equal to 2.6 in phase A.

The second period is the longest interval of the short circuit. In this period, the current behaviour resembles the normal operation, but with different magnitude.

The third period, starts when the short circuit is cleared and lasts until normal operation is reached. In this period, several peaks occur in $I_{converter}$, and because of that, the period to some extent is similar to the first period. The magnitude of these peaks is dependent on the time the short circuit is cleared. This aspect will be addressed in Section 6.3.

Control Scheme 2

The shape of $I_{converter}$ turned out to be similar, throughout the tests with control scheme 2. Figure 6.1.2 illustrates $I_{converter}$ for a 100 ms three-phase short circuit, with this control scheme. Except from the Reactive Control Mode being different, all other parameters are similar in the tests illustrated in Figure 6.1.1 and Figure 6.1.2.

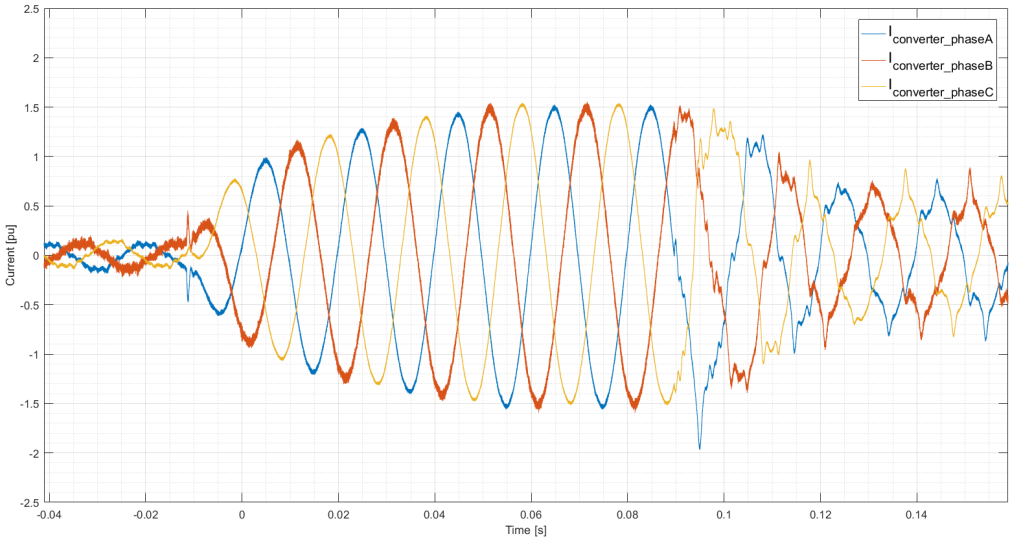


Figure 6.1.2: $I_{converter}$ for a 100 ms three-phase short circuit with I_{active_ref} equal to 0.1 pu, T_{sync} equal to 9.8 ms and Z_{sc} equal to 2 mH, with control scheme 2.

With control scheme 2, the converter current behaviour, can be divided into three periods, based on the corresponding behaviour during these intervals.

In the first period, peaks occur in the positive and negative cycle. The magnitudes of these peaks are small compared to the magnitude of $I_{converter}$ during the rest of the short circuit. In the test result illustrated in Figure 6.1.1, $I_{initial\_peak\_positive}$ becomes 0.45 pu. For the same test, I_{sc_max} becomes 1.53 pu. This illustrates that the magnitude of the initial peak, is no longer the largest.

In the second period, $I_{converter}$ increases with respect to normal operation, until it reaches a magnitude which ensures stable operation. With the parameter settings in Figure 6.1.1, this value, I_{sc_max}, is equal to 1.53 pu. This happens approximately 69 ms after the short circuit occurs. After this, the magnitude of the oscillations in $I_{converter}$ is constant. In this test, the ratio between I_{sc_max} and the peak during normal operation, $R_{\frac{SC\_max}{normal}}$ is equal to 10.4.

The third period, starts when the short circuit is cleared and lasts until the control scheme regain normal operation. In this period, peaks with large magnitudes arise. The magnitude of these peaks is illustrated with Figure 6.1.2. In this situation, a peak occur in phase A with a magnitude of -1.97 pu. This could be seen as an evidence that the end of the short circuit is becoming more important. Still, the duration of the peak is short, so by itself it does not play a major role. It should be mentioned, that the observed behaviour in this period differ to some extent, from when control scheme 1 is implemented. This will be explained further in Section 6.4. After the initial peak, the converter current decreases. However, for the time frame captured in this test, the control is not able to regain normal operation. The decay of $I_{converter}$ is slow, with this control scheme. This indicates that the converter scheme struggles to regain normal operation after the short circuit is cleared.

The shape of the converter short circuit current could be dived into three periods, for both control schemes. However, the magnitude $I_{converter}$ in the different short circuit tests, will vary. This will be elaborated in Section 6.2 and Section 6.3.

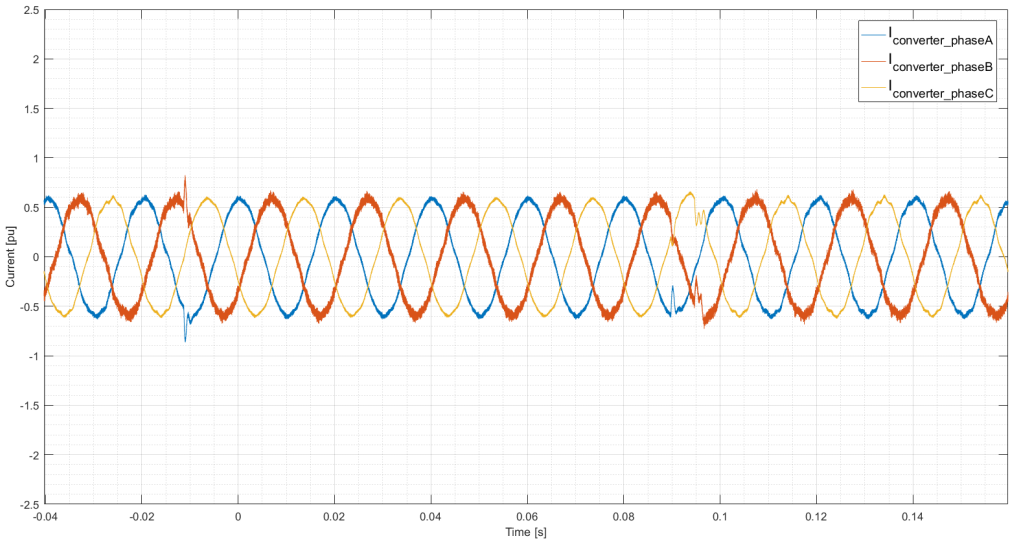
In the test results presented in the following sections, one parameter is changed at the time. If nothing else is specified, the other variable parameters will be equal to the original settings in Table 5.3.3 and Table 5.3.4.

6.2 Impact of Control Parameters

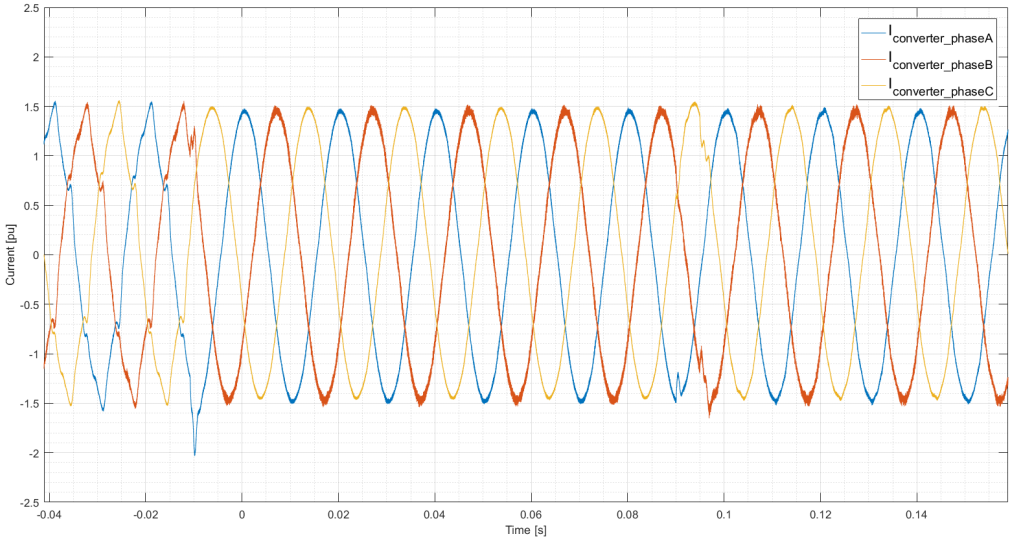
In order to investigate the impact the variation of control parameters has on $I_{converter}$, I_{active_ref} has been varied. The impact of this variation will be described separately for the two control schemes.

Control Scheme 1

Figure 6.2.1 illustrates $I_{converter}$, when I_{active_ref} varies from 0.40 pu to 1.00 pu, with control scheme 1. When the tests were performed, I_{active_ref} was also changed from 0.20 pu to 0.30 pu. Still, the graphs in Figure 6.2.1 are deemed adequate to illustrate the effect of an increasing I_{active_ref}. $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{SC}{normal}}$ for the other values of I_{active_ref}, can be found in Table C.2.1 in Appendix C.2.



(a) $I_{active\_ref} = 0.40$ pu.



(b) $I_{active\_ref} = 1.00$ pu.

Figure 6.2.1: $I_{converter}$ for a 100 ms three-phase short circuit for different values of I_{active_ref}, with control scheme 1.

In the following, Figure 6.1.1 and Figures 6.2.1 (a) and (b) will be compared.

In the first period of the short circuit, peaks occur for both values of I_{active_ref}. However, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ increases when I_{active_ref} increases. To exemplify, when I_{active_ref} increases from 0.10 pu to 1.00 pu, $I_{initial\_peak\_positive}$ increases from 0.48 pu to 1.55 pu. The same increase of I_{active_ref}, changes $I_{initial\_peak\_negative}$ from -0.45 pu to -2.03 pu.

In the second period of the short circuit, the converter current behaviour is similar when I_{active_ref} is varied. However, the magnitude of the oscillations differs. The magnitude increases when I_{active_ref} increases. This is as excepted, because the control scheme regulates the converter back to normal operation in the second period. A higher I_{active_ref} increases the magnitude during normal operation.

An interesting observation is that the difference between the peak and the normal operation decreases as I_{active_ref} increases. When I_{active_ref} is equal to 0.10 pu, $R_{\frac{SC}{normal}}$ in phase A is equal to is 2.6. On the other hand, when I_{active_ref} is equal to 1.00 pu, $R_{\frac{SC}{normal}}$ in phase A is only 1.3. Even though the $R_{\frac{SC}{normal}}$ ratios are approximations, this result indicates that the higher the normal operational current, the lower the ratio between the normal and the initial peak current. $R_{\frac{SC}{normal}}$ in phase B decreased from 2.8 to 1.0.

The magnitude of the peaks occurring in the third period are negligible. The disturbance decreases as I_{active_ref} increases. When I_{active_ref} is 1.00 pu, the disturbance is almost negligible.

Control Scheme 2

In Figure 6.2.2 the converter current behaviour is illustrated for I_{active_ref} equal to 0.40 pu, with control scheme 2. When I_{active_ref} increases from 0.10 pu to 0.40 pu, the magnitude of the peaks in the first period of the short circuit increases. To exemplify, $I_{initial\_peak\_positive}$ increased from 0.45 pu to 0.72 pu, for this increase in I_{active_ref}. This is the same effect as when I_{active_ref} was changed with control scheme 1.

The impact of varying I_{active_ref} is small in the second period of the short circuit. When I_{sc_max} is 0.10 pu and 0.40 pu, I_{sc_max} is equal to 1.53 pu and 1.61 pu, respectively. This means that the difference between the two situations is only 0.08 pu. This indicates that the short circuit behaviour during the second period is not dependent on I_{active_ref}.

Variations in I_{active_ref} cause similar behaviour during the third period. When I_{active_ref} is 0.40 pu, a peak occurs with a magnitude of -1.94 pu. Then the oscillations decays to a magnitude below 1.00 pu. This decay takes approximately one time period. After this the decay of $I_{converter}$ is slow. The reason being that the control struggles to reach normal operation.

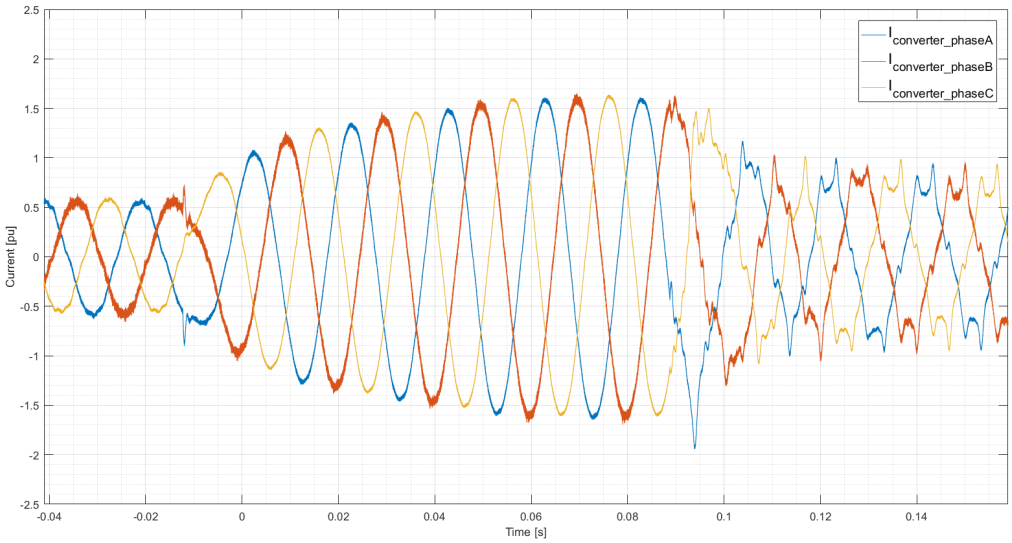


Figure 6.2.2: $I_{converter}$ for a 100 ms three-phase short circuit for I_{active_ref} equal to 0.40 pu, with control scheme 2.

6.3 Impact of External Factors

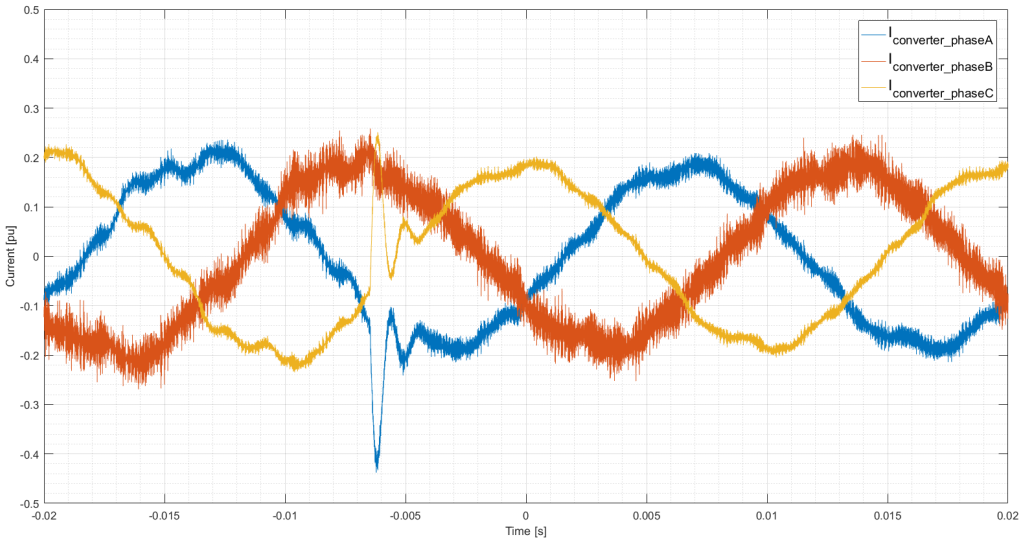
This section presents the impact of the following external factors:

1. Time of occurrence, T_{sync}
2. Short circuit duration, T_{short}
3. Short circuit impedance, Z_{sc}
4. Type of short circuit

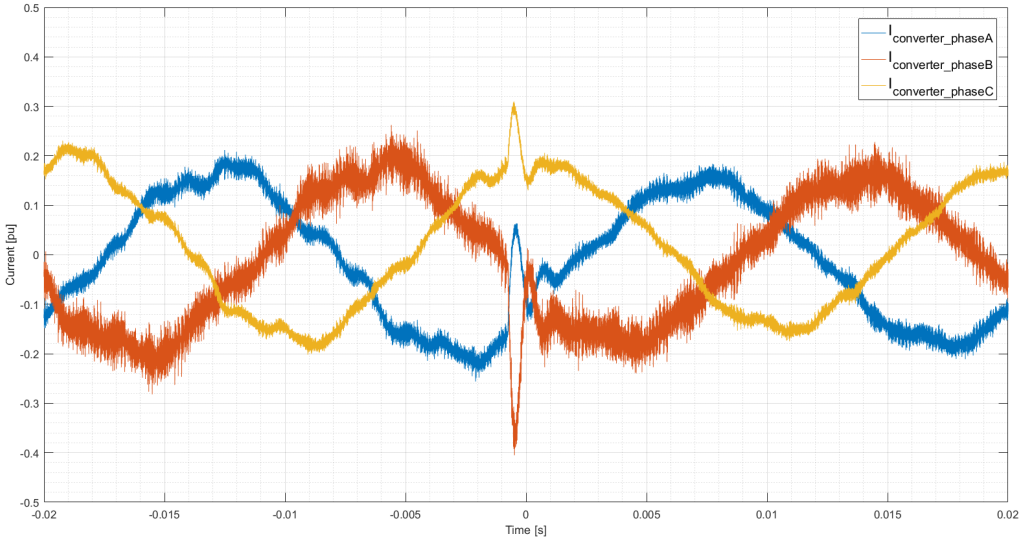
These parameters were tested for values beyond the ones described in this section. Still, the results presented will describe the effect of these parameters in an adequate manner.

Time of Occurrence

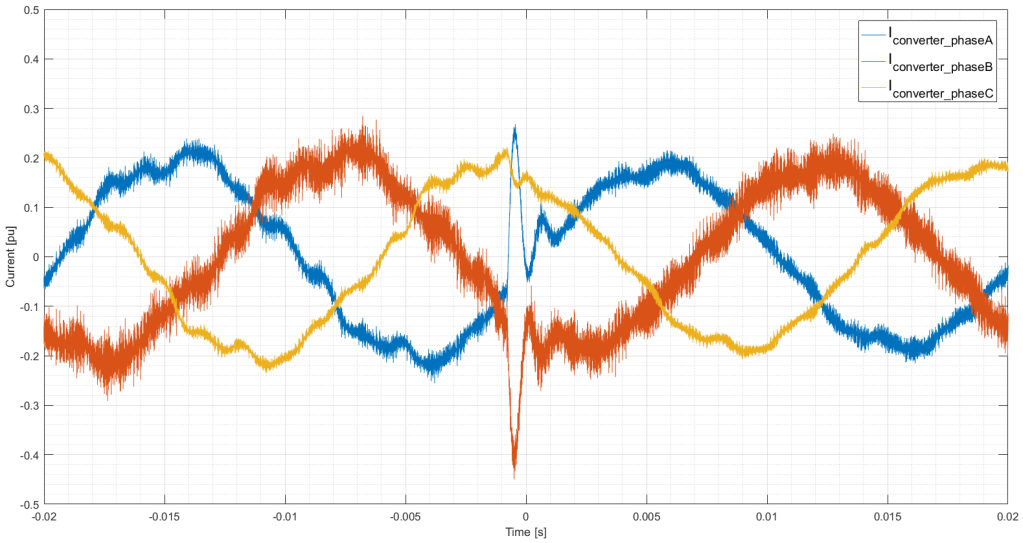
The varying T_{sync} only affects the first and third period of the short circuit. Therefore, only the first and third period are discussed here. The behaviour during the first period, is similar with both control schemes. For this reason, the effect of T_{sync} will be illustrated only with control scheme 1 results. Figure 6.3.1 illustrates the beginning of the short circuit for different values of T_{sync}, with control scheme 1. The full short circuit duration when T_{sync} is equal to 13.3 ms, is illustrated in Figure C.3.1 in Appendix C.3.



(a) T_{sync} = 13.3 ms.



(b) T_{sync} = 18.3 ms.



(c) T_{sync} = 20.0 ms.

Figure 6.3.1: $I_{converter}$ for a 100 ms three-phase short circuit for different values of T_{sync}, start of short circuit, with control scheme 1.

As shown in Figure 6.3.1 (a) to (b), which phase experiencing the initial peak, depends on T_{sync}. When T_{sync} is equal to 13.3 ms, the initial negative peak arises in phase A, while for T_{sync} equal to 18.3 ms the initial peak arises in phase B.

Figure 6.3.1 (b) to (c) illustrates as T_{sync} increases from 18.3 ms up to 20.0 ms, $I_{initial\_peak\_negative}$ increases from -0.41 pu to -0.44 pu. In the same interval of T_{sync}, $I_{initial\_peak\_positive}$ decreases from 0.31 pu to 0.27. This can also be illustrated with the help of the $R_{\frac{SC}{normal}}$ ratio, which changes from 1.9 to 2.0 in phase B, when T_{sync} changes from 18.3 ms to 20.0 ms.

The following describes, the converter current behaviour during the third period. With control scheme 1, the converter current experiences peaks in the current during this period. As mentioned in Section 6.1, the magnitude of these peaks is dependent on the time instance the short circuit is cleared. This is illustrated in Figure 6.3.2.

A comparison of Figure 6.3.2 and Figure 6.3.1 (a), shows that more peaks occur during the third period. A further distinction between these two periods, is that peaks occur in all three phases during the third period. One reason, is that the control scheme struggles more when the short circuit is being cleared versus when it arises.

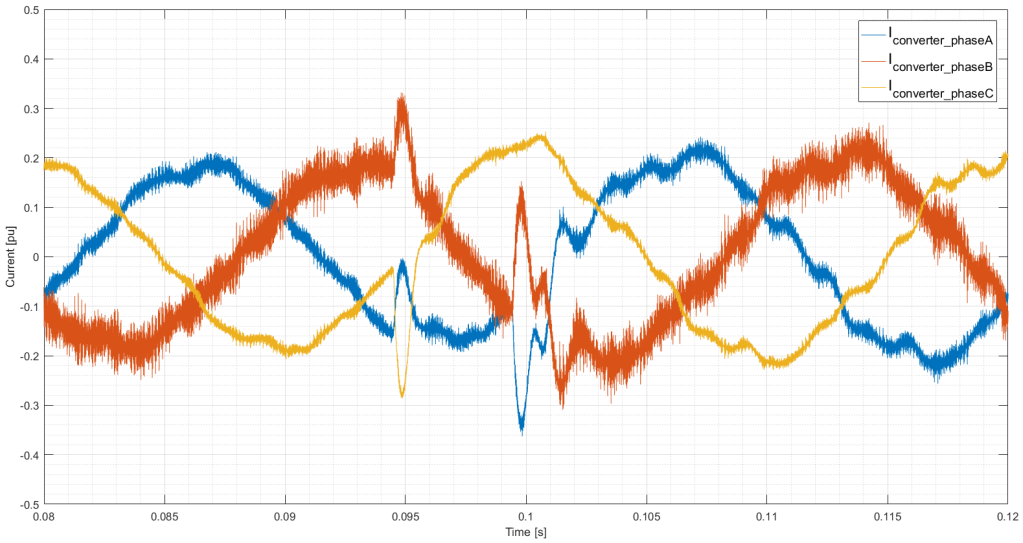


Figure 6.3.2: $I_{converter}$ for a 100 ms three-phase short circuit for T_{sync} equal to 13.3 ms, end of short circuit, with control scheme 1.

As previously mentioned, the current behaviour during the first period is similar with control scheme 1 and control scheme 2. While the current behaviour during the third period is different with these two control schemes, the impact of T_{sync} is the same. Therefore, the test results with control scheme 2 and a varying T_{sync} are not illustrated in this section. However, illustrations of these results, can be found in Figure C.3.2 in Appendix C.3.

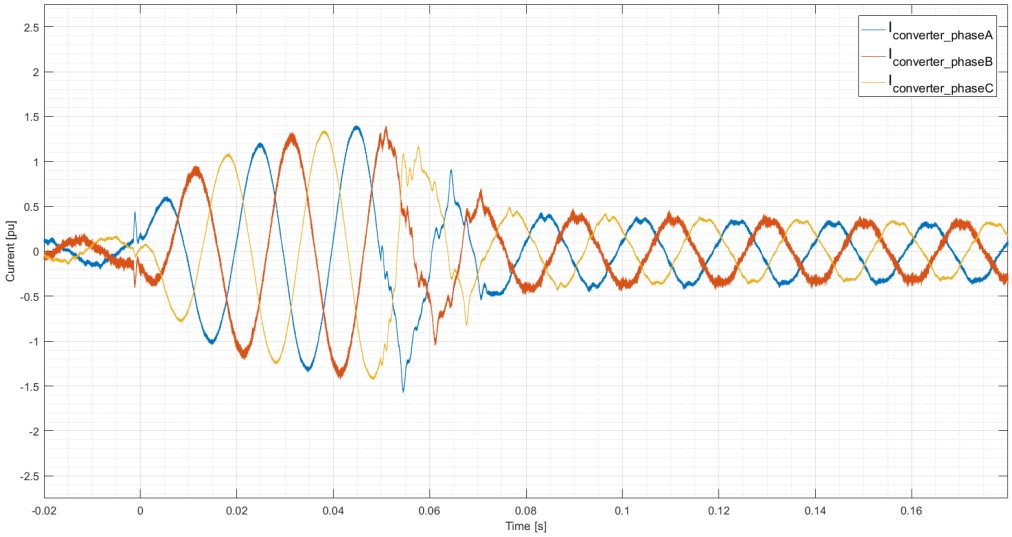
Still, these results can be used to illustrate that the second period of the short circuit will be constant when T_{sync} changes. To exemplify, I_{sc_max} is equal to 1.51 pu, 1.51 pu and 1.48 pu, when T_{sync} is equal to 6.6 ms, 13.3 ms and 20.0 ms, respectively. This means that the ratio, $R_{\frac{sc\_max}{normal}}$, also is approximately like for each value of T_{sync}. The small difference in the values, can be assigned to the uncertainty regarding the pinpointing of these values.

Short Circuit Duration

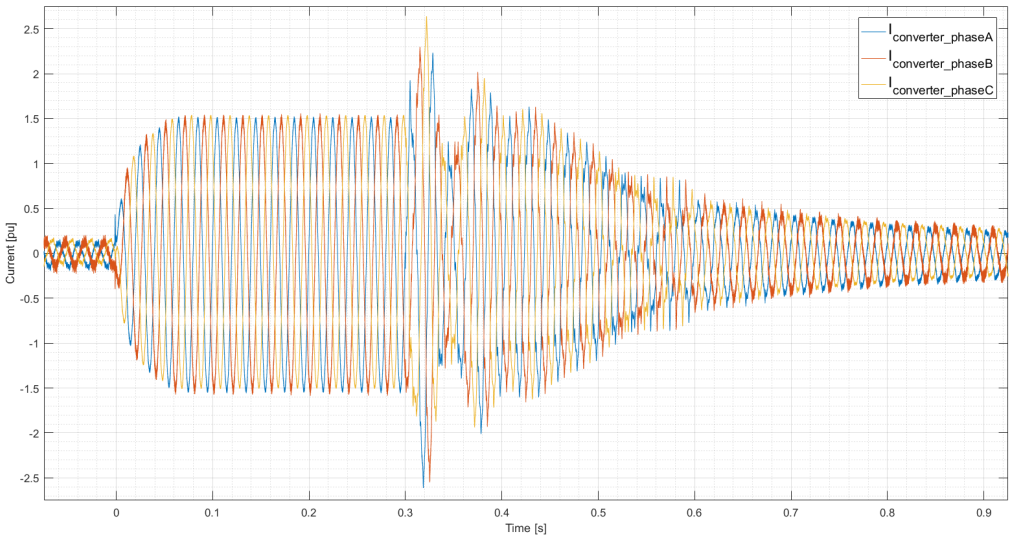
The impact of T_{short}, when control scheme 1 and control scheme 2 are implemented, is quite different. With control scheme 1, only small variations occurred when T_{short} was varied. Therefore, illustrations of $I_{converter}$ with varying T_{short} and with this control scheme, are omitted from this section. However, Figure C.3.3 in Appendix C.3 illustrates $I_{converter}$ for a 500 ms three-phase short circuit with control scheme 1.

The rest of this section focuses on the test results, with control scheme 2. Figure 6.3.3

illustrates $I_{converter}$ for three-phase short circuits, with different values of T_{short}. It should be noted, that the x-axis is different in the two graphs.



(a) $T_{short} = 50$ ms.



(b) $T_{short} = 300$ ms.

Figure 6.3.3: $I_{converter}$ for three-phase short circuits with different values of T_{short}, with control scheme 2.

The behaviour during the first period of the short circuit is similar for both values of T_{short}. Therefore, this period will not be elaborated any further.

During the second period of the short circuit, $I_{converter}$ is effected by T_{short}. When T_{short} is 300 ms, the control scheme uses approximately 69 ms to reach constant oscillations. This is

the duration the control scheme needs, to correlate with the new state of the system. The test results in Figure 6.1.2, had the same time duration. When T_{short} is 300 ms, I_{sc_max} is equal to 1.49 pu. After this, the magnitude of the converter current is constant throughout the second period of the short circuit.

When T_{short} is equal to 50 ms, the duration is too short for the current magnitude to reach oscillations with constant magnitude. Therefore, I_{sc_max} is equal to 1.40 pu. The smaller magnitude impacts $R_{\frac{SC\_max}{normal}}$, which decreases from 10.6 to 10.0, when T_{short} decreases from 300 ms to 50 ms.

T_{short} has the largest impact on $I_{converter}$ during the third period. When T_{short} is 300 ms, the converter control uses longer time to regulate the converter back to normal operation. After the short circuit is cleared, there are both negative and positive peaks in $I_{converter}$. The maximum positive peak occurs in phase C and is equal to 2.64 pu, while the largest negative peak occurs in phase A and is -2.61 pu.

After these peaks, $I_{converter}$ decreases for a short time, before it again increases. After the second interval with peaks, $I_{converter}$ slowly decreases to normal operation. The second interval with peaks, did not happen when T_{short} was equal to 100 ms.

This indicates, that when T_{short} increases, the control scheme struggles even more to regain normal operation.

Short Circuit Impedance

The impact of varying the short circuit impedance, was only tested with control scheme 1. Figure 6.3.4 illustrates $I_{converter}$ for a 100 ms three-phase short circuit, with Z_{sc} equal to 1 mH.

In the first period of the short circuit, an increase in the current magnitude was experienced as compared to when Z_{sc} was 2 mH. In this test, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ were 0.66 pu and -0.66 pu, respectively.

The increase in these values, illustrate the impact of Z_{sc}. The impact can also be illustrated with $R_{\frac{SC}{normal}}$ for phase B, which increased from 2.8 to 3.3, when Z_{sc} decreased.

$I_{converter}$ stays unaffected by the change of Z_{sc} in the second period. However, the third period is affected. Still, the change of Z_{sc} only leads to small magnitude variations. Therefore, these two periods will not be elaborated any further in this thesis.

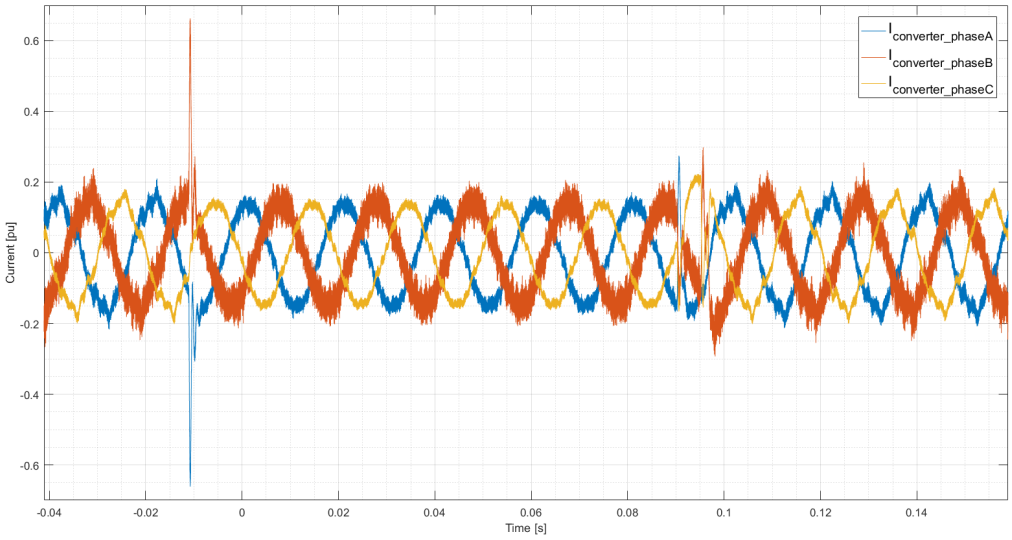


Figure 6.3.4: $I_{converter}$ for a 100 ms three-phase short circuit with Z_{sc} equal to 1 mH, with control scheme 1.

Type of Short Circuit

Test results from three-phase short circuits have been described in the previous sections. To investigate the impact the type of short circuit has on $I_{converter}$, test results from phase-to-phase short circuits, are included in this section. Phase-to-phase short circuits were only tested, with control scheme 1.

Figure 6.3.5 illustrates $I_{converter}$ for a 100 ms phase A to phase B short circuit, when I_{active_ref} was equal to 0.40 pu and T_{sync} equal to 20.0 ms. In the first period of the short circuit, $I_{converter}$ behaved similar as when a three-phase short circuit occurred.

The impact of increasing I_{active_ref} is also similar to when a three-phase short circuit occurs. When I_{active_ref} increased from 0.10 pu to 0.40 pu, $I_{initial\_peak\_positive}$ increased from 0.24 pu to 0.82 pu. This is the same effect as observed for a three-phase short circuit.

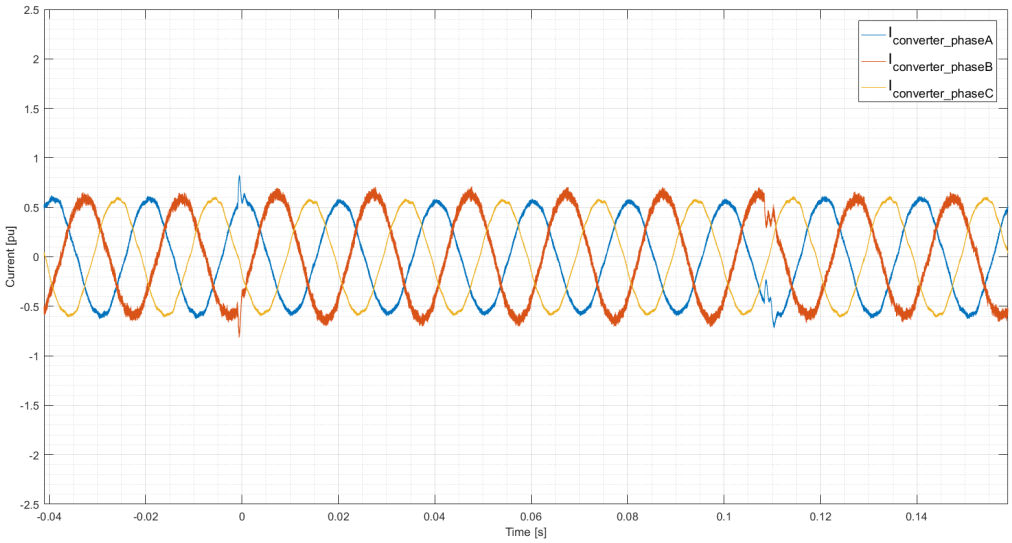


Figure 6.3.5: $I_{converter}$ for a 100 ms phase A to phase B short circuit, for I_{active_ref} equal to 0.40 pu, and T_{sync} equal to 20.0 ms, with control scheme 1.

Changing T_{sync} has similar impact on a three-phase and a phase-to-phase short circuit. The main difference in the first period, is the phases the peaks occur in. Therefore, the test results from varying T_{sync} will not be included here. For illustrations of these results the reader is referred to Figure C.3.4 in Appendix C.3.

However, some observations are of interest and will be included. For the three-phase short circuit with T_{sync} equal to 13.3 ms, the initial positive and negative peak occurred in phase C and phase A, respectively. On the other hand, when a phase A to phase B short circuit occurred, the positive and the negative initial peak occurred in phase B and phase A, respectively.

In the second period of the short circuit, a three-phase short circuit and a phase-to-phase short circuit causes similar $I_{converter}$. However, the magnitude of the current oscillations in the two short circuit types, are not the same. For example, with a phase A to phase B short circuit the magnitude of the three phases in $I_{converter}$ are not equal. Still, this magnitude difference is small.

$I_{converter}$ shows different behaviour during the third period of a three-phase and a phase A to phase B short circuit. The main difference is that there are fewer peaks and phase C is unaffected by the fault extinguishing. The impact of varying I_{active_ref} and T_{sync} is the same as during three-phase short circuit.

Laboratory tests were also performed for phase A to phase C short circuits. The current behaviour during these tests are the same during a phase A to phase B short circuit. The only thing that differs, is the involved phases. Therefore, the results from phase A to phase C short circuits will not be included here. For detailed description of these results, the reader is referred to Figure C.3.5 in Appendix C.3.

6.4 Impact of Implemented Control Scheme

This section investigates the impact of the implemented control scheme. In the laboratory tests, two different control schemes were tested. The difference between these two control schemes is the Reactive Control Mode reference. This was described in Section 5.3. To make comparison easier, the periods are described one at the time.

The First Period

The converter current behaves similarly during the first period of the short circuit, with both control schemes. In the first period, a positive and a negative peak occur in $I_{converter}$. The magnitude of these peaks changes when T_{sync}, I_{active_ref} and type of short circuit, are varied. These factors have already been explained in Section 6.2 and Section 6.3.

The importance of these peaks with respect to relay protection, can be questioned.
Compared to the time delay commonly used in over-current protection, the time duration of these peaks is short. This indicates, that even if the magnitude of a peak was to match the pick-up setting of the over-current relay, the time delay would prevent tripping of the relay. In the laboratory tests the largest value of an initial peak was, -2.03 pu. This is too low to trip an over-current relay.

The Second Period

In the second period of the short circuit, the behaviour of $I_{converter}$ differs for the two control schemes. This can be seen by comparing Figure 6.1.1 and Figure 6.1.2. Control scheme 1 regulates the current back to normal operation, while control scheme 2 increases the injected current. $I_{converter}$ increases until the control has adapted to the new system state.

To illustrate the magnitude difference, one can perform a few simplified calculations. These calculations are performed with values from the results illustrated in Figure 6.1.1 and Figure 6.1.2. With control scheme 1, the magnitude of the last positive peak in phase A of $I_{converter}$ was 0.17 pu. When control scheme 2 was implemented, the magnitude of the last positive peak in phase A was 1.48 pu. Therefore, the magnitude was almost nine times larger when control scheme 2, was implemented.

The effect of varying external and internal parameters is different for the two control schemes. This is illustrated with the results from Section 6.2. When control scheme 1 was implemented, the magnitude of $I_{converter}$ increased when I_{active_ref} increased. In the second period, the $I_{converter}$ peak value, increased from 0.17 pu to 0.60 pu, when I_{active_ref} increased from 0.10 pu to 0.40 pu. On the other hand, when control scheme 2 was implemented, I_{sc_max} only experienced an increase of 0.08 pu. This indicates that the impact of I_{active_ref} is negligible with control scheme 2, but not with control scheme 1.

The effect of varying external parameters had negligible impact on the second period, with control scheme 1. The value of I_{sc_max} is approximately the same for all the laboratory tests, with control scheme 2. This indicates that the magnitude of $I_{converter}$ is independent of the tested parameters. This is as expected since the control scheme is regulated to support the voltage, and therefore it is more dependent on external factors. One of which being, the type of short circuit. It should be mentioned that control scheme 2, was not tested with different values of Z_{sc} or different short circuit types.

The Third Period

In the third period of the short circuit, $I_{converter}$ is somewhat different. The most important difference, is that control scheme 2 struggles more to regain normal operation. This leads to large current peaks at the end of the short circuit. The effect of T_{short} was negligible with control scheme 1. With control scheme 2, T_{short} turned out to have a large impact. When T_{short} was increased to 300 ms, the control scheme struggled to regain normal operation. Because of this, large peaks occurred in the current with magnitudes up to 2.64 pu.

The Main Finding

The main finding of the laboratory tests is summarized in the following.

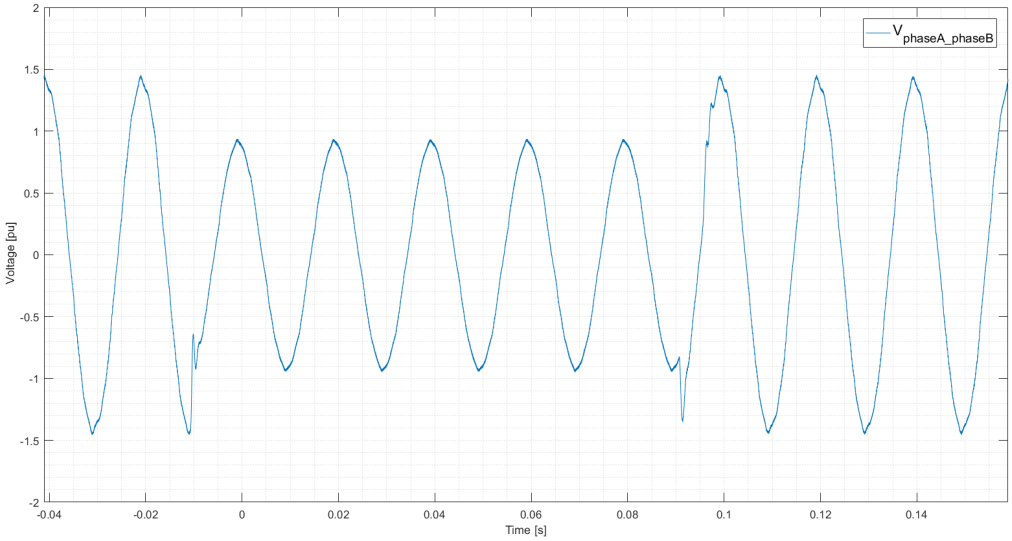
(i) The current contribution from converter A is largest with control scheme 2 implemented.

More precisely, the current contribution in the second and third period is larger than with control scheme 1. One reason, is that control scheme 2 provides voltage support. This voltage support, makes the voltage larger compared to when control scheme 1 is implemented. This principle is elaborated in the following.

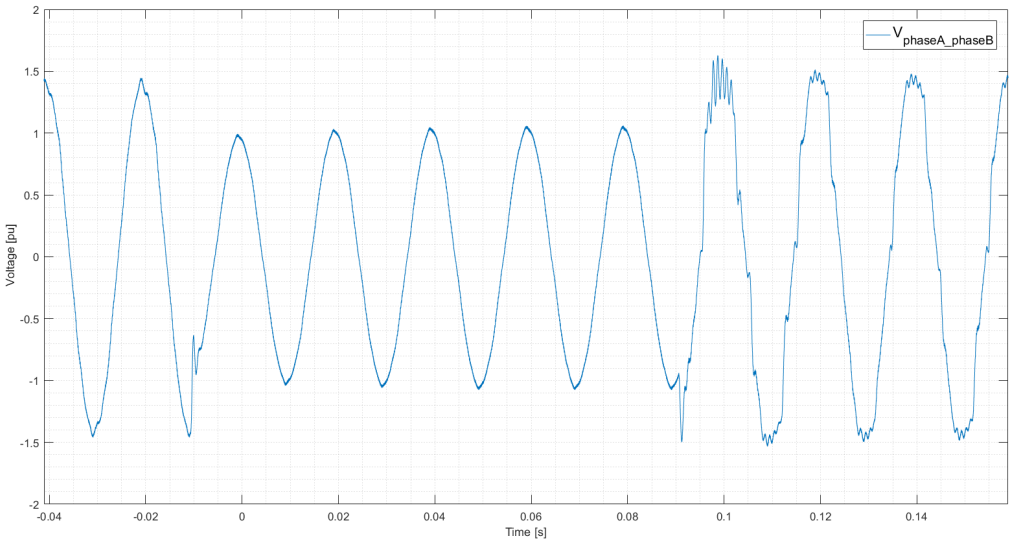
As described in Section 5.3.2, control scheme 2 is configured to increase the AC voltage during short circuits. Figure 6.4.1 illustrates the phase A to phase B voltage measured at the DQC bus-bar, V_{phaseA_phaseB}, during three-phase short circuits with the original settings described in Table 5.3.2 and Table 5.3.4. The parameter settings in both graphs are equal, except from the Reactive Control Mode reference.

The voltage magnitude during short circuit is larger with control scheme 2. During a 100 ms three-phase short circuit, the voltage oscillates five times. The magnitude of the positive peak voltage increases from 0.99 pu in the first cycle, up to 1.06 pu in the fifth cycle, with this control scheme. The converter control increases the injected reactive power, which leads to an increase in the AC voltage.

During a 100 ms three-phase short circuit with control scheme 1, the voltage magnitude throughout the short circuit, is equal to 0.94 pu. The magnitude difference between the two control schemes, increases from 0.05 pu to 0.12 pu during the short circuit.



(a) Control scheme 1.



(b) Control scheme 2.

Figure 6.4.1: V_{phaseA_phaseB} for a 100 ms three-phase short circuit with I_{active_ref} equal to 0.10 pu, T_{sync} equal to 9.8 ms and Z_{sc} equal to 2 mH, with both control schemes.

6.5 Current Contribution from the Converter versus the Main Supply

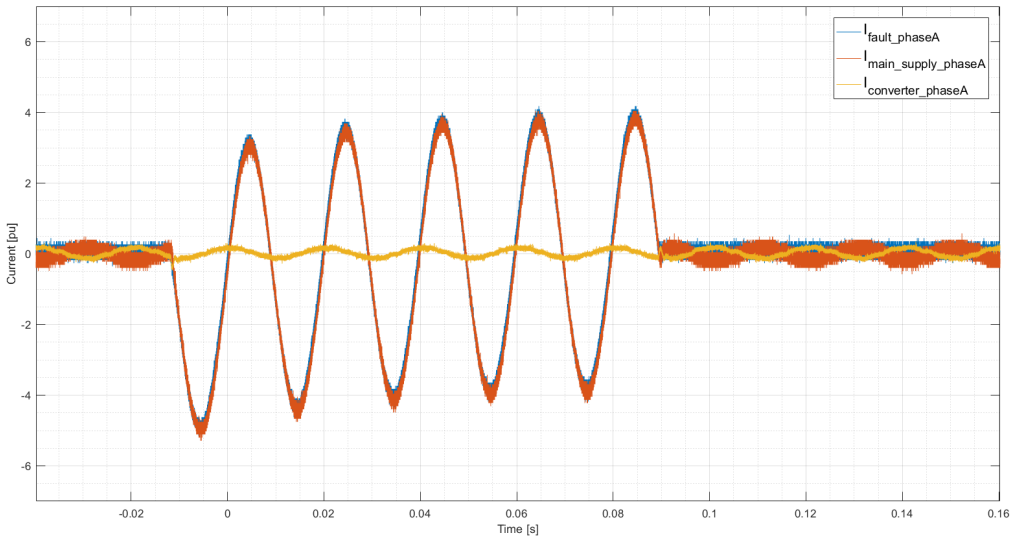
The results in this section, illustrates how varying the parameters, changes the ratio between the main supply and the converter short circuit currents. This ratio will be described separately for the two control schemes. As will become evident, this ratio becomes smaller with control scheme 2.

Control Scheme 1

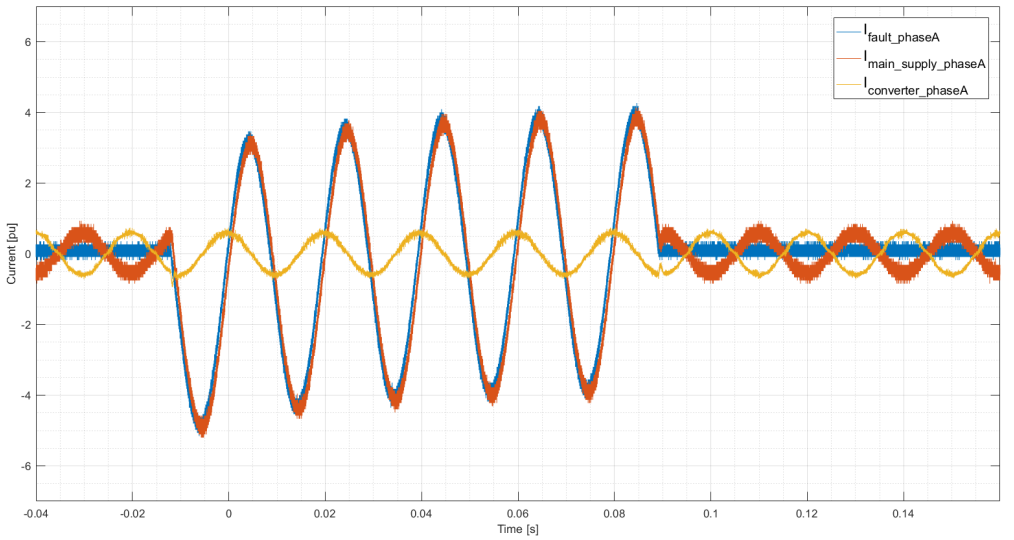
Figure 6.5.1 illustrates I_{fault_phaseA}, $I_{main\_supply\_phaseA}$ and $I_{converter\_phaseA}$ for a 100 ms three-phase short circuit, for two different values of I_{active_ref}. This figure illustrates how small the short circuit current contribution from the converter is compared to the contribution from main supply.

In the tests in Figure 6.5.1 (a), the first peak in $I_{main\_supply\_phaseA}$ is negative, and has a value equal to -5.30 pu. The peak-to-peak current is approximately constant, but the negative and positive peak-value changes. This is because of the DC-offset, and at the end

of the short circuit, $I_{main\_supply\_phaseA}$ is starting to stabilize and oscillate around zero. The short circuit duration is not long enough for the DC-offset to disappear.



(a) $I_{active\_ref} = 0.10$ pu.



(b) $I_{active\_ref} = 0.40$ pu.

Figure 6.5.1: I_{fault_phaseA}, $I_{main\_supply\_phaseA}$ and $I_{converter\_phaseA}$ for a 100 ms three-phase short circuit with varying I_{active_ref}, with control scheme 1.

To get an impression of the difference in magnitude between I_{main_supply} and $I_{converter}$, some simple calculations with the result from Figure 6.5.1 (a) will be performed. The last normal negative peak in I_{main_supply} was approximately -3.87 pu, while in $I_{converter}$ the last negative peak during second period was approximately -0.17 pu. In this situation, I_{main_supply} is

almost 23 times larger than $I_{converter}$. These calculations, give a rough idea of the magnitude difference between I_{main_supply} and $I_{converter}$, during a short circuit.

Changing parameters can change the ratio between the injected short circuit current from the main supply and the converter. One way to do so, is by increasing I_{active_ref}. An important aspect of I_{active_ref}, is that a change in this value, do not affect the magnitude of I_{fault}. This indicates that an increase in I_{active_ref} equals a decrease in I_{main_supply}. Which again, indicates that the ratio between the current injected by the main supply and the converter current during short circuits, decreases. To exemplify, with I_{active_ref} equal to 0.40 pu, the magnitude of the last negative peak in $I_{converter}$ during second period is approximately -0.65 pu. In this situation, I_{main_supply} is approximately six times larger than $I_{converter}$. This is an decrease with respect to the test where I_{active_ref} was 0.10 pu.

Figure 6.5.1 (b) illustrates I_{fault_phaseA}, $I_{main\_supply\_phaseA}$ and $I_{converter\_phaseA}$ when I_{active_ref} is 0.40 pu. Because of the phase shift introduced by the short circuit, the peaks do not occur at the same time instance. This is illustrated in Figure in 6.5.1 (b). Still, these calculations are considered to give an impression of the magnitudes in questioning.

On the other hand, varying Z_{sc} impacts I_{fault}. When Z_{sc} is decreasing, I_{fault} is increasing. By decreasing Z_{sc} from 2 mH to 1 mH, the first negative peak in $I_{main\_supply\_phaseA}$ increased from -5.30 pu to -7.69 pu. This is an increase of 2.39 pu. At the same time, the magnitude of $I_{converter}$ is only effected during the beginning and the end of the short circuit, this was explained in Section 6.3. This implies that the converter did not contribute with more current when Z_{sc} was decreased. Which further implies that the ratio between I_{main_supply} and $I_{converter}$ will increase.

Control Scheme 2

As mentioned in the beginning of this section, the ratio between the main supply and the converter becomes smaller with control scheme 2. Figure 6.5.2 illustrates the behaviour of the current injected by the main supply, during the same short circuit as in Figure 6.1.2.

The magnitude of $I_{converter}$ increases in these tests. Therefore, the current injected by main supply will be smaller compared to when control scheme 1 is implemented. To get an impression of the ratio between I_{main_supply} and $I_{converter}$ some simple calculations will be performed. The measurements of $I_{converter}$ and I_{main_supply} are done in Figure 6.1.2 and

Figure 6.5.2, respectively.

The values are measured in phase B for the last negative peak in each current. Close to the end of the short circuit, the magnitude of $I_{converter}$ is at its largest, while the magnitude of I_{main_supply} is at its smallest. Therefore, this will give the smallest magnitude difference, and is reason the measurements are done here.

The negative peak in I_{main_supply} during the second period is approximately -2.89 pu, while in $I_{converter}$ the last negative peak is approximately -1.53 pu. In this situation, I_{main_supply} is almost two times larger than $I_{converter}$. These calculations give a rough idea of the difference in magnitude between I_{main_supply} and $I_{converter}$, during a short circuit. This is much smaller than the ratio calculated with control scheme 1.

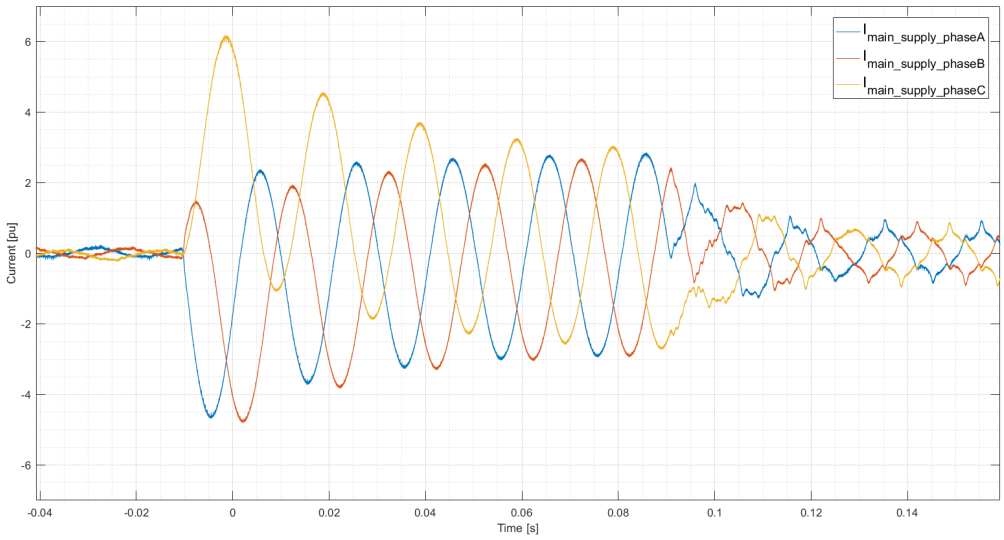


Figure 6.5.2: I_{main_supply} for a 100 ms three-phase short circuit with I_{active_ref} equal to 0.10 pu, T_{sync} equal to 9.8 ms and Z_{sc} equal to 2 mH, with control scheme 2.

Comparison of the Two Control Schemes

In the following the difference between the two control schemes, and the ratio between injected converter and main supply short circuit current, is illustrated. This will be done through a comparison of the simple calculations performed previously in this section. The only thing that differentiated these calculations, are the implemented control schemes.

With control scheme 1 and control scheme 2, the last negative peak was -0.17 pu and -1.53 pu, respectively. This indicates that the current magnitude is nine times larger with control

system 2. This will impact the injected current from the main supply. The ratio between I_{main_supply} and $I_{converter}$ decreased from 23 to 2, when the control changed from control scheme 1 to control scheme 2. These ratios are only calculated to give a rough idea of the magnitude differences, and these values cannot be considered to be exact values.

6.6 Summary of the Results

Section 6.6.1 presents the main finding from the laboratory tests. Section 6.6.2 and Section 6.6.3 presents summaries of the results with control scheme 1 and control scheme 2, respectively. Finally, in Section 6.6.4 the credibility of the results is briefly discussed.

6.6.1 The Main Finding

The main finding from the Smart Grid Laboratory tests, is:

(i) The current contribution from converter A is larger with control scheme 2 than with control scheme 1.

With control scheme 1 implemented, the converter short circuit current contribution, was negligible. Therefore, the following will focus on the impact of control scheme 2.

The current injected with control scheme 2 is the largest, because it is configured to supply AC voltage support to the grid. In comparison, control scheme 1 is configured to directly control the converter current. With this configuration, the control regulates the converter current to resemble normal operation. Most converter connected DG-units in the grid, are controlled with direct current control. Still, as the penetration level of DG increases, voltage support might be a requirement.

With respect to over-current relay protection, the magnitude of the current during short circuit is of special interest. The pick-up settings in these devices are configured based on a large short circuit contribution from the main supply. This makes the ratio between the injected short circuit current from the main supply and the converter interesting.

This ratio was smallest with control scheme 2 implemented. This can be illustrated with the simplified calculations conducted in Section 6.5. The magnitude of I_{main_supply} at the

end of the short circuit, was only two times larger than $I_{converter}$.

However, in this situation the magnitude of I_{sc_max} was 1.53 pu. This value indicates that the injected short circuit current from the converter, is small. Further, the test results show that varying the parameters has small impact on the converter current. When I_{active_ref} increased to 0.40 pu, I_{sc_max} increased to 1.61 pu. For the same change in I_{active_ref}, $R_{\frac{SC\_max}{normal}}$ decreased from 10.4 pu to 2.8 pu. This indicates, that even if I_{active_ref} was increased further the impact on I_{sc_max} would be small. Based on these two aspects, the impact of $I_{converter}$ is not significant in these laboratory results.

A conclusion regarding the impact of control scheme 2 cannot be drawn. More research is needed, in order to investigate how other external factors affect this control scheme. One suggestion being conducting laboratory tests with larger voltage dips. This could potentially affect the injected short circuit current-level from the converter. One way of increasing the voltage drop, is by decreasing the short circuit impedance. An interesting aspect would be to tests at which level the internal protection would disconnect the unit.

6.6.2 Summary of Control Scheme 1

In the following some other correlations that prevailed during the testing with control scheme 1, are summarized. These aspects have been discussed throughout this chapter, and will therefore not be elaborated further here.

Table 6.6.1 summarizes $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{SC}{normal}}$ for the results presented in this chapter. As mentioned in the beginning of this chapter, several tests beyond the ones presented here were performed. In Table C.2.1 and Table C.2.2 in Appendix C.2, the results from all the laboratory tests with control scheme 1 are summarized.

The correlations can be summarized as follows:

(i) Throughout the tests, the converter current behaviour was similar, and can be dived into three periods. In the first period, initial peaks occur in the converter current. In the second period, the converter current resembles normal operation. In the third period, more peaks occur in the converter current. Several factors affect the current magnitude.

(ii) The time duration of the current peaks in the first and the third period, are too short to trip an over-current relay.

(iii) In the second period, there is a larger ratio between the current injected by the main supply and the converter is large.

(iv) An increase in I_{active_ref} increases the converter current in the first and the second period. The impact on the converter current in the third period, is negligible. However, an increase in I_{active_ref} leads to a decrease of $R_{\frac{sc}{normal}}$. An increase in I_{active_ref} do not impact the total fault current.

(v) T_{sync} impacts the magnitude of the converter current in the first and the third period. The impact in the second period is negligible.

(vi) A decrease of Z_{sc}, increases the initial peaks in the first period. The impact on the second period is negligible, while the impact on the third period is small. A decrease of Z_{sc}, also leads to an increase in the total fault current.

(vii) The impact of changing the short circuit type, was small. The main difference, being that in some tests the involved phase or phases changed.

(viii) The impact of varying T_{short} was negligible.

Table 6.6.1: Summary of $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{SC}{normal}}$ from the test results illustrated in this chapter, with control scheme 1.

Variations	$\mathbf{I}_{initial\_peak\_positive}$[pu]	$\mathbf{R}_{\frac{SC}{normal}}$[-]	$\mathbf{I}_{initial\_peak\_negative}$[pu]	$\mathbf{R}_{\frac{SC}{normal}}$[-]
Original Settings	0.48 (phase B)	2.8	-0.45 (phase A)	2.6
Case 1.1: $\mathbf{I}_{active\_ref}$ [pu]				
0.40	0.82 (phase B)	1.4	-0.86 (phase A)	1.4
1.00	1.55 (phase B)	1.0	-2.03 (phase A)	1.3
Case 1.2: $\mathbf{T}_{sync}$ [ms]				
13.3	0.25 (phase C)	1.1	-0.44 (phase A)	2.0
18.3	0.31 (phase C)	1.4	-0.41 (phase B)	1.9
20.0	0.27 (phase A)	1.2	-0.44 (phase B)	2.0
Case 1.4: $\mathbf{Z}_{sc}$[mH]				
100	0.66 (phase B)	3.3	-0.66 (phase A)	3.7
Case 1.5: $\mathbf{I}_{active\_ref}$ [pu]				
0.10	0.24 (phase A)	1.1	-0.49 (phase B)	2.1
0.40	0.82 (phase A)	1.4	-0.82 (phase B)	1.4
Case 1.6: $\mathbf{T}_{sync}$ [ms]				
13.3	0.38 (phase B)	1.8	-0.28 (phase A)	1.3

6.6.3 Summary of Control Scheme 2

In the following some other correlations that prevailed during the testing with control scheme 2, are summarized. These aspects have been discussed throughout this chapter, and will therefore not be elaborated further here. Table 6.6.2 summarizes I_{sc_max} and $R_{\frac{SC\_max}{normal}}$ for the results presented in this chapter.

The correlations can be summarized as follows:

(i) Throughout the tests, the converter current behaviour was similar and can be dived into three periods. In the first period, initial peaks occur in the converter current. In the second period, the converter current increases until the control has adapted to the new system state. In the third period, several peaks occur in the converter current.

(ii) The control scheme struggles to regain normal operation after the short circuit is cleared.

(iii) The magnitude of the initial positive and negative peak are small, compared to the magnitude of $I_{converter}$ during the rest of the short circuit.

(iv) An increase in I_{active_ref}, increased the magnitude of the initial peaks. The effect during the second period is small. This can be illustrated with I_{sc_max}, which only increased by 0.08, when I_{active_ref} increased from 0.10 pu to 0.40 pu. The impact is small in the third period.

(v) The impact of varying T_{short} is small in the first and the second period. However, in the third period the impact is significant. The converter struggles more to regain normal operation when the short circuit duration increases.

(vi) The impact of varying T_{sync} is similar to when control scheme 1 was implemented.

Table 6.6.2: Summary of I_{sc_max} and $R_{\frac{SC\_max}{normal}}$ from the test results illustrated in this chapter, with control scheme 2.

Variations	$\mathbf{I}_{sc\_max}$[pu]	$\mathbf{R}_{\frac{SC\_max}{normal}}$[-]
Original Settings	1.53	10.4
Case 2.1: $\mathbf{I}_{active\_ref}$ [pu]		
0.40	1.61	2.8
Case 2.2: $\mathbf{T}_{sync}$ [ms]		
6.6	1.51	10.8
13.3	1.51	10.8
20.0	1.48	10.6
Case 2.3: $\mathbf{T}_{short}$[ms]		
50	1.40	10.0
300	1.49	10.6

6.6.4 Credibility of the Results

In this section the credibility of the results will be discussed. This discussion includes errors effecting the result, and factors that limit the extent to which the results can be used to corroborate the hypothesis.

As described in Section 5.1.3, a wide range of control settings for the converters, are available. Compared to the possibilities facilitated by the control system, the tests performed in this thesis are quite sparse. From the results in this chapter, it is evident that the implemented control scheme impacts the converter short circuit current behaviour. The combination of these two aspects, is a limiting factor.

Another limiting factor is that one specific converter type, was used in the tests. A wide range of different converter topologies exists, constructed to suit specific applications. The converter topology will affect the converter behaviour during short circuits. To what extent the converters behaviour differ, should be investigated by laboratory tests.

Other limiting factors, are the topology of the circuit and the number of DG-units implemented. In this laboratory setup, one converter connected DG-unit was imitated. The penetration of converter connected DG-units increases. Therefore, investigation of the aggregated short circuit contribution from several converters, is of interest. This was not possible with this laboratory setup.

These aspects limit the extent to which the results can be used to corroborate the hypothesis. Still, the test results presented in this chapter are valid, and they give an introduction in to the converter short circuit current behaviour. However, other aspects should be investigated, some suggestions for further work are summarized in Chapter 7.

There are sources of error present, which might affect the test results. One source of error is the noise in the current signals. Because of the noise, the exact magnitude of the current is difficult to pinpoint, which again effects the credibility of the results.

By changing the acquisition mode from Sample mode to Hi Res mode, the noise interference will decrease in the resulting curves in the oscilloscope. Hi Res mode measures the values between the measuring points, and calculates the average. There are both advantages and disadvantages related to this. One advantage, is that some of the noise in the signals will be removed. A disadvantage, is that transients also can be removed. Hi Res acquisition mode is used in the tests. One reason is that the record length is set to 1 million measuring points. The large number of measuring points will make the probability of removing transients smaller.

To see how the change of acquisition mode from Sample to Hi Res effects the measured converter current signal, the reader is referred to Figure C.3.6 in Appendix C.3. When the acquisition mode was equal to Sample and Hi Res, $I_{initial\_peak\_positive}$ was equal to 0.511 pu and 0.451 pu, respectively.

This illustrates that the acquisition mode can impact the magnitude of the current values. Therefore, two contradictory aspects need to be considered when evaluating the test results. The first aspect, is that the measured peak magnitude could be limited by the Hi Res mode. The second aspect, is that the measured peak magnitude could be heightened by the noise in the signal.

Chapter 7

Summary and Conclusion

The scope of this master's thesis is to investigate the short circuit current contribution from converters. The hypothesis was that the short circuit current contribution from a converter is negligible. In order to corroborate this hypothesis, this thesis investigates the research questions from Section 1.2. This has been done through a literature review presented in Chapter 3, Simulink simulations presented in Chapter 4 and tests in the Smart Grid Laboratory presented in Chapter 5 and Chapter 6. The investigation has led to the following main findings:

(i) The implemented control scheme impacts the converter short circuit current contribution.

(ii) The laboratory results show that a control scheme that operates as an AC voltage regulator, injects a larger current during short circuits than a control scheme directly controlling the current.

(iii) The specific control settings and external factors could impact the converter short circuit current contribution. The extent of the impact depends on the implemented control scheme and the factor in questioning.

(iv) The ratio between the current injected by the main supply and the converter, depends on the implemented control scheme.

In the following, these findings are elaborated.

No papers in the literature review described the implemented control scheme in detail. Therefore, it was impossible to draw conclusions on the impact of a specific control scheme.

Still, some observations and trends were observed. One general observation was that the type of control scheme implemented, do impact the converter short circuit behaviour. A trend in the papers, was that the control scheme was programmed to rapidly control the short circuit behaviour to resemble normal operation. The magnitude of the oscillations depended on the maximum output current limit.

This control scheme is similar to control scheme 1 used in the Smart Grid Laboratory tests. The short circuit converter current could be dived into three periods, when control scheme 1 was implemented. In the first period, initial peaks occurred for a short period. In the second period, the converter current resembled normal operation. In the third period, more peaks occurred for a short period.

Control scheme 1 is configured to directly control the converter current. Therefore, the injected current was regulated to resemble normal operation in the second and longest period. For this reason, the converter current contribution with control scheme 1 was small. The largest magnitude was measured in the first period, and was equal to -2.03 pu. The time duration of the initial peaks was short, because of the fast response of the current control scheme. Therefore, is the converter current contribution negligible.

The converter short circuit behaviour changed when control scheme 2 was implemented. Still, the converter current also can be dived into three periods with this control scheme. The first period, was similar to the first period with control scheme 1. In the second period, the converter current increased until the control had adapted to the new system state. In the third period, several peaks occurred. This control scheme was configured to supply AC voltage support to the grid. Therefore, the converter injected reactive power during the short circuit, which led to an increase in the voltage level.

The current contribution from converter A is largest when control scheme 2 was implemented. This can be illustrated with the ratio between the converter current with control scheme 1 and control scheme 2. In one of the tests, the ratio became nine during the second period of the short circuit. Most converter connected DG-units in the grid, are controlled with direct current control. Still, as the penetration level of DG increases, voltage support will be more important.

The literature review supports that external and internal factors impact the short circuit current. The review showed that the short circuit current can never exceed the hardware

over-current protection. Therefore, the low thermal overload capability of power electronics is a restraining factor with respect to the magnitude of the converter short circuit current. Within the range set by this restriction, the implemented converter control determines the short circuit behaviour. One paper illustrated how the controller implemented in the inner current loop affects the short circuit current behaviour. One of the controllers that were tested, was the PI controller in *dq*-frame. This is the same current controller that were used in the Simulink simulations and the laboratory tests. The behaviour of the converter short circuit current was similar in the Simulink simulations, the laboratory tests, and the paper, with this controller. This is as a sort of validation of the laboratory tests and Simulink simulations.

By comparing the two control schemes in the laboratory tests, it becomes evident that the implemented control scheme constrains the impact of external and internal factors. This will be illustrated by one internal control setting, I_{active_ref}, and one external factor, T_{short}. With control scheme 1, a change in I_{active_ref} from 0.10 pu to 0.40 pu in the second period of the short circuit, led to a magnitude increase of 0.43 pu. With control scheme 2, the increase was only 0.08 pu in the same period. This control setting did not have a significant impact on the converter short circuit current when control scheme 2 was implemented. The same cannot be said about control scheme 1. However, with control scheme 1, the converter magnitude is too low to impact an over-current relay.

The impact of a varying T_{short} was negligible when control scheme 1 was implemented. However, the impact differed when control scheme 2 was implemented. The most important difference, being that control scheme 2 struggles more to regain normal operation. When T_{short} was 300 ms, both negative and positive peaks occurred when the short circuit was cleared. The magnitude of the peaks varied from -2.61 pu and 2.64 pu. After these peaks, $I_{converter}$ decreased for a short time, before it again increased to peaks with magnitudes between -2.00 pu and 2.10 pu. After the second interval with peaks, $I_{converter}$ slowly decreased to normal operation. The second interval with peaks, did not happen when T_{short} was equal to 100 ms. This indicates, that when T_{short} increases, the control scheme struggles even more to regain normal operation. For this external factor, the impact on the short circuit current contribution was significant with control scheme 2 implemented, but not with control scheme 1.

The ratio between the short circuit current injected by the main supply and the converter

has also been investigated. In the Simulink simulations the ratio became large, while the ratio varied in the laboratory tests. The smallest calculated ratio occurred with control scheme 2 and it was equal to two. However, the peak converter current during the short circuit in this test, was 1.53 pu. This indicates, that even if the ratio was low, the actual contribution from the converter was not significant.

Conclusion

The literature review corroborates the hypothesis to some extent. The literature review in this thesis illustrates that the short circuit current contribution from a converter, is small. Some papers went as far as stating that the converter short circuit current contribution, is negligible.

The results from the Simulink simulations showed that the short circuit contribution from one converter is small. However, this result is only accurate for the specific control scheme implemented in the simulation model. It should be noted, that several simplifications and assumptions were made when this model was created, as described in Section 4.2.2.

Some of the laboratory test results corroborate the hypothesis. The short circuit current contribution with control scheme 1 was negligible. However, the short circuit current with control scheme 2 was the largest. Still, the results from these tests are not enough to make a general conclusion regarding the short circuit current contribution from a converter. To make such a conclusion, more research is needed.

7.1 Recommendations for future work

The complex converter control system used in the laboratory tests, opened for numerous possibilities. Compared to the possibilities facilitated by the control system, the tests performed in this thesis are quite sparse. The time constrain was a natural limiter of the number of tests. Therefore, recommendations for future work includes performing extensive testing with the VSC control system in the Smart Grid Laboratory.

This testing should include investigation of the impact of varying external factors when control scheme 2 is implemented. For example by increasing the voltage drop to see how this

would affect the injected current. The results showed that this control scheme struggled to regain normal operation as the time duration increased. Therefore, it would be interesting to increase the time duration even further. Another suggestion is to change the current controllers from PI regulators in the *dq*-frame to hysteresis regulators in the *dq*-frame, in the built-in control system. According to [71], these controllers have a faster response to transients. These are just three suggestions in a sea of opportunities.

Another suggestion for future work is to investigate the impact of an increased penetration level. The findings from the literature review, the Simulink simulations and the laboratory tests illustrated that the short circuit contribution from one converter is small. Therefore, testing the aggregated contribution of several converters would be interesting.

Chapter 8

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Appendix A

Additional Information on Simulations in Simulink

In this Appendix, some additional information regarding the simulations in Simulink, is presented.

A.1 Detailed Model Description

In this section, more details about the Simulink model, are included. In Figure A.1.1 the VSC grid interface, is illustrated. This grid interface, consist of a LCL-filter, an average-model VSC and a DC-link capacitor.

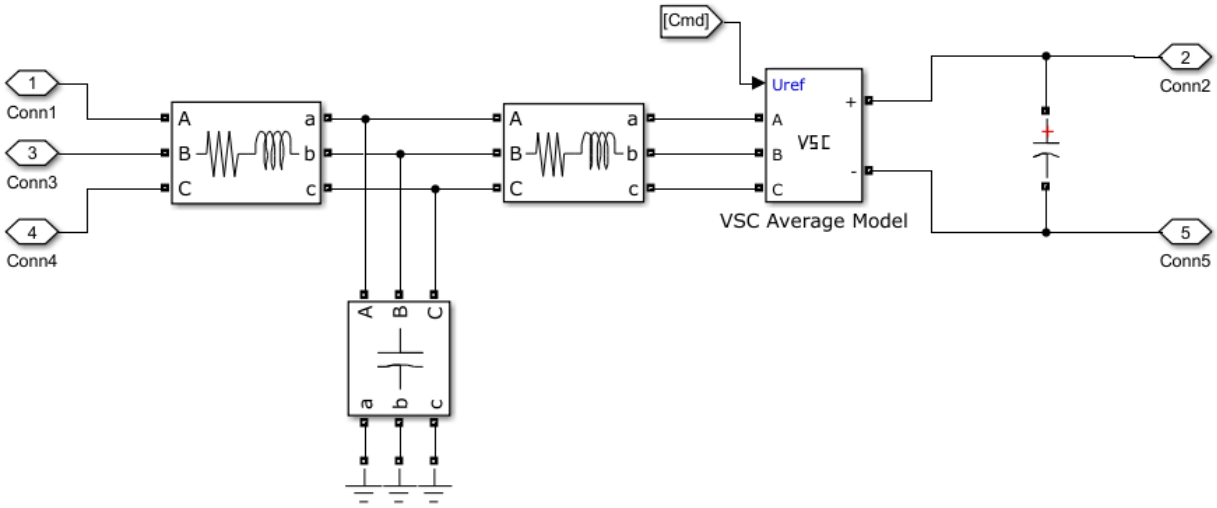


Figure A.1.1: The VSC grid interface used in the Simulink simulations.

In Figure A.1.2, the PLL used in the Simulink simulations, is illustrated. This is a simplified model of the PLL described in Section 5.1.3.

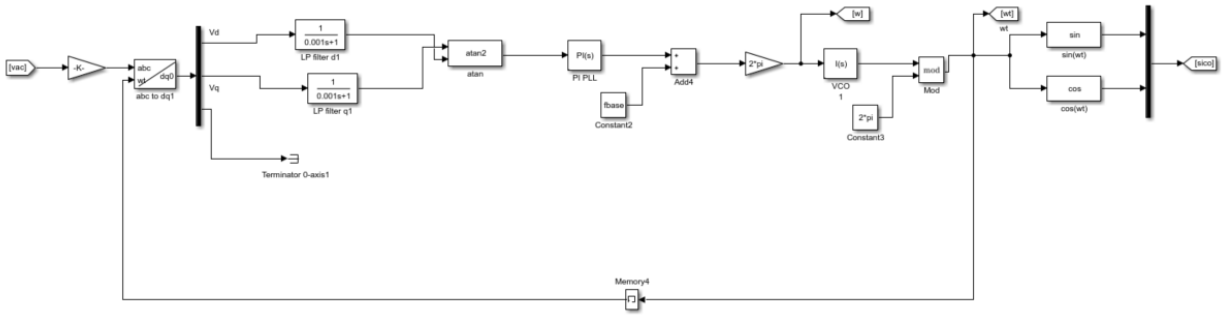


Figure A.1.2: The PLL used in the Simulink simulations.

In Figure A.1.3, the current control loop used in the Simulink simulations is illustrated. The current is controlled in the *dq*-frame. The basis for the current control is created by Santiago Sanchez Acevedo. To properly imitate the current control in VSC in the Smart Grid Laboratory, the parameter values have been changed.

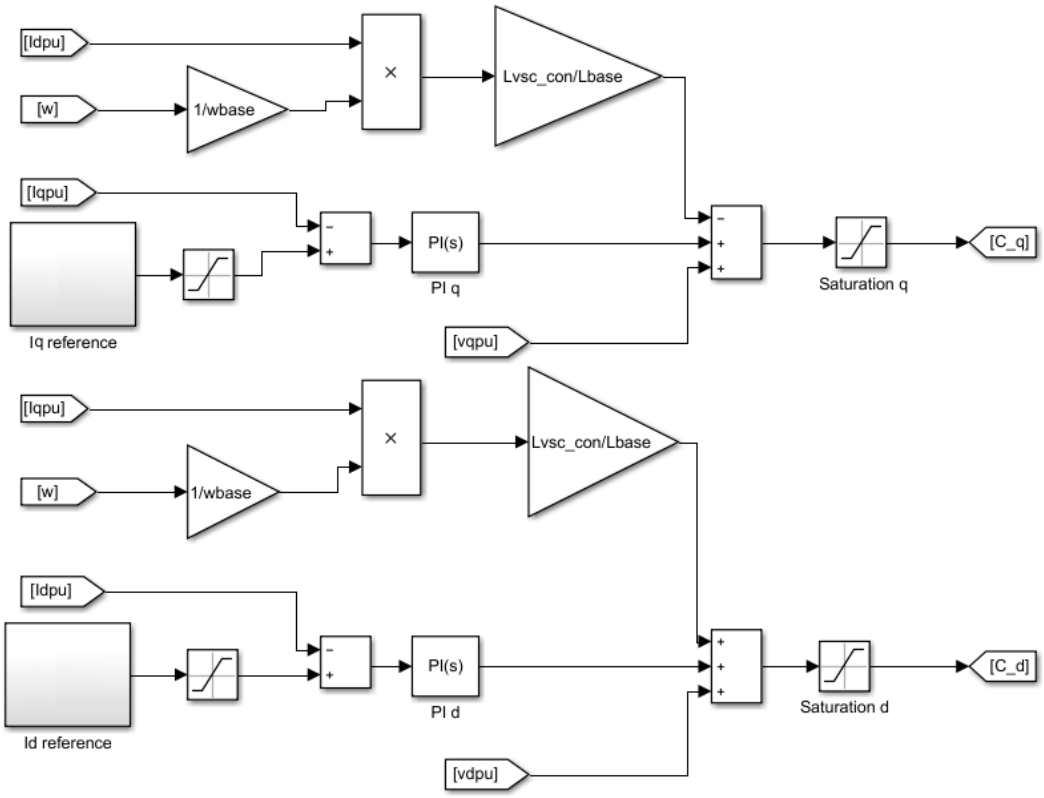


Figure A.1.3: The current control loop used in the Simulink simulations.

A.2 MATLAB Script

The MATLAB script calculates the base values from the Smart Grid Laboratory VSC values. These base values are then used as base values for the rest of the circuit. The script also transform discrete PI controller values to continuous parameters. This MATLAB script is also used to initialize these parameter values in the Simulink model.

```
%%%%Parameters for the MasterThesis_simulation_model.slx

%% Base Values
Sbase=5e4; %base aparent power
Vbase=326.5986;% %base voltage 1ph% peak value
Ibase=2*Sbase/(3*Vbase); %base current 1ph
Vdcbase= 653.1973; %2.2268*Vbase; %DC base voltage def.
Idcbase=Sbase/Vdcbase;%(3/2)*Ibase;  % IDC base current calculation
fbase=50; %base frequency
wbase=2*pi*fbase; %base rotational frequency
Zbase=Vbase/Ibase; %base impedance
Zdcbase=Vdcbase/Idcbase;
Xlbase=Zbase;
Lbase=Xlbase/wbase;
Cbase=1/(Xlbase*wbase);
Ldcbase=Zdcbase/wbase;
Cdcbase=1/(Zdcbase*wbase); %base dc capacitor
fsw=5e3; % switchin frequency
Ts=400e-6;

%% PI- Controllers
%kpvsc: PI current Proportional gain, PI type: kp+ki/s
%kivsc: PI current integral gain
%kppll:  PI PLL Proportional gain, PI type: kp+ki/s
%kipll: PI PLL integral gain
%% Current controller
kp_vsc=0.5;
ki_vsc=65;
Tsc=2/1e4;

Hcd=tf(kp_vsc,[0,1],Tsc)+ki_vsc*(Tsc/2)*tf([1,1],[1,-1],Tsc); %%discrete
    model
```

```
32
33 [num_c,den_c]=tfdata(d2c(Hcd),'v'); %From discrete to continues
34 kpvsc=num_c(1);
35 kivsc=num_c(2);
36
37 %% PLL
38 kp_pll=5.3052;
39 ki_pll=58.9463;
40 Tspll=2/1e4;
41 TIpf=0.01;
42
43 Hplld=tf(kp_pll,[0,1],Tspll)+ki_pll*(Tspll/2)*tf([1,1],[1,-1],Tspll); %
       discrete model
44
45 [num_pll,den_pll]=tfdata(d2c(Hplld),'v'); %From discrete to continues
46 kppll=num_pll(1);
47 kipll=num_pll(2);
48
49 %% Setting the LCL parameters and the capacitor link parameter
50
51 %Cvsc_dc :  capacitor link DC vsc                    [F]
52 %Cvsc:      capacitor AC vsc                         [F]
53 %Lvsc_con:  inductor AC vsc converter-side = L_f     [H]
54 %Lvsc_grid: inductor AC vsc grid-side  = L_f_g       [H]
55 %Rvsc:      resistor AC vsc = R_f =R_f_g             [ohm]
56
57 Cvsc_dc=0.004;
58 Lvsc_con= 0.0005093;
59 Lvsc_grid= 0.00020372;
60 Rvsc=0.032;
61 Cvsc=0.000049736;
```

Appendix B

Supplementary Information Laboratory Tests

B.1 Additional Information on Laboratory Setup

Figure B.1.1 illustrates the grid interface used in the tests. There are several configuration possibilities available, and these are indicated in Figure B.1.1 [70].

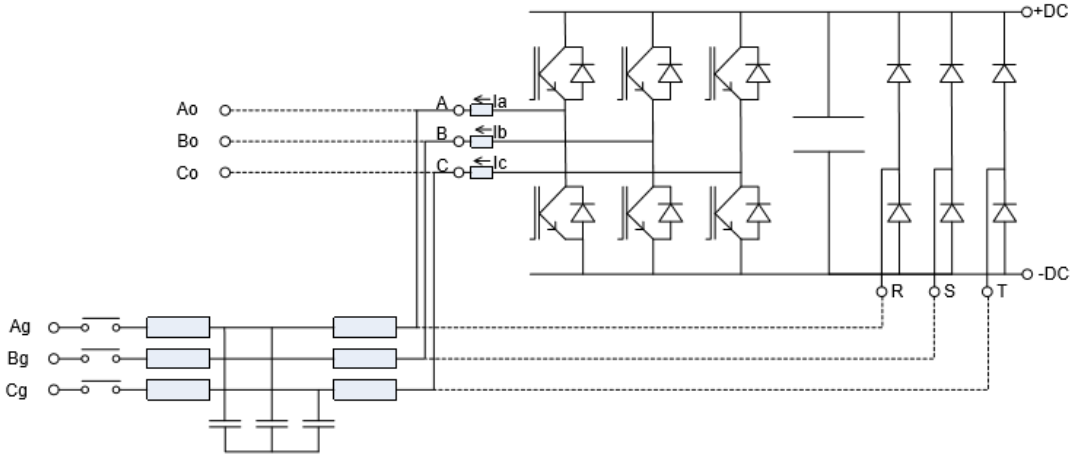


Figure B.1.1: Power circuit of the converter, with alternative configurations [70].

The following list entails the different parameter values and control signal lists available in the built-in control system of the VSC used in the tests.

1): Signal Parameters
2): Operation Mode Parameters
3): Current Measurement Parameters
4): Current Regulator Parameters
5): Hyst_reg Parameters
6): U DC link Regulator Parameters
7): U DC link Protection Parameters
8): AC Voltage Measurement Parameters
9): AC Voltage Regulator Parameters
10): AC Grid Voltage Protection
11): VCO Parameters
12): PLL Parameters
13): PLL Weighing Factor Parameters
14): PLL lock, Sync Detector Parameters
15): AC Frequency Regulator Parameters
16): AC Grid Frequency Protection
17): Active Damping Parameters
18): Temperature Parameters
19): Default Reference Signals
20): CAN Bus Parameters
21): DA Converter Parameters
22): Display Signal Config

Some additional converter control parameter value and control signal settings can be found in Table B.1.1. Only the parameter deemed necessary for understanding the tests in this thesis, are included.

Table B.1.1: Some additional converter control parameter value and control signal settings from the built-in control.

Parameters	**B03-0432**	**B03-0431**
Control Signal Source	Menu	Fixed
Ref Limit max value (1)	1000 [pu]	1000 [pu]
Limit_value_coupling	Separate	Separate
Ireact/Iact ratio	20 [%]	0 [%]
Autostart protection	No	Yes
I trip level	245 [A]	245 [A]
I rated current	90 [A]	90 [A]
I reg KP	400 [%pu/pu]	400 [%pu/pu]
I reg Ti	1000 [μs]	1000 [μs]
Angle delay comp	50 [μs]	50 [μs]
Switching frequency	7000 [Hz]	10000 [Hz]
U DC link rated voltage	not relevant	600 [V]
U DC reg Kp	not relevant	1000 [%]
U DC reg Ti	not relevant	30 [ms]
U DC trip	730 [V]	730 [V]
U DC low limit start	-10 [V]	-10 [V]
Rated AC voltage	400 [V]	400 [V]
U AC reg filter tc	10 [ms]	not relevant
U AC reg Kp	100 [%]	not relevant
U AC reg Ti	100 [ms]	not relevant
U AC high trip level	1400 [V]	1400 [V]
VOC operation mode	PLL	PLL
PLL reg Kp	1000 [%]	1000 [%]
PLL reg Ti	100 [ms]	100 [ms]

(1) 1000 pu = 100% [71].

B.2 Additional Information on Approach

As mentioned in Section 5.1.5, the current signals were measured with an oscilloscope. The responding wave-forms from each test, was then saved in a csv-file. This file was then accessed with MATLAB, and plots were created. In the following, a MATLAB script illustrating this process for one situation, is given.

```
Values = tdfread('tek0096ALL.csv', 'comma');

%% Parameter explanation
%The parameters depends on the measured current. This csv-file contains the
%measurement of the three phases of the converter current.

%Values.TIME --> time intervall                    [s]
%Values.CH1 --> phase A I_converter                [A]
%Values.CH2 --> phase B I_converter                [A]
%Values.CH3 --> phase C I_converter                [A]

Ibase_rms=90; % RMS CURRENT. Rated current in built-in control

%% Matrix containing the three-phase current
Three_current_signals=[Values.CH1 Values.CH2 Values.CH3];

%% Plot figure of the three-phase current

figure(1)
plot(Values.TIME, -Three_current_signals/Ibase_rms)
%axis TIGHT  %([XMIN XMAX YMIN YMAX])
axis([Values.TIME(1) Values.TIME(1000000) -0.5 0.5])
grid on;
grid minor;
xlabel('Time [s]')
ylabel('Current [pu]')
lgd = legend('I_{converter\_phaseA}','I_{converter\_phaseB}','I_{converter\
    _phaseC}');
lgd.FontSize = 14;
saveas(gcf, 'Tsync_166_I_converter_three_phase_3ph_tek0096', 'fig')
```

Appendix C

Supplementary Laboratory Results

In this Appendix, supplementary information and illustrations from some of the tests, can be found. These illustrations are included for an even deeper understanding of the results, but are not essential for the fundamental understanding of them.

C.1 Parameters Used for Comparison

To be able to compare the results more easily, set of parameters are used. The set of parameters differ when control scheme 1 and control scheme 2, are implemented. In this section the reasoning behind the chosen parameters and the calculations of these, are explained.

Control Scheme in Scenario 1

The set of parameters in scenario 1, consists of $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{\_sc\_}{normal}}$. Most of the protection devices in the distribution grid today are over-current relays, as mentioned in Section 2.2.2, and thus the maximum current during short circuits, is of interest. $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ is included, because these peaks have the largest magnitude. $R_{\frac{\_sc\_}{normal}}$ illustrates the correlation between the magnitude during normal operation and the magnitude of the initial peak during short circuits. How $R_{\frac{\_sc\_}{normal}}$ was calculated is explained in this section.

To be able to calculate $R_{\frac{\_sc\_}{normal}}$, the converter current during normal operation is needed.

In Table C.1.1 the peak converter current during normal operation, $I_{normal\_operation\_peak}$, is given. The table only includes the values from the test results presented in Chapter 6.

Table C.1.1: The normal operation peak current, $I_{normal\_operation\_peak}$, with control scheme 2.

Variations	$\mathbf{I}_{normal\_operation\_peak}$[pu]	
	Positive Cycle	**Negative Cycle**
Original Settings	0.17 (phase B)	-0.17 (phase B)
Case 1.1: $\mathbf{I}_{active\_ref}$ [pu]		
0.40	0.60 (phase B)	-0.60 (phase A)
1.00	1.54 (phase B)	-1.58 (phase A)
Case 1.2: $\mathbf{T}_{sync}$ [ms]		
13.3	0.22 (phase C)	-0.22 (phase A)
18.3	0.22 (phase C)	-0.22 (phase B)
20.0	0.22 (phase A)	-0.22 (phase B)
Case 1.4: $\mathbf{Z}_{sc}$[mH]		
100	0.20 (phase B)	-0.18 (phase A)
Case 1.5: $\mathbf{I}_{active\_ref}$ [pu]		
0.10	0.21 (phase A)	-0.23 (phase A)
0.40	0.58 (phase A)	-0.60 (phase B)
Case 1.6: $\mathbf{T}_{sync}$ [ms]		
13.3	0.21 (phase B)	-0.21 (phase A)

Two values of $I_{normal\_operation\_peak}$ are given for each test result. One value is measured during the positive half cycle, while the other is measured during the negative half cycle. The chosen phase for each test result, depends on which phase $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ occurred. Simply put, if $I_{initial\_peak\_positive}$ occurred in phase A, the positive cycle value is the normal peak value of phase A.

These values have been obtained with the Data Cursor in MATLAB. It has been difficult to pinpoint these values precisely. One reason being the noise in the current signals. These values should therefore only be used as an indication on what the magnitude of these values might be, not as fact-based truths.

The values in Table C.1.1 have together with $I_{initial\_peak\_negative}$ and $I_{initial\_peak\_positive}$ been used to calculate the increase in each test result. For the positive initial peak Formula C.1 has been used, while Formula C.2 has been used for the negative initial peak.

$$R_{\frac{\_SC\_}{normal}}[-] = \frac{I_{initial\_peak\_positive}[pu]}{I_{normal\_operation\_peak}(PositiveCycle)[pu]} \tag{C.1}$$

$$R_{\frac{\_SC\_}{normal}}[-] = \frac{I_{initial\_peak\_negative}[pu]}{I_{normal\_operation\_peak}(NegativeCycle)[pu]} \tag{C.2}$$

Control Scheme in Scenario 2

In the tests with control scheme 2, the set of parameters consists of I_{sc_max} and $R_{\frac{SC\_max}{normal}}$. With this control scheme, $I_{initial\_peak\_positive}$ and $I_{initial\_peak\_negative}$ no longer have the largest magnitudes. Therefore, is I_{sc_max} included in the parameter set instead. I_{sc_max} is the maximum peak current during the short circuit, and it occurs when the control system becomes steady. The positive and negative cycle resemble, and therefore I_{sc_max} is only calculated for the positive cycle. To be able to compare the results, ratio $R_{\frac{SC\_max}{normal}}$ is calculated for each situation. How these ratios are calculated, are explained in the following.

In Table C.1.2 the peak current during normal operation, $I_{normal\_operation\_peak}$, for case 2.1, case 2.2 and case 2.3, are given. These values were measured at the last peak before the fault occurred. These values are approximations and some uncertainty is associated with them. These values should therefore only be used as indication of the actual magnitude.

Table C.1.2: $I_{normal\_operation\_peak}$, with control scheme 2.

Variations	$\mathbf{I}_{normal\_operation\_peak}$[pu]
Original Settings	0.15
Case 2.1: $\mathbf{I}_{active\_ref}$ [pu]	
0.40	0.57
Case 2.2 $\mathbf{T}_{sync}$ [ms]	
6.6	0.14
13.3	0.14
20.0	0.14
Case 2.3: $\mathbf{T}_{short}$[ms]	
50	0.14
300	0.14

The behaviour during short circuits, both in the negative and positive cycle are the same. For this reason, $I_{normal\_operation\_peak}$ is only calculated for the positive cycle. The ratio, $R_{\frac{SC\_max}{normal}}$, for each situation is calculated with Formula C.3.

$$R_{\frac{SC\_max}{normal}}[-] = \frac{I_{sc\_max}[pu]}{I_{normal\_operation\_peak}[pu]} \tag{C.3}$$

C.2 Summary of the Test Results

Table C.2.1 and Table C.2.2 summarizes the set of parameters, $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{SC}{normal}}$, for the tests with control scheme 1. In these tables, the parameter value from all tests are included.

Table C.2.1: Summary of the set of parameters, $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{SC}{normal}}$, from case 1.1 to case 1.4.

Variations	$\mathbf{I}_{initial\_peak\_positive}$[pu]	$\mathbf{R}_{\frac{SC}{normal}}$[-]	$\mathbf{I}_{initial\_peak\_negative}$[pu]	$\mathbf{R}_{\frac{SC}{normal}}$[-]
Original Settings	0.48 (phase B)	2.8	-0.45 (phase A)	2.6
Case 1.1: $\mathbf{I}_{active\_ref}$ [pu]				
0.20	0.61 (phase B)	2.1	-0.59 (phase A)	1.9
0.30	0.72 (phase B)	1.7	-0.72 (phase A)	1.6
0.40	0.82 (phase B)	1.4	-0.86 (phase A)	1.4
1.00	1.55 (phase B)	1.0	-2.03 (phase A)	1.3
Case 1.2: $\mathbf{T}_{sync}$ [ms]				
6.6	0.30 (phase B)	1.4	-0.41 (phase C)	1.9
13.3	0.25 (phase C)	1.1	-0.44 (phase A)	2.0
16.6	0.42 (phase C)	2.0	-0.28 (phase B)	1.2
18.3	0.31 (phase C)	1.4	-0.41 (phase B)	1.9
20.0	0.27 (phase A)	1.2	-0.44 (phase B)	2.0
Case 1.3: $\mathbf{T}_{short}$[ms]				
200	0.49 (phase B)	3.0	-0.44 (phase A)	2.5
300	0.49 (phase B)	2.8	-0.43 (phase A)	2.4
500	0.51 (phase B)	3.0	-0.44 (phase A)	2.5
Case 1.4: $\mathbf{Z}_{sc}$[mH]				
100	0.66 (phase B)	3.3	-0.66 (phase A)	3.7

Table C.2.2: Summary of the results from case 1.5 to case 1.7.

Variations	$\mathbf{I}_{initial\_peak\_positive}$[A]	$\mathbf{R}_{\frac{\_sc\_}{normal}}$[-]	$\mathbf{I}_{initial\_peak\_negative}$[A]	$\mathbf{R}_{\frac{\_sc\_}{normal}}$[-]
Case 1.5:				
$\mathbf{I}_{active\_ref}$ [pu]				
0.10	0.24 (phase A)	1.1	-0.49 (phase B)	2.1
0.40	0.82 (phase A)	1.4	-0.82 (phase B)	1.4
Case 1.6:				
$\mathbf{T}_{sync}$ [ms]				
6.6	0.34 (phase B)	2.0	-0.14 (phase A)	0.8
8.3	0.45 (phase B)	2.7	-0.35 (phase A)	2.0
9.8	0.49 (phase B)	2.2	-0.43 (phase A)	1.1
9.9	0.50 (phase B)	2.9	-0.43 (phase A)	2.3
13.3	0.38 (phase B)	1.8	-0.28 (phase A)	1.3
Case 1.7:				
$\mathbf{I}_{active\_ref}$ [pu]				
0.10	0.40 (phase C)	2.4	-0.47 (phase A)	2.7
0.40	0.83 (phase C)	1.4	-0.81 (phase A)	1.3

C.3 Additional Test Results

In this section some additional test results are included. These results are considered to be supplements to the findings presented in Chapter 6.

Time of occurrence

Figure C.3.1 illustrates $I_{converter}$ for a 100 ms short circuit with T_{sync} equal to 13.3 ms, with control scheme 1. T_{sync} was also set to 6.6 ms, 16.6 ms, 18.3 ms and 20.0 ms. Except from the first and the third period of the short circuit, the $I_{converter}$ was similar for the different tests. The impact of T_{sync} on the first and second period, was illustrated in Section 6.3. Therefore, the graphs for the other values of T_{sync}, are not included. Still, $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{\_sc\_}{normal}}$ for these tests can be found in Table C.2.1.

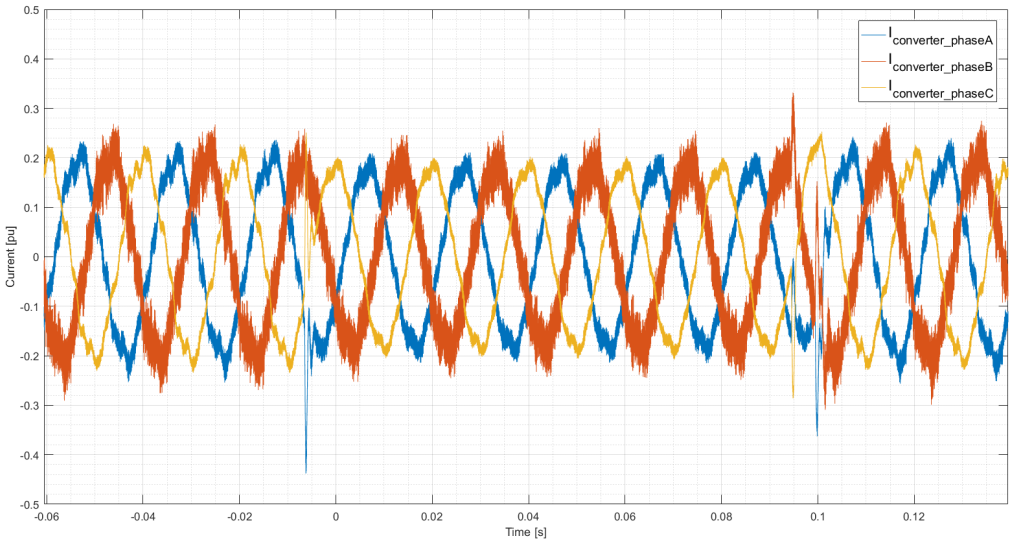
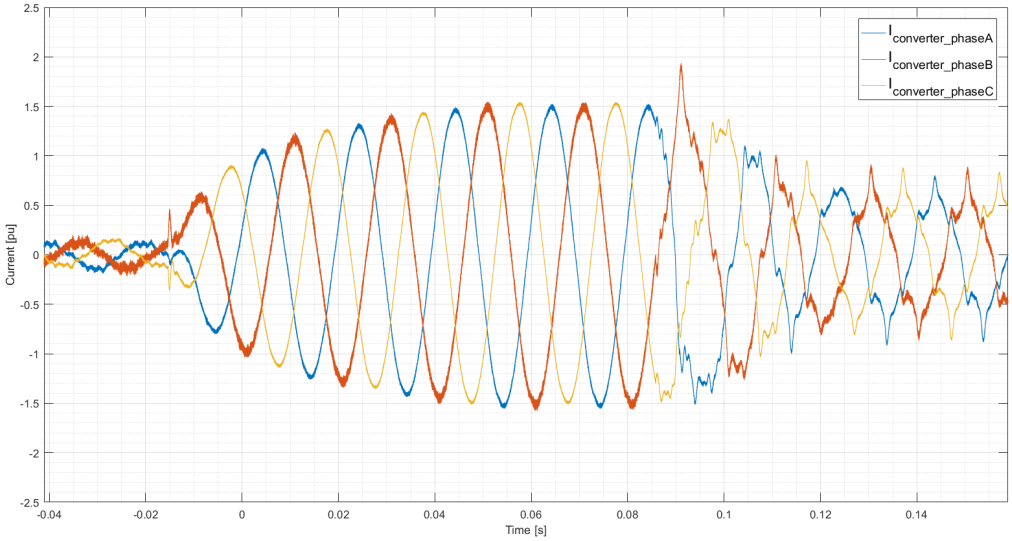


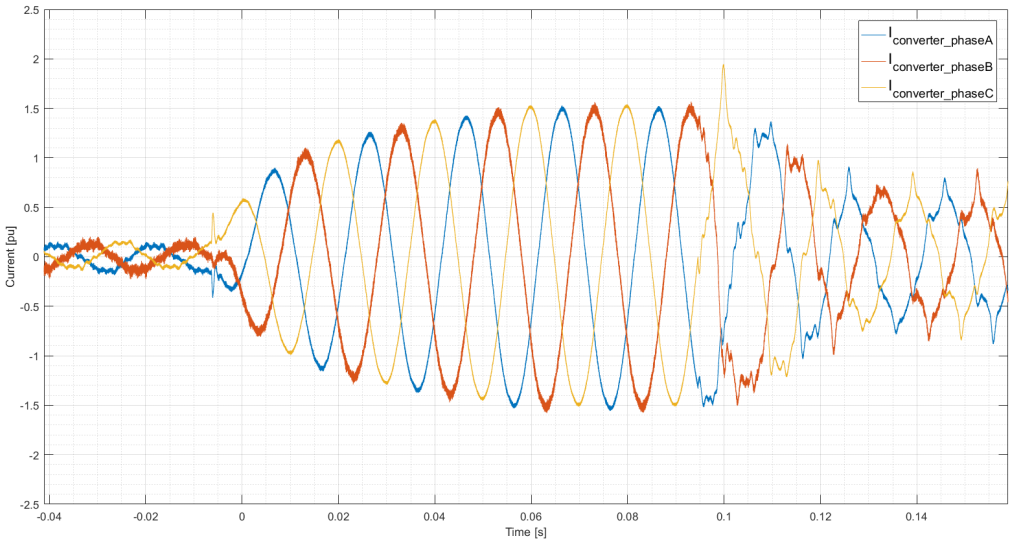
Figure C.3.1: $I_{converter}$ for a 100 ms three-phase short circuit for T_{sync} equal 13.3 ms, with control scheme 1.

The impact of changing T_{sync} is similar for both control schemes. Therefore, were only tests results from control scheme 1 presented in Section 6.3. However, test results from control scheme 2 are presented here.

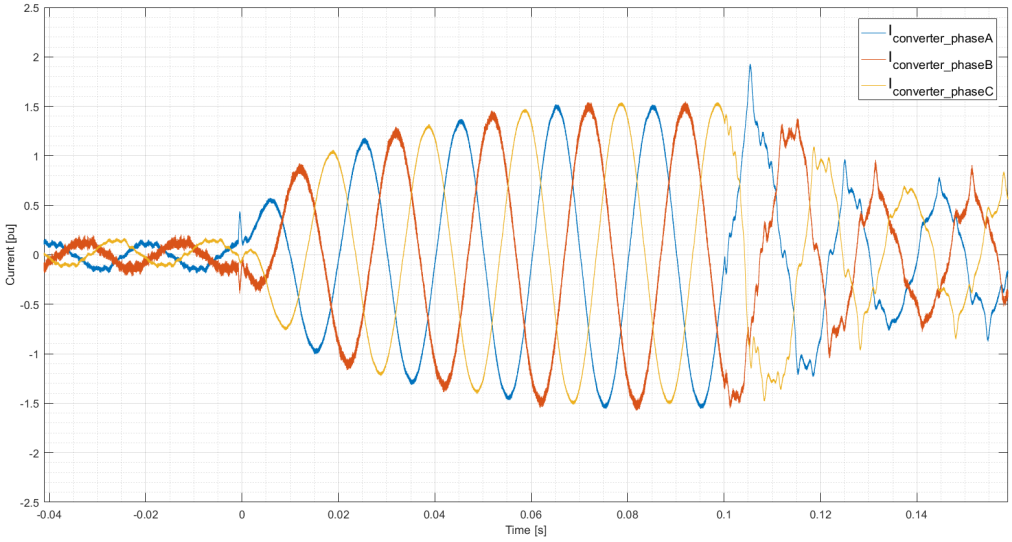
Figure C.3.2 illustrates $I_{converter}$ for a 100 ms three-phase short circuit for different values of T_{sync}, with control scheme 2.



(a) T_{sync} = 6.6 ms.



(b) T_{sync} = 13.3 ms.



(c) T_{sync} = 20.0 ms.

Figure C.3.2: $I_{converter}$ for a 100 ms three-phase short circuit for different values of T_{sync}, with control scheme 2.

Short circuit duration

Figure C.3.3 illustrates $I_{converter}$ for a 500 ms three-phase short circuit, with control scheme 1. T_{short} was also set to 200 ms and 300 ms, the behaviour of $I_{converter}$ was similar in these tests. Therefore, these graphs are not included here. Still, $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{\_SC\_}{normal}}$ for these tests can be found in Table C.2.1.

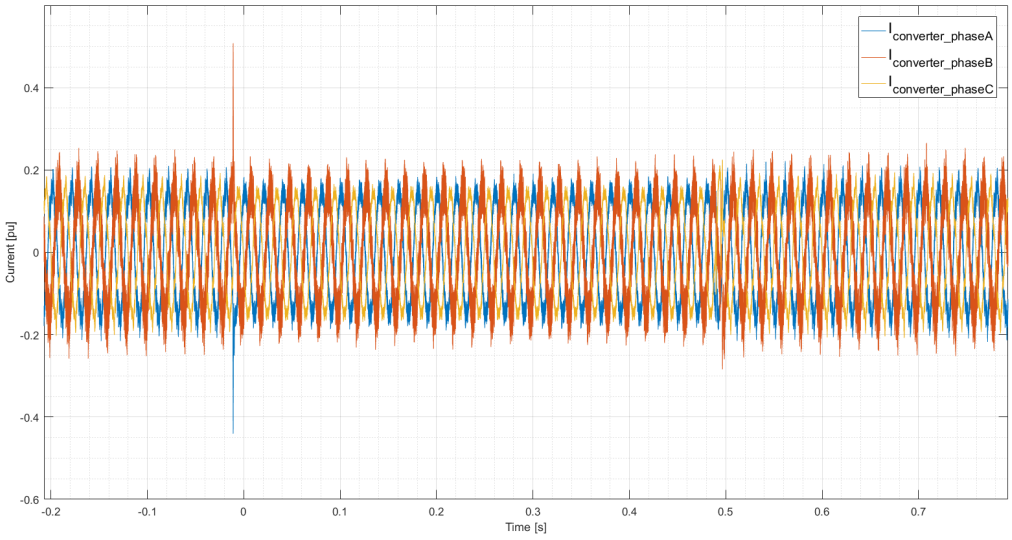


Figure C.3.3: $I_{converter}$ for a 500 ms three-phase short circuit,with control scheme 1.

Type of Short Circuit

The effect of changing T_{sync} is similar when a phase-to-phase short circuit occurs, as when a three-phase short circuit occurs. Figure C.3.1 illustrates $I_{converter}$ for a 100 ms phase A to phase B short circuit, with control scheme 1. T_{sync} was also set to 6.6 ms, 8.3 ms, 9.8 ms, 9.9 ms. Except from the first and the third period of the short circuit, the $I_{converter}$ was similar for the different tests. The impact of T_{sync} on the first and second period were illustrated in Section 6.3. Therefore, these graphs are not included. Still, $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{\_SC\_}{normal}}$ for these tests can be found in Table C.2.2.

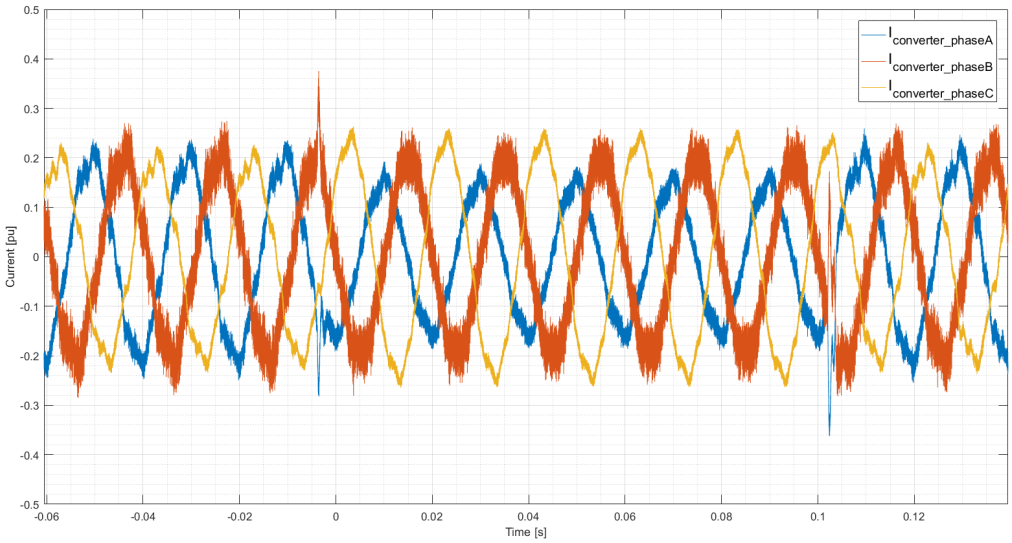
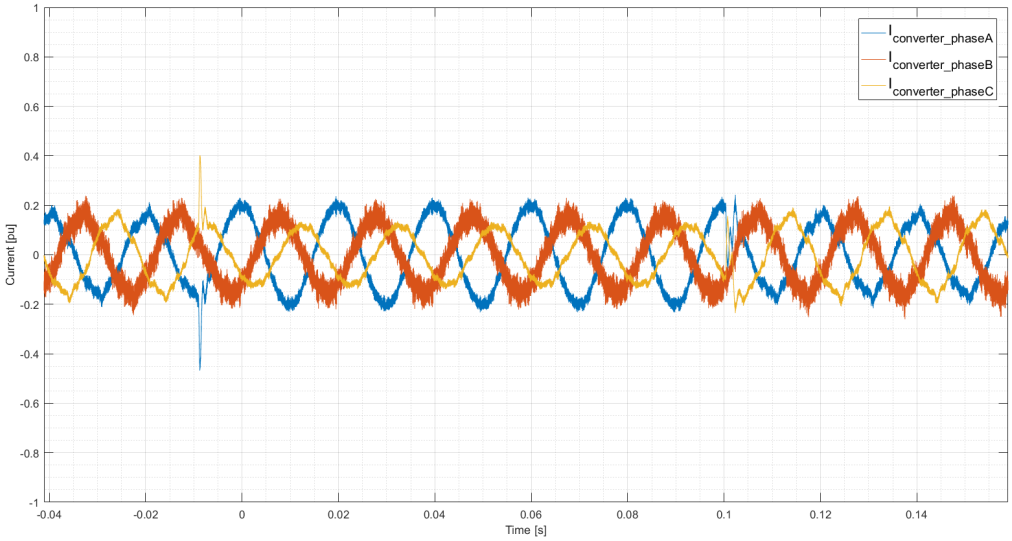
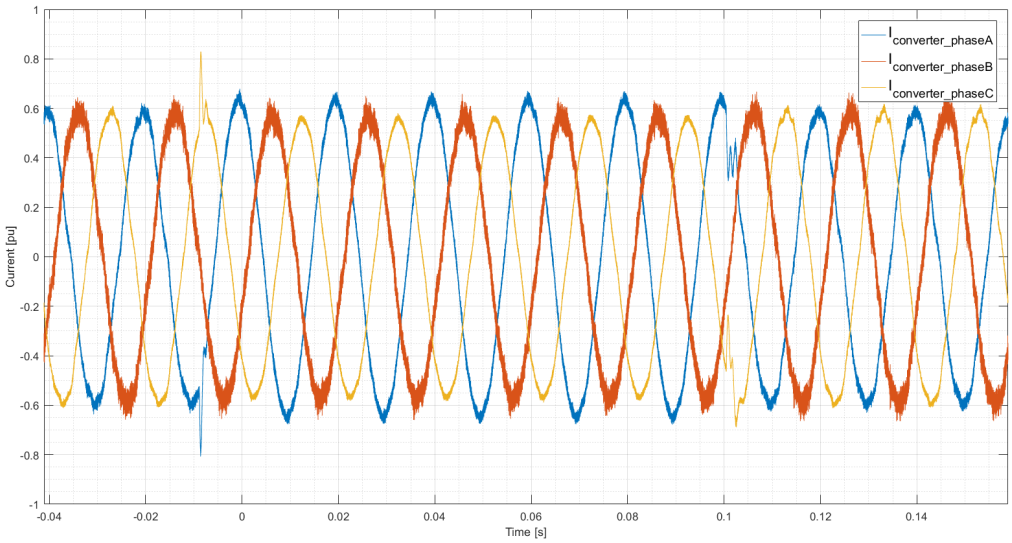


Figure C.3.4: $I_{converter}$ for a 100 ms phase A to phase B short circuit with T_{sync} equal 13.3 ms, with control scheme 1.

Figure C.3.5 illustrates $I_{converter}$ for a 100 ms phase A to phase C short circuit, with control scheme 1. In the tests I_{active_ref} was changed from 0.10 pu to 0.40 pu, while T_{sync} was equal to 13.3 ms. $I_{initial\_peak\_positive}$, $I_{initial\_peak\_negative}$ and $R_{\frac{SC}{normal}}$ for these tests can be found in Table C.2.2.



(a) $I_{active\_ref} = 0.10$ pu.

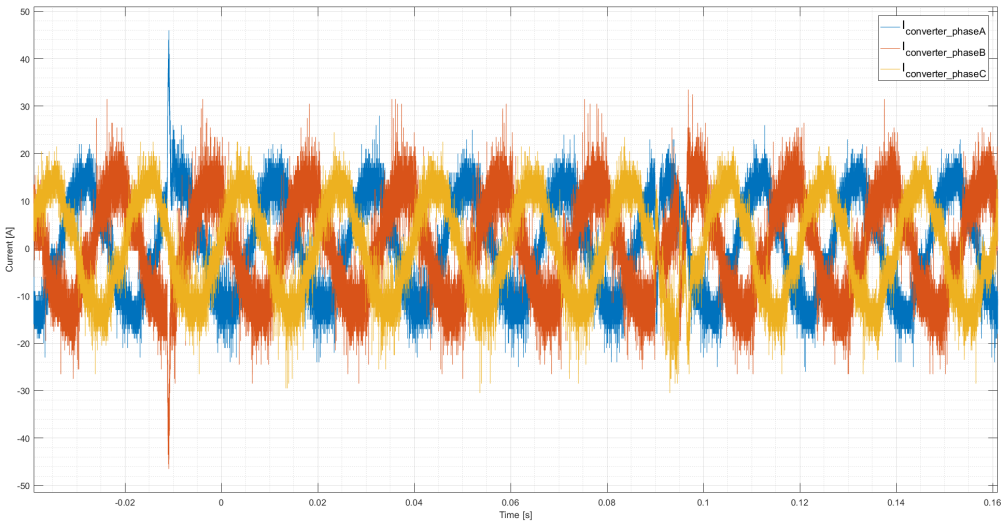


(b) $I_{active\_ref} = 0.40$ pu.

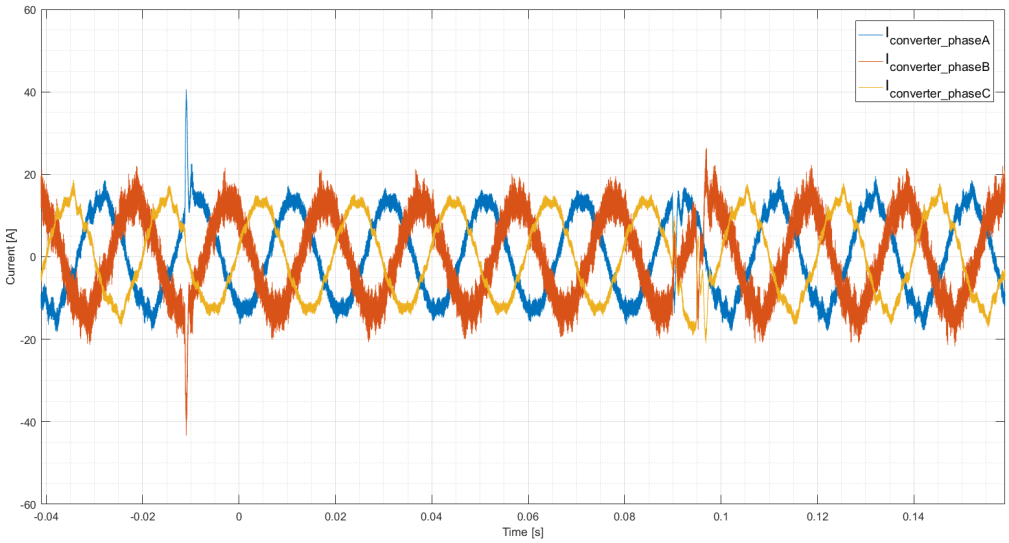
Figure C.3.5: $I_{converter}$ for a 100 ms phase A to phase C short circuit for different values of I_{active_ref}, with control scheme 1.

Additional Comments to the Results

In this section the effect of changing acquisition mode from Sample to Hi Res is illustrated. In Figure C.3.6 (a) $I_{converter}$ is illustrated with the acquisition mode set to Sample, while in Figure C.3.6 (b) $I_{converter}$ is illustrated with the acquisition mode set to Hi Res. Apart from this, every parameter settings are equal in the two tests. It should be noted that these graphs are illustrated in real-units.



(a) Sample Mode.



(b) Hi Res Mode.

Figure C.3.6: $I_{converter}$ for a 100 ms three-phase short circuit with I_{active_ref} equal to 0.10 pu, T_{sync} equal to 9.8 ms and Z_{sc} equal to 2 mH, for two different acquisition modes.