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Design and Performance Analysis of an Electric Motor Drive utilizing Sillicon Carbide MOSFETs

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Abstract

The recent commercialization SiC technology, has made it desirable to use SiC in electrical motor drives for marine applications, due to the superior material qualities of SiC compared to conventional Si based technology. This Master thesis will present an analysis of the switching performance of a SiC MOSFET module from ROHM Semiconductor, and an accompanying investigation of how a high performance SiC based motor drive can be realized.

As part of the thesis work, the many critical components of an electrical motor drive system was investigated, and this will be described in this thesis. Two printed circuit boards were produced to enable the SiC modules to be operated using a motor controller. In addition, a low inductive three phase DC-bus was designed, produced and tested.

The three phase DC-bus design will be described through theoretical considerations, before an experimental analysis of the stray inductance of the DC-bus is presented. It will be shown that a low inductive design can be realized through the use of planar copper conductors, and the DC-bus design has good inductive capabilities compared with a single half-bridge DC-bus which was used in the experimental SiC characterization.

The SiC module performance characterization was conducted by performing double-pulse testing, both in simulations and in laboratory experiment. It was shown that the presence of stray inductive elements in the circuit causes voltage overshoots up to 110 V over the nominal voltage of 600 V and long lasting ringing. The switching characteristics calculated from these tests will be presented, and the circuit dynamics giving rise to these effects discussed. A comparison between the simulation results and experimental results was made, and it will be shown that while the simulation model captures some switching characteristics well, it fails to model the large voltage overshoots observed in laboratory experiments.

Further more, it was investigated if switching performance could be improved through the introduction of snubber circuits, in particular RC turn-off snubbers and DC-snubbers. Both the simulation results and the experimental results showed that the RC turn-off snubbers failed to remove the overvoltages completely, but was able to reduce it to 35 V with a snubber damping constant of 0.4. This comes at the cost of increased switching losses however, and it is clear that a trade off must be made.

Sammendrag

I nylig tid har utviklingen av kraftelektronikk-teknologi basert på silisiumkarbid nådd kommersialisering. Ettersom silisiumkarbid innehar mange overlegne materialegenskaper sammenlignet med konvensjonell silisiumsbasert teknologi, er det ønskelig å utnytte silisiumkarbid i motordrivere for marine anvendelser. Denne masteroppgaven presenterer en analyse av brytningsforløpet til en silisiumkarbid-MOSFET-modul levert av ROHM Semiconductor, og en tilhørende analyse av hvordan en motordriver basert på silisiumkarbid med høy ytelse kan realiseres.

Deler av komponentene som inngår i en motordriver ble utforsket som en del av masterarbeidet, og vil bli beskrevet i denne oppgaven. Det ble utviklet og produsert to kretskort som muliggjør styring av silisiumkarbid-modulen med et eksisterende kontrollsystem. I tillegg ble det designet, produsert og testet en lavinduktiv trefase DC-buss.

DC-bussen vil bli beskrevet gjennom teoretiske betraktninger, før en eksperimentell analyse av strøinduktansen til DC-bussen blir presentert. Det ble vist at et lavinduktansdesign kan realiseres ved å benytte et plant design til bussen, og at dette designet har lave induktansverdier sammenlignet med en eksisterende DC-bus laget for en enkelt halvbro.

Karakteriseringen av silisiumkarbid-modulen ble gjennomført ved hjelp av dobbelpuls-testing, og denne testingen ble gjort både gjennom datasimuleringer og eksperimentelt arbeid i laboratoriet. Det ble vist at strøinduktans i kretsen fører til overspenninger på opp til 110 V over det nominelle spenningsnivået på 600 V, og langvarige osilleringen oppstår. De beregnede brytningskarakteristikkene fra testene vill bli presentert, og ulik kretsdynamikk som påvirker disse karakteristikkene blir diskutert. Det ble gjort en sammenligning mot simuleringsresultatene, og det vil bli vist at mens simuleringsmodellen klarer å gi noen av karakteristikkene som ble målt i det eksperimentelle arbeidet, klarer modellen ikke å gi de samme overspenningene som ble observert i laboratoriet.

Det ble også undersøkt hvorvidt ytelsen kunne forbedres ved hjelp av kretser som øker kretsens demping, såkalte snubber-kretser. DC-snubbere og avslags-snubbere ble benyttet i denne undersøkelsen. Både simuleringsresultatene og det eksperimentelle arbeidet viser at avslags-snubberen ikke klarer å fjerne all overspenning fullstendig, men at overspenningen kan reduseres til rundt 35 V for en avlsags-snubber med 0.4 dempingskonstant. Dette kommer riktignok med den prisen at kretsens totale tap øker, og det er opplagt at det må gjøres en avveining mellom ulike faktorer.

Preface

I had the pleasure of spending my fourth year of university on exchange at ETH Zürich in Switzerland. There, I was introduced to the field of power electronics, and was able to learn from arguably one of the best people in the field, Prof. Johan Kolar. It was only natural that I continued my studies of power electronics when I got home and received an internship at Rolls-Royce Marine in Trondheim. When I started working there for the summer, and began working on the project that later developed into this Master thesis, I wasn't entirely sure what to expect of my choice of direction. Today however, I am truly grateful that I made it. While I have certainly felt the immense pressure caused by the unpredictable, though seemingly bound to arise, problems related to practical laboratory work at times, the one year's work put into this project has been interesting, fulfilling, and even great fun!

I would like to thank my supervisor Prof. Ole-Morten Midtgård for his thoughtful advice and guidance. He has been able to provided a sense of direction in the project at times when it was much needed. I would like to express my sincere gratitude to Dr. Richard Lund, at Rolls-Royce Marine in Trondheim. It has been a pleasurable and great learning experience working with him. I regret not meeting him more often, but Skype for Business did at least work for us sometimes, and gave me the opportunity to seek his essential guidance. I also would like to thank Ole Christian Spro, a PhD student at the Department of Electric Power Engineering at NTNU. He became a great support to me, at the time when I spent my most intense days and nights in the lab, always willing to help with any question I might have had.

Finally, I would like to thank my parents. I would not have known about the wonderful world of science and technology that knowledge and learning open the door to, if it weren't for them, and for that I will be forever grateful.

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List of Abbreviations

BOM	Bill of materials
BJT	Bipolar junction transistor
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
MOSFET	Metal-oxide-semiconductor field-effect-transistor
PWM	Pulse width modulation
SBD	Schottky barrier diode
SiC	Silicon Carbide
SPICE	Simulation program with integrated circuit emphasis

Chapter 1

Introduction

1.1 Problem Background

In recent years, power electronic components which utilize wide bandwidth materials has begun to reach commercialization. Wide bandwidth materials, such as silicone carbide (SiC) and gallium nitride (GaN), provide many desirable qualities compared to conventional silicone technologies, commonly used in power electronics today. These qualities include the possibility for faster switching, decreased power loss and improved thermal conduction capacbilities [3]. The conventional power electronic system in the mid-level voltage range relay primarily on silicon IGBTs today, but the advancements in wide bandwidth materials, in particular SiC, has started to make these technologies viable alternatives [3]. While SiC technology has been researched for many years, the technology has not reached commercialization until now, due to the difficulties involved in the production process [4], [7].

The increasing deployment of electrical equipment in a wide range of applications requires power electronic converters with a high level of robustness and efficiency. This is of particular importance in marine power systems, where the converters will experience harsh environments, and also need to be highly compact. The converter volume can be decreased by reducing losses, which influence the size of the cooling system. If a passive cooling system can be deployed, this has important effects on the robustness of the converter, as the system's complexity can be reduced. Passive filter components also influence converter volume, and these components can be reduced in size by increasing the switching speed of a converter [3].

The superior material qualities in SiC technology makes it possible to reduce both losses and filter component sizes, and it therefore seems desirable to utilize SiC in marine power electronic systems. The use of wide bandwidth materials, and exploitation of their qualities, introduces some challenges that needs to be tackled however. The fast switching of the SiC switches causes problems with voltage overshoot and potentially severe EMI problems, due to stray inductances present in the converter circuit. A careful approach to the design and development of SiC based converters should be taken, to mitigate such problems. Important actions to decrease voltage overshoot and EMI problems include stray inductance minimization, and deployment of snubber circuits [8].

1.2 Objective of Master Thesis

Part of the objective of this Master thesis was to test, analyze and improve the performance of a SiC based MOSFET half-bridge module. This should be done through computer simulations, and experimental testing. A comprehensive analysis software was developed in the project work [1], to run computer simulations of the MOSFET module using LTspice. The laboratory work here investigated if these simulations, and the calculations done in the subsequent analysis, could be used in the converter design process to a satisfactory degree, by comparing the calculated characteristics. Further, the laboratory work had as goal to characterize the switching transitions of a SiC MOSFET module, and see if the performance could be improved through snubber circuits.

In addition to this, other components needed in a complete SiC based converter system should be investigated and designed. Of particular importance is the DC-bus bar, acting as a DC-link to the converter. The DC-bus bar is a potential source of high stray inductance, so a DC-bus having low inductive qualities should be designed.

The work done in this Master thesis has been part of a longer spanning project at Rolls-Royce Marine to develop a high-performance SiC MOSFET based electric motor drive. The objective in this thesis was to push the development of such a motor drive forward, through the design and testing of critical parts of the system, such as the SiC MOSFET half-bridges and the low inductive DC-bus. The Master thesis work was conducted as a natural following of a project in the previous semester, and many of the aspects investigated here builds on the work that was done as part of that project [1].

1.3 Report Outline

Following this introduction chapter, is a theory chapter outlining important theoretical background necessary for the continuation. Because this Master thesis is a natural continuation of the project work, focusing on many of the same aspects, most parts of the theory chapter is a repetition of the theoretical background that was presented in the project report [1].

After the theory chapter, a comprehensive description of the theoretical and practical design aspects of a three phase DC/AC converter is presented and discussed. In this chapter a piggyback board design, developed to expand the functions of the gate driver used in the laboratory tests, is presented. The design is based on the gate driver design that was presented in the project report. A DC-bus design for a three phase converter is also presented in this chapter.

The next chapter presents the laboratory setup and procedures that was used to investigate the SiC MOSFET module performance in this thesis work. The results from a preliminary double-pulse test, which was used to determine the stray inductance present in the experimental setup, is also discussed. Then the same inductance is investigated through the use of an impedance analyzer, and the stray inductance of the DC-bus used in the laboratory setup is compared with the inductance of the new DC-bus designed for a three phase converter.

In chapter five the LTspice simulations methodology and results are presented. In these tests, a double-pulse equivalent to the one used in the experimental tests, is used to investigate switching characteristics of a simulation model of the test object later used in the laboratory.

Chapter six includes the result and analysis of the experimental double-pulse tests conducted with the 120 A-module. These results are compared to the simulation results of the same MOSFET module.

The last chapter concludes the Master thesis, and provides a discussion of scope of future work.

Chapter 2

Theory

Parts of this chapter are taken from the theory chapter written for the project report [1], as it is also relevant for this thesis. Some parts are modified, and additional sections have been added.

2.1 Semiconductor Physics

The SiC half-bridge modules investigated in this project consists of MOSFETs, with Schottky barrier diodes connected in anti-parallel with the MOSFETs. The following sections contain a brief description of the physics of these devices.

2.1.1 Power Diodes

Regular diodes are built from simple pn-junctions, and are so called minority carrier devices [8]. This means that both minority carriers and majority carriers are contributing to conduction. When semiconductor materials with different doping levels are placed together, some of the free holes in the p-type material jumps over to the n-type material where they create a positive charge. Similarly some of the free electrons of the n-type material move to the p-type material where they create a net negative charge. The charged layer that is formed is called a depletion layer [8]. If a voltage is connected to the pn-junction, with the positive terminal connected to the p-type material, the depletion layer decreases and the diode will become forward biased. If the polarity of the voltage switches, the depletion layer is increased and the diode is able to block the voltage across it. The diode is now said to be reverse biased.

At turn-on of minority carrier devices, minority carriers must be injected into the device, and are stored in the device during the turn-on interval. At turn-off these charges must be removed from the device through recombination, for the device to be able to become reverse biased and block voltage. This charge removal leads to a reverse recovery current, which is undesirable [8].

Schottky barrier diodes (SBD) are fundamentally different from regular power diodes, as they contain no pn-junction. Instead, a thin metal film is deposited on a doped material. Due to the difference in the absolute potential energies of the two materials, a depletion layer is still formed [8]. SBDs are majority carrier devices, and need therefore not be injected with minority carriers to become forward biased. Due to the reduction in recovery time, SBDs are faster switching devices than the pn-junction diodes [14]. In addition, SBDs have significantly smaller voltage drops than regular power diodes at turn-on. The breakdown voltage of silicon based SBDs is limited to 200 V typically [8], however the introduction of SiC in the SBDs increases this limit, making it possible to utilize SBDs for higher voltage applications [14].

2.1.2 Power MOSFETs

Metal-oxide-semiconductor field effect transistors (MOSFET) are created from pnp-junction or npn-junctions. They are three terminal devices, where the current between the drain and source terminals can be controlled by applying a voltage to the gate terminal [8]. MOSFETs are majority carrier devices, making them fast switching compared to minority carrier devices. Compared to minority carrier devices, they have higher turn-on losses and lower breakdown voltage however. This has made minority carrier devices such as IGBTs more prominent in the mid level voltage range, though the recent introduction of SiC in MOSFETs have made these devices able to compete [3].

2.2 Silicon Carbide

Silicon carbide (SiC) is a wide bandgap semiconductor, and offers several beneficial properties compared to silicon (Si). SiC has a bandwidth energy of 3.26 eV, compared to 1.12 eV for Si [6]. This means that the electrons in the SiC material require a larger energy for the covalent bonds between the atoms to be broken. For this reason the leakage current of SiC is significantly smaller for a given blocking voltage, and the material can sustain higher junction temperatures before the leakage current becomes too large.

The saturated drift velocity of SiC is $2 \cdot 10^7 \mathrm{cm\,s^{-1}}$, twice as large as for Si [6]. The higher drift velocity makes faster switching possible, as the electrons can move faster through the material. Increase in switching frequency is desirable, as filter components can be reduced and the converter volume with it [7].

SiC has 10 times higher critical electrical field for breakdown, compared to Si [5]. This enables higher blocking voltages for SiC devices compared to similar Si technologies. Further more the higher electrical breakdown field makes it possible to make the SiC devices thinner. Shorter distance of the drain-source region leads to lower resistance in the device at turn-on [8].

Finally, the thermal conductivity of SiC is approximately three times higher than that of Si [6]. The improved thermal conductivity leads to better heat transportation away from the junction, reducing the risk of thermal runaway.

All of the properties described above enable SiC devices to be much more compact, compared to Si devices with similar current and voltage ratings. By increasing the switching frequency, smaller passive filter component can be deployed. The improved thermal properties, both in terms of less dissipated heat due to lower losses and better thermal conductivity, makes it possible to use smaller and more efficient cooling systems.

2.3 Power Electronic Converters

A large variety of different converter topologies exists. A simple buck converter and a three phase topology will be described to highlight some important aspects when designing power electronic converters.

2.3.1 Buck Converter

The basic circuit of a buck converter is shown in figure 2.1. The switch T is an ideal switch, i.e. it has no losses and switches instantly. The switch is turned on and off periodically, with a frequency f_s. Within one switching period, $T_s = 1/f_s$, the ratio between the time interval the switch is turned on and the full switching period is given by the duty ratio $D = t_{on}/T_s$ [8].

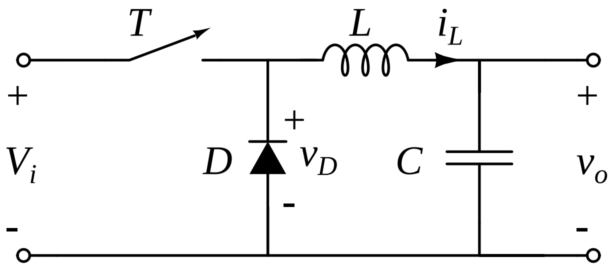

Figure 2.1: Buck converter.

In the turn-on interval, the switch conducts the current i_L from the voltage input to the output side. The voltage across the freewheeling diode D_f will now be equal the input voltage V_i. As the switch is turned off, the current through the switch instantly goes to zero. The inductor L cannot have an infinite di/dt and impresses the current i_L through the diode D_f instead. The diode is said to be freewheeling the current when the switch T is turned off, hence the term freewheeling diode [8]. The voltage across the diode is zero when it is forward biased, and the diode voltage v_D thus gets a square shape. The diode voltage is filtered by a LC low pass filter, and so the output voltage v_o can be approximated by the average voltage across the freewheeling diode over a switching period [8]:

$$v_o \approx \frac{1}{T_s}\int_0^{T_s} v_D(t)dt = \frac{1}{T_s}\left(\int_0^{DT_s} V_i dt + \int_{DT_s}^{T_s} 0 dt\right) = \frac{1}{T_s} DT_s V_i = DV_i. \tag{2.1}$$

In reality the low pass filter will slip some AC voltage through, resulting in a small ripple in the output voltage around the DC voltage described by the equation above. The magnitude of this ripple can be controlled by tuning the component values of the low pass filter.

2.3.2 Three Phase Full-Bridge Converter

Figure 2.2 shows a three phase full-bridge configuration. The configuration consists of three separate bridge legs. The dashed line in the figure marks one bridge leg. A bridge leg consists of two switches, only capable of conducting current in one direction. Each switch has a diode connected in anti parallel, meaning the diode conducts current in the opposite way of the switch. For each bridge leg, an output terminal is connected between the switches.

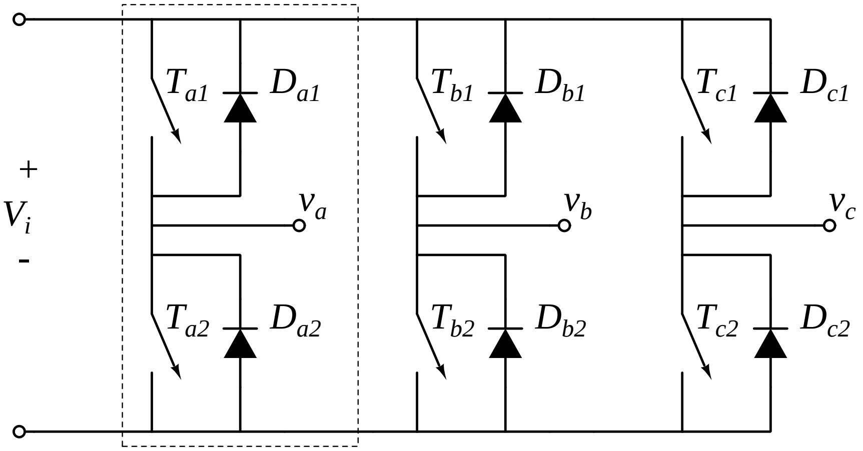

Figure 2.2: Three phase full-bridge configuration.

The operation of the full-bridge converter will now be described, by first considering the behavior of one bridge leg. Figure 2.3 shows a bridge-leg with an output load. It is assumed that the load is connected after a low pass filter with a large inductor. The large inductor will force the output current to remain at an almost constant level over one switching period, and for this discussion the load will therefore be simplified as a current source. The left and right circuit in the figure shows the load current i_{load} being poitive and negative, respectively.

The switches T_1 and T_2 cannot be closed simultaneously, as this will lead to short circuiting the input voltage V_i. When switch T_1 is turned on, the output terminal voltage v_a will be clamped to the input voltage. When switch T_2 is turned on, after turning off switch T_1, the output voltage v_a will be clamped to zero. The output voltage of a bridge leg will therefore switch between the input voltage and zero in a square shaped manner.

When a load is connected on the output terminal, the current path will be determined by the current direction. The left circuit of figure 2.3 shows the situation with positive load current. As the figure shows, the conduction path goes through the switch T_1 when the output terminal is clamped to the upper rail, and through diode D_2 when the output terminal is clamped to the lower rail. As switch T_2 turns off, the constant load current needs a current path and must therefore go through diode D_2, in the same way as described for the buck converter. This will happen immediately as the upper switch is turned off, and also here the diode is said to be freewheeling. The circuit to the right shows a negative load current, and here the opposite conduction paths occur. When T_2 is turned on the output terminal is clamped to zero and switch T_2 conducts the load current. Right after T_2 turns off the load current impresses a current through diode D_1, causing it to get forward biased.

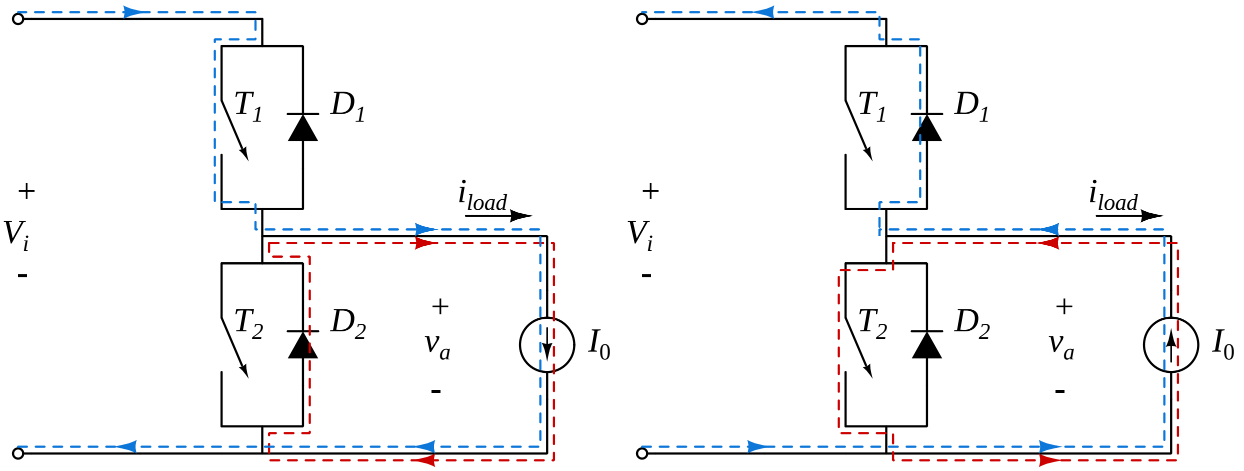

Figure 2.3: Bridge leg conduction paths.

A half-bridge configuration can be used to generate sinus waves. This is done by turning the switches on and off, with a varying duty ration, as described in more depth in section 2.3.3. Though this is also possible with a buck type topology (the left circuit of figure 2.3 is essentially a buck type topology, since the components D_1 and T_2 are not in use), a full-bridge topology has the advantage that it can conduct current in both positive and negative direction [8]. This would for example occur when a load is connected between terminal a and b in figure 2.2, and bridge leg a is clamped to zero while bridge leg b is clamped to the upper rail. When the three bridge legs in figure 2.2 are switched with a phase shift between the legs, a three phase sinusoidal voltage is generated, while allowing current conduction in the appropriate directions.

The three phase bridge configuration can be used to convert DC voltage to AC voltage, with a controlled output frequency and voltage magnitude. The three phase DC/AC converter described is commonly used for electrical motor drives. If a rectifier is connected on the input, along with a capacitor bank, a typical AC/AC converter topology is formed [8].

2.3.3 Control

The principle of how gate signals might be generated is shown in figure 2.4. A triangular wave v_{tri}, referred to as the carrier signal, is fed to a comparator along with a control signal v_{ctrl}. When the control signal has a higher voltage than the carrier signal, the output of the comparator goes high. Else the comparator output goes low. The control method of applying a square pulse with a given duty ration to control the output voltage of a switch is called pulse width modulation (PWM) [8]. Depending on the application, the PWM signal could be amplified to allow a higher power supply to the gate. This is shown in the figure, where the comparator output signal controls two BJTs in totem-pole configuration, so the final gate voltage v_{GG} switches between the correct voltage levels, while being able to handle large enough currents.

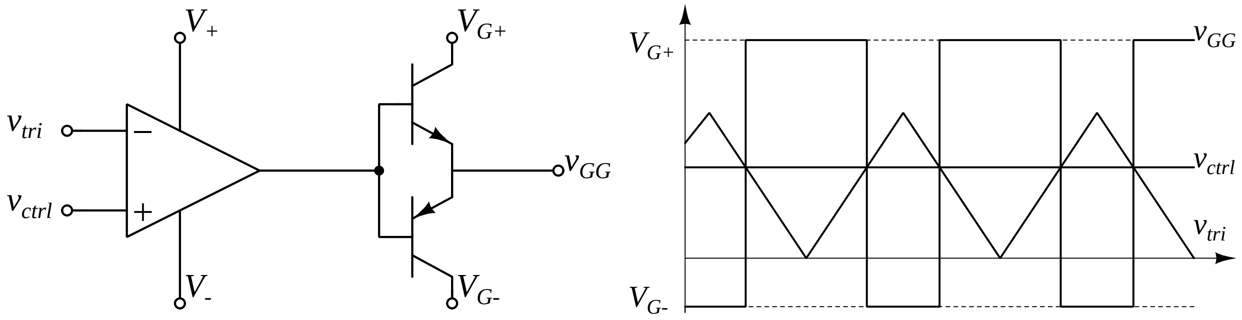

Figure 2.4: Gate signal generation

If the control signal v_{ctrl} is a sinus curve with frequency much lower than the triangular carrier signal, the pulse width modulated gate signal will get a varying duty ratio so that its first harmonic is a sinus curve [8]. In this case the control signal is called the modulation signal, as it is modulating the gate voltage. Through pulse width modulation, a half-bridge topology can convert DC voltage to sinusoidal AC voltage. By applying the same switch signal on all bridge legs, though with a $2\pi/3$ radians phase shift between the signals to each bridge, the output on the terminal will be a three phase sinusoidal voltage.

An important consideration in the switching operation of bridge legs, is making sure the switches in a bridge leg are not turned on simultaneously. To account for non idealities such as turn-on and turn-off times, a time interval between turning one switch off and the other on should be applied. This time interval is called the dead-time, and causes a negative impact on the converter performance [10].

2.4 Characteristics of Power MOSFET Operation

The turn-on and turn-off switching characteristics of power MOSFETs will be described in the next sections. A simple DC-DC converter will be used to discuss the transients, and a constant load current I_0 will be assumed. Power MOSFETs have parasitic capacitances between all of the three terminals; drain, source and gate [8]. In the discussion of the switching transients however, the drain-source capacitance will be neglected, as it does not affect the switching waveforms [8].

The circuit model used for the MOSFET is showed in figure 2.5. The constant load current I_0 can be seen in parallel with the freewheeling diode D. The MOSFET can be modelled as a voltage controlled current source initially, and further be modelled as a resistance as the MOSFET reaches the ohmic region in the turn-on transition [8]. During the turn-off transition the MOSFET is first considered a resistance, and then a voltage controlled current source as the gate voltage decreases. The parasitic capacitances C_{GD} and C_{GS}, the gate-drain and gate-source capacitance respectively, are also shown in the figure. The gate voltage source V_{GG} is series connected with a gate resistance R_G.

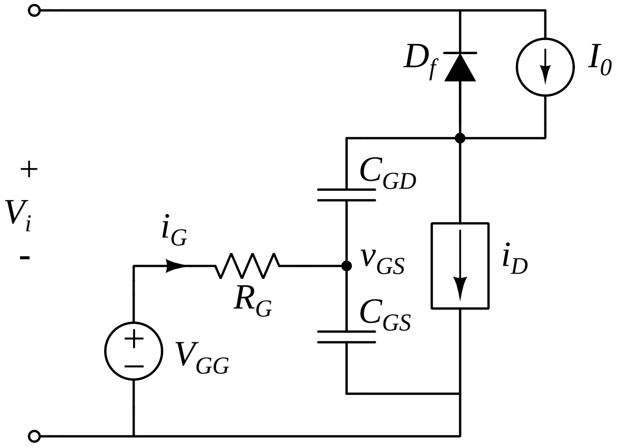

Figure 2.5: Circuit model of MOSFET.

The gate-drain capacitance has a significant drain-source voltage dependence [8], however it is approximated to be constant in this consideration for simplicity.

2.4.1 Switching Waveforms

Figure 2.6 shows approximated waveforms of MOSFET in the turn-on transition. The turn-on transient begins as the gate voltage source V_{GG} steps up to its on-state voltage level, at time $t = 0$. The gate voltage v_{GS} then starts to rise with the an exponential trajectory, until it reaches the threshold voltage $V_{GS,Th}$, as shown in the figure. The exponential curve has time constant $\tau_{turn-on} = R_G(C_{GD} + C_{GS})$. Now the MOSFET starts to conduct, and the drain current is given by [8]

$$i_D = g_m(v_{GS} - V_{GS,Th}). \tag{2.2}$$

The drain-source voltage remains clamped to the input voltage, as the freewheeling diode is still conducting. The time used for the current to reach its on state level is the current rise time t_{ri}. The rate of which v_{GS} changes is given by the time constant $\tau_{turn-on}$, so the current rise time t_{ri} and the di/dt can be changed through adjustments of the gate resistance.

Once the MOSFET is conducting all of the load current, the diode can become reverse biased. Assuming an ideal diode with no reverse-recovery current, the diode becomes reverse biased instantly. The voltage across the MOSFET is not yet in the ohmic region, and the gate-source voltage v_{GS} is clamped to v_{GS,I_0}, the level necessary to carry the drain-current I_0 while the drain-source voltage starts to fall. Since the gate-source voltage is clamped, the entire gate current i_G flows through the gate-drain capacitance, discharging it as the drain-source voltage decreases. The drain-source voltage and gate-drain voltage now change at an equal rate, given by [8]

$$\frac{dv_{GD}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = \frac{V_{GG} - v_{GS,M}}{R_G C_{GD}}. \tag{2.3}$$

The drain-source voltage fall time is t_{fv}, and from equation (2.3) its clear that the fall time an the dv/dt of the transient can be varied by adjusting the gate resistance.

The turn-on transient is over once the MOSFET leaves the active region, and the drain-source voltage reaches its on-state voltage fall $V_{DS,on} = R_{DS,on} I_0$.

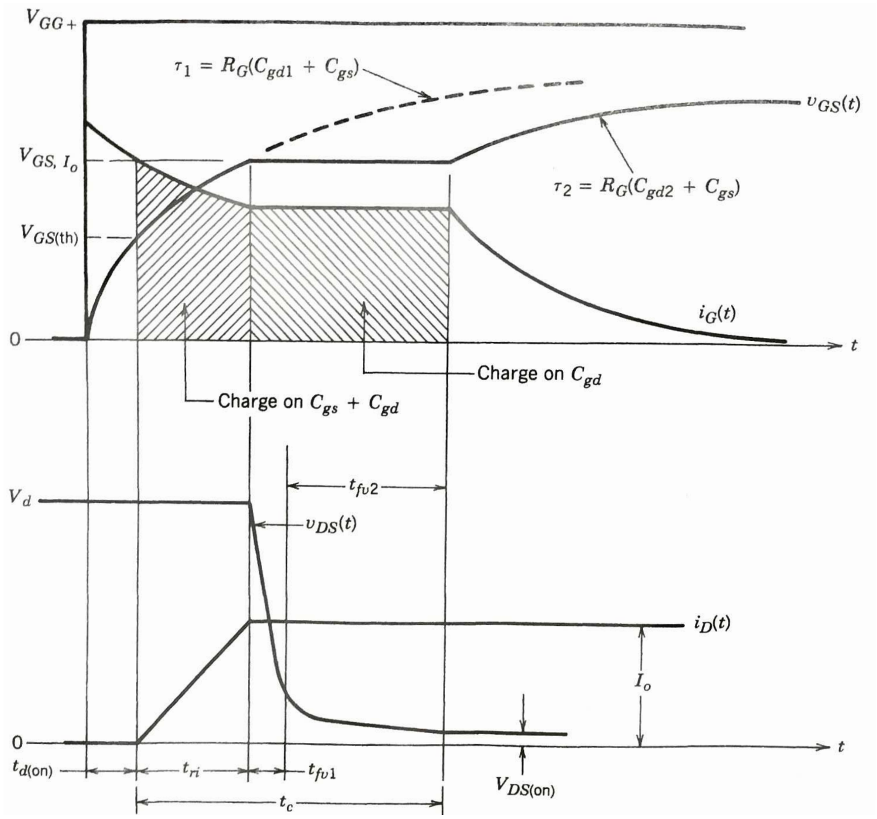

Figure 2.6: Turn-on switching waveforms of MOSFET [8].

The turn-off transient of a MOSFET is essentially the same as the turn-on transient, in a reversed order. The voltage rises to the same value as the input voltage, before the drain-current starts to fall.

2.4.2 Power Loss

At the switching transients of a MOSFET, there is an overlap where both the drain-source voltage and the drain current is non-zero. At turn-off the current through the MOSFET does not start to fall until the voltage across the MOSFET has reached the turn-off value, and at turn-on the voltage does not start to fall before current reaches the constant conduction values. For this reason switching losses occur in the transient intervals. In addition there is a slight voltage fall across the MOSFET at turn-on, causing conduction losses [8]. A small leakage current is also conducted at turn-off, however this is usually small compared to the other sources of power loss in the MOSFET [13], and will therefore not be considered.

The average power loss in the MOSFET in any time interval T, beginning at t_0, is given by [16]

$$P_{sw} = \frac{1}{T}\int_{t_0}^{t_0+T} v_{DS}(t) i_D(t) dt. \tag{2.4}$$

The switching loss can then be calculated by identifying when the switching transient begins, i.e. t_0, and the duration of the switching transient T. As seen in the above section, the switching intervals increase with increasing gate resistance. Increasing the gate resistance will therefore increase switching losses, since a larger interval where the voltage and current are non-zero will be produced.

The average conduction losses P_c are given by

$$P_c = V_{DS,On} I_D = I_D^2 R_{DS}, \tag{2.5}$$

as the current through and voltage across the MOSFET is constant at turn-on [8]. The on-state resistance can thus be calculated by measuring the voltage fall over the MOSFET, and the drain current through it.

2.4.3 Non-Ideal Switching Characteristics

Due to parasitic capacitances and inductances present in power electronic circuits, oscillations in voltage and current occur in the switching transients. To consider the oscillations of the voltage across a MOSFET at switching, the MOSFET will be modelled as an ideal switch with a parasitic capacitance C in parallel. When the transistor is used in a circuit with a stray inductance L and total resistance R, the circuit model in figure 2.7 is obtained.

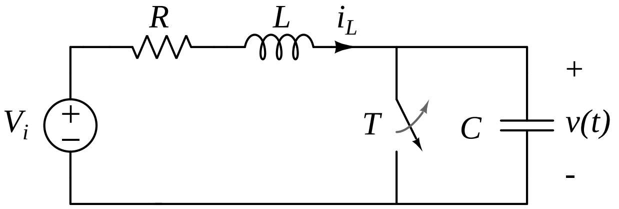

Figure 2.7: LC-tank model.

The differential equation of the circuit, when the switch is turned-off, is given by [16]

$$LC\frac{d^2v(t)}{dt^2} + RC\frac{dv(t)}{dt} + v(t) = V_i, \tag{2.6}$$

and the solution to its characteristic equation is

$$\lambda = -\alpha \pm i\beta = -\frac{R}{2L} \pm \frac{1}{2}\sqrt{\frac{R^2}{L} - 4\frac{1}{LC}}. \tag{2.7}$$

If the expression under the square root evaluates to a negative value, the voltage $v(t)$ will be underdamped and oscillations will occur. In power electronics, this is often referred to as ringing. The ringing is characterized by its frequency, peak value and exponential decay. When the circuit is underdamped, the oscillating voltage can be expressed as [16]

$$v(t) = v_{ss} + C_1 e^{-\alpha t}\cos(\omega t), \tag{2.8}$$

where v_{ss} is the steady-state value of the oscillation, which equals the input voltage V_i in the circuit model described by equation (2.6). α is the decay ratio, and C_1 is a constant given by the initial conditions of the circuit, as the switch T turns off. ω is the oscillation frequency, given by β in equation 2.7. In the case of the circuit model shown above, the decay ratio is given by $R/2L$.

When a voltage oscillation is measured, the frequency can be calculated by measuring the time between two peaks of the oscillation, t_0 and t_1. The oscillation frequency is given by

$$\omega = 2\pi f = \frac{2\pi}{\Delta T} = \frac{2\pi}{t_1 - t_0}. \tag{2.9}$$

In the time instances where the voltage reaches its peaks we have that $\cos(\omega t) = 1$. The exponential decay, given by the decay ration α, can be calculated by measuring the time and voltage of two consecutive peaks $\hat{v_0}$ and $\hat{v_1}$:

$$\hat{v_0} = v(t_0) - v_{ss} = C_1 e^{-\alpha t_0}, \quad \hat{v_1} = v(t_1) - v_{ss} = C_1 e^{-\alpha t_1}. \tag{2.10}$$

The decay ration can now be found using the ratio between the magnitude of the two peaks:

$$\frac{\hat{v_1}}{\hat{v_0}} = e^{-\alpha(t_1 - t_0)} = e^{-\alpha \Delta T}, \tag{2.11}$$

$$\alpha = -\frac{1}{\Delta T}\ln\left(\frac{\hat{v_1}}{\hat{v_0}}\right). \tag{2.12}$$

From equation 2.7 we get that expression for the ringing frequency of an underdamped circuit is

$$\omega = \beta = \frac{1}{2}\sqrt{4\frac{1}{LC} - \frac{R^2}{L}}. \tag{2.13}$$

The equation above can be simplified by assuming that the resistance in the circuit is significantly smaller than the inverse of the parasitic capacitance, i.e. $R^2 \ll 1/C$. In doing so we get the equation of the circuits undamped frequency:

$$\omega = \frac{1}{2}\sqrt{4\frac{1}{LC}} = \frac{1}{\sqrt{LC}}. \tag{2.14}$$

By assuming that the ringing frequency of the circuit is closely approximated by the undamped frequency, the circuit's total stray inductance can be determined by measuring the ringing frequency when the parasitic capacitance is known, and vice versa when the inductance is known. The parasitic drain-source capacitance of MOSFETs is typically given in the datasheet, indirectly through the following relationship

$$C_{DS} = C_{oss} - C_{rss}. \tag{2.15}$$

C_{oss} is the output capacitance, which is the sum of the gate-drain capacitance and the drain-source capacitance, and is measured from the drain terminal with the gate and source terminals shorted. C_{rss} is called the reverse transfer capacitance, which equals the gate-drain capacitance.

2.5 Snubbers

2.5.1 Turn-On Snubbers

Turn-on snubbers are primarily used to reduce the turn-on losses of power transistors, and reduce the reverse recovery current of diodes [8]. The turn-on snubber consists of an inductor, in parallel with a diode and resistor in series, and the turn-on snubber is connected in series with the transistor.

Figure 2.8 shows a MOSFET in series with a turn-on snubber. As described in section 2.4, the voltage will remain constant across the MOSFET in the turn-on transient, until the MOSFET carries the full current. Using a turn-on snubber this voltage can be lowered, since voltage will be induced over the snubber inductor. Assuming a constant current rise, the voltage fall across the inductor will equal

$$v_{L_S} = \frac{L_s I_{DS}}{t_{ri}}, \tag{2.16}$$

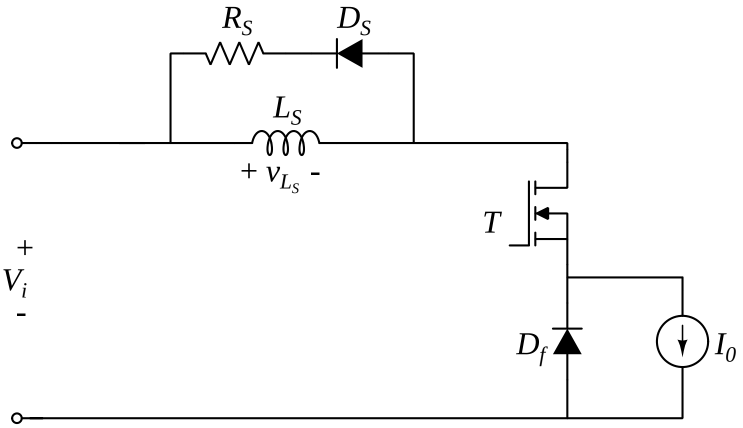

Figure 2.8: Turn-on snubber.

and the voltage across the MOSFET will be lowered to

$$v_{DS} = V_0 - v_{L_S} = V_0 - \frac{L_s I_{DS}}{t_{ri}}. \tag{2.17}$$

At turn-off, the inductor current will be dissipated through the snubber resistor. The resistor and the inductance must be dimensioned so the inductor has enough time to sufficiently recharge during the off state.

The reverse-recovery current of a diode is has an upper bound described by the inequality

$$I_{rr} < \sqrt{2Q_F \frac{di_D}{dt}}, \tag{2.18}$$

where Q_F is the stored charge removed from the diode by the reverse-recovery current [8]. i_D is the diode current, and equals the drain-source current of a MOSFET when the diode is used as a freewheeling diode. The current time derivative is equal the di/dt across the turn-on snubber. If we assume a sufficiently large snubber inductance L_s, so that the whole input voltage V_0 lies across the inductance, we get

$$I_{rr} < \sqrt{2Q_F \frac{V_0}{L_S}}. \tag{2.19}$$

From equation (2.19) it is clear that the reverse-recovery current through the freewheeling diode, and subsequently the current overshoot of the MOSFET being turned on, can be limited by utilizing a turn-on snubber with sufficiently high inductance. This will increase the turn-on time however, as the inductor di/dt is decreased.

2.5.2 Turn-Off Snubbers

A turn-off snubber tries to achieve zero voltage across a transistor, as the transistor is switching from on-state to off-state [8]. The turn-off snubber can be implemented as a RCD network connected across a transistor, as shown in figure 2.9.

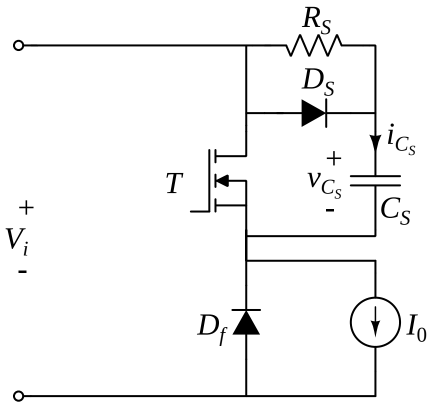

Figure 2.9: Turn-off snubber.

As the transistor is turned off, the current I_0, originally flowing through the transistor, starts to charge the snubber capacitor. When the capacitor is fully charged and reaches V_d, the freewheeling diode gets forward biased and the input voltage V_d is clamped across the transistor. The voltage across the diode, and the transistor, is given by [8]

$$v_{C_s} = \frac{1}{C_s}\int_0^t i_{C_s} dt = \frac{I_o t^2}{2C_s t_{fi}}, \tag{2.20}$$

where v_{C_s} is the voltage across the snubber capacitor C_s, i_{C_s} is the current through the snubber capacitor, and t_{fi} is the time the transistor current uses to turn off, i.e. go to zero. If we set $t = t_{fi}$, the voltage across the transistor and snubber capacitor reaches V_d as the current through the transistor reaches zero, and this yields a snubber capacitance of

$$C_S = \frac{I_d \cdot t_f}{2 \cdot V_{DS}}. \tag{2.21}$$

Increasing the capacitance further will give even lower turn-off losses, since the voltage across the transistor is kept low as the current decreases. However the capacitor will be charged to a higher energy, and this energy must be dissipated at turn-on. The overall losses in the converter might therefore not be minimized by choosing a high capacitance in the turn-off snubber. The capacitor energy will be dissipated through the transistor at turn-on if no snubber resistor is included. Heat transport is usually easier through a resistor however, and using a snubber resistor is therefore desired. The current through the snubber resistor should be higher than the peak recovery current, which is usually limited to under $0.2I_0$ [8]. This gives a lower bound on the snubber resistance at

$$R_S > \frac{V_{DS}}{0.2 \cdot I_D}. \tag{2.22}$$

The turn-off snubber should not be used in bridge configurations, with a turn-off snubber across each transistor, without including a turn-on snubber as well. The reason is that additional turn-on losses will occur. If the goal of including a snubber is to reduce EMI problems however, a modified RC snubber can be used [8].

2.5.3 Snubbers for Bridge Configurations

When two power electronic switches are placed in a half-bridge configuration, the switching dynamics change. RCD turn-off snubbers can no longer be placed across the two switches as unacceptable turn-on currents will be experienced. Thus a turn-on snubber must also be deployed. Alternatively, simpler RC snubbers can be used, if the primary goal is to reduce EMI problems caused by to high dv/dt [8].

2.5.4 RC Snubber Impedance Calculation

The circuit model in figure 2.7 will be used to evaluate reasonable values for the RC-snubbers. To simplify the calculations, an undamped circuit will be assumed, i.e. $R = 0$. The resulting LC-circuit is sometimes referred to as a ”tank” [17].

As discussed in section 2.4.3, the LC-tank resulting from parasitic elements of the half-bridge cause oscillations at turn-on and turn-off. To damp these oscillations a damping resistor is applied across the MOSFET. In the frequency domain the voltage across the MOSFETs can be described approximately as the step response of the transfer function [17]

$$T(s) = \frac{\frac{1}{L_\sigma C_{DS}}}{s^2 + \frac{1}{R_s C_{DS}} s + \frac{1}{L_\sigma C_{DS}}}, \tag{2.23}$$

where L_σ is the stray inductance, C_{DS} is the drain-source capacitance, and R_s is a snubber-resistance in parallel with the transistor. When no dedicated resistance is introduced extensive ringing will be observed, as there is little damping in the circuit. The transfer function $T(s)$ takes the general second order form

$$T(s) = \frac{\omega_r^2}{s^2 + 2\zeta\omega_r s + \omega_r^2}, \tag{2.24}$$

where ζ is the damping coefficient and ω_r is the natural frequency in radians. The natural frequency is observed as the ringing frequency when the half-bridge MOSFETs are switched. The ringing frequency can thus be expressed in terms of the values of the circuit elements, giving

$$f_r = \frac{1}{2\pi\sqrt{L_\sigma C_{DS}}}. \tag{2.25}$$

Solving the second term of the denominator of equation (2.24) for damping, using the values in the denominator of equation (2.23), gives

$$\zeta = \frac{1}{2\omega_r R_s C_{DS}}, \tag{2.26}$$

and its clear that we now can express the resistance R_s as a function of the damping constant ζ. This will make it possible to calculate the snubber resistance. The resistance is given by

$$R_s = \frac{1}{2\zeta\omega_r C_{DS}}, \tag{2.27}$$

and assuming a desired damping constant of $\zeta = 1$, this reduces to

$$R_s = \frac{1}{4\pi f_r C_{DS}} = \frac{1}{2}\sqrt{\frac{L_\sigma}{C_{DS}}}. \tag{2.28}$$

Utilizing pure resistances across the MOSFETs to damp the oscillations will lead to unacceptable power dissipation. This can be dealt with by introducing a capacitance in series with the resistance. The capacitance will block DC and lower frequency voltage, but pass the higher frequency ringing. In addition the capacitance will help mitigate the overvoltage, as described in section 2.5.2. Hagerman [17] suggests a snubber capacitance of approximately

$$C_s = \frac{2\pi\sqrt{L_\sigma C_{DS}}}{R_s} = \frac{1}{R_s f_r}. \tag{2.29}$$

2.5.5 DC-snubbers

An alternative to the RC turn-off snubbers, which are connected across each transistor in the half-bridge, is the DC-snubber. The DC-snubber consists of an RC-series, connected in parallel with the DC-link capacitor at the input of the half-bridge. The DC-snubber works by damping the voltage ringing across the half-bridge, and should be connected as close as possible to the transistor bridge as possible. The dynamics of the damping are similar to those of the RC turn-off snubber [9], and the resistance and capacitance of the DC-snubber can therefore, with some approximation, be calculated the same way as the RC turn-off snubbers. Equation (2.27) and (2.29) could thus be used in the dimensioning of the DC-snubber as well.

Chapter 3

Description and Design of the Power Converter System

3.1 Overview of Power Converter System

A power electronic system consists of several important components. In addition to electronics designated to control and drive the power electronic switches, safety features such as voltage isolation and overcurrent protection must be included. This chapter will describe the implementation of these components, as they have been designed for this particular converter. The testing of the components are presented in chapter 4.

Figure 3.1 shows a block diagram of critical parts of this converter design. Part of this system was used in the laboratory experiments, as the double-pulse tests were performed, and the same system will be used for the full three-phase converter.

Each of the MOSFETs has a dedicated gate driver, which supplies the correct voltage levels for the switching. The gate drivers are implemented on an evaluation board, which is available from ROHM Semiconductor and fits right on top of the MOSFET modules. The evaluation board drives both the upper and lower side of each MOSFET module, and has an integrated circuit (IC) for each side. The IC isolates the primary controller side, from the secondary driver side. The driver side is powered by isolated DC/DC converters, which provides the necessary bias voltages to drive the MOSFETs.

A controller board interacts with the evaluation boards through an interface board. The interface board splits and amplifies the signals from the controller to each of the evaluation boards. One of these signals is an enable signal, and if a fault is detected by a sensor on one of the boards, the enable signal will be set to false immediately by the interface. The need to go through the slower controller board is thus eliminated.

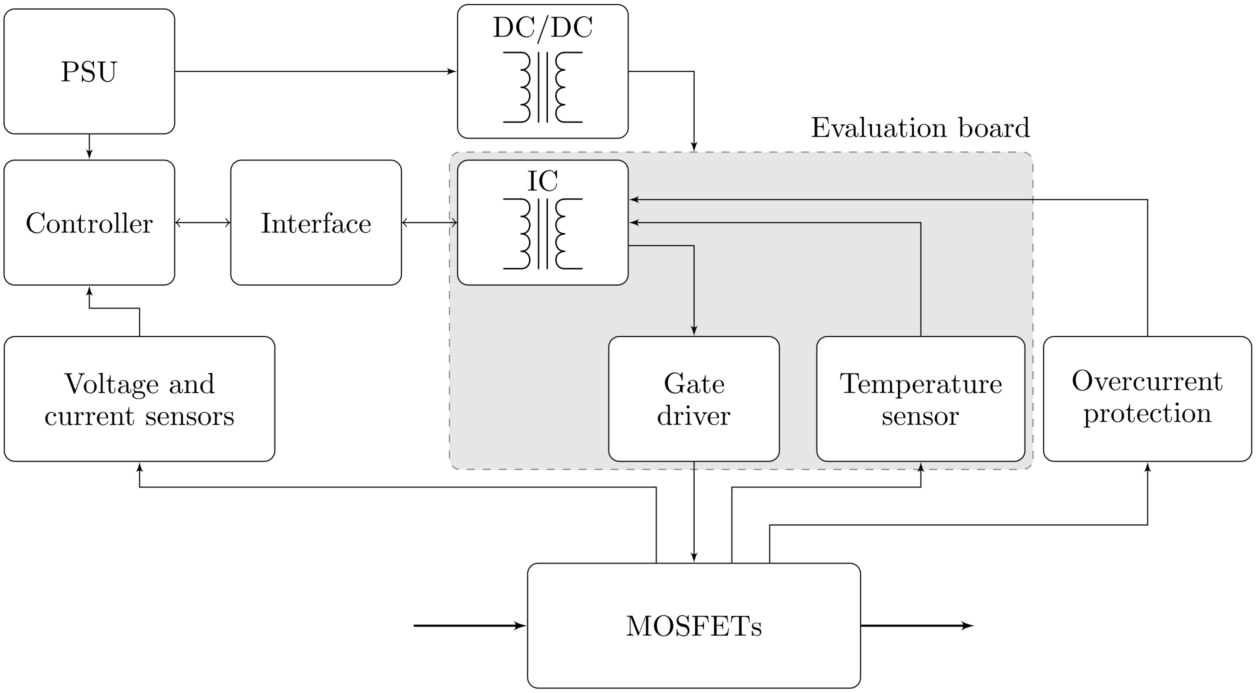
PSU
DC/DC
Evaluation board
Controller
Interface
IC
Voltage and current sensors
Gate driver
Temperature sensor
Overcurrent protection
MOSFETs

Figure 3.1: Control flow of converter system

The IC on the evaluation board features inputs to detect if the current or temperature is too high. A temperature sensor is implemented on the evaluation board, which interacts with the thermistor integrated in the MOSFET module. Circuitry to detect overcurrent is not included however, so this must be implemented outside the evaluation board.

A so called piggyback board was designed, to fit on top of the evaluation board. This board implemented the overcurrent protection, as well as the DC/DC voltage supply for the evaluation board. In addition the RC-snubbers for each of the MOSFETs in the half-bridge were included in the piggyback design.

3.2 SiC MOSFET modules

The converter system design aimed to use the SiC power module BSM300D12P3E005, from ROHM Semiconductor [23]. This module consists of two SiC MOSFETs in half-bridge configuration, where each of the MOSFETs has a SiC Schottky diode connected in anti-parallel. The BSM300D12P3E005 module is rated for a current of 300 A, and a voltage of 1200 V. This module will be referred to as the 300 A-module in the following.

3.2.1 Rated Operation of the Converter

The system was designed to output a three phase line-to-line RMS voltage of 400 V. A 400 V sinusoidal voltage will have an amplitude of $\sqrt{2} \cdot 400\,\mathrm{V} = 566\,\mathrm{V}$, and using pulse width modulation, 600 V is commonly chosen as the DC-link voltage. Since the BSM300D12P3E005 module has a 300 A current rating, the nominal RMS output current was chosen to be 150 A. This gives a current amplitude of $\sqrt{2} \cdot 150\,\mathrm{A} = 212\,\mathrm{A}$, which is well within the rated limits of the module.

The total power P of a balanced three phase system is given by

$$P = 3\frac{V_L}{\sqrt{3}} I_L \cos\phi = \sqrt{3} V_L I_L \cos\phi, \tag{3.1}$$

where V_L is the line-to-line RMS voltage, I_L is the RMS current and $\cos\phi$ is the power factor. Assuming a power factor of 0.9, common for nominal operation of induction motors, the achievable power rating with the chosen MOSFET modules can be calculated:

$$P = \sqrt{3} \cdot 400\,\mathrm{V} \cdot 150\,\mathrm{A} \cdot 0.9 = 94\,\mathrm{kW}. \tag{3.2}$$

The RMS current of 150 A will be used in the following in the double-pulse tests, to investigate the performance of the MOSFET modules.

3.2.2 Theoretical Loss Calculations

Theoretical losses for the power converter can be calculated using datasheet values. This will serve as a basis for dimensioning the heat sink which the MOSFET modules will be placed on. Relevant characteristics of the MOSFET module, found in the datasheet, are listed in table 3.1. This will be used for the theoretical loss calculations presented in the following.

Table 3.1: Various physical characteristics of MOSFET module [23].

Description	Symbol	Value
Threshold voltage diode	$V_{F,D}$	0.7 V
Turn-on resistance diode	R_F	11.7 mΩ
Turn-on resistance transistor	$R_{DS,On}$	8.0 mΩ
Turn-off energy transistor	$E_{Off,T}$	4 mJ
Turn-on energy transistor	$E_{On,T}$	6.8 mJ
Turn-off energy diode	$E_{Off,D}$	1.4 mJ

Conduction Losses

The conduction losses in the transistor of a pulse width modulated inverter can be derived analytically to be given by the following equation [28], [29]:

$$P_{T,con} = \frac{V_{F,T}\hat{I}_L}{2}\left(\frac{1}{\pi} + \frac{M}{4}\cos\phi\right) + R_{DS,On}\hat{I}_L^2\left(\frac{1}{8} + \frac{M}{3\pi}\cos\phi\right), \tag{3.3}$$

where $V_{F,T}$ is the threshold voltage of the transistor, M is the modulation depth and $\cos\phi$ is the power factor of the output from the inverter. $\hat{I}_L$ is the amplitude of the fundamental frequency of the load current. The rest of the variables are described in table 3.1. The transistors used are MOSFETs, which are bipolar devices. Such devices does not have a threshold voltage at turn-on, and the first term of the above equation is therefore zero. The equation for the conduction loss of the MOSFET thus reduces to

$$P_{T,con} = R_{DS,On}\hat{I}_L^2\left(\frac{1}{8} + \frac{M}{3\pi}\cos\phi\right). \tag{3.4}$$

In a similar manner as for the transistors of the PWM inverter, the conduction losses of the diodes can be derived to be [28], [29]:

$$P_{D,con} = \frac{V_{F,D}\hat{I}_L}{2}\left(\frac{1}{\pi} - \frac{M}{4}\cos\phi\right) + R_F\hat{I}_L^2\left(\frac{1}{8} - \frac{M}{3\pi}\cos\phi\right). \tag{3.5}$$

The modulation depth M is assumed to be 1. As in section 3.2.1, a power factor of 0.9 is used, which is reasonable considering the nominal operation of an induction motor. It is assumed that the inverter is operated at the rated level presented in 3.2.1, so the amplitude of the fundamental of the load current will be 212 A. Evaluating the above expressions using the values from table 3.1, gives the conduction loss of the transistor and diode below:

$$P_{T,con} = 79\,W, \;\; P_{D,con} = 22W. \tag{3.6}$$

Switching Losses

The switching losses $E_{T,On}$ and $E_{T,Off}$ of the MOSFETs, and the turn-off switching losses in the diodes $E_{D,Off}$, can be found in the datasheet [23]. Using these datasheet values, the averaged switching power loss for one MOSFET half bridge is given by [29]

$$P_{T,sw} = \frac{1}{\pi} f_{sw}(E_{T,On} + E_{T,Off}), \tag{3.7}$$

and the power loss caused by the anti-parallel diodes switching is given by

$$P_{D,sw} = \frac{1}{\pi} f_{sw} E_{D,Off}. \tag{3.8}$$

If datasheet values were measured under different conditions than the ones considered here, the scaling below can be used [29]:

$$P_{sw} = \frac{1}{\pi} f_{sw} (E_{T,On} + E_{T,Off} + E_{D,Off}) \cdot \frac{V_{DC} \cdot \hat{I}_L}{V_{ref} \cdot \hat{I}_{ref}}, \tag{3.9}$$

where V_{DC} is the DC-link voltage, and $\hat{I}_L$ is the amplitude of the fundamental frequency of the load current. V_{ref} and $\hat{I}_{ref}$ are the datasheet measurement conditions. The conditions are the same as for the datasheet however, so the values of table 3.1 can be used without scaling. This yields the below switching powers for the transistor and diode, for a switching frequency of 50 kHz:

$$P_{T,sw} = 172W, \;\; P_{D,sw} = 22W. \tag{3.10}$$

3.3 Snubbers

It is desirable to implement snubber circuits to reduce the voltage overshoot and ringing occurring in the MOSFET switching transitions. As discussed in section 2.5.3 in the theory, RC-snubbers are suitable when the main concern is to reduce EMI effects. While more complex snubber circuits could be used to improve the overall performance, it is desirable to keep the design simple in the initial design iteration, to better understand the impact of component values on the characteristics of the converter operation.

The RC-snubbers for the half-bridge configuration is implemented by connecting an RC-series in parallel with each of the MOSFETs in the half-bridge. Since the tests to be performed in the laboratory would involve experimenting with several different snubbers, it was decided to implement the RC-snubbers on the piggyback board. This enables easier soldering of the resistors and capacitors, and assembly with the rest of the experimental setup.

The placement of the RC turn-off snubbers on the piggyback board is described in section 3.4.2, where the electrical clearance of the snubber circuitry is discussed.

3.4 Gate Driver

3.4.1 Overview

It was initially planned to use the gate driver board designed in the project work leading up this Master thesis [1]. However, due to delays in the production of this board, the BP59A8H gate driver evaluation board from ROHM [19] was used as a basis for the converter system design instead. The custom gate driver design was based on this evaluation board, and thus only minor adjustments in the setup had to be made. The BP59A8H evaluation board does not include circuitry to detect overcurrents, so this had to be implemented. Additionally the voltage supply to the secondary side of the board should be isolated. These features were implemented on a second piggyback board, which could mount on top of the evaluation board. The RC-snubbers were also included on the piggyback board. The full design of the piggyback board will be presented in the following.

3.4.2 Piggyback Board

Figure 3.2 shows the implementation of the piggyback board in EAGLE. The connection to the gate driver evaluation board is made through the header JP1. Six of the connections from the JP1 header are forwarded to a new set of header pins, JP2, where the interface from the interface board should be connected. These pins provide a direct connection between the interface board and the gate driver, transferring switching and fault signals. A more through description of the functions of these signals is provided in section 3.5.

DC/DC-converters

For safety reasons the secondary side voltage supply to the gate driver should be isolated. This can be achieved through isolated DC/DC converters. The bias voltages, used for the gate voltage of the MOSFETs, are specified in the datasheet of the gate driver evaluation board [19]. According to the datasheet, these voltages should be 18 V and -3 V.

A common voltage input is used to supply the DC/DC-converters. The voltage input is parallel connected to a capacitor ensuring a stable voltage input, and a Zener diode to prevent overvoltages from damaging the DC/DC-converters. The DC/DC-converters R12P212D and R12P205S from Recom were chosen for the application. These converters have an isolation voltage of 6.4 kV, as well as a very low isolation capacitance [21]. The R12P212D converter provides a dual output of 12/-12 V, and the R12P205S a single output of 5 V. To achieve a -3 V voltage in the output, the single output DC/DC converter should have an output of 3 V, however this model was not in supply when the piggyback board was produced. It

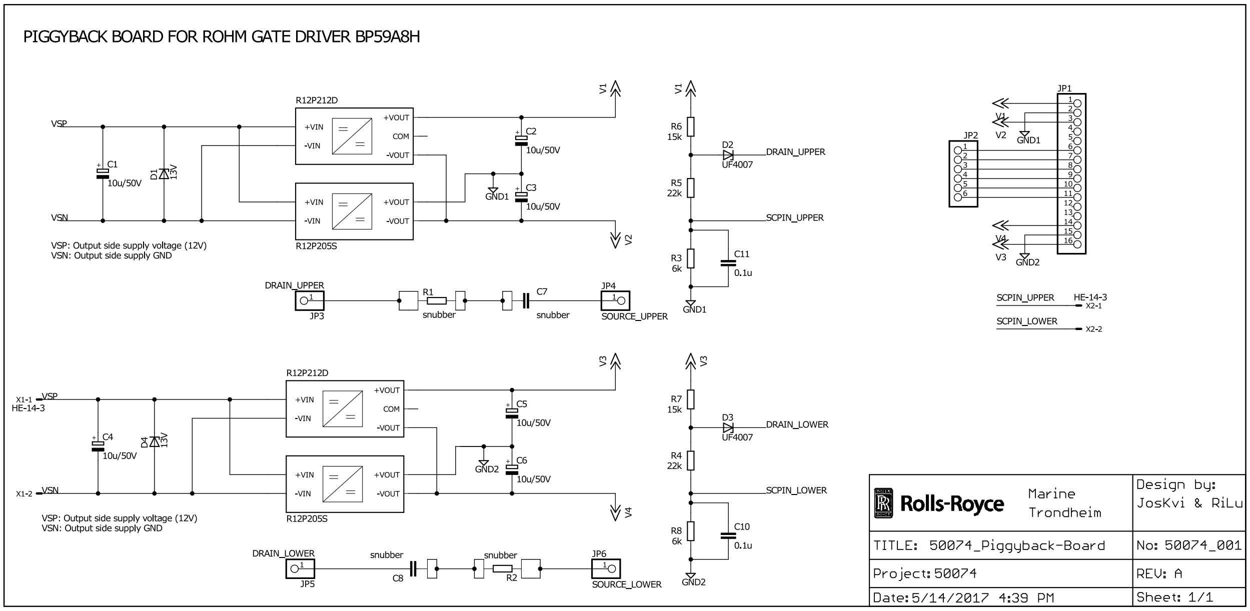
PIGGYBACK BOARD FOR ROHM GATE DRIVER BP59A8H
R12P212D
R12P205S
+VIN
-VIN
+VOUT
COM
-VOUT
VSP
VSN
C1 10u/50V
D1 13V
C2 10u/50V
C3 10u/50V
GND1
V1
V2
VSP: Output side supply voltage (12V)
VSN: Output side supply GND
R6 15k
R5 22k
R3 6k
D2 UF4007
DRAIN_UPPER
SCPIN_UPPER
C11 0.1u
DRAIN_UPPER
JP3
R1 snubber
C7 snubber
JP4 SOURCE_UPPER
JP1
JP2
GND2
V3
V4
SCPIN_UPPER HE-14-3 X2-1
SCPIN_LOWER X2-2
X1-1 HE-14-3
X1-2
C4 10u/50V
D4 13V
C5 10u/50V
C6 10u/50V
R7 15k
R4 22k
R8 6k
D3 UF4007
DRAIN_LOWER
SCPIN_LOWER
C10 0.1u
DRAIN_LOWER
JP5
C8 snubber
R2 snubber
JP6 SOURCE_LOWER
Rolls-Royce
Marine Trondheim
Design by: JosKvi & RiLu
TITLE: 50074_Piggyback-Board
No: 50074_001
Project: 50074
REV: A
Date: 5/14/2017 4:39 PM
Sheet: 1/1

Figure 3.2: EAGLE schematic of the piggyback board.

was therefore decided to use a Zener diode voltage regulator to down-regulate 5 V to 3 V. A thorough description on how this can be achieved is provided in appendix B.

By connecting the negative outputs of the DC/DC-converters, and using the 5 V output of the R12P205S converter as GND, two voltage supplies with the voltages 19 V and -5 V can be obtained. This arrangement can be seen in figure 3.3.

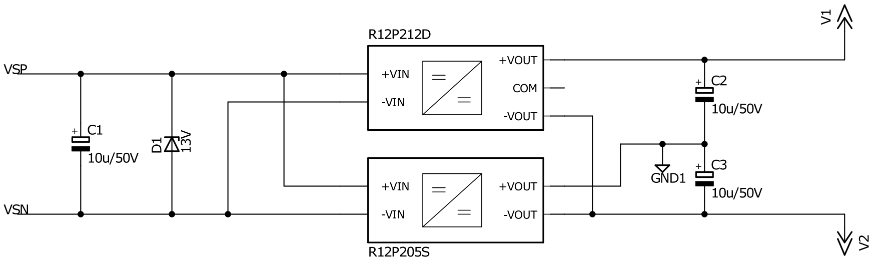
R12P212D
R12P205S
VSP
VSN
+VIN
-VIN
+VOUT
COM
-VOUT
C1 10u/50V
D1 13V
C2 10u/50V
C3 10u/50V
GND1
V1
V2

Figure 3.3: Circuit diagram of the DC/DC-converters.

Capacitors are connected across the output voltages as well, again to ensure a stable voltage. The zener diode voltage regulator was added between the 5 V capacitor and the output to the gate driver, after the piggyback board was produced. The final output voltages are fed directly to the evaluation board, through the JP1 header.

Overcurrent Protection

An identical overcurrent protection circuit as the one implemented on the piggyback board was presented in the report of the project work leading up to this Master thesis [1], where the same overcurrent protection was implemented in a complete gate driver board. The following section is an excerpt from the project report, repeated here for completeness.

The IC of the gate driver has a short current detection pin, SCPIN. If a voltage above the threshold level of 0.74 V is detected at this pin, the IC sends a shutdown signal to the MOSFET it is driving [20]. A fault signal is sent to the input side as well, so the controller can make sure the other MOSFETs also shuts down.

A short current through the MOSFET can be detected by measuring the drain-source voltage V_{DS}, as this voltage will vary linearly with the drain-current. Using voltage division to scale the drain-source voltage, will then make sure the SCPIN voltage reaches the threshold level at a certain drain-current [2]. The datasheet of the IC [20] shows how the circuit could be implemented, and a diagram of this circuit is shown in figure 3.4. The diode D is used to block current when the MOSFET is in the off-state. In the on-state, the SCPIN voltage is given by [20]

$$V_{SCPIN} = \frac{R_3}{R_2 + R_3}(V_{FD} + V_{DS}), \tag{3.11}$$

where V_{FD} is the forward voltage of the diode. The diode needs to have fast recovery, and block voltages above 600 V, so the ultrafast power diode AU1PM-M3 from Vishay was used [24]. This diode is able to block up to 1000 V, and has a forward voltage of 1.85 V. The 300 A-module has a drain-source resistance of 5 mΩ [23], so for a current of say 320 A, by Ohms's law the drain-source voltage V_{DS} will be 1.6 V. The resistances in figure 3.4 should be chosen so that V_{SCPIN} is 0.74 V at this drain-source voltage and from equation (3.11) we get that this can be achieved with the resistances $R_2 = 22\,\text{k}\Omega$ and $R_3 = 6\,\text{k}\Omega$.

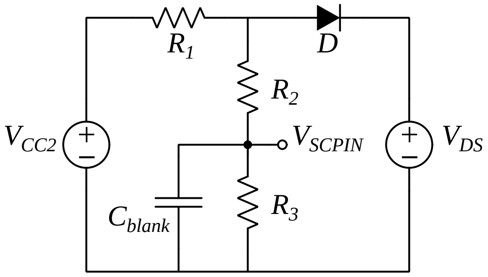

Figure 3.4: Overcurrent protection equivalent circuit.

For the voltage V_{SCPIN} to be able to reach the threshold voltage, the following must hold [20]:

$$V_{CC2} > 0.74V \cdot \frac{R_1 + R_2 + R_3}{R_3}. \tag{3.12}$$

R_1 was therefore chosen to 20 kΩ. The blanking capacitor C_{blank} determines the blanking time t_{blank}, i.e. how fast the circuit will reach the threshold voltage. For a larger capacitance, the voltage V_{SCPIN} use longer time to build up, thus giving a longer blanking time. A blanking capacitor of 0.1 μF was chosen, as this have previously been shown to yield good results [2]. The implementation of the overcurrent protection in EAGLE, with the chosen values, is shown in figure 3.5.

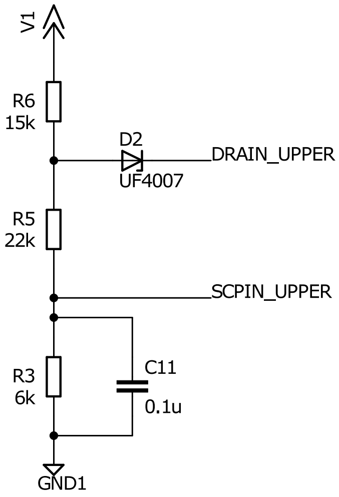

Figure 3.5: Overcurrent protection EAGLE implementation.

Layout of the Piggyback Board

Because the RC turn-off snubbers will be connected to the drain and source of the MOSFETs, the voltage potential of the traces connecting the snubber components must be considered. To determine the electrical clearance between the RC turn-off snubber circuitry and the rest of the piggyback board, the voltage across the snubber components were determined through simulations in LTspice, using a simulation model of the 300 A-module provided by ROHM. The simulation methodology was identical to that presented in section 5.2. By simulating the hard-switching of the 300 A-module at 150 A, it was found that the maximum voltage across the snubber capacitor would be 700 V, and the maximum voltage across the RC series with respect to GND would be 722 V. Based on the IPC-2221 standard [25], presented in appendix C, the clearance from the traces of the RC-snubber to the rest of the piggyback board traces should be $722\text{V} \cdot 0.005$ mm/V $= 3.6$ mm.

The EAGLE layout of the piggyback board is shown in figure 3.6. The red is the copper traces on top of the board, and the blue is the bottom side copper traces. Larger copper fill areas were made for the ground traces, to improve ground connection and reduce EMI effects.

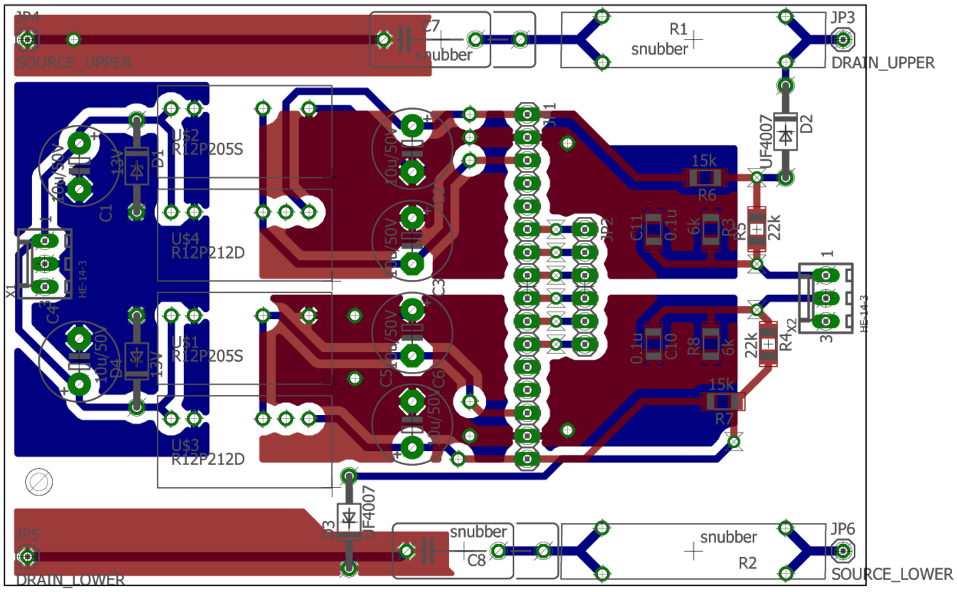
JP4
SOURCE_UPPER
C7
snubber
R1
snubber
JP3
DRAIN_UPPER
U$2
R12P205S
D1
13V
10u/50V
C1
10u/50V
C2
UF4007
D2
JP1
15k
R6
C11
0.1u
6k
R3
R5
22k
JP2
U$4
R12P212D
10u/50V
C3
X1
1
3
C4
HE-14-3
1
3
X2
HE-14-3
U$1
R12P205S
10u/50V
D4
13V
10u/50V
C5
C6
10u/50V
0.1u
C10
R8
6k
22k
R4
15k
R7
U$3
R12P212D
D3
UF4007
JP5
DRAIN_LOWER
snubber
C8
snubber
R2
JP6
SOURCE_LOWER

Figure 3.6: EAGLE layout of the piggyback board.

The finished production of the piggyback board can be seen in figure 3.7. The Zener diode voltage regulation was implemented on the bottom of the board, and can be seen on the left side of the 16 bit header connection to the gate driver.

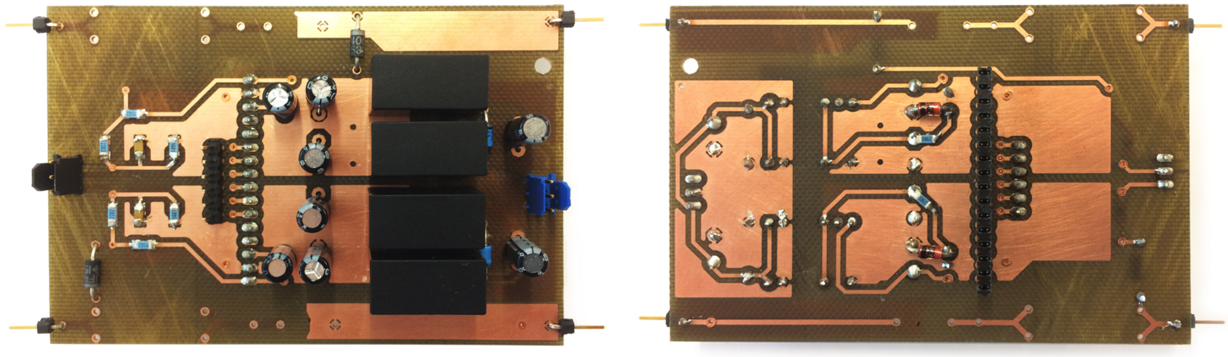

Figure 3.7: Piggyback board.

3.5 Control

A controller developed by Rolls-Royce Marine was used in the laboratory experiments. The controller can take voltage and current sensor inputs, and act as a full motor drive controller. Additionally, the controller has special software to be used to perform double-pulse tests.

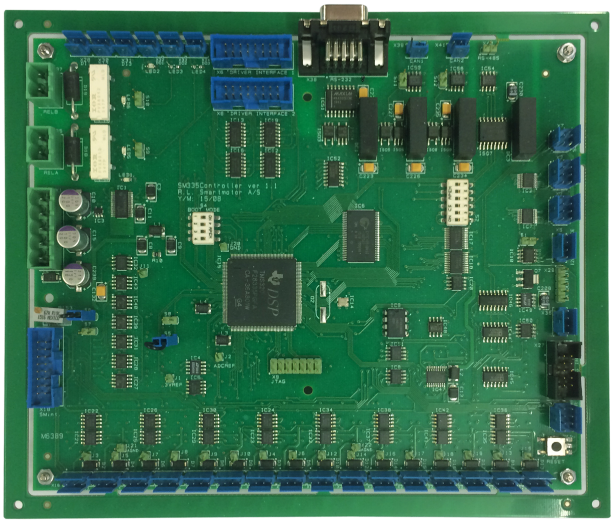

Figure 3.8: Controller board.

The controller has a 16 bit interface for communication with the three gate drivers of the converter. To split this signal, an interface board was implemented. The interface board should distribute the PWM gate signals to each of the drivers, and block these signals if a fault occurs. The schematic of the interface board is shown in figure 3.9.

A description of the information carrying bits in the interface from the controller is presented in table 3.2. The controller outputs a gate signal for each of the upper and lower MOSFETs in the three phases. These signals are sent through MCP14E4-EP MOSFET drivers on the interface board. The controller also outputs an enable signal named ONIN. The EN signal sent to the enable gates of the MOSFET drivers, is created by ANDing the ONIN signal from the controller and the OK signal from the drivers. This ensures that all of the MOSFET gates goes low immediately, if a fault is detected by either the controller or one of the drivers. The AND operation is created by using two NAND gates. The NAND gates have Schmitt triggers, to make sure noise does not accidentally create disturbances in the signals.

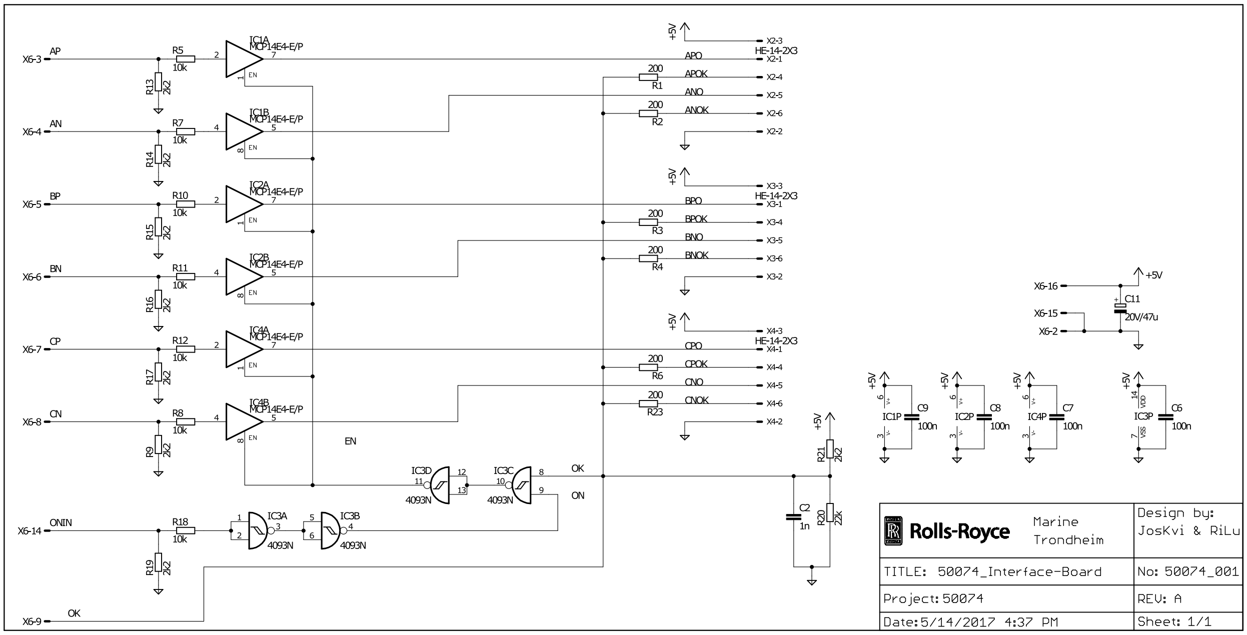
X6-3
AP
R5
10k
R13
2k2
IC1A
MCP14E4-E/P
X6-4
AN
R7
R14
IC1B
X6-5
BP
R10
R15
IC2A
X6-6
BN
R11
R16
IC2B
X6-7
CP
R12
R17
IC4A
X6-8
CN
R8
R9
IC4B
EN
X6-14
ONIN
R18
R19
IC3A
IC3B
4093N
IC3D
IC3C
OK
ON
X6-9
+5V
APO
APOK
ANO
ANOK
R1
R2
200
HE-14-2X3
X2-1
X2-2
X2-3
X2-4
X2-5
X2-6
BPO
BPOK
BNO
BNOK
R3
R4
X3-1
X3-2
X3-3
X3-4
X3-5
X3-6
CPO
CPOK
CNO
CNOK
R6
R23
X4-1
X4-2
X4-3
X4-4
X4-5
X4-6
R21
R20
22k
C1
1n
X6-16
X6-15
X6-2
C11
20V/47u
IC1P
C9
IC2P
C8
IC4P
C7
IC3P
C6
100n
VDD
VSS
Rolls-Royce
Marine
Trondheim
Design by:
JosKvi & RiLu
TITLE: 50074_Interface-Board
No: 50074_001
Project: 50074
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Figure 3.9: EAGLE schematic of the interface board.

Table 3.2: Controller/interface connector

AP	Gate signal upper, phase A
AN	Gate signal lower, phase A
BP	Gate signal upper, phase B
BN	Gate signal lower, phase B
CP	Gate signal upper, phase C
CN	Gate signal lower, phase C
ONIN	Enable signal from controller
OK	OK signal from driver

The connection between the interface board and the gate driver of phase A is described in table 3.3. The connections to the two other phases are equal. The APO and ANO are the gate signals for the upper and lower MOSFETs. Each of the drivers outputs an ok signal for the upper and lower MOSFETs they are controlling, APOK and ANOK respectively for phase A, which go low if the drivers detect a fault. These signals are connected, giving the common OK signal which gets ANDed with the ON signal. The OK signal goes low if any of the gate drivers detect a fault for either the upper or lower MOSFET in the half bridges.

Table 3.3: Interface/driver connector phase A

APO	Gate signal upper
APOK	OK signal lower
ANO	Gate signal lower
ANOK	OK signal upper

As can be seen in the schematic in figure 3.9, the controller supplies a 5 V voltage. This is used to power the logic gates and the amplifiers. Capacitors are placed parallel to the voltage supply close to the packages to ensure a stable voltage. The 5 V voltage supply is also forwarded to the drivers, to power the primary side logic of the evaluation boards.

The layout of the components of the interface board was designed using EAGLE, and then soldered on a prototype board. The layout is shown in figure 3.10, and the finished soldered prototype board can be seen in figure 3.11. The bill of materials for the interface board is listed in appendix A.

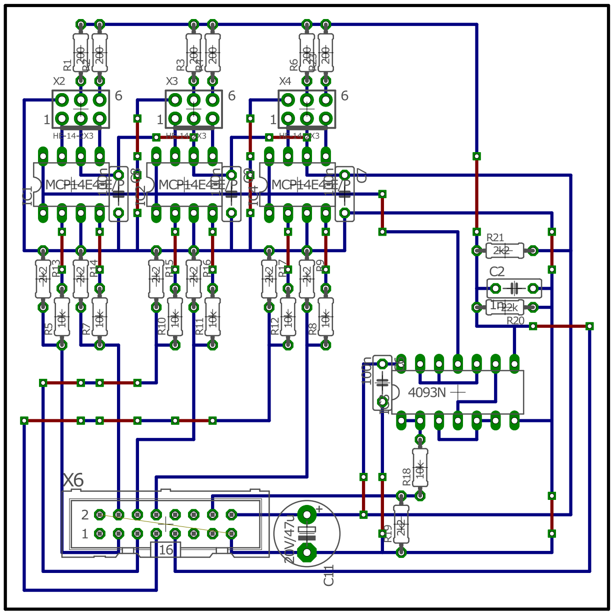

R1
R2
R3
R4
R6
200
X2
X3
X4
6
1
MCP14E4E/P
IC1
R13
R14
R15
R16
R17
R5
R7
R10
R11
R12
R8
R9
2k2
10k
R21
C2
1n
22k
R20
4093N
100n
R18
R19
X6
2
1
16
25V/47u
C11

Figure 3.10: Layout of the interface board.

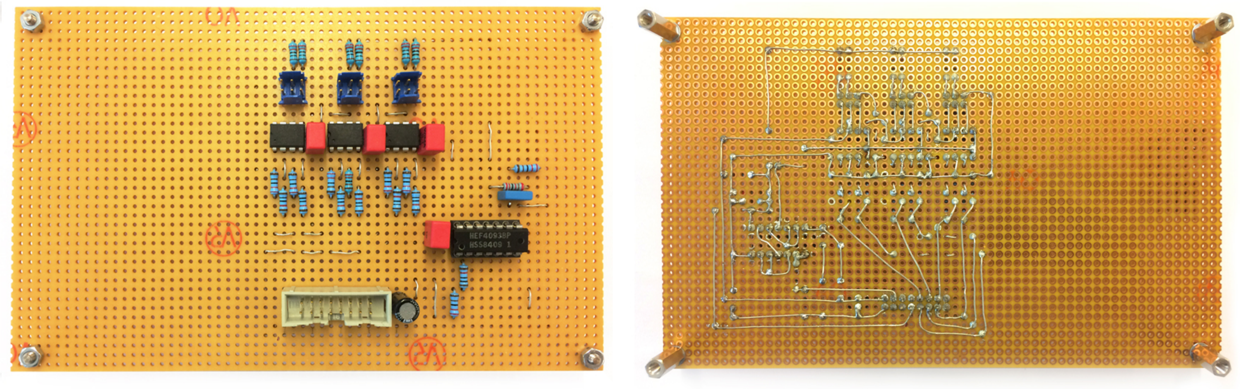


Figure 3.11: Prototype board implementation of the interface board.

3.6 DC-Bus Design

A DC-bus bar was designed to work as a common DC-link for the three half-bridges in the converter. As described in 2.4.3, the stray inductance of the design is an important concern. Minimizing the stray inductance is important to reduce EMI effects and voltage overshoots in the switching waveforms, and thus achieving a good switching performance. A planar bus bar design, where the positive and negative poles are plates with a thin insulation layer between them, minimizing the distance between the conductors, can be used to achieve a low inductive design [11].

The bus bar was made by using two copper plates as positive and negative terminals, with an insulation layer between the terminals. Lexan was chosen as the insulation material for the design. Lexan is a polycarbonate with good insulation and thermal capabilities [26]. The insulation layer should be kept thin, as this will increase the stray inductance. Lexan has an electrical breakdown strength of about 67 kV/mm, and a insulation layer thickness of 1 mm was chosen, given more than sufficient breakdown margin.

3.6.1 Choice of DC-Bus Capacitors

The DC-bus should supply a stable current at a near constant voltage to the full-bridge converter. Three WIMA MKP6 DC-link capacitors, each with a capacitance of 550 μF, were chosen. These capacitors have a voltage rating of 700 V, and are well suited to carry the total RMS current of 150 A per phase.

Due to large ESR in large bulk capacitors, they have limited effect on the ripple voltage created when the converter switches. To mitigate ripple voltage, low ESR ceramic input capacitors can be used, placed directly over the input terminals to the half-bridge modules [27].

3.6.2 Stray Inductance Considerations

The most important parameter to minimize EMI effects, and achieve a high EMC performance [11], is the stray inductance in the converter. Reducing the stray inductance of the bus bar leads to lower voltage ringing and overshoot in the switching transitions. This is of particular importance in SiC applications, as higher switching frequencies at faster switching speeds can be applied.

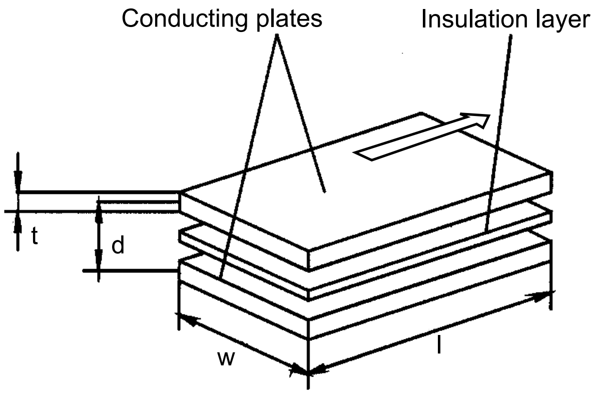


Figure 3.12: Planar bus bar illustration [11].

A planar bus bar design is illustrated in figure 3.12. The big arrow on the top defines the direction of current flow. The inductance of this bus bar can be described as the sum of its internal and external inductance, L_i and L_e. An approximate expression for the sum of these inductances is [11]

$$L = L_i + L_e = \frac{\mu_0 \mu_r}{8\pi} \cdot l + 2\mu_0 \mu_r \cdot \frac{t \cdot l}{\pi(t+w)}, \tag{3.13}$$

where μ_0 is the permeability in vacuum and μ_r is the relative permeability of the insulation material between the conduction plates. From equation 3.13 it is clear that the insulation thickness should be as small as possible, and the conduction path should preferably be wide, to reduce the stray inductance. The other dimensions should also be kept small, however these are constrained by other design factors to a larger extent.

At the terminals to the MOSFET modules, the plates are no longer in a planar arrangement. This can be seen in figure 3.13, where the terminals that would be connected to the MOSFET module are shown on the right side.

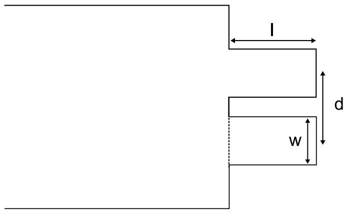


Figure 3.13: Illustration of DC-bus bar termination.

An approximation of the inductance for the conductors at the terminals is [12]

$$L = \frac{\mu_0 \mu_r}{\pi} \left(l \cdot \ln(\frac{2d - w}{w}) + d \cdot \ln(\frac{2l - w}{w}) \right). \tag{3.14}$$

Typically the inductance of the terminals of the DC-bus contributes a lot to the total inductance of the bus bar, length d should be kept low. Lumping the inductances in equation 3.13 and 3.14 together gives a theoretical approximation for the stray inductance from the bus bar, however other effects must be factored in. Nuts and bolts in the bus bar, and the terminals between the capacitors, adds increased inductance. Additionally the MOSFET modules have an internal stray inductance, adding to the total stray inductance.

3.6.3 Current Density Calculations

Determining the dimensioning current density of the design is complex, as the value depends on heat transportation capabilities, maximum allowable temperature and allowable voltage drop across the conductor. The IPC-2221 standard [25] provides curves to determine the appropriate copper area for a given current and temperature rise relative to the ambient temperature. Applying a curve fitting to the curves provided in the IPC-2221 standard yields the following equation:

$$A = a \cdot \left(\frac{I_L}{k \cdot \Delta T^b} \right)^{1/c}, \tag{3.15}$$

where A is the cross section area of the copper conductor, I_L is the RMS value of the load current and ΔT is the temperature difference between the copper and the ambient. The constants can be obtained from the curve fitting, which gives that $k = 0.048$, $b = 0.44$ and $c = 0.725$. The areas of the curves are given in square mils, which are scaled to square millimeters by the factor $a = 6.4516 \cdot 10^{-4}$. It should be noted that the curves in the IPC-2221 standard are only plotted for cross sections areas below $0.45\,\mathrm{mm}^2$ and currents below 35

A, but equation 3.15 can be used to extrapolate those curves for the application considered here. This likely introduces some inaccuracies however.

The allowed temperature rise above the ambient is chosen to be 10 °C, and we know that the load current I_L should be 150 A. Equation 3.15 gives that the cross section area of the conductor should be more than $10.6\,\mathrm{mm}^2$. This is equivalent to a maximum current density of 14.2 A/mm^2, and in accordance with the advice of using a dimensioning current density of 10 A/mm^2 given by engineers at Rolls-Royce Marine.

The width of the smallest conduction paths will be dimensioning for the thickness of the copper plates, which are at the terminals connecting to the MOSFET modules. This can be seen in figure 3.14. Here the width is 12.5 mm. Using the calculated cross section area gives a minimum copper plate thickness of 0.84 mm. The copper plates that were used when the DC-bus bar was produced 1.44 mm, giving some margin to allow for errors in the calculations.

3.6.4 DC-bus Layout and Final Design

A sketch of the DC-bus layout is shown in figure 3.14. The red area is the top copper plate, which is the negative pole of the DC-link voltage. The bottom plate, with the opposite polarity, has a similar shape, but terminates at the other terminals on top of the DC-bus.

The distance between the capacitors and the MOSFET terminals was kept as the short as the capacitor diameter and MOSFET placement on the heat sink would allow. This was done to reduce stray inductance, and keep the volume of the design at a minimum. The distance between the terminals causes the stray inductance of the conductors to increase at the termination, as discussed in section 3.6.2.

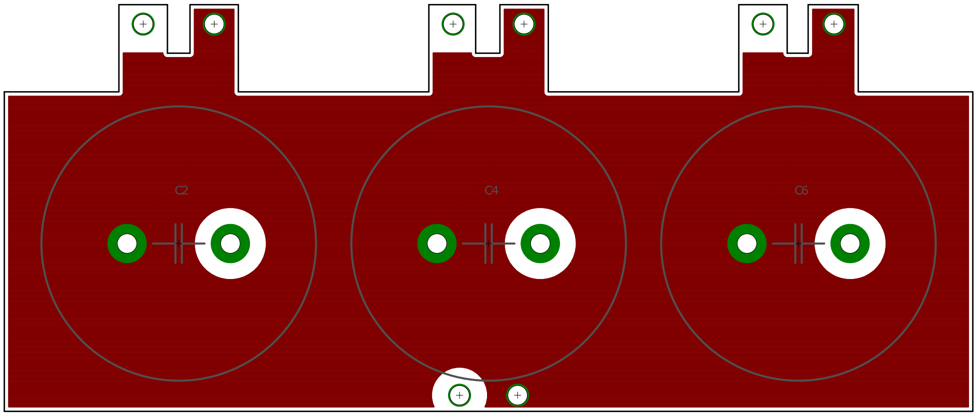


Figure 3.14: Outline of DC-bus.

According to the IPC-2221 standard, shown in appendix C, the electrical clearance should be $600\text{V} \cdot 0.005\text{V/mm} = 3$ mm. Based on this, the DC-bus was designed with an electrical clearance of 5 mm, to allow for inaccuracies in production and provide some operational safety margin. The electrical clearance can be seen in figure 3.14, for example at the right terminal of the capacitors, where the white space indicates an isolated area between the poles.

The assembled DC-bus, with mounted capacitors, can be seen in figure 3.15. A bleed resistor was mounted over one of the capacitor, to decrease capacitor discharge time when the voltage supply to the DC-bus is turned off. This is a feature included to increase safety when experimenting with the DC-bus in the laboratory under high voltage.

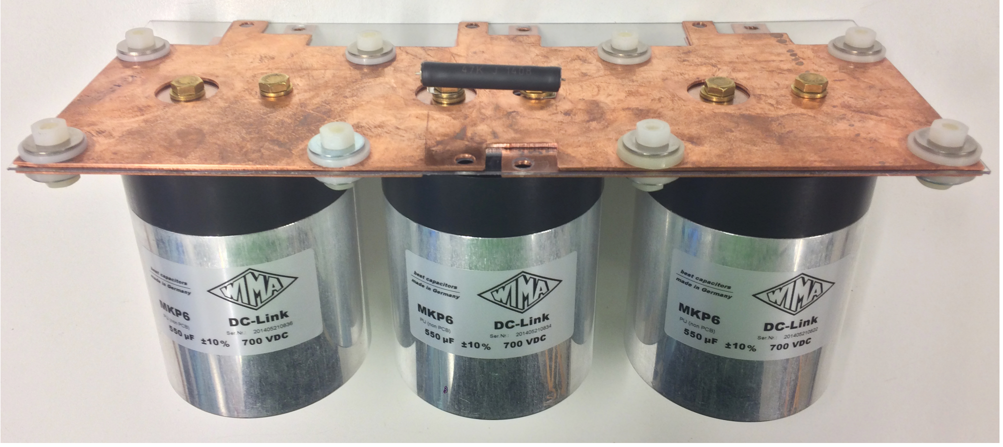

WIMA
MKP6
DC-Link
550 µF ±10% 700 VDC
WIMA
MKP6
DC-Link
550 µF ±10% 700 VDC
WIMA
MKP6
DC-Link
550 µF ±10% 700 VDC

Figure 3.15: DC-bus with capacitors mounted.

Chapter 4

Description of Laboratory Setup and Preliminary Component Tests

4.1 Introduction

This chapter describes the laboratory setup that was used to conduct SiC MOSFET module experiments. The double-pulse test that was used to investigate the MOSFET module performance is described in detail, and the individual parts of the laboratory test setup is presented. The results from a single double-pulse test was used to calculate the stray inductance of the DC-bus that was used, and this will serve as a basis for the parameter choices used in the simulations presented in chapter 5.

It was not possible to conduct the laboratory experiments with the 300 A-module that the system design presented in the last chapter was based on. This was due to delays in shipping from the manufacturer. A laboratory setup, using the BSM120D12P2C005 SiC MOSFET half-bridge module from ROHM, was therefore used. This module has a rated current of 120 A and a rating voltage of 1200 V [30]. The BSM120D12P2C005 module will be referred to as the 120 A-module in the following. The 120 A-module module was used in a previous Master thesis [2], and the experimental setup from that project included a DC-bus fitted for the 120 A-module, as well as a gate driver evaluation board from ROHM with similar capabilities as the one presented in the previous chapter. The control and interface board that were presented in the previous chapter where used to conduct the experiments with this laboratory setup.

In addition to calculating the DC-bus stray inductance using the results from a double-pulse test, impedance measurements were performed on both the 120 A-module DC-bus and the three phase converter DC-bus presented in the previous chapter. The results form the impedance measurements were used to calculate the stray inductance of the DC-bus used in the experiments with the 120 A-module. The inductance value was then compared with the stray inductance calculated in the double-pulse test. Further, the stray inductances of the two DC-buses were compared. A description of the impedance tests, and the results from these tests, is presented at the end of the chapter.

4.2 Laboratory Setup

4.2.1 Double-Pulse Test

When the SiC MOSFET module is used in a PWM controlled three phase inverter, the MOSFETs are hard switched. This was discussed in more depth in section 2.4.3. To emulate the conditions under hard switching, a so called double-pulse test can be used. In a double-pulse test, two consecutive turn-on signals are sent to one of the MOSFETs in the half-bridge, while the other MOSFET is turned off. The MOSFET being fed the two pulses will be hard-switched, and is thus the device under testing (DUT).

A circuit schematic showing the main components of the test circuit is shown in figure 4.1. The half-bridge is the 120 A-module, and an inductor coil L_{load} is connected between the drain and source terminals of the upper MOSFET. A voltage source is connected between the input terminals of the module, i.e. the drain terminal of the upper MOSFET and the source terminal of the lower MOSFET. A bulk capacitor is connected in parallel with the voltage source, to ensure a stable voltage during the test.

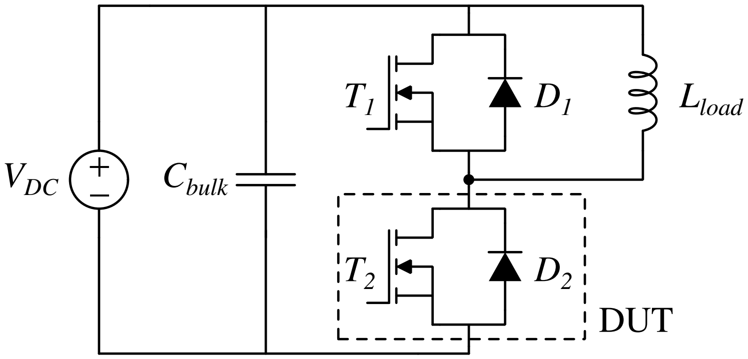


Figure 4.1: Principal circuit for double-pulse testing.

When the first turn-on signal is sent to the lower MOSFET, the full input voltage V_{DC} will be laying over the inductor L_{load}, and the current through the inductor and the DUT will rise according to

$$\Delta I = \frac{V_{DC}\Delta t}{L_{load}}, \tag{4.1}$$

where Δt is the length of the first pulse. The length of the first pulse will therefore determine the current under which the hard switching occur. As the current reaches this level, the DUT is turned off, and the characteristics of the DUTs turn-off interval can be measured. Then a second turn-on signal is sent to the DUT, so the turn-on characteristics can be measured. The inductor coil should be large enough so that the current does not decrease significantly when the DUT is turned off, and the current is freewheeling through the upper diode D_1. A load inductor with an inductance of 250 μH had been proved to behave satisfactory with the same laboratory setup [2], and was used here as well.

4.2.2 Overview of Laboratory Test Setup

The double-pulse tests were performed using the setup shown in figure 4.2. The DC-bus is connected to the MOSFET module left in the picture, and the MOSFET module is placed on top of a small heat sink. In each test variation, only a single double-pulse was sent, so no significant power was dissipated in the module. The inductor coil can be seen right of the heat sink. A rogowski coil current probe is connected around the negative terminal of DC-bus, where it is connected to the MOSFET module. To prevent accidents, the components not isolated from the 600 V power supply were placed under an acrylic glass box.

On the right side of the picture, the controller board can be seen, connected to the interface board through a ribbon cable. The 6 bit interface to the driver is then connected on top of the piggyback board, which is connected to the gate driver evaluation board.

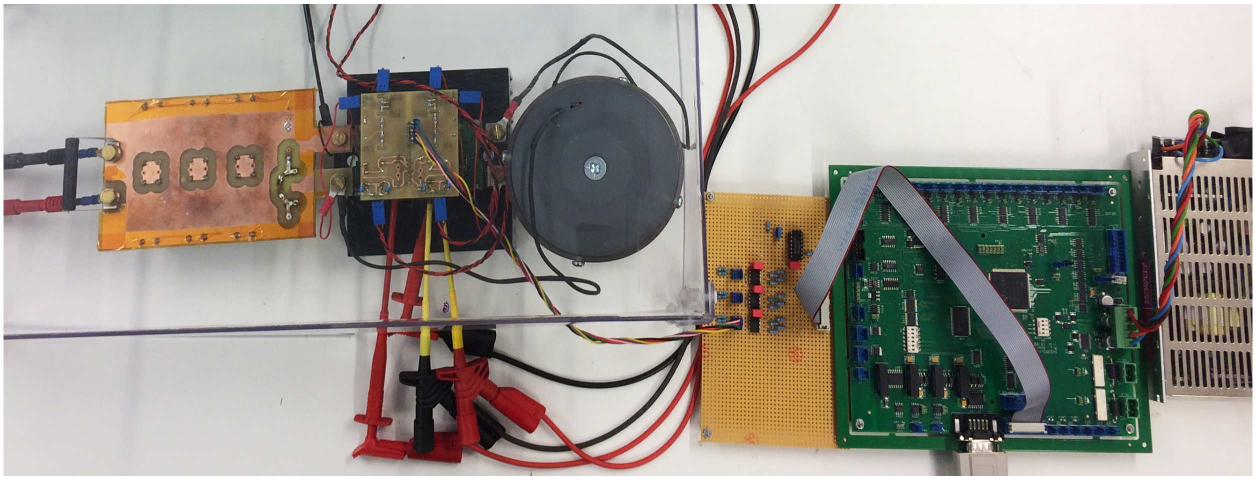


Figure 4.2: Experimental double-pulse setup.

Figure 4.3 shows how the gate driver evaluation board is placed on top of the MOSFET module. The piggyback board then connects on top of the gate driver through a 16 bit interface, similar to the piggyback board which was described in section 3.4.2. The connection to the interface board can be seen on top of the piggyback board. The voltage probes can be seen connected to the drain, source and gate terminal of the DUT.

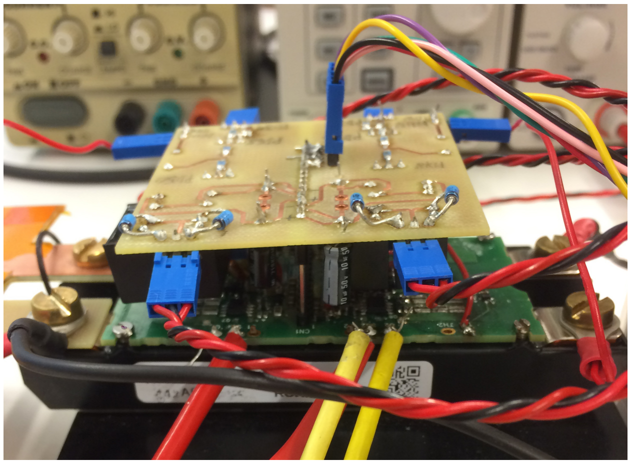


Figure 4.3: Components from bottom to top: MOSFET module, gate driver, piggyback board.

4.2.3 Measurement Instruments

Oscilloscope

The mixed signal oscilloscope MSO2024B from Tektronix was used. This oscilloscope offers voltage sampling at up to 1GS/s, which gives a bandwidth of 200 MHz. As will be presented in the following the most high frequent dynamics observed in the results has a frequency at maximum 25 MHz, so the oscilloscope bandwidth is more than sufficient.

It is important that the measurement probes has a bandwidth of no more than the oscilloscope bandwidth of 200 MHz, to prevent signal aliasing. The bandwidth is commonly defined as the frequency where the signal gain crosses the -3 dB line from above [32], and this is also the case for the probes used here. For signal frequencies above the bandwidth, the probes attenuate the signal.

The oscilloscope can export measurement data as .csv files, so the measurements can be analyzed more thoroughly on a computer. A description of the methods used to analyze the data is presented in chapter 6, where the results from the experimental testing is also presented.

Voltage Probes

The high-voltage differential probe P5200A from Tektronix was used to measure gate-source and drain-source voltage. The same probe was also used to measure the voltage across the snubber resistor, when tests with RC snubbers were conducted. The P5200A differential probe has a bandwidth of 50 MHz, and a voltage rating of 1.3 kV.

Current Probe

Initially, the CWT6B rogowski coil current probe from PEM was used to measure drain current in the double-pulse tests. This instrument has a bandwidth of 16 MHz, which is less than the ringing frequency that can be observed occurring in the module at hard-switching. The attenuation of the higher frequency components of the signal leads to a erroneous measurement, and the CWT6B probe was therefore substituted with the CWTUM6B current probe from PEM instead. A comparison of measurements of the turn-off current in a double-pulse test can be seen figure 4.4. Evidently the lower bandwidth probe fails to capture the full dynamic of the transient. As will be shown in the following, a significant part of the turn-off loss occurs when the current and voltage are ringing, so it is critical to get an accurate measurement here.

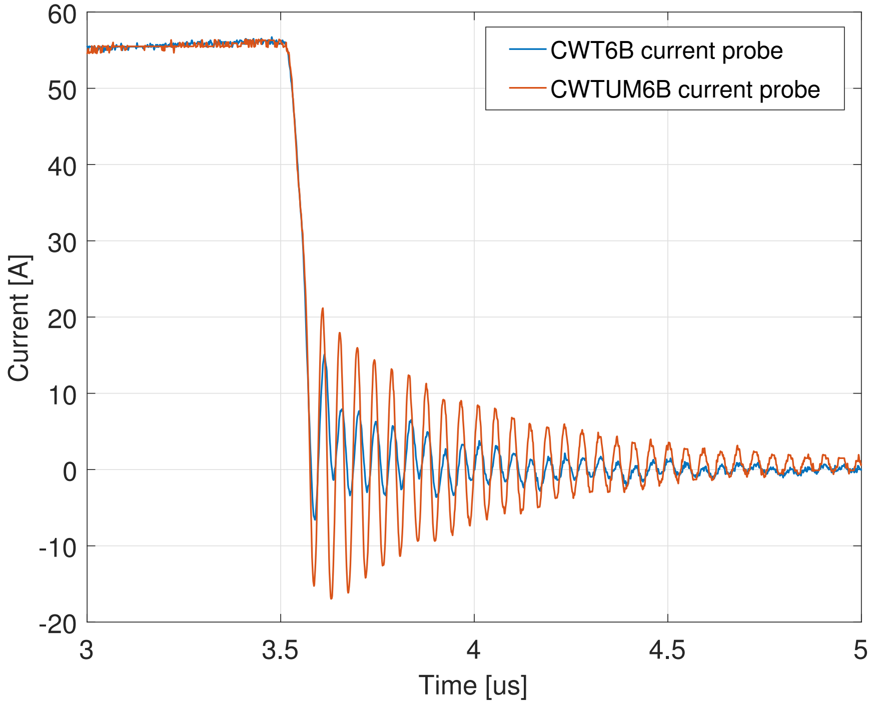


Figure 4.4: Comparison of current at turn-off, measured with the two different current probes CWT6B and CWTUM6B.

4.2.4 List of Laboratory Equipment

A full list of the equipment used in the double-pulse test is presented in table 4.1. The circuit boards that was made for this particular project is not included, however the components used to make these boards are listed in the bills of materials shown in appendix A.

Table 4.1: List of Laboratory Equipment

Application	Equipment	Model	Manufacturer
Current measurement	Rogowski coil	CWTUM6B	PEM
Current measurement	Rogowski coil	CWT6B	PEM
Voltage measurements	High-voltage differential probe	P5200A	Tektronix
Waveform capturing	Oscilliscope	MSO2024B	Tektronix
600 V DC power supply	DC voltage supply	HCP 350 - 3500	Fug
Gate driver power supply	DC voltage source	72-2540	Tenma
Gate driver power supply	DC voltage source	320-KD3005D	RND Lab
Pulse generation	Control board	SM335Controller	SmartMotor
Control board power supply	Power supply unit	TXL 060-0533TI	Traco Power
Gate driver	Gate driver evaluation board	BW9499H	ROHM
Device under testing	SiC MOSFET module	BSM120D12P2C005	ROHM

4.3 Preliminary Double-Pulse Testing

A preliminary series of double-pulse tests were conducted, to determine the relevant stray inductance value to be used in the LTspice simulations. The gate resistances that were used in the test, and that were used in all tests with the 120 A-module presented in this thesis, were 4.5 Ω and 2.2 Ω for the turn-on resistance and turn-off resistance respectively. This choice was made based on simulation tests conducted in the project work [1], where it was shown that the turn-on resistance must have a higher value to reduce the current peak occuring through the lower MOSFET at turn-on.

The full waveforms of the drain current and drain-source voltage measured in a laboratory double-pulse test can be seen in figure 4.5. As explained in section 4.2.1, the first pulse turns on the DUT, allowing the current to rise linearly through the load inductor. When the current reaches the targeted level, the DUT is switched on and off, allowing the characteristics to be investigated at hard-switching. Thus, in figure 4.5, the relevant measurements occur in the time interval from 25 μs to 35 μs.

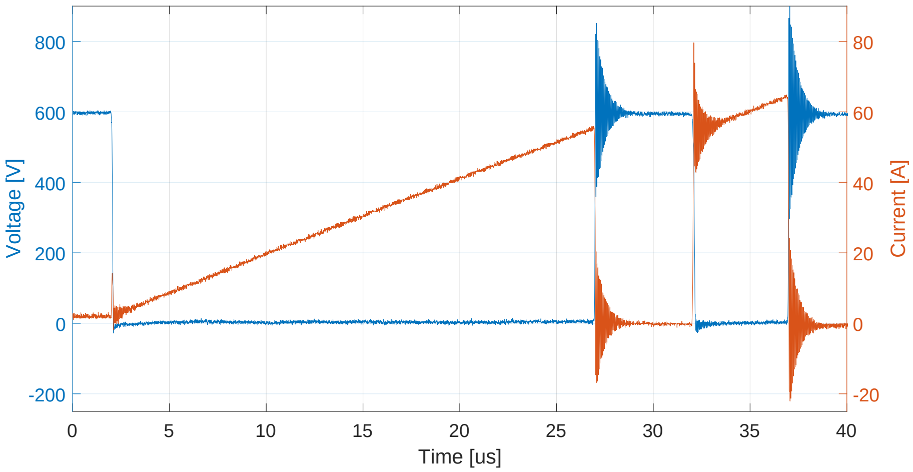


Figure 4.5: Full waveform measured in double-pulse test.

As was discussed in section 2.4.3, the stray inductance can be approximated using the expression for the undamped ringing frequency. Using equation 2.14, we get that the stray inductance L_s is given by

$$L_s = \frac{1}{(2\pi f_r)^2 \cdot C_{DS}}, \tag{4.2}$$

where f_r is the ringing frequency of the drain-source voltage of the DUT and C_{DS} is the parasitic drain-source capacitance. The ringing frequency can be calculated by measuring the time period between voltage peaks, and an average of the time interval of the first five periods was used to calculate the frequency. The waveforms of the voltage and current at turn-off and turn-on switching of the DUT is shown in figure 4.6.

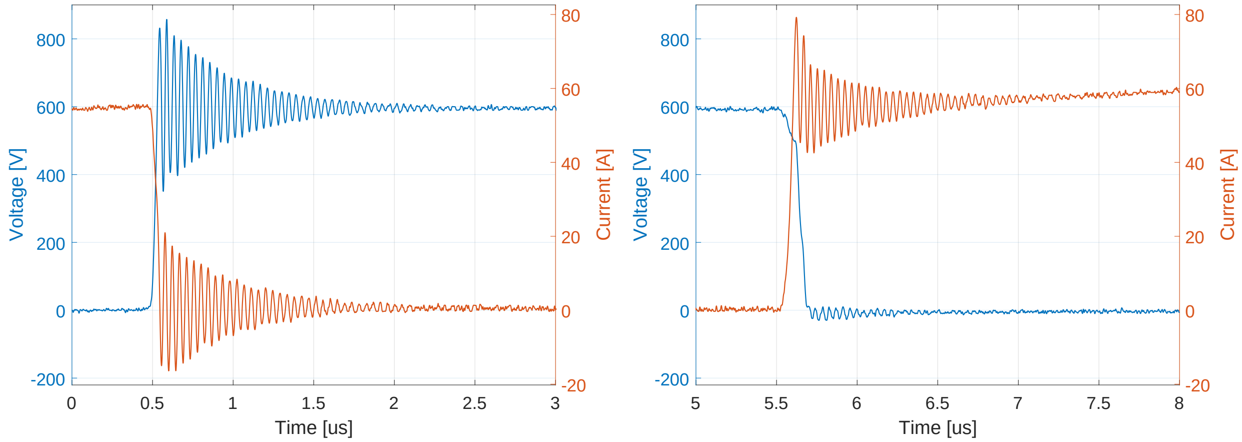


Figure 4.6: Waveforms from preliminary double pulse test. Left: Turn-off. Right: turn-on.

The waveforms in figure 4.6 is filtered using a second order Butterworth filter with 100 MHz cutoff frequency, to remove noise. Additionally, the current bias caused by the rogowski coil is removed. These preprocessing methods on the measurement data is described in more depth in chapter 6. The frequency of the ringing was calculated to be 22.5 MHz. This matches the frequency of the distinct spike in amplitude seen in the Fourier transform of the voltage measurement in figure 4.7.

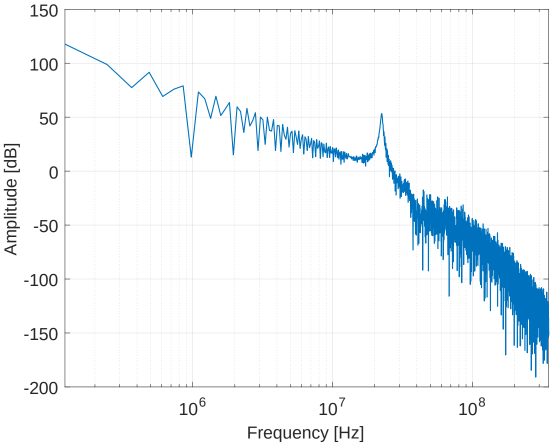


Figure 4.7: Fourier transform of drain-source voltage, corresponding to above waveforms.

As was explained in section 2.4 the drain-source capacitance vary with the drain-source voltage. The voltage ringing primarily occurs around the nominal turn-off voltage level of 600 V, which can be observed in figure 4.6, and the parasitic drain-source capacitance of the MOSFET module at 600 V will therefore be used in the calculations. The output capacitance C_{oss} and reverse transfer capacitance C_{rss} can be found in the datasheet [30], and the drain-source capacitance can be calculated from these values using equation (2.15):

$$C_{DS} = C_{oss} - C_{rss} = 890\,\mathrm{pF} - 50\,\mathrm{pF} = 840\,\mathrm{pF}. \tag{4.3}$$

The stray inductance can now be calculated:

$$L_s = \frac{1}{(2\pi \cdot 22.5\,\mathrm{MHz})^2 \cdot 840\,\mathrm{pF}} = 60\,\mathrm{nH}. \tag{4.4}$$

The internal inductance of the MOSFET module is 25 nH [30], so it can be concluded that the stray inductance of the DC-bus is 35 nH. This external stray inductance value will be used in simulating the double-pulse tests of the 120 A-module.

4.4 Impedance Measurements

The E4990A impedance analyzer from Keysight Technologies was used to investigate the impedance of the DC-bus that was designed for the three phase converter, and the smaller DC-bus used in the double-pulse tests with the 120 A-module. The aim of the investigation was to see whether the inductance calculated from the impedance measurements matched the inductance that can be calculated based on the double-pulse test results. Additionally it was interesting to see what stray inductance was achieved in the three phase DC-bus, as this gives an indication about the switching performance of the future SiC based three phase inverter using this DC-bus.

4.4.1 Overview of Impedance Test Setup

The impedance analyzer gives the possibility to measure a large variety of parameters, e.g. capacitance, inductance, resistance, Q-factor and so on. All of these parameters are calculated from a measured impedance, applying some circuit model of the testing object, e.g. an RLC-circuit. It was decided to measure the impedance absolute value $|Z|$ and impedance angle θ in the tests, so inductance could be calculated manually by applying a fitting circuit model of the test objects.

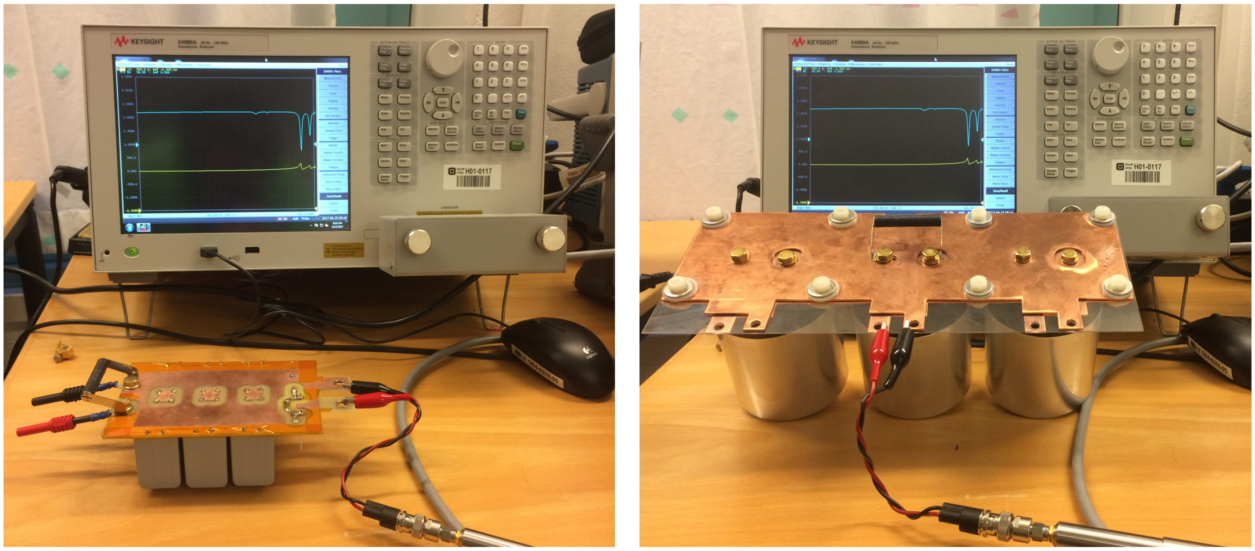


Figure 4.8: Test objects at under analysis. Left: 120 A-module DC-bus. Right: Three phase DC-bus.

The probe from the impedance analyzer was attached to the output terminals of the DC-buses, where they should connect to the MOSFET modules. The input terminals were left open. The test objects under analysis can be seen in figure 4.8. A circuit model of the DC-bus for the 120 A-module is shown in figure 4.9. A stray inductance L_{mid} is assumed to be placed between the positive and negative terminals of each of the parallel connected bulk capacitors C_{DC}. Further more, the stray inductances L_{in} and L_{out} are placed at the positive and negative poles of the input and output terminals respectively.

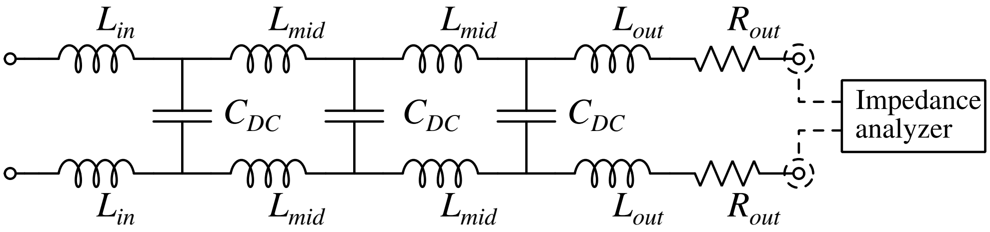


Figure 4.9: Circuit model of DC-bus.

As was shown in section 3.6.2, most of the stray inductance in the DC-buses is located on the output terminals, where the distance between the positive and negative terminal is large. It is therefore assumed that the inductance between the bulk capacitors can be neglected. Lumping the stray inductances together, and the output resistances together, we get an RLC-series seen from the impedance analyzer. The impedance of the RLC-series is given by

$$Z = R + i\left(\omega L - \frac{1}{\omega C}\right), \tag{4.5}$$

where R is the sum of the two output resistors R_{out}, L is the sum of the two output stray inductances L_{out}, and C is the total DC bulk capacitance resulting from the parallel connection between the capacitors C_{DC}. ω is the angular frequency of a specific measurement. The same circuit model was also used for the three phase DC-bus inductance calculations.

Using equation (4.5), the inductance L can be calculated from the impedance measurement from the analyzer instrument:

$$L = \frac{1}{\omega^2 C} + \frac{1}{\omega}\mathrm{Im}\big(|Z|e^{i\theta}\big). \tag{4.6}$$

The total bulk capacitance of the DC-bus used in the double-pulse tests with the 120 A-module is 120 μF, and the DC-bus designed for a three phase converter has a total capacitance of 1650 μF.

4.4.2 Impedance Test Results

The measurement probe consisted of two wires to connect to the terminals of the test objects. The wires were twisted to reduce the inductance of the probe, however the wires were still influencing the test results. A test where the terminals of the probe were short circuited was therefore conducted, to determine the inductance of the probe, as seen in figure 4.10. The inductance was calculated using equation (4.6), though ommiting the capacitive term. The probe inductance was then subtracted from the test results with the DC-buses.

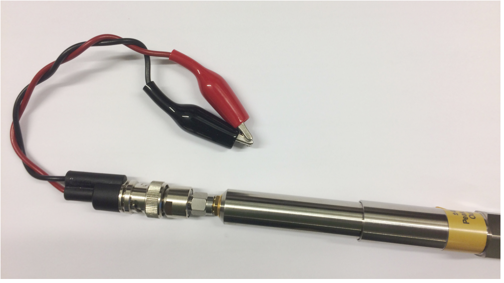


Figure 4.10: Short circuit test of probe.

The result of the inductance calculation of the 120 A-module DC-bus can be seen in figure 4.11. We see that for lower frequencies, the inductance is 35 nH, which is the same value that was calculated based on the results form the double-pulse test in the previous section. It is observed that the inductance stays relatively stable until an irregular behavior occurs in the frequency interval from 20 MHz to 35 MHz. This could be explained by the simplified model used to perform the inductance calculations. A model capturing more of the dynamics of the DC-buses could applied, however it would require more sophisticated testing scheme to find all circuit parameters.

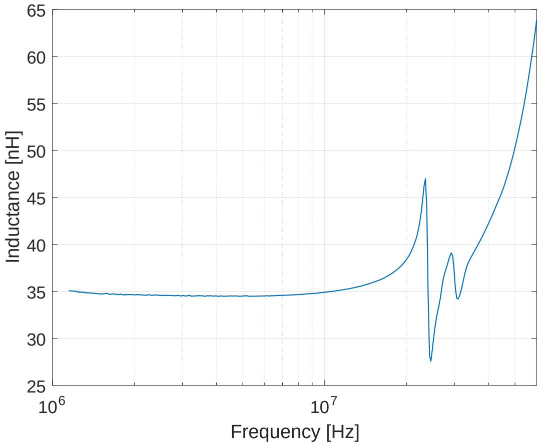


Figure 4.11: Calculated inductance for the 120 A-module DC-bus

Figure 4.11 shows the test results with the three phase DC-bus. Here, two separate tests were conducted, where the measurement probe was attached to the middle terminals of the bus and the terminals on one of the sides. Both plots shows that the stray inductance is reduced in the three phase DC-bus, compared with the DC-bus used for the 120 A-module double-pulse tests. The reason is that the conduction paths are wider in the three phase DC-bus, and this reduces inductance, as explained in section 3.6.2. Additionally, the distance between the terminals of the 300 A-modules, for which the three phase DC-bus was designed for, is shorter than the terminal width of the 120 A-module.

The measurements from the middle terminal show less inductance, compared to the side terminal. This is because the middle terminal has a shorter distance to the capacitors, and a wider trace width in both directions, perpendicular on the conduction direction.

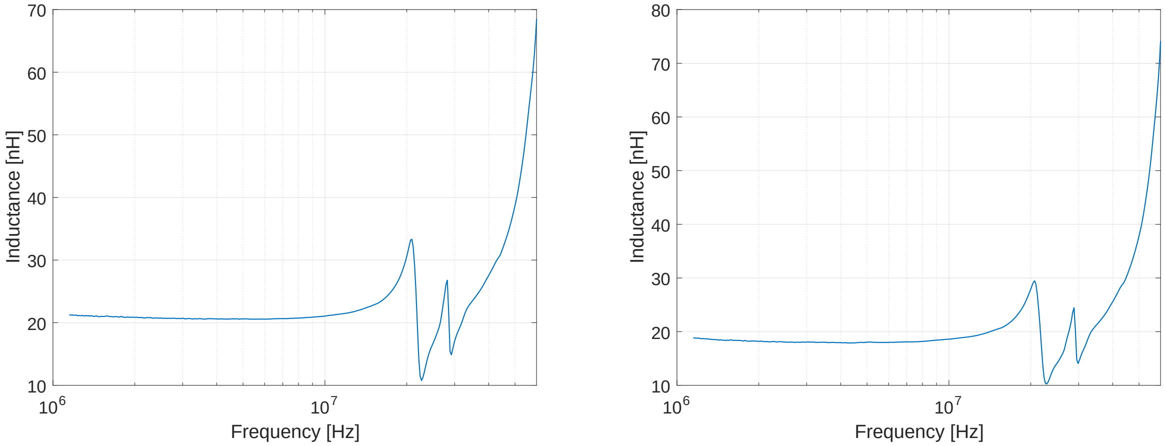


Figure 4.12: Calculated inductance for the three phase converter DC-bus. The left plot shows the inductance measured from one of the terminals on the side of the bus, and the right plot shows the inductance measured from the middle terminal.

Due to the smaller stray inductance in the three phase DC-bus seen here, smaller voltage overshoots and ringing can be expected in the final SiC MOSFET three phase converter, compared to what the simulation and laboratory with the 120 A-module results will show in the following. This is very important, because the final design aims to utilize the BSM300D12P3E005 modules from ROHM, which have a rated current of 300 A. Aiming to use higher currents in the design, will amplify issues with EMI and voltage overshoot, and thus a reduced stray inductance in the final DC-bus bar design is a desirable result.

Chapter 5

Simulations

5.1 Introduction

It is common for producers of electronics to provide simulation models of the hardware, so the characteristics and performance of the hardware can be explored in an effective and simplified way. ROHM Semiconductor, who produces the BSM120D12P2C005 and BSM300D12P3E005 SiC MOSFET modules, provides such simulation models of their SiC MOSFET modules. The simulation models can be used in a circuit simulation program called LTspice IV, which is an implementation of Simulation Program with Integrated Circuit Emphasis (SPICE), a general purpose electronic circuit simulation program [33].

The aim of simulating the MOSFET modules is to characterize the performance of the module, and explore how the performance can be improved with snubber circuits in a simple manner. This methodology allows for trial and error more quickly than what would otherwise be possible in an approach with just laboratory experiments. The results from the simulations were verified through experiments, and a thorough comparison will be presented in the next chapter, highlighting important limitations of the simulation model.

This chapter will present switching times, switching losses and characteristics related to ringing such as frequency and damping. These values will be presented for different circuit configurations and parameters.

In the project work [1] leading up to this thesis, some simulations were performed using the 120 A-module. As part of the project work, a software add-on was developed, to work with the LTspice software. The add-on was developed to simplify simulations with large sets of different parameters, fasten data extraction from LTspice and automate calculations of performance characteristics. The add-on was used in performing the simulations here as well. The add-on is available in its entirety on GitHub [35], and documented thoroughly in the project report [1]. Only key aspects of its implementation will be highlighted here.

5.2 Methodology

The main circuit, used to conduct double-pulse simulations in LTspice, is shown in figure 5.1. The MOSFET half-bridge, with anti-parallel diodes, is the simulation model of the BSM120D12P2C005 module provided by ROHM Semiconductor. This model implements all relevant electrical characteristics of the physical device. The lower MOSFET was hard-switched in the double-pulse test, in the way explained in section 4.2.1, and is thus the device under testing (DUT). The current will free-wheel through the upper diode when the lower MOSFET is in the off-state, and the waveforms and different switching characteristics will be investigated for the upper part of the module as well.

The circuit design includes circuit elements to imitate the circuit used in the laboratory testing as close as possible. To include the external stray inductance caused by the DC-bus, an inductance L_{stray} was connected between the positive terminal of the DC source, and the half-bridge. This value was set to the stray inductance calculated in section 4.3. A current source was used to set the current conducting through the DUT during the double-pulse test. In the laboratory experiments a large inductor coil was be used to create this current, as described in section 4.2.1, however a current source enables easier control of the current in the simulations, while giving the same results.

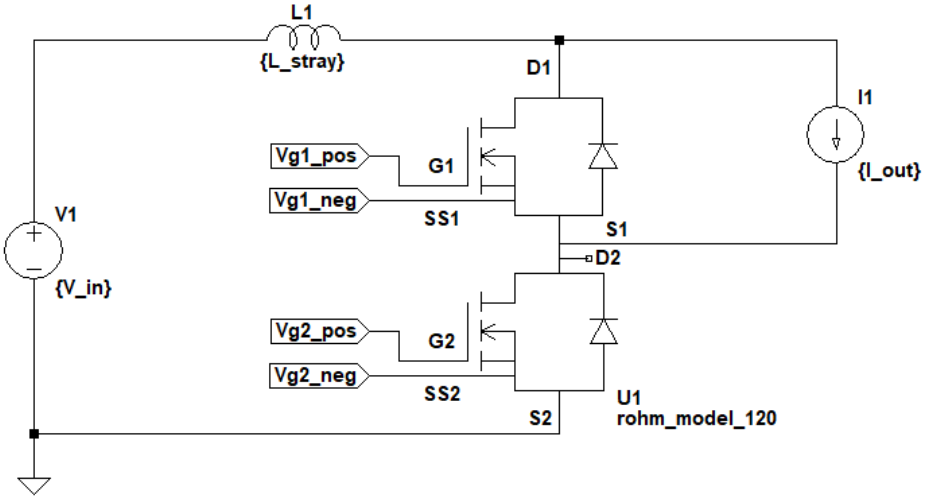


Figure 5.1: LTspice simulation circuit.

The gate signals are sent through separate turn-on and turn-off resistors, by connecting the resistors in series with a diode to set the conduction direction. This enables separate control of turn-on and turn-off time. The gate circuitry is shown in figure 5.2. The gate signal to the DUT is a single pulse, corresponding to the second pulse in the double-pulse test. The first pulse used in a double-pulse is not necessary, as this pulse is used to build the current through the load inductor, which is substituted by a current source in the simulation circuit. The gate-source voltage of the upper MOSFET is kept at a constant level of -5 V, i.e. the upper MOSFET is constantly turned off. In PWM operation the upper MOSFET would be switched as well, however when the lower MOSFET is conducting the load current, the anti-parallel diode will carry the current through the upper part. The upper part will therefore behave in the same way as if the MOSFET was turned off, and keeping the upper MOSFET turned off for the double-pulse test simplifies the experiment without impacting the result.

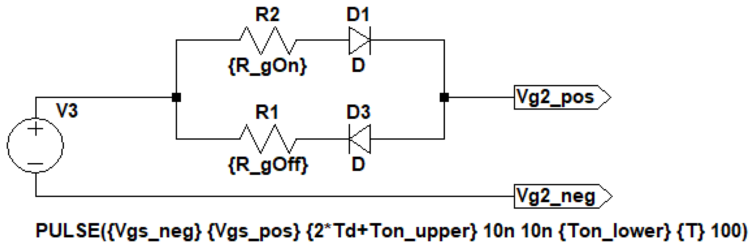

R2
D1
{R_gOn}
D
V3
R1
D3
{R_gOff}
D
Vg2_pos
Vg2_neg
PULSE({Vgs_neg} {Vgs_pos} {2*Td+Ton_upper} 10n 10n {Ton_lower} {T} 100)

Figure 5.2: LTspice simulation circuit

The Python program developed in the project work [1] was used to automate the simulations, and the calculations of switching characteristics. The program calculates the rise and fall times of the drain-source current and voltage, the ringing frequency, overshoots and damping of the drain-source current and voltage. Based on the time instances of the switching intervals, which are also used to calculate the rise and fall times, and the damping of the ringing, the program can calculate the switching losses. In total, these values characterize the switching transitions of the MOSFETs to a large degree, as discussed in 2.4, and can be used to compare the simulation model with the experimental laboratory setup. A more complete discussion and documentation can be found in the project report [1].

5.3 Initial Simulation Results

In this section, simulation results using from what will be referred to as the base circuit will be presented. The base circuit has the parameters presented in table 5.1. The stray inductance is the value that was calculated in section 4.3, using the result from the preliminary double-pulse test in the laboratory. The gate resistance values were investigated in the project work [1]. There it was decided that, based on a trade-off between current overshoot and switching losses, the turn-on resistance should be 4 Ω, and the turn-off resistance should be 2 Ω. However in the laboratory, the closest match to these values were 4.5 Ω and 2.2 Ω respectively. To match the conditions under the laboratory experiments, these resistors were used in the simulation as well.

The base case circuit was used in the initial simulations, which are presented in the following, before snubber circuits were introduced. The switching characteristics were investigated

Table 5.1: Base circuit parameters

Parameter	Value
L_{stray}	35 nH
R_{gOn}	4.5 Ω
R_{gOff}	2.2 Ω

for varying load current, which will serve as a basis for comparison with the experimental results.

5.3.1 Switching Waveforms of Base Circuit

The switching waveforms of the upper and lower part of the half-bridge are shown in figure 5.3 and 5.4 respectively, for a load current of 60 A. 60 A would be the defined nominal RMS current for a three phase inverter utilizing 120 A current rated MOSFET modules. The current shown will be conducted through the lower MOSFET, and freewheel through the upper anti-parallel diode when the lower MOSFET is turned off. The positive current direction are therefore source-drain for the upper MOSFET and drain-source for the lower MOSFET.

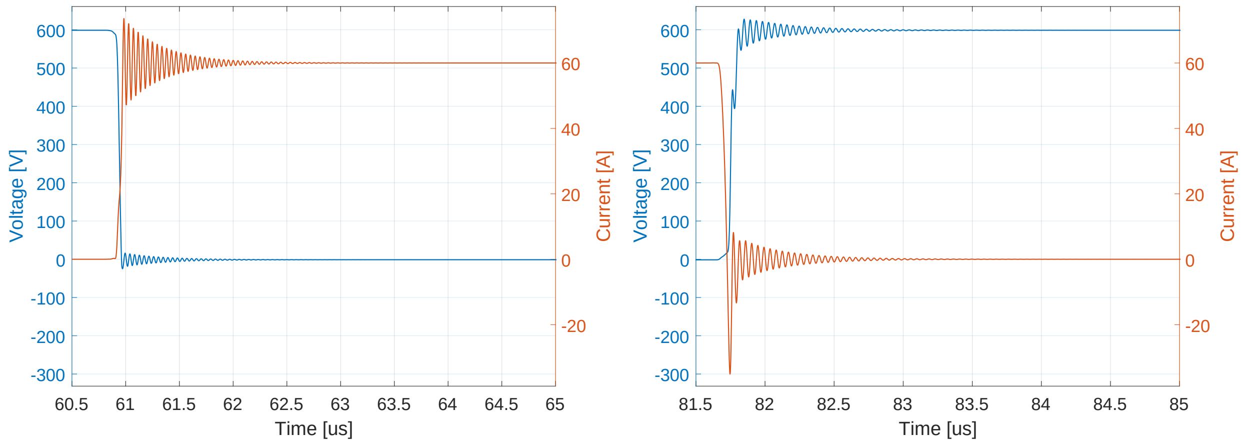


Figure 5.3: Waveforms of upper MOSFET in base case. Left: Turn-on. Right: Turn-off.

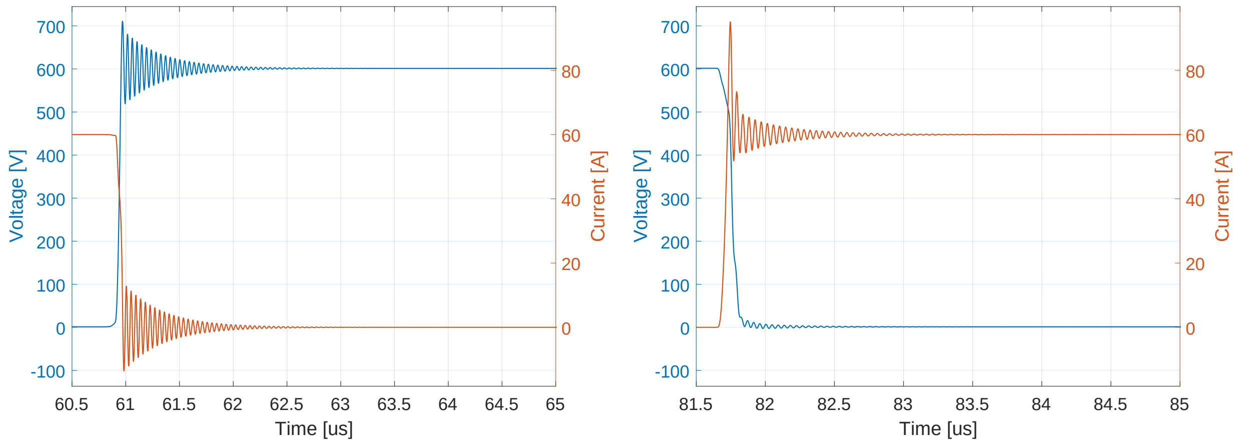


Figure 5.4: Waveforms of lower MOSFET in base case. Left: Turn-off. Right: Turn-on.

From the waveforms, we see that there is a difference in the switching waveforms of the upper and lower part of the half-bridge. It was shown in the project report [1] that these waveforms mirrors as the current direction is changed. The analysis made here can therefore be generalized to hold for any current, and for example the total switching loss will be independent on current direction.

A large current overshoot can be seen in lower MOSFET at turn-on, and it is observed that this peak corresponds closely to the current conducted through the upper part of the MOSFET module at the same time. At DUT turn-on, the freewheling diode must get reverse biased, and the current spike seen in the DUT turn-on transition is caused by the reverse recovery current of the freewheeling diode. It was shown in equation (2.18) in the theory that the reverse recovery current increases with increasing di/dt of the diode, and we can therefore expect the current overshoot to increase with the load current.

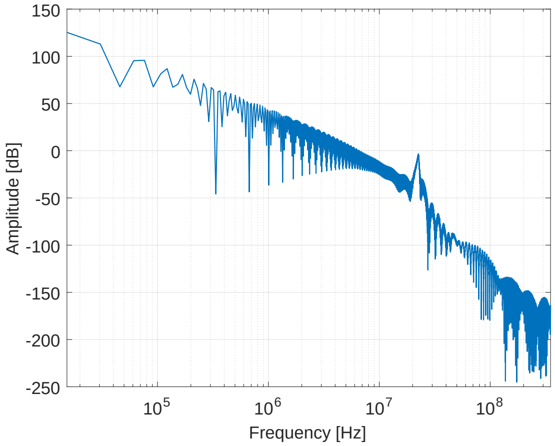


Figure 5.5: Fourier transform of drain-source voltage of DUT

The Fourier transform of the DUT voltage measurement from the results is shown in figure 5.5. The Fourier transform is observed to correspond closely to the Fourier transform of the laboratory voltage measurement, presented as part of the preliminary double-pulse tests in section 4.3. The spike in amplitude occurs at the same frequency as for the laboratory results, which indicates that the stray inductance value used is correct. The amplitude is smaller than in the laboratory Fourier transform however, and this indicates that the voltage overshoot measured in the simulation results is too small. The differences between the simulation results and experimental results will be discussed in more depth in the next chapter.

5.3.2 Output Current Influence

The switching characteristics were investigated for a varying output current between 30 A and 90 A. The voltage peak $\hat{V}$ and current peak $\hat{I}$ of the upper and lower part of the MOSFET module are presented in table 5.2, where the subscripts *up* and *lo* denote that the variable is given for the upper and lower part respectively. The frequency of the ringing f, and the damping constant of the ringing α are also given.

Table 5.2: Switching characteristics

I_{out}[A]	$\hat{V}_{up}$[V]	$\hat{I}_{up}$[A]	f_{up}[MHz]	α_{up}[Ms^{-1}]	$\hat{V}_{lo}$[V]	$\hat{I}_{lo}$[A]	f_{lo}[MHz]	α_{lo}[Ms^{-1}]
30	611.1	35.9	22.7	2.2	640.3	59.7	22.6	2.8
60	627.7	73.6	22.6	2.1	710.7	95.1	22.3	3.8
90	641.5	108.5	22.6	2.5	768.8	128.4	22.1	4.3

The switching characteristics given in the table shows that the voltage overshoot across both MOSFETs, and the ringing of these voltages, increases as the current is increasing. The voltage overshoot and ringing is in particular severe for the lower MOSFET, which is being hard-switched. In the right plot of figure 5.6, the switching times of the lower MOSFET are plotted against the increasing load current. Here it can be seen that the turn-off transition time, i.e. the current fall time and voltage rise time, decreases as the output current is increased. In addition the current interval increases, and the circuit experiences an increase in di/dt. This growing di/dt induces voltage across the stray inductance in the circuit, and give rise to the increased voltage overshoot. Table 5.2 reveals that the voltage overshoot across the upper MOSFET also increases with the output current, however not as extreme as for the lower MOSFET. The left plot in figure 5.6 shows that the turn-off transition time increases with the current, so the time interval of the current change increases and thus limits the di/dt. The large change in current is higher relative to the transition time change however, giving a net increase in di/dt and voltage overshoot.

The frequency of the voltage oscillations can be seen to remain almost stable as the current changes, however the damping constant of the ringing increases, both for the upper and the lower MOSFET, i.e. the time constant of the exponential decay decreases.

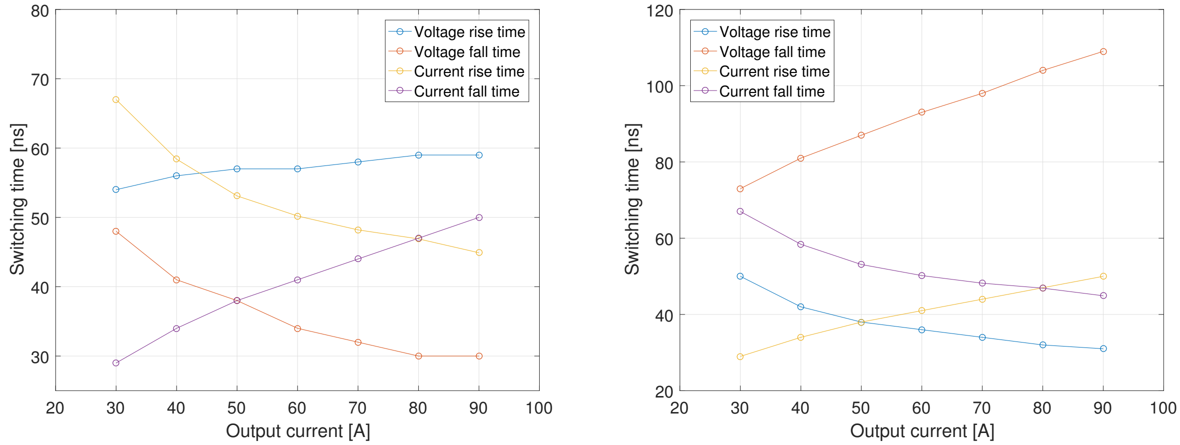


Figure 5.6: Switching times of the MOSFETs in base case. Left: Upper. Right: Lower.

The switching losses calculated for the upper and lower part of the module are presented in figure 5.7. We see that the upper part of the module has a negative power loss in the turn-on transition. This is due to the parasitic capacitance across the MOSFET and diode, which stores an amount of energy as the capacitor gets charged, and is released as the voltage across the diode decreases to zero. When the current then increases, the ohmic losses increase, and the net turn-on loss approaches zero.

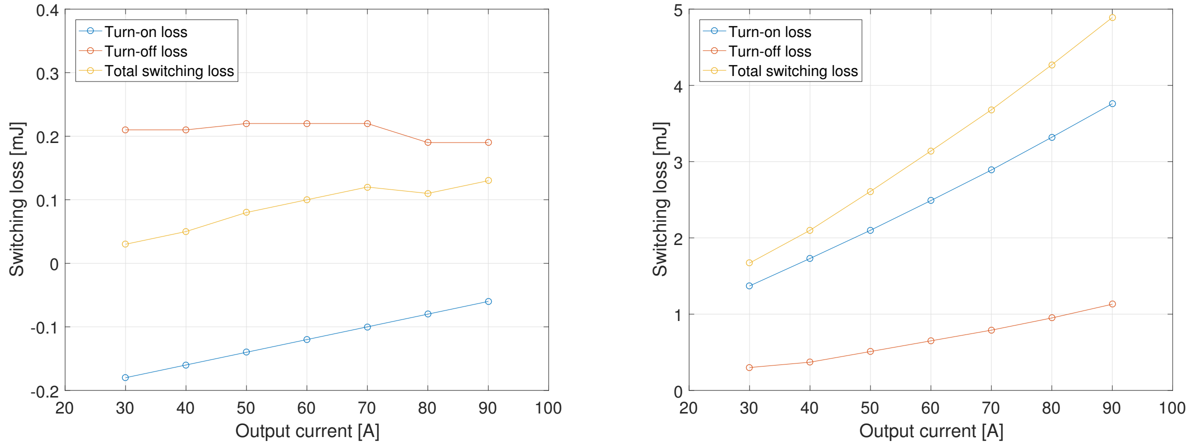


Figure 5.7: Switching losses in the MOSFETs in base case. Left: Upper. Right: Lower.

The lower MOSFET losses increase with the output current. The turn-on losses increase faster than the turn-off losses, and this can be explained by the fact that the turn-on transition time increases with the current, as opposed to the turn-off time, as seen in figure 5.6. This gives a longer interval where both voltage and current are non-zero, and switching losses occur. While the switching interval decrease with current for the turn-off transition, the increase in current is large enough for the dissipated losses to increase. The longer ringing interval at turn-off also contributes, as the net power loss here is positive.

5.4 Simulation Results from Circuit with Snubbers

5.4.1 Configuration and Simulation Scheme

The LTspice simulation circuit with snubbers included is shown in figure 5.8. The circuit includes both a DC-snubber and a RC turn-off snubber, which were both discussed in section 2.5 in the theory chapter. The simulations were performed with the DC-snubber and the RC turn-off snubbers separately, and then together with appropriate snubber parameters. Both snubber types were included in the circuit from the beginning to ease the automation of the simulations. Either snubber can be disabled by setting the capacitance of the snubber to zero, hence blocking any current from being conducted through that parallel of the circuit.

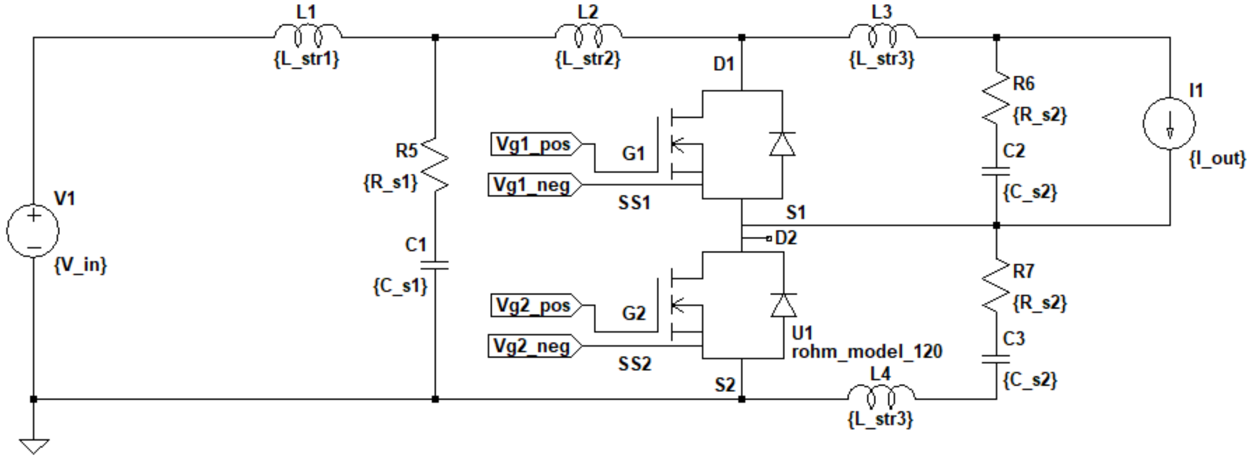


Figure 5.8: LTspice simulation circuit, with snubbers included.

The stray inductance from the DC-bus was split up into two separate inductances on each side of the DC-snubber. The inductance closest to the DC-bus, $L1$ in the schematic, was set to 25 nH, wheras the other one was set to 10 nH. Stray inductances were also included in the turn-off snubbers, where each inductance was set to 10 nH. The stray inductances of the RC turn-off snubbers does not affect the circuit when simulations are performed with the turn-off snubbers diabled, as the load current is constant and the di/dt across the stray inductances therefore are zero.

5.4.2 Calculation of Snubber Values

Using equation (2.27) and (2.29), derived in section 2.5.4, the RC-snubber values can be calculated. From section 4.3 we know that the drain source capacitance C_{DS} is 840 pF. The simulation results from the previous section showed that the ringing frequency varies slightly with current. The frequency of 22.6 MHz at the nominal output current of 60 A was used in the calculation of the RC-snubber values. These values are presented in table 5.3.

The snubber values presented in table 5.3 will also used to dimension the DC-snubbers. The reason for the use of identical snubber values in the RC turn-off snubber and the DC-snubber is the similarity in their damping dynamics, and was explained in 2.5.5.

Table 5.3: Snubber Values

Damping	R_s [Ω]	C_s [nF]
0.1	41.9	1.1
0.2	21.0	2.1
0.3	14.0	3.2
0.4	10.5	4.2
0.5	8.4	5.3
0.6	7.0	6.3
0.7	6.0	7.4
0.8	5.2	8.4
0.9	4.7	9.5
1.0	4.2	10.6

5.4.3 Results with RC Turn-Off Snubber

Table 5.4 presents the voltage and current overshoots, for the upper and lower part of the module, at different levels of damping. The ringing frequency and damping constants are not included, as the voltage oscillates with only one or two peaks for damping constant above 0.1, and the damping constant was therefore not considered a meaningful measure.

Table 5.4: Switching characteristics with RC turn-off snubber

Damping	$\hat{V}_{up}$[V]	$\hat{I}_{up}$[A]	$\hat{V}_{lo}$[V]	$\hat{I}_{lo}$[A]
0.1	610.3	61.5	675.2	98.1
0.2	605.7	60.0	649.5	101.0
0.4	605.7	60.0	635.0	106.7
0.8	616.8	60.0	629.3	135.4
1.0	621.3	60.0	627.8	150.1

The table shows that the voltage across the lower MOSFET decreases significantly when the damping constant is increased, however the voltage is not removed entirely. This suggests that the simple MOSFET switching model that was presented in section 2.4.3, and applied in the snubber impedance calculations presented in section 2.5.4, is inaccurate.

The voltage across the upper MOSFET is reduced by introducing the RC-snubbers, compared to the voltage measured for 60 A, presented in table 5.2. It increases a little for higher damping constants however, but is still smaller than the overshoot across the lower MOSFET.

The current peak of the lower MOSFET increases above the current rating of the module as the damping constant is set to higher values. While the maximum current through the diode remains at a constant level, the negative peak corresponds to the maximum value measured through the lower MOSFET, as was discussed in the previous section. A larger current than what is reflected in the table is therefore also conducted through the upper part of the MOSFET. This current peak, that occurs at turn-on of the lower MOSFET, increases due to the increase in snubber capacitance for higher damping constants. From basic circuit theory it is known that the current through a capacitor is given by

$$i_C = C\frac{dv_C}{dt}, \tag{5.1}$$

so an increase in the capacitance C give rise to a larger current, for an equal dv/dt. This current gets conducted from the snubbers, through the MOSFET module. In figure 5.9 it can be seen that the voltage fall time of the lower MOSFET increases with the damping constant, and changes with a factor of 1.3 when the damping factor is increased from 0.1 to 1. Since the voltage interval is the same, the increased voltage fall time corresponds to a fall in dv/dt with a factor of 0.77. At the same time, the snubber capacitance is increased with a factor of 10, so a net increase in current is expected. It should be noted that the full drain-source voltage does not lay across the capacitor when it starts to conduct, due to the resistor, so the net increase in current is smaller than the factors presented above indicate.

The switching times of the upper and lower part of the MOSFET module are presented in figure 5.9. From the plot of the switching times of the upper MOSFET, the current rise time appears to behave somewhat unpredictable, compared to the rest of the switching times. This artifact is caused by the definition of the switching times. The rise time for the current for example is defined as the time interval when the current is between $0.1 \cdot I_{out}$ and $0.9 \cdot I_{out}$, and the other switching times are defined similarly. Artifacts as the one seen in figure 5.9 arise, when the waveforms have distortions in their waveforms which change with the circuit parameters. The odd current rise time behavior is explained by the small plateau occurring on the rising edge of the current in figure 5.11, which arise at a lower level for higher damping constants.

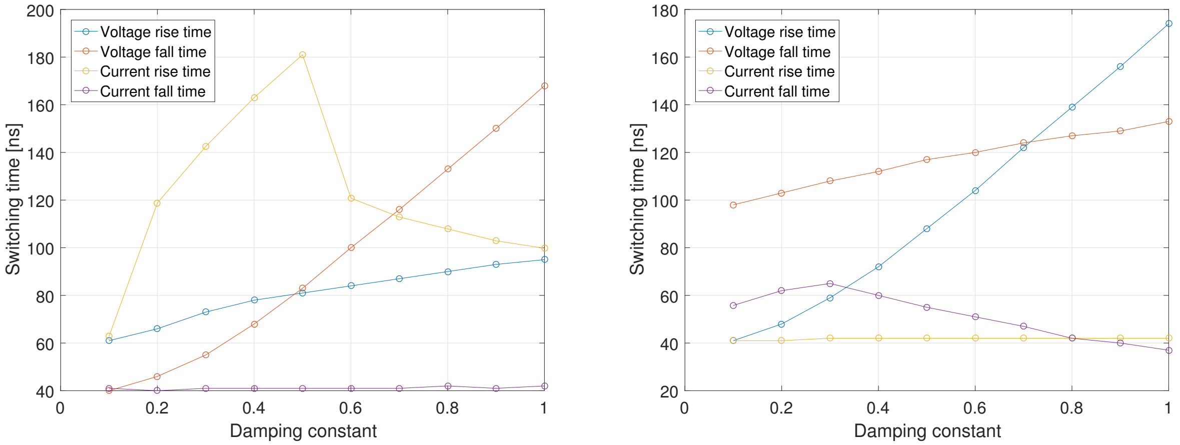


Figure 5.9: Switching times of the MOSFETs with RC-snubber. Left: Upper. Right: Lower.

From the switching time plots presented in figure 5.9, it can be seen that the voltage rise time increases with a factor of more than 4 for an increase in damping constant from 0.1 to 1.0. The same increase can be seen in the voltage fall time across the upper MOSFET. Simultaneously, the current fall time decreases. The increasing voltage rise time of the lower MOSFET does not result in a larger turn-off loss however, because the current through the MOSFET is redirected to the turn-off snubber as the voltage starts to rise.

The switching losses calculated for different damping constants are shown in figure 5.10. We see that the turn-off loss decreases with increased damping constant of the snubber, in accordance with the explanation above. The energy stored in the snubber capacitors is given by

$$E_s = \frac{1}{2} C_s V_{DS}^2, \tag{5.2}$$

where V_{DS} is drain-source voltage at turn-off, which is the input voltage equal to 600 V. For a damping constant of 1.0, the snubber capacitance is 10.6 nF, so the energy stored in the snubber capacitors at turn-off is 1.9 mJ. The loss dissipated in the snubber resistor is almost equal for the upper and lower resistor, indicating a similar charge and discharge transition for the upper and lower snubbers. Part of the snubber loss occurs as the capacitor is charged at turn-off, and we see that the energy stored in the capacitor at for example a damping constant of 1.0 is smaller than the total snubber loss, so it is clear that some of this energy is dissipated elsewhere in the circuit. We see that the turn-on loss of the lower MOSFET increases significantly with the damping constant, partly due to the increase in voltage fall time and subsequently an increase in switching interval, and partly due to dissipation of snubber capacitor energy.

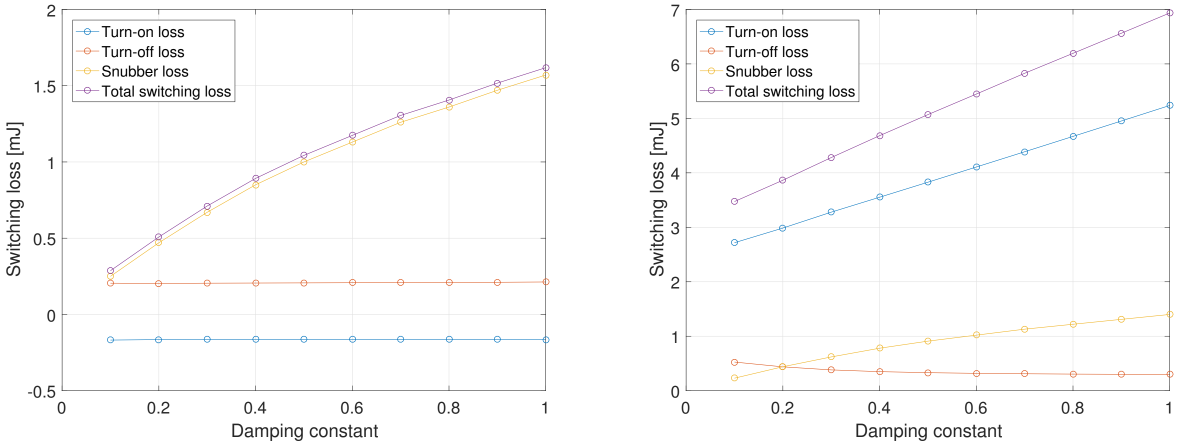


Figure 5.10: Switching losses in MOSFETs with RC-snubber. Left: Upper. Right: Lower.

The switching waveforms of the upper part of the module can be seen in figure 5.11, when a turn-off snubber with a 0.4 damping constant was used. Already for this small level of damping, the voltage ringing of the upper MOSFET is almost eliminated.

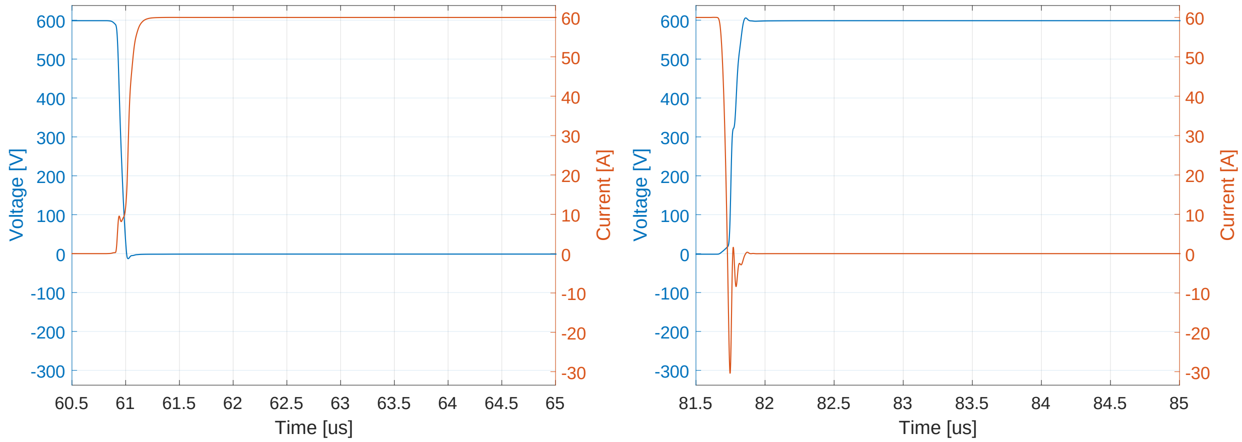


Figure 5.11: Waveform of upper MOSFET using RC turn-off snubber with 0.4 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

Figure 5.12 shows the switching waveforms of the lower MOSFET. A slight voltage overshoot at turn-off can still be observed, however it is reduced considerable compared to the overshoot seen in the base case circuit. While the rise time of the voltage is increased with the turn-off snubber, the overlap between current and voltage being non-zero is reduced, explaining the reduction on turn-off loss.

The current overshoot at turn-on consists of two peaks, almost at identical levels for a damping constant of 0.4. The first peak corresponds to the negative current spike seen in the simultaneous turn-off of the upper part of the module, caused by the reverse recovery current of the diode, which was discussed in section 5.3.1. The second peak, not seen in the waveforms of the base case circuit, is caused by the discharge of the snubber capacitor. The discharge current of this capacitor is given by

$$i_C = C\frac{dv_C}{dt}, \tag{5.3}$$

and as expected the discharge current is largest when the voltage fall is at its steepest. The first peak is not affected in a significant degree by the damping constant, which can be seen from the additional waveforms provided in appendix D.1. Since the snubber discharge current gives a higher peak than the reverse recovery current for damping constants above 0.4, the snubber have a damping constant lower than this if it is considered critical to reduce the current overshoot.

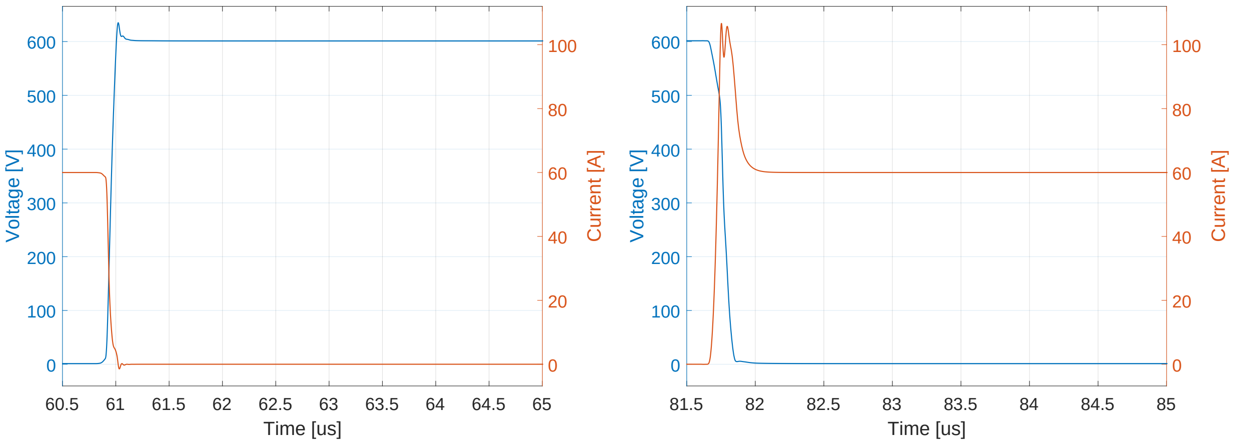


Figure 5.12: Waveform of lower MOSFET using RC turn-off snubber with 0.4 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

5.4.4 Results with DC-Snubber

Table 5.5 shows the voltage and current overshoot measured in the simulation results, as well as the calculated damping constant for the voltage across the lower voltage, for different damping constants. The damping constant of the voltage across the upper MOSFET is not presented for the same reason as in the previous section, namely that the voltage overshoot and ringing is too small to reasonable calculate. As seen from the table, the voltage overshoot across the upper MOSFET is reduced to zero for higher damping constants. The voltage overshoot across the lower MOSFET is not reduced significantly however, as for the current overshoots.

Table 5.5: Switching characteristics with DC snubber

Damping	$\hat{V}_{up}$[V]	$\hat{I}_{up}$[A]	$\hat{V}_{lo}$[V]	$\hat{I}_{lo}$[A]	α_{lo}[Ms^{-1}]
0.1	617.95	72.95	709.33	94.67	6.36
0.2	610.29	72.35	707.88	94.29	8.98
0.4	599.99	71.25	704.78	93.61	14.0
0.8	598.69	69.58	699.67	92.62	21.4
1.0	598.69	68.98	697.63	92.26	22.8

It is clear form the table that while the voltage overshoot across the lower MOSFET is only marginally reduced, the damping of the voltage ringing is increased by several factors. The damping without any snubber was shown to be 3.8 Ms^{-1} in table 5.2, and the damping factor is increased to 22.8 Ms^{-1} for a damping constant of 1.0. This is equivalent to a reduction in time constant from 263 ns to 44 ns.

The switching times and switching losses calculated for the MOSFET module does not show any significant change by introducing DC-snubber into the circuit. Both the switching times and the losses vary slightly up and down, without showing any clear trend, as the damping constant of the DC-snubber is increased. The plots of these characteristics are therefore omitted here. The power loss dissipated in the DC-snubber increases from 7 μJ to 31 μJ for DC-snubber damping constants between 0.1 and 1.0, and is thus negligible compared to the losses dissipated in the MOSFET module.

The switching waveforms of the upper and lower part of the module are shown in figures 5.13 and 5.14 respectively, using a DC-snubber with damping constant 1.0 at a 60 A load current. From the waveform it is evident that the ringing of both voltages and currents are greatly reduced, while the rising and falling edges remain mostly unchanged compared to the base case waveforms provided in figures 5.4 and 5.3 in section 5.3.1.

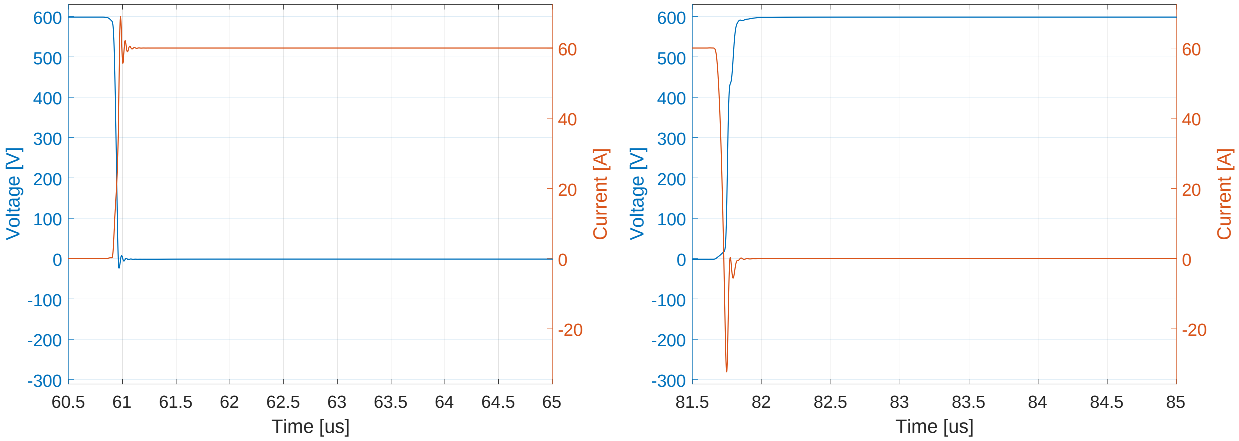


Figure 5.13: Waveform of upper MOSFET using DC-snubber with 1.0 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

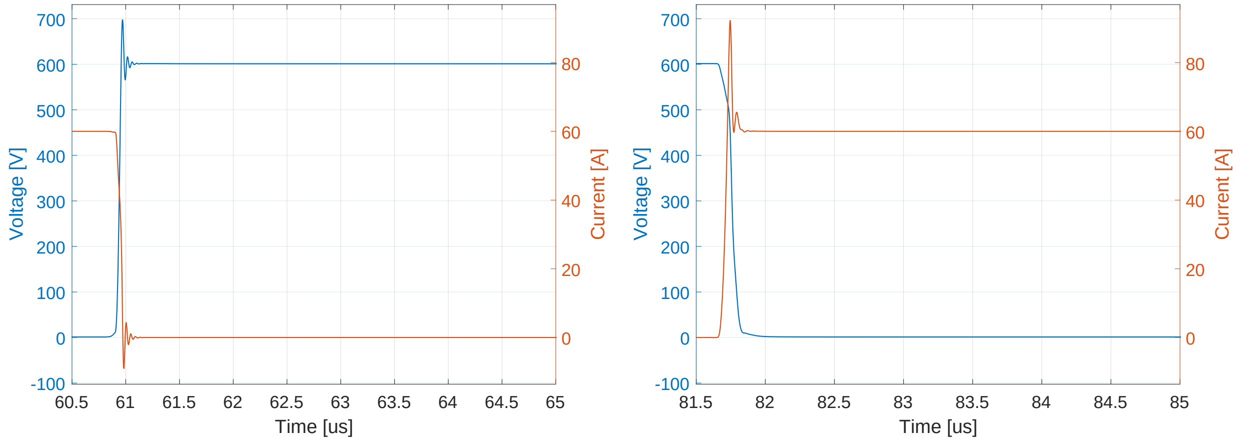


Figure 5.14: Waveform of lower MOSFET using DC-snubber with 1.0 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

Due to the improvements in ringing and overshoot provided by the DC-snubber, without any impairment on the switching losses, the DC-snubber can be considered a good option for reducing the negative effects caused by fast switching of the SiC MOSFET module.

5.4.5 Results with RC Turn-Off Snubber and DC-Snubber

Based on the results of the previous section, where it was shown that the DC-snubber does not cause increases in switching losses, even for large damping constants, it was decided to use a DC-snubber with a damping constant of 1.0 in combination with different RC turn-off snubber variations. The simulations were performed as for the turn-off snubbers alone, where the turn-off snubber damping was varied from 0.1 to 1.0 for a load current of 60 A.

An excerpt of the voltage and current overshoots measured for different turn-off snubber dampings are shown in table 5.6. Comparing these results with the results from using a pure turn-off snubber, presented in table 5.4, shows that combining the DC-snubber with a turn-off snubber does not improve the characteristics of using a pure turn-off snubber significantly. When the damping constant of the turn-off snubber is lower than 0.4, the current overshoot is slightly lower than what was observed using a pure turn-off snubber. This is because the DC-snubber lowers the reverse recovery current slightly, and the discharge current peak from the turn-off snubber does not exceed this current peak.

The switching times and switching power of the DC-snubber and turn-off snubber combination are shown in figure 5.15 and 5.16 respectively. It is observed that these characteristics are essentially unchanged from the ones seen with just a turn-off snubber, provided in figure 5.9 and 5.10. This is expected, since the DC-snubber did not change the switching time and switching loss of the MOSFET module to any significant degree.

Table 5.6: Switching characteristics with DC and turn-off snubber

Damping	$\hat{V}_{up}$[V]	$\hat{I}_{up}$[A]	$\hat{V}_{lo}$[V]	$\hat{I}_{lo}$[A]
0.1	598.69	60.03	669.16	95.14
0.2	599.87	60.03	646.68	97.94
0.4	606.42	60.02	631.81	104.22
0.8	617.24	60.02	627.45	135.92
1.0	621.74	60.02	626.35	150.41

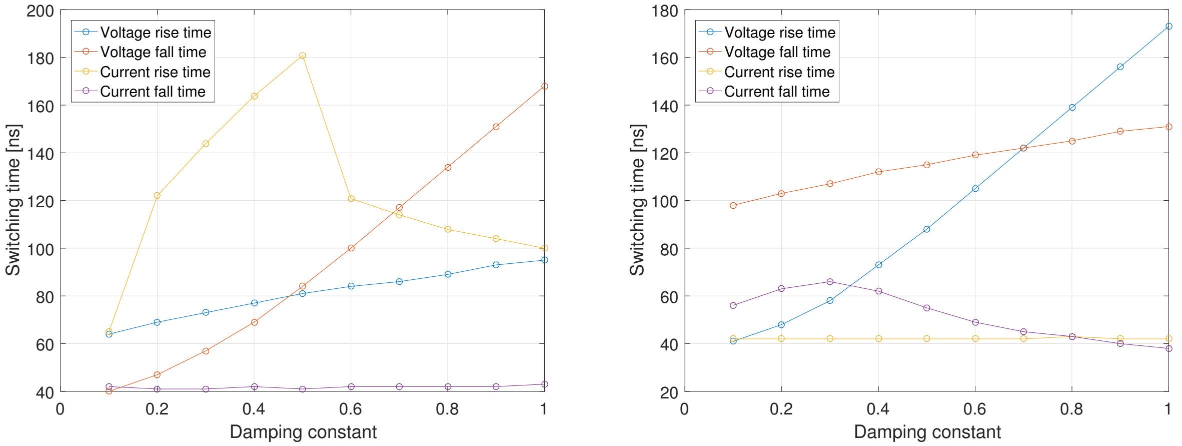


Figure 5.15: Switching times of the MOSFETs with RC turnoff-snubber and DC-snubber. Left: Upper. Right: Lower.

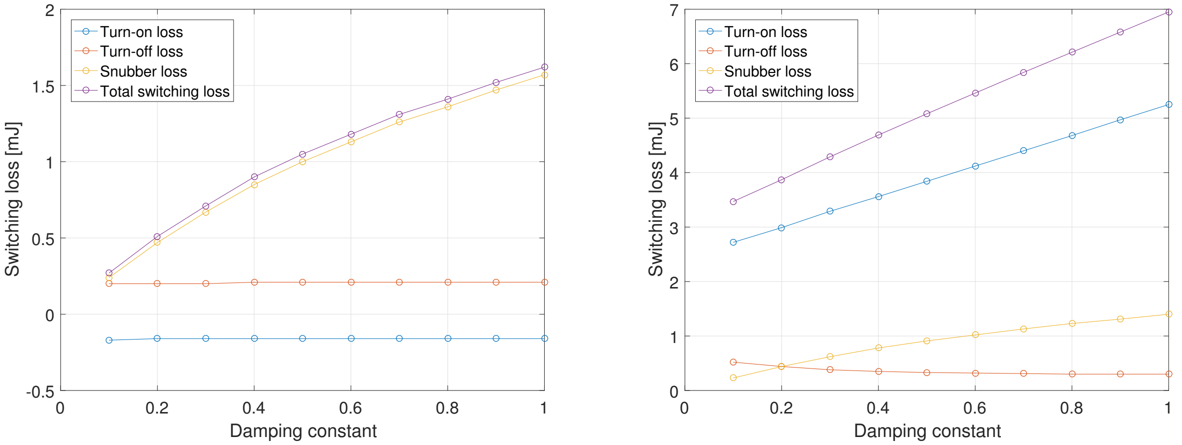


Figure 5.16: Switching losses in the MOSFETs with RC turnoff-snubber and DC-snubber. Left: Upper. Right: Lower.

The waveform of the lower MOSFET is shown in figure 5.17, for a turn-off snubber with damping constant 0.4 at 60 A output current. As the characteristics presented above suggests, the waveform is more or less indistinguishable from the waveforms shown for the turn-off snubber with the same damping constant. This is also the case for the upper MOSFET, and the waveform here is therefore omitted.

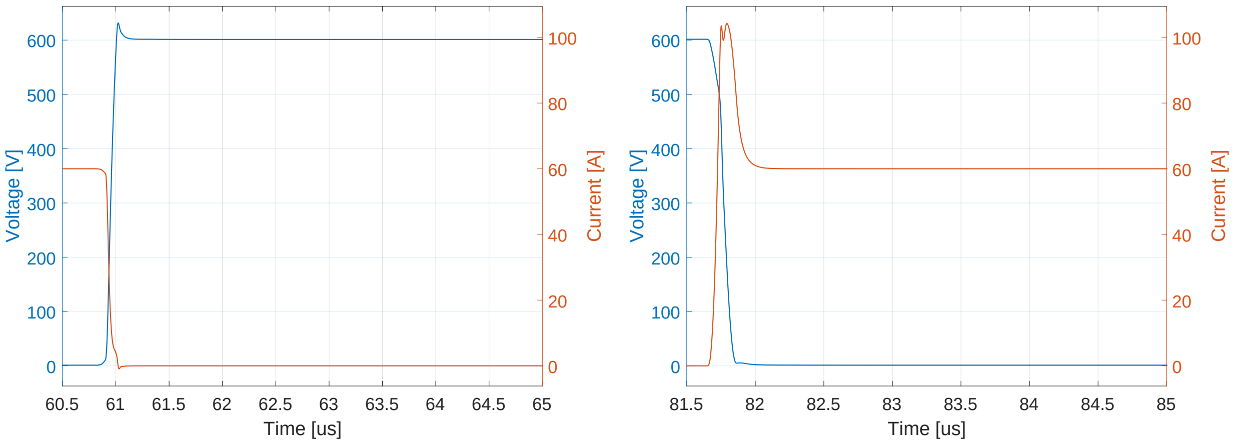


Figure 5.17: Waveform of lower MOSFET using DC-snubber with 1.0 damping constant; 60 A load current. Left: Turn-off. Right: Turn-on.

From the results presented in this section, it is clear that adding a DC-snubber with the turn-off snubbers does not add any significant improvements over the characteristics observed from the simulation results using only turn-off snubbers. The reason is the turn-off snubber affects the ringing and voltage to a larger degree than the DC-snubber, the DC-snubber does not seem to be able to give any additional benefit to these characteristics, with the turn-off snubber present.

5.5 Discussion of Results

The simulation results that have been presented in this chapter show that the half-bridge MOSFET module experiences extensive ringing and overshoot, when being hard-switched. Using the stray inductance value that was calculated from the laboratory double-pulse test, the DUT showed a voltage overshoot of 110 V above the DC-voltage of 600 V for the target output load current of 60 A. The reverse recovery current of the freewheeling diode also gives a large current spike through the lower MOSFET when it is being turned on.

It was showed that with the use RC turn-off snubbers, the voltage overshoot could be reduced to a minimum of 28 V without any voltage ringing present. The introduction of turn-off snubbers reduces the turn-off switching loss slightly, due to a smaller overlap between the voltage and current. The turn-on losses, however, double with a turn-off snubber with damping constant 1.0, as a result of increased switching times, and snubber capacitor discharge. This causes an overall increase in losses.

The use of DC-snubbers was shown to provide a reduction in voltage ringing, but the voltage overshoot could not be reduced to less than 98 V. Since the voltage overshoot is still significant with the use of DC-snubbers, the DC-snubber was not considered sufficient to reduce the problems caused by fast switching. As the DC-snubber provides some benefit without introducing additional switching losses, it was investigated whether a combination of DC-snubber and RC turn-off snubbers could improve the performance compared with either one of them. Here it was observed that the characteristics matched those observed for a pure turn-off snubber solution.

As the combination of turn-off snubber and DC-snubber did not appear to provide any significant benefits over a single turn-off snubber solution, a pure RC turn-off snubber will probably be the preferred solution in the end, since the use of DC-snubbers is not sufficient in improving switching performance. The simulation results should be compared to the physical tests done in the laboratory, to see whether the analysis done here holds. This comparison is done in the following chapter.

The switching times of the turn-off snubber showed some artifacts in the trend for increasing damping constants. This was explained in section 5.4.3, where it was shown that the odd behavior was caused by the definition of switching times used in the Python program doing the calculations. Since the main reason for calculating switching times is the evaluation of dv/dt and di/dt in the circuit, a better way to calculate the switching times could be to iterate over the voltage and current data, find the steepest point, and use the slope here to calculate a switching time. These switching times could then easily be used to calculate maximum dv/dt and di/dt.

Chapter 6

Experimental Analysis of SiC MOSFET Module Performance

6.1 Methodology

The laboratory setup used in the experimental double-pulse tests was presented in chapter 4. This chapter included an explanation of the double-pulse test used in the tests, and a description of the measurement procedures used to obtain data in the tests. The measurement data was analyzed through the use of MatLab and the Python analysis program, that was also used to calculate switching characteristics of the simulation data. All scripts can be found on GitHub [35], where the source code of the simulation analysis program can also be found.

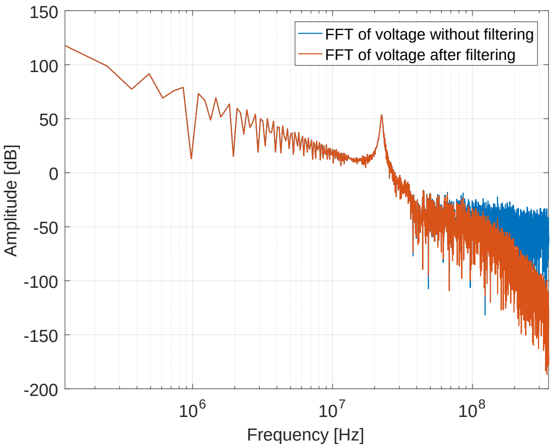


Figure 6.1: Fourier transforms of the voltage signal, before and after filtering, measured at a 54 A output current.

The raw oscilloscope data contains quite a lot of noise, which should be filtered away before any further calculations are done. This was done using a second order Butterworth low-pass filter in MatLab. The cutoff frequency was chosen to 100 MHz, which well above the bandwidth frequency of all probes used to obtain the measurements. The Fourier transforms of the voltage data before and after filtering can be seen in figure 6.1, and we see that only high frequent noise is attenuated. The interesting ringing dynamics occurring at 22.5 MHz remain unchanged from the filtering.

The current probe showed a current bias in the turn-off interval of the double-pulse test. The current bias was usually in the order of a couple of amperes. The current bias is caused by the current probe integrator not being fully calibrated to zero between each test. The current bias was removed in the script by calculating the average current in the turn-off interval, and subtracting this average value from the current data.

After the raw data was filtered, and the current bias removed, the switching characteristics were calculated using the same analysis program as was used to do the calculations on the simulation results. This was done automatically by the MatLab script calling the appropriate Python functions of the analysis program. The analysis program was thoroughly documented in the project report [1]. The calculated switching characteristics are presented in the following.

6.2 Laboratory Results With Base Circuit and Current Variation

6.2.1 Switching Characteristics

The voltage overshoot, current overshoot and voltage ringing characteristics measured for the DUT are shown in table 6.1. Comparing table 6.1 with the corresponding table 5.2 that was presented in section 5.3.2, we see that the ringing frequencies match reasonable well, in particular for 60 A, which is the current for which the stray inductance was calculated. The damping measured in the laboratory experiments is smaller however, and the voltage overshoot is larger, so while the ringing frequency is the same for the experiment measurements and simulation results, a more extensive ringing is experienced in the lab. The current overshoot is smaller than what was measured in the simulations, however a significantly high current peak is still experienced.

Figure 6.2 shows the measured switching times from the experimental double-pulse test, for different output currents. These measurements are showed in a solid line. The simulation switching times given similar circuit parameters, previously presented in section 5.3.2, are shown in the same plot with dashed lines, but same color for the same switching time.

The plot of the switching times shows that the turn-on times in the simulation are smaller

Table 6.1: Switching characteristics

I_{out}[A]	$\hat{V}$[V]	$\hat{I}$[A]	f[MHz]	α[Ms^{-1}]
27	683.56	49.86	22.36	2.33
54	857.31	79.23	22.36	2.57
81	992.70	107.15	22.29	2.31

than the ones observed in the laboratory. The turn-off times are larger for the simulation measurements. The deviation is about 10 ns for all switching times, except for the voltage fall time, where the deviation increase to about 20 ns for the higher load currents.

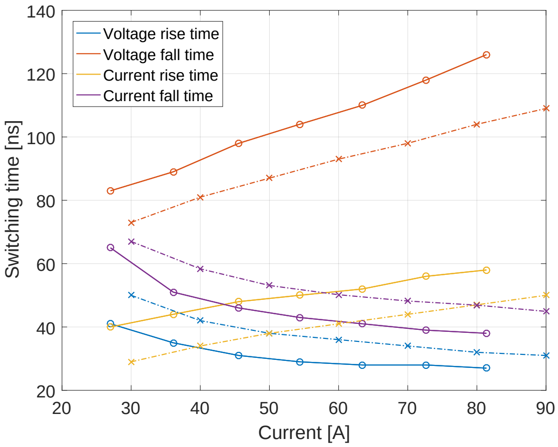


Figure 6.2: Switching times of the MOSFETs in base case. Solid lines show laboratory results, dashed lines are from the simulations.

The deviations could be caused by a deviation in the value of the gate resistances used in the gate driver in the laboratory, and the resistances that were deployed in the simulations. This seems unlikely however, as the gate resistances were thoroughly tested in the laboratory setup. Another possible factor causing the error could be a difference in the edge times of the pulses being fed from the interface board to the gate driver, and the pulse from the voltage sources in the simulation. The errors could be caused by different rising edges of the actual voltage and current waveforms, where distortions cause problems with the switching time definition, in the same way as was discussed in section 5.4.3.

The switching losses are plotted in figure 6.3, where as for the swathing item the solid lines show the results from the laboratory, and the dashed lines show the simulation results. Here we see that the turn-on losses are equal for laboratory experiment and simulations, though with a slight deviation for the higher currents. The turn-off loss shows a larger deviation, increasing up to about 1 mJ, for a load current of 80 A.

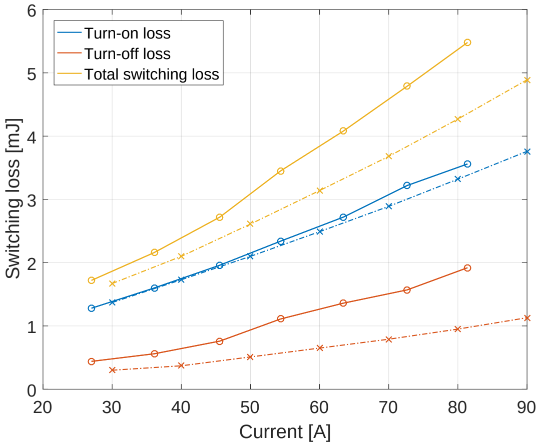


Figure 6.3: Switching losses of the MOSFETs in base case. Solid lines show laboratory results, dashed lines are from the simulations.

6.2.2 Switching Waveform Evaluation

The switching waveforms of the DUT at a 60 A load current are shown in figure 6.4, for both the simulation and laboratory measurements. The results from the laboratory are plotted in a dashed line, and the simulation results are plotted with the solid lines. Equation (4.1) was used to calculate the double-pulse timing intervals. However, the values presented in section 4.2.1 were revealed to be slightly off, so the currents in the simulation and laboratory waveforms do not match perfectly.

Even though the switching times differ somewhat, as was seen in figure 6.2, the rising and falling edges in the results follow similar trajectories in the simulation and laboratory results. As was discussed in the beginning of this section, the most critical deviation between the simulations and the laboratory experiments is the overshoots in voltage and current occurring at turn-off. As was discussed, the frequency of the oscillations matches reasonably however, and this can be observed in the switching waveforms as well.

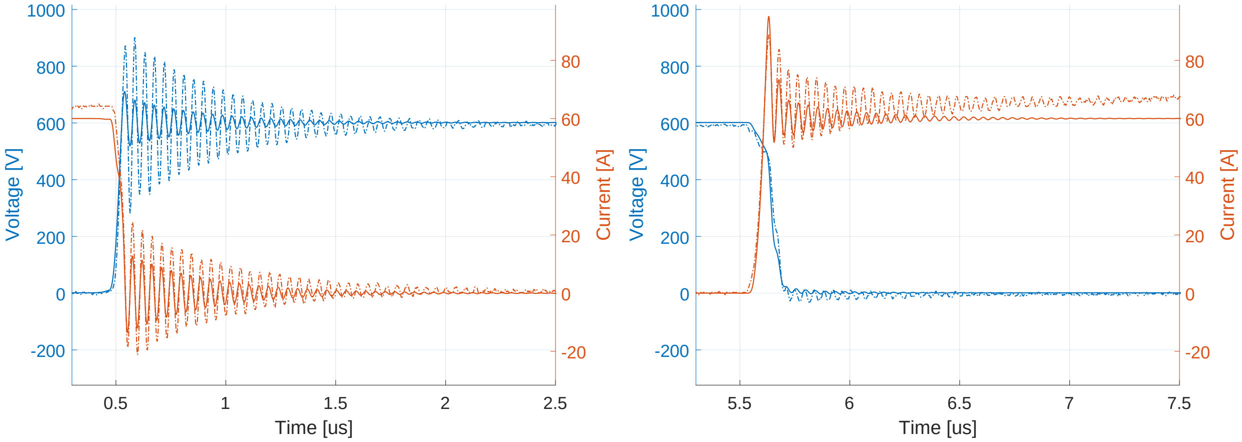


Figure 6.4: Basecircuit results at 60 A. Left: Turn-off. Right: Turn-on. Dashed lines show laboratory results, solid lines are from the simulations.

The turn-on transition from the simulation matches the laboratory results good, though the laboratory current has a slightly smaller damping constant, and thus dies out slower. Some of the deviation in the turn-on current transition can be explained by the smaller simulation current, and the fact that the output current continues to rise in the double-pulse test used in the laboratory. However, it is likely that errors in the simulation circuit model also contributes to the deviations observed at turn-on.

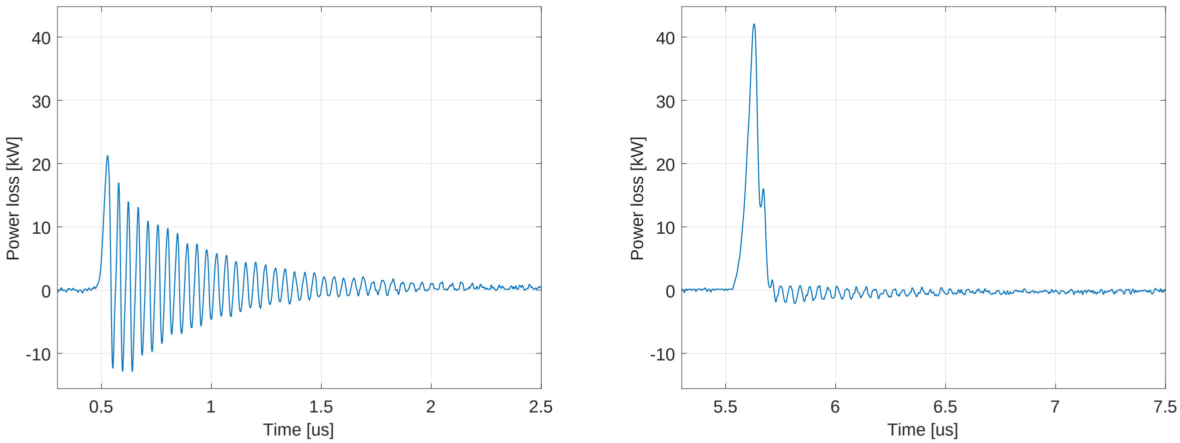


Figure 6.5: Power loss in DUT at 60 A. Left: Turn-off. Right: Turn-on.

The significant increase in ringing in the turn-off transition, observed in the laboratory, influences the switching power loss as well. As can be seen in figure 6.5, the switching power oscillates heavily at turn-off. Integrating the power from the first half period of the ringing has passed, i.e when the current first oscillates below zero, until the ringing dies out, shows a positive power loss of 0.8 mJ. The power loss in the same interval for the simulation waveforms is 50 μJ. Figure 6.3 shows that the difference in turn-off power loss between simulation and laboratory is about 0.7 mJ, and hence the difference in ringing amplitude largely accounts for the difference in turn-off power loss.

From figure 6.5 it can also be seen that most of the power is lost before the current ringing occurs at turn-on. The switching trajectories in the simulation and laboratory are very similar at turn-on, explaining the small deviation in turn-on loss.

The simulation and laboratory switching waveforms measured using an output current of 80 A are compared in figure 6.6. An even larger difference in ringing at turn-off can be seen here, which is consistent with the increasing deviation between the turn-off losses, for increasing currents, seen in figure 6.3.

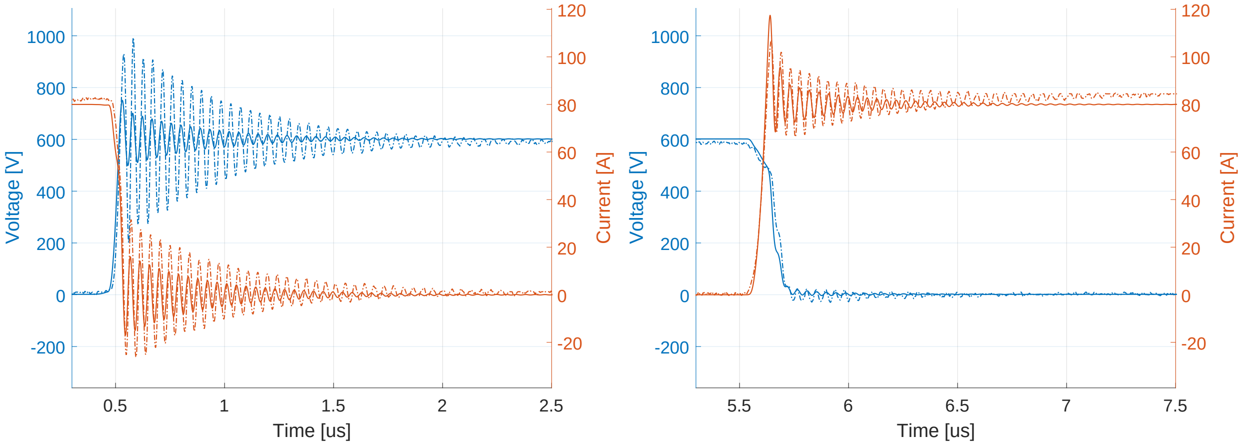


Figure 6.6: Basecircuit results at 80 A. Left: Turn-off. Right: Turn-on. Dashed lines show laboratory results, solid lines are from the simulations.

There could be several reasons for the large deviation in ringing, between simulation and experimental results, seen in the switching waveforms. One reason is that the stray inductance could be inaccurately modelled in the simulation circuit. This was discussed more in depth in section 4.4, where the impedance measurements of the DC-buses were presented. The impedance measurements showed that the inductance varies with frequency, which is not accurately modelled in the simulation model. In addition to this, it could be that the internal inductance of the MOSFET module is not accurately modelled in the simulation model provided by ROHM. Another possible reason for the deviations, could be measurement errors created by too large loop inductance of the voltage probes. Significant deviations are seen in the current measurements as well however, making measurement errors a less likely cause.

6.3 Turn-off Snubber Evaluation

Laboratory tests were done with turn-off snubbers with two different damping constants, namely 0.4 and 0.85. The reason why so few test were done was the limited availability of low inductive snubber resistors. The results from the test are presented in separate sections, and the results are compared with the simulation results for equivalent conditions.

For both snubbers the switching waveforms of the voltage and currents show larger oscillations than what was observed in the simulations, however the trajectories are similar. Both snubbers provide a voltage overshoot about equal to the overshoots observed in the simulation results, and the snubber capacitor discharge current influence on the current overshoot is less than in the simulations.

6.3.1 Turn-Off Snubber with Damping Constant 0.4

The switching times of the DUT are shown in figure 6.7. The rise times show little deviation compared to the simulation results. The fall times show larger differences compared with the simulation results, and in particular the current fall time, which has a deviation of about 200 ns at an output current of 30 A. This large difference can be explained by considering the plots of the switching waveforms measured at 64 A load current, shown in figure 6.9. Here we see that the current plateaus on the falling edge, around 30 A, before continuing to fall with the same slope as before the plateau. The deviation in voltage fall time can be accounted for by the distortions seen in the voltage on the falling edge.

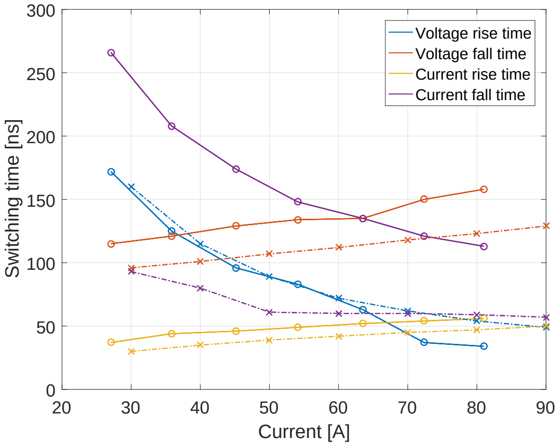


Figure 6.7: Switching times of the DUT at varied output current. Solid line is laboratory results, and dashed line is simulation results.

The switching losses are plotted in figure 6.8, where the solid lines show the laboratory results and the dashed lines show the results from the simulations. As expected, a large deviation can be seen for the turn-off loss, cased by the much larger overlap between voltage and current due to the current plateauing on the falling edge. The turn-on loss shows a slight deviation as well, though a beneficial one, as the turn-losses observed in the laboratory results are lower than what could be expected from the simulations. The main reason for this reduction in turn-on loss is the reduced current overshoot at turn-on, seen in figure 6.9.

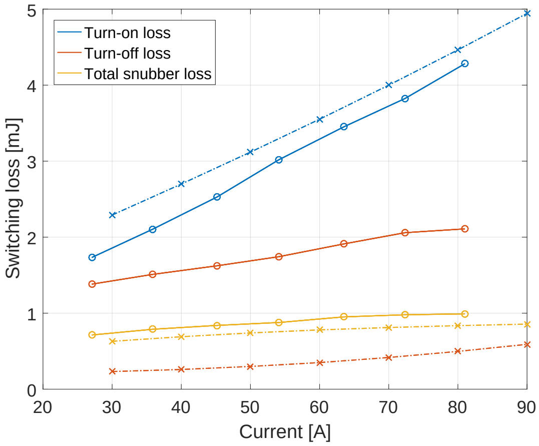


Figure 6.8: Switching losses of the DUT at varied output current. Solid line is laboratory results, and dashed line is simulation results.

Figure 6.9 presents a comparison between the voltage and current waveforms of the lower MOSFET, measured in the laboratory test and simulation test, for a load current of 64 A. The dashed lines show the laboratory results, and the solid lines show the simulation results. High frequent oscillations can be seen in both voltage and current waveforms, creating distortions on the rising and falling edge of the drain-source voltage. The current also has oscillations on the current overshoot associated with the snubber capacitor discharge current, however, as mentioned above, the overshoot is not as severe as the one observed in the simulations results. The voltage overshoot of the laboratory waveform is about the same as in the simulations, though the ringing is not eliminated to the same degree as in the simulation results.

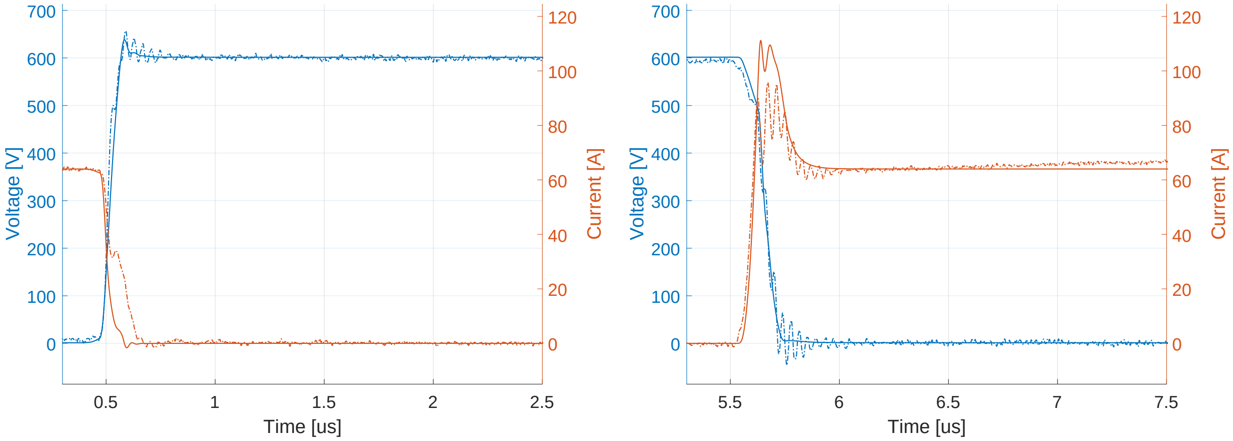


Figure 6.9: Simulation and lab comparison with 0.4 turn-off snubber at 64 A. Left: Turn-off. Right: Turn-on. Dashed lines show laboratory results, solid lines are from the simulations.

6.3.2 Turn-Off Snubber with Damping Constant 0.85

The switching times and switching losses calculated form the laboratory test results are plotted and compared with the simulation results in figure 6.10 and 6.11 respectively. The same deviations as was seen for the previous turn-off snubber can be seen here. The current fall time is increased significantly by the plateau on the falling edge, and this also causes a large deviation in the turn-off loss.

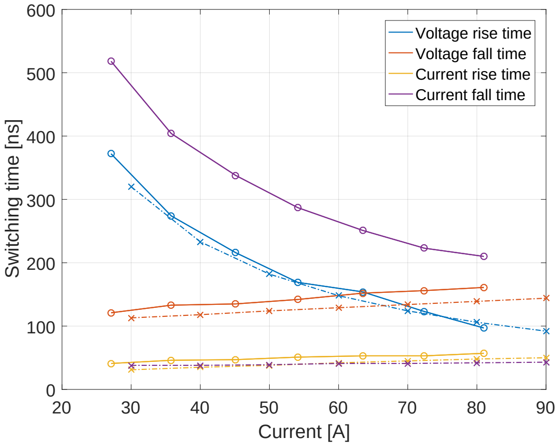


Figure 6.10: Switching times of the DUT at varied output current. Solid line is laboratory results, and dashed line is simulation results.

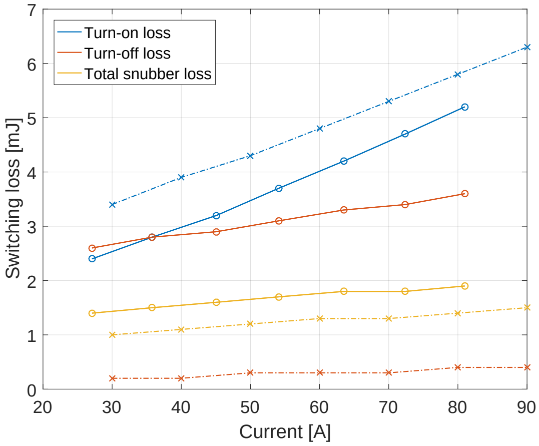


Figure 6.11: Switching losses of the DUT at varied output current. Solid line is laboratory results, and dashed line is simulation results.

The switching waveforms are shown in figure 6.12, again at a load current of 64 A. A longer lasting plateau can be seen in the current at turn-off, than for the results with the turn-off snubber with lower damping, and the voltage oscillations seen on the rising and falling edges can be observed to have magnified. The voltage overshoot is still comparable to the voltage overshoot in the simulation test, though a slight ringing action is occurring.

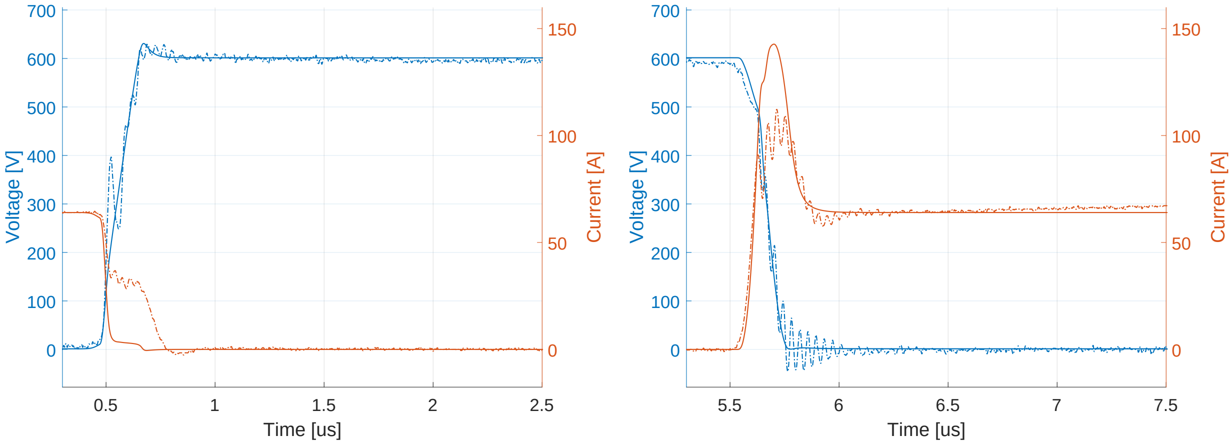


Figure 6.12: Simulation and lab comparison with 0.85 turn-off snubber at 64 A. Left: Turn-off. Right: Turn-on. Dashed lines show laboratory results, solid lines are from the simulations.

6.4 DC-snubber

The simulations showed that the switching losses did not increase with the damping of the DC-snubber, so it was decided to perform double-pulse tests with a DC-snubber a resistance of 3.3 Ω and capacitance of 13.3 nF. This corresponds to a damping constant of 1.3. The voltage and current characteristics from the test are shown in table 6.2. Here it is observed that the DC-snubber does not provide the same level of damping as was seen from the simulations, however for higher currents the voltage overshoot is reduced significantly.

Table 6.2: Switching characteristics

I_{out}[A]	$\hat{V}$[V]	$\hat{I}$[A]	f[MHz]	α[Ms^{-1}]
27	682.7	50.0	23.3	2.9
54	811.3	79.5	23.0	2.5
81	919.4	106.0	22.8	2.9

The switching times when the DC-snubber was included are shown in figure 6.13. The switching times calculated from the results without any snubber, previously shown in figure 6.2, are also plotted and shown with a dashed line. The only significant change in switching time can be observed for the voltage fall time, which is reduced slightly when the DC-snubber is included.

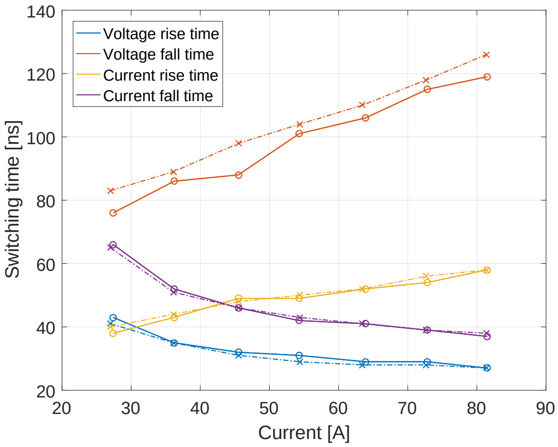


Figure 6.13: Switching times of the DUT with DC-snubber.

Figure 6.14 shows the switching losses calculated from the results with the DC-snubber. Here we see that the turn-off loss is reduced, in particular for higher currents. This is caused by the reduction in voltage fall time, and reduced ringing. As was discussed in section 6.2.1, the laboratory tests show a much higher voltage overshoot and ringing than in the simulations, and a significant portion of the turn-off losses occur in the interval of the ringing action in the laboratory results, as opposed to what was observed in the simulations. A reduction in the ringing will therefore also have a significant effect on the turn-off losses, contrary to what was observed when the DC-snubber was introduced into the simulation circuit.

The losses dissipated in the DC-snubber resistor were calculated to be maximum 0.1 mJ, for the highest currents. This is higher than in the simulations, however still small enough to be considered negligible.

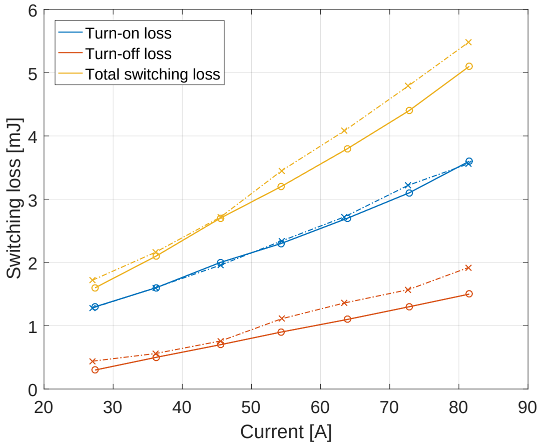


Figure 6.14: Switching loss in DUT using DC snubber.

Overall the DC-snubber has a positive impact on the switching characteristics in the circuit, as both ringing and overshoot is reduced, in addition to switching losses. The switching waveforms of the DUT at a 60 A load current, with the DC-snubber included in the circuit, can be seen in figure 6.15. The voltage overshoot and ringing is still extensive, and the use of does not seem to be a viable choice in the effort to reduce EMI problems.

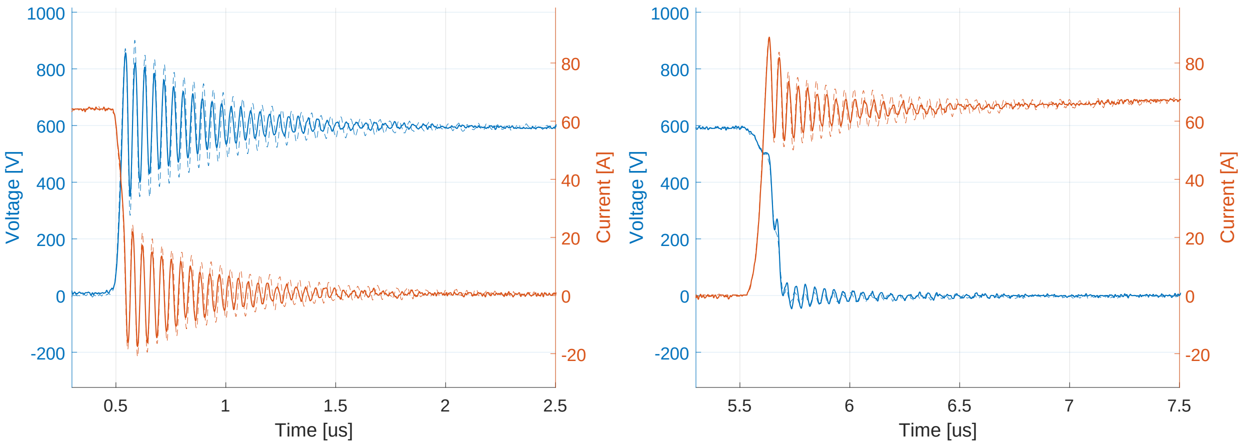


Figure 6.15: DC-snubber results at 60 A. Left: Turn-off, right: turn-on.

6.5 Summary and Discussion of Results

This chapter has presented the results from the experimental double-pulse tests with the 120 A-module. It was shown that the switching characteristics seen in the experiments match the simulation results to a varying degree. In general the switching trajectories were comparable in the simulation and experimental results, but the more extensive ringing and overshoots observed in the lab caused large deviations in some of the switching characteristics. The most important reason for this is likely an inaccurate stray inductance model in the simulations.

In the simulations it was shown that such a combination does achieve any increase in switching performance, compared with the less complex solution of using pure RC turn-off snubbers. Because the DC-snubber did not provide the desirable reduction in ringing time seen in the simulations, it was therefore decided to not conduct the experiments where the DC-snubber was combined with a RC turn-off snubber.

The experimental results with turn-off snubbers showed that this snubber topology succeeds in improving the voltage overshoot and ringing. Additionally, the waveforms were very similar to the measurements observed in the simulation results, including similar current and voltage overshoots. The turn-off transient of the current differed quite a lot in the experiments though, increasing the total switching losses compared with the simulation results.

Chapter 7

Conclusion and Scope of Future Work

7.1 Conclusion

This Master thesis work has investigated various design and performance aspects, related to the utilization of SiC based MOSFETs in an electrical motor drive. The key aspects that were investigated are:

- The crucial components of a SiC MOSFET three phase converter was identified, and theoretical considerations investigated. Several converter system component designs were presented, including two boards for the controller/gate driver system, and a low inductive three phase DC-bus.
- An interface card was implemented on a prototype board, to enable control with an existing motor controller system from Rolls-Royce Marine. The interface card was developed for the ROHM gate drivers that can be used with the SiC modules BSM300D12P3E005 and BSM120D12P2C005. The interface card was used with the controller system, in subsequent experimental work with the BSM120D12P2C005 module.
- A piggyback board, designated for the BP59A8H evaluation gated driver from ROHM, was designed. The design was based on a complete gate driver, which was designed as part of the project work leading up this thesis, and added critical system functionality to the BP59A8H evaluation board. Because a different SiC module and accompanying gate driver were used in the laboratory work, the piggyback board did never undergo extensive testing.
- Low inductive DC-bus design was discussed, and a low inductive DC-bus bar for a three phase converter was designed and produced. The inductive characteristics of the

DC-bus were investigated through impedance analysis, and the bus bar design was shown to have good inductive capabilities compared with an existing design, namely a 75% decrease in inductance was observed.

- The stray inductance of a DC-bus for the BSM120D12P2C005 SiC module was determined through an experimental double-pulse test, and shown to be 35 nH. In addition, the stray inductance was investigated with an impedance analyzer, and the results showed an equal stray inductance in the frequency range 1 MHz - 20 MHz, however for higher frequencies the impedance analysis showed an irregular pattern in the inductance trend for increasing frequencies. It was discussed whether this could be caused by a too simplified circuit model of the DC-bus.
- The stray inductance calculations were used as a basis for computer simulations of the BSM120D12P2C005 module in the simulation program LTspice. Here it was shown that the MOSFET module experiences extensive current and voltage overshoot and ringing at hard-switching, due to the presence of stray inductance in the circuit. At the target RMS-current for the BSM120D12P2C005 module, a voltage overshoot of 110 V over the nominal DC-voltage of 600 V was measured, and the ringing had a frequency of 22 MHz and a damping constant of 3.8 Ms^{-1}. The damping constant shows that the exponential decay of the ringing has a time constant of 263 ns. For switching transition times in the range of 30 ns - 90 ns, this was considered quite extensive.
- The use of snubber circuit to improve switching performance was investigated through the LTspice simulations. Two different snubber types were tested, namely the RC turn-off snubber and the DC-snubber. The RC turn-off snubber proved to be able to reduce both voltage overshoot and voltage and current ringing, as expected from the theory. However, it was shown that the introduction of RC turn-off snubbers increases both current overshoot at turn-on, and the total switching losses. The DC-snubbers showed a good ability to reduce the time constant of the ringing, however the voltage overshoot was not reduced to a significant degree. The combination of RC turn-off snubbers and DC-snubber did not provide any significant benefits over using pure RC-snubbers. It was concluded that a trade-off must be made between the different switching characteristics, when snubber circuits are deployed. The trade-off depends on the specific use of the power converter, as both losses and converter volume will be affected by how the snubbers are dimensioned.
- The BSM120D12P2C005 module was tested in the laboratory, using the same double-pulse testing scheme as in the simulation tests. The results of the experimental tests were compared with the simulation results, both for base case circuit testing, and using snubber circuits. Several deviations in the switching characteristics were observed, but in general the characteristics matched fairly well. The snubber circuit were not as effective in the experimental tests as they were shown to be in the simulations, in particular the DC-snubber. The RC turn-off snubber reduced the voltage overshoot

and ringing to almost the same degree as in the simulations, however the turn-off loss in the experiments was shown to be significantly larger. The DC-snubber did not provide any significant improvements in switching characteristics. A reason for this could be that the stray inductance configuration in the simulation circuit with the DC-snubber deviates from the actual values in the realization of the snubber.

7.2 Scope of Future Work

The work done in this Master thesis has driven the project of developing a SiC based electrical motor drive for harsh environments forward, however several topics of investigation remains. To realize such motor drive, important parts of the continuation of the project are:

- The interface board that was developed proved useful in the experiments, as a motor controller could be used to control the experiments programmatically. The interface board was implemented using a prototype board, and in the future this card should be laid out and produced as a PCB. One possibility is to include the interface card as part of the gate driver board design that was presented in the project work [1].
- A dedicated and complete gate driver should be produced and tested with the SiC MOSFET module of choice. This driver should implement all critical functionality that was implemented on a piggyback board in this thesis work. The driver must be tested, and aspects such as EMC compliance should be investigated. This is in particular important for fast switching converters using SiC, where voltage ringing is a very relevant concern.
- The DC-bus that was designed as part of this thesis should be used in double-pulse tests, to confirm whether the lower stray inductance of the DC-bus measured in the impedance analysis affects the switching performance as expected. It is clear that the conduction dynamics from the DC-bus become more complex when the DC-bus is used in three phase operation, and it should be investigated if this influences the switching performance in unexpected ways.
- A more comprehensive investigation of the dynamics of the inductance could be performed. It was shown that the stray inductance of the DC-buses had a frequency dependence, and this was not reflected in the LTspice simulations. This is an important way the simulation model can be improved, as it was shown not to accurately reflect the voltage overshoots seen in the experimental tests. A more accurate inductance study could be done through FEM modelling in for example COMSOL.
- The experimental testing showed that the introduction of RC-snubber circuits provided a significant improvement in switching characteristics, however at the expense of switching losses. While the RC snubber types were chosen due their simplicity, other snubber topologies could be tested. As noted in the theory, turn-off snubbers could

be complimented with turn-on snubbers to reduce switching losses, and the Undeland snubber is a compact and suitable variation of this snubber topology [8] that could be explored.

- It was shown in both the simulation results, and the experimental results, that the analysis software, which calculated the switching characteristics, creates some artifacts in the calculations of the switching times. The algorithm performing these calculations should be reimplemented, so a more consistent and comparable switching time is outputted.
- The full converter system should be implemented and tested. A heat sink should be dimensioned appropriately to the converter system. It is desirable to reduce the heat sink volume, so a deeper investigation of the appropriate trade-off made between snubber damping, switching loss, and EMI performance should be made.

Bibliography

[1] J. D. Kvitvang, *Theoretical Design Aspects in the Utilization of Silicon Carbide MOSFETs for Electrical Motor Drives*, Project report, NTNU, 2016.

[2] B. Torsæter, *Evaluation of Switching Characteristics, Switching Losses and Snubber Design for a Full SiC Half-Bridge Power Module*, Master thesis, NTNU, 2016.

[3] A. Elasser, T. P. Chow, *Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems*, Proceedings of the IEEE, Vol. 90, No. 6, pp. 969 - 986, June 2002.

[4] J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, J. W. Palmour, *Status and Prospects for SiC Power MOSFETs*, IEEE Transactions on Electron Devices, Vol. 49, No. 4, pp. 658 - 664, April 2002.

[5] I. Abuishmais, T. M. Undeland, *SiC Devices for Renewable and High Performance Power Conversion Applications*, Advances in Power Electronics, Vol. 2012, p. 5, 2012.

[6] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer US, 2008.

[7] T. Kimoto, J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*, Wiley-IEEE Press, November 2014.

[8] N. Mohan, T. M. Undeland, W. P. Robbins, *Power Electronics: Converters, Applications and Design*, John Wiley & Sons, Inc., 3rd edition, 2003.

[9] P. C. Todd, *Snubber Circuits: Theory, Design and Application*, Unitrode Power Supply Seminar, SEM-900, May 1993.

[10] S. G. Jeong, M. H. Park *The Analysis and Compensation of Dead-Time Effects in PWM Inverters*, IEEE Transactions on Industrial Electronics, Vol. 38, No. 2, April 1991.

[11] M. C. Caponet, F. Profumo, R. W. De Doncker, A. Tenconi, *Low Stray Inductance Bus Bar Design and Construction for Good EMC Performance in Power Electronic Circuits*, IEEE Transactions on Power Electronics, Vol. 17, No. 2, pp. 225 - 231, March 2002.

[12] K. Y. Chen, K. G. Chen, K. Smedley, *Analysis and Measurement of small Inductance of Loops and Vias on Printed Circuit Board*, Industrial Electronics Society Conference, 29th Annual Conference of the IEEE, vol. 2, March 2003.

[13] D. Graovac, M. Pürschel, A. Kiep, *MOSFET Power Losses Calculation Using the Data-Sheet Parameters*, Application Note - Infineon, v 1.1, July 2006.

[14] ROHM Semiconductor, *SiC Power Devices and Modules*, Application Note, Rev. 1, June 2013.

[15] Toshiba, *Power MOSFET Electrical Characteristics*, Application note, November 2016.

[16] J. W. Nilsson, S. A. Riedel, *Electric Circuits*, Pearson Education, Inc., 9th edition, 2011.

[17] J. Hagerman, *Calculating Optimum Snubbers*, Hagerman Technology, 1995.

[18] E. Kreyzig, *Advanced Engineering Mathematics*, Wiley, 10th edition, 2011.

[19] ROHM Semiconductor, *Gate drive circuit board for 300A SiC Power Module*, BP59A8H Instruction Manual, January 2016.

[20] ROHM Semiconductor, *1ch Gate Driver Providing Galvanic Isolation BM6101FV-C*, Datasheet, Rev. 3, December 2015.

[21] Recom, *RxxP2xx Isolated DC/DC converter*, Datasheet, Rev. 1, 2014.

[22] Agilent Technologies, *Practical Temperature Measures*, Application Note, January 2012.

[23] ROHM Semiconductor, *SiC Power Module BSM300D12P3E005*, Datasheet, Rev. B, September 2016.

[24] Vishay, *Surface Mount Ultrafast Avalanche Rectifiers*, Datasheet, February 2015.

[25] *Generic Standard on Printed Board Design*, IPC standard 2221, February 1998.

[26] General Electric, *LEXAN FR-60, FR-63, FR-65, FR-66 FILM*, Product Data Sheet, SPD-5001, November 1998.

[27] J. Arrigo, *Input and Output Capacitor Selection*, Application Report, Texas Instruments, SLTA055, February 2006.

[28] Y. Ikeda, J. Itsumi, H. Funato, *The power loss of the PWM voltage-fed inverter*, Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE, April 1988.

[29] M. H. Bierhoff, F. W. Fuchs, *Semiconductor Losses in Voltage Source and Current Source IGBT Converters Based on Analytical Derivation*, Power Electronics Specialists Conference, 2004. PESC 04. 2004, IEEE 35th Annual, June 2004.

[30] ROHM Semiconductor, *SiC Power Module BSM120D12P2C005*, Datasheet, Rev. B, May 2013.

[31] ROHM Semiconductor, *Gate Drive Circuit Board for SiC Power Module BW9499H*, Instruction Manual, Rev. B, June 2014.

[32] S. Skogestad, I. Postlethwaite, *Multivariable Feedback Control: Analysis and Design*, John Wiley & Sons, Ltd., 2nd edition, 2005.

[33] L. W. Nagel, D. O. Pederson, *Simulation Program with Integrated Circuit Emphasis*, Memorandum No. USB/ERL M382, April 1973.

[34] C. Warwick, *Everything you always wanted to know about SPICE*, The EMC journal, Issue 82, pp. 27 - 29, May 2009.

[35] J. Kvitvang, *LTspice-cli*, GitHub Repository, https://github.com/joskvi/LTspice-cli.

Appendix A: Bill of Materials

A.1 Piggyback Board BOM

Table A.1: Bill of materials for piggyback board

Component	Id	Farnell no.
Recom DC/DC	R12P212D	2440280
Recom DC/DC	R12P205S	2440279
Vishay ultrafast diode	UF4007-E3/54	1467503
Snubber resistor 10 ohm	BPR10100J	9432442
Snubber capacitor 3.3 nF	MKP10	

A.2 Interface Board BOM

The logic gates used in the implementation of the interface board are presented in table A.2. In addition to these components, regular through-hole resistors and capacitors were used, according to the circuit schematic specification.

Table A.2: Bill of materials for interface board

Component	Id	Farnell no.
MOSFET driver	MCP14E4-E/P	1578355
NAND gates	HEF4093BP	385815

Appendix B: Zener Diode Voltage Regulation

A Zener diode is a diode which can reliable operate in the breakdown region and conduct a reverse current at a well defined reverse voltage. This can be exploited to make a simple voltage regulator. The current-voltage characteristic of the Zener diode V_Z can be approximated to follow an exponential relationship around the operating point:

$$I_Z = a \cdot e^{b \cdot V_z} + c \cdot e^{d \cdot V_z}. \tag{B.1}$$

The output voltage from the Zener diode voltage regulator should be 3 V, so a Zener diode with a 3 V Zener voltage was chosen. The iv-characteristic of this Zener diode was investigated by measuring the current through it, and voltage across it at different voltage levels. The curve fit function `fit(i, v, 'exp2')` was applied in MATLAB, which gives a curve fit consisting of a sum of two exponential functions, as in equation B.1. The curve fit gave the parameters $a = 2.436 \cdot 10^{-18}$, $b = 10.29$, $c = 9.917 \cdot 10^{-6}$, $d = 2.648$. The measurement results, with the resulting curve fit, is shown in figure B.1.

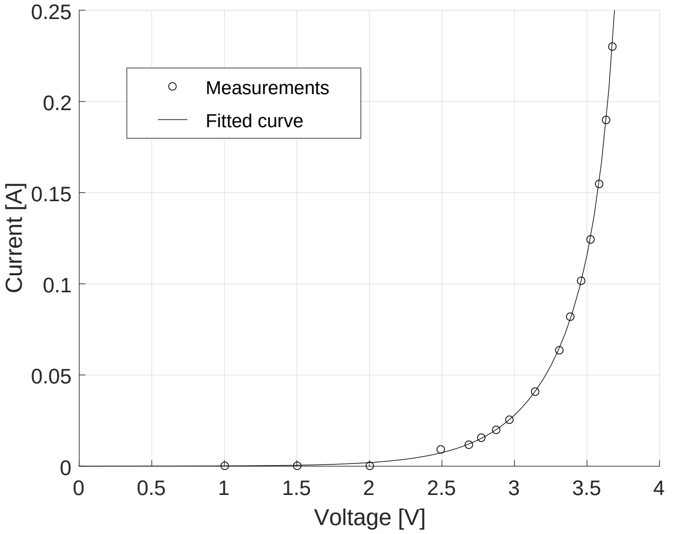


Figure B.1: iv-characteristic of Zener diode.

The circuit shown in figure B.2 can be used to create a voltage regulator. The voltage will be divided between the Zener diode and the resistor, and the resistance should thus be dimensioned so that the Zener voltage is 3 V for the appropriate output current.

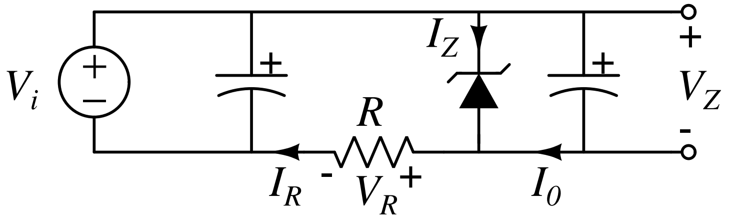


Figure B.2: Voltage regulator circuit.

The voltage V_R across the resistor R will be given by

$$V_R = R \cdot (I_Z + I_0) = V_i - V_Z. \tag{B.2}$$

The resistor R should be calculated for operation at the desired Zener voltage, when a certain current I_0 is outputted. The current I_0 is the gate current of the MOSFET when it is turned off. As was discussed in section 2.4 in the theory chapter, a charge must be removed from the parasitic gate-source and gate-drain capacitors the MOSFET to turn off. This charge, called the gate charge Q_G, is dependent on the positive bias of the gate-source voltage. For a given switching frequency f, this charge must be removed f times per second, thus giving the current

$$I_0 = f \cdot Q_G. \tag{B.3}$$

The gate charge of the MOSFETs in the modules can be found in the datasheet. The gate charge is 780 nC for a positive gate-source voltage of 19 V. With a 30 kHz switching frequency, the output current I_0 will be 23.4 mA. The resistor value that will ensure an output voltage of 3 V for driver operation at 30 kHz can now be calculated:

$$R = \frac{V_i - V_Z}{I_Z + I_0} = \frac{5\,\mathrm{V} - 3\,\mathrm{V}}{28.0\,\mathrm{mA} + 23.4\,\mathrm{mA}} = 38.9\,\Omega \tag{B.4}$$

The output voltage will increase if the output current goes down. This will be the case when the double-pulse tests are being run, since the MOSFET gates are only discharged twice for each test being run. The output current is thus essentially zero. To calculate what the output voltage will be, the following equation must be solved

$$R(I_0 + a \cdot e^{b \cdot V_z} + c \cdot e^{d \cdot V_z}) = V_i - V_z, \tag{B.5}$$

and this equation does not have an analytical solution. Numerical methods must therefore be used. Newton's method gives a fast algorithm to solve the equation [18]. For an output current of 0 mA, it was calculated that the output voltage will rise to 3.19 V. This deviation from the desired voltage level can be avoided by changing resistors between the double-pulse test, and operation at higher switching frequencies.

Figure B.3 shows how the output voltage of the regulator will vary as the switching frequency of the converter increases. For a frequency interval between 0 and 50 kHz, the voltage vary from 3.2 V to 2.7 V. This is well within the rated limits of the evaluation board and MOSFET module, given in the datasheets [19], [23].

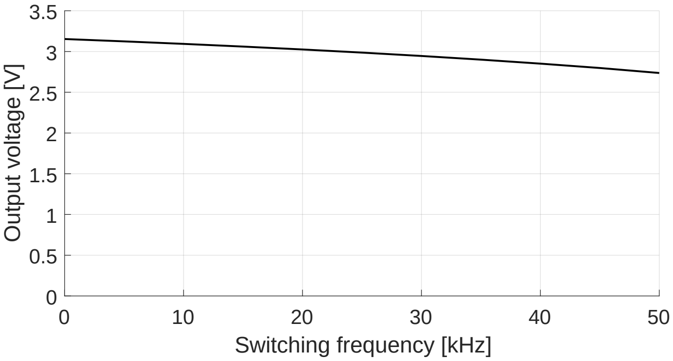
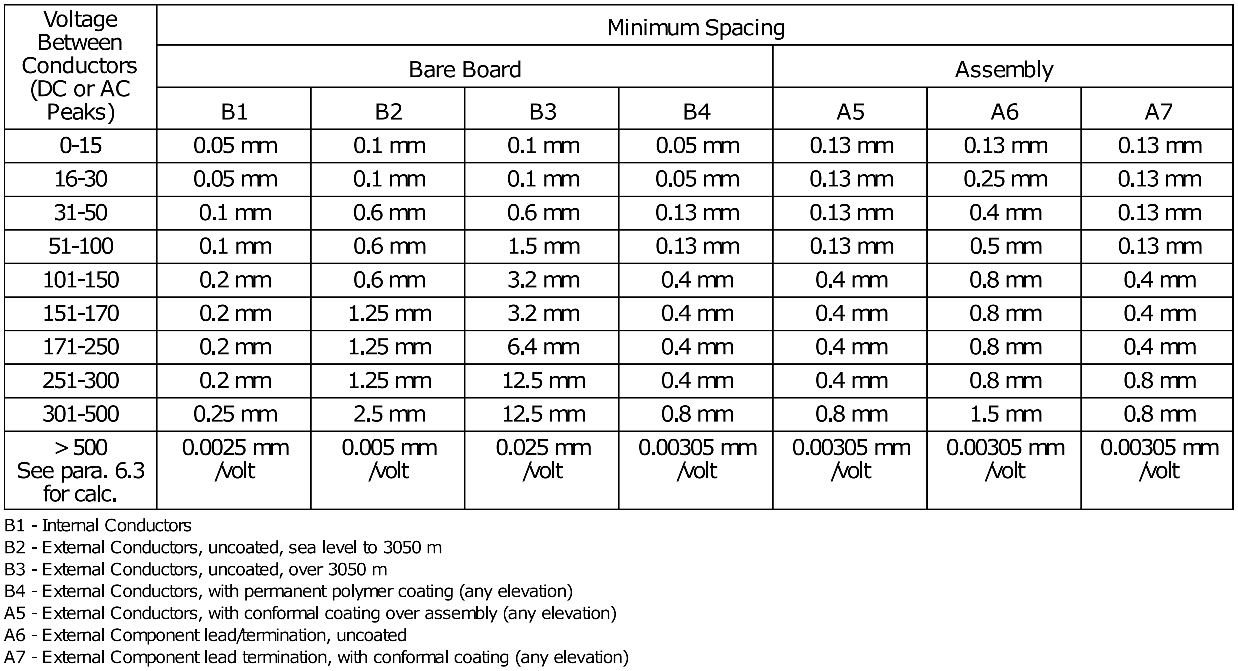


Figure B.3: Voltage output at different switching frequencies.

Appendix C: Electrical Clearance

Figure C.1 shows a table specifying electrical conductor spacing, given in IPC-2221 [25]. For this project, the relevant column is B2, showing minimum spacing between external bare board conductors, uncoated, at sea levels up to 3050 m. Many of the conductors considered in the designs in this thesis have voltages over 500 V, so for two conductors a and b with such a voltage V_{ab} between them, the electrical clearance between a and b, d_{ab} should at minimum be

$$d_{ab} = 0.005\text{mm/V} \cdot V_{ab}. \tag{C.1}$$



Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm	0.13 mm
16-30	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.25 mm	0.13 mm
31-50	0.1 mm	0.6 mm	0.6 mm	0.13 mm	0.13 mm	0.4 mm	0.13 mm
51-100	0.1 mm	0.6 mm	1.5 mm	0.13 mm	0.13 mm	0.5 mm	0.13 mm
101-150	0.2 mm	0.6 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
151-170	0.2 mm	1.25 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
171-250	0.2 mm	1.25 mm	6.4 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
251-300	0.2 mm	1.25 mm	12.5 mm	0.4 mm	0.4 mm	0.8 mm	0.8 mm
301-500	0.25 mm	2.5 mm	12.5 mm	0.8 mm	0.8 mm	1.5 mm	0.8 mm
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m
B3 - External Conductors, uncoated, over 3050 m
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated
A7 - External Component lead termination, with conformal coating (any elevation)

Figure C.1: Electrical conductor spacing, from IPC-2221 [25].

Appendix D: Additional Waveforms

D.1 Simulation Waveforms

Turn-Off Snubber

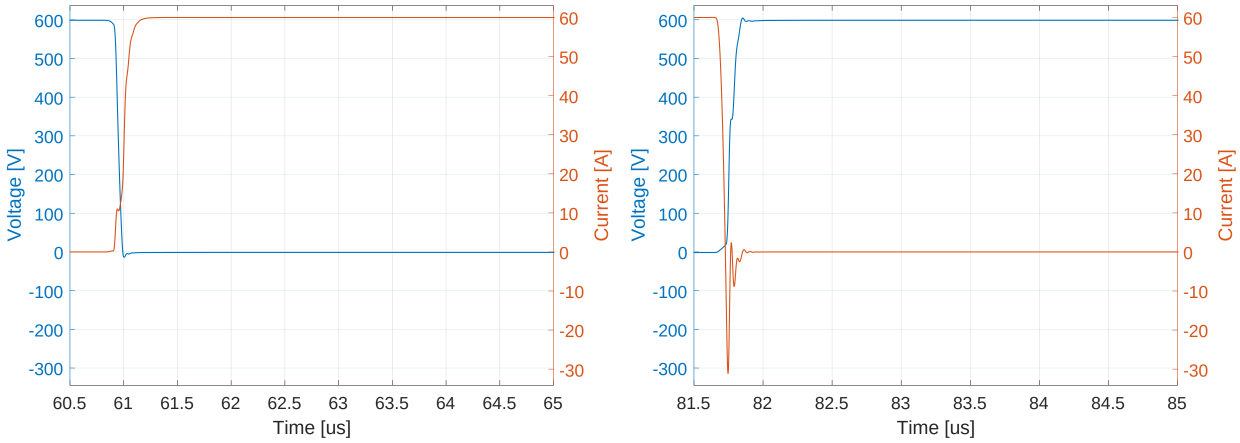


Figure D.1: Waveform of upper MOSFET using RC turn-off snubber with 0.3 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

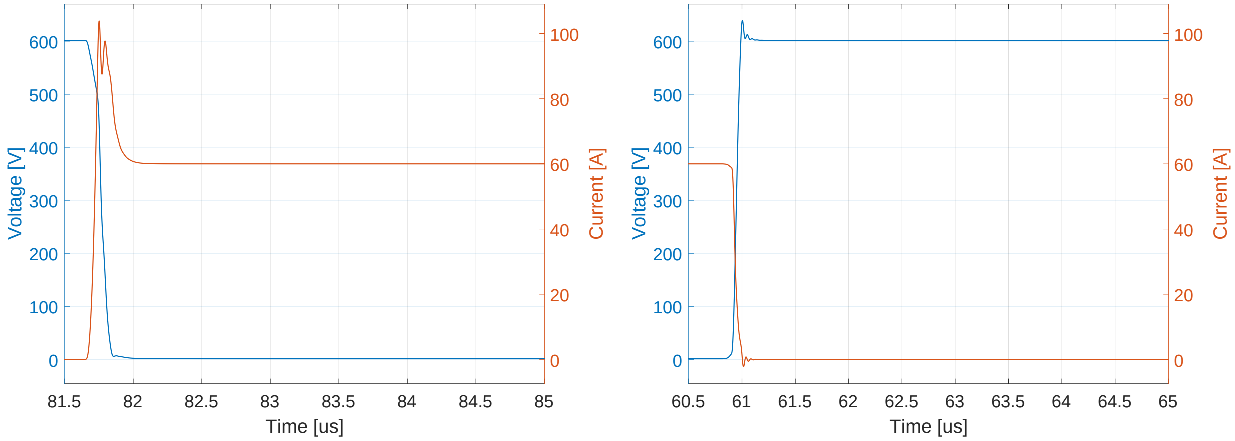


Figure D.2: Waveform of lower MOSFET using RC turn-off snubber with 0.3 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

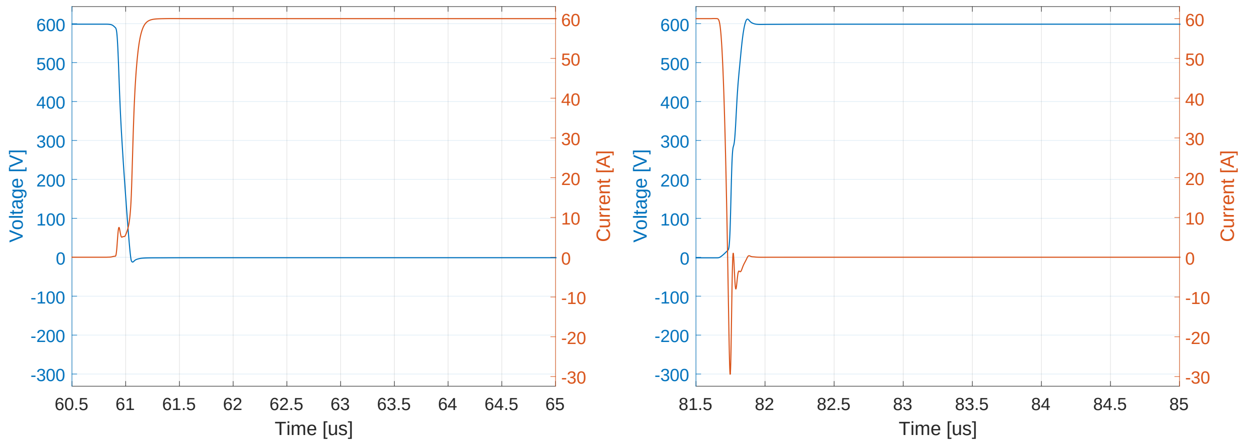


Figure D.3: Waveform of upper MOSFET using RC turn-off snubber with 0.6 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.

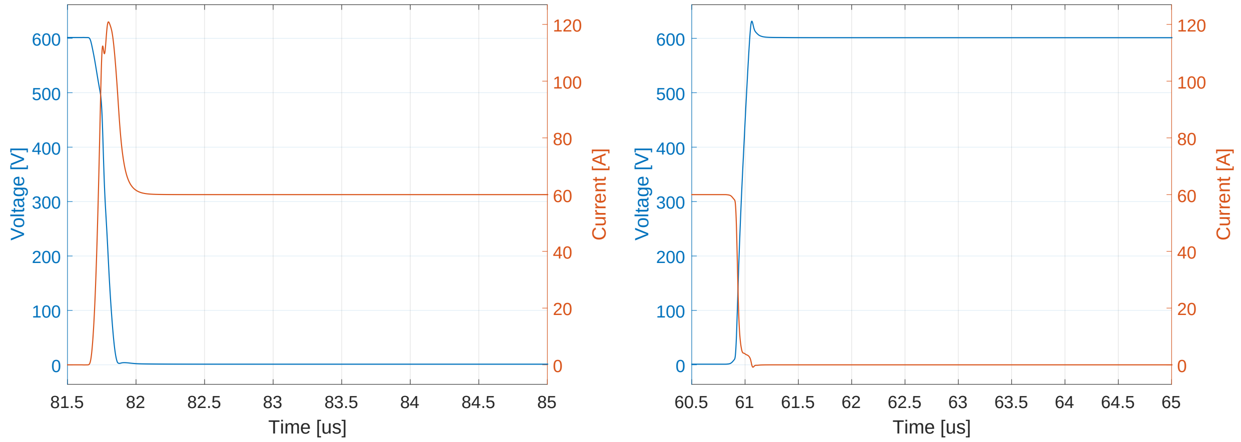


Figure D.4: Waveform of lower MOSFET using RC turn-off snubber with 0.6 damping constant; 60 A load current. Left: Turn-on. Right: Turn-off.