

Modeling, simulation and control of the alternate arm converter

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Preface

Master Thesis was carried out at the Norwegian University of Science and Technology, Department of Electric Power Engineering and Delft University of Technology, Department of Electrical Sustainable Energy during the spring semester of 2017.

This Master Thesis is for the joint education programme European Wind Energy Master (EWEM) with a focus of Electrical Power Systems (EPS) track. It was wrote for two universities Norwegian University of Science and Technology and Delft University of Technology.

I hereby declare that this thesis titled "Modeling, simulation and control of the alternate arm converter" and the work presented in it is my own.

Trondheim, 04^{th} August 2017

Donatas Dembinskas







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Abstract

The fast evolving technologies have resulted in an extensive use of the power electronics. More intelligent grids can be made by implementing the power electronic devices. In response to global increasing energy demand and significance of the clean and sustainable future the renewable energy sources, like sun, wind and water are exploited. Power electronic devices together with the renewable energy resources create a new type of grids. The new type of grids create a new challenges. Nowadays more often the new energy production resources are moved outside the land in the seas or the oceans, while the land is used for the accommodation of people. The energy resources moved outside the land require the transmission of the energy, where it is used. Connecting all those three dots: power electronic devices, sustainable and clean future and the new location of the renewable energy sources results in the question how to create the grid for energy transmission and transit the energy in the cheapest and the most sustainable way.

The offshore energy mostly are delivered to the land by the cables. With increasing length of the cable losses increases, in order to avoid losses the AC voltage are transformed to the DC voltage. The transformation of the voltage from AC/DC requires somewhere in the sea or ocean a substation. A substation contains a converter where the all nearby distributed energy resources are connected. The voltage is transformed to DC in these substations. The voltage are transformed again from DC/AC in the next substation usually located onshore. The costs and the reduction of the substation size requires to look for a new and better voltage transformation topology.

In this study a new hybrid voltage source converter based topology is modeled, simulated and controlled. This new topology is usually known as alternate arm converter. For the simulation developing MATLAB/Simulink software is used. With the MATLAB/Simulink software the model of alternate arm converter is developed from the scratch. Firstly the simple one-phase average mathematical model is developed and implemented in the simulation. Then the balancing control between the arms voltages is implemented in the onephase model. The simple one-phase with a simplified control model is evaluated. Then the three-phase model is created in the same MATLAB/Simulink software. Firstly the threephase model is evaluated as working in the island mode, which means that it is working alone, not connected to the grid. The improved control is implemented in this 3-phase model in order to increase the performance of the converter. The 3-phase model with improved control model is connected to the grid by using MATLAB/Simulink software. The grid connection is simulated with the voltage sources and phase locked loop control. The phase locked loop constantly adjust the voltage in order to lock onto the phase and frequency. Furthermore it is extract a voltage angle for the used dq0 transformation, which simplifies control. The grid connected model is simulated and evaluated. After this evaluation the MATLAB/Simulink simulation model of the alternate arm converter, together with control is connected in the point to point scheme. The point to point scheme repre-

sents the energy transmission from the one point to another or in the different case it can also transmit the energy in the other side. The point to point system is represented in the MATLAB/Simulink model, together with additional droop control, which controls the DC voltage accordingly to the active power. If the active power reaches the maximum value the DC voltage decreases accordingly to the drop value and the way around. The six study cases are simulated in the MATLAB/Simulink software, with the point to point connection. In the first case the operation points are evaluated of the system and the behaviour of the AC voltages, AC currents, DC voltage, arm voltages, arm currents and circulating currents are observed in the terminal 1 and terminal 2, which is AC/DC and DC/AC converters, respectively. The second study case is aimed to inspect the DC side capacitance effect to the DC voltage. In this study case is evaluated that by increasing the DC side capacitance the DC voltage ripple reduces, therefore the AC currents with less harmonic distortions are presented. The third case shows the droop control behaviour for the different drop values. When the drop value is increasing the gain value of the droop control decreases and the smaller deviation of the active power is presented. The forth, fifth and sixth cases arise, because of the problem confronted during the operating point case simulations. The voltages between the upper and lower arms in some of the operating points are not balanced. This issue creates an arm voltage balancing problem, which in the forth study case is solving by increasing overlap time. The observation is made, that by increasing overlap time the balance between the arm voltages becomes better, but the alternate arm converter are forced to approach and change the topology to modular multilevel converter, when the 10 ms is reached in this case. The fifth study case investigates the cell capacitance effect for the arm voltage balance. In this case was found that increasing or decreasing the cell capacitance in the submodules, do not fix the arm voltage balancing problem. This approach makes voltage balance between the arms even worse. The last study case introduces the case of the arm voltage balance technique by using third harmonic current flow together with 1 ms overlap time. This study case requires a minor changes in the point to point system. The results of this technique are evaluated and it shows that this type of the balancing technique is the best technique of the voltage balancing between the arms in this system of the point to point connection.

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Abbreviations

COP Conference of the Parties, RES Renewable energy source, HVDC high voltage direct current, DER distributed energy resources, **HVAC** high voltage alternating current, LCC line commutated converter, **VSC** voltage source converter, MMC modular multilevel converter, AAC alternate arm converter.

DC = direct current, AC = alternating current,

FACTS = flexible alternating current transmission system,

GTO = gate turn off,

IGCT = integrated gate commutated thyristors,IGBT = insulated gate bipolar transistor,

SVC = static var compensation,

STATCOM = static synchronous compensator, TCSC = thyristor controlled series capacitor,

PAR = phase angle regulators, AVM = average value model, ICC = inner current controller, OVC = outer voltage controller, PLL = phase locked loop,

TSO = transmission system operator,

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INTRODUCTION

1.1 Background

Nowadays the rapidly changing world and the booming population will require more and more energy generation. Old thermal and nuclear plants are not capable to provide that huge amount of energy, furthermore the carbon footprint left by generating energy from these power plants will increase with the increasing number of the new power plants. The nuclear plants are debatable to be safe anymore after couple of the incidents and the nuclear waste storage are unsolved issue [9][10]. The non-renewable energy sources are limited and increasing population will increase usage of them, therefore the new solutions should be planed, otherwise in the nearly future it will be a lack of the fossil fuel [11].

Another huge risk is a global warming. The situation is getting worse and worse each year, that is why a such events as United Nations climate change conferences are organized. Conference COP 21 was held in 2015. In this conference 195 countries were participating and by now 154 [20-05-2017] countries signed an agreement to reduce green house gasses and keep the global warming temperature well bellow than 2°C [12]. This conference directed a new point of view in the energy production, transformation, transmission and even usage. The production will be achieved by using renewable energy sources (RES) as wind parks, solar systems, hydro plants, biomass, geothermal energy and so on. Transformation efficiency and the reliability will be increased. The bulky power transmission systems to become more efficient are requiring less energy losses, therefore the high voltage direct current (HVDC) transmission systems are taking over. Nowadays smarter ways how to save energy get more trend. The word "smart" gets a new meaning, where saving of the energy are highlighted in the every step and people are encourage to save energy even in the smallest amounts. People are taught how to use the produced energy widely. A simple example even of the smallest thing like "turnoff" of the TV standby mode, can make huge impact, when it will be used widely. Increasing energy production can not stand alone, it should be supported by the usage of it in the most efficient way. The production of the energy should be harmless to the environment, therefore the world driven of the green energy getting more fashion than before.

The situation requires to coupe people from the different places. Most of them to produce energy are implementing solar systems, which are the best solution for the households. The energy production for the communities, villages or even towns are wind energy, biomass or hydro plants. These different access points are called distributed energy resources (DER), where the access are distributed to the energy in the area and are not centralized to one energy production resource. Distributed energy resources at some point have to be coupled with the grid access point. The connection should satisfy certain limits as voltage, current or frequency levels and during the connection should not disturb the grid. Today most of the DER are connected with a grid using an alternating current (AC), but it is not a solution in the future, due to the difficulties of synchronization, satisfaction of the grid constraints and increasing requirement of the efficiency in the transmission systems. While the relatively small DER can still be coupled easier with the strong grid by using AC. The high voltage direct current transmissions or links are better solution to couple large DER to the grid. Huge converter stations are used to collect and covert from AC to DC all the DER. The offshore wind energy parks are the good example of the converter station terminals in the sea, since most of the time they are connected through the cables, which generates more reactive power, than the lines.

1.2 Objective of the work and motivation

The substation converter can connect and convert high voltage alternating current (HVAC) and HVDC links and vise versa. Two types of the converter topology are used nowadays. Line commutated converters (LCC) and voltage source converters (VSC) [4]. Nowadays VSC can be divided into proven two types of the converters: two level converters and modular multilevel converters (MMC).

The new topology of VSC arises, which is a hybrid of merged two of mentioned VSC types. It is known as alternate arm converter (AAC) and was firstly introduced in [13]. The converter type is under investigation nowadays and not yet proven technology to be used commercially. The study aims to create a MATLAB/Simulink model to test the behaviour of the converter. First the model of AAC will be created in Simulink, together with a simple control schemes. Then it will be tested in the island mode, by observing its operation and understanding its working principle. After that the connection to the grid and implementation of the improved control will be observed. Finally the simulation of the converter will be used in the point to point connection. The connection scheme are illustrated in Figure 1.1. As it can be seen in this case the wind turbine park is considered operating in offshore. The wind turbines are connected to the substation, which is placed in offshore. The connections of the wind turbines to the substation are through AC submarine cables. The distance between the wind park and the offshore substation is feasible to still use AC voltage. Offshore and onshore converter stations converts AC to DC and DC to AC, respectively. LCC and VSC topology can be used in these converter stations. The converters are connected through the HVDC link. The HVDC link consist of the HVDC submarine cables and transfers power to the onshore substation.

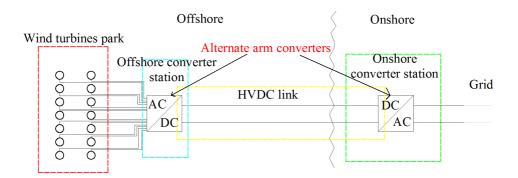


Figure 1.1: Example of the possible realization of the AAC.

Considering all of the above mentioned steps and remarks Master thesis project motivates to inspect the new topology of the converter - AAC and its behaviour in the point to point connection, which can be usefull in the future renewable energy sources, especially wind energy.

1.3 Outline of the thesis

Chapter 1 [Introduction]

This chapter firstly represents briefly the movement towards and need of renewable energy sources. The rise of the distributed energy resources and couple of them in the network. The next subsection represents objective of the work and motivation.

Chapter 2 [High voltage transmission technologies]

This chapter introduces two types of the high voltage transmission technologies and comparison between them. The introductory part of the high voltage alternating current technology is presented in the first section. The second section presents high voltage direct current technology and future aspects of the network connection. The connection types of high voltage direct current are also explained in this section. The third section is comparison between high voltage alternating current and high voltage direct current. The comparison of the power amount transferred in both of the transmission systems are presented. The amount of the losses occurring during power transfer and the costs of the each transmission system, break-even distance.

Chapter 3 [Topology of the converters]

The topology of two commonly used converters are introduced in this section. Line current commutated converters are briefly represented in the first section and voltage source converters are represented in the second section, with 2 subsections of the already used in the commercial projects voltage source converters. The one is called 2-level converter and other modular multilevel converter. The brief topology is explained of these two voltage source converter types.

Chapter 4 [Modeling an alternate arm converter]

The new hybrid topology of the voltage source converter is introduced in the first section of this chapter. The type of the voltage source converter high voltage direct current

is introduced in the second section. Chosen average value model type is discussed. The third sections talks about the mathematical representation of the alternate arm converter. The simple mathematical model is derived. The forth section shows one-phase simple average model simulated in the Simulink by using mathematical model representation of the previous section. The simple controls of the arm voltage balancing are implemented in the following sections. The fifth sections shows the derivation of the "sweet spot" voltage and its implementation in the one phase simulation model. The sixth section provides information about overlap balancing technique and implementation in the one-phase Simulink model. The different constant values of the overlap control are investigated and represented in the Appendix A.

Chapter 5 [Control strategy of the alternate arm converter]

In this chapter controls are adapted for the 3-phase island mode simulation model. In the first section the Park-Clarke transformations are represented in order to simplify further control schemes. The second section shows steps of the control strategy used in the 3-phase island mode simulation model and the current control as inner loop. The third section represents outer loop control, which for this simulation model is voltage control.

Chapter 6 [Alternate arm converter in the point to point connection]

This chapter represents the alternate arm converters connected in the point to point connection, its behaviour, simulation results and problems arise during the connection. The first sections introduces system components and evaluation and why they are needed. The control required for the converters in this type of the connection is briefly introduced. The second section introduces six study cases in the point to point connection. The study cases are splat up in the six subsections. The first subsection introduces the study case for the different operating points of the point to point connected alternate arm converters. The second subsections shows the DC side capacitance effect for the DC voltage. The third subsection introduces effect of the different droop control drop values for the active power and DC voltage. The forth subsection shows arm voltage balance problem and its solution by varying overlap time, which is confronted in some operating points during the first subsection. The fifth subsection continues solve the arm voltage balance problem with the different approach, by changing cell capacitance value. The results and observations are represented in this subsection. The sixth subsection introduces a new arm voltage balancing technique with circulating third harmonic current. This technique is used together with overlap control. This merged technique solves the issue confronted in the forth subsection, when the AAC typology is forced to change a topology to the MMC, in order for the better balance between the arm voltages. This balancing way required a small system changes in order to implement it.

Chapter 7 [Conclusion]

The final conclusion and discussion will be represented in this chapter.

Chapter 8 [Future work]

The possible future work will be stated in this chapter.



HIGH VOLTAGE TRANSMISSION TECHNOLOGIES

The first thing about high voltage comes in mind that it is harmful for the livings. The definition of the high voltage exists, due to the classification of the voltage levels. The classification can be made differently in each country, but mainly the high voltage term is considered to be when the voltage level can cause the spark in the air. Therefore the term high voltage means that the level is above the threshold limits. The high voltage can be used everywhere starting from the power transmission, medical equipment like X-RAY, laboratory equipment like arcing demonstration or at home like TV. In this chapter HVAC, HVDC and comparison between them will be discussed.

2.1 High voltage alternating current technology

At the very beginning electric power transmission system was created to be direct current. By operating direct current (DC) transmission system increase or decrease voltage level at that moment was not that easy, because the different type of loads required the different levels of the voltage and these issues required different generators and circuits. The certain events like evolution of the induction motors and the development of the transformers, allowed easily to transmit power and distribute it in the required voltage levels. Therefore the alternating current transmission system spread all over the world.

The first high voltage (at that time) commercial alternating current (AC) transmission system was build in 1891. The transmission line was 15kV and 175km long, it connected Lauffen and the Frankfurt [14]. The electrical power system consist of the generation, transmission and distribution parts. The vertical power transmission system is represented in Figure 2.1. Mainly the power of the electrical power system are produced by the AC generators, after that the AC voltage level is increased by transformers in order to reduce

conduction losses, due to the fact that voltage have opposite proportionality of current. Mostly long and bulky transmission systems are operating in high voltage level by transmitting power along overhead lines or cables to the following substation. At the receiving substation the transformer lowers the voltage level to the feasible for the distribution. The distribution system depends on the type of the customers, they require different voltage levels, therefore the distribution substations can contain several transformers.

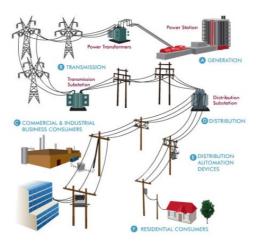


Figure 2.1: AC transmission diagram [1]

The transmitted power is defined by the equation 2.1, where P is an active power flow, V_s is sending end voltage, V_r is receiving end voltage, X_s is line impedance and δ_{sr} is voltage-phase angle at the sending end with respect to the receiving end. As it can be seen from the equation 2.1 the limiting factor of the power transmission is line impedance X_s . Therefore the lower is line impedance the higher active power flow can be achieved. The power consumption grows and forces to search for a new ways of the power transmission. One of the ways is to create a parallel line for the power flow in the vertical power transmission. The issue comes when the power flow is shared and one of the line caries higher amount of power than other, therefore the control should be obtained for the equal power flow. In the meshed systems this issue creates even more complications, since reliability should be maintained. The solutions can be high voltage direct current usage, which is represented in section 2.2, or flexible alternating current transmission systems (FACTS).

$$P = \frac{V_s V_r}{X_S} \sin \delta_{sr} \tag{2.1}$$

In order to reduce the line impedance or have a ability to control line impedance FACTS are used in the HVAC transmission systems. It was developed in 1980s at EPRI in USA [15]. The power flow is regulated and control with the power electronic devices in the high voltage alternating current transmission systems. Implementation of the FACTS allow to reduce investment costs of operation and transmission, increase reliability and security of the system, transfer higher power through the system and control dynamic re-

active power with fast acting power electronic devices. Power flow capability can be only limited by the thermal limits.

Depending on the power electronic devices, which are used for the FACTS, they can be divided. Thyristor based: gate turn off (GTO) and integrated gate commutated thyristors (IGCT), which are switched at the low frequency. Insulated gate bipolar transistor (IGBT) based, which are switched at the high frequency. FACTS not only allows to control line impedance, but also voltage and delta angle between buses. The voltage can be controlled by the shunt compensation FACTS like static var compensation (SVC), STATCOM. Line impedance control can be achieved by using series compensation schemes as thyristor controlled series capacitor (TCSC). For the controlling angle delta, the phase angle regulators (PAR) are used [15].

2.2 High voltage direct current technology

The first commercial high voltage direct current (HVDC) transmission link was between the Gotland island and the Swedish mainland. The link was launched in 1954 with the rated voltage value of 100 kV. Since then the HVDC evolved and populated dramatically over the world [16].

High voltage direct current has very attractive characteristics for the certain applications. Mostly HVDC are used for the high power transmissions over the long distance. In addition the advantage is asynchronous connections between the networks, where the two power systems are not synchronized with each other. Mostly HVDC technology are used, when the two networks should be connected through the submarine cables. The technology is advantageous, because of the no reactive power are transmitted in the HVDC. With the increasing amount of the renewable energy resources in the power system like offshore wind energy farms more often direct current technology is used for the bulky power transmission. Research and usage of the power electronics increase HVDC technology spread worldwide even more. With the newest power electronics converters come better reliability, voltage stabilization and the lower price, which still are the huge drawback for the HVDC network for the short time period, because the initial investments into the power electronics converter stations are higher than for the HVAC. During the long term period the costs become smaller comparing with the HVAC.

The projects and the capacity of the HVDC networks are increasing worldwide. Figure 2.2 illustrates one of the possibilities to connect whole world in HVDC transmission system. Every year capacity of the HVDC transmission systems are expanding. This phenomena allows to escalate another, but not new concept presented in 1889 by Thomas Alva Edison. At that time due to complexity and absence of the power electronics the distributed energy resources (DER) concept was hard to maintain and the distribution of the generation required huge investments. Therefore the concept of the DER at that time was faded away. Nowadays, where the power electronics are ruling every our step, the concept of DER is likely possible, so the concept gain new breath. Figure 2.3 provides an example of DER. As it can be seen the power flow is no more unidirectional by implementing DC in the grid the bidirectional power flow is easy to achieve. Bidirectional power flow allows higher usage and flexibility of the renewable energy resources. For example the solar systems on the house rooftops are capable to generate electricity and accumulate in the

energy storage places during the day, while in the evening the energy can be consumed by same household. Similar situation can be implemented for the wind turbine parks, when the wind is blowing generated energy can be stored at the storage units, when the wind stops the energy are consumed from storage places. Since more and more equipment in our houses are using power electronics, it will be easier if the grid will be DC. The initiative concept of the DC grid are also represented among researchers [17], but long distance bulky power transmission are more important case.

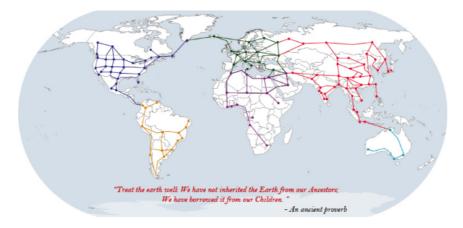


Figure 2.2: Future aspect of the possible HVDC network connection [2]

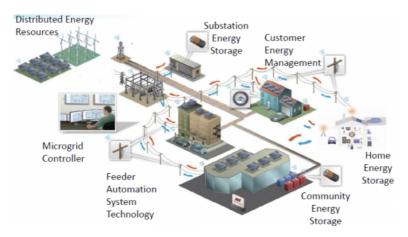


Figure 2.3: Network example of the distributed energy resources connection [3]

Long distance HVDC transmission has variety of configurations. The configuration depends on the systems design. Factors such as power transfer capability, voltage level or cable technology are taken into account, when the configuration is determined. The main configurations are monopolar, bipolar, back to back and multiterminal.

Three types of the monopolar configurations are illustrated in Figures 2.4a 2.4b and

2.4c. The figure 2.4a represents the cheapest and the most used type of the HVDC configuration for the offshore transmission. The idea behind this is to use the ground as the return conductor. It can be achieved since the sea or ocean water is salted. This solution is the cheapest, because it is not required the return conductor, it uses only ground electrodes. The main drawbacks are limited power transfer and the cause of the metallic objects corrosion. The monopolar configuration with ground return can not work if the return ground path is very resistive. The monopolar configuration with the metallic ground return is illustrated in the Figure 2.4b to overcome these issues. The issue of the corrosion is solved, by implementing metallic neutral or low voltage cable as the return conductor. The return conductor can be grounded, which results in the asymmetrical monopole with metallic return configuration. The advantage of this configuration, DC conductor does not require full insulation, whereas the symmetrical monopole configuration with not grounded return conductor requires full DC conductor insulation [18]. In order to implement the redundancy in the monopolar configuration the midpoint of the ground connection are used. The Figure 2.4c represents the solution, if one of the transmission line fails, other still remains operational.

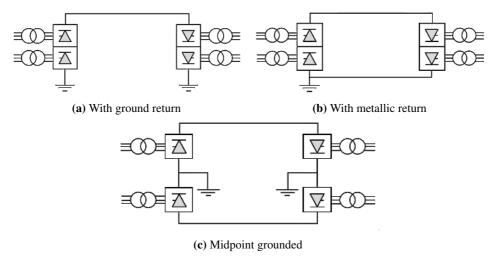


Figure 2.4: Monopolar configurations [4]

Bipolar configurations are represented in Figures 2.5a and 2.5b. This configuration consist of the two poles, where one is positive and other one is negative. Each pole has their grounded neutral points. For the normal operation the current flows in the loop, therefore there is no current flowing in the ground. This type allows to prevent the corrosion. Furthermore if the fault occurs at one of the poles, the configuration still can operate as the monopolar with the ground return. The Figure 2.5b illustrates the solution in the bipolar configuration during the fault in one of the poles with metallic return. The metallic return used for the ground connection prevents corrosion, when the configuration operates as monopolar [18]. The power transmitted through the bipolar configuration is double, than one transmitted in the monopolar configuration, because the bipolar configuration has 2 poles. The power flow reversal can be controlled by changing polarities of two poles in

the case of line commutated converter. The main drawback is the higher costs, than the monopolar solution.

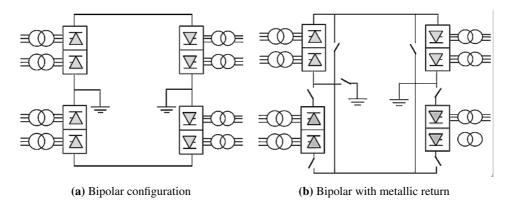


Figure 2.5: Bipolar configurations [4]

Back to back configuration is illustrated in Figure 2.6. Mainly back to back configuration are used as an interconnection of the asynchronous AC networks and when the system has two different frequencies, like in Japan. The two converters are placed close to each other, most of the time in the same station due to additional substation costs. The power transfer capability are limited by the connected AC system.

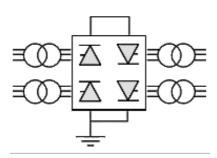


Figure 2.6: Back to back configuration [4]

Multiterminal configuration is shown in Figure 2.7. The configuration has three or more converter stations. The idea behind this is to connect multiple generation resources to one terminal. This allows to save cots of the terminals and reduces the conversion loses. The multiterminal configuration is useful for distributed energy resources and for the offshore industry, like wind farms, oil and gas rigs.

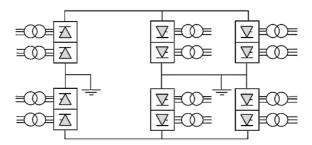


Figure 2.7: Multiterminal configuration [4]

2.3 Comparison of the HVAC and HVDC in transmission system

Comparison between HVAC and HVDC will be discussed in this section. Two calculations will be held in order to justify advantages of HVDC system in the bulky power transmission.

First of all the active power transfer capability is compared. Assuming AC and DC systems with the same properties and length. Two systems in AC have 6 conductors in total, because each system is three phase so three conductors per system. DC results in 3 systems, due the same amount of the 6 conductors, where direct current needs only 2 conductors per system. The first observation is that the DC capable to transfer higher amount of power, due to higher number of the systems. The comparison per phase voltage between AC and DC can be calculated by the equation 2.2, where V_{DC} is voltage of the one conductor in DC, V_{AC} is voltage of the one phase in AC. Then the active power for AC systems assuming current I can be written by equation 2.3. Active power for DC systems with the same current value I and substituted V_{DC} value from 2.2 equation results in equation 2.4. By equating P_{DC} , which is active power in DC and P_{AC} , which is active power in AC results in equation 2.5.

$$V_{DC} = \frac{\sqrt{2}}{\sqrt{3}} V_{AC} \tag{2.2}$$

$$P_{AC} = 2\sqrt{3}U_{AC}I\tag{2.3}$$

$$P_{DC} = 3(2\frac{\sqrt{2}}{\sqrt{3}}U_{AC}I) \tag{2.4}$$

$$P_{DC} = \sqrt{2}P_{AC} \tag{2.5}$$

As it can be seen from equation 2.5 the DC active power is higher than AC active power by $\sqrt{2}$. Furthermore DC transmission does not transfer reactive power, there is no dielectric losses, no skin effect losses and no proximity effect, so the active power transmitted in DC is even higher than $\sqrt{2}$. The greater power can be transmitted in DC

transmission system per conductor, because the active power in AC transmission has more losses, so that becomes lower.

The second case is comparison of the transmission conduction losses in the conductor. Assuming same properties and the length, same insulation level, same transferred power and same resistance for AC and DC. The relation of the current flowing in DC conductor and AC can be calculated by the equation 2.6, where I_{DC} is current in DC conductor and I_{AC} is current in AC conductor. The active power losses in DC can be calculated by the equation 2.7, where P_{L-DC} is active power losses in DC and P_{L-AC} is active power losses in AC. This gives that the active power losses in DC system is only half of the one in the AC system.

$$I_{DC} = \frac{I_{AC}}{\sqrt{2}} \tag{2.6}$$

$$P_{L-DC} = (\frac{1}{\sqrt{2}})^2 P_{L-AC} \tag{2.7}$$

HVDC transmission systems comparing with HVAC has simpler line construction, which has lower environmental effect. The conductors can be set closer to each other, because HVDC has no proximity effect. Less conductors are needed for the higher active power transmission capability. This results in smaller and less number of towers for HVDC in order to transfer same amount of the power.

The cable transmission system has a different behaviour than the overhead lines. The main issue in the long distance HVAC are current limit in the cables. The limitation arises, because the AC cable current consist of two components - active current and mainly capacitive current. Long HVAC cables has very high capacitive component in it, therefore the capacitive current becomes high, which causes higher reactive power transmission through long HVAC cables. The long HVAC cables have a limitation of distance. In order to reduce the capacitive current FACTS can be used in the system, which compensates capacitive current with the inductive current. Another solution to avoid this issue will be HVDC cables. The HVDC does not transfer the reactive power. The situation of the long HVAC transmission systems are severe in the overhead lines also. The distance are longer in the overhead lines than for the cable, but the problems arise when the overhead lines reaches 500 – 800 km [19]. In the system with fully maintained heavy loads collapse of the system can be observed even in the half of the desired distance. No loading or very small loading has a so called Ferranti effect. The effect is, that the voltage at the receiving end will rise and can exceed the required voltage limits, therefore damaging some equipment [20].

The greatest disadvantage of the HVDC transmission systems are costs of the converter station. The Figure 2.8 illustrates the break-even distance for the costs of HVAC and HVDC systems. As it can be seen in the left side Figure the costs of the DC terminal itself covers together AC terminal costs and half of the AC line costs. DC line costs are smaller than AC line. Initial investments for the DC system is way higher than AC, but the total investments, taking into account losses are higher for the AC system. Therefore the break-even distance of the costs can be observed. Break-even distance for the overhead lines is typically $700-800~\mathrm{km}$ [19] and for submarine cables $40-70~\mathrm{km}$ [21]. The break-even distance can vary depending on the properties of the project, transmitted power or voltage

levels. The right side Figure shows break-even distance for HVAC and HVDC taking into account the additional cost of the shunt compensation in the HVAC systems, therefore the break-even distance costs between HVAC and HVDC becomes even smaller.

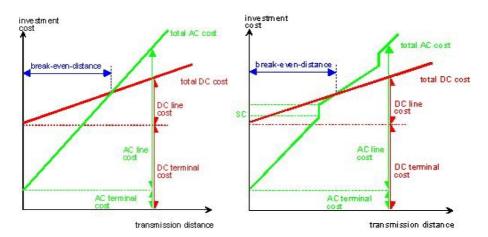


Figure 2.8: Break-even distance of the costs for the HVAC and HVDC systems [5]

Another disadvantage of the HVDC system is limited overload capability of the converter. The overload capability in the converters are getting higher each year, due to semiconductor devices and increasing researches. Line commutated converters are called traditional HVDC converters. These converter stations require reactive power, has harmonic pollution, due to thyristors switching, which require filtering. The filtering in the HVDC traditional converter stations occupies huge amount of space. In the section 3.1 the traditional line commutated converters are described. The following section 3.2 points out the relatively new voltage source converter technology.

	7			
Chapter	J			

TOPOLOGY OF THE CONVERTERS

3.1 Line current commutated converters

Line current commutated converters are based on the thyristor switches. When the first commercial HVDC lines were used, they were based on thyristor valves, due to the high reliability [7]. Thyristors have wide voltage blocking capability and large current conduction. The thyristor symbol is represented in 3.1. Thyristors have three terminals, where anode is positive, cathode-negative and gate represents triggering pulse of the thyristor. Anode has a higher potential than the cathode, therefore current are flowing from anode to cathode, only then when a small pulse are applied to the gate terminal, otherwise the conduction is not happening. After triggering, the pulse can be removed from the gate terminal and conduction process running till the flowing current drops to zero. After that a new pulse should be triggered again. The gate allows to turn-on thyristor at a desired time. Assuming frequency/time domain (ωt), the time when the pulse is triggered is called firing angle, α . Phase voltage zero crossover defines the firing angle. Zero is the earliest point when the thyristor can be gated on [22]. Commonly thyristors are used with the snubbers connected to the device in parallel. Snubbers protect semiconductor from voltage transients, reduce the response of dv/dt and can be used for the soft switching and reduces losses [7].

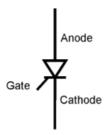


Figure 3.1: Thyristor symbol [6]

Classical line current commutated converters require the thyristor devices. The devices for operation require synchronized voltage source. Graetz bridge is the basic building block for the three phase conversion of the 6-pulse configuration converter. Definition of the 6-pulse means, that the converter has a six switching operations per period, causing the dc output voltage to be a harmonic ripple of six times the harmonic frequency [4]. The converter is illustrated in Figure 3.2. During the conduction period the current I_d flows through one of the upper thyristor (T_1,T_3) and T_5 and one of the bottom thyristors (T_2,T_4) and T_6 . The commutation between thyristors occurs naturally since they are displaced 120° [7]. The average DC voltage can be controlled by the firing angle α or by applied voltage magnitude. The relationship are represented in equation 3.1, where V_D is an average DC side voltage, V_{LL} is rms value of line-line voltage, α is a firing angle, L_8 is AC-side inductance (stray inductance), ω is angular frequency and I_d is converter DC current.

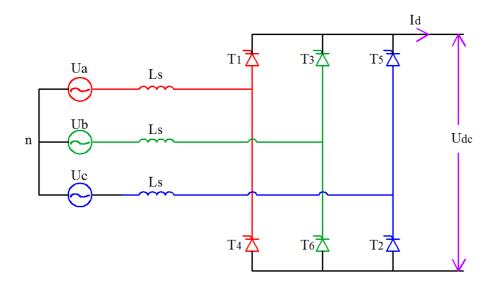


Figure 3.2: 3-phase 6-pulse converter

As it can be seen from the equation 3.1 the average DC voltage can be increased by increasing the V_{LL} . Furthermore the increased alpha reduces the V_D . Assuming the ideal situation, when the stray inductance $L_s=0$ and keeping V_{LL} constant, the relevant cases can be observed. When $\alpha=0^\circ$ the operation is similar to the diode operation. When $\alpha=90^\circ$ the average voltage of the DC goes to zero. If the α is increased further, the converter starts behave as the inverter. Since the thyristor only operates in two quadrants and the current flows in one way, during the inverter operation voltage polarity changes, therefore the power flow starts to flow from DC side [22].

$$V_D = \frac{3\sqrt{2}}{\pi} V_{LL} \cos \alpha - \frac{3\omega L_s}{\pi} I_d \tag{3.1}$$

Before the assumption of the ideal situation when $L_s=0$ leads to simultaneous change from one thyristor to another. In reality there is always leakage inductance, which slows down that transition. The transition time is defined by the current changing steepness di/dt. This results in releasing and receiving phase voltages and transferring current at the same time. This process is called overlap and it is defined by the overlap angle, μ . The Figure 3.3 represents overlap, μ , in the rectifier operation, during the commutation, the line to line voltage is shorted and released energy are absorbed by L_s , till the transfer of the current is finished [7]. In order to extend overlap time the value of the inductor can be increased, but from the equation 3.1 can be seen that larger inductor will reduce the overall average DC voltage output.

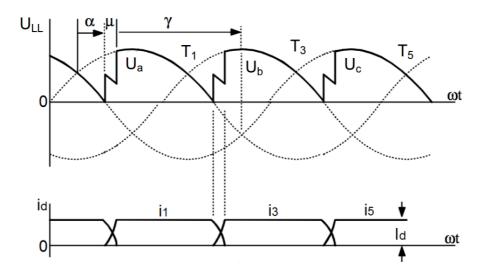


Figure 3.3: Commutation of the rectifier operation [7]

The commutation of the inverter operation is represented in Figure 3.4, as it can be seen the commutation process should be done before the voltage intersection, because the thyristor should recover its blocking capability. The minimum advance limit angle for safe commutation is called β . It is related to the μ and γ . Where γ is the angle for the thyristor

to regain its capability to withstand positive voltage after current conduction (extinction angle) [7]. Relation between μ and γ is showed in formula 3.2, where the link between α and β is presented by equation 3.3.

$$\beta = \mu + \gamma \tag{3.2}$$

$$\alpha = 180^{\circ} - \beta \tag{3.3}$$

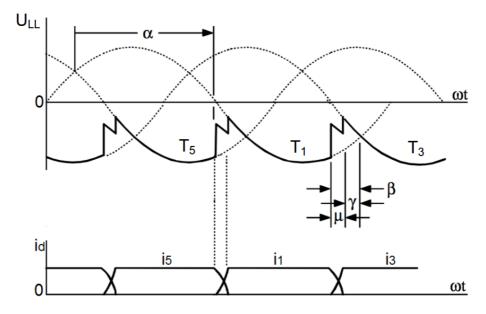


Figure 3.4: Commutation of the inverter operation [7]

Commonly the ideal thyristors should stop conducting when the current reaches zero crossing, however the real thyristors conduct further even the current reaches zero crossing, due to the reverse recovery charge. Commutation failure arises, when the flow of the current from one thyristor to another is not completed, before voltage commutation reverses across following thyristor. In order to avoid commutation failure the minimum turn-off time should be ensured. This allows thyristor to go to the reverse recovery state, where it can regain full forward voltage blocking capability. The turn-off time is associated with the extinction angle γ [22]. The failure causes high short circuit currents, therefore converter components are damaged. The minimum extinction angle should be ensured for the thyristors, otherwise during the system disturbances commutation failure is inevitable. During disturbances on the AC side are important to have safe margin for the extinction angle, however the large margin will require higher reactive power consumption. A trade of the extinction angle and reactive power, which depends on how strong is the AC grid, should be considered when designing LCC.

3.2 Voltage source converters

The first voltage source converters were introduced in the late 1990s. Since then the evolution in design, rapid grow of the power ratings and higher voltage levels are achieved [23]. Mainly the voltage source converters use power electronic valves, which can be turned-on and turned-off at desire. Usually valves are established with the insulated-gate bipolar transistors (IGBT). The IGBT circuit diagram is represented in the Figure 3.5a. The controllable signal is provided in the gate (G) port, which is the signal with two degrees of freedom turns on and turns off. When the signal has a turn-on command the IGBT starts to conduct current from the collector (C) to emitter (E). The current flow from the collector to emitter is called unidirectional, since it flows only in one way. However, in order to create the bidirectional current flow the anti parallel diode is introduced in the IGBT circuit diagram shown in the Figure 3.5b. Furthermore the IGBT has an excellent and simple switching characteristics, but the switching loses in it are higher than in thyristor based converters [24].



Figure 3.5: IGBT representations

With increasing power the voltage and current grow up. IGBTs are connected in series to withstand the higher voltage levels. Series connection provides higher voltage blocking capability. To withstand higher current ratings, the current is shared by connecting IGBTs in parallel. The anti parallel diode has to be design to prevent the stress created by the faults in the system. Usually the implementation of these features are done in the production and the IGBTs are provided in modules for the higher power applications.

In comparison voltage source converters with line commutated converters, the advantages and disadvantages depends on the project requirements. The VSC has a "black start capability", insignificant level of harmonic generation (valid not for 2-level converter, but for MMC type), hence no filters required, smoother reactive power control, easier power flow reversal, since it can be done by reversing current flow, compact site area. While the line commutated converter technology is more mature, therefore more reliable, the higher power transmission capability, good overload capability, lower station losses, lower cost [16].

3.2.1 2 level voltage source converters

Two-level converters were the first generation of the voltage source converters, introduced in the beginning of this chapter 3.2. The 2-level VSC converters are using self commutated IGBT switches, which are able to turn on and turn off at will. The IGBT switches, which are doing this procedure are represented in section 3.2. The topology of the 2-level VSC converter is represented in the Figure 3.6.

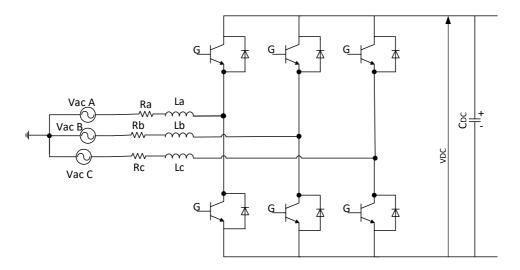


Figure 3.6: Two level 3-phase voltage source converter topology

The 2-level 3 phase converter consist of the 6 arms or 3 legs. The IGBTs are representing switches in each arm, where the terminal G of the IGBTs is the gate, where the switching signal is provided. The operation principle is very straight forward. The switches in each leg are complementary, which means while upper is on the lower is turned-off. Therefore the each leg can produce half of the DC voltage, when the upper switch is turned-on the AC terminal voltage is connected to the positive DC terminal voltage, resulting in $+0.5V_{DC}$ and when the lower switch is turned-on the AC terminal is connected to the negative DC terminal voltage, resulting in $-0.5V_{DC}$ [25]. Therefore the resulting output voltage signal is a square wave with positive half value of DC and negative half value of DC.

3.2.2 Modular multilevel converters

The modular multilevel converter (MMC) commercially was firstly used in the Trans bay project in San Francisco [26]. The topology of the MMC is illustrated in the Figure 3.7. The 3 phase MMC consist of 6 arms or 3 legs as the 2-level converter 3.2.1. Different from a 2-level converter the MMC consists of the number independent submodules in the each arm and the submodules contain its own capacitor. Each arm contains an inductor with the small resistance [27].

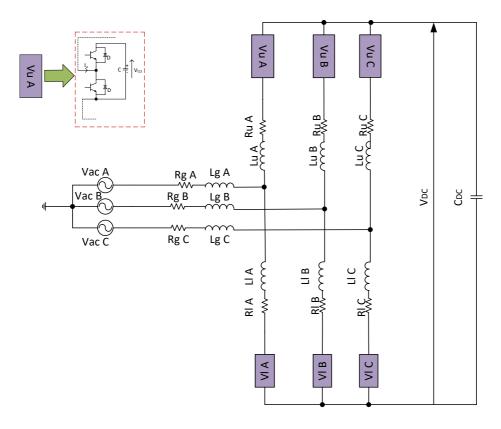


Figure 3.7: Modular multilevel converter topology

The operation principle of the MMC is a bit different than other converters, because the MMC has no turn-on or tun-off state for the flowing current. Therefore the current in the MMC flows continuously. The DC current divides equally into 3-phases and a 3-phases AC current splits equally in the upper and lower arms of the each phase [26]. The submodules existing in the arms are controlled in a way that the capacitor is inserted in the circuit or bypassed. This results for submodules act as the independent converters, where inserted voltage can be 0 or V_{stcell} . Depending on the current direction the capacitor in the submodule can be charged or discharged. When the sufficient amount of submodules are connected in series the stepped voltage wave form close to the sinusoidal can be generated. The generated sine wave contains low level harmonics distortion [27].



MODELING AN ALTERNATE ARM CONVERTER

Alternate arm converter topology and operating principle will be discussed in the beginning of this chapter. The average dynamics model is developed in 4.3 section. This model will be used for the system studies. In this model the computation time will be significantly reduced, because the full model with all the dynamics increase simulation time, and results in slowing down system simulation studies. The average model will be constructed i the MATLAB/Simulink software and mathematically modeled in the following sub-sections.

4.1 Topology of the alternate arm converter and operation principle

An alternate arm converter was firstly introduced in paper [13], where it was represented in the Cigre conference as a hybrid voltage source converter. The AAC topology is pictured in the Figure 4.1. A 3-phase converter consist of 3 legs, one leg per-phase. One leg consist of the 2 arms: upper and lower. The arms are identical and has arm resistor, arm inductor, director switches and submodules. The submodule of the upper arm V_{uA} is illustrated in the Figure 4.1, where u indicates upper arm and A denotes phase. Several submodules are connected in the series in order to generate close to the sinusoidal stepped voltage signal. The director switches in each arm are IGBT connected in series, which also are represented in the Figure 4.1. Each arm has an inductor and the resistor, which shows arm resistance and director switch resistance combined together.

Operation principle of the AAC is similar to 2-level converter 3.2.1, it has so called director switches, which direct current to the upper or lower arms. The director switches are IGBT, connected in series, because of to withstand higher voltage ratings, when they are open. Like the MMC 3.2.2, the hybrid model has stack of cells in each arm responsible for the multistep voltage generation. The main advantage is, that only half of the voltage period is generated in one arm, therefore allowing to reduce amount of the cells

in stack. Unlike the MMC the AAC current does not flow continuously, because the director switches can interrupt it, therefore the AAC has a turn-on and turn-off states for the flowing current.

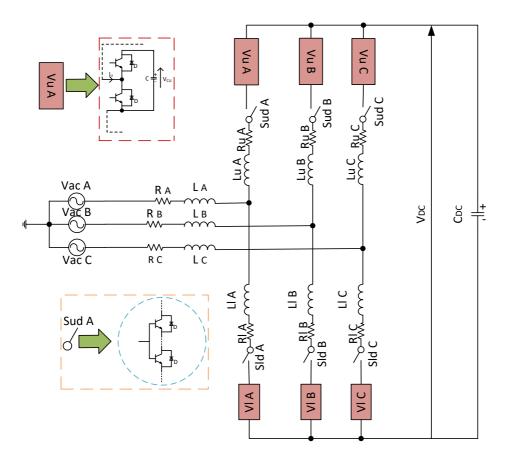


Figure 4.1: Alternate arm topology

4.2 Types of VSC HVDC models

Types of the VSC HVDC models depends on the studies. The studies depends on the time frame of phenomena being analyzed in the DC grid [28]. In this document [28] 7 types of models are represented. The brief representation of all types of models are reviewed in this section and the most suitable type is chosen for further simulation studies.

• Type 1 - Full physics based models - not suitable for the grid modeling, since the switches and diodes are represented by the differential equations, therefore it is complex to parameterize.

- Type 2 Full detailed models simplified non linear IGBT models are used, where
 the IGBT/diodes are represented by a nonlinear resistance, therefore this type of
 models can represent each one conduction mode of the bridge.
- Type 3 Models based on simplified switchable resistances the IGBT/diodes are represented by two value resistors.
- Type 4 Detailed equivalent circuit models this model represents accurate impacts
 of different capacitor voltages at each module level, but a reduction is evaluated to
 reduce the number of electrical nodes, which characterize converter.
- Type 5 Average value models (AVM) based on switching functions AC and DC aspects are modeled as controlled voltage and current sources, with different harmonic representation. The assumption that module capacitor voltages are balanced. This type has simulation speed advantage and are useful in DC grid system performance studies.
- Type 6 Simplified average value models AC and DC side components are modeled as controlled current and voltage sources. The sources produce waveform, that tracks their control-function input values, without switching harmonics. The upper level controls remains complete and a valve models is simple, which gives fast simulation time. Can be used for the large AC/DC grid simulations.
- Type 7 RMS load-flow models the outputs of the converter in steady state are using by load-flow models. The detailed transients are not presented.

Assuming that the converter will be used in the DC grid performance studies and point to point connection, behaviour of the converter will be investigated. The Type 5 model is considered to be used, for the studies. Resulting in the assumption, that the module capacitor voltages are balanced, which means that the capacitance voltage in the submodules are balanced (the same), while the arms voltages should be balanced by implementing control strategies.

4.3 Mathematical representation of the alternate arm converter average model

Usually arms submodules are consisted inside with the independent small converters, which are connected in half bridge or in the full bridge. These converters are connected in each arm in series and are called stacks of the modules. The half-bridge and the full-bridge sub-modules are represented in 4.2a and 4.2b, respectively in the Figure 4.2. As it can be seen the 4.2a sub-module has a half amount of the IGBT than 4.2b.

The half-bridge IGBTs S1 and S2 are complementary, which means when one is closed other should be open, otherwise the submodules are shorted. When the current is flowing inside the sub-module and the S1 is closed, the capacitor is charged. When the current direction is opposite and the S1 is closed the capacitor is discharged. Therefore the current direction defines if the capacitor will be charged or discharged. When the S2

is closed and the S1 is open regardless of the current direction if it flows inside submodule or outside submodule the capacitor is bypassed.

In the full-bridge connection the IGBTs are working in pairs, therefore S1 and S3, S2 and S4 are complementary. The S1 can not be in close state together with S3 and S2 can not be closed at the same time as S4, because it cause a short circuit. When the current is flowing in the submodule, S1 and S4 are closed, S3 and S2 are open the capacitor is charged. If the S3 and S2 are closed, S1 and S4 are open with the current flowing in the submodule the capacitor is discharged. When the current flows in opposite direction (it flows out of the submodule) and S2 and S3 are closed it charges a capacitor, and capacitor is discharged when the S1 and S4 is closed while S2 and S3 are open. The capacitor will be bypassed when the S1 and S2 are closed or when the S3 and S4 are closed. The charge or discharge of the capacitor in the full-bridge regardless of the current direction can be achieved by manipulating only the IGBT pairs. This advantage allows to generate positive and the negative wave form.

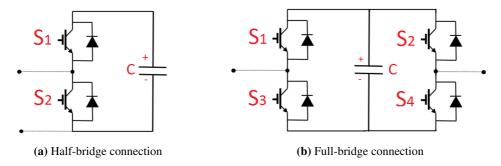


Figure 4.2: Submodule connection types

If the DC voltage blocking capability is not required, in order to reduce the number of switches in the submodules, the half-bridge connection is used. Here for the average model of the AAC the half-bridge is used, because the aim is not to study faults in the system or in the converter. In order to simplify modeling, ideal switches will be used instead of the IGBTs. The submodule is represented in the Figure 4.3. The submodule voltage V_{sm_i} can be written with equation 4.1. Where i is a number of the submodule, n_i is 0 or 1 depending on if the capacitor is bypassed or activated, V_{c_i} is the voltage across the capacitor located in the submodule.

$$V_{sm_i} = n_i V_{c_i} \tag{4.1}$$

The voltage dynamics in the capacitor can be calculated with the equation 4.2, where C is capacitance value, i_m is current flowing in submodule.

$$C\frac{dV_{c_i}}{dt} = n_i i (4.2)$$

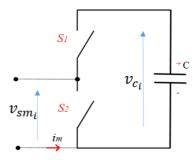


Figure 4.3: Ideal half-bridge submodule

Assuming the N number of the submodules in the stack and deriving the average model for upper and lower arms A phase , because other phases are derived in the same way only shifted 120° from each other. The Figure 4.4 illustrates A phase upper and lower arms, where the IGBTs are replaced with ideal switches. Voltage dynamics for the upper and lower arms can be written as equations 4.3 and 4.4 respectively respectively, where i_u is a current in the upper for one phase arm and i_l is a current in the lower arm for one phase. For the N number of submodules V_{cuN} and V_{clN} represent the voltage across N number of capacitors for the upper and lower arm, respectively. Subscript u indicates upper arm and subscript l denotes lower arm.

$$\begin{cases}
C \frac{dV_{cu_1}}{dt} = n_1 i_u \\
C \frac{dV_{cu_2}}{dt} = n_2 i_u
\end{cases}$$

$$C \frac{dV_{cu_N}}{dt} = n_N i_u$$
(4.3)

$$\begin{cases} C \frac{dV_{cl_1}}{dt} = n_1 i_l \\ C \frac{dV_{cl_2}}{dt} = n_2 i_l \end{cases}$$

$$C \frac{dV_{cl_N}}{dt} = n_N i_l$$

$$(4.4)$$

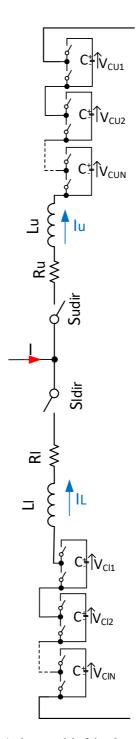


Figure 4.4: Ideal A phase model of the alternate arm converter

Upper and lower arms submodules are connected in series, therefore the capacitors voltage dynamics of the equations 4.3 and 4.4 can be rewritten as 4.5, 4.6.

$$C\frac{d\sum_{i=1}^{N} V_{cu_i}}{dt} = \sum_{i=1}^{N} n_{u_i} i_u$$
 (4.5)

$$C\frac{d\sum_{i=1}^{N} V_{cl_i}}{dt} = \sum_{i=1}^{N} n_{l_i} i_l$$
 (4.6)

The sum of the voltage across the modules can be written as equation 4.7 for the upper arm and the equation 4.8 for the lower arm. These equations are result of the two aggregated voltages per arm instead of 2N sub-modules representation.

$$\sum_{i=1}^{N} V_{cu_i} = V_{cu}^{\Sigma} \tag{4.7}$$

$$\sum_{i=1}^{N} V_{cl_i} = V_{cl}^{\sum} \tag{4.8}$$

The n_u and n_l can be rewritten as equations 4.9 4.10 respectively.

$$n_u = \frac{1}{N} \sum_{i=1}^{N} n_{u_i} \tag{4.9}$$

$$n_l = \frac{1}{N} \sum_{i=1}^{N} n_{l_i} \tag{4.10}$$

By substituting 4.7, 4.9, 4.8, 4.10 in the 4.5 and 4.6 respectively the aggregated voltage dynamics across capacitors can be represented in the equations 4.11 4.12.

$$\frac{C}{N}\frac{dV_{cu}^{\Sigma}}{dt} = n_u i_u \tag{4.11}$$

$$\frac{C}{N}\frac{dV_{cl}^{\Sigma}}{dt} = n_l i_l \tag{4.12}$$

In order to calculate current dynamics Kirchhoff's voltage law is used for the upper and lower arms of A phase. The loops are represented in the Figure 4.5. The voltage drops across each element in the upper arm are represented in the equation 4.13 and for the lower arm in equation 4.14, where V_{DC} is DC voltage, L_u is inductor in upper arm, L_l is inductor in lower arm, R_u and R_l are resistances in upper and lower arm respectively, V_{ac} is AC voltage. The current dynamics in the B and C phases can be calculated in the same way only a 120° phase shift difference between them.

$$\frac{V_{DC}}{2} - V_{ac} - \frac{L_u di_u}{dt} - R_u i_u - \sum_{i=1}^{N} (n_{u_i} V_{cu_i}) = 0$$
(4.13)

$$\frac{V_{DC}}{2} + V_{ac} - \frac{L_l di_l}{dt} - R_l i_l - \sum_{i=1}^{N} (n_{l_i} V_{cl_i}) = 0$$
(4.14)

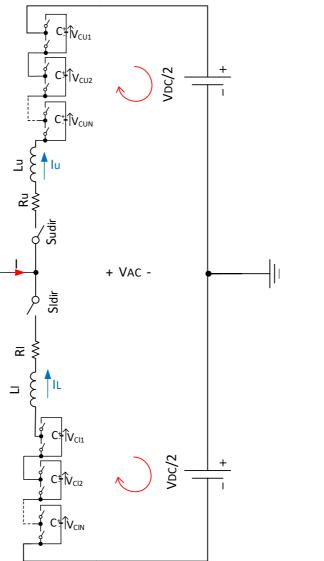


Figure 4.5: Kirchhoff's voltage law for the alternate arm converter

The instantaneous information of the voltage drop in all the submodules are needed. In order to realize this information, an ideal balancing assumption should be made. All the capacitors in the same arm will have the exact same voltage wave form. By following this

assumption the voltage in the modules can be approximated and represented as a single wave form in the equation 4.15 for the upper arm and equation 4.16 for the lower arm. The V_{cu}^{Σ} and V_{cl}^{Σ} represents same voltage wave form in the modules, which results the same voltage V_{cu} for upper arm and V_{cl} for lower arm. Multiplying V_{cu} and V_{cl} by the N number of the modules in each arm.

$$V_{cu}^{\Sigma} = V_{cu}N\tag{4.15}$$

$$V_{cl}^{\sum} = V_{cl}N \tag{4.16}$$

The stack modules are represented as the single generated voltage. The equation for the upper arm generated voltage is shown in formula 4.17 and for the lower arm in the equation 4.18, where the V_{ustack} is arm voltage of the modules in the upper stack and V_{lstack} is voltage in the lower arm stack of the modules.

$$V_{cu}Nn_u = V_{cu}^{\sum} n_u = V_{ustack} \tag{4.17}$$

$$V_{cl}Nn_l = V_{cl}^{\sum} n_l = V_{lstack} \tag{4.18}$$

In order of following the ideal balancing assumption V_{ustack} and V_{lstack} are placed in the equations 4.13 and 4.14 respectively. This will result in equation 4.19 for upper arm and 4.20 for lower arm.

$$\frac{V_{DC}}{2} - V_{ac} - \frac{L_u di_u}{dt} - R_u i_u - V_{ustack} = 0 {(4.19)}$$

$$\frac{V_{DC}}{2} + V_{ac} - \frac{L_l di_l}{dt} - R_l i_l - V_{lstack} = 0 \tag{4.20}$$

To sum up this section the voltage dynamics are represented for the upper and lower arms in the equations 4.11 and 4.12 respectively. The current dynamics across the inductor are determined from the Kirchhoff's voltage law and are shown in 4.21 for the upper arm, 4.22 for the lower arm.

$$\frac{L_u di_u}{dt} = \frac{V_{DC}}{2} - V_{ac} - R_u i_u - V_{ustack} \tag{4.21}$$

$$\frac{L_l di_l}{dt} = \frac{V_{DC}}{2} + V_{ac} - R_l i_l - V_{lstack} \tag{4.22}$$

4.4 1-phase alternate arm converter average model Simulation in Simulink

In this section 1-phase alternate arm converter average model is simulated in Simulink, by using mathematical expressions represented in section 4.3. Data to perform a simulation are shown in the Table 4.1. Some of the information of the model are taken from the source of "Reduced dynamic model of the Alternate arm converter" [29]. Arms inductance

and cell capacitance values are adapted from the paper [29] to this simulation model. The calculations for the number of modules in arm N_{cell} and number of series connected director switches N_{dir} are represented in the paper [30]. The resulting number of cells per stack, can be calculated by equation 4.23, where V_{ustack} is voltage of the upper arm modules and can be found from formula 4.17 and V_{cell} is the nominal voltage of a cell. The number of the director switches can be calculated according equation 4.24, where V_{dir} is a voltage peak across the director switches. According to the paper [30] the submodules and the director switches calculations presented only under the minimal requirement and normal operation. The additional margin of the number should be added with the different operations applied to each project.

Rated power P_r	20MW
DC Voltage V_{DC}	$\pm 10kV$
Converter AC voltage V_{ac}	10kV
Operating frequency f	50Hz
Arm inductor L_u and L_l	$100\mu H$
Cell capacitor C_{cell}	4mF
Cell voltage V_{cell}	1,5kV
Load R_{load}	2Ω
Number of cells in arm N_{cell}	9
Number of series Director switch N_{dir}	5

Table 4.1: Data of the 1-phase average model alternate arm converter

$$N_{cell} = \frac{V_{ustack}}{V_{cell}} \tag{4.23}$$

$$N_{dir} = \frac{\hat{V_{dir}}}{V_{cell}} \tag{4.24}$$

The paper [29] simulated the AAC in the point to pint connection. This paper showed reduced dynamic model, where the submodules were used as controlled voltage sources. Full scale model represented in [30] and reduced dynamic model simulation performance was compared. In the paper [29] the performance of the reduced dynamic model is faster, it was 17 times faster than the full scale model. The fault scenarios for the reduced dynamic model and full scale model closely matches in the paper. Master thesis aims to simulate and control average model of the AAC converter, by implementing it into point to point connection. The submodules are presented in more detailed mode, but the assumption that each submodule is balanced still valid, therefore the arm voltage balance is needed.

The simulation model is performed in the Simulink software. First of all the one phase simulation model is built with controlled voltage sources instead of the more detailed model in order to evaluate behaviour. In the Figure 4.6 model is represented. Here the simulation is performed imitating A phase of the converter with the 0° shift of the voltage, while the other other phases can be represented in the same way only the 120° phase shifted apart from each other.

In the Figure 4.6 upper and lower arms stack of the generated voltage are represented in the subsystem. The subsystem contains model of the voltage dynamics across the capacitors. Mathematical model of the voltage dynamics in the upper arm of the capacitors in the sub-modules is represented in the equation 4.11 and the equation 4.12 represents voltage dynamics for the lower arm. The Figure 4.7 illustrates generated voltage reference in the upper arm modules and Figure 4.8 - for the lower arm.

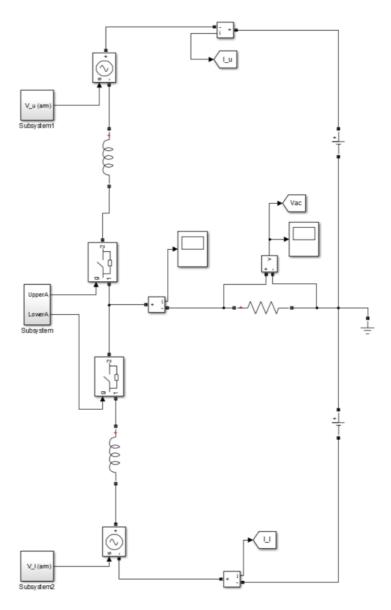


Figure 4.6: Average model of the alternate arm converter A phase in Simulink

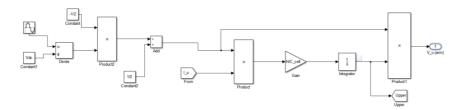


Figure 4.7: Average model of the upper arm stack voltage in Simulink

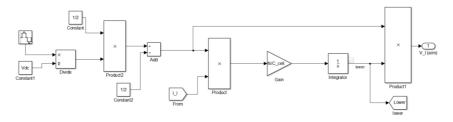


Figure 4.8: Average model of the lower arm stack voltage in Simulink

Referring to the Figure 4.7 and to the table 4.1, V_{ac} is inserted in the simulation as 10kV, the same amount as V_{DC} . The Simulink model are created for the equation 4.25 of the upper arm and 4.26 of the lower arm. These two equations creates either 0 or 1 depending on, which arm is conducting. Referring to the upper arm n_u is multiplied by the measured current in the upper arm i_u . The aggregated voltage dynamics in upper arm are inserted, where assuming the same voltage wave form for all the capacitors in the submodules. The multiplication of the n_u and i_u are integrated by time. The N is a number of the sub-modules inserted in the arm stack voltage. The integration results in the voltage of the capacitors in the upper arm. Integration and n_u product gives the voltage reference signal in the upper arm. For the lower arm the same Simulink model is presented in 4.26 with the minor change of the n_v , which is now refers to equation 4.26. The results of the voltage balance in the arms are represented in the Figure 4.9.

$$n_u = -\frac{1}{2} \frac{V_{ac}}{V_{DC}} + \frac{1}{2} \tag{4.25}$$

$$n_l = \frac{1}{2} \frac{V_{ac}}{V_{DC}} + \frac{1}{2} \tag{4.26}$$

The simulation is performed and most importantly the arm voltage balance is observed. The Figure 4.9 represents arm voltages without any balancing techniques. The red curve illustrates the voltage balance in the cell capacitors for the upper arm of the converter. The blue curve therefore refers to the voltage balance in the cell capacitors for the lower arm of the converter. As it can be seen the capacitors charges and discharges, without a balance till the voltage reaches its upper limits and then settles down. The arm voltages are not balanced at all.

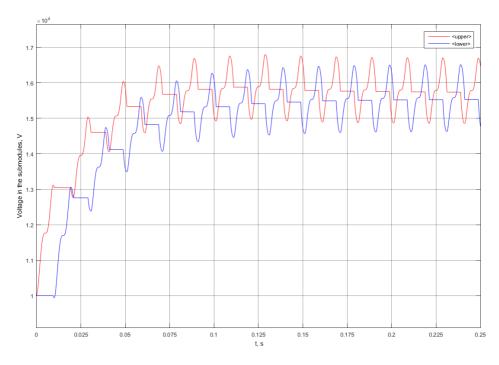


Figure 4.9: Voltage in the sub-modules for upper and lower arm without balancing techniques

The converter are simulated for the half-bridge connected cells. Half-bridge connected cells can only generate half of the voltage reference, while the full-bridge connected cells can produce positive and negative voltage reference. This allows generated AC voltage by the full bridge modules to be 2 times higher, than the V_{DC} voltage [30]. The Figure 4.10 represents simulation results of the arm voltage balance if the V_{ac} voltage will be generated by full-bridge modules. The red curve represents upper arm voltage and the blue curve illustrates lower arm voltage. Firstly, the capacitors are discharged and then they are charged till the certain level, where the voltage balance in the upper and lower arms are maintained. The balance are maintained in the upper limit of the voltage, however this forces capacitors in the submodules each time fully charge and discharge. The voltage fluctuations are high. The currents in the arms are distorted, therefore the output voltage will be not sinusoidal. In order to balance the voltage in the modules, the balancing techniques should be used. The most simple technique does not require any additional control feature. The balancing technique are achieved by the surplus of submodules connected in the half-bridge or submodules connected in the full-bridge, which can be considered if the DC voltage blocking capability is needed. In order to try out this balancing technique assumption that the half more submodules are needed in each arm. The voltage balancing technique called "sweet spot" will be mathematically derived and used in the following section.

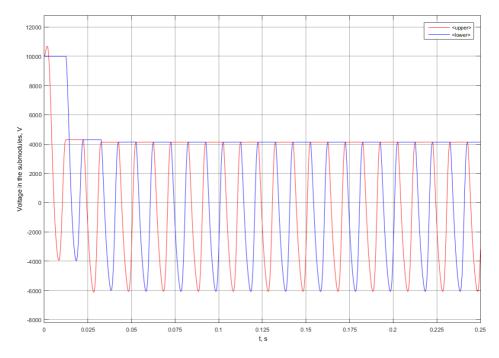


Figure 4.10: Voltage in the sub-modules for upper and lower arm with double AC voltage input

4.5 Sweet spot derivation and implementation in the average model

The "sweet spot" voltage is one of the arm voltage balancing techniques. The equilibrium of the energies from the AC side of the converter and the DC side of the converter should be satisfied. To achieve this the AC voltage should be 1, 27 times higher than the DC voltage. The idea behind "sweet spot" voltage balancing technique is guided by that amount of the AC voltage. "Sweet spot" derivation in order to achieve voltage balance in the arms is done in this section and proof of the arm voltage balance will be evaluated. The derivation are done for the one phase. It is also can be assumed for the 3 phase as the A phase, while other 2 phases B and C will be the same but shifted 120 and 240 degrees respectively.

When $V_A > 0$, which is A phase voltage in this case, is positive then the current in the A phase is defined by the upper arm current $i_u = i_{ac}$. When the $V_A < 0$, the voltage is negative then the current in the A phase will be defined by the lower arm current $i_l = i_{ac}$.

The power in the upper arm P_{upper} can be written as represented in equation 4.27, where i_u is current in the upper arm and v_u is voltage in the upper arm.

$$P_{upper} = i_u v_u (4.27)$$

Instead of the v_u the average voltage in the upper arm submodules will be used, assuming as the perfect balance of the capacitor voltages in the arms. The n_u is introduced,

where it is an average voltage either 1 or 0 of the upper arm voltage. Substituting $n_u \times V_{cu}$ in the equation 4.27 will result equation 4.29.

$$n_u = -\frac{V_{ac}}{2V_{DC}}i_u + \frac{i_u}{2} \tag{4.28}$$

$$P_{upper} = \left(-\frac{V_{ac}}{2V_{DC}} + \frac{1}{2}\right)V_{cu}i_u \tag{4.29}$$

Differentiating P_{upper} for the V_{cu} will result in the equation 4.30

$$C\frac{dV_{cu}}{dt} = -\frac{V_{ac}}{2V_{DC}}i_u + \frac{1}{2}i_u \tag{4.30}$$

Introducing Γ_i in the equation 4.31, where it is a step function, which will be positive when the current is flowing through the arm and 0, when the arm is not conducting. The cosine signal instead of the sinusoidal signal are used for the Γ_i , therefore the time when the upper arm is conducting are defined from $-\frac{\pi}{2}$ till $\frac{\pi}{2}$, which is the half of the conduction period. The graphic representation of the Γ_i and cosine wave form is in Figure 4.11.

$$\Gamma_i = \begin{cases} 1, & \text{if } -\frac{\pi}{2} \leqslant \omega t \leqslant \frac{\pi}{2} \\ 0, & \text{elsewhere} \end{cases}$$
 (4.31)

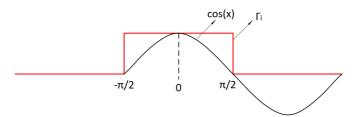


Figure 4.11: Cosine wave form and Gamma window representation

Integrating 4.30 for the one upper arm conduction period with the Γ_i window results in formula 4.32

$$CV_{cu} = \int_{-\frac{T}{4}}^{\frac{T}{4}} \left[-\frac{V_{ac}i_{ac}}{2V_{DC}}\Gamma_i \right] dt + \int_{-\frac{T}{4}}^{\frac{T}{4}} \left[\frac{i_{ac}}{2}\Gamma_i \right] dt$$
 (4.32)

The V_{ac} , i_{ac} and the T are represented respectively in the equations 4.33, 4.34, 4.35, where T is a period, V is max value of the voltage and I is max value of the current.

$$V_{ac} = V\cos\left(\omega t\right) \tag{4.33}$$

$$i_{ac} = I\cos(\omega t + \phi) \tag{4.34}$$

$$T = \frac{2\pi}{\omega} \tag{4.35}$$

By integrating first left part of the equation 4.32 together with the Γ_i window. Substituting equations 4.33, 4.34 and using product identities of trigonometry the equation 4.36 obtained.

$$-\frac{V_{ac}i_{ac}}{2V_{DC}} = -\frac{VI}{2V_{DC}} \frac{1}{2} \left[\cos\left(\omega t - \omega t + \phi\right) + \cos\left(\omega t + \omega t + \phi\right) \right] =$$

$$= -\frac{VI}{4V_{DC}} \left[\cos\left(\phi\right) + \cos\left(2\omega t + \phi\right) \right]$$
(4.36)

The result of the equation 4.36 is substituted in the equation 4.32 first integral part, which will result in the equation 4.37

$$\int_{-\frac{T}{4}}^{\frac{T}{4}} -\frac{VI}{4V_{DC}} \left[\cos\left(\phi\right) + \cos\left(2\omega t + \phi\right)\right] \Gamma_i dt = -\frac{VI}{8V_{DC}} \cos\left(\phi\right) \tag{4.37}$$

The second integral of the equation 4.32 will result in equation 4.38.

$$\int_{-\frac{T}{4}}^{\frac{T}{4}} \left[\frac{i_{ac}}{2} \Gamma_i \right] dt = \frac{I}{4\pi} \left[\sin\left(\frac{\pi}{2} + \phi\right) - \sin\left(-\frac{\pi}{2} + \phi\right) \right]$$
(4.38)

Applying trigonometry sum identities and integrating the equation 4.38 will result in equation 4.39.

$$\frac{I}{2\pi}\cos\left(\phi\right)\tag{4.39}$$

The full representation of equation 4.32 after integration will be equation 4.40.

$$C\frac{dV_{cu}}{dt} = \left[\frac{1}{2\pi} - \frac{V}{8V_{DC}}\right]I\cos\left(\phi\right) \tag{4.40}$$

The $C\frac{dV_{cu}}{dt}$ will be zero, when the $\cos{(\phi)}$ will be 0 or when the $\frac{1}{2\pi}-\frac{V}{8V_{DC}}=0$. The first option requires the case only of the reactive power flow, when the $\phi=\frac{\pi}{2}$. This is not an answer for this case, therefore only selection for this case will be the second, when $\frac{1}{2\pi}-\frac{V}{8V_{DC}}=0$. The V_{DC} is fixed here, therefore by solving this for V will result in the equation 4.41, where V is V_{ac} voltage.

$$V = \frac{4V_{DC}}{\pi} \tag{4.41}$$

The equation 4.41 is a "sweet spot" voltage. This results in the perfect balance of the arm voltages in the stacks. The sweet spot voltage is inserted in the simulation model, where V is the V_{ac} . The simulation results are represented in the Figure 4.12.

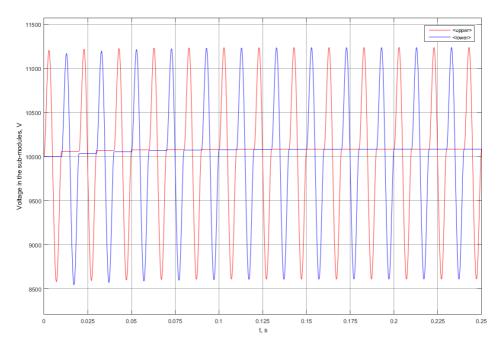


Figure 4.12: Voltage in the sub-modules for upper and lower arm with sweet spot voltage input

The perfect balance is maintained for the arm voltages. This allows easily balance the voltage between the arms, without using other techniques. The sweet spot can be achieved in the full-bridge module of the stack, because the full-bridge module allows to generate the higher AC voltage by two times. When the AC voltage generated in the stacks is 1,27 times higher than the V_{DC} voltage, the energy balance in the stacks can be naturally achieved, without using any other energy balancing techniques. This is the main advantage of the full-bridge connected stack cells [30], comparing to the half-bridge connection. The main drawback of the full-bridge, that the switching losses and the conduction losses are higher, due to the two additional switches (IGBT's) in the cell. Nevertheless in order to achieve the "sweet spot" voltage, the half-bridge connected modules can be used, if the amount of the modules are about 30% higher than the required, amount for the V_{ac} voltage generation. By using half-bridge modules and the 30% higher amount of them in order to reach the "sweet spot" V_{ac} voltage generation. This approach allows still to reduce the switching and conduction losses in the switches comparing with the full-bridge modules.

The "sweet spot" voltage generated in the stacks was maintained for the 3-phase average model of the alternate arm converter. The result of the each arm voltage are represented in the Figure 4.13. The converter is a 3-phase with only resistive load. In the beginning the arm voltages are a bit higher, due to initial conditions of the converter, but later on the values settle down and reach the balance. The figure bellow represents small portion of the simulation time from 1,7 to 1,8 seconds, it can be seen, that the voltages in the arms stays in the same magnitude and not fluctuating, therefore the voltages are kept in balance, when the "sweet spot" voltage is generated.

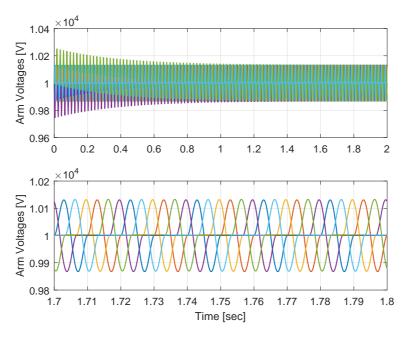


Figure 4.13: Arm voltages for upper and lower arms with a "sweet spot" voltage applied

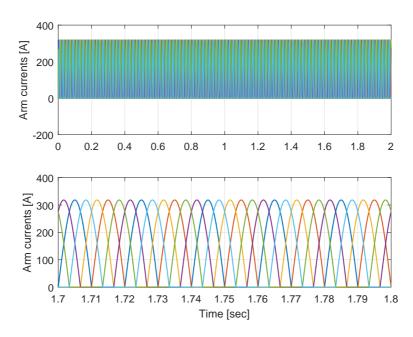


Figure 4.14: Arm currents for upper and lower arm with "sweet spot" voltage input

In the Figure 4.14 the currents for the upper and lower arms of the same 3-phase converter are represented. It can be seen the are currents are smooth and sinusoidal. However the measurements of the arm voltages and arm currents were taken of the island mode of 3-phase converter with the resistive load. The main drawback of the "sweet spot" voltage balancing technique is that it is hard to maintain and keep it stable. This balancing case is very sensitive to disturbance or any changes to the system. For example the resistance was introduced in the DC side and the arm voltage balance with "sweet spot" voltage was distorted. The new calculations should be made in order to account for DC side resistance. The accurate control can be implemented for control "sweet spot" voltage value value by taking into account a lot of the disturbances in the system In order to avoid unbalance by using this technique the precise control of the system should be implemented. The following section discusses another balancing technique called overlap time.

4.6 Implementation of the overlap in the average model

Another arm voltage balancing technique, which does not require additional sub-modules and can be implemented in the half-bridge connected modules. It requires only additional control feature, which controls the director switches, therefore the cheaper approach can be reached. However this leads to additional problems as control stability and circulating current, while both arms are in conduction. If the DC fault blocking is not required [30] the half-bridge connected cells are used. This approach allows to reduce conduction and the switching losses in the stacks. The half-bridge cell connection eliminates the opportunity to use the "sweet spot" arm voltage balancing technique, therefore arm voltage balancing technique with overlap time in the upper and lower arms can be considered.

The main idea behind it, is to use circulating current, which is flowing when the upper and lower arms are both in conduction process during the short amount of time. This can be done at the vary moment, when one arm delivers conduction to another. This generates a small amount of the dc current flowing through these arms across stacks capacitors. The current flowing to the dc side charges or discharges those cell capacitors. This will allow to exchange the energy between the stacks of the cells and the dc side of the converter [30].

The implementation of the overlap time control are illustrated in the Figure 4.15. First of all the output phase A voltage signal is compared with the negative constant through the switch. The small delay time should be implemented in the switches in order allow them to work synchronized with the output signal. For the upper arm the negative constant is compared to the output signal, when the negative constant signal is lower than the output voltage signal, then the pulse signal is provided in the upper arm, otherwise the provided pulse signal is 0. For the lower arm, when the positive constant signal is higher than the output A phase voltage signal, then the pulse signal is provided to the lower arm, otherwise the provided signal is 0. The signals are represented in Figure 4.16, where the red curve represents output AC voltage signal, blue - negative constant signal and the yellow - positive constant signal.

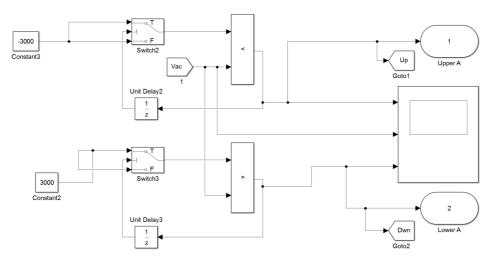


Figure 4.15: Overlap implementation in phase A for the upper and lower arms

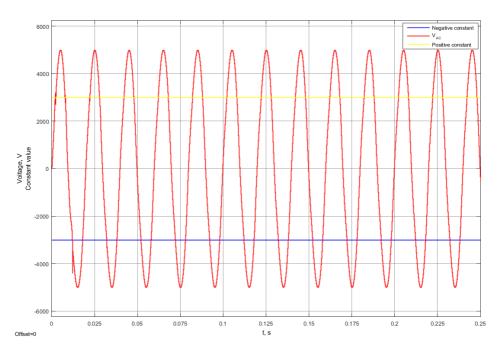


Figure 4.16: Signals provided to gain overlap

The Figure 4.15 illustrates 4.2 ms overlap, which results in the balanced arm voltages. The different overlap time were inspected for the one phase model. The results are represented in the Appendix A .1. The constant values were changed from 0 to 5100 with the step value of the 300. The constant values were chosen in a way that it should be in the

boundaries of the AC output voltage signal. Changed constant values resulted in the different overlap time from 0, when the constant is 0ms till 8.2ms, when the constant value was 4800. The constant value 5100 results in the unbalanced voltage, because it reached its upper AC voltage output limits determined by $\frac{V_{DC}}{2}$. The results represent voltage balancing in the arm voltages, with the different overlap time. The different overlap time results in the different time of the circulating current flowing across capacitors. As it can be seen the overlap depends on the constants value. The lower the negative constant and the higher is positive constant, then higher is overlap time. Furthermore the overlap can be regulated with the arm inductors, due to the current transition of the di/dt, therefore the overlap time is longer with the higher arm inductor value.

The ringing in the output voltage occurs. It can be seen in some cases from the Appendix A .1 ringing are very high in some are smaller. The ringing occurs, when the voltage drop occurs on the arm inductors. It creates a current running through it, when the current is interrupted by the switch, while it is not zero it creates an oscillations in the output voltage curve. At some of these points, which were examined, the interrupted current was higher, which led to the higher oscillations.

The case was simulated for the island model of the alternate arm converter, with the overlap time of 1 ms. The Figure 4.17 illustrates arm voltages of the converter. Balancing technique with overlap time comparing to the "sweet spot" balancing cause a fluctuations in some of the arm voltages, but in general the balance is maintained.

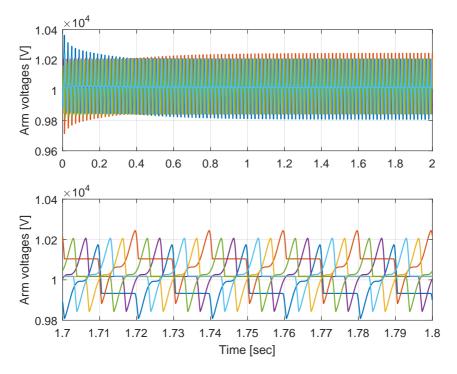


Figure 4.17: Arm voltages with 1 ms overlap implementation

The Figure 4.18 illustrates arm currents, when the overlap time is 1 ms. During the transition of the overlap time the current spikes appears, at this moment both arms are in conduction. At conduction moment, the running current of the DC side balances the arm voltages. The current spikes magnitude during the overlap time depends on the moment, when the current flowing across the arm inductor was interrupted, since the current across the inductor can not change immediately, due to the $\frac{di}{dt}$ transition.

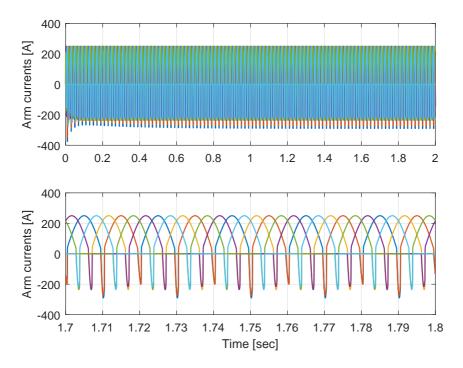


Figure 4.18: Arm currents with 1 ms overlap implementation

In this sense comparing overlap balancing technique and "sweet spot" balancing technique used in section 4.5, the less ringing effect are confronted in the "sweet spot" balancing case, but this technique is sensitive to the disturbances or changes in the circuit. In the following chapters related to the control and grid connection the overlap time balancing technique is used.



CONTROL STRATEGY OF AN ALTERNATE ARM CONVERTER

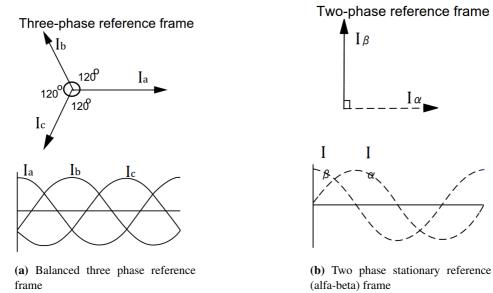
5.1 Park-Clarke transformation

Same as the machines, behaviour of the converters can be described by the current and voltage equations. The current and voltage are time varying variables, therefore the mathematical modeling of these variables become complex. In order to reduce the complexity such tools as mathematical transformations are used. The tools decouple variables and allow to solve equations associating time varying quantities, which refers to all variables for the same reference frame. As an example current variable will be used in this section, however the transformations can be used for any time dependent variable. The mostly used transformation methods are:

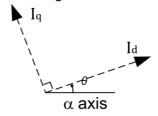
- Clarke transformation
- •Park transformation

Clarke transformation converts balanced three phase quantities represented in Figure 5.1a into balanced two phase quadrature quantities illustrated in Figure 5.1b. In the Figure 5.1a three phase balanced current quantities I_a , I_b , I_c are represented, with the angle of 120° between each other. The Figure 5.1b shows same three phase currents converted into two phase quadrature quantities in orthogonal stationary reference frame. The I_α is along α axis and I_β is along β axis, which is perpendicular to each other, but in the same plane as the three-phase reference frame [8].

Park transformation converts quantities from balanced two phase orthogonal stationary reference frame represented in 5.1b to orthogonal rotating reference frame illustrated in 5.1c. In Figure 5.1c orthogonal rotating reference frame, where the I_d current is at an angle θ (rotation angle) to the α axis and current I_q is perpendicular to I_d along q axis [8].



Rotating reference frame





(c) Two phase rotating reference (d-q) frame

Figure 5.1: Park-Clarke transformation [8]

The i_a, i_b, i_c represent instantaneous phase currents, where under balanced conditions it is 0, equation 5.1. Current space vector of these currents can be represented in equation 5.2, where $\vec{i_s}=i_\alpha+i_\beta$ the current in the stationary reference frame. a is the mathematical operator, which represents angle in complex plane $a=e^{j\frac{2\pi}{3}}$ and $a^2=e^{j\frac{4\pi}{3}}$. k is the constant typically $k=\frac{2}{3}$.

$$i_a + i_b + i_c = 0 (5.1)$$

$$i_s = k(i_a + ai_b + a^2i_c)$$
 (5.2)

By separating phase currents into real part and imaginary part. The formula for the α and β is obtained. The α plane represents the real part of the phase currents and the β plane represents the imaginary part of the phase currents. The equation 5.3 shows the transformation from the three phase currents to the two phase currents in the orthogonal stationary frame. The transformation matrix is known as Clarke transformation matrix.

$$\begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix} = k \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \times \begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix}$$
 (5.3)

Beside the stationary reference frame, the general reference frame, which rotates at the general speed ω can be formulated. An angle between d axis and the stationary reference frame α axis is θ . The current in the general rotating reference frame can be written as an equation 5.4. The d and q represents an axes of the general rotating plane, which is represented in the Figure 5.1c. Since the d and q axis rotates perpendicular together with a speed ω and creates an angle between rotating plane and stationary plane, with axes α and β . Therefore stationary reference frame can be transformed to the rotating reference frame. The transformation is called Park transformation and is written in equation 5.5 [31].

$$\vec{i_G} = \vec{i}e^{-j\theta} = i_d + i_a \tag{5.4}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \times \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$
 (5.5)

All signals with time dependent variables can be converted from a three phase frame to the stationary reference frame and then to the rotating reference frame using Clarke and Park transformation matrices. The opposite signal transformation is also possible. In the following sections mostly currents and voltages will be transformed into these, more suitable for control applications, reference frames

5.2 Implementation of the control strategy

The goal of the system control is to somehow control physical quantities in a way that ensures that the they take on the value that is specified. In other words it means that the system should adapt and follow specified values. Good control of the system must answer these questions: what should system do and how well is system doing control. In this section only two type of controls will be represented, because the control is implemented in DC/AC converter. The DC side is connected to the AAC, which creates AC that is connected to the R_{load} . The controllers are connected in the cascade, which makes them to be in hierarchy mode. The hierarchy of the controllers is defined by the speed. The faster

acting controllers are placed in the inner loop and slower controllers are placed in so called outer loop and every controller before the outer loop controller should be slower in order to have stable system. System is in island mode so that inner control, which typically is current and outer control, which typically is voltage, should be enough to control it. When the system expands the another controls, not only current and voltage should be implemented in the system to make it stable.

5.2.1 Inner current control

Usually inner controller should be faster than outer controller. In power converters controlled variables are currents on the inductors and voltages on the capacitors. The currents on the inductors are faster than the voltages on the capacitors, therefore the inner loop controls current and outer loop controls voltage [32]. First of all the abc current frame is transformed to the dq0 frame. Reference and measured current values are transformed. This approach is used due to the easier way of control, because the signals becomes constant dc values. After transformation current controller takes an error of the current between the reference and measured current values and provides it through the PI controller and the decoupling factors, which are compensated by the feed-forward loop. The general block diagram of the current controller is represented in the Figure 5.2. In this block diagram C represents PI controller, P refers to the plant (system performance) and F represents a filter, which will delay and filter the output signal. Each block of the controller are explained in the following subsections.

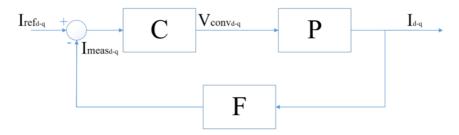


Figure 5.2: General block diagram of the current controller

5.2.2 PI regulator

PI regulator in the Laplace domain is represented in equation 5.6, where K_p is proportional gain, K_i- integral gain and $s=j\omega$

$$C(s) = K_p + K_i \frac{1}{s} = \frac{K_i}{s} \left(\frac{K_p}{K_i} s + 1 \right)$$
 (5.6)

The proportional and integral gain ratio can be written as a time constant $T_i = \frac{K_p}{K_i}$, which is specified as a design parameter.

5.2.3 Filter

Filter in the controller is represented in order to delay measured signal and to filter out some noise for the better performance of the control. The general diagram of the filter are illustrated in the Figure 5.2. Since the model is a discrete signals instead of the continuous integrator the discrete one are used in the Simulink. The sampling time is $T_s=50\mu s$, which is very small and the simulation can be considered as continuous. This will justifies the continuous operators s used in the equations.

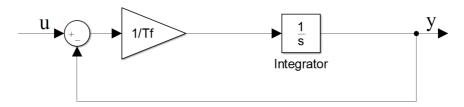


Figure 5.3: Filer representation in the Simulink

The transfer function of the filter in the Laplace domain can be written as shown in the equation 5.7, where $s=j\omega$ and T_{fi} is a filter time constant, which is design parameter mostly specified referring to the small portion of the switching period.

$$F(s) = \frac{1}{T_{fi}s + 1} \tag{5.7}$$

5.2.4 System

The system can be written as shown in the equation 5.8 for the d axis. The equation 5.9 shows system for the q axis.

$$V_{c,d} = \frac{L_u di_d}{dt} + R_{load} i_d + R_u i_d + \omega L_u i_q$$
(5.8)

$$V_{c,q} = \frac{L_u di_q}{dt} + R_{load} i_q + R_u i_q - \omega L_u i_d$$
(5.9)

In order to obtain a good performance of the controller and separately control d current and q current, the decoupling terms are introduced in the current controller. The d and q axis have speed/frequency induced terms respectively ωL_d and ωL_q . The decoupling terms allows to eliminate the ωL_d and ωL_q in the vector control. The opposite signs ωL_u as noted in the equation 5.8 is written for the d axis, were in this case results $-\omega L_u i_q$. The same thing is done with the equation 5.9 for the q axis, where the decoupling term is inserted as $+\omega L_u i_d$. Therefore the system will be represented in a two separate d and q reference frames. The system consists with the resistive load only, arm resistor and arm inductor. Considering upper arm is in conduction and the system are decoupled for the d and q axis, therefore equation 5.10 results system in a d axis and equation 5.11 results system in the q axis, where V_{dac} and V_{qac} are voltage across the load in the d and q axis

respectively, R_{load} and R_u are resistors in the load and in the upper arm respectively, during conduction load resistor and upper arm resistor are in the series connection therefore, both resistors can be added and be considered as one resistor just R_{load} . L_u represents upper arm inductor.

$$V_{dac} = \frac{L_u di_d}{dt} + R_{load} i_d + R_u i_d \tag{5.10}$$

$$V_{qac} = \frac{L_u di_q}{dt} + R_{load}i_q + R_u i_q \tag{5.11}$$

As it can be seen equations 5.10 and 5.11 are the same only the current axis is different, therefore only d axis will be represented further since the q axis has the same representation and just copied and presented in q axis of the simulation. The decoupling terms of the current controller are illustrated in the Figure 5.4.

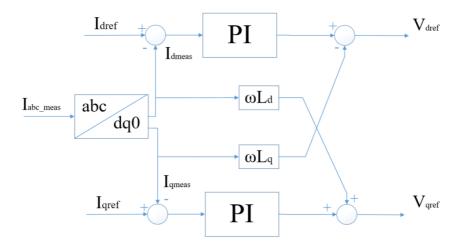


Figure 5.4: Decoupling terms representation in ICC

In order to find systems transfer function equation 5.10 is transformed to the Laplace function and represented in equation 5.12. The transfer function of the plant P in Laplace function are represented in the equation 5.13, where $R_{load} + R_{uarm} = R_{loadua}$

$$V_{dac(s)} = (L_u s + R_{load} + R_u)i_{d(s)}$$
(5.12)

$$P(s) = \frac{1}{L_{uarm}s + R_{loadua}}$$
 (5.13)

5.2.5 Tuning of the regulator

Referring to the Figure 5.2, where the each block elements are represented as a transfer functions. Using these transfer functions PI controller can be tuned. The tuning is the

process of setting optimal values for proportional and integrator gains in order to get the best performance close to ideal of the PI controller. There are many methods how the PI regulator can be tuned. The most simple methods are "guess and check" or Ziegler-Nichols method [33]. In the first method the gains are just guessed by following some thumb rules. The second one Ziegler-Nichols method is when the all gains are set to zero except the proportional, which is increased until the loop starts to oscillate. The proportional gain are then noted together with the oscillation period and other gains of the regulator are adjusted according to tables [33]. In this section two methods of the tuning are tried. One is so called "guess and check" with some assumptions of the transfer functions. Another one is Modulus optimum method. This method is widely used for the voltage source converters for the inner current controllers, due to the fast response and simplicity [34]. The idea behind the method is to cancel out the dominant pole, while achieving the highest cutoff frequency and still staying in the systems constraints [35]. The measurements and the system outputs are taken at the point after the filter F. The output of the signal is chosen at this point, due to the better performance of the signal and filter some noise. This consideration of the system sets up C, P and F blocks in series, where the open loop transfer function $G_{ol}(s)$ of the controller becomes as represented in equation 5.14.

$$G_{ol}(s) = C(s)P(s)F(s)$$
(5.14)

The first tuning method is used with some assumptions, which neglects the arm inductor, because it is very small value referring in the table 4.1. This assumption results in the 1st order approximated function. Another assumption is that time constant of the filter is setup to the value $T_{fi}=0.002s$. In this method the plant $P(s)=\frac{1}{R_{loadua}}$. By placing equations 5.6, 5.7 and $P(s)=\frac{1}{R_{loadua}}$ into equation 5.14. The open loop transfer function represented in equation 5.15 is formed, where $\frac{K_p}{K_i}=T_i$ and assuming that T_i time constant is equal to filter's time constant T_{fi} , $T_i=T_{fi}$. The poles cancel each other and the open loop transfer function can be rewritten as equation 5.16.

$$G_{ol}(s) = \frac{K_i}{s} \left(\frac{K_p}{K_i} s + 1\right) \frac{1}{R_{loadua}} \frac{1}{T_{fi}s + 1}$$

$$(5.15)$$

$$G_{ol}(s) = \frac{K_i}{s} \frac{1}{R_{loadua}} \tag{5.16}$$

The closed loop G_{cl} transfer function is represented in the equation 5.17. The $\frac{1}{R_{loadua}}$ can be rewritten as K, which simplifies equation.

$$G_{cl}(s) = \frac{\frac{K_i K}{s}}{1 + \frac{K_i K}{s}} \tag{5.17}$$

By simplifying equation 5.17 it results in equation 5.18.

$$G_{cl}(s) = \frac{1}{\frac{s}{K_i K} + 1} \tag{5.18}$$

In equation 5.18 assuming $K_iK=\frac{1}{T_{eq}}$ as T_{eq} being an equivalent time constant, which is the first order approximation of closed loop current controller response, $T_{eq}=0.05s$.

The integral gain for the PI controller can be calculated referring to equation 5.19 and therefore the proportional gain results in equation 5.20.

$$K_i = \frac{1}{T_{eq}K} = 400, 2 (5.19)$$

$$K_p = T_{fi}K_i = 0,8004 (5.20)$$

The integrator and proportional gains are entered in the inner current control PI regulator, the same values for the d and q current axis. The setup of the ICC is modeled in Simulink-Simscape and the results are represented in the Figure 5.5.

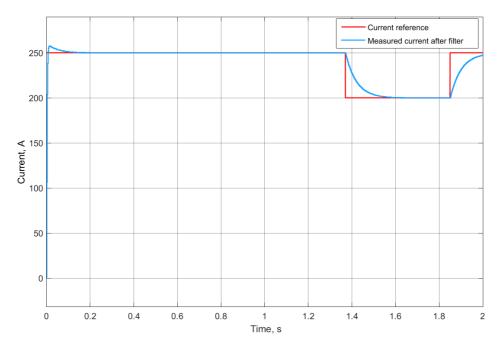


Figure 5.5: Response of the ICC for the first order system

The red line represents current reference with disturbance, which takes time between 1,37s and 1,85s. The blue line represents PI regulator response in ICC for the current d axis. As it can be seen the response follows the reference signal. The oscillations do not appear and 0,505% undershoot is noticed during disturbance. However the slow speed of the response is observed during disturbance, therefore the second tuning method modulus optimum is adapted below.

Tuning technique of the modulus optimum method. In this method the arm inductor is included in the systems transfer function, which is governed in equation 5.13. The value of the arm inductor is specified in Table 4.1. This leads to the second order approximated function for the controller. The time constant of the filter $T_{fi}=0.002s$. By placing equations 5.6, 5.7 and 5.13 into equation 5.14. The open loop transfer function is formed

in equation 5.21, where assuming that $\frac{K_p}{K_i} = T_i$ and assuming that T_i are equal to the $\frac{L_u}{R_{loadua}}$ time constant, $T_i = \frac{L_u}{R_{loadua}}$, therefore the poles will cancel each other and the open loop transfer function can be rewritten as equation 5.22.

$$G_{ol}(s) = \frac{\frac{K_i}{s} \left(\frac{K_p}{K_i} s + 1\right) \frac{1}{R_{loadua}}}{(T_{fi}s + 1) \left(\frac{L_u}{R_{loadua}} s + 1\right)}$$
(5.21)

$$G_{ol}(s) = \frac{\frac{K_i}{R_{loadua}}}{s(T_{fi}s+1)}$$

$$(5.22)$$

The closed loop transfer function results in equation 5.23. Dividing equation 5.23 top and the bottom by T_{fi} , the transfer function results in equation 5.24.

$$G_{cl}(s) = \frac{\frac{K_i}{R_{loadua}}}{T_{fi}s^2 + s + \frac{K_i}{R_{loadua}}}$$

$$(5.23)$$

$$G_{cl}(s) = \frac{\frac{K_i}{T_{fi}R_{loadua}}}{s^2 + \frac{s}{T_{fi}} + \frac{K_i}{T_{fi}R_{loadua}}}$$
(5.24)

The numerator of the equation 5.24 setting in the general second order system results in formula 5.25, where ζ is a damping coefficient set to $\zeta=\frac{1}{\sqrt{2}}$ for suitable overshoot and ω_n is a frequency of the natural oscillation [36] and here it will be equal to $\omega_n=\sqrt{\frac{K_i}{T_{fi}R_{loadua}}}$. Therefore the integral gain will result in equation 5.26. The proportional gain from the $\frac{K_p}{K_i}=T_i$ and $T_i=\frac{L_u}{R_{loadua}}$ outcomes in to equation 5.27.

$$s^{2} + \frac{s}{T_{fi}} + \frac{K_{i}}{T_{fi}R_{loadua}} = s^{2} + s2\zeta\omega_{n} + \omega_{n}^{2}$$
 (5.25)

$$K_i = \frac{R_{loadua}}{2T_{fi}} = 5002, 5 (5.26)$$

$$K_p = K_i \frac{L_u}{R_{loadua}} = 0,025$$
 (5.27)

The integrator and proportional gains are entered in the inner current control PI regulator, the same values for the d and q current axis. The setup of the ICC is modeled in Simulink-Simscape and results are represented in the Figure 5.6.

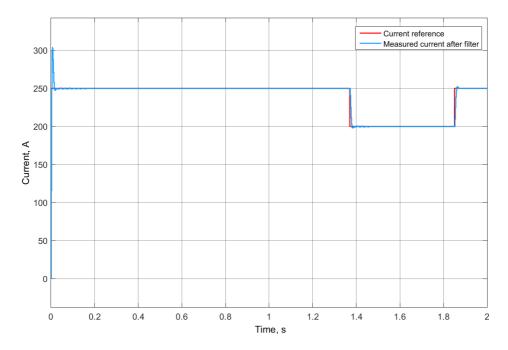


Figure 5.6: Response of the ICC for the second order system

The red line represents current reference with disturbance, which takes time between 1,37s and 1,85s. The blue line represents PI regulator in ICC response for the current d axis. As it can be seen the response follows the reference signal very well. The short oscillations appears, but it is quite well damped, the 3,646% undershoot during disturbance is noticed. The 3,646% undershoot is in boundaries of 4,3% for the PI regulator [37]. Since the systems response and oscillations are in boundaries, therefore this optimization method is better than only using the assumptions and resulting in the first order system. Comparing Figure 5.5 with the Figure 5.6 it can be seen that the systems response to the disturbance in the second Figure is way faster than in the first Figure. Despite some oscillations the gains of the modulus optimum tuning technique will be used further for ICC.

5.3 Voltage control

The inner control loop is designed as the current controller and the outer controller is represented as voltage controller in this section. Controllers are connected in cascade, where the several measured signals aims to control one variable. The cascade control is achieved by nesting control loops. In this situation the AC voltage is the controlled variable and it controls AC voltage and current. The current control loop is called the secondary control and usually is much faster than the outer control loop called primary control. The cascade control can also consist of more than two nested loops [33] [38]. The secondary loop reacts to disturbance much faster than the outer loop, but the outer loop is much more

precise, therefore the secondary controller deals with remaining disturbance signal. The rule of thumb that the ratio between the inner and outer loops should be at least 5 times [33]. The voltage control implemented in the system are represented in the Figure 5.7. In this diagram C represents voltage PI regulator, ICC is inner current control loop and G is the gain, which is in this case are load resistance and arm resistance in series, the filter in outer loop control is 10 times lager, than for current control, therefore the time constant is 10 times slower.

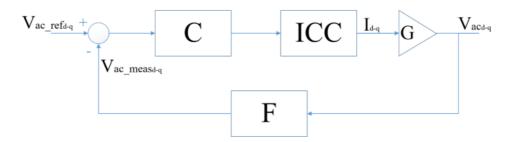


Figure 5.7: General block diagram of the voltage control

The PI regulator is represented in equation 5.6. G is represented in equation 5.28. The filter in this case is represented as the voltage filter and is shown in equation 5.29

$$G(s) = R_{load} + R_u (5.28)$$

$$F(s) = \frac{1}{T_{fv}s + 1} \tag{5.29}$$

The approximation of the ICC transfer function is determined as simplified first order equivalent time constant T_{eq} [34]. By neglecting one pole and equating the error of two transfer functions, one from equation 5.25, where $2\zeta\omega_n=\frac{1}{T_{fi}}$ and the second is approximated to the first order transfer function $\zeta\omega_n=\frac{1}{T_{eq}}$. This results in equation 5.30 and equivalent equation is shown in 5.31.

$$\frac{2}{T_{eq}} = \frac{1}{T_{fi}} \tag{5.30}$$

$$T_{eq} = 2T_{fi} (5.31)$$

The transfer function of ICC in Laplace domain is represented in equation 5.32

$$ICC(s) = \frac{1}{T_{eq}s + 1} \tag{5.32}$$

As for the secondary loop the measurements and the systems output are taken at the point after the filter F. The output of the signal is chosen at this point, due to the better performance of the signal and filtered noise. This consideration of the system will set up C, ICC, G and F blocks in series, where the open loop transfer function $G_{ol}(s)$ of the outer

controller becomes as represented in equation 5.33. The full representation of the open loop primary control transfer functions is shown in equation 5.34.

$$G_{ol}(s) = C(s)ICC(s)G(s)F(s)$$
(5.33)

$$G_{ol}(s) = \frac{\frac{K_i}{s} \left(\frac{K_p}{K_i} s + 1\right) (R_{load} + R_u)}{(T_{eq} s + 1)(T_{fv} s + 1)}$$
(5.34)

In order to optimize the open loop transfer function the approximated current control equivalent time constant is equating to PI regulators time constant $\frac{K_p}{K_i} = T_{eq}$ from the equation 5.34. This will result in cancellation of the transfer functions. After the cancellation closed loop transfer function is represented in equation 5.35. In this case the time constant of the filter inside the ICC and accounted together with equivalent time constant T_{eq} is $T_{fi} = 0.0002s$, therefore it is not visible in these equations. The voltage filter time constant $T_{fv} = 0.002s$ since the voltage controller should be slower than the current controller.

$$G_{cl}(s) = \frac{\frac{K_i(R_{load} + R_u)}{s} \frac{1}{T_{fv}s + 1}}{1 + \left(\frac{K_iR_{load} + R_u}{s} \frac{1}{T_{fv}s + 1}\right)}$$
(5.35)

By doing the same steps as for a current controller the integral gain of the regulator will result in equation 5.36 and the proportional gain for the PI regulator results in equation 5.37

$$K_i = \frac{1}{2(R_{load} + R_u)T_{fv}} (5.36)$$

$$K_p = K_i T_{eq} (5.37)$$

The integrator and proportional gains are entered in the outer voltage control PI regulator, the same values for the d and q current axis. The setup of the OVC is modeled in Simulink-Simscape and the results are represented in the Figure 5.8.

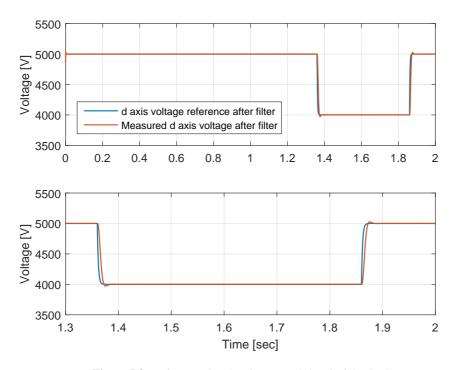


Figure 5.8: Reference signal and measured signal of the OVC

The blue line represents voltage reference with disturbance, which takes time between 1,37s and 1,85s. The red line represents outer voltage control systems response for the voltage d axis. As it can be seen the response follows the reference signal. The short oscillations appears, but it is quite well damped, the 2,577% undershoot during disturbance is noticed. The 2,577% undershoot is in boundaries of 4,3% for the PI regulator [37], so the oscillations of the system response are in boundaries.

The secondary loop behaviour with OVC is represented in Figure 5.9. In this Figure 5.9 d axis current reference signal is represented. In blue and the red curves are measured values of d axis current, both signals are measured after filtering. In this graph can be seen that the measured value of ICC follows reference signal, because response to disturbance is fast. However this fast response cause small oscillations and higher than 4,3% undershoot. In this case the undershoot is 4,737%. Fast response of the secondary controller outweigh higher than required undershoot. The undershoot is attenuated in the primary controller, where the speed of the measured signal is slower, but the accuracy is higher and undershoot is reduced.

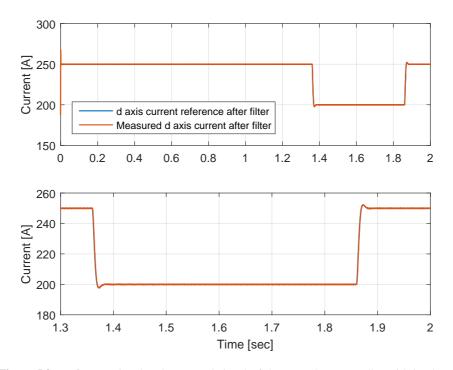
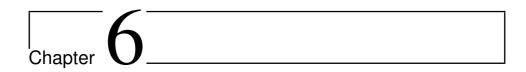


Figure 5.9: Reference signal and measured signal of the secondary controller with implemented primary control



ALTERNATE ARM CONVERTER IN THE POINT TO POINT CONNECTION

In this chapter the alternate arm converters are considered to be connected to a point to point HVDC scheme. The scheme is represented in Figure 6.1. The type of connected system is represented in paper [39]. The paper represents a new HVDC network system for electromagnetic transient analysis. The scheme is used for HVDC power system dynamic studies in order to test behaviour and interactions with the converter [39].

As it can be seen in the Figure 6.1 the AC grid 1 is connected to the AC grid 2 via 20 kilometres of the HVDC link. The various cases can be represented as point to point connection onshore or only offshore, but in this case is considered of mixing offshore and onshore connection. Since the study focuses on power transmission, a simplified dynamic model of the alternate arm converter terminals T1, T2 are used. The behaviour of DC link voltages are investigated in several power flow cases.

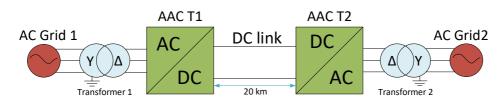


Figure 6.1: Block diagram of the point to point connection

6.1 System components

The components of the system and control are described in this section. The system and converter parameters are represented in the table 6.1. Considering in this case power flow from AC Grid 1 to AC Grid 2. The AC Grid 1 is connected through the transformer 1. The primary voltage side is way grounded connection type. The secondary side is delta connection. Transformer 1 connects secondary voltage side to the alternate arm converter terminal 1. The AAC T1 converts AC to DC and via DC link connects to another alternate arm converter terminal 2, which converts DC to AC. The terminal 2 converter is connected through transformer 2 to the AC Grid 2. The transformer 2 primary side is connected in delta. The secondary side of the transformer is way grounded and connected to AC Grid 2. The power reversal case will force the power flow from AC Grid 2 to AC Grid 1, therefore for this notation the transformers primary and secondary side changes.

Parameter	Value	Unit
Base power S_b	20	MVA
DC Voltage V_{DC}	±10	kV
Operating frequency f	50	Hz
AC voltage line-line V_{acLL}	11	kV
Source inductance L_s	0.3	mH
Source resistance R_s	0.3	$m\Omega$
Grid resistance R_g	60, 5	$m\Omega$
Grid inductance L_g	4,1	mH
Arm inductance L_u, L_l	100	μH
Number of series Director switch N_{dir}	5	
Cell capacitor C_{cell}	4	mF
Cell voltage V_{cell}	1,5	kV
Number of cells in arm N_{cell}	9	
Overlap time/angle $t_{overlap}/\angle$	1/9	$ms/^{\circ}$

Table 6.1: System and converters parameters

6.1.1 Converter

The alternate arm converters are used as the topology in this simulation in order to test its behaviour. The two similar alternate arm converters are implemented in the system as terminal 1 and terminal 2. The parameters of the converter are represented in table 6.1. The simplified dynamic model is simulated for this grid test system [29]. Assuming, that the voltage in the stack of the cells across the capacitor is balanced, the reduced dynamics mathematical model of AAC represented in section 4.3.

Three phase alternate arm converter topology used in this simulation is illustrated in Figure 6.2. The arms are identical and have arm resistor, arm inductor, director switch and stack of the cells. The stacks are series connected half bridge cells as represented in Figure 6.2 top, miniature picture. The director switches consist of several IGBT connected in

series, in order to withstand higher voltage ratings. The assumption of the current direction in grid connected application is illustrated in the Figure 6.2. The red arrows illustrate grid current and the light blue arrows show current flow direction of the arms.

The transformers of the system are represented as the R_g and the L_g together with the grid side resistance and grid side inductance for the each phase.

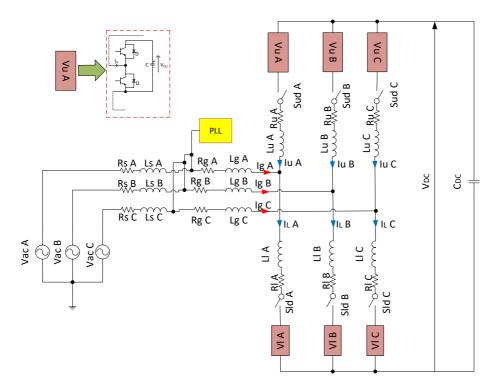


Figure 6.2: AAC 3-phase model

6.1.2 Point to point connected converters control

The converter consist of the several controls. The required controls are phase locked loop controller, current controller, active- reactive power controller, droop controller, overlap controller and additional if needed "sweet spot" voltage controller.

PLL controller

Phase locked loop controller is used as Simulink block and placed in the converter as shown in the Figure 6.2. PLL constantly adjust a voltage in order to lock onto the phase and frequency of an input signal, therefore the frequency is kept stable for the output. Furthermore the PLL is used to extract voltage phase angle for the following used d-q0 transformation.

Inner current controller

In order to simplify signals for inner and outer loop controllers, d-q0 transformation is used. The abc reference frame is transformed to the rotating d-q0 reference frame. The resulting constant signals are provided into controllers. The transformation is explained in section 5.1. The droop, outer and inner controllers are represented in Figure 6.3. The inner controller controls current and its tuning is represented in section 5.2. Following the current direction assumption for the grid connected application mentioned in subsection 6.1.1. The signs for common coupling and the grid measured voltage are opposite comparing with the case in section 5.2, but the rest, are the same. The grid measured voltage is introduced in this control in order to achieve a better performance of the control and avoid the high changes of the controllers value if the grid voltage will fluctuate often. Therefore the grid voltage and measured part of the grid voltage cancel each other and only a small deviation will be needed to control.

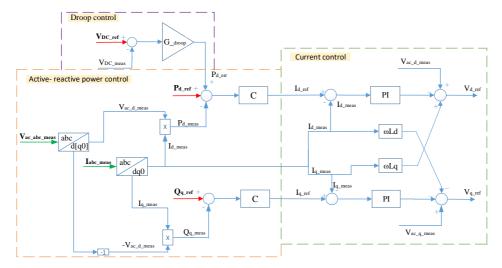


Figure 6.3: Droop, outer and inner controllers

Outer active reactive power controller

The active and reactive power control is implemented as the outer loop control. The similar tuning and block diagram as introduced in section 5.3 will be used, but the gain (G) in this case will be the AC phase voltage. The filters are used for each outer loop control signal. Since the primary control should be slower than the secondary control, the filters time constants are 2ms. The active- reactive power controller is represented in Figure 6.3. Active power controls current d reference frame and the reactive power controls q reference frame of the current controller. Considering power invariant case measured power in rotating d-q0 reference frame can be calculated according to equations 6.1, 6.2 for active and reactive power respectively [40]. The gain $\frac{3}{2}$ before each power is not represented in the Figure 6.3 directly. It is assumed that this gain is already accounted for in this Figure. This value is only the gain therefore the further simulations it should not

affect. For the more accurate and mathematically correct simulations the gain should be implemented in the future work.

$$P_{d_meas} = \frac{3}{2} (V_{ac_d_meas} I_{d_meas} + V_{ac_q_meas} I_{q_meas})$$
 (6.1)

$$Q_{q_meas} = -\frac{3}{2} (V_{ac_d_meas} I_{q_meas} + V_{ac_q_meas} I_{d_meas})$$

$$(6.2)$$

When the PLL is used in the system the voltage q axis is controlled to 0, therefore the simplified equations of 6.1, 6.2 are represented in 6.3, 6.4 respectively. At the point of common coupling the voltage can be made constant, so as it can be seen from equations, only the current left to be controlled [41].

$$P_{d_meas} = \frac{3}{2} (V_{ac_d_meas} I_{d_meas})$$
(6.3)

$$Q_{q_meas} = -\frac{3}{2}(V_{ac_d_meas}I_{q_meas})$$
(6.4)

By using equations 6.3, 6.4 the measured values of the active and reactive power can be calculated. The reference values of the outer loop controller are decided according system parameters. Reference and measured values of the power are compared and the error signal is passed through the PI controller (C). The signal after PI (C) provides the reference current signals for the secondary control, where the active power will be I_d current reference signal and reactive power will be I_q current reference signal.

Droop control

Current flowing in the DC side capacitor charges and discharges it, therefore the DC voltage is not a constant value as it was assumed in the beginning of the modeling a simulation. The DC voltage increases and decreases. When the power production increases, the DC voltage overshoot is noticed and, when the power decreases the undershoot in DC voltage appears. In other words from the point of view of DC voltage control, the power changes cause the voltage fluctuations [38]. Control of the DC voltage can be managed through the control of the power exchanged by the converter with the grid or through the control of DC/DC converter [38]. The second case will not be considered, because the converter does not play any role in regulating a DC link [38]. The first case, when the control is managed through the power exchange between the converter and the grid causes challenges to achieve it in multiterminal system. If DC voltage control is used in multiterminal system, each of the converter regulates their own DC voltage individually, because the power changes are different in the each converter connection. This cause a chaos between the converters, because each of them tries to adjust DC voltage individually. The solution for this can be, that one of the converters is labeled as master and others are labeled as slaves. In this case the master converter only regulates the DC voltage. The main drawback of this solution, that the master converter should be oversized in order to compensate all the slave converters power changes and adapt control for DC link. This results in higher power ratings of the converter and therefore size. Another drawback of this solution is the failure

of the master converter. If the failure is observed, all the multiterminals slave converters should be shut down, because the DC voltage control can not be achieved anymore and slave converters start to pull each other. Therefore the safer option in multiterminal systems is to implement the droop control.

Considering that this system in the future work will be used as multiterminal the droop control is used, due its simplicity and its effectiveness. The novel approach of the droop control was firstly introduced in [42], where the current sharing and voltage regulation was greatly improved. The case for the connected parallel inverters frequency and voltage control is discussed in the paper [43], where the frequency droop is controlled by synchronizing the power source with the grid with a phase angle difference and voltage droop controlled by imitating voltage source with finite-output impedance. The different droop controls are summarized in the paper for the microgrid case [44]. In this review the frequency or omega is controlled by active power and the voltage is controlled by the reactive power. Considering the advantages, simplicity and multiterminal approach for this study the DC voltage droop control is implemented for the active power. Therefore the outer loop active power is supervised by the droop control. The droop control of the DC voltage is represented in Figure 6.3.

The main idea behind the droop controller is shown in Figure 6.4, where the V_{DC} is DC voltage, P_{max} in this case is with power factor of 1, therefore $S_b = P_{max}$ and ρ is the DC voltage drop percentage. When the active power increases to its maximum values the DC voltage should drop by the amount of ρ and if the voltage increases the less power should be provided. Typical value of ρ is 5-10%.

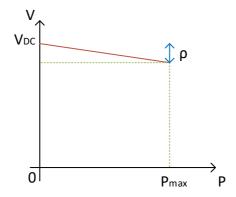


Figure 6.4: Droop control characteristic

The gain for the droop value (G_{droop}) can be calculated by using equation 6.5, where the $S_b=P_{max}$. As it can be seen from the equation if the DC voltage is allowed to decrease by 10%, the gain of the droop becomes smaller.

$$G_{droop} = \frac{S_b}{\rho V_{DC}} \tag{6.5}$$

Overlap control

Overlap controls the director switches in a way that the upper and lower arms director switches are closed at the same time for the small time period. It causes the DC current flow in both arms at the same time, which helps to balance arm voltages. The explanation and implementation of the overlap time control is explained in section 4.6. The minor changes are made in this overlap control model. The control is implemented into AC voltage signal.

The flow charts for the overlap control are illustrated in the Figure 6.5 and the MAT-LAB/Simulink implementation is represented in Figure 6.6. As it can be seen in the Figure 6.6 the 3 phase AC voltage signal is compared with the negative constant value and with the positive constant value. The constant values can be calculated by using equation 6.6, where the $V_{overlap}$ is the constant values and are $V_{overlap} = pos_constant$ or $V_{overlap} = neg_constant$, V_{phac} is a phase AC voltage, ω is angular rotating frequency, $t_{overlap}$ is the decided overlap time, usually in milliseconds. The small adds and subtracts in the constants, allows to compare values momentary. The voltage signal is sent to SR flip flop set port if it is greater, than the negative constant value with small add and SR flip flop gives the output. If the AC voltage signal is smaller than the negative constant value with small subtract it resets SR flip flop. The similar but opposite comparison is adapted for comparing the AC voltage signal and the positive constant.

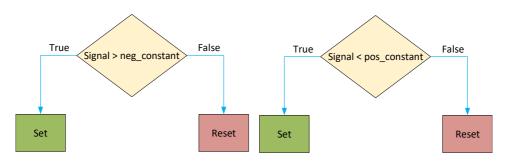


Figure 6.5: The flow chats of the overlap

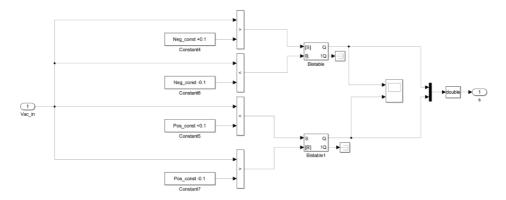


Figure 6.6: Overlap control implementation in MATLAB/Simulink

$$V_{overlap} = V_{phac} \sin(\omega t_{overlap} 0.5) \tag{6.6}$$

"Sweet spot" voltage control

The "sweet spot" voltage control is a type of the control where the generated AC voltage in the stacks is 1.27 times higher, than the DC voltage. This allows to match the energy balance in AC and DC side. The "sweet spot" voltage point is derived in the section 4.5. In the same section 4.5 it is implemented in the 1-phase model and in the 3-phase model. The problem with this control was observed, when the AC voltage changes. The small oscillations of the AC voltage caused the instability of the voltage balance in the arms. The one solution to deal with this problem the precise control of AC voltage, but it can be not enough because voltage drops in the elements also cause instability. Considering this and focusing on the various type of the voltage control, this type of control is not investigating further.

6.1.3 Cable

A different cable and transmission line modeling techniques can be found depending on the various study cases. Some of them going in different depths of the modeling. The most used modeling techniques are pi equivalent model and frequency- dependent model [45]. Values of the cable are represented in table 6.2. The length and the resistance are referring to the paper [29]. Each of the converters DC side capacitance is calculated. The equation of energy stored in the capacitors during 10ms is represented in equation 6.7.

Parameter	Value	Unit
Resistance	11,3	$m\Omega/km$
Capacitance	2	mF
Length	20	km

Table 6.2: Cable parameters.

$$\frac{1}{2} \frac{C_{DC} V_{DC}}{S_h} \le 10ms \tag{6.7}$$

The nature of my study case is control and low frequency dynamics. The length of the link is short (20 km). Focusing on high frequency transients in this case is not that important, therefore the frequency-dependent model, will not be applied in this thesis. The DC link is modeled as simple pi equivalent cable model [46]. The resistance of the cable is calculated by multiplying length and the resistance given in table 6.2 per kilometer. The total capacitance of the cable and both filters of the converters is 2mF, by implementing pi equivalent model, the capacitance is divided in two equal parts for the both sides of the link. The one side of the capacitance contains 1mF, while the other will be similar.

6.2 Study cases

The study cases investigate behaviour of the converters and the system.

- The first case shows the behaviour of the converters, when different active power ratings and the reversed active power flow is applied in point to point connection. The generation and performance of the system is investigated, when only reactive power in both of the converters are generated or absorbed. The detailed power scenarios will be explained in the subsection 6.2.1.
- The second study case refers to the DC side capacitance. The capacitor in the cable and filter will be assumed as one capacitance in the point to point connection. The overall capacitance is designed as lumped element. Mostly DC side voltage effect and interesting observations will be represented in the subsection 6.2.2.
- The third case investigates the droop control behaviour with different values of ρ . The ρ is a value by which the drop is govern in the droop control. The droop control was represented in subsection 6.1.2. The investigation and observations will be show in the subsection 6.2.3.
- The forth case provides information and observations of the arm voltages by extending overlap time. The time of the overlap will be changed till the 1 cycle of circulating current will be reached, this means till 10 ms. The results will be represented in the subsection 6.2.4.
- The fifth case shows balancing in the arm voltages by changing the capacitance value in the cell of the submodule. The observations will be represented in the subsection 6.2.5.

• The sixth case introduces and investigates arm voltage balancing technique with third harmonic injection in the system. The minor system changes for this investigation will be provided to the point to point connection. All the changes and results will be represented in the subsection 6.2.6.

6.2.1 Operation points of the system and behaviour

The point to point system is simulated with $\pm 10 \text{kV}$ DC voltage and apparent power of 20 MVA. The data of the system are represented in Table 6.1. The operation points of this simulation case are illustrated in Figure 6.7. The Figure represents operations with 1 p.u. ratings of the voltage and the different active power injections or reactive power generation and absorption. The active power injection considered to be from AC grid 1 towards AC grid 2 and can be indicated with positive number. If the active power has a negative sign it means that power flow is reversed and flows from AC grid 2 towards AC grid 1. This active power flow case can not be possible if the assumption, that AC grid 1 is offshore wind farm, but is shown anyway in order to test converters T1 and T2, if the different scenario arises.

- A an only full active power is injected in the system, which results in $P=20~\mathrm{MW}$ and $Q=0~\mathrm{MVar}$.
- B an only full reactive power of the system is generated, this results in $P=0\,\mathrm{MW}$ and $Q=20\,\mathrm{MVar}$.
- C an only full reversed active power of the system is injected, this results in P=-20 MW and Q=0 MVar.
- D an only full reversed reactive power of the system is generated, in other words absorbed, this results in P=0 MW and Q=-20 MVar.
- E half of the reversed active power is injected and half of the reversed reactive power is generated in the system, this results in P=-10 MW and Q=-10 MVar with S=14,14 MVA.
- F half of the active power is injected and half of the reactive power is generated in the system, this results in P = 10 MW and Q = 10 MVar with S = 14, 14 MVA.
- G no power is injected in the system this results in P = 0 MW and Q = 0 MVar.

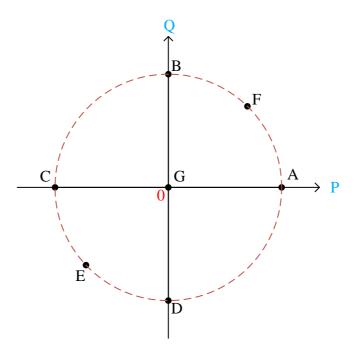


Figure 6.7: Simulated operation points

If the offshore wind park is considered as AC Grid 1 and onshore connection to the grid is considered as AC Grid 2, then the operating points C, E and G are not necessary, because of the active power flow direction. The grid codes, which should be implemented in order to provide power to the AC Grid 2. The active power flow and reactive power generation or absorption should fit in the envelope provided by transmission system operator (TSO). The boundaries vary very much depending on the country. As an example the boundaries of Tennet transmission system operator is represented in the paper [47]. The paper [48] represents wind power grid integration from the PSC conference, where the reactive power is limited and the only active power is provided from one side (from wind turbines), because the wind turbines don't need to consume active power. According to the papers and TSO TenneT [47] [48] the full active power can be provided to the grid, while the reactive power is limited. The limits of the the reactive power, in the overexcited regime is 40% of the rated active power value. In the underexcited regime the reactive power value is 30%. This means that the system can provide to the grid maximum 40% reactive power of the rated active power value and can absorb maximum 30% reactive power of the rated active power value. When the active power generation reduces and reaches 20% of the rated active power, the reactive power generation and absorption should reduce as well. If the active power reaches 0 value the system should be shut down, which means no reactive power should be provided. The active power is not reversed if the wind park considered as generation and is providing power to the onshore AC grid.

In order to test system capabilities in the extreme cases the operating points considered as mentioned above and not strictly following the grid codes. Both of the grids can inject

or absorb active power, therefore the active power reverse is also tested in C case. The full reactive power, 100% of the rated active power value, is generated and absorbed, when the active power is 0 of the system. The B and D cases illustrate this operating points. The E case represents the half of the active power of the rated active power value and the half of the reactive power of the rated active power value, providing from T2 towards T1, where the F case is from T1 to T2.

The operations are implemented in 10 s simulation, where each of the operating points are presented. Transition points of the operation are illustrated in Figure 6.8. The simulation is divided in the sections by the time. A operating point section simulation runs from 0-2 s with the unity power factor, with active power flow from T1 towards T2. The B operating point simulation section takes time from 3-3, 5 s with the power factor of 0. C operating point is simulated between 4, 5-5 s and shows reversed full active power flow with 0 reactive power. D operating point takes time in 6-6, 5 s, which represents the full reversed reactive power only. E operation is between 7-7, 5 s, with the half of the reversed active power flow and half of the reactive power 10 MW and 10 MVar respectively, total injected apparent power consists of 14, 14 MVA. F operation is between 8, 5-9 s with not reversed active power of 10 MW and not reversed 10 MVar, with the same total apparent power of 14, 14 MVA. The last operating point G takes time between 9, 5-10 s and shows operation of 0 powers injection. The behaviour of the powers, AC voltages, AC currents, DC voltages, arm voltages, arm currents, circulating currents are represented of the each operation points cases.

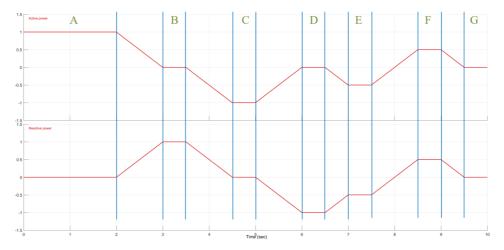


Figure 6.8: Operation points during 10 s simulation

Active power flow and reactive power generation or absorption are illustrated in Figure 6.9. The blue curves represent active and reactive powers measured at terminal 1, while the red curves represent active and reactive powers measured at terminal 2. As it can be seen the active power is a bit lower, than 20 MW due to the droop control, which regulates DC voltage. Furthermore the active power never drops to 0, because the droop control gain with 5% of ρ value will provide ± 20 kW margin of the power.

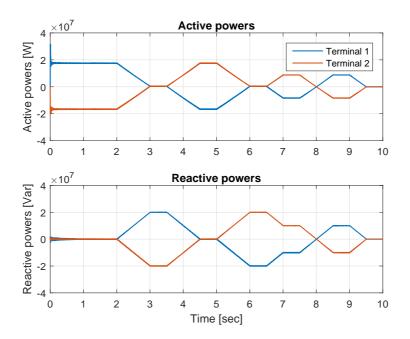


Figure 6.9: Active and reactive power injection during simulation

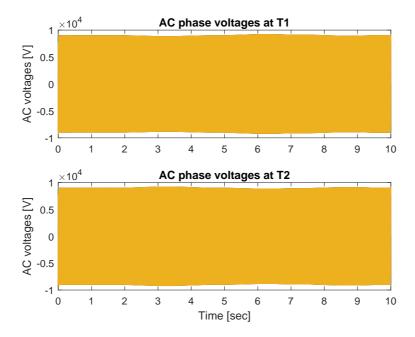


Figure 6.10: AC voltages during full simulation of 10 s in T1 and T2

The AC phase voltages in T1 and T2 are represented in Figure 6.10. As it can be seen the AC voltages increases a bit, when the full reactive power is presented. This case can be used, when the grid requires the reactive power injection or absorption. By increasing reactive power increase AC voltage in the terminals.

The AC currents in the T1 and T2 are represented in the Figure 6.11, for the full simulation time. As it can be seen the current follows the power injection in the system, when the active power flows or reactive power are generated or absorbed. The currents are slightly higher in the operating points, where is it flowing from the one terminal to the another. For example, when the active power flows from T1 to T2 during 0-2 s the current is higher in the Terminal 1, due to the resistance between the transition. The opposite will happen, when the active power is reversed and flows from T2 to T1, then the current is slightly higher in T2, for the same reason of transition resistance. During full reactive power generation or absorption, while the active power is 0, currents slightly increase to its rated values.

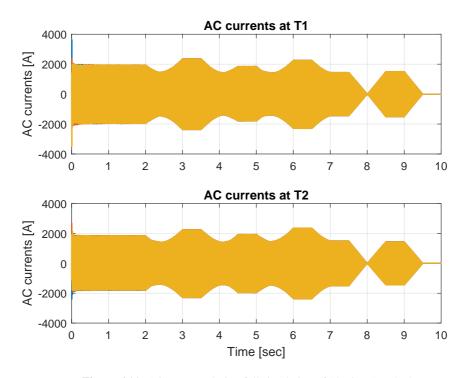


Figure 6.11: AC currents during full simulation of 10 s in T1 and T2

DC voltages in the both of the terminals are compared together in one graph and are illustrated in the Figure 6.12. The blue curve illustrates the DC voltage in T1, while red curve is terminal 2 DC voltage. Power flow direction is determined depending on, which terminals DC voltage is higher. At the beginning from 0-2 s power flows from T1 towards T2, because the T1 DC voltage is higher as it can be seen in the Figure 6.12. Since the active power has a droop control it has a margin of the power, therefore it does not drop

to zero as it can be seen during 3.5-4 s. In the simulation time section, when the active power is reversed, the direction of power flow can be seen from the Figure 6.12, there at 4,5-5 s the DC voltage is higher in T2, therefore the direction of the power flow is from T2 towards T1. Similar goes for the reactive power, it is injected towards T2 from T1, when the DC voltage is higher in T1 and absorbed by T1 when the DC voltage is higher in T2. DC voltage ripples are higher during the active power flow, than during only reactive power or active power flow and reactive power.

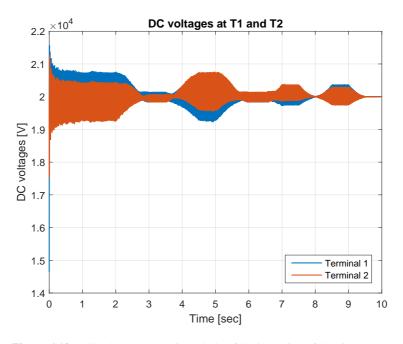


Figure 6.12: DC voltages comparison during full simulation of 10 s in T1 and T2

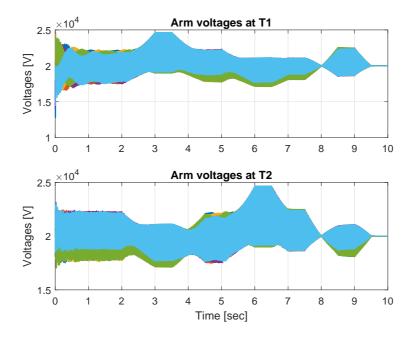


Figure 6.13: Arm voltages in T1 and T2

Voltages in the arms at T1 and T2 are represented in the Figure 6.13. The arm voltages are slightly unbalanced. The small deviations in different colors can be seen in the Figure 6.13. The closer look of the arm voltages in each operation points are introduced further in this subsection. The highest peaks of the arm voltages are observed when the full reactive power is appeared from one terminal to another. In the beginning of the simulation the arm voltages fluctuates, due to initial conditions. The small unbalance also can be seen when the arm voltages are going from one transition point to another, while in the steady state can be seen small arm voltages deviations.

The arm currents are represented in the Figure 6.14 during the full simulation 10 s time. The upper part, above 0 of the first plot represents the circulating current, created during the overlap period, while the both arms, lower and upper are in conduction. The same representation of the circulating currents are illustrated in second plot, but now it is bellow 0 value. In some operation points the circulating currents are higher than the arm current, therefore the switches capability of conduct the current should be determined by the circulating currents magnitude.

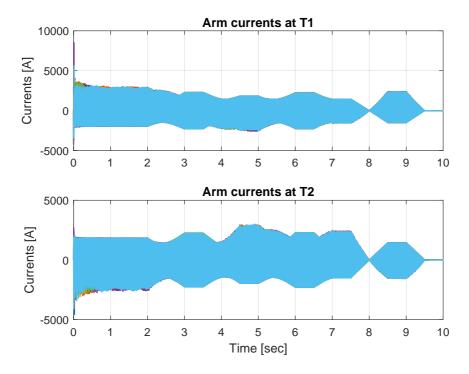


Figure 6.14: Arm currents in T1 and T2

Circulating currents for the whole simulation time are illustrated in the Figure 6.15. By following current direction assumption for the grid connected converter represented in Figure 6.2, it can be seen that the positive circulating currents presents in T1 and negative in T2. Circulating currents help to charge or discharge the stack capacitors, therefore balancing voltages in the arms. During the active power injection the circulating current magnitudes are the highest, therefore the capability of the conduction of the elements should be taken into account by following the highest current peak, even if it small duration of time. During only reactive power flow the circulating currents are in balance for the positive and negative areas, where the areas of circulating currents positive and negative sides matches. During no power transfer the circulating current is zero.

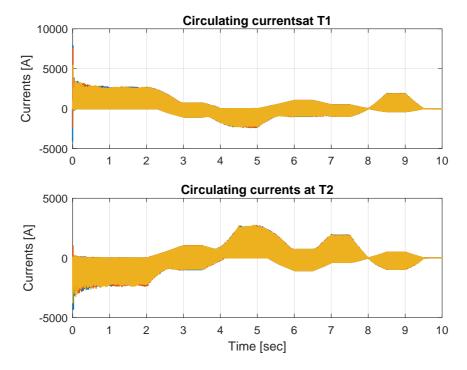


Figure 6.15: Circulating currents in T1 and T2

The closer look of the operation points will be discussed below, where the simulation for different operating points is presented for a small time duration, which is $0,04\,\mathrm{s}$ for each case. The simulation results are presented for the T1 and T2 separately. The results ate the same when the active or reactive power is reversed from T2 to T1, comparing with the results, when the power flow from T1 to T2. The AC currents, AC voltages and DC voltages are represented in the time snap of $0.1\,\mathrm{s}$, because it is better to analyze. These results are illustrated for the each operating point separately. The results of AC currents, arm voltages, arm currents, circulating currents are zero or the value near zero, so that the last operation point G are not presented in the comparisons.

The Figure 6.16 illustrates the AC voltages, AC currents and DC voltages at A operating point and takes time between 1,7-1,8 s at T1 and T2. The blue curve represents phase A, red - phase B and yellow is phase C for the AC values. In the terminal 1 the AC voltages are sinusoidal as in the terminal 2. The T1 AC currents contains some harmonics as the T2, but the magnitude of the T2 currents are lower than T1, because of the active power transfer from T1 to T2 and the resistance between transition. The only active power is transferred from T1, therefore the AC voltages and AC currents in the T1 are in phase of each other and with the same sign. The AC voltages and currents are in phase in T2 also, but with the opposite signs, when the voltages are positive the currents are negative and, when the voltages are negative the currents are positive. This indicates that the active power is injected in this terminal. The active power transfer at operation point A is indi-

cated in the last graph, where the DC voltages are illustrated. T1 DC voltage is higher, than T2, so that the active power flows from T1 to T2.

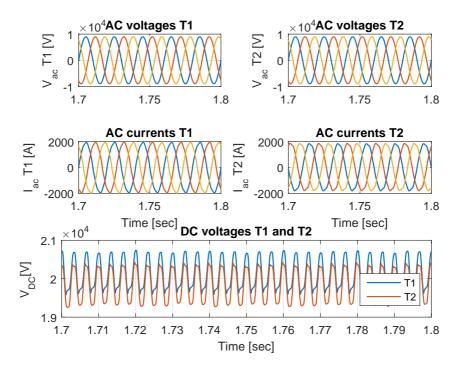


Figure 6.16: AC voltages, AC currents and DC voltages at operating point A

The Figure 6.17 represents the operation at point B, where the full reactive power is generated in T1 and T2. The time snap of the simulation is 3,2-3,3 s. The case can be used for the ancillary services if the grid need support of the reactive power in order to increase the voltage. The AC voltages and AC currents are not sinusoidal in the both terminals. At the T1 the voltages are lagging the currents by the 90° , since the only reactive power is generated, this means the T1 produces reactive power. At the T2 the reactive power is absorbed by the T2, therefore the voltages are leading the current by the 90° . The AC voltages are absorbed by the T2, therefore the voltages in T2 are slightly higher and exceeds $V_{ac} = 11000\sqrt{2/3}$ per phase, at the same time the phase currents are slightly smaller at T2 than T1. The DC voltages indicates that the reactive power is generated in T1 and absorbed in T2, because the DC voltage is higher at T1. The ripple of DC voltage comparing with the Figure 6.16 is lower in B operating point.

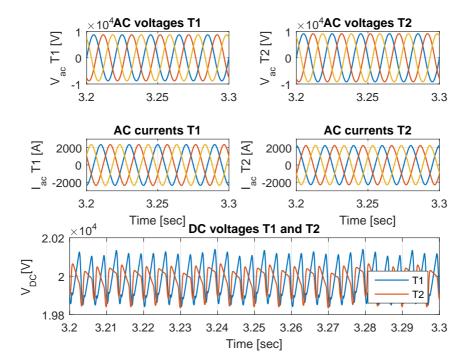


Figure 6.17: AC voltages, AC currents and DC voltages at operating point B

The C operating point is represented in Figure 6.18, where the time snap is 4,7-4,8 s. This operation point represents the reversed active power flow, when it flows from T2 towards T1. The AC voltages, AC currents and DC voltages just exchange places between terminals comparing with the Figure 6.16, where T1 had the same graphs as now T2 have and T2 had similar graphs as T1 have now. The DC voltage is higher at T2 than T1 this indicates that active power flows from T2 towards T1. At operating point C the voltages are in phase with the currents in the both terminals, when the T1 AC voltages are positive, then the AC currents are negative, for the T2, while AC voltages are positive the currents also are positive.

The Figure 6.19 illustrates the reversed reactive power appearance, when it is generated in T2 and is absorbed in T1. The simulation time snap is 6, 2-6, 3 s. The reactive power is absorbed at T1, because the AC voltages are leading the AC currents. Only reactive power is transferred, so the angle between the voltages and currents are 90° . Since the T2 is injecting reactive power at this operating point the AC currents are leading AC voltages. By absorbing the reactive power the AC voltages at T1 slightly increase, while in the T2 decrease. The AC currents in T2 are slightly higher than in the T1. The DC voltage indicates the reactive power generation in the T2 and absorption in T1, because the T2 DC voltage is higher than T1.

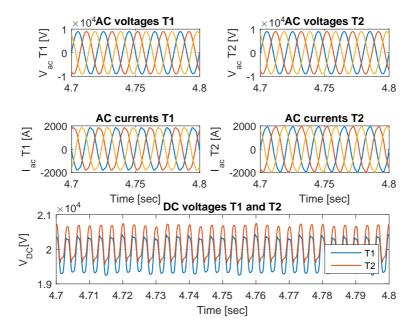


Figure 6.18: AC voltages, AC currents and DC voltages at operating point C

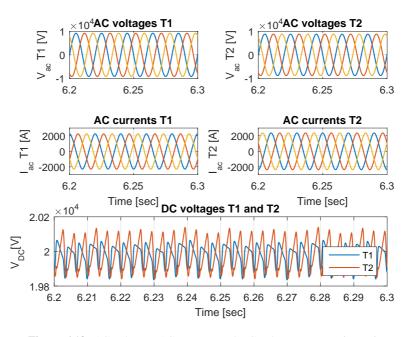


Figure 6.19: AC voltages, AC currents and DC voltages at operating point D

The Figure 6.20 shows the 10 MW active power being transferred from T2 towards T1 and 10 MVar generated reactive power in T2 and absorbed in T1. The total apparent power consists of 14, 14 MVA. This results in lower currents magnitude, then it was for the full 20 MW or 20 MVar cases. The active power transfer from T2 towards T1 is indicated by the DC voltage, where it is higher at T2 than T1. The AC currents are leading the AC voltages, because the power is injected towards T1. The angle between AC currents and AC voltages is lower than the 90°, because both, the active power is transferred and reactive power is generated at the same time.

The Figure 6.21 represents the operating point F, where the 10 MW active power is transferred from T1 towards T2 and 10 MVar is generated in T1 and absorbed in T2. The power flow direction indicates DC voltage, which in this operating point is higher at T1 than at T2. In this case the AC currents are leading the AC voltages by lower than 90° angle between them at T1. At T2 the voltages are leading current by the same lower than 90° angle between them, because the active power is received and reactive power is absorbed in T2 at the same time. F operating point is similar to the E operating point, only the direction of the active power transfer is different. The currents are smaller in magnitude at F operating point, because for the same reason as E, where not full apparent power is transferred from T1 towards T2.

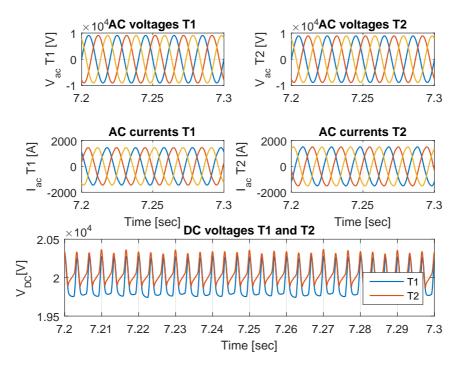


Figure 6.20: AC voltages, AC currents and DC voltages at operating point E

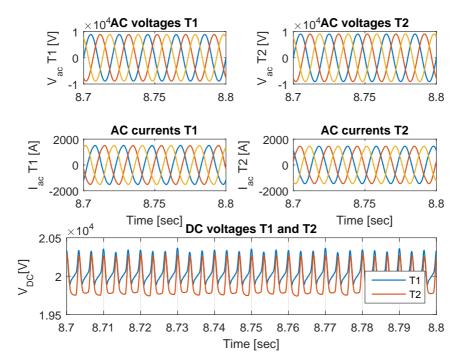


Figure 6.21: AC voltages, AC currents and DC voltages at operating point F

For the better comparison and visibility the arm voltages, arm currents and circulating currents are represented in smaller time domain for 0,04 s. The terminal 1 and terminal 2 data are illustrated in the different Figures. All the operating points are represented in one Figure. The operating point G is not presented since it is zero.

Arm voltages measured in T1 in all operating points are illustrated in Figure 6.22 and arm voltages measured in T2 are represented in Figure 6.23. The curves in the graphs are representing each phase upper and lower arm voltages, the colours are stated below.

- A phase: Blue curve represents upper arm. Red curve is lower arm.
- B phase: Green curve represents upper arm. Light blue curve is lower arm.
- C phase: Yellow curve represents upper arm. Purple curve is lower arm.

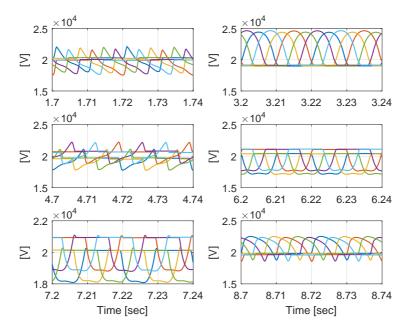


Figure 6.22: Arm voltages in all operation points at T1

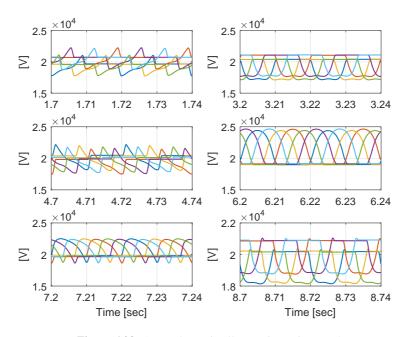


Figure 6.23: Arm voltages in all operation points at T2

Starting from the top left side and going to the right and down, like reading, the operating points can be indicated as A, B, C, D, E and F, another indication is a time snaps. The one on the top left shows the arm voltages with active power injection from T1 towards T2. By taking reference the blue curve at 1,72 s it can be seen that it charges for the short amount of time, because the voltage is going up above 2×10^4 . It reaches peak, which indicates that it is charged and slowly starts to discharge and after while the circulating current charges it again till the capacitor remains charged at 2×10^4 and stays till the next circulating current appearance for this arm. It can be seen that charging area is smaller, than the discharging in this case.

The second graph in the top right indicates arm voltages during reactive power generation in T1. The capacitor in the stacks charges to the higher magnitude, than in the first graph. By taking reference the same blue curve it can be seen that its been charged till the peak value and then it is discharged at the same speed, which gives the same areas of charging and discharging.

The graph represented in the middle left, shows the arm voltages, when the reversed active power flows from T2 towards T1. In this graph the charging area is bigger by taking blue curve as the reference, tan the discharge area. After the charging and discharging the lower arm voltages finds new balance point this results in a small deviation of voltage balance for the upper and lower arms. The small imbalance is observed in the T1, when the active power flow is reversed.

The middle right graph indicates arm voltages during the reversed reactive power generation, it can be seen that the discharging and charging areas are the same in this case. The deviation in the upper and lower arms are observed since they are not in the same line and again lower arm voltages settles in the different point than upper arm voltages.

The bottom left graph in Figure 6.22 represents arm voltages during active power flow from T2 towards T1 and reactive power generation in T2 and absorption in T1. The charging area is slightly bigger than discharging area. The imbalance between upper and lower arms are observed, because the voltages are not staying in one line. Furthermore it can be said, whenever the active power flow is from T2 towards T1 and reactive power generation is in T2 and absorption in T1, the lower and upper arms voltage are not in the same line they have a difference between the voltages.

The last graph in the bottom right of the Figure 6.22 shows the arm voltages during active power flow from T1 to T2 and reactive power generation in T1 and absorption in T2. It can be indicated that discharge area is bigger than the charging area. The arm voltages have very small imbalance, because the small deviation can be observed, but it is not that big like in operating points C, D and E. By taking blue curve as a reference, when the curve goes up the capacitors in stacks are charging, when the curve goes down the capacitors are discharging. The similar arm voltages also are represented in Figure 6.23, but measured in T2. This will result in the mirror image of the operating points.

Arm currents are represented in the Figure 6.24 measured at T1 and in the Figure 6.25 measured at T2. The arm currents together with the circulating currents charges and discharges capacitances in the stack of the cells, therefore the arm voltages balance can be achieved. Depending on the operation points the different shapes of the arm current forms are indicated in the Figures 6.24 and 6.25. The arm currents illustrated in the Figure 6.24 top 2 graphs are the same as represented in the Figure 6.25 middle graphs, because the

power injection direction is the same, only measured in different terminals.

The circulating currents are illustrated in the Figures 6.26 and 6.27 at T1 and T2, respectively. The circulating currents are formed, due to the overlap time. The highest circulating currents are in the active power flow cases, than in the other cases. The circulating currents and the arm voltages balance are depending on the overlap time in the Figure 6.22. The arm voltages in the middle graphs and bottom left graph are with the highest imbalanced. The lower and upper arms are not in the same line, which result the lower arm voltages of being higher than upper arms voltages. The reason can be that the overlap time is not enough to balance the voltages in the arms, which gives this deviations between the upper and lower arms. Therefore the effect of the increased overlap time is interesting to investigate and subsection 6.2.4 represents this investigation.

Another case to balance the arm voltages can be if the arm cell capacitance is increased or reduced. By following this hypothesis the increased arm cell capacitance can affect the arm voltage deviations and reduce it or make it worse. The case will be investigated in the following subsection 6.2.5.

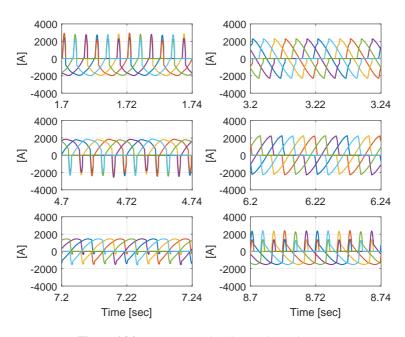


Figure 6.24: Arm currents in all operation points at T1

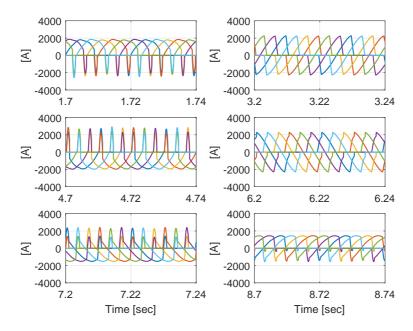


Figure 6.25: Arm currents in all operation points at T2

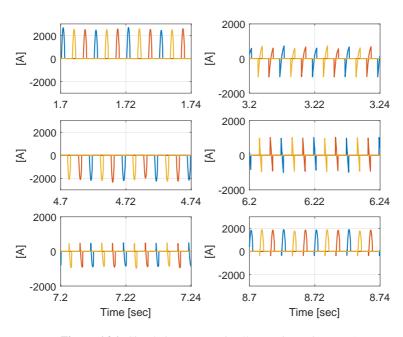


Figure 6.26: Circulating currents in all operation points at T1

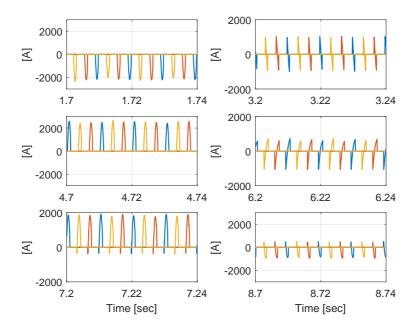


Figure 6.27: Circulating currents in all operation points at T2

6.2.2 Effect of the DC side capacitance

The study case aims to investigate the effect and behaviour of DC link voltage with alternate arm converter by changing capacitance values in DC side. The power with unity power factor is injected from the AC Grid 1, towards AC Grid 2. The active power injection starts from 0 and will be ramped to the full active power in 2 seconds interval. The full simulation time takes 10 seconds, with $\pm 10kV$ and 20MW. The capacitance is calculated for the each side of the cable, therefore creating the pi equivalent model for the cable. The overall capacitance value is 20ms or 2mF. By introducing lumped elements in the DC side system, the capacitance value in each side of the cable becomes 1mF. In order to investigate the DC side capacitance effect the first case will be with doubled overall capacitance and in another case it is reduced by half of the reference 2mF value. Overall capacitance are doubled for the first case, therefore reference value becomes 4mF in DC side and in the second case overall reference value becomes 1mF. The simulation runs 3 times, with different capacitance values, while AC voltage, AC current, DC voltage, arm voltages, arm currents and circulating current information will be recorded and introduced bellow for comparison in this section. The graphs show data of the whole simulation time and the small segment of time, because of the better behaviour visibility.

Rated capacitance value 2mF

The first case is simulated with rated 2mF capacitance value. The active powers represented in Figure 6.28 in d-q0 reference frame. The AC phase voltages, ac currents and

DC voltage at terminal 1 and terminal 2 are represented in Figure 6.29, where 6.29a is Terminal 1 measurements and 6.29b is Terminal 2 measurements.

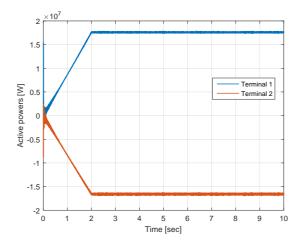


Figure 6.28: T1 and T2 active powers

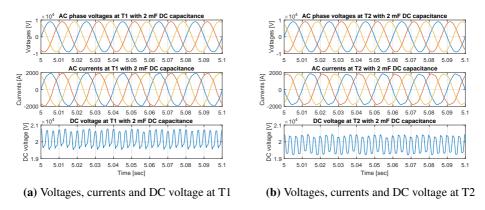


Figure 6.29: AC phase voltages, ac currents and DC voltage at T1 and T2

As it can be seen the oscillations in active power d-q0 reference frame are noticed. The voltages are sinusoidal in both terminals. The currents in T1 and T2 are close to sinusoidal, but it can be seen that current measured at T2 is a bit more distorted. In T1, when the voltage is positive the currents is positive too, while in T2 when the voltage is positive current is negative and the way around. The DC voltage in T1 is higher than in T2, this will indicate that the power flow is from T1 towards T2. The DC voltage is observed with some ripple. The comparison of the DC voltages is illustrated in Figure 6.30, where it can be seen proper DC voltage comparison between two terminals. The power oscillations can be caused by droop control and DC voltage fluctuations, since the droop 5% gain is quite

large and DC voltage oscillations are caused by charging and discharging DC capacitance and circulating current.

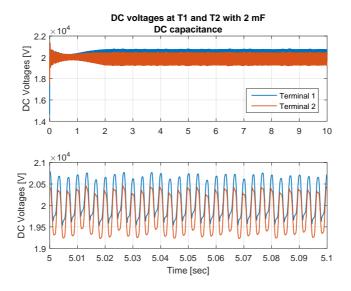
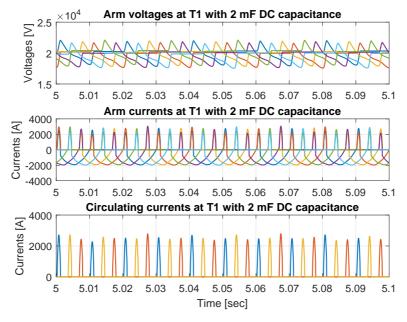
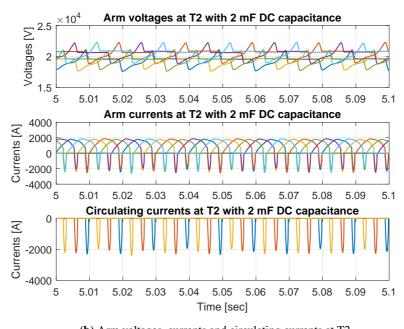


Figure 6.30: DC voltages at T1 and T2 with 2mF capacitance value

The arm voltages, currents and circulating currents are illustrated in this case with 2mF, and measurements at T1 and T2 shown in Figure 6.31, where 6.31a is T1 and 6.31b T2 measurements. Blue, green and yellow curves represent upper arm for A, B, C phases respectively. Red, light blue and purple curves represent lower arm for A, B, C phases respectively. The arm voltages look balanced and not differs in magnitude or oscillation at T1. While at T2 the difference of upper and lower arm voltages can be observed. Therefore a small unbalance in T2 can be observed. The arm currents are represented together with the circulating current, which illustrated as a spikes. In the bottom plot of the Figure 6.31 the circulating currents are represented. It can be observed that the peak magnitude of the circulating currents are even higher than the arm currents. The control of the circulating current is not implemented in this master thesis. Therefore a careful attention should be paid, when designing the director switches. The director switches should be design in order to conduct the maximum peak current, where in this case it is circulating current, but not a arm current. In this master thesis is assumed that director switches are designed to withstand these circulating currents, otherwise the control is recommended.



(a) Arm voltages, currents and circulating currents at T1



(b) Arm voltages, currents and circulating currents at T2

Figure 6.31: Arm voltages, currents and circulating currents at T1 and T2

Doubled capacitance value 4mF

The second case is simulated with doubled 4mF capacitance value. The active powers are illustrated in Figure 6.32 in d-q0 reference frame. The AC phase voltages, ac currents and DC voltage at terminal 1 and terminal 2 are represented in Figure 6.33, where 6.33a is Terminal 1 measurements and 6.33b is Terminal 2 measurements.

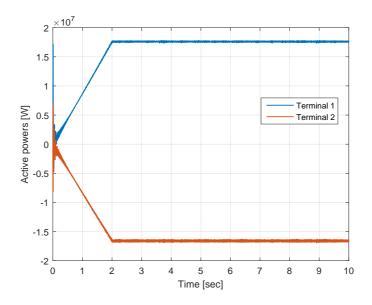


Figure 6.32: T1 and T2 active powers

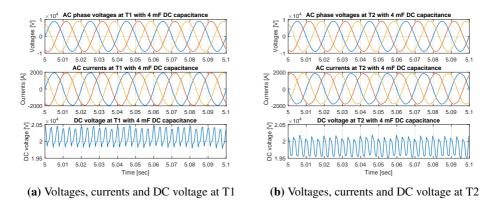


Figure 6.33: AC phase voltages, ac currents and DC voltage at T1 and T2

As it can be seen the smaller oscillations are noticed in active power d-q0 reference frame. This reduction comes due to the reduced DC voltage fluctuations. The voltages are

sinusoidal in both terminals as it is in previous case. The currents look more sinusoidal than in the previous case. The DC voltage in T1 is higher than in T2, this will indicate that the power flow is from T1 towards T2. The DC voltage is observed with smaller ripple, than in the case before with 2mF capacitance value. The comparison of the DC voltages of two terminals is illustrated in Figure 6.34, where it can be seen proper DC voltage comparison between two terminals.

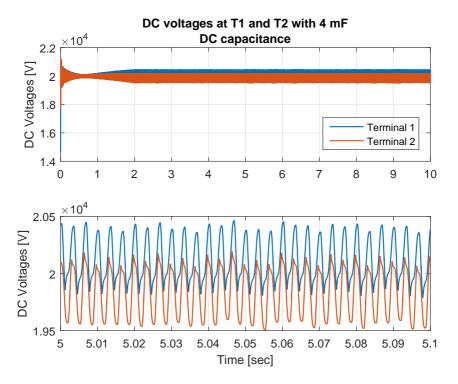
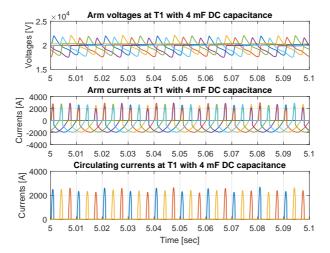
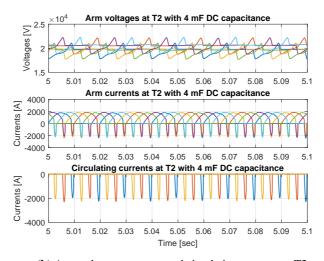


Figure 6.34: DC voltages at T1 and T2 with 4mF capacitance value

The arm voltages, currents and circulating currents are illustrated in this case with 4mF, and measurements at T1 and T2 shown in Figure 6.35, where 6.35a is T1 and 6.35b T2 measurements. As in the previous case the arm voltages are balanced at T1, while the difference in the balance between upper and lower arms are still noticed at T2. The circulating current looks slightly smaller comparing with 2mF case. The more detailed comparison will be introduced in the subsection 6.2.2.



(a) Arm voltages, currents and circulating currents at T1



(b) Arm voltages, currents and circulating currents at T2

Figure 6.35: Arm voltages, currents and circulating currents at T1 and T2

Reduced by half capacitance value 1mF

The second case is simulated with doubled 1mF capacitance value. The active powers represented in Figure 6.36 in d-q0 reference frame. The AC phase voltages, ac currents and DC voltage at terminal 1 and terminal 2 are represented in Figure 6.37, where 6.37a is Terminal 1 measurements and 6.37b is Terminal 2 measurements.

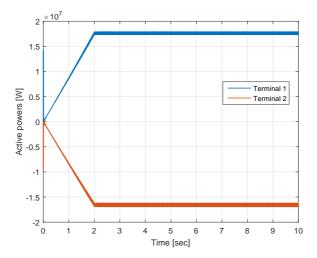


Figure 6.36: T1 and T2 active powers

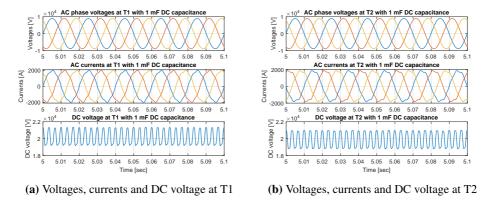


Figure 6.37: AC phase voltages, ac currents and DC voltage at T1 and T2

As it can be seen the oscillations in active power d-q0 reference frame are highest comparing to all of these cases. The voltages are sinusoidal in both terminals. The currents starts to contain more harmonics, therefore the non sinusoidal curves are appearing. In T1, when the voltage is positive the currents is positive too, while in T2 when the voltage is positive current is negative and the way around. The DC voltage in T1 is higher than in T2, this indicates that the power flow is from T1 towards T2. The DC voltage is observed with ripple. The comparison of the DC voltages is illustrated in Figure 6.38, where it can be seen proper DC voltage comparison between two terminals.

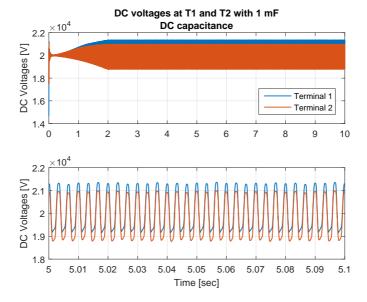
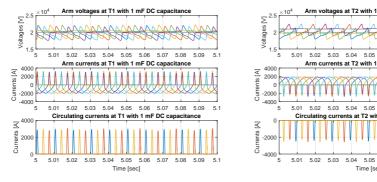


Figure 6.38: DC voltages at T1 and T2 with 1mF capacitance value

The arm voltages, currents and circulating currents are illustrated in this case with 1mF, measurements at T1 and T2 shown in Figure 6.39, where 6.39a is T1 and 6.39b T2 measurements. The arm voltages are the same as in previous cases, but the arm currents are distorted, due to additional harmonics. The 3 cases are compared in the following subsection 6.2.2.



(a) Arm voltages, currents and circulating currents at T1

(b) Arm voltages, currents and circulating currents at T2

5.06 5.07 5.08

5.06 5.07 5.08

Figure 6.39: Arm voltages, currents and circulating currents at T1 and T2

Comparison of all 3 cases

The most important comparisons of the data with different values of capacitance are presented in this subsection. First of all the arm voltages especially in T2 are not very well balanced between the upper and lower arm. The unbalance remains during the changes of capacitance values, therefore it indicates that the DC capacitance value does not play a role in arm voltage balance. The circulating currents in T1 and T2 are represented in Figure 6.40, where 6.40a is T1 circulating currents for the different capacitance values and 6.40b T2 circulating currents. The circulating current values is a bit higher in the case with 1mF capacitance. The cause of the circulating current is due to the overlap period in order to balance the voltages in arms. This is one of the arm voltage balancing techniques. The circulating currents have a high spikes in all 3 cases, this is caused, because of the interruption of the current, when the director switches is opening. The circulating current slightly distorts DC voltage.

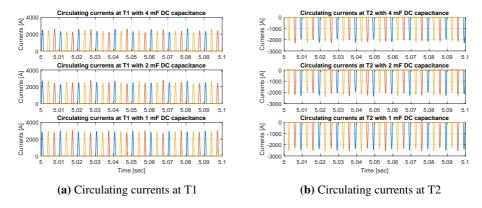


Figure 6.40: Circulating currents at T1 and T2 with different DC side capacitance values

The wave forms of DC voltages for all 3 cases and its ripples are represented in Figure 6.41, where 6.41a is DC voltages in T1 and 6.41b is DC voltages in T2. As it can be seen the DC voltage in T1 is higher, than in T2, this will directs the power flow, which is in these cases from T1 towards T2. All 3 cases with different capacitance value and DC voltage behaviour are illustrated and compared between each other. The ripples in DC voltage in the worst case with overall capacitance value of 1mF are around 10%, but the higher the capacitance value the less ripples are observed in DC voltage. The DC side capacitance is acting like a filter, which filters the DC voltage ripples. In order to reduce the ripples in DC voltage, higher capacitance value should be chosen. The reduced ripples in DC voltage and better performance is a trade of the size of the capacitor and the increased costs of the system. The higher capacitance value leads to the higher costs.

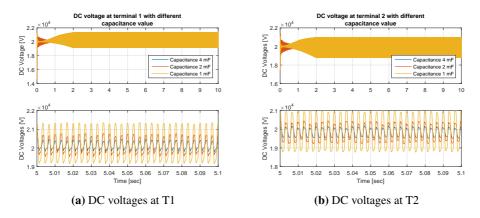


Figure 6.41: DC voltages at T1 and T2 with different DC side capacitance values

Furthermore the AC currents are compared in the Figure 6.42, where 6.42a is currents in T1 and 6.42b currents in T2. As it can be seen the currents with a case of 1mF are distorted the most, because the highest DC voltage ripple is observed in this case. The DC voltage is in the loop of this system, therefore distortions in DC voltage causes the distortions in AC currents. At the beginning of the modeling it was assumed, that DC voltage is a constant value, but with the system changes and implementation of the capacitors instead of constant DC voltage source, the DC voltage becomes not constant anymore, because the capacitors are charged and discharged. The more constant value of DC voltage can be achieved by implementing circulating current control or reducing the ripples in DC voltage. The Figures show the larger the capacitance the more sinusoidal AC currents will flow. Despite that the capacitance value and accepted distortions should be in balance, because the larger the capacitance value, the higher is the systems costs and size. The balance in this should be maintained.

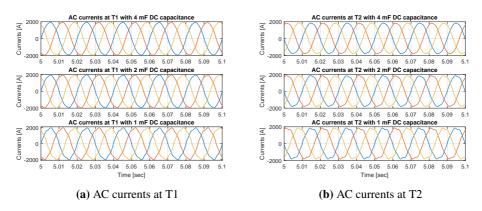


Figure 6.42: AC currents at T1 and T2 with different DC side capacitance values

The THD of the measured A phase AC currents for the different overall capacitance

values are represented in the Figures 6.43, 6.44, 6.45, 6.46, 6.47 and 6.48, with 4mF, 2mF, 1mF overall DC capacitance value respectively in both T1 and T2 . THD of the A phase AC current with overall capacitance value of 4mF at T1 in Figure 6.43 is 2.69% and at T2 in Figure 6.44 is 3.23%. THD in the same current, but with overall capacitance value of 2mF at T1 is 3.26% and at T2 is 3.89%. THD with overall capacitance value of 1mF at T1 is 1.9% and at T2 is 1.9% at T1 is 1.9% and at T2 is 1.9% and at T2 is 1.9% and at T2 is 1.9% are Eq. (1.9\%).

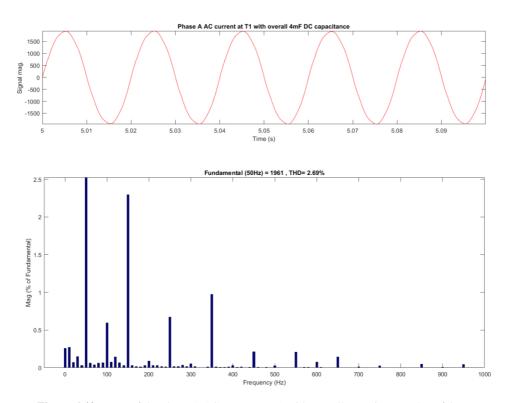


Figure 6.43: THD of the phase A AC current at T1 with overall capacitance value of 4 ms

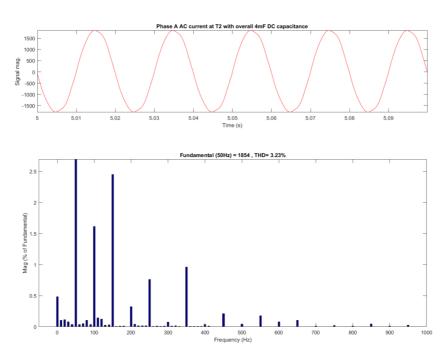


Figure 6.44: THD of the phase A AC current at T2 with overall capacitance value of 4 ms

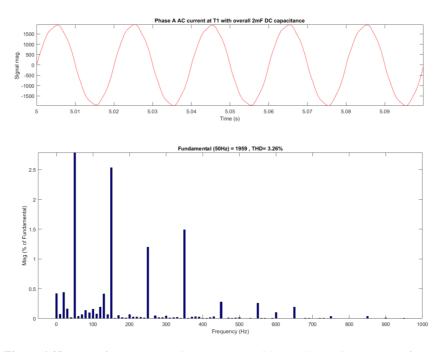


Figure 6.45: THD of the phase A AC current at T1 with overall capacitance value of 2 ms

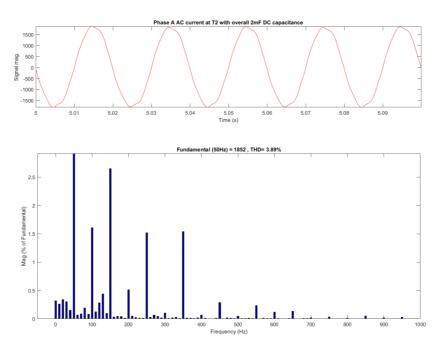


Figure 6.46: THD of the phase A AC current at T2 with overall capacitance value of 2 ms

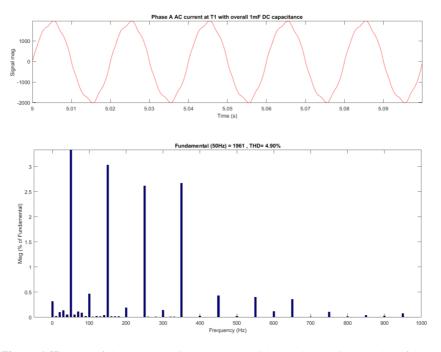


Figure 6.47: THD of the phase A AC current at T1 with overall capacitance value of 1 ms

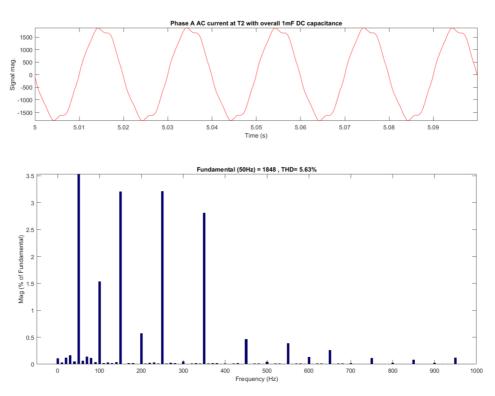


Figure 6.48: THD of the phase A AC current at T2 with overall capacitance value of 1 ms

6.2.3 Effect of the different droop control drop values

The droop control was introduced in subsection 6.1.2. The simulation performs different drop (ρ) values: 5%, 10% and 20%. The higher the drop value the smaller is the gain, by which DC voltage is regulated. The simulations are performed with unity power factor injection from the AC Grid 1, towards AC Grid 2, which means that only active power flows. The active power injection starts from 0 and will be ramped to the full active power in 2 seconds interval. The full simulation time takes 10 seconds, with $\pm 10kV$ and 20MW. The overall capacitance values of DC side is 2mF. The simulation runs 3 times, with different drop gain (ρ) values, but the values will be the same in T1 and T2. The 2 more simulations runs with different drop (ρ) values for droop control in T1 and T2. The forth one will be with 10% of drop in T1 and 5% of drop in T2. The fifth simulation runs with 5% in T1 and 10% in T2. In total this study case results 5 simulations.

The droop controls DC voltage, by following outer loop active power control, in a away when the DC voltage drops to certain limitations in these cases it will be 5%, 10% and 20%, then the active power increases. The active powers and the DC voltages are represented for these cases, since they are focus for this study case. First of all the simulation with 5%, 10% and 20% drop in both T1 and T2 droop controllers are entered, which result in droop control gains $20000\ 10000$ and 5000 respectively. In the next 2 simulations the 20% of DC voltage drop is not considered, since the voltage should not differ by more

than $\pm 10\%$ of its rated value [50]. So that the next two simulation performed with 10% of drop in T1 and 5% in T2. The last simulation will be 5% in T1 and 10% in T2.

The active powers and DC voltages at T1 with different ρ are represented in Figure 6.49. In this Figure it can be seen the active power with a different ρ values. As the percentage drop ρ values increase, the smaller the droop control gains are result. The smaller control gains results in smaller active power decrease. The smaller controller gain allows to regulate the active power with the smaller difference, but in order to increase the controller gain the higher ρ value should be implemented. This is not the case because the ρ value is typically 5% - 10%. In the Figure 6.49 it can be observed, that when the ρ value is the highest 20%, the active power yellow curve are the highest, but the DC voltage curve is the lowest. The closer look of the simulation measured in T1 of the active powers and DC voltages with different ρ values is illustrated in the Figure 6.50. In this Figure it can be seen that the active powers fluctuate, it is a cause of the DC voltage ripples investigated in subsection 6.2.2. The active power as expected is the highest with the highest ρ value and are the lowest with the smallest ρ value. The ρ value creates a difference between the powers. The highest is ρ value the smaller should be the DC voltage in the steady state. From investigation the observations can be seen, the purple and green curves. The green curve is above the purple. The green curve represents the ρ values, when in the T1 it is 5% and in the T2 it is 10%. The purple curve represents the ρ values, when in the T1 it is 10% and in the T2 it is 5%. When the ρ is smaller in the T1 than in T2, then the active power is higher comparing with, when the ρ is higher in T1 than T2. The purple and the green curves are in between the 10% and 5%, ρ value curves.

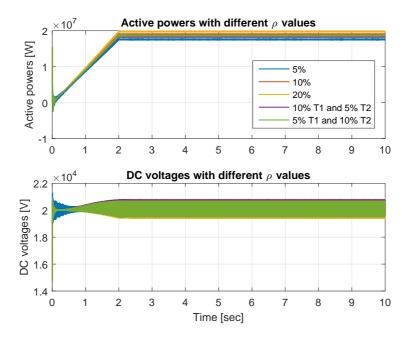


Figure 6.49: Active powers and DC voltages with different ρ values measured at T1

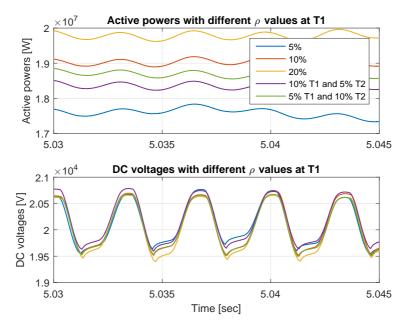


Figure 6.50: Closer look of the active powers and DC voltages with different ρ values measured in T1

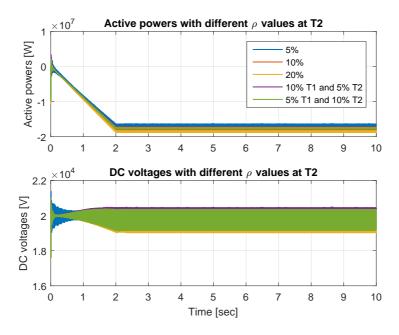


Figure 6.51: Active powers and DC voltages with different ρ values measured at T2

The active powers and DC voltages measured at T2 with different ρ are represented in the Figure 6.51. The active power flow is from T1 towards T2, therefore the reversed active power flow can be seen in the Figure 6.51, which has a negative sign. The droop control working principle is the same as before, as it can be seen by taking example the yellow curve when the ρ value is the highest, the gain is smallest, therefore the smaller difference of the rated active power value is created, while the DC voltage is the lowest.

The closer look of the data measured at T2 are illustrated in the Figure 6.52. The DC voltage fluctuates differently, when it is measured in the T2, therefore active power fluctuates also differently.

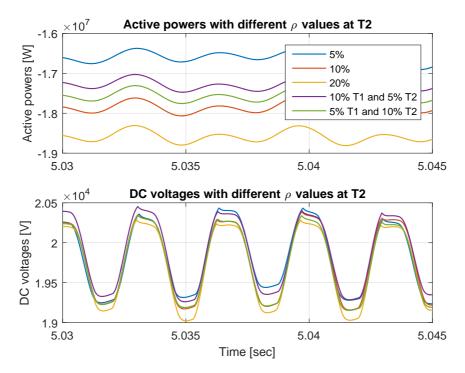


Figure 6.52: Closer look of the active powers and DC voltages with different ρ values measured in T2

6.2.4 Different overlap times

As it was stated in subsection 6.2.1 the arm voltage imbalance are observed in the some of the operating point cases. The imbalance in the upper and lower arms can appear, because of the short time of the overlap. The lower arm voltages can not drop and be in the same line as upper arm voltages, because the 1 ms overlap time are not discharge stack of the cells capacitance fully, therefore the lower arms find new balancing point for itself. In this subsection the 4 different overlap times are investigated. The values are 3 ms, 5 ms, 7 ms and 10 ms. The overlap time of 10 ms creates 1 cycle of the circulating current. This

makes the AAC act like the MMC, where the circulating current is always present. With this simple increase of the overlap time the converter from the alternate arm can simple be transformed into modular multilevel converter. The overlap time is increased because of extension of circulating current time, which balance the arm voltages between upper and lower arms in some cases. The different time values give different constant values, it can be calculated according to the equation 6.6. The case is focusing only on the arm voltages, arm currents and circulating currents, which are illustrated in the Figures.

The main features of the overlap time increase will be balance of the arm voltages in some of the operating point cases and the $10~\rm ms$ overlap time will represent the converter transition from AAC to MMC, therefore the same simulation model can work as AAC and as MMC.

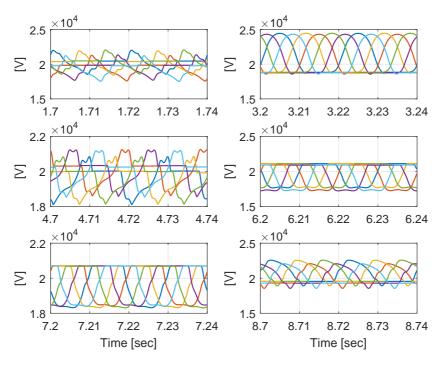


Figure 6.53: Arm voltages for the different operation points with 3 ms overlap time

The arm voltages with extended 3 ms overlap time are represented in the Figure 6.53. It can be seen that in some operation cases the arm voltages balance becomes better. As for comparison with 1 ms overlap time, which is represented in the Figure 6.22, the arm voltage balance for the D and E operating points becomes better. The count down of the graphs in the Figure start similar as in the subsection 6.2.1 from left to the right and goes down. For 3 ms overlap time the E case, which is the bottom left graph, becomes completely balance, while the D operating point case, which is in the middle right side, has a very small deviation between upper and lower arms. However the 3 ms overlap time still can not balance the arm voltages in the A, top left graph, and C, middle left graph,

operating point cases. Therefore the overlap time is increased further to 5 ms.

With the increased overlap time to $5~\rm ms$, the arm voltages in the operating point cases become more balanced as it can be seen in the Figure 6.54. The above mentioned cases with fair balance A, top left side graph, and C, middle left side graph, becomes better, the other cases remain in balance of the arm voltages, with very slight deviation between upper and lower arms. As it can be seen the case D, middle right side, still has very small difference in arm voltages as the cases A and C. But comparing with $1~\rm ms$ and $3~\rm ms$ overlap the balance becomes better. Further the overlap time is increased to the $7~\rm ms$.

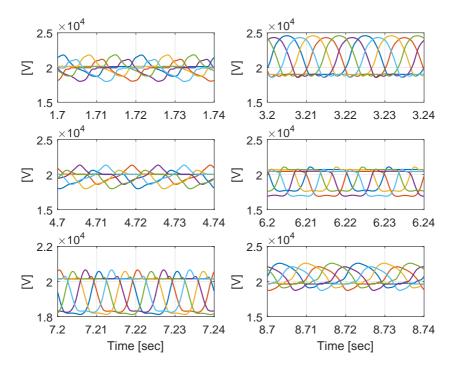


Figure 6.54: Arm voltages for the different operation points with 5 ms overlap time

The Figure 6.55 shows the 7 ms overlap time implemented in the system. As it can be seen the balance becomes way better comparing with the other overlap time values represented before. The balance is maintained in the arm voltages for all cases. The main point is that, when the overlap time is increased the converter starts to act more and more as modular multilevel converter, where the circulating current flows all the time.

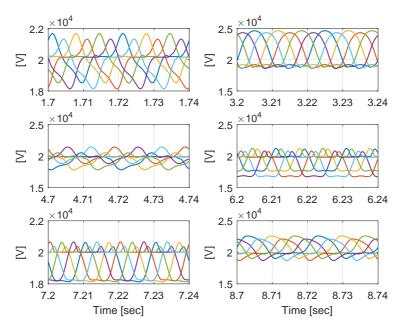


Figure 6.55: Arm voltages for the different operation points with 7 ms overlap time

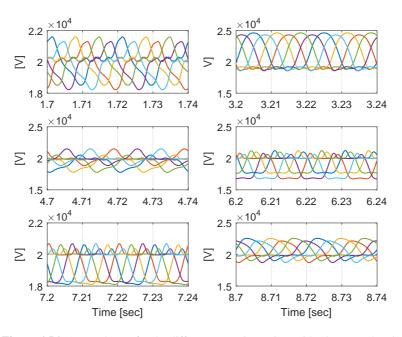


Figure 6.56: Arm voltages for the different operation points with 10 ms overlap time

The Figure 6.56 illustrates the overlap time of 10 ms, which is basically the 1 cycle of the circulating current. The arm voltages are balanced in this case since the circulating current is present for the long time. The overlap control allows to step from AAC mode to the MMC. When the circulating current is flowing all the time the converter is considered to work as MMC. In order to operate converter as alternate arm the overlap time should not reach 10 ms, if the overlap time reaches the 10 ms the converter starts act as modular multilevel. Therefore at this point there is a trade of between good balance of the arm voltages with the increased overlap time and the operation in MMC mode. This choice forces to look for the better arm voltage balancing techniques, where the advantages of the AAC can be kept, where advantages are mentioned in chapter 4.

The arm currents for the different overlap times are represented in the Figures 6.57, 6.58, 6.59 and 6.60 with 3 ms, 5 ms, 7 ms and 10 ms, respectively. The changing overlap time also affect the arm currents, since the circulating current flow is longer. The arm currents together with the circulating current charges and discharges the stack of the cell capacitors. The shape of the arm currents determine, what shape will be the arm voltages showed in the above Figures. When the current curve is increasing the capacitor charges and when the current curve is descending the capacitor is discharge. In the different operating points, as it can be seen in the Figures below, the current rising and decreasing times can be different or equal, which results in the different or equal charging and discharging areas.

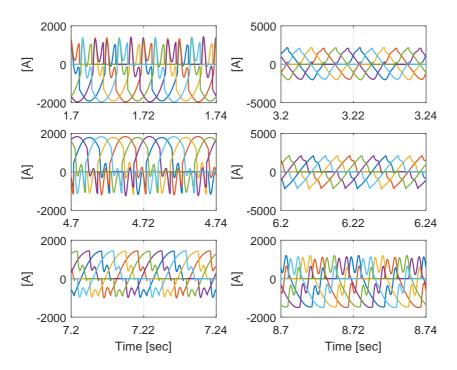


Figure 6.57: Arm currents for the different operation points with 3 ms overlap time

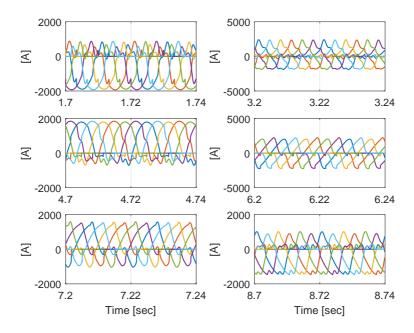


Figure 6.58: Arm currents for the different operation points with 5 ms overlap time

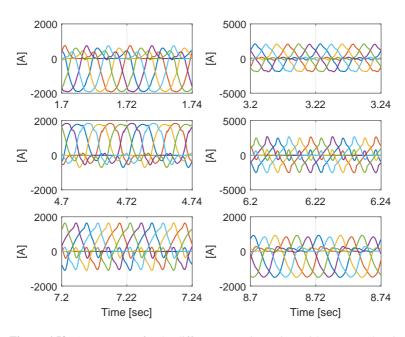


Figure 6.59: Arm currents for the different operation points with 7 ms overlap time

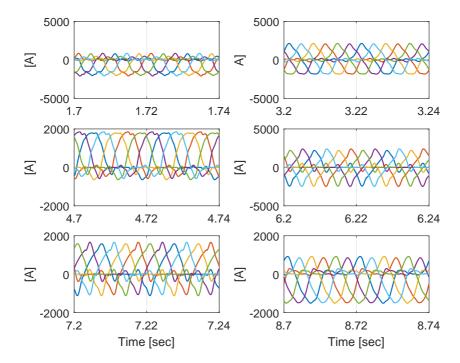


Figure 6.60: Arm currents for the different operation points with 10 ms overlap time

The circulating currents are observed for the different overlap time values in the Figures 6.61, 6.62, 6.63 and 6.64, with 3 ms, 5 ms, 7 ms and 10 ms, respectively. With the increasing overlap time it can be seen, that the presence are increased of circulating currents. As the circulating currents are appearing longer the magnitude of them are reduced. Therefore it can be said that with the increasing overlap time the circulating currents shape becomes wider and smaller. Smaller circulating current cancels designing problem, when the designer should pay attention in the circulating current magnitude, while designing director switches conduction capability. When the overlap time reaches 1 cycle, 10 ms the circulating current becomes uninterrupted and flows all the time, this can be seen in the Figure 6.64.

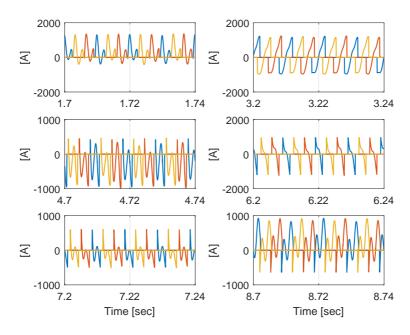


Figure 6.61: Circulating currents for the different operation points with 3 ms overlap time

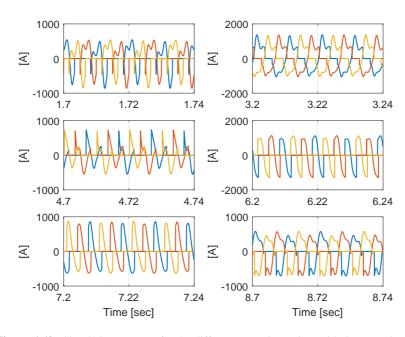


Figure 6.62: Circulating currents for the different operation points with 5 ms overlap time

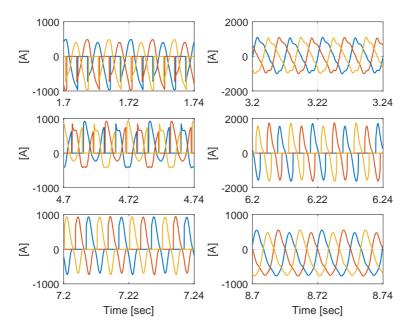


Figure 6.63: Circulating currents for the different operation points with 7 ms overlap time

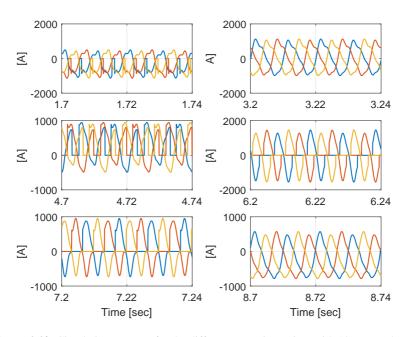


Figure 6.64: Circulating currents for the different operation points with 10 ms overlap time

In conclusion increased overlap time, balances arm voltages for all the operating point cases, but the converter is approaching MMC topology. Therefore the choice of the changing topology or better arm voltage balance should be made. This forces to search the new balancing techniques of the arm voltages. The solution can be the implementation of the third harmonic balancing technique. The main idea behind this is to inject the third harmonic current in the system by creating a way for it between the middle point of the DC and the neutral point of the star transformer in the converter side. The balancing technique is represented in the papers [51] and [52].

The third harmonic injection is done as mentioned above in the papers by connecting one side to the star-point transformer, which is common element in the transmission system, while the other side should be connected to the middle point of the DC link capacitor. Therefore the capacitance in DC link should be splat in two, to create a midpoint. This will require the 2 capacitors i other words the DC capacitance should be divided in two [52]. The result of injecting third harmonic current allows to create the DC component of current into the converter legs. This DC component produces total flow of the energy, which can flow in the cell capacitors or out of them depending on the phase and the magnitude of the injected current [52]. This balancing technique with minor system changes is represented in subsection 6.2.6.

6.2.5 Different values of the capacitance in the cell

As it was mentioned above in the section 6.2.1 the arms cell capacitance will be increased in order to see the effect of the balance in the arm voltages. By following results that by increased capacitance for DC link as it is was done in the subsection 6.2.2 reduces the DC ripple in the DC voltages. The hypothesis can be stated by following these results from subsection 6.2.2: maybe the increased arm cell capacitance will affect the arm voltage deviations and reduce it, therefore the voltages between arms become balanced. The Figure 6.65 represents the arm voltages for all the operation point cases mentioned in subsection 6.2.1 with 8 mF of the cell capacitance for the each submodule, which will result in 80 ms in p.u. system. The overlap time for this case is 1 ms. As it can be seen in the Figure 6.65, when the arms cell capacitance is increased, in this case doubled, the imbalance of the voltage between the arms increases more, comparing with the rated value of 40 ms (4 mF). This results, that increased arm cell capacitance more than the rated value will cause imbalance in the arm voltages. The higher imbalance can be caused, because the higher capacitance value is presence and the short overlap time doesn't have enough time to discharge the lower arm capacitance to the balanced level, therefore the lower arm voltages finds new balancing point and keep balance there. The deviations are even higher between the arm voltages.

Another value of the arm cell capacitance is used of 20 ms or in this system as 2 mF. The Figure 6.66 shows the arm voltages balance in all the operating point cases. In comparison with the Figure 6.22 it can be seen that the reduced cell capacitance value does not help that much to reduce the imbalance between the arm voltages. Still high imbalance are presence in some of the operating point cases. Further reducing the arm capacitance will result in the simulation crash. The crash is observed and Matlab doesn't run anymore. The crash can be related to the fact that circulating current flowing during the 1 ms overlap time discharge capacitance very fast and very fast interruption of current

can not be handled by this system.

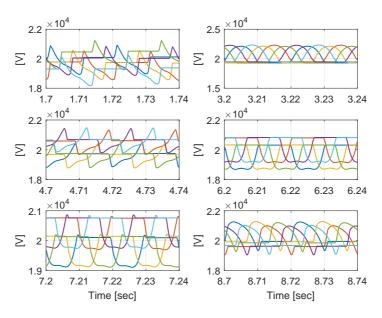


Figure 6.65: Arm voltages with the cell capacitance of 80 ms

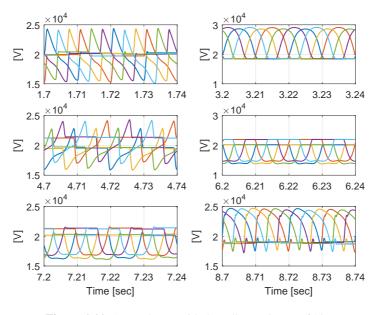


Figure 6.66: Arm voltages with the cell capacitance of 20 ms

The arm currents for the 80 ms in p.u. and 20 ms in p.u. are represented in the Figures 6.67 6.68, respectively. Comparing both Figures with 6.24 it can be seen that the shapes of the arm currents is similar as in Figure 6.67, but the shape of the arm currents in the Figure 6.68 differs from the Figure 6.24. The short and steep spikes can be observed during overlap time, which can be the fast discharge or charge of the arm cell capacitance.

The circulating currents of the both capacitance values are represented in the Figures 6.69 and 6.70 for 80 mF and 20 mF in this system, respectively. It can be seen that in some operating point cases the circulating currents are higher with the 20 mF of the arm cell capacitance, comparing with 80 mF arm cell capacitance. The higher and steeper spikes of the circulating currents are observed with the reduced value of the cell capacitance.

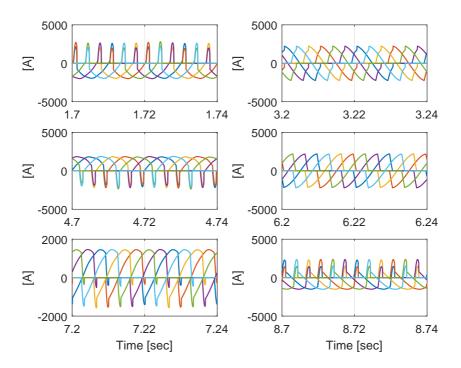


Figure 6.67: Arm currents with the cell capacitance of 80 ms

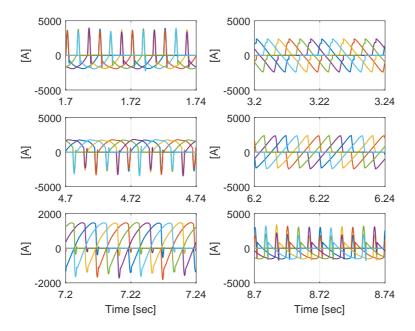


Figure 6.68: Arm currents with the cell capacitance of 20 ms

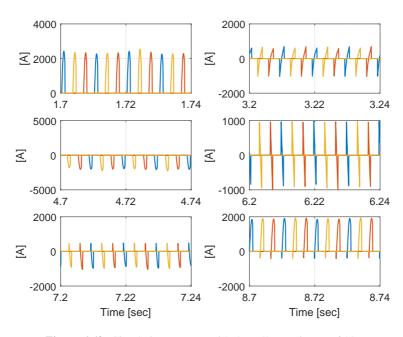


Figure 6.69: Circulating currents with the cell capacitance of 80 ms

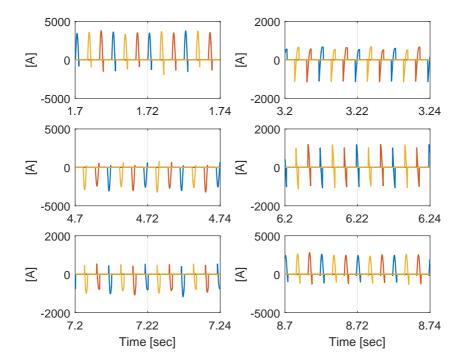


Figure 6.70: Circulating currents with the cell capacitance of 20 ms

To conclude the changes in the arm cell capacitance does not balance the arm voltages. If the capacitance are increased the imbalance becomes even higher. Therefore the way to balance arm voltages is to increase the overlap time as it was presented in the subsection 6.2.4. But this balancing way forces into the change of the topology, when the overlap time is increased till 10 ms.

6.2.6 Balancing technique with the third harmonic current

In this section the third harmonic balancing technique is implemented and different from the mentioned in the subsection 6.2.4 and papers [51], [52] the third harmonic are not injected in the system and controlled. This approach will only creates a path for the third harmonic flow in the converter. The third harmonic originate due to the switching in the converter and circulate in it together with the fundamental current, therefore the balancing of the energy between cell capacitors and DC sides can be achieved by creating a path for the third harmonic current. The connection of the third harmonic implementation for balancing is illustrated in the Figure 6.71. Implementation of the third harmonic path requires a small system changes. It can be seen that the mid point for the capacitance in the DC side is created, additional element as delta - star with neutral point transformer is implemented in the system. Delta - star with neutral point transformer arrangement does not allow the zero sequence third harmonic propagate to the primary side, therefore the

third harmonic only flows between the converter side and DC side. The transformers now are delta - star with neutral point, where star with neutral side belongs to converter side. The transformers do not change voltage level. The wire through impedance Z is connected to the neutral of the star transformer. This type of the connection allows to circulate the third harmonic current between converter side and DC sides. During overlap appearance flowing third harmonic current will increase and helps to balance the arm voltages.

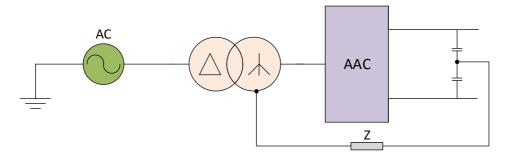


Figure 6.71: Path created by the third harmonic

The impedance, which is located in the wire between the mid point of the capacitors and the secondary side of the transformer, which is star with neutral point. It is consist of the pure inductor, because not to dissipate active power, but reactive and reduce the heating, since the energy will be stored or released in the inductor or from it. The inductor value is tuned to suppress 3rd harmonic current, three different impedance values are selected $Z_1=0.1\Omega$, $Z_2=1\Omega$ and $Z_3=10\Omega$, so that the value of inductor is calculated in equation 6.8, where L_{3rd} is the third harmonic inductor value, f_{3rd} is the 3rd harmonic frequency from fundamental in this case fundamental frequency f=50Hz and Z_i is one of the selected value of impedance.

$$L_{3rd} = \frac{Z_i}{2\pi f_{3rd}} \tag{6.8}$$

Increasing or reducing impedance, reduces or increases the current flowing through the wire. If the flowing current is small the balancing during the overlap will be worse, than when the flowing current is higher. The higher current balances the arm voltages faster than the small current. This hypothesis allows to inspect the different impedance values and compare the arm voltage balancing, during 1 ms of the overlap. The simulation runs for the same operating points, represented in subsection 6.2.1, where the Figure 6.23 represented the arm voltages balancing measured in T2. In this Figure 1 ms overlap time is maintained and as it can be seen the arm voltages balance between the upper and lower arms are different, which means the voltages between arms is not balanced. The high unbalance can be seen during operation points A, B, C, F in the Figure 6.23. The worst case is F, in the bottom right side, where the unbalance is pretty high. The third harmonic current flow during 1 ms overlap time between the upper and lower arms should reduce the unbalance. The worst balanced arm voltages is chosen for the representation from the Figure 6.23, where the operating points A, top left graph, and F, bottom right graph, represent that.

The simulation results with different values of the impedance are represented in the Figure 6.72 for A, top left side from Figure 6.23, operating point and Figure 6.73 for operating case F, bottom right side from Figure 6.23.

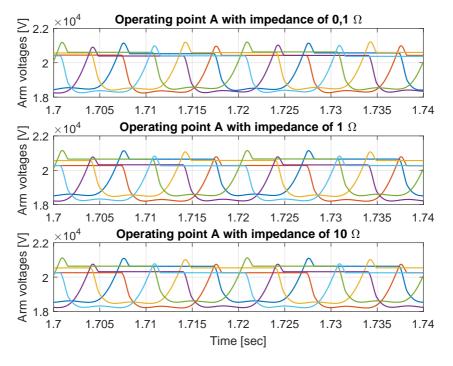


Figure 6.72: Arm voltages with varied value of the impedance for 3rd harmonic of 0.1Ω , 1Ω and 10Ω during operating point A

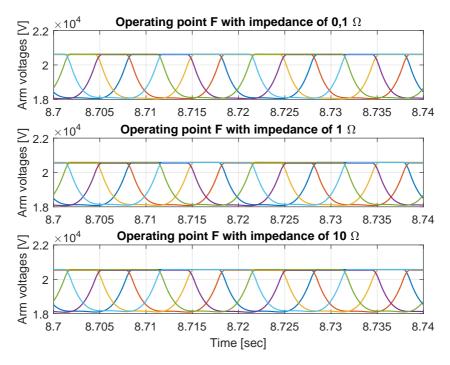


Figure 6.73: Arm voltages with varied value of the impedance for 3rd harmonic of 0.1Ω , 1Ω and 10Ω during operating point F

In the Figures 6.72, 6.73 it can be seen, especially in the first one, when the flowing current is higher, then the arm voltages balance is better. In the second Figure the arm voltages for all impedance values becomes almost the same, because there is enough 3rd harmonic current flowing to help balance the arm voltages.

In comparison with the impedance values the same only resistance values are selected and simulated with the same operating points. The Figures are represented in the 6.74 and 6.75. Very close behaviour comparing with impedance values are observed in these Figures. It can be seen that by increasing resistance or impedance value the balancing gets worse, because the circulating current in the wire between mid point of capacitors and star neutral point becomes smaller. Comparing both cases, one with impedance (pure inductance) and one with resistance it can be say, that both cases give similar arm voltage balancing. The impedance (pure inductance) does not contain active power loses and energy are stored and released in the inductor, while the energy in the resistor is dissipated, furthermore the reactive power are observed in the inductor and not active, which implies to better use impedance in this case than the resistor.

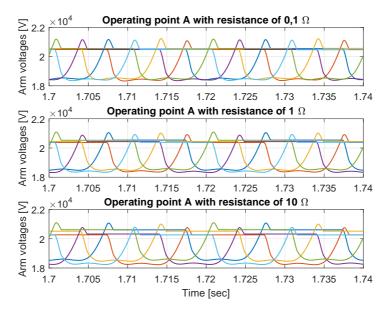


Figure 6.74: Arm voltages with varied value of the resistance for 3rd harmonic of 0.1Ω , 1Ω and 10Ω during operating point A

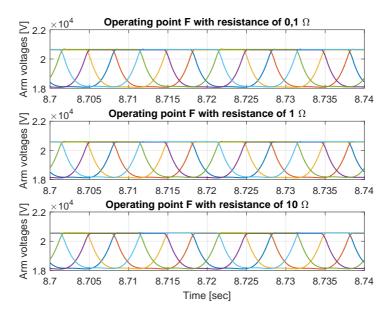


Figure 6.75: Arm voltages with varied value of the resistance for 3rd harmonic of 0.1Ω , 1Ω and 10Ω during operating point F

By creating a path for the circulating third harmonic current, the delta - star with neutral point transformer is necessary. The delta connected primary side does not contain zero sequence current, since they are natural filtered by transformers nature. In order to confirm that the converter current, which is measured current after transformer and the grid current, which is measured before the transformer are compared, with different impedance values. Furthermore the total harmonic distortion (THD) are represented, for the grid current and the converter current. In order to confirm the necessity of this type of the transformer the grid current and the converter current are compared. The THD are represented for the grid currents and for the converter currents.

First of all the Figure 6.76 illustrates the converter currents during different impedance values in the wire and are compared with a grid current, which is similar for all impedance variations. The Figure 6.76 shows A phase of the grid and different converter currents measured in T1. It can be seen that the converter currents are lagging by around 30° from the grid current. The currents are compared during full active power flow from T1 towards T2. The THD analysis is done by using Simulink powergui FFT analysis tool. The FFT of converter currents with different impedance values and the grid current are analyzed and results are represented in the Figures 6.77, 6.78, 6.79 and 6.80. The high bar value of the third harmonic current in the converter currents can be seen in the Figures 6.77 and 6.78, while in Figure 6.79 the third harmonic current does not cause that much influence.

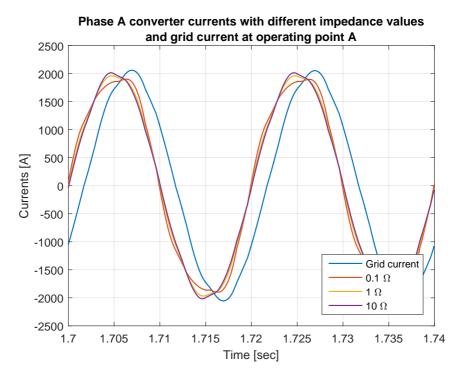


Figure 6.76: Comparison of the grid current and 3 different converter currents due to the different impedance values in the path created for the third harmonic

The Figure 6.77 shows Converter current, when the impedance value is 0.1Ω , which does not suppress third harmonic current a lot, therefore the effect can be seen. It is clearly represents that the fundamental and the 3rd harmonic frequencies are the biggest in this Figure. The total harmonic distortion in this case is 9,83%, which is the highest comparing with other two cases. Nevertheless, the higher third harmonic current is flowing in the converter the faster and better will be arm voltage balance.

The Figures 6.78 and 6.79 illustrate, that by suppressing the third harmonic current the converter current contains less circulation of the third harmonic current.

The grid current in all three cases stays very similar. The phase A grid current and the THD content is represented in the Figure 6.80. Due to the nature of the transformer the third harmonic current does not propagate to the primary side, therefore it is not present there. The harmonics content of the grid current are in boundaries, where they are represented in the article [49]. In this article [49] Table 2 shows current distortion limits for systems rated 120 V through 69 kV. By choosing the maximum short circuit current and maximum demand load current ratio the harmonic content boundaries can be specified by the content. By choosing $I_{sc}/I_L <$ 20, for this case it can be seen that total demand distortion (TDD) for odd harmonics is 5%. TDD is very similar to the THD [53]. Furthermore the boundaries for separate harmonics content is represented separately in Table 2 of [49]. Non of the harmonics reaches the boundaries. This will justify the advantage of using this type of the transformer in the system in order to use a third harmonic balancing technique.

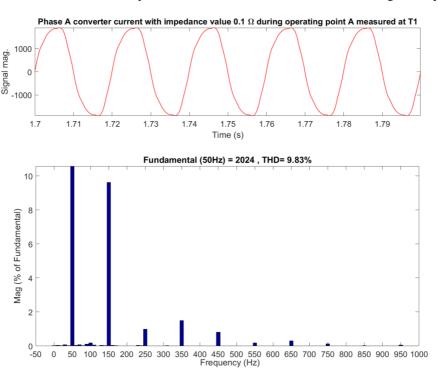


Figure 6.77: Phase A converter current with impedance value 0.1Ω during operating point A measured at T1 and it THD analysis with frequency magnitude in percentage of the fundamental

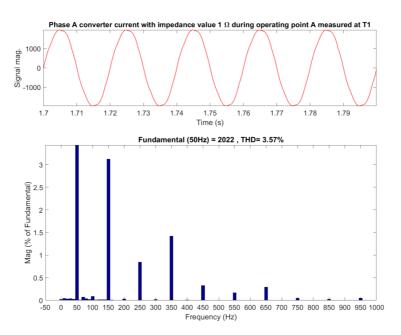


Figure 6.78: Phase A converter current with impedance value 1Ω during operating point A measured at T1 and it THD analysis with frequency magnitude in percentage of the fundamental

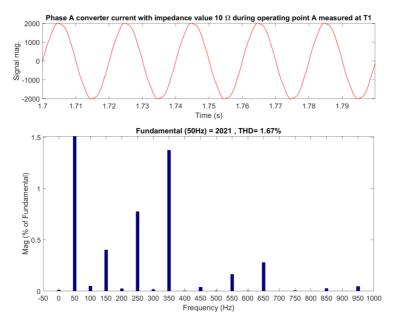


Figure 6.79: Phase A converter current with impedance value 10Ω during operating point A measured at T1 and it THD analysis with frequency magnitude in percentage of the fundamental

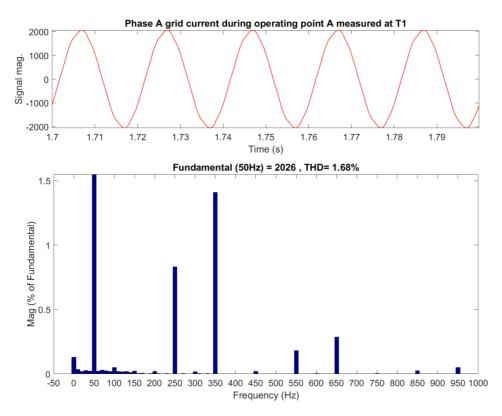


Figure 6.80: Phase A grid current during operating point A measured at T1 and it THD analysis with frequency magnitude in percentage of the fundamental

In conclusion it can be said that using balancing technique with 3rd harmonic current together with overlap time balancing technique allow to balance the arm voltages very well. Nevertheless the system requires additional components as an inductor between the mid point of the capacitors and the star neutral connected point and 2 separate capacitor in DC side in order to create a midpoint. Furthermore the transformers has to be with switched sides, while in the beginning it was star with neutral point - delta and for this case it should be delta - star with neutral point. The trade of between this balancing technique and the costs should be evaluated. The arm voltage balance is achieved without increasing an overlap time, which forces converter topology to change from AAC to MMC, but this technique require additional elements. The transformers in the power system are used anyways, therefore this type of balancing technique can be used, which allows to achieve better arm voltage balance. The harmonics content in the grid current are in boundaries and match IEEE 519 [49] requirements.



CONCLUSION

In this master thesis the simulation of the average alternate arm converter model is created. The simulation model is created from the beginning, by starting from the one-phase model and end up in the point to point connection scheme. The behaviour and improvement of the simulation were done in the small steps till the results were reasonable for continuation of the further steps. In the beginning of the one-phase simulation the problem was confronted of the frequent simulation crash, therefore the Simscape block diagrams were introduced.

The two balancing techniques for the one-phase average model was implemented.

- The "sweet spot balancing technique balanced arm voltages well, but the main drawback, was sensitive to the AC voltage changes.
- The overlap balancing technique was implemented, where the circulating current for the short period of time are created, by closing both upper and lower arms director switches. Therefore both arms are in conduction and running current balance the voltage in the arms. This arm voltage balancing technique was used in entire master thesis in order to keep balance between the arm voltages.

The simulation end up with the point to point connection scheme. The improved control of the system was implemented. The improved and expanded control created additional challenges. Some of the challenges were converted in the study cases.

The main challenges of the point to point connection scheme study cases are found to be:

- Voltage balance between the arms. Especially in the point to point connection scheme, when the different operating points were simulated. The issue was solved by implementing third harmonic current control merged together with used overlap control.
- Circulating current during the overlap period, which requires an additional designing attention in order to evaluate director switch conduction capabilities. This issue can be solved by extending the overlap time. The extended overlap time result in smaller but wider circulating current.

• DC voltage ripple due to circulating current and mainly due to the charging and discharging DC side capacitance. In the beginning of the modeling a simulation DC side was assumed to be constant value, therefore charging and discharging capacitors results in DC voltage oscillations. This issue can be solved as it was did, by increasing the DC side capacitance value. Nevertheless increased capacitance value results in higher costs and bigger size of the capacitor.



FUTURE WORK

Considering that it is a new topology of the converter lot of the things can be done in the future. Some of the future work suggestions are stated below:

- Circulating current can be controlled, the control strategy should be implemented therefore it can cause less DC voltage ripple and neglects the design issue for the director switch conduction capability.
- Implementation of the new ways to balance the voltages between the arms, which was the main issue in this master thesis.
- Creating simulation of the full scale model, in order to investigate the physics and the behaviour of the separate submodule in the arms. This can also result in the more difficult challenges, because the balancing should be done in couple loops, like cell voltage balance and then arm voltage balance.
- AAC comparison with the MMC topology can be done for the same system.
- Building a prototype model. The prototype model will be interesting and more accurate of investigating a behaviour of the alternate arm converter, nevertheless it costs more than making simulation.

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Appendix A

.1 Overlap analysis for one-phase simulation model of AAC

Case 1

With 0 time overlap of the director switches the arm voltages represented in Figure 1

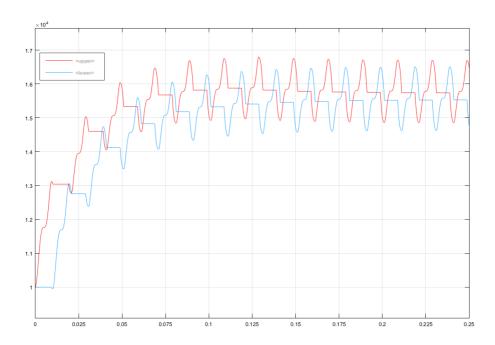


Figure 1: Voltage dynamics in the arm stacks case1

Case 2

Same conditions. The constant in the overlap model is -300 and 300. This gives the overlap time 0.01005-0.0092=0.00085s This is 0.85ms, which is small. The voltage dynamics for this case represented in Figure 2

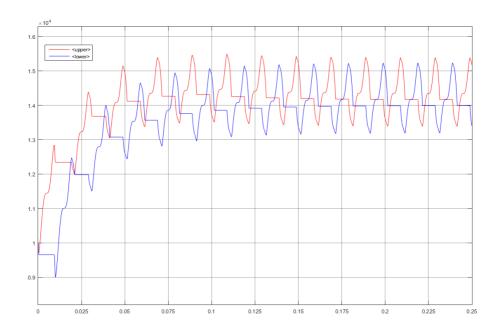


Figure 2: Voltage dynamics in the arm stacks case2

Same conditions. The constant in the overlap model is -600 and 600. This gives the overlap time 0.01015-0.0091=0.00105s This is 1.05ms. The voltage dynamics for this case represented in Figure 3. The voltage in the arms align more in the line, the voltage is better balanced when the overlap is around 1ms.

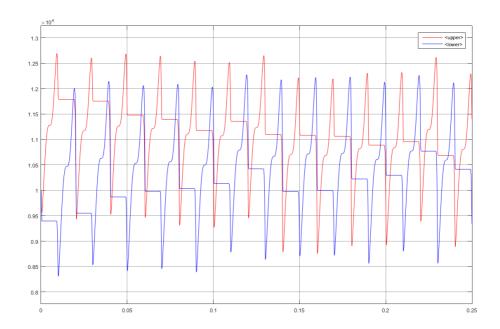


Figure 3: Voltage dynamics in the arm stacks case3

Same conditions. The constant in the overlap model is -900 and 900. This gives the overlap time 0.0103-0.00895=0.00135s This is 1.35ms. The voltage dynamics for this case represented in Figure 4. The voltage in the arms align more in the line, the voltage is better balanced when the overlap is around 1.3ms.

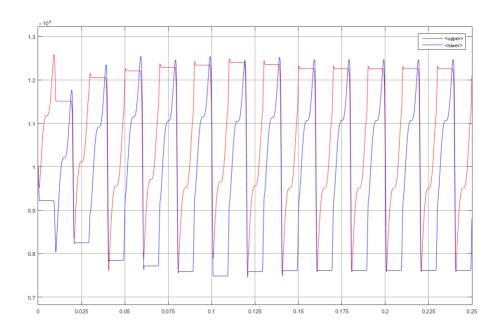


Figure 4: Voltage dynamics in the arm stacks case4

Same conditions. The constant in the overlap model is -1200 and 1200. This gives the overlap time 0.01045-0.0088=0.00165s This is 1.65ms. The voltage dynamics for this case represented in Figure 5.

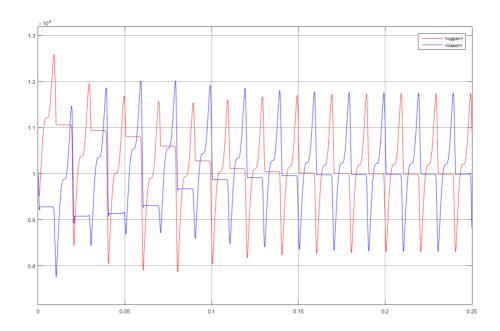


Figure 5: Voltage dynamics in the arm stacks case5

Same conditions. The constant in the overlap model is -1500 and 1500. This gives the overlap time 0.01065-0.00865=0.002s This is 2ms. The voltage dynamics for this case represented in Figure 6.

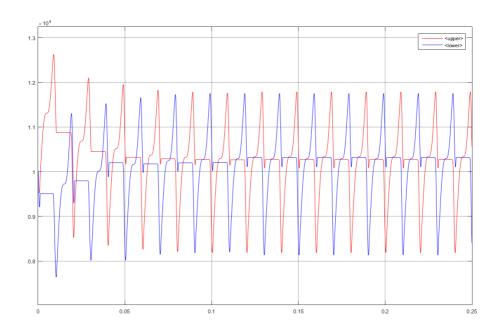


Figure 6: Voltage dynamics in the arm stacks case6

Same conditions. The constant in the overlap model is -1800 and 1800. This gives the overlap time 0.0107-0.00845=0.00225s This is 2.25ms. The voltage dynamics for this case represented in Figure 7.

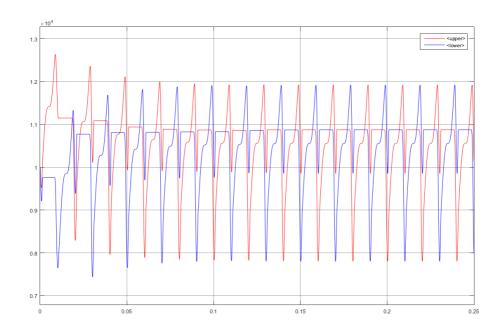


Figure 7: Voltage dynamics in the arm stacks case7

Same conditions. The constant in the overlap model is -2100 and 2100. This gives the overlap time 0.0112-0.00835=0.00285s This is 2.85ms. The voltage dynamics for this case represented in Figure 8.

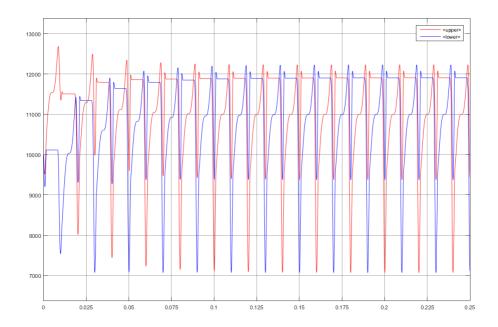


Figure 8: Voltage dynamics in the arm stacks case8

Same conditions. The constant in the overlap model is -2400 and 2400. This gives the overlap time 0.01155-0.0082=0.00335s This is 3.35ms. The voltage dynamics for this case represented in Figure 9.

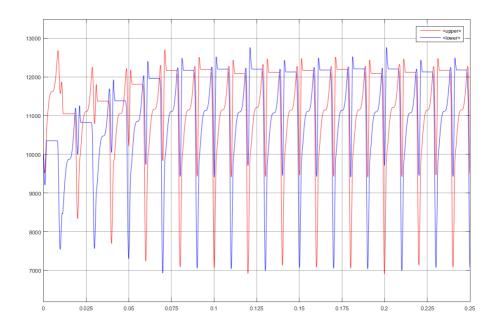


Figure 9: Voltage dynamics in the arm stacks case9

Same conditions. The constant in the overlap model is -2700 and 2700. This gives the overlap time 0.01195-0.008=0.00395s This is 3.95ms. The voltage dynamics for this case represented in Figure 10.

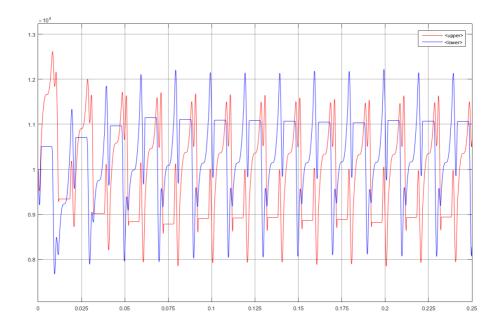


Figure 10: Voltage dynamics in the arm stacks case 10

Same conditions. The constant in the overlap model is -3000 and 3000. This gives the overlap time 0.012-0.0078=0.0042s This is 4.2ms. The voltage dynamics for this case represented in Figure 11.

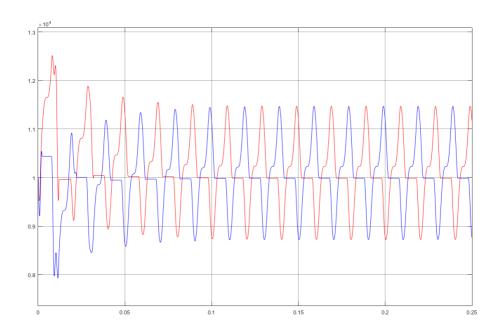


Figure 11: Voltage dynamics in the arm stacks case11

Same conditions. The constant in the overlap model is -3300 and 3300. This gives the overlap time 0.0121-0.0076=0.0045s This is 4.5ms. The voltage dynamics for this case represented in Figure 12.

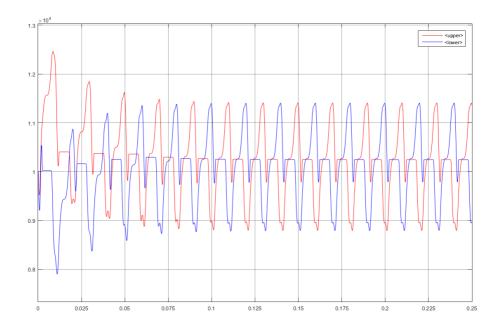


Figure 12: Voltage dynamics in the arm stacks case 12

Same conditions. The constant in the overlap model is -3600 and 3600. This gives the overlap time 0.0126-0.0073=0.0053s This is 5.3ms. The voltage dynamics for this case represented in Figure 13.

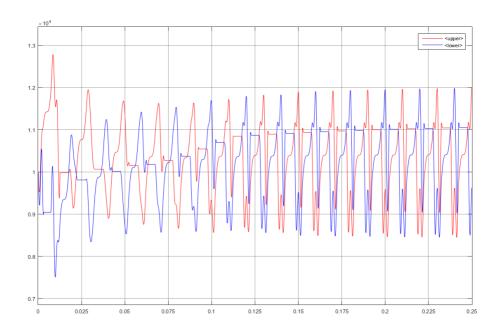


Figure 13: Voltage dynamics in the arm stacks case 13

Same conditions. The constant in the overlap model is -3900 and 3900. This gives the overlap time 0.01265-0.00705=0.0056s This is 5.6ms. The voltage dynamics for this case represented in Figure 14.

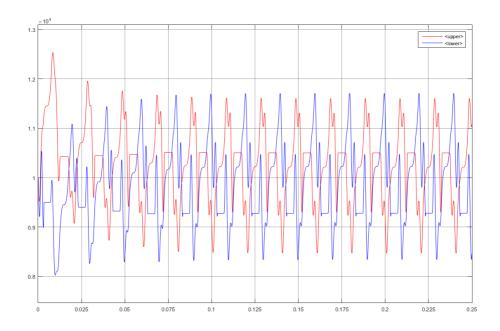


Figure 14: Voltage dynamics in the arm stacks case14

Same conditions. The constant in the overlap model is -4200 and 4200. This gives the overlap time 0.0133-0.00675=0.00655s This is 6.55ms. The voltage dynamics for this case represented in Figure 15.

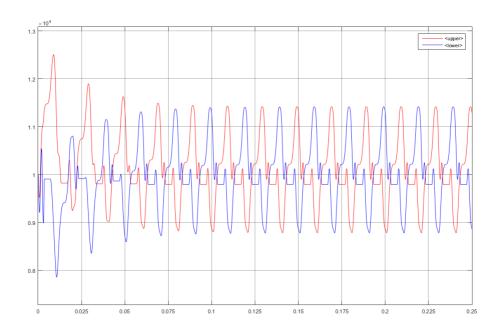


Figure 15: Voltage dynamics in the arm stacks case 15

Same conditions. The constant in the overlap model is -4500 and 4500. This gives the overlap time 0.0134-0.0065=0.0069s This is 6.9ms. The voltage dynamics for this case represented in Figure 16.

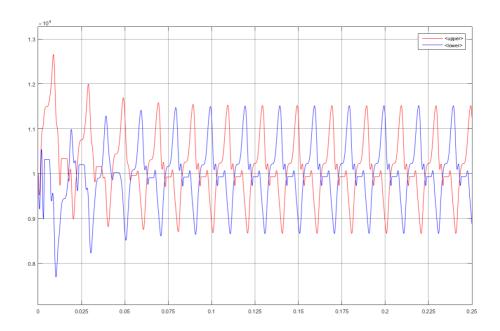


Figure 16: Voltage dynamics in the arm stacks case 16

Same conditions. The constant in the overlap model is -4800 and 4800. This gives the overlap time 0.07415-0.06595=0.0082s This is 8.2ms. The voltage dynamics for this case represented in Figure 17.

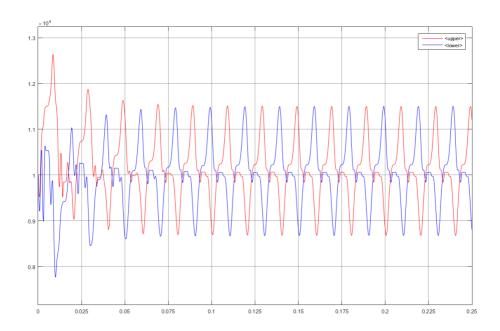


Figure 17: Voltage dynamics in the arm stacks case17

Same conditions. The constant in the overlap model is -5100 and 5100. The one director switch are mostly on, this gives the arm voltage output instability. The overlap time at some points are more than 10ms and sometimes does not appear at all. The voltage dynamics for this case represented in Figure 18. As it can be seen the dynamics for this case is unstable, the voltage fluctuates, charge or discharge the capacitors. By increasing the constants and the overlap time, the output AC voltage will be even more distorted the voltage fluctuates in the arms faster.

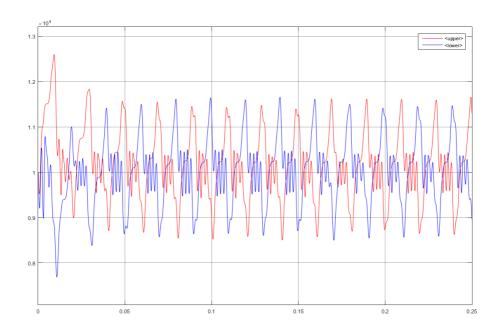


Figure 18: Voltage dynamics in the arm stacks case 18

All the data represented in the Figure 19

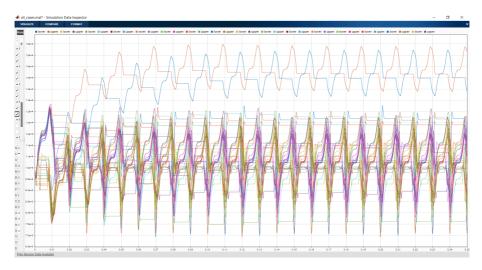


Figure 19: All data

Conclusion

The case number 11 and number 4 is interesting. The case 11 for further investigation where that flat moment of the voltage in the curve was on 10000kV. The constant, which

was got on that line was -3008 and 3008, this gives 4.2 ms of the overlap time. This is the most balanced moment because the charging and discharging for the both arms are more or less symmetrical, except in the beginning for the first 40 ms, due to the initial conditions. After 150 ms the flat part, where the capacitor nor charges or discharges are at the same line and not fluctuate anymore. In same cases the output AC voltage has some spikes, which result in the director switches to open and close rapidly. This creates the circulating current flowing and therefore charges and discharges capacitor. The result of this is rapidly fluctuated voltage in the some cases.

The spikes mostly occur in the beginning of the simulation, where later on it settles down. Very high resistance in parallel with the inductor does not reduce spikes. The diode does not reduce the spikes either, furthermore it creates even more distorted output AC voltage.

Appendix B

.2 MATLAB codes

MATLAB code for the island mode of the AAC

```
clc
clear all
close all
Ts = 50e - 6;
%% Values of the converter
% Rated power
P_r = 20e6;
V_ac = 0.5*10e3;
% DC voltage
Vdc = 10e3;
% Ac voltage of the converter
%V_ac = (4/pi)*Vdc/2;
% Cell voltages
Vce11_u = -5e3;
Vcell_1 = 5e3;
Vbias = 10e3;
Init_amp = 10e3;
% Frequency
f = 50;
w = 2 * pi *f;
% Inductance
L = 100e - 6;
R = 0.01;
```

```
% Load
R_load = 20;
L_1oad = 2*R_1oad/w;
Rdc = 0.001:
% Switches
Ron = 0.000001;
% Cells information
N = 9; % Number of cels per arm in the converter
C_{-cell} = 4e-3; % Capacitance in one submodule
% Making p.u. system:
S_base = 20e6;
V_base = 20e3;
%% Control part
%% Overlap
Rs = 1e-3;
toverlap = 1*1e-3;
voverlap = V_ac*sin(w*toverlap*0.5);
Neg\_const = -voverlap;
Pos_const = voverlap;
%% Filter
Ti = 0.0002;
\%\% Tunning 1 - 1st order assumption
% This method are using by making assumption
% of the first order
% system by neglecting the arm inductor.
%This assumption leads to
% the 1st order response.
%Where the Ti = 0.002s, time constant for
% filter and the equivalent time constant
```

```
%Teq = 50e-3 first order
% approximation of closed loop current
%controller response.
\% \text{ Teq} = 50e - 3;
\% K = 1/(R_1oad + R);
\% \text{ kid} = 1/(\text{Teq} * \text{K});
% kpd = kid*Ti;
%
% kpq = kpd;
% kiq = kid;
\%\% Tunning 2 - 2nd order
% The second tuning method with the arm inductor,
%which governs a
% time constant of that L/R division.
T1r = L/(R_1oad+R);
kid = (R_load + R)/(2*Ti);
kpd = kid * Tlr;
kpq = kpd;
kiq = kid;
% Voltage PI controller tunner
Teq = 2*Ti;
Tv = 10 * Ti;
kidV = 1/(2*(R_1oad + R)*Tv);
\%kidV = 1/((R_load + R)*10e-3);
kpdV = kidV * Teq; %(L/(R_load+R));
kpqV = kpdV;
kiqV = kidV;
MATLAB code for the grid connected AAC
clc
clear all
close all
Ts = 50e - 6;
%% Values of the converter
```

```
% Rated power
P_r = 20e6;
VacLL = 11e3;
V_ac = VacLL* sqrt(2/3);
% DC voltage
Vdc = 20e3;
% Grid connected case
Lg = 4.1e - 3;
Rg = 0.0605;
Rsource = 0.0003;
Lsource = 0.3e-3;
% Cell voltages
Vce11_u = -5e3;
Vcell_1 = 5e3;
Vbias = 10e3;
Init_amp = 10e3;
% Frequency
f = 50;
w = 2 * pi *f;
% Inductance
L = 100e - 6;
R = 0.01;
% Load
R_{-1}oad = 20;
L_1oad = 2*R_1oad/w;
Rdc = 0.001;
% Switches
Ron = 0.000001;
% Cells information
N = 9; % Number of cels per arm in the converter
C_{cell} = 4e-3; % Capacitance in one submodule
```

```
% Making p.u. system:
S_base = 20e6;
V_base = 20e3;
% Overlap
Rs = 1e - 3;
toverlap = 1*1e-3;
voverlap = V_ac*sin(w*toverlap*0.5);
Neg\_const = -voverlap;
Pos_const = voverlap;
%% Filter
Ti = 5e - 4;
T1r = (Lg+L)/(Rg+R);
kid = (Rg + R)/(2*Ti);
kpd = kid * Tlr;
kpq = kpd;
kiq = kid;
%% P- Q control
Pf = 10e-3; % Active reactive power filter
Teq = 2 * Ti; % Equivalent current control time constant
Vd = V_ac;
Ki_Pd = 1/(2* Pf * Vd);
Kp_Pd = Ki_Pd * Teq;
Ki_Pq = -Ki_Pd;
Kp_Pq = -Kp_Pd;
```

MATLAB code for the point to point connected system

clc

```
clear all
close all
Ts = 50e - 6;
%% Values of the converter
% Rated power
P_{r} = 20e6;
VacLL = 11e3;
V_ac = VacLL* sqrt(2/3);
% DC voltage
Vdc = 20e3;
%% Grid connected case
Lg = 4.1e - 3;
Rg = 0.0605;
Rsource = 0.0003;
Lsource = 0.3e-3;
% Cell voltages
Vce11_u = -5e3;
Vcell_{-1} = 5e3;
Vbias = 10e3;
Init_amp = 10e3;
% Frequency
f = 50;
w = 2 * pi *f;
% Inductance
%L = 0.00001;
%L = 0.005;
L = 100e - 6;
R = 0.01:
% Load
R_1oad = 20;
L_1oad = 2*R_1oad/w;
Rdc = 0.001;
% Switches
```

```
Ron = 0.000001;
% Cells information
N = 9; % Number of cels per arm in the converter
C_{-cell} = 4e-3; % Capacitance in one submodule
% Making p.u. system:
S_base = 20e6;
V_base = 20e3;
% Control part
%% Overlap
Rs = 1e-3;
toverlap = 1*1e-3;
voverlap = V_ac*sin(w*toverlap*0.5);
Neg\_const = -voverlap;
Pos_const = voverlap;
% Filter
Ti = 5e-4;
Tlr = (Lg+L)/(Rg+R);
kid = (Rg + R)/(2*Ti);
kpd = kid * Tlr;
kpq = kpd;
kiq = kid;
%% P− Q control
Pf = 2e-3; % Active reactive power filter
Teq = 2 * Ti; % Equivalent current control time constant
Vd = V_ac;
Ki_Pd = 1/(2* Pf * Vd);
Kp_Pd = Ki_Pd * Teq;
Ki_Pq = -Ki_Pd;
```

```
Kp_Pq = -Kp_Pd;
%% DC side calculations
1 = 20;
c_DC = 0.212e - 6;
C\_DC = 1 * c\_DC;
C_dc_side = (0.01 * 20e6)/(0.5 * Vdc^2);
i_c = (C_dc_side*Vdc)/0.01;
% Droop controll
% This is ok. calculations in the sheet
delta = 0.05;
rho = delta * (Vdc/P_r);
Gain_droop = 1/rho;
frq_rho = delta*(f/P_r);
% DC side parameters
r_dc_side = 11.3e-3;
R_dc_side = 1 * r_dc_side;
```

Appendix C

.3 Simulink models of the point to point connection

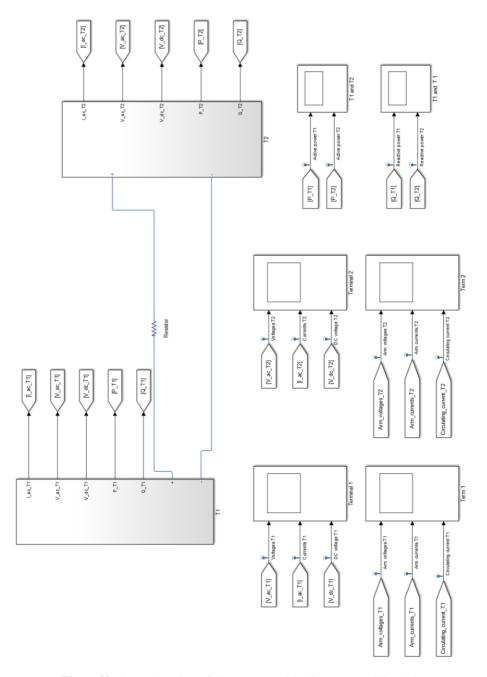


Figure 20: General preview of the system modeled in MATLAB/Simulink

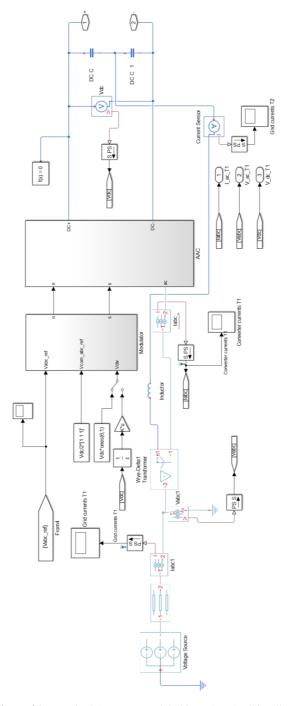


Figure 21: Terminal 1 system modeled in MATLAB/Simulink

161

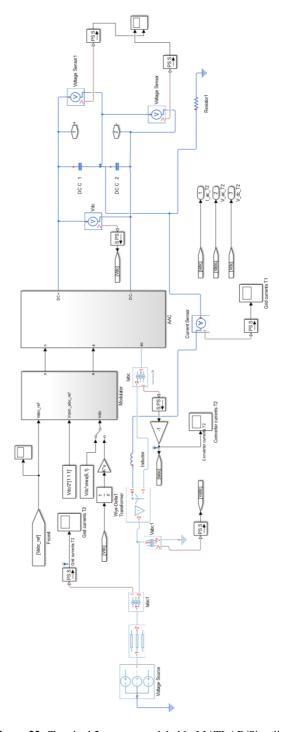


Figure 22: Terminal 2 system modeled in MATLAB/Simulink

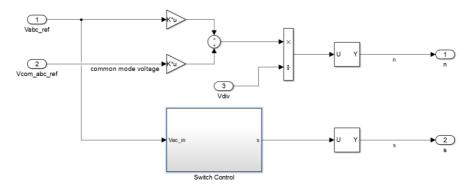


Figure 23: Modulator modeled in MATLAB/Simulink

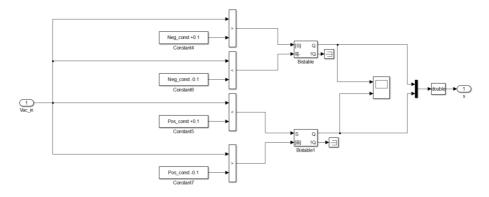


Figure 24: Overlap control for the switches modeled in MATLAB/Simulink

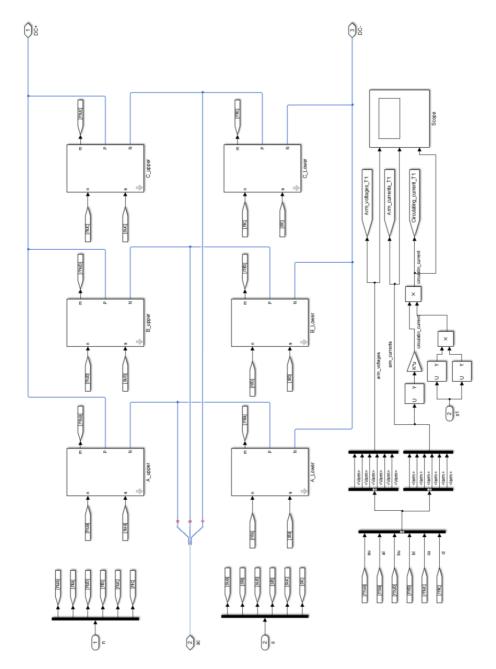


Figure 25: Alternate arm converter representation modeled in MATLAB/Simulink

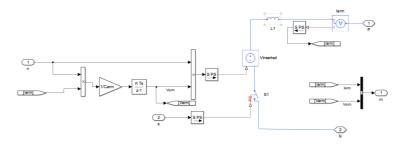


Figure 26: Upper arm of the AAC modeled in MATLAB/Simulink

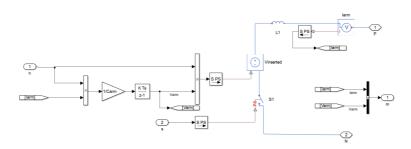


Figure 27: Lower arm of the AAC modeled in MATLAB/Simulink

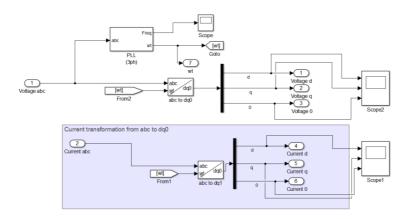


Figure 28: Transformation from abc reference frame to the dq0 reference frame modeled in MAT-LAB/Simulink

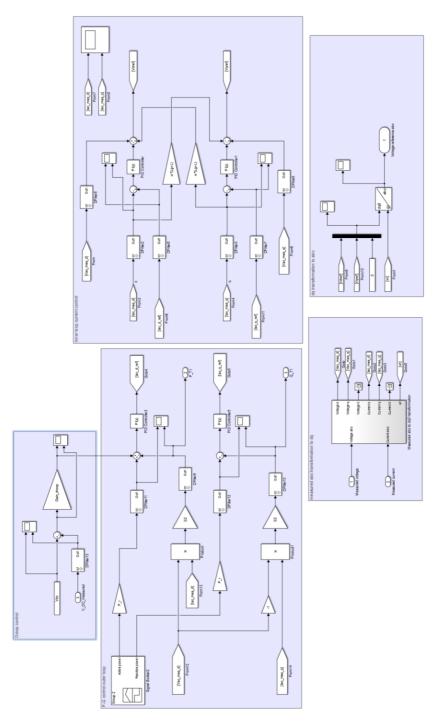


Figure 29: Control in T1 of the point to point connected system modeled in MATLAB/Simulink