Technologies enabling 3D stacking of MEMS

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Abstract—**In order to realize reliable 3D stacking of micro electromechanical systems (MEMS), interconnection and through wafer via technologies have been adapted from other areas and verified for MEMS applications. True stacking of a system including MEMS requires vias through the MEMS and electrical and mechanical interconnection to other devices like signal conditioning units and communication- and power devices. MEMS will typically have specific requirements regarding mechanical issues like stiffness, robustness, volume, and mass. The mechanical issues limit the range of applicable technologies. In this work three interconnection technologies have been selected, evaluated, and compared: Au stud bump bonding, SnAg micro bumps, and the SLID (solid liquid interdiffusion) technology using Sn and Cu. One via technology has been considered, namely hollow vias, which has been improved and tested in this work.**

Index Terms—**MEMS, through wafer vias, stud bump bonding, micro bumps, through silicon vias, SLID**

I. Introduction

3D stacking provides the advantages of short interconnections, miniaturization, and compact packaging. Within the CMOS-chip community, substantial research has been carried out with the objective of realizing 3D stacked chips. Chip stacking technologies have been presented by among others Tohoku University (ZyCube) [1], Tezzaron (SuperVias™/FaStack™) [2], Rensselaer Polytechnic Institute (RPI) [3], Fraunhofer IZM (VSI®) [4], Infineon [5], Toshiba [6], ASET [7], IBM [8], IMEC [9] and MIT [10]. To obtain a broader range of applications, CMOS chips are often combined with sensor or actuator functions and power supplies. However, to integrate such devices into a 3D stack implies additional challenges compared to 3D stacks consisting solely of CMOS chips. Stacking of micro electromechanical systems (MEMS) can be more challenging than 3D stacking of purely electronic devices due to mechanical concerns. In order to achieve truly compact, 3D stacked MEMS units, it is necessary to provide electrical interconnections *through* the individual devices in addition to mechanical and electrical interconnections *between* the devices. In this manner, electrical access to all the various parts within the integrated MEMS unit can be achieved through the top (or bottom) of the unit, without the need of complex wiring schemes to the individual devices.

For the electrical interconnection through the MEMS, through wafer vias (holes through the wafer with isolated walls filled or coated with conductive material) are needed. The available via technologies [1-10] for CMOS chips are all based on thinning the silicon wafer, since only a thin surface layer on the front side of the wafer is required for proper operation. Although thinning of wafers makes it easier to realize through-wafer vias, this is not always a viable solution for MEMS. Many MEMS sensors require mechanical stability and strength, while a certain volume and mass are needed for most MEMS actuators. Therefore, vias through wafers with a thickness of ~200-400 µm are required for most MEMS. The smallest holes that can realistically be made through such a wafer thickness have a diameter of about 10 to 20 µm.

A few via technologies suitable for MEMS have been presented. PlanOptik [11] produces wafers with vias by structuring a silicon wafer by DRIE and filling the cavities with a borofloat glass. After filling, the wafer is ground and polished, leaving a wafer containing Si pins isolated by glass trenches. Silex [12] proposes a technology where silicon wafers are etched by DRIE. A dielectric that fills the trenches is deposited, and finally the wafers are ground on the back side to expose the filled trenches. For both technologies the typical via pitch is 100 µm and the via resistance is in the range of a few ohms.

Earlier, we have presented a solution for hollow vias with aspect ratio (AR) 15 in 300 µm thick, 100 mm wafers [13]. By keeping the vias hollow, the costly and time-consuming process of filling 10-20 µm diameter holes is avoided. Hollow vias also eliminate the reliability concerns related to the large mismatch in coefficient of thermal expansion between the substrate silicon and filling materials like for instance Cu. If hermeticity is desired, the vias can be sealed by bonding to other layers. In this paper, we describe the development of a via process for 300 µm thick, 150 mm wafers with AR 6-15 (rectangular holes). The process is versatile, robust, and suitable for industrial production.

For the electrical and mechanical interconnection between devices, wire bonding, tape automated bonding (TAB), and flip chip bonding are technologies that can be considered. However, flip chip bonding is the most relevant technology

This report is partly based on the e-CUBES project (http://ecubes.org) which is supported by the European Commission under support-no. IST-026461. Preben Storås is with REC Solar, P.O. Box 59, NO-1302 Sandvika, Norway. Maaike, M. V. Taklo and the other authors are with SINTEF, Gaustadalléen 23C, 0373 OSLO, NORWAY (phone: +47 22067592; fax: +47 22067321; e-mail: MaaikeMargrete.Visser.Taklo@ sintef.no).

for stacking of chips with a small footprint. Both wire bonding and TAB require larger bonding areas than the flip chip technology and they are also normally limited to provide electrical connections to only one side of the chips. The bonding pads for the flip chip technology can be placed anywhere on the device. This feature combined with vertical vias may be used to stack more than two chips.

Flip chip bonding is a mature process. There are numerous commercial suppliers of flip chip services, like FCI [15], Amkor [16] and IBM (C4NP) [17]. In addition, various bonding technologies based on thermocompression, plasma activation, or gluing have been presented [1, 2, 3, 9, 10, 14]. However, 3D stacking of MEMS is different from the common use of flip chip processes, so only a few existing processes are applicable.

The footprints of the chips to be bonded are expected to change from design to design, thus a chip-to-wafer bonding process is needed. The chips to be bonded will all be made of silicon, so stress issues are believed to be negligible. Therefore, small bumps and a small stand-off height are desired, in contrast to the large bump size used for flip chip bonding a silicon device onto a ceramic or plastic substrate. To comply with the post-processing of the 3D stack, the bonding should be able to withstand temperatures in the range of 200-300°C without significant deterioration. Finally, environmental concerns demand the use of lead-free materials.

The technologies that fulfilled all the requirements of chip-to-wafer bonding (i.e. low gap size and high temperature tolerance) were Au stud bump bonding, lead-free electroplated solder bumps, and the SLID (solid liquid interdiffusion) technology using Sn and Cu [4]. Electroplated SnAg micro bumps were selected among the available lead-free solder bumps. This paper describes the testing of the selected technologies for 3D stacking of MEMS.

II. Experimental

A. Vias

Two different test designs were prepared for the via experiments; one containing square via holes in the range of 14 µm x 14 µm to 26 µm x 26 µm (referred to as 1st generation), and another one containing 20 µm x 50 µm and 50 µm x 50 µm holes (referred to as 2nd generation). Each of the designs included three mask layers: Via etching (DRIE), front side metal layer, and backside metal layer. The designs contained test structures for evaluation of via pitch, DRIE processing, and electrical measurements. One of the dies contained within the mask layout for the 2nd generation design is shown in Fig. 1. The metal layers on the front and back sides, along with the vias, formed a daisy chain permitting measurements through via arrays ranging from 2 to 100 vias. Metal pads for probing of the structures were provided on the front side of the wafer. The via pitch varied from 50 µm to 200 µm depending on via size and array configuration.

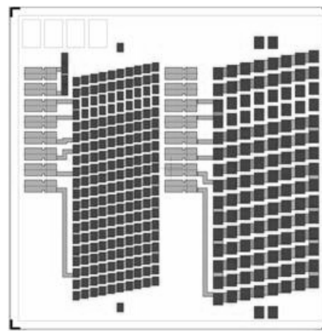

Fig. 1. Two arrays of rectangular 20 µm x 50 µm vias with different pitch. Dark grey: back side metal; Light grey: front side metal. The vias are arranged in a staggered formation to ease inspection of cross sections after etching.

DRIE processing was performed on DRIE tools AMS200SE I-Speeder and AMS200SE I-Productivity from Alcatel built up around ICP reactors. Two options were available, electrostatic and mechanical clamping. A Bosch-type etching process was used. The goal was to find a fast and reproducible process, giving vertical sidewalls. More than seventy 150 mm wafers with thicknesses ranging from 300 µm to 650 µm were provided for the via process development. Blind holes ~300 µm deep were etched in thick wafers before cleaving and inspection whereas through holes were etched in thinner wafers. The 1st generation vias were etched with a 2 µm thermal SiO_2 etch mask and mechanical clamping. The back side material of the wafers was either Al, SiO_2, or Al over SiO_2. For the 2nd generation vias the mask material was changed to Al due to the high selectivity of the plasma etch to Al. Electrostatic clamping was used. Etch processes showing promising results were selected for small-scale "production" runs to evaluate the ability for processing several wafers in succession. The simulated production runs consisted of processing 6 consecutive wafers. The evaluation of via cross sections was performed in a scanning electron microscope (SEM) Quanta 600 FEG from FEI Company.

The etched wafers were thermally oxidized, coated with 1 µm polysilicon, doped and sputtered with Al as described earlier in [13]. The 1 µm LPCVD polysilicon was deposited in a hot-wall batch furnace. Phosphor gas-phase doping of the polysilicon was performed with a $POCl_3$ source.

The patterning of the conductive layers could not be performed with standard lithography using spin coating of resist due to the presence of through holes in the wafers. To cover wafers containing through-holes, the dry-film resist MX5015 from DuPont was used instead. The wafers were laminated using a LEONARDO 200 laminator from Microcontrol Electronic. The resist patterning was performed at Fraunhofer IZM [19]. After resist patterning, different etching processes were evaluated. Wet etching of the Al with Al-etch (40-50°C) and the polysilicon with TMAH (70-80°C) was tested. Other wafers were dry etched. The dry etching was done at Philips [20].

B. *Interconnection points*

Dummy chips and dummy substrate wafers without vias or actual MEMS structures were bonded for testing the interconnection points. Two test chips were designed for the bonding experiments. Alignment test chips (288 contact points per chip) were designed for visual inspection. The desired alignment accuracy was 5-10 µm. Electromechanical test chips (212 contact points per chip) had two electrical test geometries: A daisy chain of 100 interconnection points (pitch 100 µm) with a spy pad inserted at interconnection point no. 50 (left in Fig. 2), and a realistic MEMS structure with 10 I/O pads placed in a line at the edge of the chip (right in Fig. 2). The area between the two test structures was filled with dummy metal, where dummy interconnection points could be placed in order to increase the mechanical strength of the bond.

Test die wafers and test substrate wafers were designed, so that individual dies could be bonded onto a full wafer. On the die wafers the chip dimension was 2 mm × 2 mm. On the substrate wafers, the chip dimension was 4 mm × 4 mm. Fig. 2 shows an overlap image of the 4 mm × 4 mm area on the substrate with the location of the bonded die in the centre. The Al patterns of the two surfaces overlapped in the areas where the interconnection points were to be placed.

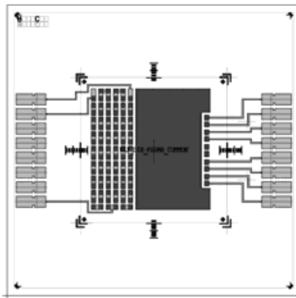

Fig. 2. The design of the electromechanical test chip. Overlay of metal layers is dark grey.

Test wafers were fabricated to compare the three technologies selected for electrical and mechanical interconnection between devices. Silicon wafers with thickness 600 µm, diameter 150 mm, and <100> orientation were used. A layer of 750 nm thermal SiO_2 was grown, and 1.2 µm thick Al was sputtered for routing. On the wafers to be bonded with SnAg bumps and SLID technology, a 500 nm thick PECVD layer was deposited on top of the Al routing. 10 µm × 10 µm openings in the PECVD oxide were made at the location of the contact points.

Table I shows an overview of the bonded substrate wafers. The bonding of Au stud bumped dies was done with a chuck temperature of 220°C and a constant tool temperature of 250°C. The bond force was 40 N and the time per chip was 10 s. Two wafers were bonded with an underfill, NCP DELO MONOPOX MK055, and two wafers were bonded without underfill, see Table I.

TABLE I
OVERVIEW OF BONDED SUBSTRATE WAFERS

Wafer name	Process and process details
Substrate 2	Au stud, NCP DELO MONOPOX MK055
Substrate 3	Au stud, NCP DELO MONOPOX MK055
Substrate 4	Au stud, No underfill
Substrate 5	Au stud, No underfill
Substrate 5	Au stud, Epotek 353 ND (only selected chips)
Substrate 6	SnAg micro bumps, 8 µm Cu UBM
Substrate 7	SnAg micro bumps, 8 µm Cu UBM
Substrate 8	SnAg micro bumps, 5 µm Ni/1 µm Cu UBM
Substrate 9	SLID, Al removed
Substrate 10	SLID, Al not removed

Some chips on one of the wafers initially bonded without an underfill, were underfilled with Epotek 353 ND after bonding and dicing. A wafer with bonded dies can be seen in Fig. 3. The Au stud bumping of the dies was done by Kulicke&Soffa [21] and the bonding to substrate wafers was done by Datacon [22].

Fig. 3. Dummy MEMS chips flipped and bonded to a substrate wafer with Au stud bumps. No underfill was included.

A cross section of the SnAg microbumps is seen in Fig. 4. A plating base of Ti:W (200 nm) and Cu (300 nm) was sputtered before a thick layer of photo resist was patterned. UBM layers, see Table I, were plated in the resist openings. The SnAg solder material was plated on the die wafers before the resist was removed and the plating base selectively etched. After alignment, the chips were pressed down on to the surface of the substrate wafer without any heating. The chips were held in position by using a small amount of diluted flux. After the complete assembly of the chips on the substrate wafer, the stack was transferred into a batch oven and a standard reflow process for SnAg with inert atmosphere and a peak temperature of 270°C was applied to complete the bonding process. The bump deposition and bonding was done at Fraunhofer IZM [19].

The resist mask used for the substrates to be bonded with SnAg microbumps was also used for the substrates to be bonded with SLID technology, but the plated materials (Cu/Sn-Cu instead of Cu/SnAg-Cu) and the layer thicknesses were different, see Fig. 4. The dies were bonded to the substrate in a special forming gas atmosphere (10% H_2 in N_2) at a bonding temperature of maximum 325°C, applying a tool pressure of about 3 kN. The Al pattern of substrate 9 was etched away during a cleaning process, but the stack was still useful for mechanical tests. The plating of the layers for SLID

was done at Fraunhofer IZM [19]. Assembly of the dummy MEMS dies on a special handling wafer was done by Datacon [22], and the bonding was done by the Munich division of Fraunhofer IZM [23].

The bonded substrates were tested visually, mechanically, and electrically. Cross sections of alignment test structures from all technologies were analyzed with a Quanta 600 FEG scanning electron microscope (SEM) from FEI with EDX. Shear tests were performed using a DAGE 2400 A shear tester. Electrical tests were performed by probing the full daisy chain and by probing single points.

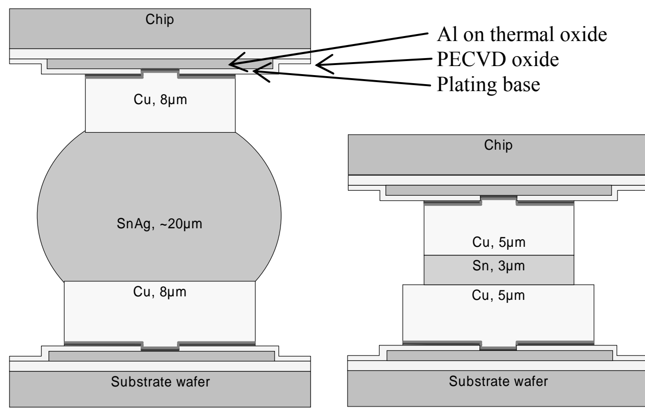

Fig. 4. Left: Bonding with SnAg micro bumps. Right: Bonding with the SLID technology. The thicknesses of the plated layers are indicated.

III. Results and Discussion

A. *Vias*

An overview of the DRIE process development for the 1st generation vias is presented in Fig. 5 with results from the test of the original 100 mm process in the first column and the last process tuning in the 11th column. By comparing profile, selectivity and etch rate for all the process tests, the latter process was deemed to be the most suited for our application. The chosen process was a combination of the recipes used for etching the vias shown in columns 1 and 6.

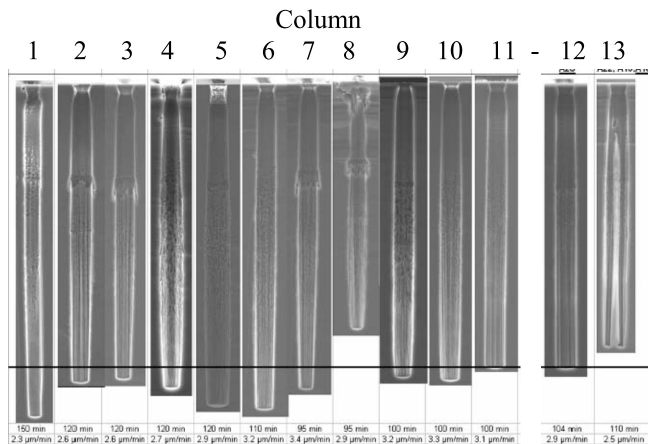

Fig. 5. Overview of the process development of the 1st generation vias (columns 1-11). Columns 12 and 13 show etching results from simulated production runs. The horizontal line marks an etch depth of 300 µm.

The 2nd generation of vias was etched with Al mask, electrostatic clamping and double-side polished wafers with Al on the back side. The choice of Al as masking material limited the possible bias voltage, and the vias resultantly exhibited a diverging shape (15 µm wider at the bottom as compared to the top). The average etch rate for the 20 µm x 50 µm vias was measured to be 3.4 µm/min. Due to the larger open area of the 50 µm x 50 µm vias, their etch rate was higher, exceeding 4 µm/min. A consequence of the different etch rates was an over-etch of approximately 20 min for the largest holes, but since Al was used as stop layer, no notching was observed. The etch uniformity over the wafer was found to be better than 1%. Changing the etch tool from the AMS200SE I-Speeder to an AMS200SE I-Productivity tool increased the etch rate to 14 µm/min and the via opening was nearly identical on the top and bottom of the hole. An image of these vias is shown in Fig. 6.

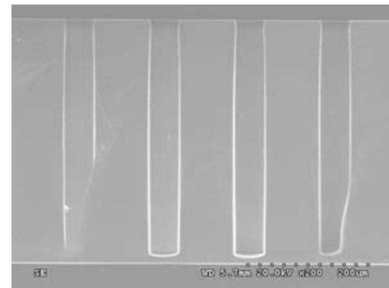

Fig. 6. Etch tests performed using SINTEF's AMS200SE I-Productivity tool from Alcatel for 50 µm x 50 µm vias. The vias are etched almost through a 400 µm thick wafer.

The results from the simulated production runs for the 1st generation vias are shown in Fig. 5 (columns 12 and 13). Only the first three wafers were etched with satisfactory results (column 12), whereas the rest of the wafers were poorly etched (column 13). A reduced wafer-to-wafer etch rate and finally a poor etching result suggested that polymers accumulated in the substrate holder for mechanical clamping during etching of 6 consecutive wafers. Polymers accumulated despite frequent O_2 plasma cleaning. For the simulated production run of the 2nd generation vias using electrostatic clamping, no decrease in etch quality was observed and the wafer-to-wafer uniformity was found to be ~1%. No part of the substrate holder used for electrostatic clamping was shielded from the plasma cleaning, and polymer accumulation was avoided.

Fig. 7 shows a cross-section of a blind via hole after thermal oxidation, polysilicon film deposition and doping. As can be seen in the figure, the polysilicon film showed excellent conformity, even within 300 µm deep via holes with 20 µm or smaller diameters. After removing the phosphor-glass layer, a sheet resistance of 5 Ω/sq was measured.

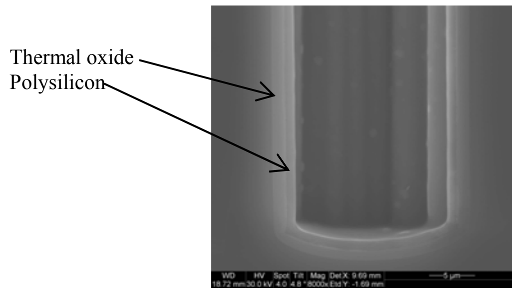

Fig. 7. Conformal coating of a blind via with thermal oxide and polysilicon.

The dry-film resist was unable to withstand wet etching of the conductive layers. There was no significant difference between Al-etch and TMAH. However, the dry etching proved feasible, and six 1st generation wafers and five 2nd generation wafers were successfully etched. A SEM image of an etched wafer is shown in Fig. 8.

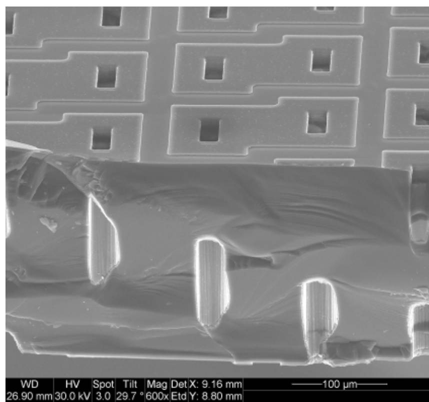

Fig. 8. A cross section of a wafer where the Al routing has been patterned using dry film resist and dry etching on both sides of the wafer. Here, the via pitch was 110 µm.

The electrical resistance per via was 6.5±0.3 Ω for 20 µm x 50 µm holes (748 vias were measured), and 3.8±0.3 Ω for 50 µm x 50 µm holes (488 vias were measured).

B. Interconnection points

Fig. 9 shows SEM images of cross sectioned Au stud bumps with and without underfill, SnAg microbumps and SLID bumps. When no underfill was present, the dicing process smeared out the actual shape of the bumps, but to a lesser extent for the stronger bonds and the harder materials. In general, the SnAg bumps were more regularly shaped than the Au studs bumps and the SLID bonding points, indicating a more stable process.

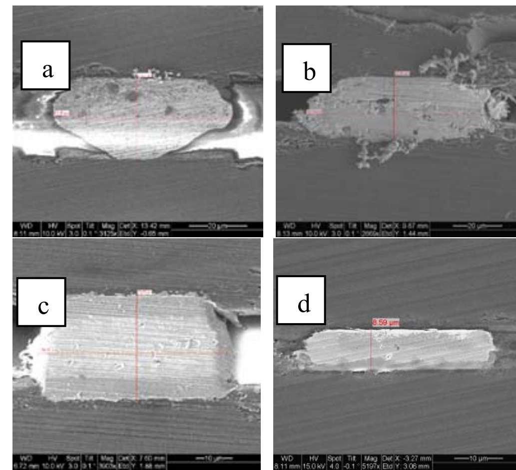

Fig. 9. Cross sections of a) Au stud bump with underfill, b) Au stud bump without underfill, c) SnAg micro bump and d) the SLID technology.

A SnAg micro bump is shown in Fig. 10. The layers were identified by EDX. No large cracks or voids were observed, indicating a reliable bond.

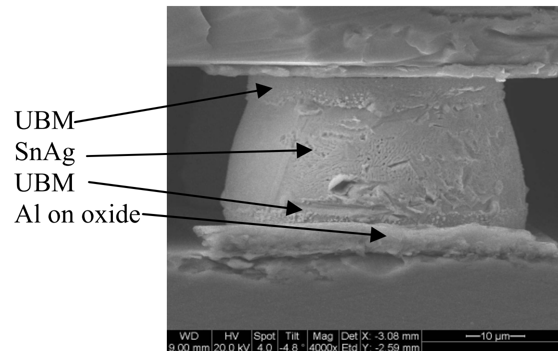

Fig. 10. A SnAg micro bump. The layers were identified by EDX.

The stand-off height was measured and found to be acceptably small for all the tested technologies (<50 µm). A height of ~8 µm was measured on the SLID samples, whereas 25 µm and 30 µm was measured for the Au stud bumps and the SnAg micro bumps, respectively. The height varied 1-2 µm across SLID and SnAg micro bump bonded samples. A height difference of 5-6 µm was measured for the Au stud bump bonded samples and a systematic tilt of 1-2 degrees was observed. The substantial tilt observed for the Au stud bump bonded samples was not satisfactory, since it resulted in a bad bond uniformity. Typically only half of the Au stud bumps were well bonded for each chip.

The results of shear testing of the samples are presented in Table II. The Au stud bump bonded samples with underfill were as expected the strongest ones. However, if only samples without underfill were compared, the SLID bonded samples were the strongest ones and the Au stud bump bonded samples (Substrate 4) the weakest ones. The strength of the Au stud bump bonded samples without underfill was so low that the samples had to be handled with special care in order to avoid fracture. The average strength of the SLID bonds was high,

but the scatter in the results was relatively large which would be typical for a process that potentially could be better controlled. The scatter in the SnAg results was smaller, indicating a well controlled process.

The fracture surfaces were studied for all the technologies after shear testing. The fracture surfaces of the Au stud bump bonded samples and the SLID bonded samples were more irregular than the fracture surfaces for the samples bonded with SnAg micro bumps. The regular fracture surfaces observed for the SnAg bumps were correlated with the small scatter in the measured shear strength values. A typical example of a fractured SnAg bump is seen in Fig. 11. The bond seemed to have fractured inside the PECVD oxide on the Al pad under the bump, indicating a good adhesion between other layers.

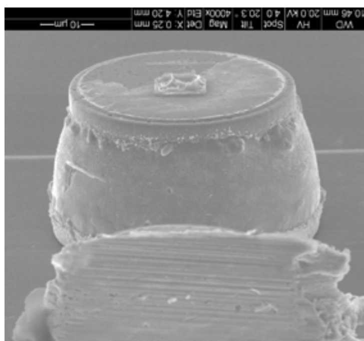

Fig. 11. A broken SnAg bump from substrate wafer 8. The bump had loosened from the sensor chip and the fracture surface could be studied.

The electrical resistance was measured in the full daisy chain and in one single point for chips from all technologies. For the single points, the resistance in the Al routing was dominating when the bonds were good. The smallest resistance measured for a single point from pad to pad was 1.93 Ω.

The electrical resistances of single points measured from pad to pad are compared in Table II. For the Au stud bump bonded chips, the full daisy chain was mainly open, and only the uppermost single point was measurable in most cases. The electrical resistance and the scatter in the results were large (>100%). The results could be explained by the tilt seen for the chips in the SEM and the irregular fracture surfaces seen after the mechanical tests. The values for the electrical resistance on chips bonded with SnAg micro bumps were lower and more repeatable, see Table II. The electrical resistance for single points for the SLID technology was satisfactory, but the scatter in the results would have to be improved for a future application.

Based on SEM inspection, shear testing and measurements of electrical resistances, the use of SnAg micro bumps for chip to wafer bonding seems to be the most promising method for electrical and mechanical interconnection between MEMS and other devices. However, Au stud bumps with underfill and the SLID technology have also proven their feasibility. Au stud bump bonding demands few process steps compared to the other tested technologies. The technology is especially interesting when a small number of interconnection points are needed, since every stud bump is positioned individually. The large strength of the SLID bumps and the small stand-off height are important features for this technology. When choosing a technology for 3D stacking of MEMS, device-specific considerations regarding cost and process complexity must be made.

TABLE II
BOND STRENGTH AND ELECTRICAL RESISTANCE OF SINGLE POINTS

Wafer name	Shear strength (g/bump)	Pad to pad (Ω)
Substrate 3, Au	75.3 ± 12.1	
Substrate 4, Au	2.3 ± 0.7	4.5 ± 6.1
Substrate 5, Au	141.5 ± 10.0	3.7 ± 4.5
Substrate 6, SnAg	4.8 ± 0.3	1.99 ± 0.04
Substrate 7, SnAg	4.7 ± 0.2	
Substrate 8, SnAg	4.9 ± 0.3	2.08 ± 0.05
Substrate 9, SLID	7.4 ± 2.2	
Substrate 10, SLID		2.7 ± 1.1

IV. CONCLUSION

Vias through 300 µm thick wafers with 6.5±0.3 Ω resistance were realized with a pitch of 110 µm. The dimensions of the via holes were 20 µm x 50 µm, which proved to be large enough for reliable dry etching of large volumes of 150 mm wafers and reliable dry film patterning and dry etching of the Al routing.

Three technologies were tested for electrical and mechanical interconnection between 3D stacked chips. The best results were achieved for the SnAg micro bumps, whereas Au stud bump bonding and the SLID technology proved to have individual advantages as well. The bond strength of the SnAg bumps was large enough (>4.5 g/bump) for normal handling without using any underfill and the electrical resistance of the bumps was small; a pad to pad resistance of ~2 Ω was measured and the value was dominated by the resistance in the routing metal. More work is ongoing in order to verify the reliability of the three technologies.

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