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Switching Performance Assessment of a 1.2 kV, 300 A, 175 °C All-SiC Half-Bridge Module Using Computer Tools

Investigation of the Impact of Internal Stray Inductance on Switching Behavior

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ABSTRACT

One of the most attractive attributes of SiC MOSFETs is the fast switching capability. This capability can enable high-power converters with a power-density not currently possible with the Si IGBT technology. However, to unfold this capability, a more thorough attention to parasitic inductances is required. This thesis investigates the limitations of what is considered state-of-the-art in high-power SiC MOSFET module design today. The main contributors to internal module parasitic inductances and the impact the power loop inductance has on switching performance are studied. The entire investigation is conducted by using computer tools.

A mechanical model of an all-SiC half-bridge module emulating a commercial available SiC MOSFET module from Cree has been developed and realized in SolidWorks. The rating of the developed module is 1.2 kV, 300 A, 175 °C. ANSYS Q3D was used to extract the parasitic inductances of the developed module. A test-circuit, rated at 800 V, 150 A, employing the extracted parasitic inductances and the device models (supplied by Cree) was used to assess the performance.

The investigation revealed that the bulky power terminals and the large DBC substrate area are the main contributors to internal inductances (tens of nanohenries). The impact of the parasitic inductances on switching performance was device voltage overshoots and ringing in device waveforms. The investigation suggests that the most viable measure to reducing the internal module inductances is to design the power terminals in a strip-line manner to utilize mutual flux cancelling effects. This investigation also validates the use of computer tools for investigating module designs, as well as being a valuable aid in studying the performance of SiC MOSFET modules.

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CHAPTER 1 INTRODUCTION

1.1 BACKGROUND

One of the strongest growing market areas for power electronics is in the transportation sector (i.e. rail, road, air and marine). The electrification of the transportation sector is recognized as being one of the most viable solutions to the growing climate concern, as this sector is responsible for about 25 % of total global greenhouse gas emissions [1]. For the electrification of this sector to succeed, stringent demands of power electronic systems in terms of cost, size, weight, power-density and reliability must be met. This is where the emerging wide bandgap (WBG) semiconductor materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), for the use in power electronic devices are expected to be a game changer, meeting most of these conflicting requirements simultaneously [2] [3]. Nowadays, the electric power conversion systems in transportation applications are often realized using power modules employing high-power Si IGBT devices, and the established power module technology is largely designed per Si IGBT capabilities.

SiC MOSFETs are expected to enter the market areas currently ruled by these Si IGBTs, providing both the benefit of the SiC material and the MOSFET capabilities. The most appealing consequences of displacing Si IGBTs with SiC MOSFETs are the possibility of attaining very high switching speeds and high junction temperatures. Exploiting the fast switching capabilities of SiC MOSFETs can downsize the size of passive components and reduce device transition times, and the high-temperature capability can relax the cooling requirements. This yields the prospect of developing high-power modules with a power-density not currently feasible with the conventional Si IGBT technology. However, commercial high-power SiC MOSFET modules are today most often designed in a similar fashion to Si IGBT modules, indicating that the switching frequency is usually limited to below 20 kHz and the maximum junction temperature restricted to 150 °C.

The internal module parasitic inductances hamper the switching capabilities of power switches by inducing voltage overshoots and provoking oscillations in device waveforms. Consequently, the superior capabilities of SiC MOSFETs are not fully exploited when they are treated as drop-in Si IGBT replacements. To make the appropriate measures, the main contributors to these parasitic inductances must be identified. This study will investigate which parts/elements of the conventional SiC half-bridge module that contribute the most to the

internal parasitic inductances, as well as investigating the impact it has on device switching behavior.

1.2 Research Objective and Motivation

The work aims at developing a mechanical model of a high-power SiC MOSFET module which emulates a commercial available half-bridge module from Cree. The Cree module is named CAS300M12BM2 and is rated at 1.2 kV, 300 A and 150 °C. Thus, the investigation will also give an insight into the mechanical design of what is considered state-of-the-art in SiC MOSFET module design today. The parasitic inductances of the developed will be extracted and incorporated into a test circuit to investigate the impact on the switching behavior. The geometry will be realized in SolidWorks and evaluated in ANSYS Q3D and LTSpice. To extend the scope of work, the developed module is also intended to be able to operate at a higher junction temperature than the real Cree module. Thus, a literature survey on the recent advances in high-temperature packaging is conducted and provided for the reader.

The entire investigation is conducted using computer tools. The usage of computer tools is increasingly being employed by manufacturers and researchers today, as specific modeling and simulation tools are becoming more accurate. Virtual fabrication, experimentation and tests by computer simulations have the latest decades become an integral part of the design methodology for power electronic devices and systems, enabling cost-efficient and time-saving development cycles [4] [5]. There are a lot of papers in the literature that support the convenience of using computer tools when testing new ideas and evaluating existing power module designs. For instance, in [6] a tear-down of a commercial available three-phase module from Cree was conducted to obtain accurate internal dimensions to accurately realize the mechanical design in a computer software. The developed module geometry was then analyzed to evaluate the electrical and thermal performance. The results complied very well with the values provided in the datasheets. In [7] [8], the use of computer aided design (CAD) tools and finite element analysis (FEA) were extensively used to investigate and validate new design approaches to common wire-bonded SiC MOSFET modules.

Attaining knowledge of the merits and the limitations in the design of commercial available SiC MOSFET modules was the main motivation for conducting this study. In

addition, as computer knowledge is an important attribute for engineers, learning various computer tools was also a big motivation for conducting this investigation.

1.3 Organization of the Report

In order to develop a realistic and accurate mechanical model of the SiC MOSFET half-bridge module and to assigning apposite materials, a thorough insight into packaging approaches is required. To give the reader the required background knowledge and a basis for interpreting the outcomings of the investigation, the thesis is organized as follows.

Chapter 2 introduces wide bandgap semiconductor materials and illuminates why Silicon Carbide is an enabling material for power electronics. Furthermore, it discusses the prospect of achieving very high power-density systems by using SiC MOSFETs for applications in the transportation sector, as well as highlighting the main impediments in achieving it.

In Chapter 3 a literature review of packaging approaches and trends is provided. The chapter has special emphasis on thermal management and the inductive design of power modules. New materials for substrates, new materials and technologies for interconnects, as well as high-temperature encapsulants are the main discussion points. The theory and conclusions drawn in Chapter 3 forms the basis for the succeeding chapters.

In Chapter 4 the development of a 1.2 kV, 300 A, 175 °C half-bridge module is presented. Based on the previous chapter, appropriate materials are selected and the mechanical geometry is determined. The mechanical model is realized SolidWorks. The realized model is then analyzed in ANSYS Q3D for extracting the parasitic inductances.

In Chapter 5 the developed half-bridge module is evaluated in LTSpice. A downscaled test circuit of 800 V, 150 A is used to assess the performance in terms of switching behavior. Current- and voltage overshoots, ringing in signal waveforms and energy losses are discussed.

Finally, Chapter 6 summarizes the main conclusions of the study and proposes suggestions for future work.

CHAPTER 2 WIDE BANDGAP SEMICONDUCTOR MATERIALS

The fundamental industry that power electronics has evolved to become today can largely be attributed to the innovations of sophisticated power devices, e.g. power MOSFETs and IGBTs, and innovations like digital signal processing occurring throughout the 70's and 80's. Later, the development of superjunction MOSFETs and Trench and Field-Stop IGBTs further raised the convenience and aided in widespread acceptance and usage of power electronic systems [9]. Power electronics is a multidisciplinary field, but the core technology behind power electronics is the power semiconductor, enabling efficient control and tuning of electric power. The most common semiconductor material in power semiconductor devices today is Silicon (Si). The mature and well-researched Si technology has largely drained the performance of present state-of-the-art devices over the years, making innovations in the Si technology very hard to accomplish. The recent breakthrough in the fabrication of devices based on so-called wide bandgap (WBG) semiconductor materials has established a new benchmark for power devices. WBG semiconductor materials such as Silicon Carbide (SiC), Gallium Nitride (GaN) and Gallium Arsenide (GaAs) enable power devices with higher power-density and efficiency, as well as increased reliability. These merits are considered key enablers for emerging applications such as all-electric (EV) and hybrid electric vehicles (HEV), energy storage systems and more-electric aircrafts. It can also help integrate renewables onto the main grid and lead to vast energy savings in various industrial processes and home appliances. All of which considered key for alleviating the growing climate concern of today.

At present, GaN and SiC are the most suitable WBG materials for power electronic devices as they give the best trade-off between theoretical material properties, availability of high-quality wafers and maturity in the processing technology. The GaN properties are slightly superior to SiC, but the fabrication process of high-quality and low-cost bulk GaN wafers proves difficult, hence only lateral GaN transistors are available today. This rules out GaN-based devices in the high voltage range as this range requires a vertical structure with a thick epilayer. However, GaN is a very attractive material for very high frequency applications due to the direct band gap (lower carrier lifetimes), and is therefore a very promising material for radio frequency applications, optoelectronics, as well as in the solid-state lighting industry. Accordingly, for high-power applications SiC-based power devices are expected to rule over

GaN-devices. Compared to standard Si, SiC has almost ten times higher breakdown field and three times the bandgap, enabling higher efficiency and reliability. In combination, this makes SiC a very attractive material in high-power applications. Furthermore, SiC exhibits a high saturation drift velocity and high thermal conductivity, which is very compatible with high switching speeds [10]. The relevant properties of Si, SiC and other attractive WBG materials are tabulated below.

Table 1: Properties of Silicon and attractive wide bandgap materials at room temperature

Properties	Si	(4H) SiC	GaAs	GaN
Crystal Structure	*Diamond*	*Hexagonal*	*Zincblende*	*Hexagonal*
Energy Bandgap [eV]	*1.12*	*3.26*	*1.43*	*3.5*
Electron Mobility $[cm^2/Vs]$	*1400*	*900*	*8500*	*1250*
Hole Mobility $[cm^2/Vs]$	*600*	*100*	*400*	*200*
Breakdown Field $[MV/cm]$	*0.3*	*3.0*	*0.4*	*3.0*
Thermal Conductivity $[W/cm°C]$	*1.5*	*4.9*	*0.5*	*1.3*
Saturation Velocity $[1e7cm/s]$	*1.0*	*2.7*	*2.0*	*2.7*

The ability of SiC devices to operate at very high switching speeds and junction temperatures can have tremendous system benefits, i.e. reduced costs, weight and size. This makes SiC an enabling material for an abundance of applications. However, SiC is particularly fitting for applications where a high power-density is one of the main design targets, such as in transportation applications. Increasing the switching speed helps reduce the size and weight of passive components (inductors, capacitors, etc.), which usually accounts for 30-40 % of the total size in common high-power electronic systems, as well as downsizing filters and transformers. Increasing the temperature durability can severely relax the cooling requirements in converters. Powerful unipolar devices are expected to bring about these merits. SiC MOSFETs, SiC JFETs and SiC SBD diodes have all penetrated the market the latest years and are now becoming an established technology enabling power electronic systems with very high efficiency and power-density. The normally-off behavior and ease of control of MOSFETs make them the preferred choice amongst available SiC devices today. In addition, the well-known Si MOSFET technology also supports the convenience of the SiC MOSFET technology.

2.1 SiC MOSFETs for High Power-Density Converters

The intrinsic properties of SiC enable MOSFETs to enter the medium voltage range (i.e. 1.2 kV – 3.3 kV) currently dominated by Si IGBTs. The conductivity modulation utilized in IGBTs enable them to have very attractive on-state characteristic, however, with the penalty of reduced switching speed capabilities due to the need to remove excess charge during switching transitions. Si MOSFETs are mainly utilized in high frequency, low voltage applications (< 300 V), such as in switch-mode power supplies, due to their fast rising on-state resistance with higher voltages. Thus, enabling MOSFET to operate in the medium voltage range can be a real game changer. Although very much praised, the SiC MOSFET technology is by no means immaculate. Earlier, SiC MOSFETs suffered strongly from functional failures and characteristic shifts during bias and temperature stresses due to a high density of defects located in the epilayer, the gate oxide and the interface S_iO_2/SiC, preventing them from entering the market. The first commercialization occurred as late as 2011, with Cree presenting the first SiC MOSFET, rated at 1.2 kV and 30 A.

It is therefore interesting to investigate the performance of recent-day SiC MOSFET dies at higher temperatures than the usual rating of SiC MOSFET modules today (150 °C) to see if high-temperature operation is feasible with current-day technology. In addition, to facilitate fast switching it is important to identify the impact of parasitic inductances on switching behavior.

2.1.1 High-temperature durability of SiC MOSFET dies

Operation at much elevated chip temperatures becomes feasible due to the wide bandgap and high thermal conductivity. The wide bandgap indicates that more energy (acquired as heat or light) must be present to produce mobile charge carriers within the semiconductor, and the high thermal conductivity aids in heat removal. Consequently, power converters employing SiC MOSFETs are anticipated to be able to operate in much harsher environments with higher current densities than if Si IGBTs were employed.

There are heaps of studies showing the superior dynamic and static characteristics of 1.2 kV SiC MOSFETs over 1.2 kV Si MOSFETs, 900 SJ MOSFETs and 1.2 kV Si IGBTs. But these studies are mostly conducted at junction temperatures as per Si capabilities. There are surprisingly little studies on the performance of commercial available SiC MOSFETs at very high temperatures (well beyond 150 °C) in the literature, but the studies that were obtained had

some very interesting remarks. In [11], the authors tested and compared the second generation SiC MOSFET dies with comparable SiC JFETs on how performance degraded with junction temperatures up to 350 ºC. It was concluded that both devices could be safely operated up to 300 ºC, however, the SiC MOSFETs showed a significant increase in leakage current, indicating that SiC JFETs were more suitable for high-temperature operation at the time (2007). The authors highlighted that the significant performance degradation of the SiC MOSFET was due to the feeble gate oxide layer.

In [12], a comprehensive performance characterization of the latest generation commercial available 1.2 kV SiC MOSFET dies from Cree, ROHM and GE for junction temperatures up to 200 ºC were conducted. The results were then compared to the results from a similar study on earlier generations. The investigated parameters included threshold voltage, specific on-state resistance, junction capacitances, leakage currents and switching energy losses. This study revealed that the latest generations showed improved high-temperature performance with a less temperature-dependent on-state resistance, lower leakage currents and negligible changes in the total switching losses with temperature compared to earlier generations.

In [13], the authors tested the DC characteristics of a commercialized TO-258 packaged SiC MOSFET for case temperatures ranging from -187 to 300 ºC. They concluded that the on-state resistance reduced for temperatures up to 100 ºC, which could be attributed to the channel resistance (negative temperature coefficient) being the most dominant for this specific device at RT (V_{GS} = 15 V). However, this effect became somewhat cancelled out by scattering effects, such as Coulomb and/or phonon scattering, when the case temperature increased beyond 100 ºC. A slight increase in $R_{DS,on}$ were observed when the temperature further was increased, as the residual resistances increasingly became more dominant (positive temperature coefficient). When the case temperature increased beyond 250 ºC, a significant increase in overall resistance were observed, which could be attributed to the very much reduced channel and residual mobility for such high temperature. These observations were largely supported by the work in [14], where several commercial dies rated at 1200 V, 30 A were tested up to 350 ºC, showing a 7±1 increase in resistance going from RT to 350ºC. However, the main issue reported when targeting operation well above 150 ºC is the threshold voltage drift. Albeit, these concerns have been somewhat suppressed in the latest generations owing to more optimal S_iO_2/SiC growth conditions. It was showed in [14] that a positive bias temperature stress (V_{GS} = 20 V at 300 ºC

for 30 min) induced a quite large positive shift in threshold voltage (ranging from 1 to 2 V) in some of the dies, but it had little impact on drain current. Of more concern was the drift in threshold voltage under negative bias temperature stress (V_{GS} = -5 V at 300 ºC for 30 min). Some of the dies were approaching a threshold voltage of only 0.5 V during the test. Owing to the negative temperature-dependence of the threshold voltage, and the negative drift under negative bias, devices with an already inherently low threshold voltage at room temperature represent a major concern when targeting high-temperature operation. Even though the stress-induced drifts can be largely suppressed by reducing the gate turn-off voltage, the negative temperature-dependence pose a concern (also a risk for parasitic turn-on due to any cross-talk or other noise). De-rating and paralleling of devices might be the solution to relax the concern at the time being.

The SiC technology is clearly under development and studies indicate that present-day SiC MOSFET dies can safely operate in real applications at temperature far exceeding their common rating of today. It is ostensibly not the dies that is constraining high-temperature operation of SiC MOSFET modules, the package and module design is.

2.1.2 THE IMPACT OF STRAY INDUCTANCE ON SIC MOSFET SWITCHING BEHAVIOR

As mentioned, to cash in on the high-temperature capabilities of SiC devices, a new take on thermal management within packages and modules are required. The same goes for exploiting the fast switching capabilities of these devices. While it is largely the charge and discharge cycles of the inherent device parasitic capacitances that determine the inherent SiC MOSFETs switching speed capability, practically it is the system circuit parasitics that determine how fast the devices can transit between states. The possibility of attaining very fast switching speed by replacing Si IGBTs with SiC MOSFETs requires advanced package designs to limit the internal package parasitic electric elements. These parasitics include inductances and capacitances. The parasitic capacitances within modules mainly originate from the active switches (fixed). The parasitic inductances originate from the electro-mechanical structure of the module. The main parasitics inside a module are depicted in Fig. 1.

As inductance is only defined for a closed contour, the various inductances contributing to restricting the attainable switching speed can be represented by a set of lumped parameters representing the main current paths; namely the commutation path inductance L_{σ}, the common source inductance $L_{S,}$ and the gate path inductance L_G.

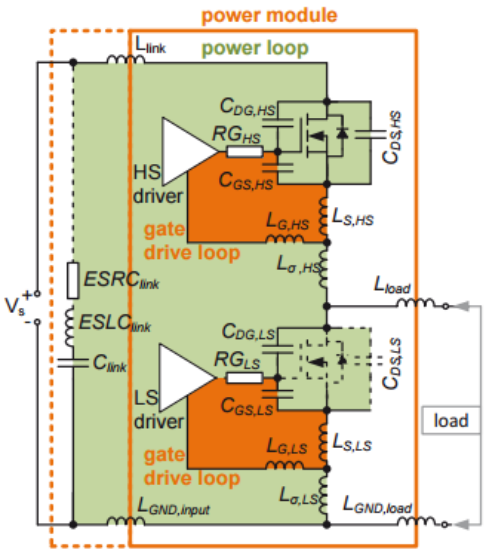

Figure 1: Equivalent circuit of a half-bridge circuit showing the main parasitic elements *[15]*

The module interior commutation path inductance L_σ originates from the source bond wires, DBC traces and power terminals, making up the power current path. This inductance prevents fast current transitions by causing overvoltages during turn-off and it also tends to resonate with the MOSFET output capacitance and diode junction capacitance causing oscillations in the transistor waveform. These oscillations can also cause ringing in the gate waveforms through the Miller capacitance. This inductance can be effectively reduced by reducing the power loop area.

The common source inductance L_S is the inductance that shares parts of the source gate path as well as of the source power path, and appears if the wires on the source pads of the dies are not separated for gate and source current [15]. This inductance acts as a device voltage slew rate reducer and supporter of parasitic turn-on (negative feedback to the gate drive). During turn-on, the inductance reduces the effective gate voltage, while during turn-off it increases the effective gate voltage. This inductance can be effectively reduced to negligible values if the source wire for the power current and gate current are separated.

The gate path inductance L_G comes from the gate and source wire bonds, the gate copper traces and the gate module connectors. The gate drive inductance limits the switching speed by slowing down the gate drive current. In addition, this inductance tends to resonate with the device input capacitance causing oscillations in gate waveforms which can provoke parasitic

switching. Keeping the gate traces short and making sure of proper layout are effective measures to reduce its impact on device switching behavior.

These parasitic inductances contribute, to various extents, to signal overshoots and oscillations in waveforms, which in turn may hamper the switching speed and performance, as well as to increasing the switching energy losses. Several strategies for achieving low-inductive power modules has been presented in the literature. The most viable strategies are given below. Manufacturers of SiC-modules are already addressing several of these strategies.

1. Separation of the power and gate source wire contacts to reduce the common source inductance.
2. Strip-line design of power terminals to utilize mutual inductance cancelling effects. In addition, the terminals should be short and wide to reduce parasitic self-inductances.
3. Implementing internal decoupling capacitors to reduce the power loop area.
4. Low-profile modules

CHAPTER 3 TRENDS IN PACKAGING DESIGN – NEW TECHNOLOGIES AND MATERIALS

Power electronic modules led to tremendous system advantages once it was first introduced in 1975 (by Semikron). Earlier, discrete devices were clamped/screwed to individual heat sinks which had to be isolated from each other. With dedicated assemblies, several chips could be mounted on the same heat sink and electrically connected with bus arrangements, yielding a much more compact, less costly and more reliable power electronic system. The power module market has been growing fast ever since it was first introduced, and the main applications nowadays are in motor drives, traction, renewable energies and automotive [16]. Power modules in EV/HEV applications constituted 30 % of the overall power module market in 2015, and is anticipated to increase to 50 % by 2021 [17]. In Fig. 2, a cross section of a modern day, high-power package design is shown. The conventional design mainly relies on aluminum (Al) wires interconnecting the topside of the chips and the substrate, a direct-bonded-copper (DBC) substrate for selective current conduction and a copper (Cu) baseplate for heat-spreading.

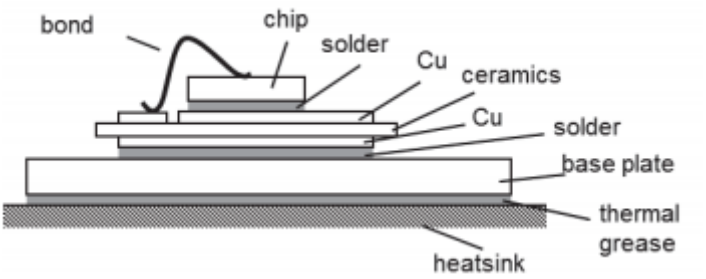

Figure 2: Cross section of a conventional package design [16]

As mentioned, the main worth in SiC lays in the high-temperature and fast-switching capabilities. SiC-based modules must support at least 175 °C, and in due course 250 °C, to offset the high cost of SiC [18]. Such technologies are not currently present in the Si technology. The same goes for higher switching frequencies. The inductive layout in conventional modules are not fit to properly unfold this extremely attractive property of SiC. These challenges have spurred a growing research in high-temperature packaging and low-inductive designs for the

next generation SiC module technology. This section is devoted to the trends in module design technologies specific to SiC to unfold is capabilities. This investigation forms the basis for the module development to come.

3.1 NEW METALLIZED SUBSTRATE MATERIALS

The substrate serves as the supporting structure for the circuitry of power modules and must have properties able to withstand very harsh environmental stresses [19]. It must isolate the various conductive parts of the internal circuit, as well as aid in removal of heat generated by the components. Ceramics are widely used, but also glass, sapphire, quarts and Silicon-based substrates are used. The materials best suited for high-power applications are tabulated below. These materials are ceramics - alumina (Al_2O_3), aluminum nitride (AlN), and beryllia (BeO) - and a silicon-based material - silicon nitride (Si_3N_4).

Table 2: Attractive materials in substrates

Materials	**Thermal conductivity (W/m ◦K)**	**CTE* (ppm/K)**	**Dielectric strength (kV/mm)**	**Flexural strength (mPa)**
Ceramics				
Al_2O_3(99%)	33	7.2	12	345
AlN	150-180	4.6	15	360
BeO	270	7.0	12	250
Si-based				
Si_3N_4	70	3.0	10	932

**Coefficient of Thermal Expansion (SiC=3.7)*

Al_2O_3 is very mature and the cheapest solution, but have a very poor thermal conductivity and average mechanical strength and are thus not the best alternative for high power-density modules. BeO has the highest thermal conductivity, but represent a health hazard in its dust particle form making it unattractive for any application. Si_3N_4, the newest material of these alternatives, have excellent mechanical strength and are therefore very attractive for stand-alone substrates. It does also have a CTE closest to that of SiC, but the high cost and somewhat inferior thermal capabilities make it impractical. AlN seems like the best choice as

it proposes the best trade-off between cost and performance (it also has a CTE close to that of SiC). The good thermal properties and high dielectric strength makes it a very attractive solution, albeit a metal base plate would be needed due to the average mechanical strength.

The metallization deposited on the substrate forms the conductive paths of the module. Direct-Bonded-Copper (DBC) substrates has been widely used in high-power applications owing to the high current-capability, high heat dissipation, flexible patterning and high reliability. Although very much used, the Cu layer in DBC substrates are prone to peel-off due to CTE mismatch between the Cu and the substrate. This has, however, largely been suppressed by using sealed step-edges (decreased thickness at edges, coated with a polymer). For really high temperatures, sintered thick film silver metallization on alumina and Direct Bonded Aluminum (DBA) on AlN substrate show promising performance [20].

3.2 SOLDERLESS MODULES

The die attach forms a very important interface between the chip and the substrate. The joint must assure that a variety of different characteristics are fulfilled to ensure that the module is a mechanically reliable and a thermal efficient system. Proper adhesion to both chip and substrate, high resilience, high thermal conductivity, a CTE matching the chip and good electric properties to conduct the necessary current are the main features needed of the die attach. This puts strict requirements on the die attach bonding process and the material, even more so when targeting to employ SiC MOSFETs. The bonding of the drain side of MOSFETs and cathode side of diodes to the substrate is today usually performed with a soft soldering process. The standard solder alloy used nowadays is the eutectic tin-lead (Sn-Pb) alloy. Tin (Sn) and lead (Pb) has a melting temperature of 323 °C and 232 °C, respectively, but their alloys have lower melting points (minimum 183 °C for 63Sn-37Pb). This results in an inadequate homologous temperature for the next generation SiC modules. Also, in high-temperature electronics, a safety margin is needed as the performance of die attach material naturally degrades with increasing temperature. However, as the lead-content increases, so does the eutectic temperature. Common Pb-rich solders (95Pb-5Sn and 90Pb-10Sn) have liquidus temperatures exceeding 300 °C, but the recognition of the harmful effects of Pb on environmental and human well-being has boosted the effort in developing Pb-free solders [21]. Solder alloys with a high content of gold (Au) have very attractive thermal performance, but the mechanical performance prove

somewhat restricted compared to other alternatives. The high cost of Au-based solders is also a limitation. Conductive epoxies are also widely used, however, mainly in low-power modules. The most interesting die attach material is silver. Silver is an excellent thermal and electrical conductor and has very good mechanical properties. More importantly, silver can sustain much higher temperatures than solders (melting temperatures over 900 °C) and, being a single-phase material, better mechanical property and reliability is anticipated. In addition, the bottom finish of dies is usually silver to aid wetting during soldering [22]. This facilitate the use of silver as die attach. However, the high melting temperature of the noble metals also represent a technical challenge as the reflow technique used for solders cannot be utilized because no device can bear such a high temperature.

The most promising die attach techniques to utilize noble materials include the Low Temperature Joining Technique (LTJT), also known as sintering, and the Transient Liquid Phase Bonding (TLPB). Sintering has emerged as a very promising technique as it allows joining at temperatures well below the melting temperature of the noble metals. Thus, the joint can be formed at relatively low temperatures, but work at high temperatures. Because there is no liquidation involved during bonding, more precise joining is also possible with the sintering approach. In LTJT, a metal (silver) is mixed with organic materials to form a paste. Further, the paste is printed on the substrate and the die is placed on the paste. By utilizing silver particles in the nanometer scale and external pressure, a sintering process at a much lower temperature is possible. This technology allows chip temperatures well above 300 °C without degradation and the typical thermal conductivity of the sintered joint is about fivefold higher than conventional solders [23]. The disadvantages of this approach are the relatively high cost and the difficulty in automating the manufacturing process as external pressure needs to be applied. However, power modules based on the sintering technique are nowadays in mass production [24].

In the second technique, the TLPB technique, a thin layer of a low-melting point material (interlayer) is placed between two thicker solid materials (baselayers). Indium and tin (and their alloys) are common interlayer materials, while silver is utilized as the base metal [25]. As the interlayer melts and diffuses into the base layer, isothermal solidification occurs. Once the interlayer is diffused into the base, one new homogeneous solid material remains which has a higher melting point than of the original interlayer. To utilize TLPB as a die attach bond, the base and interlayer materials are deposited onto two different materials (i.e. substrate

and die), and then compressed and heated. Advantages of this approach include high melting-temperature (covers full range of SiC temperature capability) and the fact that the bonding can be executed at relative low temperatures (range of 200 °C) shielding other parts from excessive temperatures. In addition, it can be made very thin, resulting in negligible thermal impedance. However, due to process complexity and high cost, manufacturers are still somewhat reluctant to embrace the TLPB approach [26] [27].

3.3 NEW INTERCONNECT TECHNOLOGIES

In electronic packaging, interconnecting the topside of the chips and the substrate electrically is usually accomplished by heavy (>4 mil) aluminum alloy wires or fine (< 4 mil) high purity gold wires. The wire-bond technology can be divided into two types depending on how the bonds are made, namely ball-wedge and wedge-wedge bonding. The former utilizes a thermosonic technique and capillary tool to accomplish a very fast process (up to 22 wires/second) and usually finds its use in microelectronics. In power electronic packaging, the most common bonding process is the wedge-wedge bonding, utilizing heavy Al alloy wires to interconnect the source/anode pads to the substrate/other chips. The two different bonding methods are depicted in Fig. 3.

In ball-wedge bonding, gold wires are most common, whereas aluminum alloys are commonly used in wedge-wedge bonds. The Al wire-bonds are considered the weakest link in common high-power Si IGBTs power modules, where mainly two kinds of failures are reported: heel cracking (due to thermal expansion or wire deformation) and wire-bond lift-offs (due to material fatigue and CTE mismatch between wire and chip). These failures are commonly named bond wire fatigue, initiated by mechanical stress induced by material thermal expansions. The elevated junction temperatures and thus wider temperature excursions expected in high-power SiC modules obviously requires a new bonding approach to avoid the reliability issues already present in the Si technology.

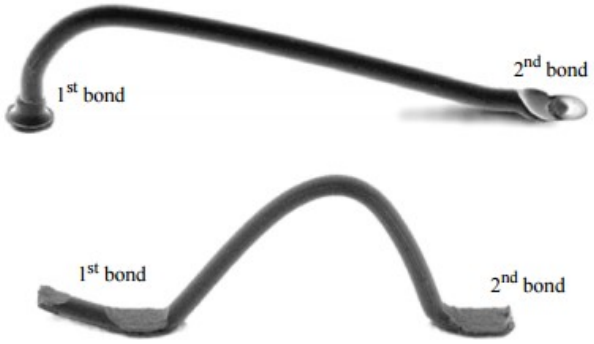

Figure 3: Side view of ball-wedge bonding (top) and wedge-wedge bonding (bottom) [12]

Copper (Cu) wires have emerged as a very attractive alternative to the traditional aluminum and gold wires, providing superior mechanical, electrical and thermal performance. In addition, the thinner Cu wires are favorable for present-day SiC chips (small chip source area limits the bond pad area for interconnects). In addition, both ball and wedge bonding is possible with Cu wires. However, implementing Cu wires also have its challenges. The higher hardness of Cu wires requires higher bonding force and ultrasonic power, which can lead to cratering for ball bonding and tearing for wedge bonding [16]. As Cu readily oxidizes, an inert bonding atmosphere is also needed. In addition, ultrasonic bonding of Cu wires favors a Cu metallization on the front side of the chips (like the Bond Buffer developed by Danfoss) as the bond strength of Cu-Al significantly reduces when the junction temperature exceeds 200 °C due to strong intermetallic growth.

The trend of Cu wires can be merely seen as an intermediate step towards high-temperature packages. The obvious limitations of the wire-bond technology have promoted research of alternative technologies to accommodate the higher performance demand of SiC modules. Displacing the wires with new interconnects that provide increased contact area, reduced parasitics and high temperature durability are considered the ultimate objective of new topside interconnections [28]. Planar area interconnects have emerged as one of the most promising new interconnect technologies, and is especially suited for high power-density applications. In this approach the wires are replaced with large area leadframes, DBC substrates or flex foils providing selective traces which are bonded to the topside of the dies. Several planar packaging technologies has been proposed to replace the wire bonds such as the Metal

Post Interconnected Parallel Plate Structure [29], the Flip-Chip Technology on flexible foils/leadframes using solder bumps [30], the Embedded Power concept [31]. In Fig. 4, the structure of a 1200V/200A half-bridge module utilizing one of the novel concepts is shown. In this half-bridge structure the dies are enclosed between two DBC substrates and arranged in a face-up/face-down manner to provide the required current paths [32]. The reduced loop area, larger bonding area and wider conductive traces significantly reduces the parasitic loop inductances and resistances.

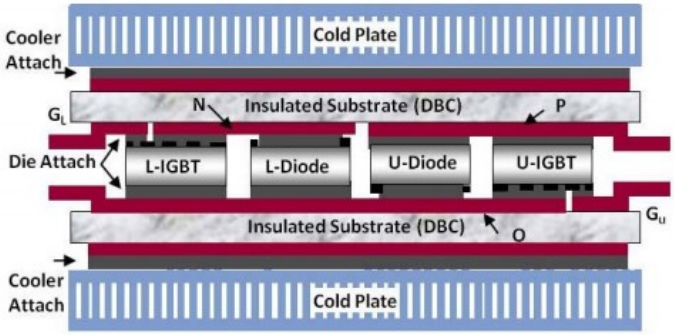

Figure 4: Planar bond packaging technology [27]

In 2011 Semikron launched their new concept called the "SkiN"-technology, where any solder has been replaced with sinters and the wire-bonds replaced by flexible circuit boards, as depicted in Fig. 5.

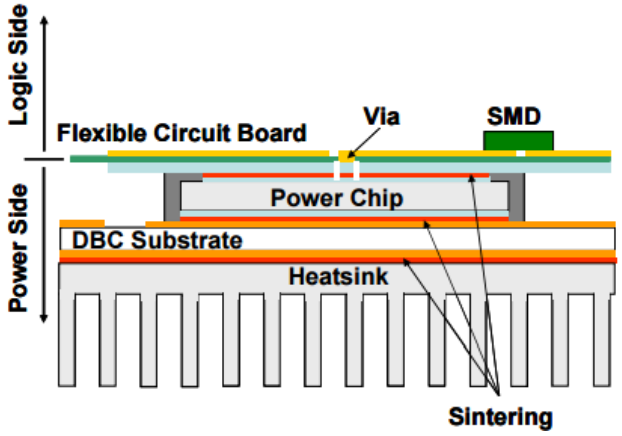

Figure 5: Schematic cross section of the SKiN technology [20]

The “flex board” is a polyimide with patterned metal tracks on both sides. The bottom “power side” of the flex board exhibits a thick metal able to carry the load current, whereas the top metal “logic side” carries the control, gate and auxiliary signals. For the gate circuit to reach the gate pad on the die the polyimide layer has an opening allowing the necessary contact, as can be seen in Fig. 5.

These “3D”-like structures allow reduced electrical parasitics compared to the conventional “2D” structures, with an additional feature of double-sided cooling. However, these structures are still not widely utilized due to manufacture issues (such as double-sided die joining capability) and lack of long term reliability validation under either thermal soaking or cycling conditions, making the wire-bond technology still the most viable today.

3.4 HIGH-TEMPERATURE ENCAPSULANTS

Polymeric soft encapsulants has been the main solution in electronic packaging for protecting the internal components from hostile environmental such as moisture, solvents and gases. In addition, the encapsulant is to provide added insulation protection between wires and traces. Silica gel is widely used in standard Si modules, however, when targeting operation with temperature well above 150 °C, new materials are needed. There are two attractive alternatives addressed in the literature, namely hydroset ceramics and polymers. However, tests show that the hard materials (hydroset ceramics and epoxies) have issues related to cracking during large power cycles [33]. Silicon elastomers seems to offer a compromise between hardness and thermal stability and have been successfully tested up to 250 °C [34] [35].

The lack of convenient encapsulation materials is considered a huge problem when targeting the future high-performance SiC modules. New module designs are anticipated to be needed to alleviate this concern.

CHAPTER 4 DEVELOPMENT AND ANALYSIS OF A 1.2 KV, 300 A, 175 °C HALF-BRIDGE MODULE

A half-bridge module rated at 1.2 kV, 300 A, 175 °C has been developed. The chips implemented are the commercial available SiC MOSFET (CPM2-1200-0040B) from Cree, rated at 46 A at 175 °C, and SiC Schottky Barrier Diode (CPW5-1200-Z050B) from Cree, which is rated at 50 A at 175 °C. Therefore, to achieve the current rating, a total number of 8 MOSFETs and 6 Schottky diodes in parallel per switch position are needed. The SiC chips, as depicted in Fig. 6, are modeled with exact dimensions as per their datasheet. The developed module emulates the commercial available 1.2 kV, 300 A, 150 °C Cree module named CAS300M12BM2, but with some design and material modifications to make way for operation at 175 °C. A different gate circuit design is also implemented to reduce the coupling effect between the power and gate path current.

As the dimensions and the physical arrangements of the Cree module are not available for the general public, a thorough investigation and research has been conducted to design the module with realistic features. It should be noted that the target was not to fully replicate the Cree module, but merely utilize the design aspects, like the location of power terminals and the current pathway, in this module to investigate the performance of what is today considered the state-of-the-art in SiC MOSFET module design.

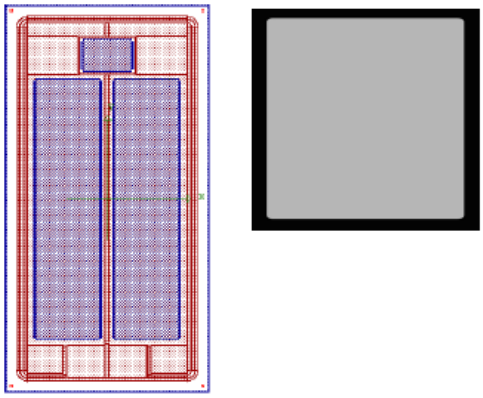

Figure 6: Outline of the SiC MOSFETs (left) and SiC Schottky diodes (right) implemented *[36]*

4.1 MATERIAL SELECTION

As power modules are multilayer structures with different materials in intimate contact with each other, the material selections play a critical in the long-term reliability of the finished product. Critical parts have carefully been selected based on the previous literature study, and the final selections are tabulated in Table 3.

Table 3: Material selection for the 1.2 kV, 300 A, 175 °C module

Assembly part	Materials	Specifications
Switch die	*Cree* SiC MOSFET	1200 V, 63 A (150 °C) Size: 3.10 x 5.90 mm^2 Pads: Al (gate and source) Ni/Ag (drain)
Diode die	*Cree* SiC SBD	1200 V, 50 A Size: 4.90 x 4.90 mm^2 Pads: Al (anode) Ag (cathode)
Topside interconnect	Cu wire	D: 8 mils In parallel: 4
Sinter joint	Ag macro sinter	T_{max} = 380 °C Thickness: 25 µm
Substrate	*Curamik* DBC AlN	Thickness: Cu/AlN/Cu 10/25/10 mils
Baseplate	*CPS Technologies* AlSiC-9	Thickness: 5 mm
Power terminals	Nickel alloy (270)	Thickness: 6 mm

The topside interconnect is selected to be Cu wires. The maximum DC current is calculated by the Preece equation:

$$I_{DC} = A * D^{1.5} \quad (1)$$

In (1), A is a constant dependent on the material selected and the bond-to-bond length. D is the diameter in inches. For Cu wires with a length > 40 mil (0.1 cm) A is 20500 [37]. Thus, for a standard wire of 8 mils, the maximum DC current is 14.5 A. Paralleling four wires at the source pads of the chips is then necessary to achieve the current needed.

As can be seen in Table 3, the baseplate and power terminals has also been considered. The baseplate serves as the mechanical support for the insulating substrate, but also serve as an important heat spreader for the heat sink. Thus, the selected baseplate must have high tensile and flexural strength, a high thermal conductivity and a CTE compatible with the substrate. An AlSiC (Aluminum/Silicon Carbide matrix composite) baseplate is selected due to the very light weight, reasonable high thermal conductivity and its close CTE match with the AlN substrate, although it is pricier than more common Cu/Mo/Cu macrocomposite baseplates. The power terminals are usually copper-based alloys or nickel-based alloys, either soldered to the metallization on the substrate or integrated into the case (connected to the DBC by wire-bonds). Nickel-based alloys (Ni 200 and 270) are generally harder, tougher and stronger than copper-based alloys, making them the preferred choice in high-temperature applications [19].

In Fig. 7, part of the internal vertical structure and its dimensions can be seen, showing the chip layer, sinter interface, DBC substrate and baseplate (not in scale).

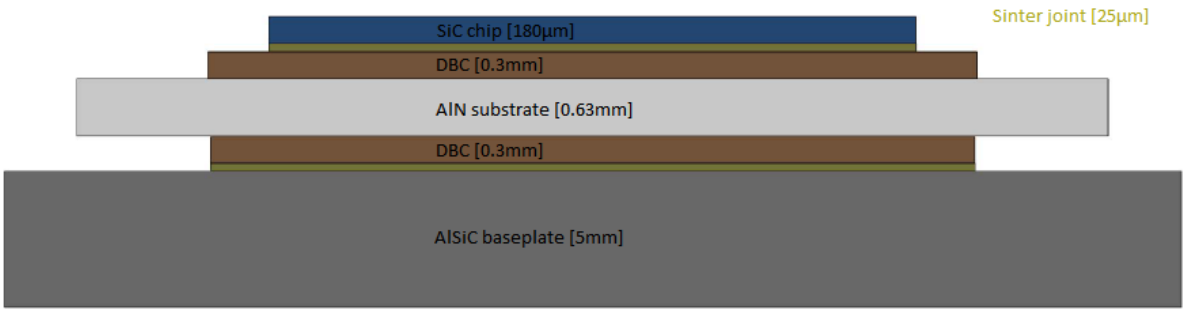

Figure 7: Vertical structure showing dimensions

4.2 POWER STAGE DESIGN

The second step in the development of the module structure, after assigning materials, involves circuit partitioning and calculating required dimensions of the DBC substrate. These dimensions are determined based on a set of design rules provided in [19]. Adding the areas required for the chips, terminals, wire-bonds and the area required for conduction yields the size of the topside metallization. In addition, copper free perimeters (at least 0.3 mm) and a certain width between individual DBCs (at least 0.5 mm) needs to be considered to destine the size of the substrate. Curamik has a selection of standard DBC AlN substrates with copper thickness of 0.3 mm and 0.4 mm for 0.63 mm substrates. For this application, a 0.63 mm substrate with 0.3 mm copper metallization is deemed appropriate. For each switch position, there are two DCB substrates, each containing four transistors and three diodes. The power stage design of one the DBC substrates of the upper switch position can be viewed in Fig. 8. The second DBC substrate is identical. The same design considerations were applied to the two DBC substrates making up the lower switch position.

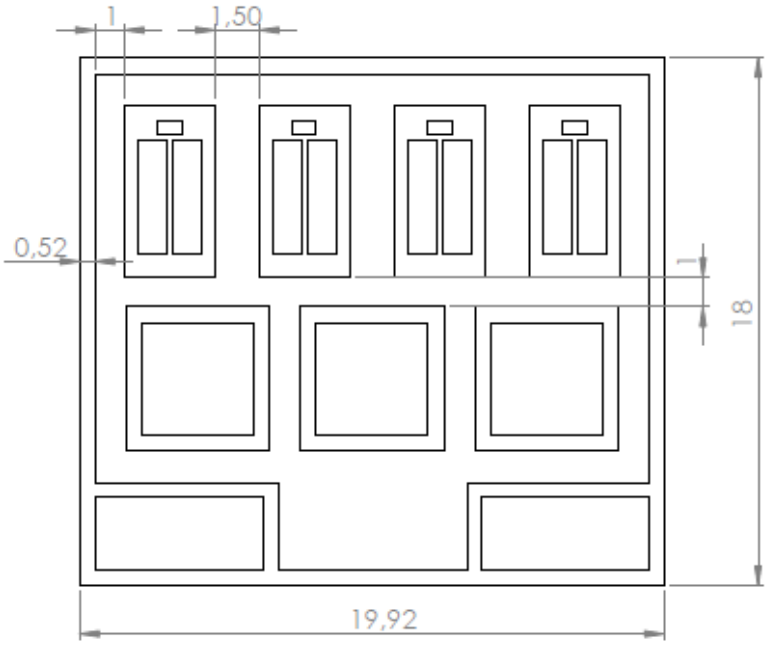

Figure 8: Top view of power stage dimensions [in mm]

4.3 3D CAD MODEL – SOLIDWORKS

The power module model was then realized in SolidWorks and the model comprises the baseplate, DBC substrate, sinter attachment, SiC chips, Cu wire-bonds, and power, gate and source terminals. The developed 3D CAD wire-bonded SiC module can be viewed in Fig. 9. The model consists of 263 individual parts which are assembled and merged together forming the half-bridge structure. The dimension of the baseplate is 58.8mm x 90mm.

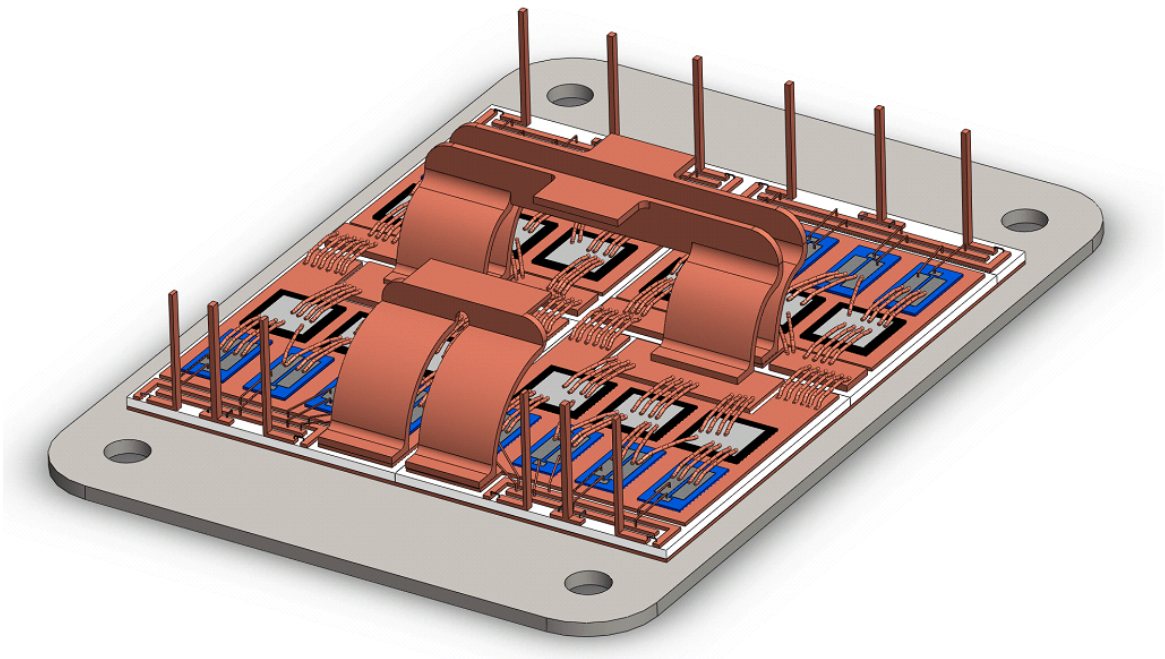

Figure 9: 3D model of the developed power module

As can be seen, a total number of 4 individual DBC substrates makes up the half-bridge module, with each substrate having two gate (return current) source connections (SG), and one gate connection (G). By implementing separate gate source paths, the common source inductance should be reduced to negligible values, as previously mentioned. The two substrates which makes up one switch position are identical and connected to their respective terminal(s). The positive (D1) and negative (S2) DC-link terminals are in the center of the structure. The output terminal (S1D2) is placed on the outer edge of the lower-side DBC substrates, as can be seen in Fig. 10. A top view can be seen in Fig. 11. The housing is not considered in this work.

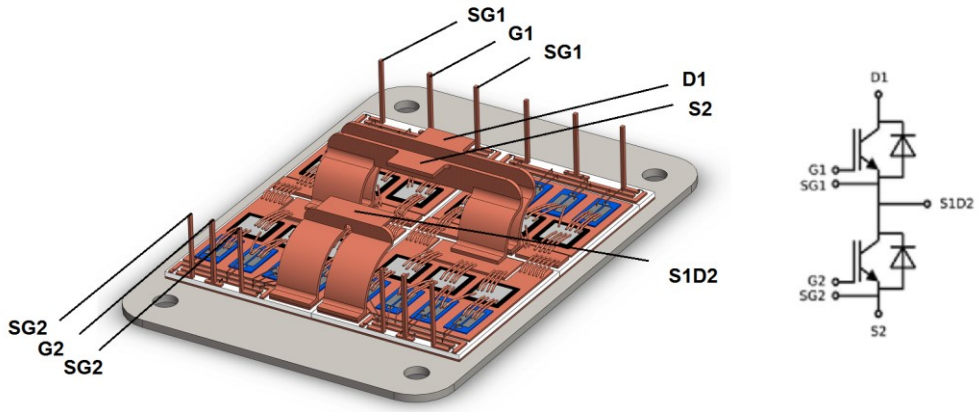

Figure 10: Connections of the developed module

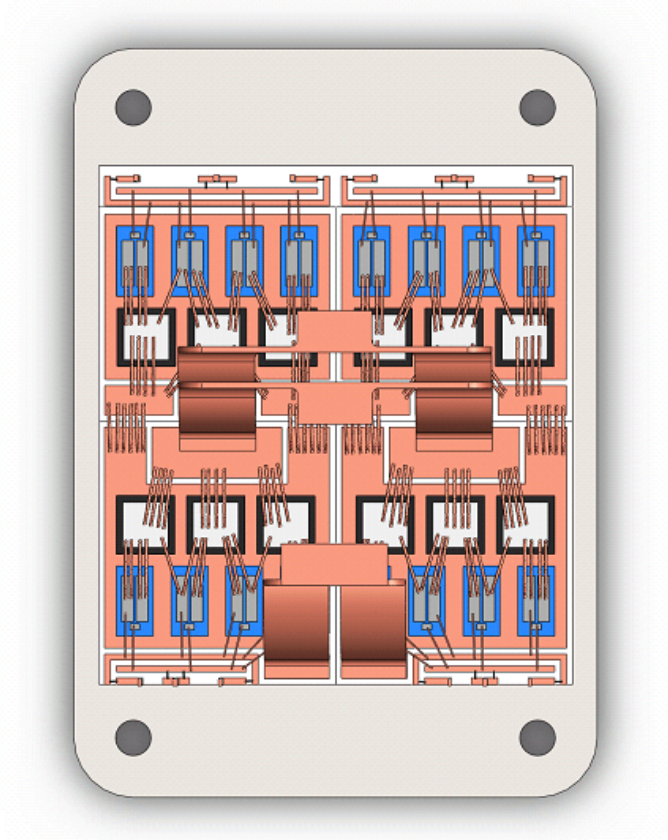

Figure 11: Top view of the developed module

4.4 ANSYS Q3D PARASITIC EXTRACTION

The 3D CAD model was imported into ANSYS Q3D Extraction to destine the stray inductance of the various parts of the geometry. ANSYS Q3D Extraction calculates electromagnetic fields and extracts parasitic components through current conduction paths using a combination of the Finite Element Methods (FEM) and the Method of Moments (MoM). For the software to identify current paths and assign nets (for measuring), the intended paths must be attributed a conductive material (i.e. copper in this work). Therefore, simulations must be conducted in several turns as the devices must be attributed copper and an insulating material (i.e. silicon) for when conducting and not conducting, respectively. After the software has identified the intended current paths (identified the conductive materials), the software can automatically identify nets. To determine which parts of the geometry the software should extract the parasitic inductances, sources and sinks had be located. Finally, a DC analysis was performed. It should be noted that the analysis only considers the partial self-inductances of the various parts of the geometry, i.e. the results are not affected by the effects of mutual inductance between two bodies carrying current in the opposite direction. Thus, the total power loop inductance will followingly deviate somewhat from what would be expected if the module was realized and tested.

In Chapter 5, the performance of the developed module will be assessed with a clamped inductive load pulse-test. The load will be connected across D1 and S1D2. To simplify the analysis (and significantly reduce computation time) the DC-analysis only includes half of the geometry and only involves the parts that are excited when the upper diodes and the lower MOSFETs conduct (as is the case for a pulse-test on the lower-side MOSFETs). The various parts of geometry which were analyzed are depicted in Fig. 12.

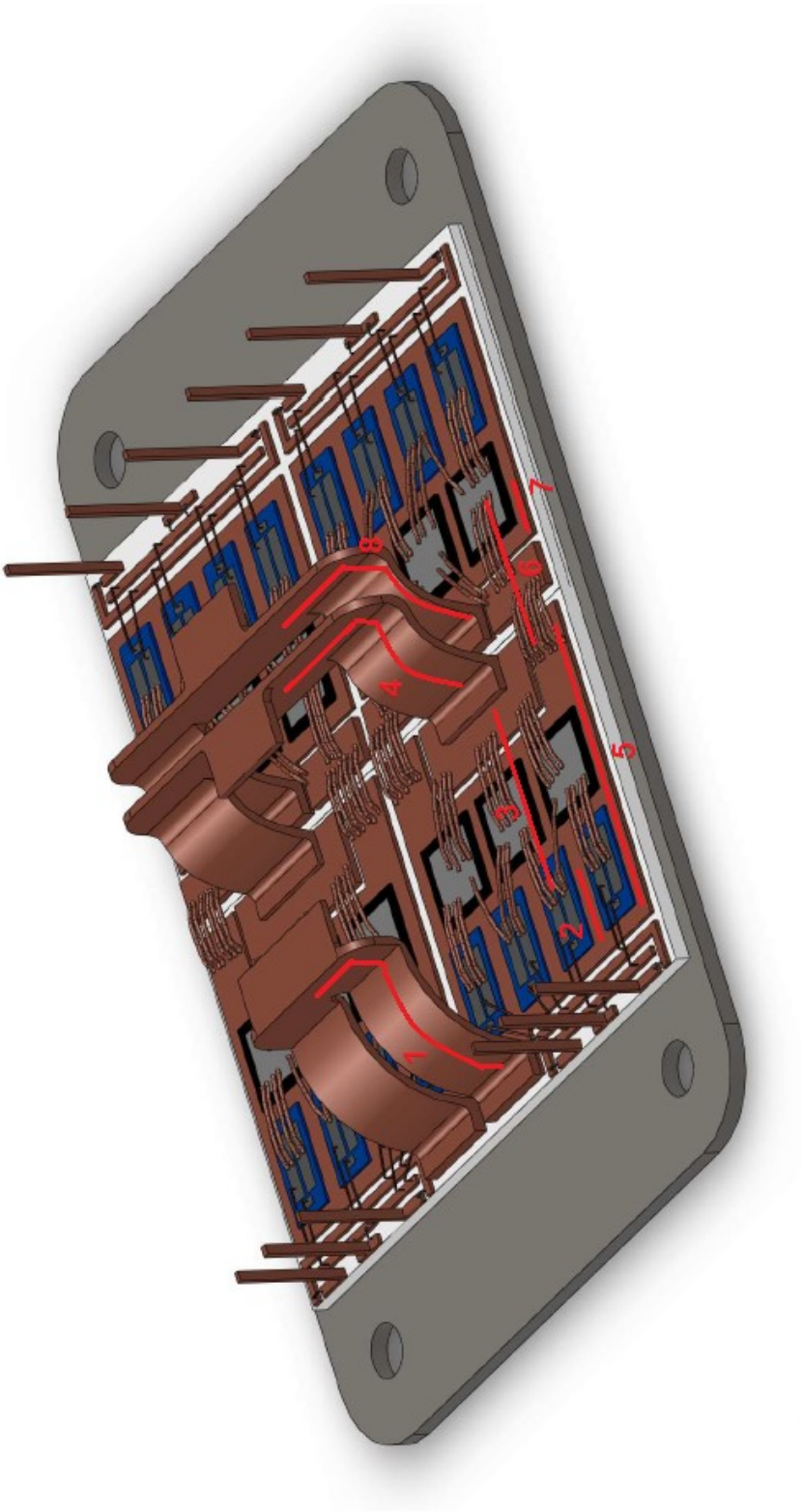

Figure 12: The markers indicate the conductive parts subject to analyses

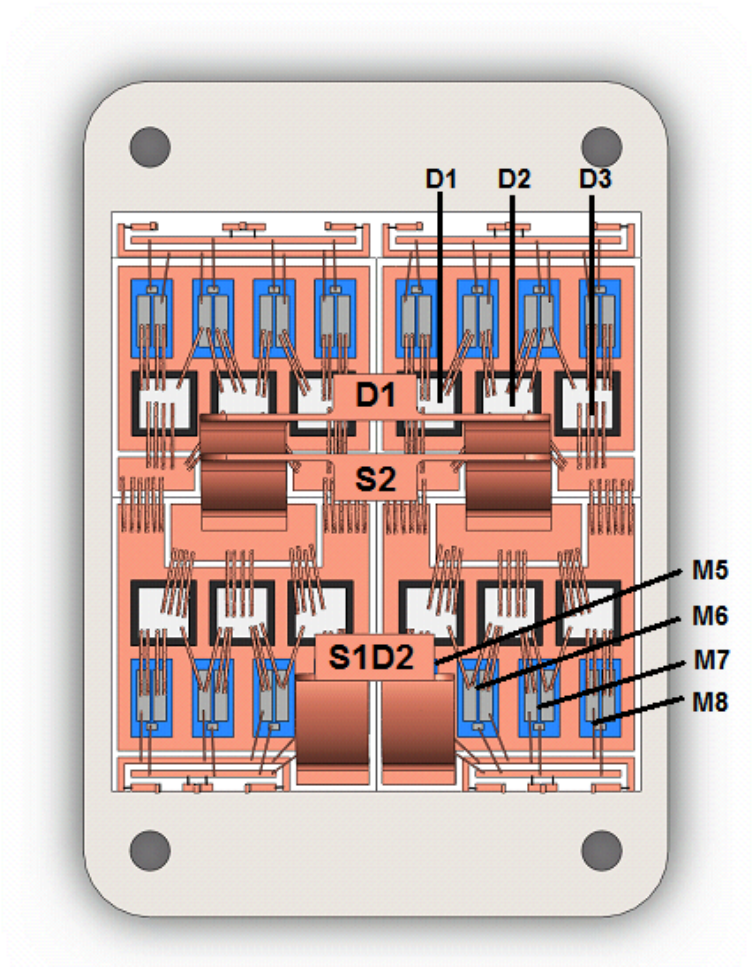

Figure 13: The devices under consideration

When the lower MOSFETs conduct (M5-M8), the current pathway is from the S1D2 terminal (1), to the DBC and up the drain side of the MOSFETs (2), through the wire-bonds (3) before it sinks at S2 (4). When the MOSFETs turn off, the current freewheels through the upper diodes (D1-D3). The current pathway in this case is from S1D2 (1), across the DBC (5), trough the wire-bonds and to the anode side of the diodes (6), trough the DBC (7), before it sinks at D1 (8). This is a simplified explanation, as the extracted parasitics will be different for each device (based on their location on the DBC). This is considered in the simulations. The extracted self-inductances of each conductive part are depicted in Fig. 14.

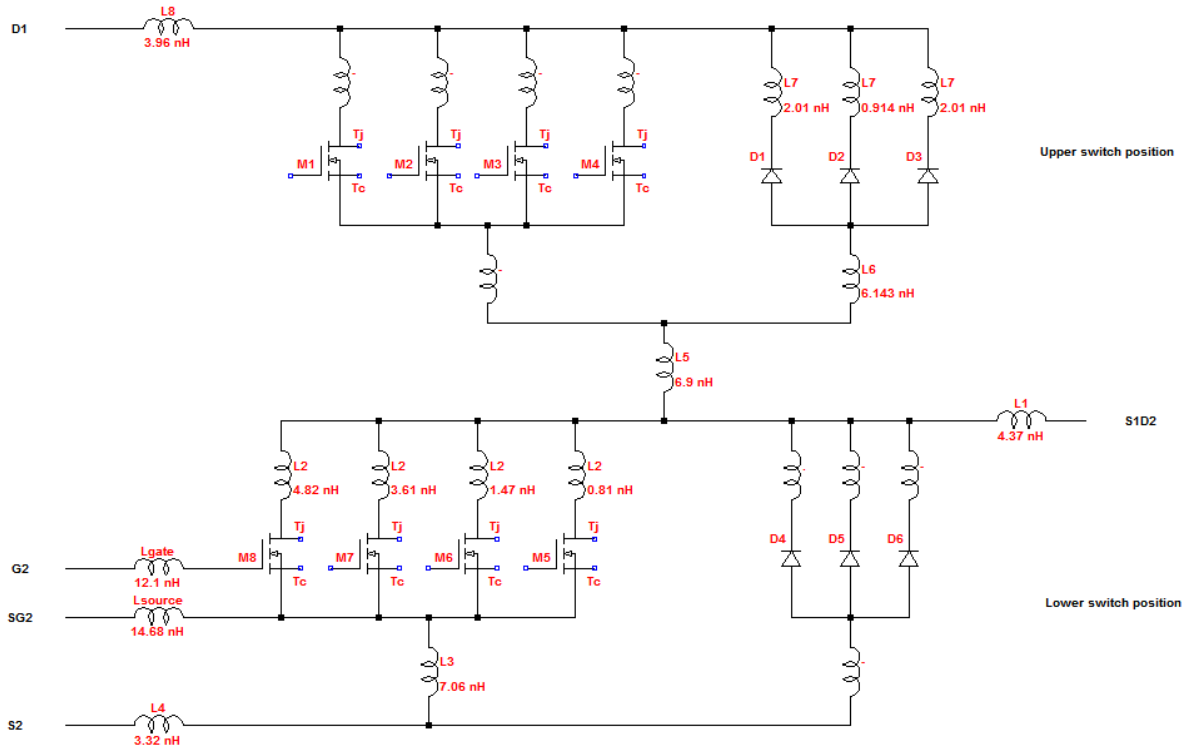

Figure 14: Extracted parasitic self-inductances

As can be seen, the power terminals introduce a great deal of stray inductance to the module. In this geometry, about 50% of the partial self-inductances originates from the power terminals. About 30% of the total partial self-inductances origins from the DBC substrate. Due to the low current rating of the devices many chips must be paralleled, which necessitates a quite large DBC substrate. The rest, about 20 %, comes from the usage of wire interconnects. The low share from the wires can be explained by the paralleling of the wires, as well as the usage of Cu wires. The high share from the power terminals is due to the thick and tall structure. As can also be observed, based on the location of the devices on the substrate, the paralleled devices will have some variations in stray inductance, despite the effort of the author trying to achieve a symmetrical design. In addition, the gate inductances are quite large due to the slender gate trace and thin wire interconnects.

CHAPTER 5 ESTIMATION OF SWITCHING PERFORMANCE - PULSE-TEST IN LTSPICE

In this section a pulse-test under a clamped inductive load is used to estimate the switching behavior of the developed module. A (double) pulse-test under a clamped inductive load is a standard approach to obtaining voltage and current waveforms during switching and thus evaluate the switching performance of devices/modules. A clamped inductive load is also a common situation for power devices in PWM, hard-switched converters, supporting the convenience. The commercial available software program LTSpice has been used for the investigation. The extracted parasitic inductances from the previous section together with the inherent parasitics of the devices makes up the parasitic elements of the circuit. The LTSpice models of the devices are downloaded from the manufacturers webpage and are implemented in the model as sub-circuits (which includes all the device parasitics).

As can be seen in Fig. 15, the device models have five terminals; Drain, Source and Gate, as well as two temperature terminals. The two temperature terminals Tj (junction temperature) and Tc (case temperature) work as voltage pins; a voltage difference of 1V refers to a temperature difference of 1 °C. The Tc terminal is set to 25 °C and the Tj terminal is set to 175 °C.

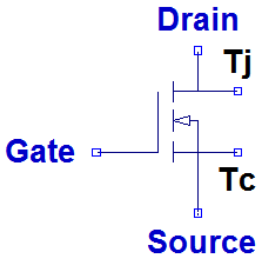

Figure 15: SiC MOSFET device model from Cree

The DC voltage is set to 800 V, and a pulse-test is conducted on the lower-side MOSFETs. As the source of the lower MOSFETs are grounded, this is also the most common setup. The LTSpice pulse-test circuit is depicted in Fig. 16. The residual power path inductance is set to 15 nH (i.e. of DC-link capacitor, bus bars and the connection arrangements). The gate voltage swing is set to 25 V (-5/20 V), as per the device datasheet, and the gate resistance is set to 10 Ω. The extracted gate path inductances are included. The gate driver circuits for the four

MOSFETs are identical and the gate pulse have a turn-on and turn-off delay time of 1µs, and a rise and fall time of 25 ns.

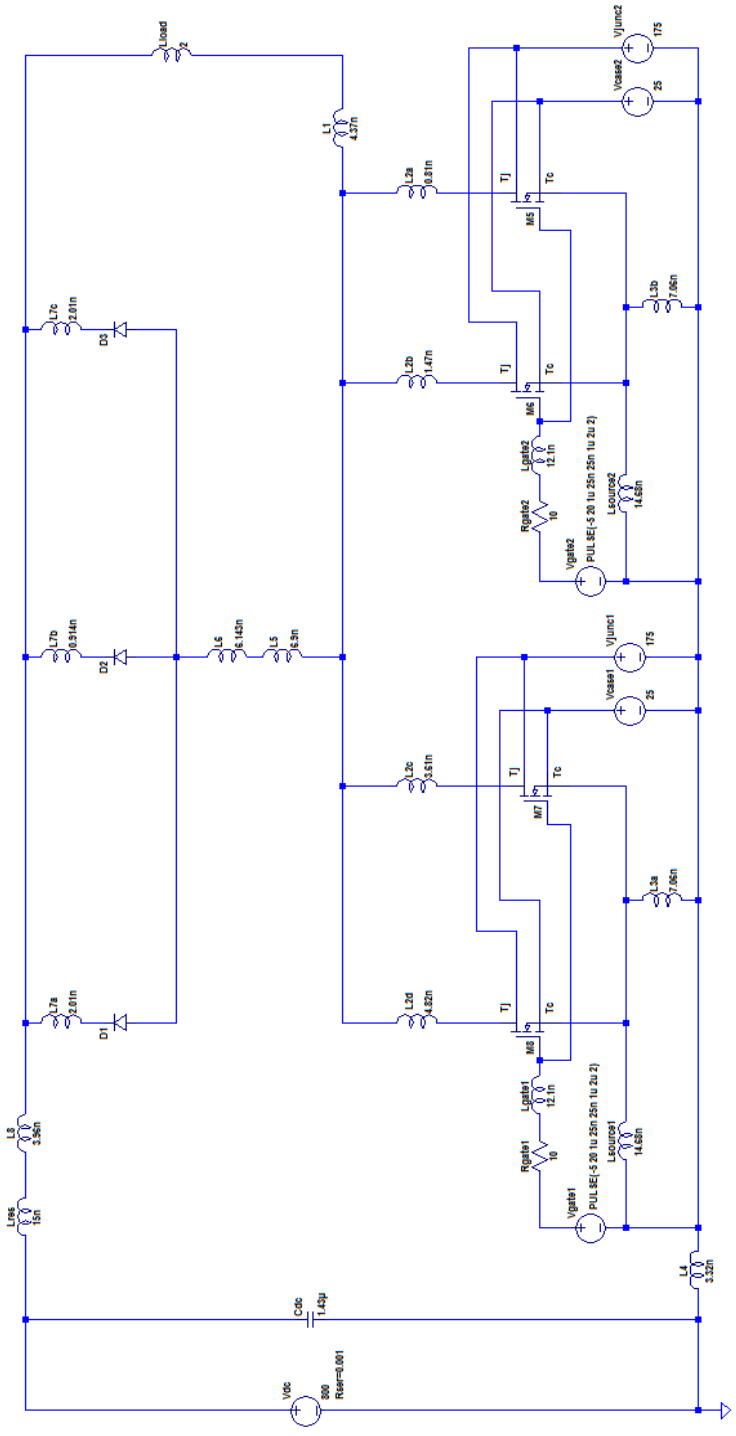

Figure 16: Pulse-test circuit in LTSpice

In a real double-pulse test the first pulse established the desired current by building up the inductor current. By controlling the duration of the gate pulse of the devices under test, one can evaluate the turn-off and turn-on switching transients at the desired device current. During the following turn-off pulse the inductor currents freewheels through the upper diodes. The second turn-on pulse lasts for only a short time. In this work, a current source of 150 A represents the load inductor, providing a constant current throughout the switching cycle, thus only a single pulse is needed. The nominal current for each MOSFET die is then 37.5 A. The simulated drain-source voltage (blue) and drain current (red) of MOSFET M5 are depicted below.

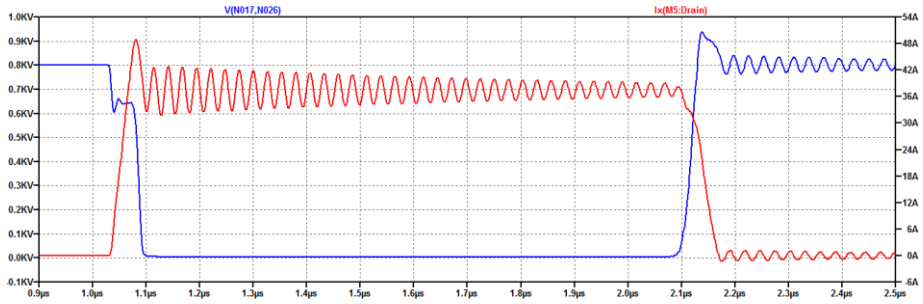

Figure 17: Turn-on and turn-off waveform of M5

As can be seen in Fig. 17, the drain current waveform contains an unfortunate high overshoot at turn-on. Although the SiC Schottky diodes exhibit zero reverse recovery charge, the charging of their junction capacitance ads to the drain current together with the load current causing the current spike. The change in diode voltage also requires current in the turn-off process, which can be seen by the current drop before the drain-source voltage reaches the off-state value. The current overshoot under these test conditions is for M5 11.38 A (30 %), which does not challenge the reliability of the device, but introduce higher losses. As can also be observed, the voltage waveform contains a notch at turn-on and overshoot at turn-off, which is due to the voltage induced upon the power loop inductances by the rising and falling drain current, respectively. The notch at turn-on and overshoot at turn-off in the drain source voltage is 193.4 V (24.2 %) and 137.2 V (17.2 %), respectively.

One big concern in SiC MOSFET multichip modules is the uneven current distribution between paralleled dies that can arise due to any circuit mismatch (variations in common source

inductance, power loop in inductance, gate driver mismatch, etc.) or die mismatches (in on-state resistance, threshold voltage, etc.) [38]. Clearly, the die models are identical in the test circuit, but the simulations also reveal very little circuit mismatch. The drain current of M5, M6, M7 and M8 are depicted in Fig. 18, showing an event transient current distribution between the devices.

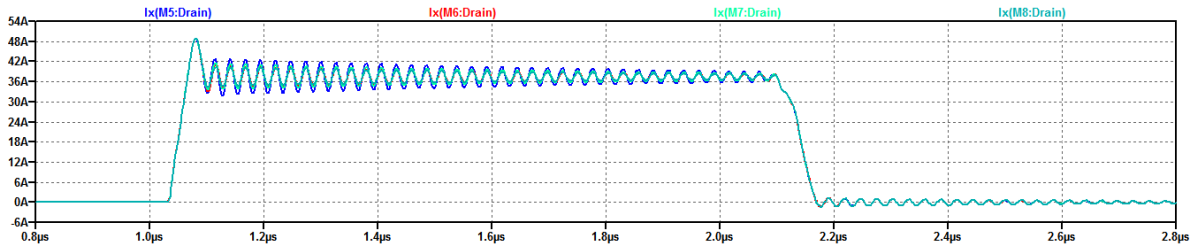

Figure 18: Current waveform in the four MOSFETs

In Fig. 19 the M5 turn-on and turn-off power loss is showed. The average turn-on power loss is 7.7 kW and the average turn-off power loss is 7.2 kW. The energy loss is 1mJ and 0.8mJ for the turn-on and turn-off process, respectively. These losses are very low (threefold less) compared to Si IGBTs for the same conditions [39]. The results are similar to the energy losses provided in the datasheet (1mJ and 0.4mJ) for the same conditions (V_{DS} = 800 V, I_D = 37.5 A).

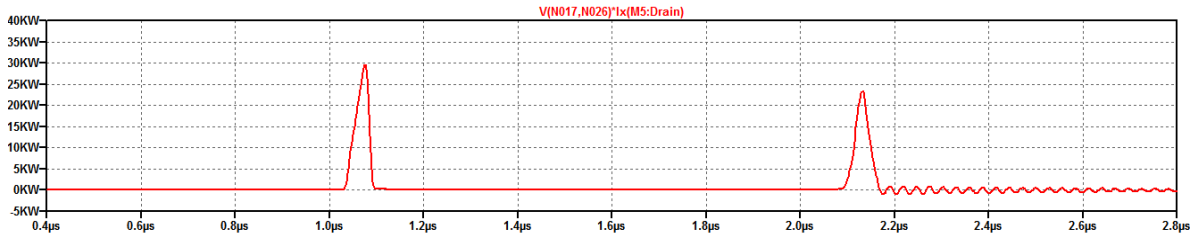

Figure 19: Turn-on and turn-off power loss of M5

As mentioned, the reason for voltage notches and overshoots are due to the power loop inductances and the transiting drain current. Thus, the estimation of total power loop inductance can be calculated based on the induced voltage and the current slew rate. The ringing frequency is also a measure of the power loop inductance; however, it requires accurate knowledge of the capacitive effects. The voltage dip at turn-on is 194.81 V and the drain current slew rate is 1.309

A/ns, indicating that the power loop inductance for one MOSFET die is 193.4/1.309 = 147.75 nH. Subtracting the contribution from the external parts yields an internal power loop inductance of 132.75 nH for one die. In turn, the total internal power loop inductance for the 150 A test setup is calculated to be 33.2 nH, indicating that the estimated total power loop inductance for the developed module is 16.6 nH. For comparison, the datasheet value of the loop inductance in the real module from Cree is 15 nH [36].

The ringing observed succeeding the turn-on and turn-off process occurs due to the very high dv/dt and di/dt in combination with circuit and device parasitics. Maintaining conformity with the standards of EMC (electromagnetic compatibility) are reported to be challenging for high-performance SiC MOSFET modules. Ringing in signal waveforms are one of the most critical issues related to hard-switched SiC MOSFETs [40] [41]. The greatly increased switching speed (di/dt, dv/dt) desired when replacing SiC MOSFETs with Si IGBT has a direct impact on the EMI (electromagnetic interference) generated. In this work, the turn-on and turn-off rise and tall times associated with switching the MOSFETs are in the range of 25-50 ns, which is very fast when compared to comparable state-of-the-art Si IGBTs (in the range of 200 ns). This enables very fast switching, but as can be observed in Fig. 20 and 21, some underdamped ringing occurs. To explain the phenomenon, the current paths need be evaluated. At turn-on, the load current shifts from the freewheeling diodes to the MOSFETs. Once the full load current and the charging current has commutated to the MOSFETs (diode stops conducting), the output capacitances of the MOSFETs (C_{OSS}) starts to discharge and the drain-source voltage begins to drop. Concurrently, the DC-link voltage builds up across the diodes, i.e. the junction capacitance (C_J) charges. Thus, the current "sees" C_J, C_{OSS} and the power loop inductance in series. For these specific devices, the MOSFET output capacitance is 1150 pF and 150 pF when the device is in the ON-state and OFF-state, respectively. The junction capacitance of the Schottky diode is 3380 pF and 173 pF, respectively. Thus, after the turn-on process the current sees a capacitance close to the value of C_J (150 pF) and the ringing frequency can be determined as (2). At turn-off, the load current is transferred back to the freewheeling diodes and as C_{OSS} gets charged while C_J gets discharged. Thus, at turn-off, the current sees a capacitance close to the value of C_{OSS} (143 pF). These effects can be viewed in Fig. 20 and 21.

$$f_{ringing} = \frac{1}{2\pi \sqrt{L_\sigma (C_J || C_{OSS})}} \tag{2}$$

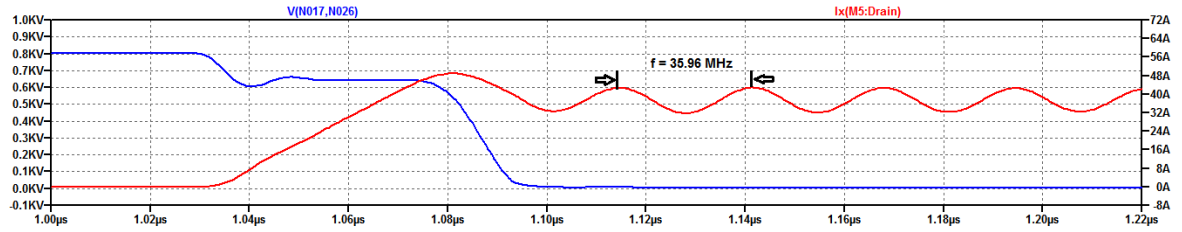

Figure 20: Turn-on waveform of M5

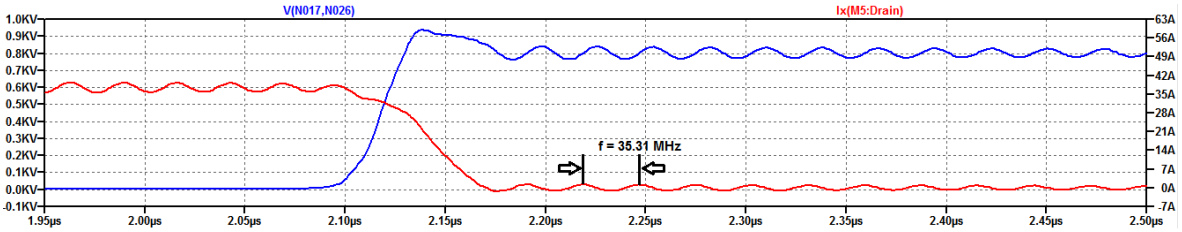

Figure 21: Turn-off waveform of M5

The measured resonant frequency after the turn-on process is 35.96 MHz, and the estimated ringing frequency based on (2) is 35.66 MHz. For the turn-off process the measured ringing frequency is 35.31 MHz, whereas the calculated is 35.19 MHz.

As has been greatly addressed in the literature and has been showed in this work, the parasitic inductances have a direct impact on switching behavior when targeting to exploit SiC MOSFETs. Especially the bulky power terminals and DBC offers too much inductance to be able to let SiC MOSFETs unfold its fast switching capabilities. The voltage and current overshoot occurring during hard-switched transients can be directly seen on the simulated waveforms. Although the overshoots were within the safe operating range for this test circuit owing to the high voltage margin (400 V) and the de-rated devices, it has an impact on the effiency. The fast switching transients and the parasitic elements of the module were also showed to cause underdamped high-frequency oscillations in signal waveforms which can provoke EMI challenges.

CHAPTER 6 SUMMARY, CONCLUSIONS AND FUTURE WORK

6.1 SUMMARY AND CONCLUSIONS

In this thesis, a half-bridge module rated at 1.2 kV, 300, 175 °C A employing SiC MOSFETs and SiC Schottky diodes has been developed and evaluated using computer tools. As the SiC MOSFETs capabilities indicate that very high power-density modules can be developed, the developed module was targeted for applications in the transportation sector. However, the conventional package and module design were disclosed to not properly display these superior capabilities. Thus, a literature study of module design trends and thrust areas for developing advanced SiC modules was necessary and were also provided for the reader. As per the investigation, to facilitate high-temperature operation and fast switching, solderless and wire-bond less technologies were highlighted as promising solutions, as well as new materials for substrates and encapsulants. Some novel design technologies for unfolding the SiC MOSFET capabilities, like the planar-bond all and the SkiN technology, was emphasized as particularly promising. However, most of the novel design technologies lack reliability testing for high-power applications, hence the developed module was designed as a conventional wire-bonded module. The developed module emulated a commercial available module from Cree. Based on the literature study, the materials were chosen and a proper power stage design was conducted. The module was realized in SolidWorks and the 3D CAD model had a baseplate dimension of 58.8x90 mm.

The 3D CAD module was then imported into ANSYS Q3D for extracting the module parasitic inductances. The results of the simulations revealed that the bulky power terminals and the large DBC substrate area (due to the low current rating of the SiC MOSFET dies) introduced large stray inductances (tens of nanohenries). In addition, variations in stray inductances between dies were disclosed. The wire-bonds did not introduce as much parasitics as one would predict, however, the biggest issue with the wire-bond technology is still the reliability during big temperature excursions. The contribution from the power terminals could have been mitigated by a strip-line arrangement, which could have readily been implemented. In addition, as the rating of SiC MOSFETs dies increase, the contribution from the DBC substrate should decrease. However, only considering the partial self-inductances can be

marked as a limitation, as mutual effects between the DBC and wires, and between the wires themselves are anticipated. Nonetheless, the findings are still very valuable.

The extracted parasitic inductances were then incorporated into a test circuit in LTSpice to investigate the switching performance of the module in the presence of these parasitics. The switching device models was provided by Cree and implemented with the recommended gate characteristics. A test circuit, rated at 800 V and 150 A, having four SiC MOSFETs and three SiC Schottky diodes was developed. Thus, the rated current of the MOSFETs and the diodes were 37.5 A and 50 A, respectively. A pulse-test with an inductive clamped load revealed that the test circuit had a power loop inductance of 33.42 nH, which yielded a drain-source voltage notch of 193.4 V (606.4 V) at turn-on and an overshoot of 137.2 V (937.2 V) at turn-off. The current transition times were in the range of 25 and 50 ns for the turn-on and turn-off process, respectively. These transition times are very fast compared to comparable Si IGBTs, yielding the possibility of achieving very high switching speeds. The charging of the diode junction capacitance gave the drain current an overshoot of 11.38 A (30 %) at turn-on. The ringing observed following the switching transients were discussed and demonstrated to be an effect of the power loop inductance resonating with the junction and output capacitances of the devices. The developed module had a mismatch of only 1.6 nH from the real Cree module and the simulated energy losses were also close to the datasheet value of the real module.

The investigation shows that using computer tools can be a viable, and time- and cost efficient approach to predicting the performance of power electronic modules. In addition, the investigation suggests that using computer software can be an excellent tool to understand and investigate the electrical performance of SiC modules.

6.2 Future Work

Many valuable investigations have been left out to future work due to lack of time. Designing and developing the 3D CAD model of the module took a large share of the provided time scope, yielding in a limited time for extensive performance assessment and evaluation. However, the developed module and the results of the electrical performance assessment forms an interesting platform for further investigations. The suggestions below are investigation I would find the most prevalent for extending the learning outcome.

- ***Parametric (sweep) study in LTSpice***

The performance assessment in this work was conducted with the circuit parameters set. The developed test circuit forms a very good platform for investigating how circuit parameters influence the switching performance of the MOSFETs/module. How the performance and device stress increase/decrease with varying gate resistance, gate-pulse characteristics and power loop inductance are characteristics that need to be investigated. Further, the turn-on and turn-off energy loss as function of drain-current and DC-link voltage could be investigated.

- ***Gate driver characteristics***

The focus in this thesis was on the parasitics in the power loop. The gate traces and the arrangement in the 3D CAD model was merely implemented as a first approximation of the gate path inductance. In addition, no fine tuning of gate driver characteristics was conducted. A more vigorous attention to gate driver characteristics and parasitics and its impact on switching performance and device reliability would be very interesting to investigate. Fine tuning of the gate resistance (for switching performance and energy losses), variations in stray inductance between paralleled dies, oscillations in gate voltage waveforms (due to Miller effect and resonant circuits) are all aspects that would be interesting to take a closer look at. These characteristics could be readily investigated with the methodology provided in this thesis.

- ***Transient thermal analysis***

One of the main objectives in the design of the half-bridge module was high-temperature operation. Yet, a thermal study to validate the design is missing (time related). In a real, proper design methodology, the electrical and thermal design considerations should be integrated, as they are strongly interdependent. The 3D CAD model with the assigned materials and the switching and conduction losses (from Ch. 5) could, by using thermal simulations in a multiphysics software (such as COMSOL, ICEPACK, etc.), be used to determine the heat flux through the module. The thermal profile from junction to case (thermal resistance and thermal coupling) could then be used to assess the junction temperature as function of DC-link voltage, drain current, switching frequency, etc. and thus assess the high-temperature performance of the developed module.

- ***Strip-line design of power terminals***

The design of the half-bridge module was inspired by the state-of-the-art Cree module. As was disclosed in Ch. 4, the power terminals introduce relatively much stray inductance in the power loop. To improve the design, the power terminals (D1 and S2) could be designed in a strip-line manner to investigate the impact of mutual flux cancellation (reduced power loop inductance) on switching behavior. This could be done in SolidWorks with little exertion.

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