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Power Electronics in Low-Voltage DC Circuit Breakers

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Abstract

Low-voltage direct current (LVDC) microgrid has recently been recognized as a feasible solution for next generation electrical power distribution network, due to several benefits that it offers an increasing amount of facilities. However, LVDC microgrids suffers from crucial concerns, which needs to be properly addressed before being conceived as a commercially and economically available solution for future power distribution. LVDC protection technology lacks experience, standards and guidelines, resulting in typical expensive and overdimensioned electrical components comprising LVDC systems. It is necessary to develop an economical DC protection solution, which is capable of conducting with low losses and rapid short-circuit currents interruption, without being destroyed in the process.

A promising circuit breaker (CB) based purely on power electronics, comprising 2 antiparallel connected commercially unavailable reverse blocking integrated gate commutated thyristors (RB-IGCTs) has been developed by ABB. Replacing the unavailable RB-IGCT devices in the original CB design with insulated gate bipolar transistors (IGBTs) or asymmetric integrated gate commutated thyristors (A-IGCTs), is evaluated. Based on proper parameterization, two CB configurations are presented, comprising either 12 parallel connected 3.3 kV rated IGBTs from Infineon, or 8 parallel connected 4.5 kV rated A-IGCTs from ABB. These configurations are compared against each other, using simulation models assembled in Matlab® Simulink. The higher voltage ratings of the A-IGCT allowed the CB to utilize larger metal oxide varistors (MOVs), which reduces the energy dissipation period with approximately 1 ms. The A-IGCT based CB is indicated to be more expensive, due the CB configuration being 60 % heavier than that of the IGBT based CB. On the other hand, the A-IGCT based CB is able of conduct nominal current with 23 % of the losses to that of the IGBT based CB. Since excessive conduction losses are one of the major disadvantages of solid-state CB, the 4.5 kV A-IGCT is concluded to be the most promising semiconductor device for the CB design.

The preferred CB is later utilized to protect three simplified isolated LVDC systems modelled in Simulink against short-circuit faults. Its breaking performance indicated that the A-IGCT based CB might be overdimensioned for the considered LVDC system, but is however conceived as a feasible solution. The promising CB configuration comprising 4.5 kV rated A-IGCTs was able of interrupting faults of 17.5 kA at 3000 V within approximately 2 ms of fault injection.

Sammendrag

Lavspente likestrøm (LVDC) mikrogrid har nylig blitt anerkjent som en mulig løsning for neste generasjons kraftforsyningsnettet, på grunn av forskjellige fordeler som oppnås i en økende mengde elektriske applikasjoner. LVDC-mikrogrider lider imidlertid av et avgjørende problem, som må behandles riktig før det kan bli en kommersiell og økonomisk løsning. Beskyttelsesteknologien for LVDC-mikrogrider mangler erfaring og standarder, noe som resulterer i typiske dyre og overdimensjonerte elektriske komponenter i LVDC-systemer. Det er nødvendig å utvikle en økonomisk beskyttelsesløsning, som kan raskt og effektivt bryte en kortslutningsstrøm uten å bli ødelagt i prosessen, og i tillegg lar seg lede med lave spenningstap.

Denne oppgaven presenterer to strømbrytere basert på halvlederteknologi med samme krets design. Den ene bryteren omfatter 12 parallelkoblede 3,3 kV-klassifiserte insulated gate bipolar transistorer (IGBTer) fra Infineon, mens den andre bryteren omfatter 8 parallelkoblede 4,5 kV-klassifiserte asymmetric insulated gate bipolar transistorer (A-IGCTer) fra ABB. Disse konfigurasjonene blir sammenlignet med hverandre ved hjelp av simuleringsverktøyet Matlab® Simulink. Den høyere spenningsklassifiseringen til A-IGCT tillot bryteren å benytte seg av større metalloksydvaristorer, som reduserte energispredningsperioden med ca. 1 ms, i forhold til den IGBT baserte bryteren. Den A-IGCT baserte bryteren var indikert for å være den mest kostbare løsningen, da den veide 60 % mer enn den IGBT baserte bryteren. På en annen side, var den A-IGCT baserte bryteren i stand til å lede strøm med 23% av tapene til den IGBT baserte bryteren. Siden store spenningstap oppfattes som en av de største ulempene ved brytere basert på halvlederteknologi, ble den A-IGCT baserte bryteren konkludert med å være det mest lovende forslaget.

Den foretrukne strømbryteren ble senere utnyttet for å beskytte tre forenklede isolerte LVDC-systemer mot kortslutningsfeil, utført i Simulink. Bryteren sin ytelse i systemene indikerte at den A-IGCT basert bryteren kan være noe overdimensjonert for det vurderte LVDC-systemet, men at den imidlertid er en gjennomførbar løsning. Den resulterende strømbryteren basert på 4.5 kV klassifiserte A-IGCTer er i stand til å avbryte kortslutningsfeil på 17,5 kA med 3000 V i løpet av ca. 2 ms etter at feilen var påført systemet.

Acknowledgments

I would like to express my appreciation to my supervisor and professor Dimosthenis Peftitsis for guidance and assistance throughout my specialization project and master thesis. He has shown patience, and been a major contributor to this project, by discussing problems and providing suggestions which made the project possible to conduct.

I would like to thank my friends at NTNU for making my student life a wonderful experience. And a final thank you to friends and family for great support.

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Abbreviations of Acronyms

AC	Alternating current
A-IGCT	Asymmetric integrated gate-commutation thyristor
CB	Circuit breaker
CLR	Current limiting reactor
DAB	Dual active bridge
DC	Direct current
DER	Distributed energy resource
EMF	Electromotive force
EV	Electrical vehicle
hDC-CB	Hybrid direct current circuit breaker
HV	High voltage
IBDC	Isolated bidirectional DC-DC converter
IGBT	Insulated-gate bipolar transistor
MC	Mechanical contact
MCB	Mechanical circuit breaker
MOV	Metal oxide varistor
MV	Medium voltage
NTNU	Norwegian University of Science and Technology
PV	Photovoltaics
PWM	Pulse width modulation
RB-IGCT	Reverse blocking integrated gate-commutation thyristor
SiC	Silicon carbide
SSCB	Solid state circuit breaker
TIV	Transient interruption voltage
VI	Voltage and current

VSC Voltage source converter

WBG Wide band gap

ZCS Zero current switching

ZVS Zero voltage switching

1 Introduction

1.1 Background

The background information provided in this thesis are obtained from a brief survey comparing AC and DC technologies found in [1]. DC technologies have gained a significant amount of attention from research during the last decades, due to the promising benefits an increasing amount of electrical applications gains by utilizing DC. Compared to the AC counterpart, DC systems have more efficient power delivery with lower losses, improved reliability, higher control flexibility, and supports simpler interconnections of asynchronous systems, such as grids with different system parameters, or sources and loads operated at variable speed [1-5]. LVDC system is a relatively new concept compared to the HVDC counterpart, and is normally used for microgrids, where efficient power electronic interfaces are utilized to achieve simple interconnections of sources, energy storage and other electronic equipment [1, 6-8]. LVDC microgrids may be applied for ships, airplanes, home applications, office buildings, EV charging stations, and data centers in the future [1, 2, 5-7, 9-12].

The main barrier hindering mass deployment of cost-effective LVDC systems, is the major absence of guidelines, standards and experience of proper fault protection technology for LVDC systems [1, 2, 6]. Conventional CBs applied for DC applications either suffers of excessive conduction losses, or insufficient fault operation speed [1, 13]. The commonly used CBs for DC applications are based on mature MCB technology applied in AC systems. MCBs operate relatively slowly, requiring several tens of milliseconds to break currents [1, 14-16]. DC systems lack large system impedances, resulting in excessive rise of fault current. It is therefore necessary for the LVDC protection system to clear the fault within a few milliseconds, to prevent great damage to the components in the system caused by excessive fault currents [1, 14-17]. Slow operating MCB for DC applications, results in expensive overdimensioned components comprising the LVDC system. Newer SSCB based purely on power electronics are capable of breaking fault currents within microseconds, but suffers from relatively large on-state losses, limiting the use of SSCBs to current sensitive applications, where conduction losses are manageable [14, 17-19]. Hybrids combining SSCB and MCB have been developed in order to eliminate the disadvantages and gain the advantages of both technologies. By parallel connecting these concepts, hDC-CBs have the conduction characteristic of MCBs and fast switching characteristic of SSCBs [20].

This thesis studies a relatively newly developed semiconductor device, able of conducting with low losses, which will be suggested to be utilized for SSCB applications, subsequently increasing the possibility of developing a cost-effective LVDC system.

1.2 Objectives

The main objectives of this thesis are:

- Develop a simple small scale microgrid, comprising the most typical electrical components.
- Establish design guidelines for the power electronic devices comprising a SSCB, which may be utilized in the considered microgrid.
- Present the operation principles of a promising bidirectional SSCB comprising RB-IGCTs.
- Analyse the opportunity of replacing RB-IGCTs in the original concept with commercially available IGBTs and IGCTs, by designing two CBs proposals, of each of these semiconductor devices. Adequate MOVs will be selected for both solutions.
- Assemble adequate test models to be used in Matlab® Simulink, in order to compare and present the most promising proposal.
- Develop Simulink models of three simplified LVDC systems, based on the presented microgrid, to further evaluate the performance of the preferred CB.

1.3 Limitations and Simplifications

To limit the scope of work, these following assumptions and simplifications were considered for this thesis:

- Components are assumed ideal.
- The selection of MCs and heat sinks will only be briefly discussed.
- The current flow through parallel connected devices is assumed to have uniform current distribution.
- Detecting relays are not considered, only the detection time.
- Thermal modelling is performed in one dimension, and only discussed.
- The protection drive of the converters are not considered.
- Switching and conducing losses of converter are not studied.
- Converter control is not implied for the simulations. Only one point of operation will be considered for each system.

1.4 Approach

A LVDC microgrid comprising some typical component will be developed. Critical aspects of faults will be discussed, and design guidelines for the CB to protect the considered microgrid will be established. Based on conclusions in [1], the operation principles of a bidirectional SSCB will be presented. The opportunity of utilizing newer developed IGCTs will also be evaluated for the considered CB, by developing two CBs configurations, based on either IGBTs or IGCTs. Adequate MOVs will be evaluated for each solutions. Test models will be established to be simulated in Matlab® Simulink, where the two CB configurations will be compared against each other. The preferable CB configurations will be used to protect three relatively complex microgrid models developed in Simulink, where the operation process of the CB will be further analysed.

1.5 Outline of the Report

Chapter 2: Development of the considered LVDC microgrid and its main components.

Chapter 3: Key aspects of faults occurring in LVDC grids.

Chapter 4: Operating principle and designer guidelines assembly of the circuit breaker under consideration.

Chapter 5: Selection and parameterization considering specific CB component.

Chapter 6: Considerations and development of the Simulink simulation models.

Chapter 7: Presentation and analysis of the result.

Chapter 8: Discussion, and conclusion.

Chapter 9: Suggestion of future work.

2 System Description

This chapter presents the considered LVDC microgrid and its main components for this thesis. Calculations and selection of system parameters are provided in this chapter.

2.1 DC Microgrid Definition

A microgrid system is a part of a distribution system interconnecting several small sources and loads able of operating as an isolated electronic power system [7]. Recently, the interest of exploring DC microgrid as a future technology has increased rapidly, due to the constant improvements and the falling cost of power electronics, the growing interest in enhancing electrical efficiency and developing environmental solutions, the increasing penetration of generators and loads operating at variable speed, and the benefits arising from utilizing DC [1]. DC systems support the increasing number of installed DER systems, by reducing the number of conversion stages compared to the AC counterpart [7]. Sources connected to DC grids mainly require voltage control, in contrast to the more complex connection requirement to AC systems, where voltage amplitude, frequency and phase of all sources must be carefully synchronized [12]. Circuit diagrams of generalized AC and DC microgrids are illustrated in Figure 2.1, to illustrate the simpler conversion requirements when interconnecting a variety of loads and sources to DC grids.

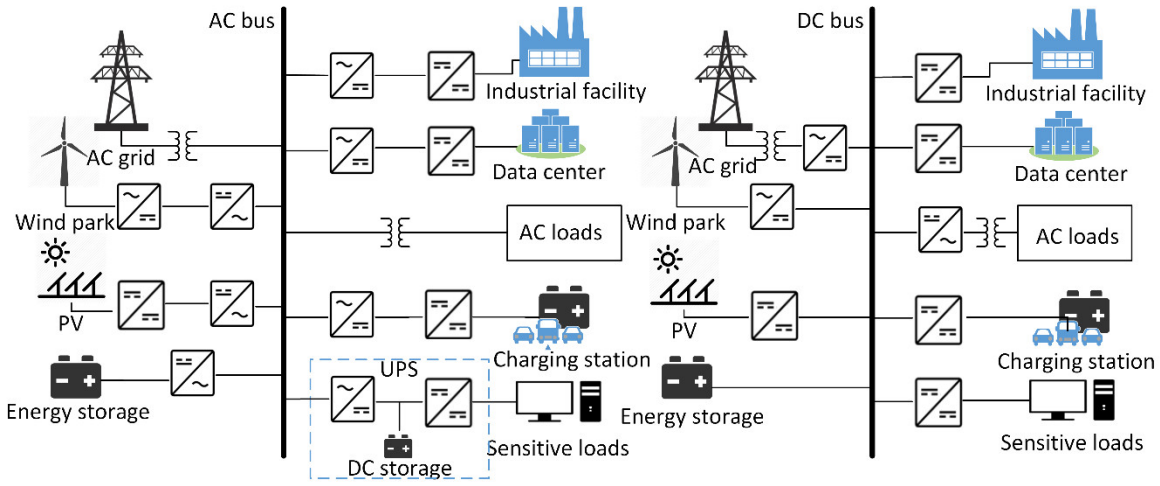

Figure 2.1 Schematic of a generic AC and DC microgrids

2.2 The Electrical System under consideration

Figure 2.2 shows the circuit schematic of the simplified LVDC microgrid considered for this thesis. The system comprises the most typical components found in microgrids, such as generators, AC grids, converters, motors and energy storage. Each electrical component is connected to a DC distribution network through a specifically designed converter. When modelling the microgrid used for simulations, the grid is divided into three isolated systems, as shown in Figure 2.2, including rectifier, inverter and battery systems. This section introduces these three systems. The considered load is assumed to absorb 250 kW, via a DC line voltage of 1000 V.

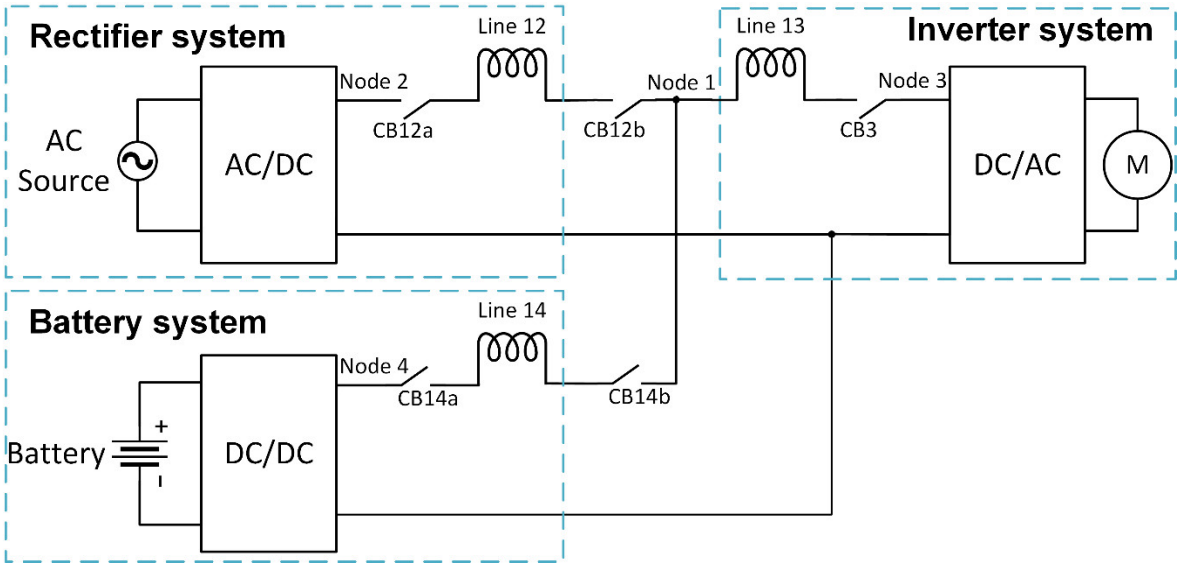

Figure 2.2 Considered LVDC microgrid schematic

2.2.1 Rectifier System

As seen in Figure 2.2, the rectifier system comprises an AC grid or generator. It is considered to be the main power supplier for the load, and must be able of delivering 250 kW to the grid through an AC/DC conversion converter. For simplicity, this thesis will consider one three-phase AC source coupled to the DC network through a 2-level full-bridge rectifier. Figure 2.3 depicts the schematics of the rectifier system.

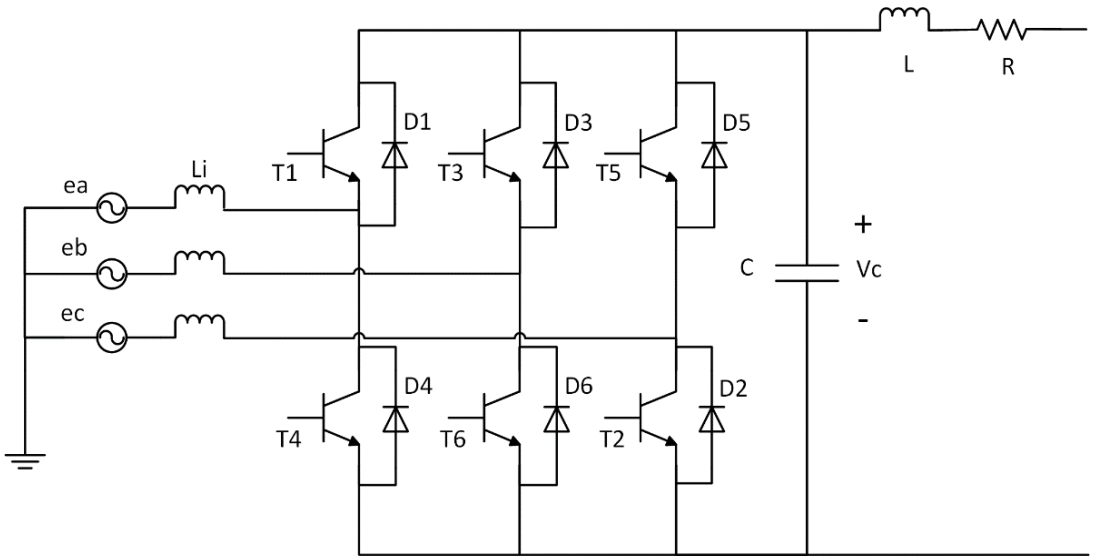

Figure 2.3 Schematic of AC source and rectifier

The full bridge comprises six valves of IGBT with parallel connected freewheeling diode, controlled by PWM technique to obtain a flexible controlling and reduce the harmonics [2] A PWM signal generator compares a reference waveform to a triangular carrier waveform, with a relationship ratio defined as modulation index *m* [21]. The relationship between the input and output voltage may be expressed as [21]:

$$\sqrt{2}V_{LL} = \sqrt{3} \cdot m \cdot \frac{V_{do}}{2} \tag{2.1}$$

$$V_{LL} = 0.612 \cdot m \cdot V_{do} \tag{2.2}$$

where

V_{LL} rms value of line-line voltage at AC side of converter [V];

V_{do} output voltage at the DC side of the converter [V];

m modulation index.

Using this equation, the values of the phase voltage $V_{\varphi,source}$ and the modulation index *m* were selected as 560 V and 0.9, respectively, in order to achieve a DC output voltage of approximately 1000 V.

2.2.2 Inverter System

A wye-connected three-phase reactive load consuming 250 kW is considered for the microgrid. The load is fed AC power through a 2-level full-bridge inverter. The schematic of the load and inverter is presented in Figure 2.4.

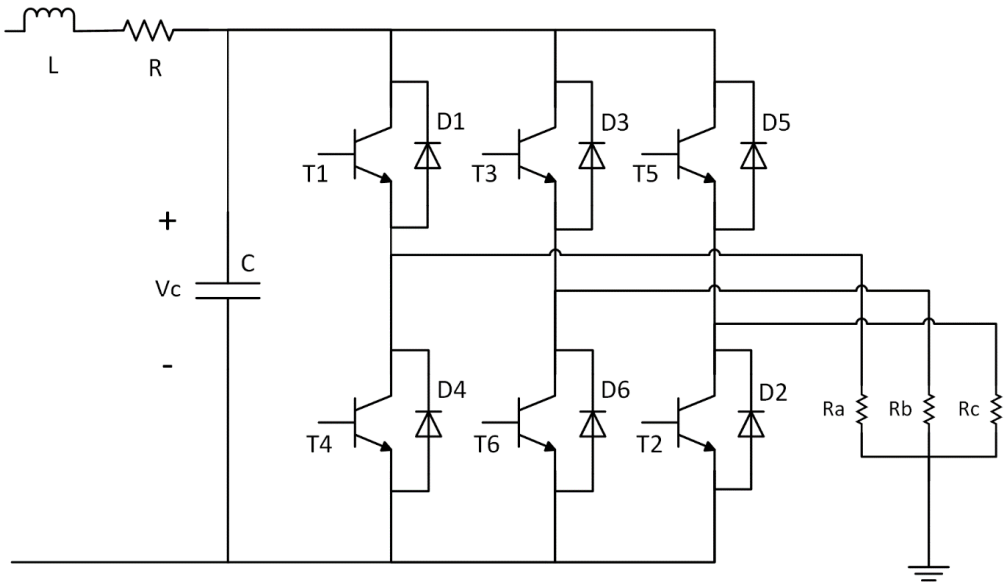

Figure 2.4 Schematic of load and inverter

The switching of the IGBT valves is controlled through a PWM generator. Consequently, the relationship between input and output voltage to be similar to that of the rectifier. Using Equation (2.2), a modulation index m of 0.9 results in a phase voltage $V_{\varphi,load}$ of 560 V. A resistive load of 2 Ω was selected, to obtain a DC current flow of 250 A.

2.2.3 Battery System

A variety of renewable resources, such as wind power and solar cells, are required to be combined with other energy or storage systems due to their typical inconsistent power generation. Implementing storage systems to networks containing DER systems, improves the quality and the security of the delivered power. Storage systems guarantees continuous power supply during short-duration power interruptions, by operating as emergency supply [22]. Due to reverse power flow occurring during charging process, the system must be capable of operating at rated current and power of 250 A and 250 kW in either direction. This thesis considers a battery able of producing a voltage of 500 V, interconnecting the DC distribution network via a DAB IBDC, introduced in [23]. This converter comprises two 2-level full-bridges on both sides of a high frequency transformer enabling bidirectional power flow. The transformer provides voltage matching between the voltage levels and galvanic isolation, which prevents current path between the battery and the grid [24]. Utilizing high frequency transformers over line-frequency transformers are preferable due to smaller physical components, higher power density and efficiency, and improved power-transmission capability [24]. Figure 2.5 shows the proposed converter schematic.

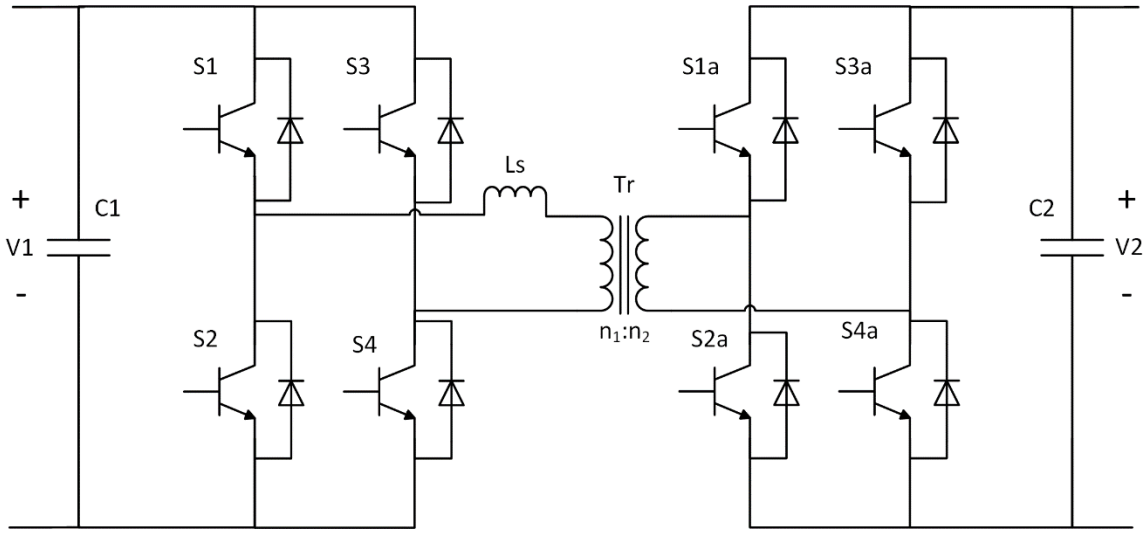

Figure 2.5 Schematic of dual active bridge isolated bidirectional DC-DC converter

The switches *S1*, *S4* and *S2*, *S3* are controlled complimentarily, with constant switching frequency f_s of 20 kHz, resulting in high frequency square waves. The switches are switched with a duty cycle of 0.49, to prevent short-circuiting the switches in the same leg, thus eliminating deadtime.

There are several strategies of controlling the power flow of DAB IBDCs survived in [24]. This thesis considers the simplest controlling strategy, where the direction and magnitude of the transferred power is controlled by phase-shifting the triggering signals of the two full-bridge converters. Assuming power flow from the primary to secondary side while neglecting losses, the transferred power of the system for traditional phase-shift control is expressed in [24] as:

$$P_{DCDC} = \frac{\frac{n_2}{n_1} V_1 V_2}{2\pi f_s L_s} \phi \left(\frac{\pi - |\phi|}{\pi} \right) \tag{2.3}$$

where

P_{DCDC} transferred power [W];

n_2/n_1 turns ratio of the transformer;

f_s switching frequency [Hz];

V_1 primary voltage [V];

V_2 secondary voltage [V];

L_s equivalent leakage inductance of the transformer [H];

ϕ phase-shift [-π/2, π/2] [rad].

For a positive phase-shift, the switching signals of the left bridge leads the switching signals of the right bridge, and vice versa for a negative phase-shift. The equation shows how the phase shift controls the power flow, such that maximum power is transferred at $\phi = \pi/2$, while no power flow occurs at $\phi = 0$, and maximum power is transferred in the opposite direction at $\phi = -\pi/2$ [25]. The chosen controlling strategy has some flaws regarding ZCS and ZVS, which accounts for power losses, consequently reducing the efficiency of the converter [24].

The auxiliary inductance L_s shown in Figure 2.5, is the equivalent leakage inductance of the transformer, and serves as the instantaneous energy storage device. The primary side is assumed perfectly stiff with a voltage source of 500 V, and the transformer ratio n_1:n_2 is selected to be 1:2.2 to make up for the minor voltage drop over the switches and the external inductor. The auxiliary inductance is calculated using Equation (2.3), such that maximum power transfer of 250 kW, occurs at a phase shift of π/2 rad. By deriving for L_s in Equation (2.3), the value of the equivalent transformer inductance is found:

$$L_s = \frac{nV_1V_2}{8f_sP_{DC\_MAX}} \tag{2.4}$$

$$= \frac{2.2 \cdot 1000V \cdot 500V}{8 \cdot 20kHz \cdot 250kW} = 27.5\ \mu H.$$

2.2.1 DC Distribution Lines

The voltage potential of the considered distribution system is 1000 V. For simplicity, all the distances between each nodes are considered to be equal, at 40 m. Since all systems must be able of delivering rated power to the load, all lines must be capable of conducting 250 A. This section will briefly present the line resistance and inductance of conducting wires.

Line resistance accounts for active power loss, which eventually converts into heat, subsequently increasing the temperature of the conductor [21]. If a conductor is exposed to an overload condition over a long period of time, the expected lifetime of the conductor is significantly decreased due to thermal derating [26]. The maximum allowed current density j is usually 4 A/mm^2 for wires isolated from air, and 6 A/mm^2 for wires in free air, limiting the minimum cross section of a cable [27].

Every conducting material experience some self-inductance. The self-inductance of a single wire in free space is expressed in [28] as:

$$L_{line} = 2 \cdot l \left\{ \ln\left(\left(\frac{2 \cdot l}{d}\right)\left(1 + \sqrt{1 + \left(\frac{d}{2l}\right)^2}\right)\right) - \sqrt{1 + \left(\frac{d}{2l}\right)^2} + \frac{\mu}{4} + \left(\frac{d}{2l}\right)\right\} \quad (2.5)$$

where

L_{line} total inductance of conductor segment [H];

l length of cable [cm];

d conductor diameter [cm];

μ permeability [H/m].

By using equation (2.5), the line inductance L_{line} of a 40 m wire segment conducting 250 A, with a maximum current density of 6 A/mm^2, is found to be 74.3 µH. Calculations are given in Appendix A.

Due to the non-altering current and voltages waveforms of DC operations, the line inductance has minor influence of the steady-state operations. It is merely under transient conditions that line inductance accounts for major system impact. The effect of this system element will shortly be discussed in Chapter 3 concerning the impact of short-circuit faults in LVDC systems.

2.3 Considered Electrical System Parameter Summary

The following table summarizes the considered system parameters discussed in this chapter, which will be used during modelling in Simulink.

Table 2.1 Electrical system parameters and values

Parameter	Value
DC distribution network voltage, V_{DC}	1000 V
Line length, l_{12}, l_{13}, l_{14}	40 m
Line inductances, L_{12}, L_{13}, L_{14}	74.3 µH
Nominal current I_o	250 A
Nominal power, P_o	250 kW
AC source phase voltage, $V_{\varphi,source}$	560 V_{rms}
AC load phase voltage, $V_{\varphi,load}$	560 V_{rms}
Modulation index, m	0.9
Load resistance, R_{load}	2 Ω
DC battery voltage, $V_{battery}$	500 V
Equivalent transformer leakage inductance, L_s	27.5 µH
Transformer ratio, n_1:n_2	1:2.2

3 Fault in DC Microgrids

This chapter introduces the key aspects of faults occurring in DC microgrids, and presents a list of requirements which the CB must meet in order to obtain reliable operation.

3.1 Critical Aspects of Fault in DC Microgrids

Dissimilar to faults occurring in AC grids, the faults occurring in DC grids are most likely permanent due to their causing conditions, which is typically cable insulation deterioration or breakdown [29]. Figure 3.1 illustrates the two possible faults occurring in a DC grid with two pole configuration, pole-to-ground and pole-to-pole faults. Pole-to-ground faults are more likely to occur, while pole-to-pole faults accounts for greater damage the system [30]. This thesis considers a short-circuit fault with a short-circuit resistance of 1 mΩ, which has previously been used in studies referred to in [31, 32].

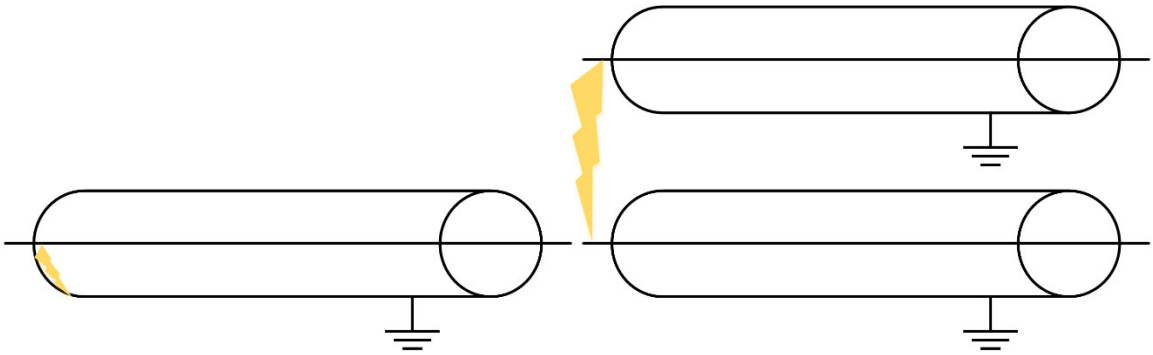

Figure 3.1 Types of DC faults. Left: pole-to-ground fault, right: pole-to-pole fault

Figure 3.2 illustrates the current flow during a fault on the DC side of a three-phase VSC system. Once the fault short-circuits somewhere at the DC lines, the DC link capacitor immediately starts to discharge through the fault, increasing the line current [14]. After the protection system recognize a fault, the IGBT valves are usually blocked for their own protection [29]. The current is forced to flow through the freewheeling diodes, causing the converter to operate similar to that of an uncontrollable diode rectifier, subsequently allowing the AC source to directly feed the fault [33].

Once the IGBT valves are blocked, the output voltage may be considered as an output voltage of an three-phase diode rectifier [21]:

$$V_{do} = \frac{3}{\pi}\sqrt{2}V_{LL} = 1.35V_{LL} \tag{3.1}$$

Diodes can only tolerate a maximum surge current for a limited period of time before being vulnerable to total component destruction [21]. For a given component, manufacturers usually provide its capability of handling short-circuits, in terms of duration and maximum surge current. It is crucial for the protection system to properly isolate and interrupt the fault rapidly, to limit the risk of overriding the short-circuit capability of the system components [1].

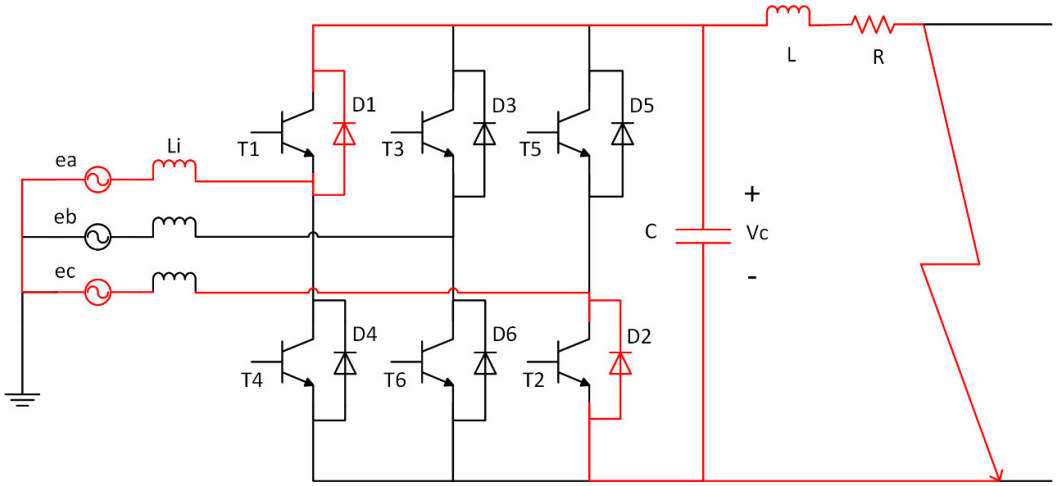

Figure 3.2 A three-phase VSC with its DC bus short-circuited

3.1.1 Effect of Line Inductance

Inductors subjected to a change of current induces a back EMF according to Faraday's law [21]:

$$\frac{V_{line}}{L_{line}} = \frac{di_{line}}{dt} \tag{3.2}$$

where

V_{line} voltage drop over line segment [V];

i_{line} line current waveform [A].

After a system with inductive elements is short-circuited, the resulting rise of fault current is found to be an inversely proportional to the inductance seen from the fault. DC systems lack large inductance sources, such as large synchronous machines and transformers, which typically provides bulky inductances in AC systems [1]. When accounting the typically short wire length of LV systems [1], LVDC systems experience significantly steep rise of fault currents. The typically slow operating MCBs applied in DC protection applications, may result in excessive peak currents. All electrical components of the system must be dimensioned to withstand the possible peak current occurring during worst case faults, increasing the size and

installation cost for the system [1]. The low inductance stresses the need to develop a CB able of breaking the fault within a few microseconds, in order to avoid excessive peak currents.

Figure 3.3 shows a circuit schematic of a CB implemented in a simplified DC destitution system, subjected to a fault short-circuiting the load.

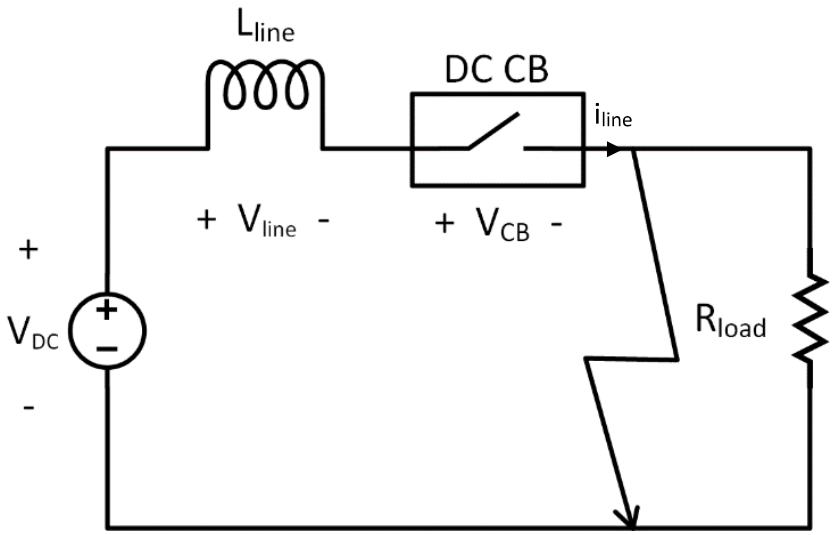

Figure 3.3 Simplified DC distribution system during fault

Another important consideration, which must be addressed when designing the CB, is that once the current is broken and reduces to zero, the line induces a negative overvoltage, defined as TIV, according to equation (3.2). Utilizing circuit analysis of Figure 3.3, the voltage potential across the CB may be expressed as:

$$V_{CB} = V_{DC} - V_{line} \tag{3.3}$$

The CB must be able of handling the TIV arising due to negative current flow. MOVs may be exploited to protect the CB components from TIV by providing sufficient counter voltage, clamping the voltage to sustainable levels [34]. The level of necessary clamping voltage is found by combining Equation (3.2) and (3.3), to derive an expression for the rate of fault current rise:

$$\frac{di_{line}}{dt} = \frac{V_{DC} - V_{CB}}{L_{line}} \tag{3.4}$$

In order for the current to decrease to zero, this equation must be negative. This can only be achieved if the MOV clamps a counter voltage greater than the DC source voltage V_{DC}:

$$V_{CB} > V_{DC} \Rightarrow \frac{di_{line}}{dt} < 0 \tag{3.5}$$

Before the fault is interrupted, the inductor elements of the lines are magnetized with fault energy. The accumulated energy in the lines may be expressed as [21]:

$$W_{line} = \frac{1}{2} L_{line} I_{fault}^2 \tag{3.6}$$

where

W_{line} fault energy stored in line inductance [J];

I_{fault} peak fault current before being broken [A].

During breaking operation, the lines releases this energy, subsequently allowing the current to fall to zero. This energy must be properly absorbed and dissipated without destroying components in the system. MOVs are also utilized as energy absorbing commutation paths, demagnetizing the lines after the fault current is broken [34].

3.2 Loss of Power Transfer

Loss of power transfer is conceived as rather expensive and should be avoided if unnecessary [30, 35]. It is important that networks comprises several CBs, such that only the CBs closest to the fault are triggered, thus allowing normal operation for the healthy part of the network. Before any CBs are triggered, a selective fault detection method must be performed, which distinguishes the faulty line from the healthy part of the network, and subsequently trigger only the preferable CBs capable of isolating the fault [30, 35, 36]. A study performed in [37] surveys several types of detection methods utilized for DC protection. The methods are mostly based on measuring and analysing changes in voltage, current and direction of current, and detecting the incident of traveling waves caused by faults [38].

As illustrated for the microgrid under consideration depicted in Figure 2.2, two CBs are installed at nearly every branch in the network to guarantee successful isolation of a short-circuit faults [1]. For cases where faults occurs somewhere on line 1-2, only CB12a and CB12b must to be triggered to properly isolate the fault. The rectifier system will then be isolated from the rest of the network, allowing the battery to deliver power to the load until normal operation may be restored. Figure 2.2 show that for branches connected to loads, one CB implemented close to the inverter is sufficient to allow the rest of the network to continue operation. If a fault

appeared somewhere on line 1-3, only CB3 must be triggered, allowing the AC source to charge the battery.

3.3 DC Circuit Breaker Requirements and Implementation to the Microgrid

There are mainly six requirements which the protection system must address in order to sufficiently protect the considered DC microgrid. The first four requirements are discussed in [1], while the two last requirements are added for the considered DC microgrid.

1. **Low conduction losses.** The CB operates at normal conditions and conducts large currents for the majority of time. To avoid excessive power losses, the on-state resistance and voltage drop of the CB should be minimized.
2. **Fast switching operation.** The interrupting period of the CB should be kept small in order to limit peak fault current, thus avoiding thermal destruction and overrated system components.
3. **Force the current to zero.** The CB must be capable of forcing the current down to zero, by switching itself to blocking-state, producing a counter voltage larger than the DC system voltage and dissipating the magnetic energy stored in the lines.
4. **Withstand a high voltage stress during breaking operation.** The CB has to withstand TIV occurring during the breaking process.
5. **Bidirectional interrupting capability.** The introduction of storage systems introduces bidirectional current flow. The CB must be capable of conducting and interrupting currents in either directions.
6. **Detective system with selective coordination operation.** Loss of power transfer accounts for major expenses and should be avoided if unnecessary. CBs must be installed at nearly all ends of each DC line, and the protection system must perform a selective coordination operation, which allows the healthy parts of the network to resume normal operation without interruption.

4 Operating Principles of Breaker under consideration

This chapter introduces the basic operating principles of the CB under consideration. Guidelines will be assembled for the components comprising the considered CB to be used for parameterization and simulation.

4.1 Presentation of considered Circuit Breaker

A variety of CB proposals were presented and compared in [1]. The most promising concept from this thesis was concluded to be a bidirectional SSCB based on two newly developed 2.5 kV rated RB-IGCTs from ABB, introduced in [39]. The concept provides favourable qualities such as bidirectional interrupting capability, high voltage ratings, superior fault current interrupting capability, low conduction losses, and simple circuit design. Figure 4.1 depicts the circuit diagram of the proposed SSCB. The state of the RB-IGCT is controlled via proper gate-emitter voltage control. RB-IGCT conducts only in the forward direction and is able of blocking voltages in both forward and reverse directions. Two RB-IGCTs are connected in anti-parallel, realising two breaker branches, ensuring bidirectional conducting and interrupting capability. The SSCB is capable of conducting 1 kA with power losses below 1 kW, thus achieving an efficiency of 99.9 % for the 1 MW rated DC system considered in [39]. The proposed SSCB design is reported of successfully breaking fault currents up to 6.8 kA at 1.6 kV within 150 µs after being triggered, and dissipate the residential energy within 38 ms [39].

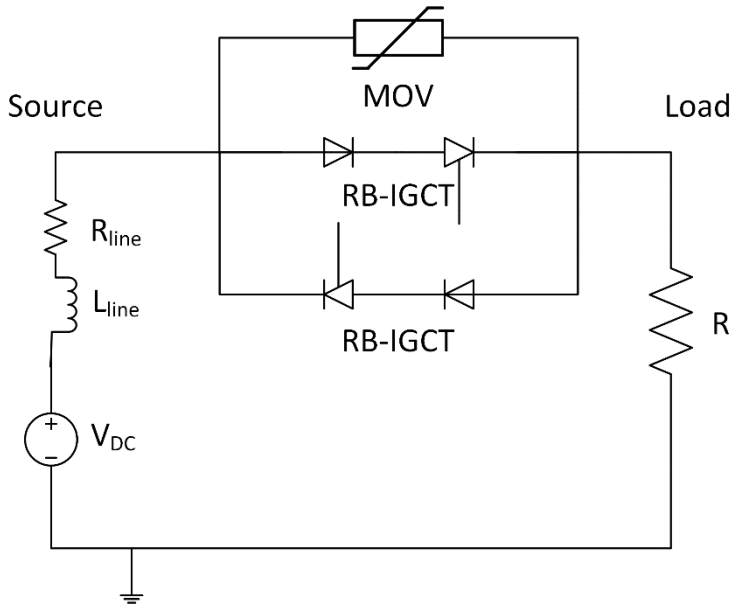

Figure 4.1 Block diagram of RB-IGCT based CB

4.2 Circuit Breaker Operating Times

This section presents the different operation periods of the CB. Figure 4.2 illustrates the line current and CB voltage waveforms for a typical SSCB during fault interrupting process.

The time prior to t_1 represents normal operations. The forward conducting branch of the CB conducts the nominal current I_o with an on-state voltage drop V_{ON} depending on the on-state characteristics of the semiconductor devices in the conducting branch [1].

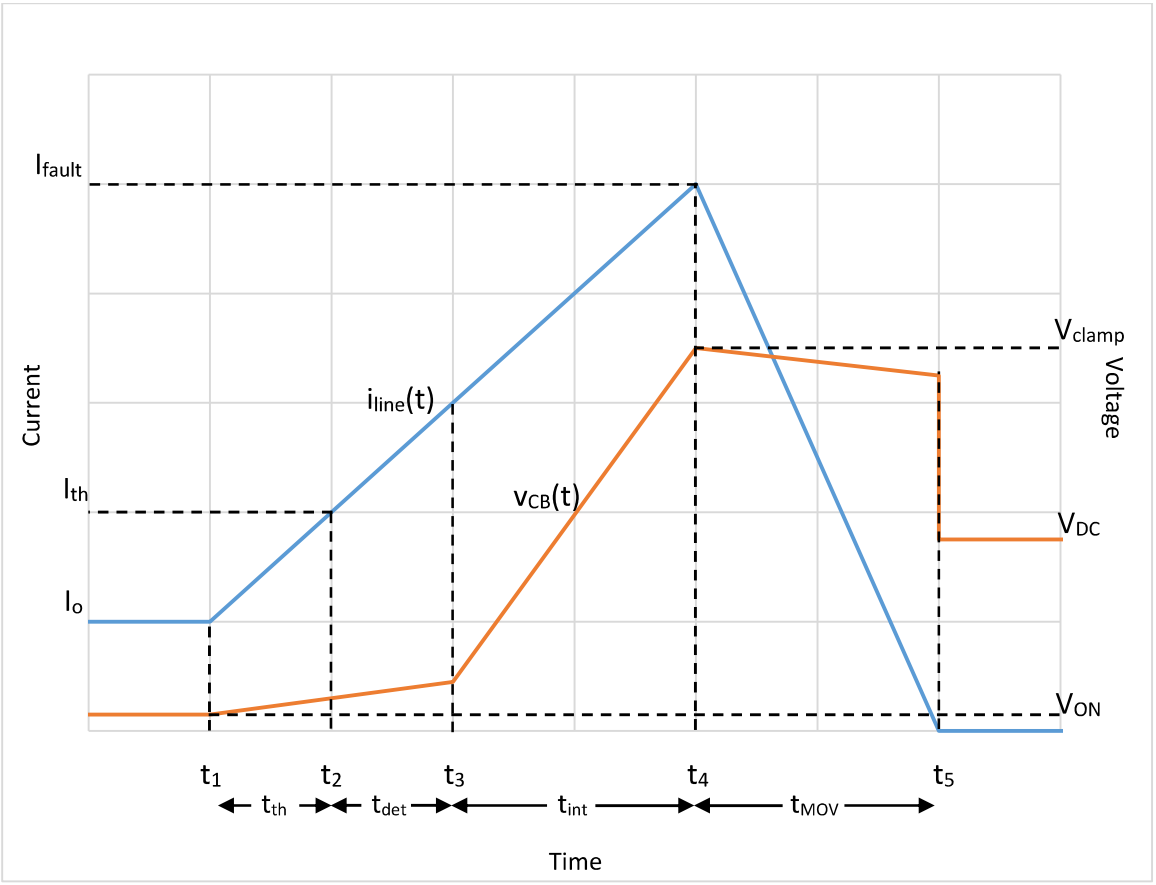

Figure 4.2 Generalized interrupting process for a typical solid state circuit breaker showing the line current and CB voltage waveforms

4.2.1 Threshold Time

After a short circuit fault has been applied to the system at t_1, the current in the system starts to increase according to Equation (3.2) undetected. As discussed in Chapter 3.2, loss of power transfer is considered expensive, and should be avoided if unnecessary [30, 35]. It is beneficial to trigger the protection system only after the current has reached a specific threshold value I_{th}. The threshold current is usually chosen in the range of 1.2-10 p.u., depending on the several factors in the considered network, such as nominal load current, system inductance, voltage source and its current sensitivity [6, 40, 41]. The threshold time t_{th} is the period of time the fault current uses to reach a threshold current I_{th}, which activates the protection driver of the CB [1].

The threshold time is the only controllable time period, prior of breaking the current at t_4. A low threshold current allows the CB be triggered faster, which limits the peak fault current. However, the threshold current should be sufficiently large in order to avoid unnecessary tripping of the CB, caused by oscillations due to normal load operations. This thesis recommends a threshold current of 2 p.u. for the considered microgrid.

The threshold time period is found by deriving Equation (3.2) and assuming constant current rise during the initiation and the breaking of the fault, as shown in Figure 4.2:

$$\frac{\Delta \mathrm{I}}{\Delta t} = \frac{V_{DC}}{L_{line}}, t_1 \leq t \leq t_4 \tag{4.1}$$

During the initiation of the fault at t_1 and detection of the overcurrent condition at t_2, the current increases from I_o, towards the selected I_{th}. Accordingly, the threshold time period may thereby be expressed as:

$$t_{th} = \frac{(I_{th} - I_o)}{\frac{V_{DC}}{L_{line}}} \tag{4.2}$$

4.2.2 Detection Time

A selective fault detection method is carried out after a fault has been recognized, in order to assure only the CBs closest to the fault are triggered. The extra time period arising due to the computation and communication of the data is defined as the detection time period t_{det} of the protection system. This time period is shown in Figure 4.2 as time period between overcurrent condition recognition at t_2 and initiation of fault current restriction through the main breaker, at t_3. This period is determined by the ability of CBs to coordinate with or support one another [36, 42]. The type of protection method influence the detection period of the breaking operation.

The lack of standards for LVDC protection systems, is reflected by the variation of information regarding detection time periods found in literature. A study in [43] mentions that a typical time-frame of a fault detection decision-process and fault detection time is in the range of 3-10 ms, for a LVDC microgrid. ABB has reported a CB for LV applications with total detection time less than 1 ms [44]. Littlefuse has manufactured relays, which are reported of detecting arcing conditions and sending tripping signals to CBs in less than 1 ms [45]. Linear Technology Corporation mentions typical trip delays of 1 ms [40]. Siemens has manufactured several SSCB constructed for DC applications with an opening delay of maximum 1 ms [46]. Several papers studying protection schemes for CB in DC applications have a tendency to

introduce a detection periods of 1 ms [6, 47-49]. There are also reported studies with detection periods of 2 ms in [18], and smaller detections delay of 18 µs in [50].

Due to most studies utilizing 1 ms as detection time period, it is assumed that this period of time is sufficient to perform selective fault detection and generate sufficient activation signal to activate the preferred CBs. A shorter detection period results in increase worker safety, less fault damage, and improved uptime. In complex systems, additional delays as a resulting from transporting signals across the lines must be accounted for [47]. This will however be excluded from this thesis, due to short wire distances.

4.2.3 Interrupting Time

The time period between the CB is triggered at t_3, to the fault current reaches its peak I_{fault} at t_4, shown in Figure 4.2, is referred to as the interrupting time period t_{int}. During the interruption time period, the semiconductor in the main path turns off, subsequently forcing the fault current to commutate towards the MOV. The duration of this period is dependent by the turn off characteristics of the semiconductor device comprising the CB. The voltage drop across the CB increases due to increased current commutating towards the MOV.

This thesis will assume a threshold time period equal to that of the most promising CB, of 150 µs [39]. The interruption time period is assumed constant, and therefore independent from type of semiconductor or level of peak fault current.

4.2.4 Energy Dissipation Time

Observed in Figure 4.2, the fault current reaches its peak and begin to reduce after the commutation process is completed at t_4. The time period between t_4 and t_5, where the lines are demagnetized by the MOV, successfully reducing the current to zero, is defined as energy dissipation time t_{MOV}. During this time period the MOV clamps the voltage at V_{clamp} to protect the CB components against TIV induced by the line inductances. The duration of the period depends on the level of the counter voltage of the MOV, the peak current I_{fault} and line inductance L_{line}.

If the clamping voltage is assumed constant during energy absorption period, the time period may derived from Equation (3.3):

$$t_{MOV} = \frac{L_{line} \cdot I_{fault}}{V_{clamp} - V_{DC}} \tag{4.3}$$

In real cases, the clamping voltage will decrease slightly as the current through the MOV decreases, subsequently increasing the energy dissipation period.

4.3 CB Components Considerations

The goal of this thesis is to construct an economical bidirectional CB, capable of rapidly interrupting fault currents occurring in a considered LVDC distribution grids, while attaining low conduction power loss during normal operation. This section presents important considerations of the components.

4.3.1 Semiconductor Devices

The semiconductor device is the main breaking component in the CB which actively restrict the fault current when triggered. The type of semiconductor device influence the cost and size of the resulting CB, in addition to its performance during both normal and fault operations. Fast switching is favourable in order to limit the peak current during short-circuit faults. The on-state resistance and voltage drop of the semiconductor should be minimized in order to optimize the on-state performance of the CB.

Large voltage ratings of the CB allows utilization of MOVs which are capable of clamping higher voltages during the energy dissipation process, which enables shorter energy dissipation period as seen by observing equation (4.3). The voltage ratings of the CB may be increased by either utilizing semiconductor devices with large voltage ratings, or series connecting several semiconductor devises. The conduction loss of the CB increase proportionally to the number of series connected semiconductor devices of the CB. Due to the fact that high conduction loss is one of the major disadvantages of SSCB [1], one series connected device per breaker path is selected to be a restriction for this thesis. For higher voltage systems, it is necessary to increase the number of series connected devices [1].

Manufacturers provide the maximum controllable turn-off current I_{CRM} for a given semiconductor device in datasheets. A single semiconductor device is probably not able to interrupt the maximum fault current I_{fault} which may occur during short-circuit faults in the considered microgrid. The current interrupting capability of the CB is increased, by parallel connecting several semiconductor devices for each breaker path. The number of required parallel connected devices M per breaker path is found by comparing the prospective fault current I_{fault} to the maximum controllable turn-off current I_{CRM} for a given semiconductor:

$$M = \frac{I_{fault}}{I_{CRM}} \tag{4.4}$$

where

M number of parallel connected power device per breaker path;

I_{fault} possible peak fault current [A];

I_{CRM} maximum controllable turn-off current per power device [A].

It may be beneficial to consider semiconductor devices with high I_{CRM} in order to limits the total number of semiconductor devices, thus minimizing the size and cost of the resulting CB.

The datasheet of the 2.5 kV rated RB-IGCT from ABB, comprising the original CB proposed in [39], is currently unavailable for commercial use. The only commercially available RB-IGCT from ABB is rated 6.5 kV [51]. Utilizing power devices with voltage ratings of that level might be considered as unnecessary bulky and expensive for the considered 1000 V DC microgrid. Other types of IGCT from ABB may be considered. A-IGCTs are available with ratings of 4.5 kV and large current interrupting capability, and will be considered for parameterization [52]. Replacing IGCTs with IGBTs will also be considered due to their wide commercial availability, ruggedness, speed and simpler gate drive [48]. A study in [53] compared the performance of the two semiconductor devices for CB applications. Although the IGCTs exhibits somewhat longer turn-off periods, the main conclusion from the study is that IGCTs have favourable characteristics for voltage ratings beyond 2000 V. This assertion will be considered when selecting the promising models when conducting parameterization in chapter 4.

WBG based semiconductor devices offers several material properties which are found adventurous for utilization in CB applications, such as fast switching, efficient heat dissipation, low conduction losses, high power density capability, and high temperature capability [1]. It has been reported that once WBG based semiconductor technology becomes mature, they will replace traditional silicon based semiconductors in protection systems [48, 54, 55]. SiC power devices offer material properties which suits ideally in the use of CB applications, such as being capable of fast switching, conducting high power density with low losses, and efficient heat dissipation. The CBs based on SiC power devices are currently in an early stage of development, and suffers from several factors such as high device costs, insufficient current capability in addition to concerns regarding their reliability [1, 14, 56]. More research is

necessary before SiC based CBs are commercial competitive. More research on this subject is required before WBG technology in CB applications are commercial competitive.

4.3.1.1 Semiconductor Conduction Loss calculations

The conduction losses of both IGBT and IGCT are calculated using the same method. Current conducting semiconductor devices are always subjected to on-state voltage drop V_{ON}, which results in power loss. The voltage drop of the semiconductor may be divided into a base threshold voltage V_{th}, which is normally provided by manufacturers in datasheets, and a voltage drop depending on the conducting current V_C [57]. The conduction loss of a semiconductor device is defined in [21] as:

$$P_{ON} = V_{ON} I_C \tag{4.5}$$

$$= (V_{th} + V_C) I_C \tag{4.6}$$

where

P_{ON} conduction loss [W];

V_{ON} voltage drop of the semiconductor device [V];

V_{th} threshold gate emitter voltage [V];

V_C voltage drop when conducting current I_C [V];

I_C collector current [A].

Transconductance g_m measure the sensitivity of collector current I_C to changes of collector-emitter voltage V_{CE} [58]. g_m is nonlinear and is found from partial derivation of the VI-characteristics provided by the manufacturers for given semiconductor devices:

$$g_m = \frac{\partial I_C}{\partial V_{CE}} \tag{4.7}$$

where

g_m transconductance [S];

V_{CE} collector emitter voltage [V].

A typical VI-characterization for a given IGBT is illustrated in Figure 4.3.

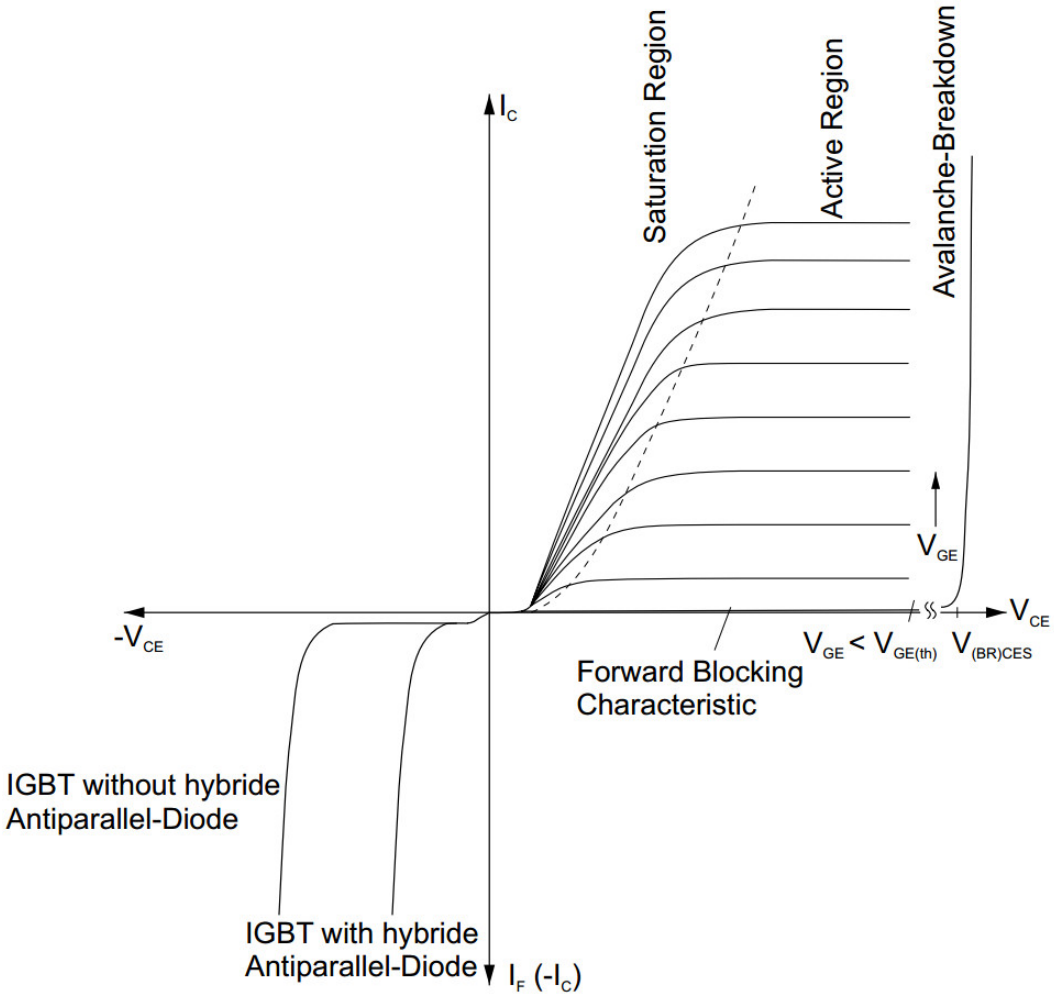

Figure 4.3 Current and voltage characteristics of a typical IGBT [59]

V_C depends on the transconductance g_m, such that for a given I_C, the conducting loss P_{ON} may be expressed as [21]:

$$P_{ON} = \left(V_{th} + \frac{I_C}{g_m}\right) I_C \tag{4.8}$$

Transresistance r_m is defined as the dual of transconductance. When the power device operates in its ohmic region, the transresistance may be linearized and defined as the on-state resistance R_{ON} [57]. Thus, the conducting loss of a single power device is derived as:

$$P_{ON} = V_{th} I_C + R_{ON} I_C^2 \tag{4.9}$$

The total conduction loss of a component comprising several power devices will increase proportionally to the number of power devices in series N, and decrease proportionally to the number of power devices in parallel, M.

Accordingly, the final formula for conduction loss of the CB may be expressed as:

$$P_{ON} = NV_{th}I_C + \frac{N}{M}R_{ON}I_C^2 \tag{4.10}$$

where

N number of power devices in series.

4.3.2 MOV Characteristics

MOVs are used in protection applications for systems ranging from low voltage circuits to high voltage systems apparatus [34]. MOVs are typically utilized to protect components against lightning surges, TIV and other overvoltages, by producing a counter voltage, as discussed in Chapter 3.1.1. They are also utilized as an auxiliary conducting path, which dissipates the magnetic energy stored in the line inductance of the system. Contrary to MCBs utilized for AC applications, SSCBs are incapable of dissipating the magnetic energy by the system itself, and are required to be implemented with energy absorbing components, such as MOVs [34]. MOVs are fundamentally nonlinear resistances, which only allows large currents to be conducted when subjected to voltage levels above a certain level, given by component datasheets by manufacturers. The non-linear VI-characteristics of a typical MOV is illustrated in Figure 4.4 [60].

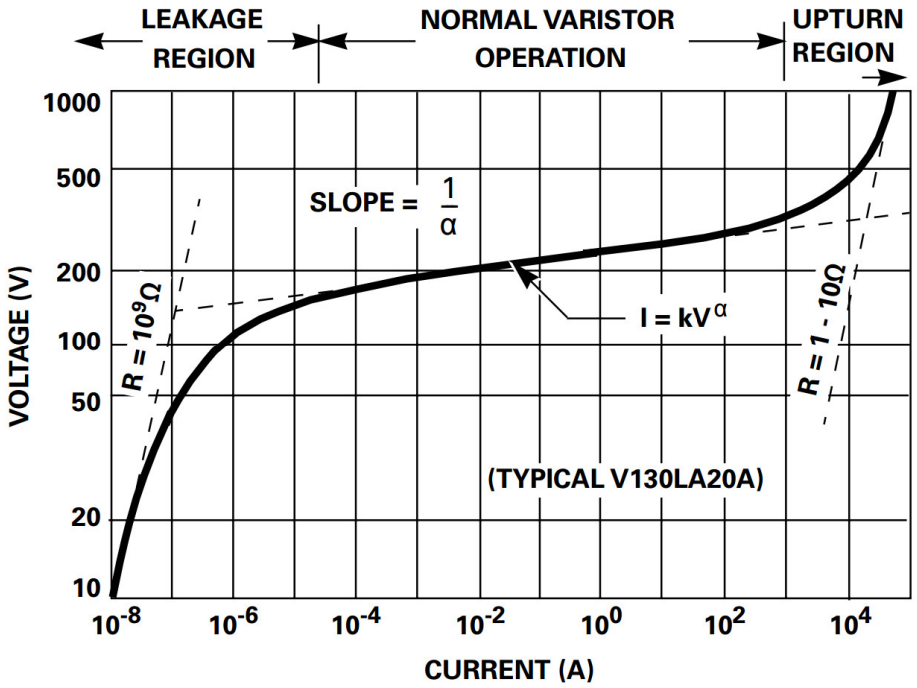

Figure 4.4 Typical VI-curve for a MOV plotted on log-log scale [60]

As illustrated in Figure 4.4, the VI-characteristics may be divided into three operation regions with gradual transition between them, including leakage region, normal varistor operation and upturn region [60]. When subjected to low voltage, the operation of the MOV is comparable to a large linear resistance, only allowing a small current to conduct through it, defining the leakage region. During normal varistor operation, a marginal increase of voltage, accounts for a high rise of current. The MOV operates in this region during energy dissipation periods. If the voltage potential over the MOV increases to beyond a certain level, linear properties are restored again and the MOV operate similar to a small resistance. This region should be avoided as it results in excessive heat generation, which may thermally destroy the component [60]. The VI-characteristics of a given MOV is provided by its manufacturers in datasheets.

For all regions the VI-characteristics may be expressed as:

$$I_{MOV} = KV_{MOV}^{\alpha} \tag{4.11}$$

where

I_{MOV} current conducing in MOV [A];

V_{MOV} voltage potential over MOV [V];

K ceramic material constant [S];

α non-linearity exponent.

The energy absorbing capability of the MOV depends on its VI-characteristics, and the period of time, which the MOV requires to properly dissipate the fault energy, t_{MOV}. The energy absorbed by a MOV during breaking operation may be expressed as [60]:

$$W_{MOV} = \int^{t_{MOV}} v_{MOV} \cdot i_{MOV} \cdot dt \tag{4.12}$$

where

W_{MOV} energy absorbed by the MOV [W];

t_{MOV} energy dissipation time [s];

v_{MOV} voltage drop over the MOV during current flow [V];

i_{MOV} current flow through MOV [A].

Manufacturers provide the maximum allowable energy absorption capability W_{MOVmax}, maximum component temperature, T_{MOVmax} and maximum average power dissipation P_{MOVmax}

for a given MOV, which if exceeded, important MOV properties are lost, and the possibility of device destruction increases, thereby limiting the expected lifetime of the device.

4.4 Thermal Considerations

During faults, the excessive fault currents within the semiconductor devices in the main conducting path leads to excessive conduction loss P_{ON}, which produces heat, subsequently increasing the temperature. If the component junction temperature, also referred as the intrinsic temperature T_j, surpasses a certain level, preferable characteristics are lost, such as low conduction loss and current breaking capability. If not adequately addressed, high temperatures may lead to the device being thermally destroyed [21]. The maximum allowable operating intrinsic temperature $T_{j,max}$ for a given semiconductor device, is provided by manufactures in component datasheets. Addressing temperature limitation of the device is proceeded by installing proper cooling systems which conduct the heat away from the critical components, allowing it to operate at optimal temperatures.

This section presents simplified circuit models emulating dynamic and steady-state characteristics of one dimensional heat transfer of semiconductor devices.

4.4.1 Thermal Resistance

Every segment of material with a temperature difference ΔT, exhibits heat dissipation P_{cond} from the side with the highest temperature towards the side with lower temperature. The conducted heat in terms of power per unit time through the considered segment may be expressed as [21]:

$$P_{cond} = \frac{\Delta T}{R_\theta} \tag{4.13}$$

where

P_{cond} conducted heat [W];

R_θ thermal resistance [°C/W];

ΔT temperature difference across the material [°C].

Thermal resistance R_θ is specific for each material, and determines how efficiently heat is transmitted through the material. Materials with small R_θ transfer heat efficiently and are used as cooling materials, while materials with large R_θ transfer heat poorly and are used as thermal insulation materials.

For the same considered segment of material, the follow equation applies:

$$P_{cond} = \frac{\lambda A \Delta T}{a} \tag{4.14}$$

where

λ thermal conductivity [W/m·°C];

a length of heat conduction path [m];

A cross-section area [m^2].

The equation shows the relationship between temperature rise, the physical form of the considered segment and amount of transferred heat.

By combining Equation (4.13) and (4.14), the thermal resistance may be derived as:

$$R_\theta = \frac{\Delta T}{P_{cond}} = \frac{a}{\lambda A} \tag{4.15}$$

The total thermal resistance between the junction and the case of a given semiconductor is often provided by the manufacturers.

4.4.2 Thermal Capacitance

Dynamic behaviour generates additional heat, which might rise the temperature towards critical values. The additional heat may be obtained by considering a heat capacitance C_θ analog to electrical capacitance. The heat capacity of a square shaped box of an arbitrary material may be expressed as [21]:

$$C_\theta = \frac{dQ}{dT} Aa \tag{4.16}$$

where

$\frac{dQ}{dT}$ heat capacity per unit volume [J/°C];

C_θ heat capacity [Jm^3/°C].

4.4.3 Thermal Circuit Models

The thermal behaviour of semiconductor devices can be described using equivalent electrical circuit models [61]. Heat conducts through layers composed of different layers of material each with specific $R_{\theta i}$ and $C_{\theta i}$.

Figure 4.5 shows the schematic of the Cauer model, which provides a real physical setup to the transient thermal equivalent impedance of an semiconductor [61]. It allows the exponential behaviour of the temperature during both steady state and the dynamic operation to be modelled as an electrical RC-circuit. The calculations are analog to electric circuits. For this model, $T_i(t)$ represents the voltage potential of that node, $P(t)$ represents current flow, and $R_{\theta i}$ and $C_{\theta i}$ represents electrical resistance and capacitance, respectively [21]. The model utilize multilayers to emulate the individual layers of the physical module, the first layer represents the junction and the last layer represents the case. The network nodes allows easy access to finding the internal temperatures of the layer sequence.

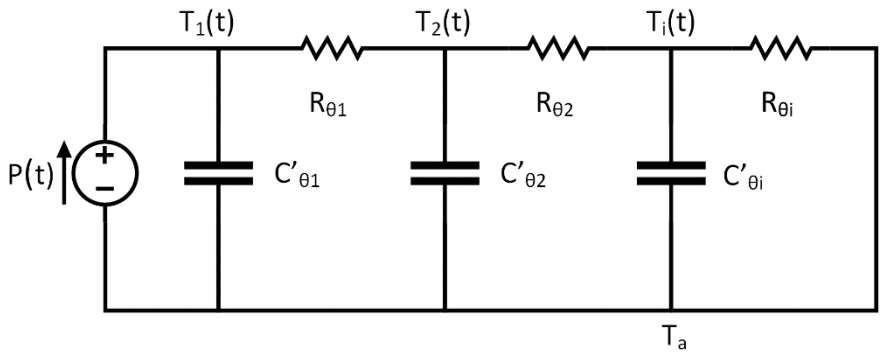

Figure 4.5 Schematic of a Cauer model

Cauer model is normally not used by components manufacturers, making it considerably complex finding all RC elements from datasheets. Component manufacturers typically use Foster model, which enables easier analytical calculations using RC-elements that do not represent the layer sequence. Figure 4.6 illustrates the schematic of the considered thermal model. The network nodes will no longer have any physical significance.

Simple analytical calculations are enabled by utilizing a transient thermal impedance that obtains the thermal transient behaviour into an exponential curve, expressed in [61] as:

$$Z_{\theta jc} = \sum_{i=1}^{n} R_{\theta i} \left(1e - e^{-\frac{t}{\tau_{\theta i}}} \right) \tag{4.17}$$

where

$\tau_{\theta i}$ thermal time constant [s];

$Z_{\theta jc}$ thermal impedance [°C/W].

The thermal impedance measures how efficiently the device dissipates heat. The coefficients used for this model are easily extracted from measuring a cooling curve of the considered module. Partial fraction coefficients are typically provided in datasheets in tabular form in pairs of $\tau_{\theta i}$ and $R_{\theta i}$ [61]. $C_{\theta i}$ is found by knowing the relationship:

$$\tau_{\theta i} = R_{\theta i} C_{\theta i} \tag{4.18}$$

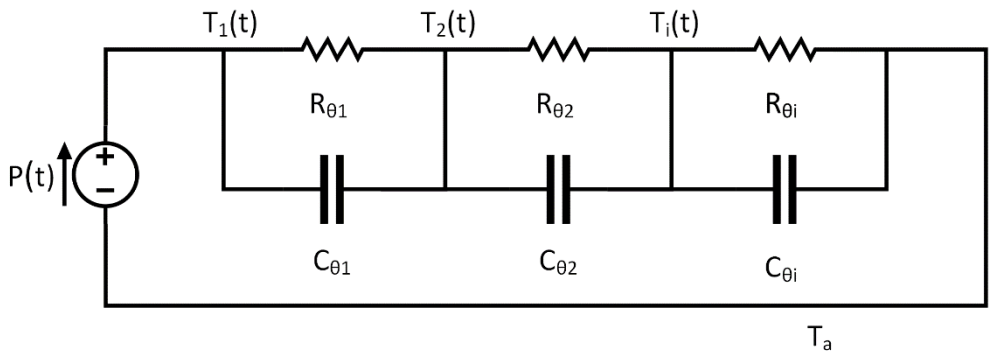

Figure 4.6 Schematic of a Foster model

4.4.4 Heat sink

The purpose of utilizing heat sinks is to realise an efficient conduction path for heat from the semiconductor device towards a cooling medium, such as ambient air [21]. Minimizing the thermal resistance between the junction and ambient $R_{\theta ja}$ allows more heat to be dissipated away from the device, allowing the device to operate at optimal temperatures. By studying Equation (4.15), it is found that a small $R_{\theta ja}$ is realised by limiting the heat conduction path and maximise its surface area in contact to the surrounding cooling medium.

The maximum allowable value of the thermal resistance of the heatsink $R_{\theta heatsink}$ is found by considering the maximum allowable thermal resistance of the heat conduction path $R_{\theta ja}$, where the component operates at its maximum intrinsic temperature T_{jmax} [61]:

$$R_{\theta ja} = \frac{T_{jmax} - T_a}{P_{ON}} \tag{4.19}$$

where

$R_{\theta ja}$ junction to ambient thermal resistance [°C/W];

T_{jmax} maximum allowable intrinsic temperature [°C];

T_a ambient temperature [°C].

Standstill air results in increased ambient temperature, which consequently results in higher intrinsic temperature, as $R_{\theta heatsink}$ is expected to be larger. This effect is eliminated, by ensuring constant movement of the cooling medium [61]. Attaching auxiliary fans to heat sinks is the most conventional solution of achieving air flow. A thin layer of thermal grease is applied between the surface to the heat sink and semiconductor device in order to remove possible air between the layers [21]. The layer should be as thin as possible to which ensures a small conduction path, subsequently resulting in a sufficiently small total thermal resistance between the junction and the ambient $R_{\theta ja}$.

4.5 Galvanic Isolation

During normal condition, the leakage current of the MOV is negligible due to the low varistor voltage caused by the low voltage drop of the semiconductors in the conducting path. After the MOV has cleared the fault, the MOV is subjected to the entire voltage potential of the DC source. The larger varistor voltage accounts for a larger leakage currents of the MOV, such that $I_{MOV}(V_{DC} = 1000\ V) \approx 1\ mA$. MOVs have negative temperature coefficient [60], consequently resulting in an self-amplifying effect where large leakage current increases the temperature of the MOV, which again results in higher leakage currents. Leakage current through the MOV results in significant on-state losses and heat generation, which increases the possibility of device failure due to P_{MOVmax} and T_{MOVmax} being reached [60]. Several standards require galvanic isolation for maintenance of power equipment, which referred to an electrically and physically separation between the input and output power circuit [62, 63]. Physical isolation after the fault has been eliminated would also remove the possibility of component destruction due to leakage current. SSCBs lack the ability of providing galvanic isolation [1, 17], making it necessary to consider implementing MCs to the circuit, which are able of providing physical isolation between the source and the CB [17, 64]. MCBs exhibit very low conduction losses, and may therefore be placed in series to the DC line without adding considerable power losses [1, 65]. MCs are incapable of interrupting DC currents, due to its lack of zero crossings [1], and will therefore not influence the breaking process for the considered CB. The MC is ignited simultaneously as the SSCB. The MC develops an arc and continues current conduction until the SSCB interrupts the fault independently. Instantly as a zero crossing current condition occurs, the arc extinguishes and the MC provides physical isolation.

One factor governing the expected lifetime of MCBs is the duration of the arc available during opening and closing of the contacts [66]. The duration of the arc should be minimized to reduce the possibility of contact erosion, which accounts for major equipment damage. In order for the MC to properly interrupt the leakage current and isolate the faulty part of a DC network, oscillations at the end of the demagnetization process is necessary. The snubber circuit of the CB may be properly selected such that the arc is extinguished instantly after the lines are demagnetized. MCs may also be installed in the AC side of the network. The fastest possible isolation time would then be half a period, which is 10 ms for a 50 Hz network. This may account for a longer arc duration than if it were placed in the DC side of the network.

Series connecting a MC between the DC source and CB allows for fast interruption followed by proper galvanic isolation, and is therefore recommended for the considered protection system. Establishing arcs between the contacts induces voltage spikes, which the MC must withstand [34]. Since the peak current is determined by the interruption process of the SSCB, the contactor switch must be able of withstand the prospected fault currents, and break and isolate the expected leakage current after the lines are demagnetized.

4.6 Criteria of designing Circuit Breakers

The semiconductor device actively restricts the flow of fault current, forcing it to commutate towards the MOV. The current continues to increase until the commutation is completed. It is therefore beneficial to select a semiconductor device capable of fast interruption, in order to limit the peak of fault current. The breaker must be designed to interrupt the highest possible fault current for the considered network, for both directions. Selecting a semiconductor device with high current interrupting capability may be advantageous in order to obtain a compact and economical CB. The semiconductor should also be able of conducting with relatively low losses, due to the frequent placement of CBs required to sufficiently isolate faults in the considered microgrid. Series connecting semiconductors increases the on-state losses, and complicates the design of the gate driver significantly, and should therefore be avoided.

The clamping voltage of the MOV must be larger than the DC bus voltage to ensure current reduction. In order for the CB to survive the breaking process, the clamping voltage of the MOV must never exceed its voltage ratings. The original literature of the proposed CB in [39], reported that the ratio between the maximum clamping voltage of the MOV of 1.6 kV, and semiconductor ratings of 2.5 kV, is 64 %. A thumb rule for the selection of MOV is developed based on this ratio. The clamping voltage of the selected MOV must never exceed 66.7% of the

voltage ratings of the considered CB. Thus, achieving a minimum safety margin of 33.3 % throughout the breaking process. Higher rated semiconductor device, which may be conceived as bulky and expensive, allows for higher clamping voltage, thus shorter energy dissipation periods.

Proper parameterization must be performed in order to assure that the resulting CB is capable of interrupting the possible peak current while surviving the TIV arising during fault operation. Connector switches able of providing physical isolation between the CB and DC source, is recommended to provide proper isolation after faults and during maintenance. Proper heat sinks must be implemented in order to provide a sufficient heat dissipation path between vulnerable devices towards a cooling material. This allows devices to operate at optimal temperatures while avoiding thermal destruction during both transient and normal operation.

5 Parameterization of Circuit Breaker Components

This chapter presents a variety of promising types of IGCTs, IGBTs and MOVs, which will be utilized for proper parameterization. Finally, two CB configurations comprising IGCTs and IGBTs will be designed, based on finding economical and power efficient solutions.

5.1 System Assumptions and Peak Current Calculation

Before performing proper parameterization, the possible peak current, which the CB must be capable of interrupting, must be obtained. Table 5.1 lists important system parameters and protection system assumptions utilized for finding the peak fault current. Best case scenario is considered for parameterization, in order to limit the size of the resulting CB. Methods for handling worst case scenarios will be discussed.

Table 5.1 System parameters and protection system assumptions

Parameter	Value
Threshold current, I_{th}	2 p.u.
Detection time, t_{det}	1 ms
Interrupting time, t_{int}	150 µs
DC voltage source, V_{DC}	1000 V
Nominal load current, I_o	250 A
Line impedance, L_{line}	74.3 µH

By neglecting additional losses, integrating Equation (3.2), and solving it for I_{fault}, the peak current is found:

$$I_{fault} = 2I_o + \frac{V_{DC}}{L_{line}}(t_{det} + t_{int}) \tag{5.1}$$

$$I_{fault} = 2 \cdot 250A + \frac{1000\,V}{74.3\mu H}(1ms + 150\,\mu s)$$

$$= 15\,977\,A$$

Based on the system assumptions, the CB needs to be capable of breaking a current of 16 kA.

5.2 Main Breaker Power Devices

There are mainly two types of semiconductors which will be considered, namely IGCTs and IGBTs. This section presents a variety of models of these semiconductor devices.

5.2.1 Asymmetrical and Reverse Blocking IGCTs considerations

ABB has one commercially available RB-IGCT rated 6.5 kV [51], which exhibits a maximum current interrupting capability of 1100 A. Other possible IGCT configurations developed by ABB, is an A-IGCT rated 4.5 kV [52], which exhibits a interrupting capability of 5000 A.

Table 5.2 presents the considered IGCTs together with obtained values from datasheets, such as voltage ratings V_N, repetitive peak collector current I_{CRM}, gate threshold current V_{GEth}, and on-state resistance R_{ON}. This table also presents the numbers of parallel connected semiconductor devices per breaker path M, required in order to break currents of 16 kA, which is found by using Equation (4.4).

Table 5.2 Types of IGCT

Model	**Voltage rating** V_N [V]	**Repetitive peak collector current** I_{CRM} [A]	**Gate threshold Voltage** V_{th} [V] [1]	**On-state resistance** R_{ON} [Ω] [2]	**Parallel connected devices** M [3]
5SHY 55L4500 [52]	4500	5000	1.12	0.004	4
5SHZ 11H6500 [51]	6500	1100	2.92	0.016	15

1) Typical value when conducting 120 mA

2) Conducting 250 A at 25°C

3) Per breaker path

5.2.2 IGBTs considerations

As previously mentioned, the simpler gate operation of IGBTs, makes them an appealing alternative in the use as the main breakers device of the considered CB. They are also available for a greater range of voltage ratings, than of that of IGCTs. ABB and Infineon provides IGBT modules with voltage ratings ranging between 1700 – 6500 V and 600 – 6500 V, respectively. For this thesis, we will only include IGBTs with rating from 1700 V, and up to 3300 V. The lower limit is selected based on the considered microgrid, while the upper voltage limit is based on IGCTs being more efficient of higher voltage ratings than of IGBTs of similar ratings [53]. Table 5.3 presents promising IGBT models within the considered voltage ratings range, together with some of their parameters.

Table 5.3 IGBT models

Model	**Voltage rating** V_N [V]	**Repetitive peak collector current** I_{CRM} [A]	**Gate threshold voltage** V_{th} [V] [1]	**On-state resistance** R_{ON} [Ω] [2]	**Parallel connected devices** M [3]
5SNA 3600E170300 [67]	1700	7200	6.30	0.004	3
FZ3600R17HE4 [68]	1700	7200	5.80	0.004	3
5SNA 1500E250300 [69]	2500	3000	5.90	0.004	6
5SNA 1500E330305 [70]	3300	3000	6.00	0.0045	6
FZ1500R33HL3 [71]	3300	3000	5.80	0.005	6
FZ1200R33KF2C [72]	3300	2400	5.10	0.007	7

1. Typical value when conducting 120 mA
2. Conducting 250 A at 25°C
3. Per breaker path

5.2.3 Loss calculation and comparison of Semiconductor Devices

Table 5.4 presents the considered semiconductor models with their corresponding on-state losses when conducting 250 A, which is found by utilizing Equation (4.10).

Table 5.4 Conducting losses comparison of considered semiconductor models

Type	Model	Gate threshold voltage V_{th} [V]	On-state resistance R_{ON} [Ω] [1]	Parallel connected devices M [2]	On-state losses P_{ON} [W] [3]
IGBT	5SNA 3600E170300 [67]	6.40	0.004	3	1683.33
	FZ3600R17HE4 [68]	5.80	0.004	3	1533.33
	5SNA 1500E250300 [69]	5.90	0.004	6	1516.67
	5SNA 1500E330305 [70]	6.00	0.0045	6	1546.88
	FZ1500R33HL3 [71]	5.80	0.005	6	1502.08
	FZ1200R33KF2C [72]	5.10	0.007	7	1337.50
A-IGCT	5SHZ 11H6500 [51]	1.12	0.004	4	342.50
RB-IGCT	5SHY 55L4500 [52]	2.92	0.016	15	796.67

1. Conducting 250 A at 25°C
2. Per breaker path
3. Based on equation (4.10) at 250 A

By observing Table 5.4, 15 parallel connected 6.5 kV rated RB-IGCTs are required per breaker path to successfully interrupt 16 kA in either direction, resulting in 30 RB-IGBTs per CB. The voltage rating of 6.5 kV is found excessive for the considered network, and indicates a significantly large investment costs when accounting size of the CB. In comparison, only 4 parallel connected 4.5 kV rated A-IGCTs per breaker path are adequate in order to interrupt fault currents of 16 kA. The lower voltage ratings and reduced number of parallel connections, indicate a compact and more economical CB solution utilizing 4.5 kV rated A-IGCTs. It is also observed from this table, that the CB comprising A-IGCTs has superior power efficiency compared to the other CB proposals. Thus, the 4.5 kV rated A-IGCT is selected to be further considered.

Observing Table 5.4, the variation of the conduction losses between the CBs comprising different types of IGBTs, is minor. Few parallel connections accounts for low investment cost, which is desirable for the final CB. It would be desirable to use the 1.7 kV rated IBT named FZ3600R17HE4 from Infineon due to the low number of required parallel connections. Series connecting two lower rated IGBTs in order to increase the voltage ratings of the CB is avoided due to excessive on-state losses and increased gate drive complexity. For higher rated IGBTs, the 3.3 kV rated IGBT named FZ1500R33HL3 from Infineon is suggested, due to its low conduction loss, and high current interrupting capability. A further investigation will be performed in section 5.4.

5.3 MOV Types

Based on previous discussion, five factors must be addressed when suggesting MOV modules for the considered electrical system and CB:

1. Only MOVs with a maximum leakage current of 1 mA while being subjected the DC bus voltage of 1000 V may be considered, in order to limit the effect of large leakage current after the lines has been demagnetized.
2. 16 columns of MOVs are considered. Each column must be able of conducting at least 1000 A, such that the total MOV is able of conducing fault currents of 16 kA, without being thermally destroyed.
3. The clamping voltage of the MOV must exceed the DC system voltage of 1000 V when conducting 1000 A, in order to force the current down to zero.
4. The clamping voltage of the MOV must never exceeds 66.7 % of the CB ratings when conducting 1000 A. The value is selected in order to provide a sufficient safety margin, and to limit the number of MOV columns.
5. The maximum operation temperature for MOV must never exceed 85 °C to avoid device failure [73].

Table 5.5 lists the possible MOV modules from the BA and BB series from Littlefuse [73], which may be utilized in the use to protecting CBs against TIV and dissipating the inductive energy stored in the lines. This table also include the estimated energy dissipation period t_{MOV} which is calculated using equation (4.3).

Table 5.5 MOV models and their corresponding operating voltage [73]

Manufacturer	Model	Average varistor voltage at 1 mA, $V_{N(DC)}$ [V]	Clamping voltage at 1000 A V_{clamp} [V] [1]	Energy dissipation period t_{MOV} [ms]	Maximum energy ratings (85°C, 2ms) [J]
Littlefuse BA Series	V661BA60	1050	1600	1.974	2300
	V751BA60	1200	2000	1.185	2600
	V881BA60	1500	2500	0.790	3200
Littlefuse BB Series	V112BB60	1850	3000	0.592	3800
	V142BB60	2300	4000	0.395	5000
	V172BB60	2765	4400	0.348	6000

1) Visually observed from VI-characteristics at 25°C

5.4 Final Parameterization

By analysing Table 5.4, the 4.5 kV rated A-IGCT module named 5SHY 55L4500 [51] has superior low conduction loss and high current interrupting capability. A CB comprising this power device will be further considered for the simulation. The power device has sufficiently large voltage ratings allowing utilization of larger MOVs, which reduces the energy dissipation period. The MOV model named V112BB60 with the clamping voltage of 3000 V, is the largest recommended MOV for this CB configuration.

None of the MOVs listed in Table 5.5 are suitable for a CB comprising 1.7 kV rated IGBTs. The smallest MOV provides a clamping voltage of 1.6 kV, which provides a too small margin to be considered. Higher ratings may be attained by series connecting two 1.7 kV rated IGBTs, which complicates the gate driver, and results in large conduction losses. The 1.7 kV based IGBTs are therefore excluded from further consideration.

Of higher rated IGBTs, the CB comprising 3.3 kV rated IGBT module named FZ1500R33HL3 [71] is expected to conduct with relatively low on-state losses, and will therefore be further studied. The V751BA60 MOV model provides a clamping voltage of 2000 V when conducting 1000 A, and is recommended to be combined with the 3.3 kV rated IGBT.

The two preferable power devices which will be further considered in this thesis, and some of their resulting breaking and conducting properties are listed in Table 5.6. Table 5.7 shows some

of the properties of the two MOVs, including the clamping voltage when conducting 1000 A, and the total maximum energy capacity P_{MOVt}.

From the component datasheets, the weight of the IGCT and IGBT modules are 2.8 kg and 1.2 kg respectively [51, 71]. Table 5.6 shows the total weight of the CBs comprising a total of 8 IGCT modules and 12 IGCT modules. The heavier weight of the IGCT based CB of 23.2 kg, compared to that of the IGBT based CB of 14.4 kg, indicates that utilizing IGCTs for CB applications is the most costly solution.

Table 5.6 Summary IGCT and IGBT properties under further consideration

Model	**Type**	**Voltage rating** V_{DRM} [V]	**Number of devices** MxN	**On-state losses** P_{ON} [W]	**Max. current int. capability** I_{MPC} [kA] [1]	**Total weight** G [kg]
5SHZ 11H6500 [51]	A-IGCT	4500	4x1	342.50	18	23.2
FZ1500R-33HL3 [71]	IGBT	3300	6x1	1502.08	20	14.4

1. Max. current interrupting capability of power device times number of devices in parallel

Table 5.7 Properties of the considered MOV under further consideration

Model	**Considered Semiconductor**	**Clamping voltage at 1000 A** V_{clamp} [V]	**Maximum energy capacity for 16 columns** P_{MOVt} [kJ] [1]
V112BB60	A-IGCT	3000	60.8
V751BA60	IGBT	2000	41.6

1. $P_{MOVt} = 16 \cdot P_{MOV}$

5.5 Higher Current Evaluation

The CB parameterizations were not performed considering worst case scenario. As previously discussed in chapter 3.1.1, the main problems concerning LVDC systems is small system inductance. If the fault occurs close to the source, the resulting inductance between the fault and source is considerably small, which results in steep rise of fault current. For example, if the inductance seen from the fault is approximately 1 μH, the fault current will reach approximately 1150.50 kA before the CB is supposedly capable of forcing the current to commutate toward the MOV, based on the constant interrupting and detection period assumed in this thesis. The calculation is presented in Appendix A, and is performed assuming an ideal DC voltage source, while neglecting resistive elements of the fault circuit. Observed in Table 5.6, the CBs based on IGCTs and IGBTs are capable of interrupting currents of maximum 18 kA and 20 kV, respectively. If the worst case scenario is not properly addressed, the CBs are not able of breaking the current, which causes the fault current to continue to rise undisturbed. This section presents two methods, which may be implemented in order to handle worst case scenarios.

5.5.1 Revaluating the number of parallel connected Semiconductors within the Circuit Breaker

The first method for handling worst case scenario, is to initially parameterize the CBs based on the worst case current. The repetitive peak collector current I_{CRM} of the preferable semiconductor devices found in Chapter 5.4, are 5000 A and 3000 A, for the selected A-IGCT and IGBT, respectively. If the CBs were designed such that they could interrupt currents of 1150.0 kA, the required number of parallel connected IGCTs and IGBTs would be 231 and 384, respectively. The peak current will most likely never reach 1150.k kA, due the resistive elements exciting the fault circuit, subsequently reducing the required number of parallel connections. Regardless of including the resistive circuit elements, the resulting CB designs are indicated to be significantly bulky and expensive, which is one of the disadvantages concerning SSCB technology [1]. The number of required semiconductor devices will be further discussed during simulations.

The most exposed system components must be rated such that they are able of withstanding the worst case peak current the considered system may experience. Increasing the current interrupting capability of the CB, does not restrict the worst case peak current, resulting in overdimensioned system components and large investment costs.

5.5.2 Current Limiting Reactors

The steep rise of fault current causes the threshold current to be reached in a short period of time, triggering the protection system relatively fast. The constant detection and interruption time periods assumed for the considered protection system is the main problem with excessive steep rise of fault current. In order to avoid unacceptable steep rise of currents, CLR is suggested to be placed in series to the CB, as illustrated in Figure 5.1. According to Equation (3.2), the additional inductance provided by the reactors, limits the rate of current rise. The slacker rise of fault current provides more time to the protection system to isolate and break the fault. A manageable peak current is easier achieved by using CLR to handle worst case scenarios. The lower peak current accounts for lower system components ratings, which accounts for lower investment costs, compare to that of increasing the current interrupting capability of the CBs.

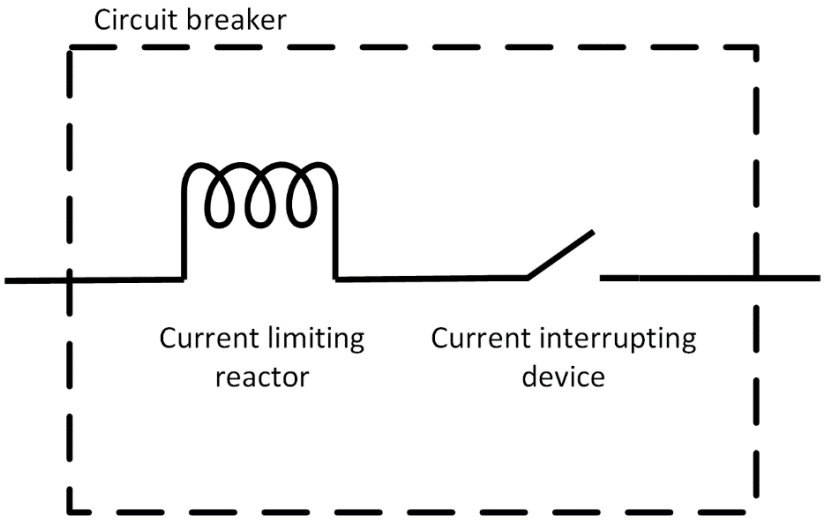

Figure 5.1 Circuit breaker with current limiting reactor

Even though higher inductance results in slacker rise of fault current, it also accounts for a stiffer grid, resulting in slower changes of current flow, which is a quality found undesirable for efficient power flow control [21]. This problem has to be addressed by the converter controllers. Additional disadvantages of utilizing inductors concerns increased cost and size of the network installation.

For air-core reactors, the following trade-off relationship between cost, size, inductance and rated current may be expressed as [29]:

$$C, G_L \propto I_{fault}\sqrt{L_{CLR}} \tag{5.2}$$

where

L_{CLR} current limiting inductance [H];

C cost [NOK];

G_L weight of inductor [kg];

A multi-objective optimization of the CLR design is necessary to minimize the cost, reactor mass and peak fault current [29].

This thesis will consider a CLR capable of limiting the current to 18 kA, which is the maximum current interrupting capability of the IGBT based CB. By deriving Equation (5.1), while assuming constant detection and interrupting time periods, the resulting current limiting inductance is found:

$$L_{CLR} = V_{DC} \cdot \frac{t_{det} + t_{int}}{I_{max} - 2I_o} \tag{5.3}$$

$$L_{CLR} = 1000V \cdot \frac{1 \cdot 10^{-3}s + 150 \cdot 10^{-6}s}{18 \cdot 10^{3}A - 2 \cdot 250A} = 65.71\ \mu H$$

A CLR of 65.71 µH is considered to be implemented in the simulation section.

6 Simulation Model Description

This chapter describes the implementation and construction of simulation models complied in Matlab® Simulink. First, the modelling description of the most basic components, including line models and short-circuit fault models are presented. Then, the construction and implementations of the standalone CB model are described. Finally, three different models are presented, based on the LVDC microgrid constructed in Chapter 2. All models presented in this chapter contain embedded blocks found in the Simscape library in Matlab® Simulink.

6.1 Basic Component Models

6.1.1 Line Model

The line are modelled using a purely inductive Series RLC Branch block as shown in Figure 6.1. Based on calculations provided in Appendix A, the line parameter is found to be 74.3 μH. The line resistance is ignored for the simulations.

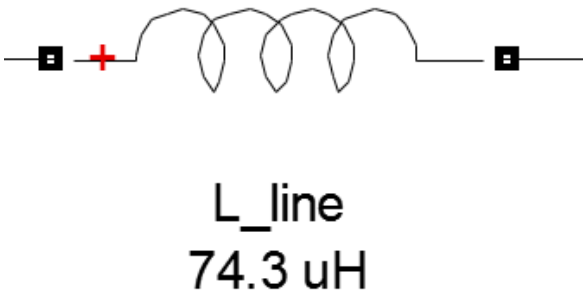

Figure 6.1 Line model

6.1.2 Fault Model

Shown in Figure 6.2, the fault is emulated using an Ideal Switch block, which is gate controlled via a Pulse block, causing a fault to occur at a specified time. The fault is triggered after the system is sufficiently stabilized, which is specific for each simulation. This figure also illustrate two fault models are implemented on each side of the line model, parallel connected to either the output of the source or the input of the load. These scenarios emulates the least and most critical fault placements of the considered systems. When simulating one if the scenarios, the other fault model is commented out, thus ignored during simulation, as illustrated in this figure, where the best case scenario is studied. The Ideal Switch blocks have an on-state resistance of 1 mΩ, emulating a small short-circuit resistance.

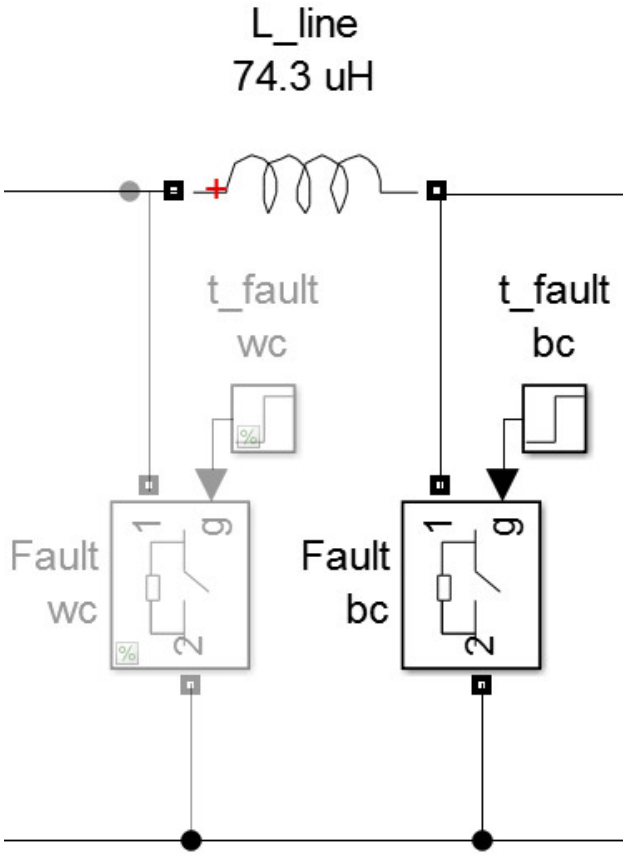

Figure 6.2 Fault model

6.2 Circuit Breaker Standalone Model

A simple design circuit is considered to examine the performance of the CB. This test model is illustrated in Figure 6.3.

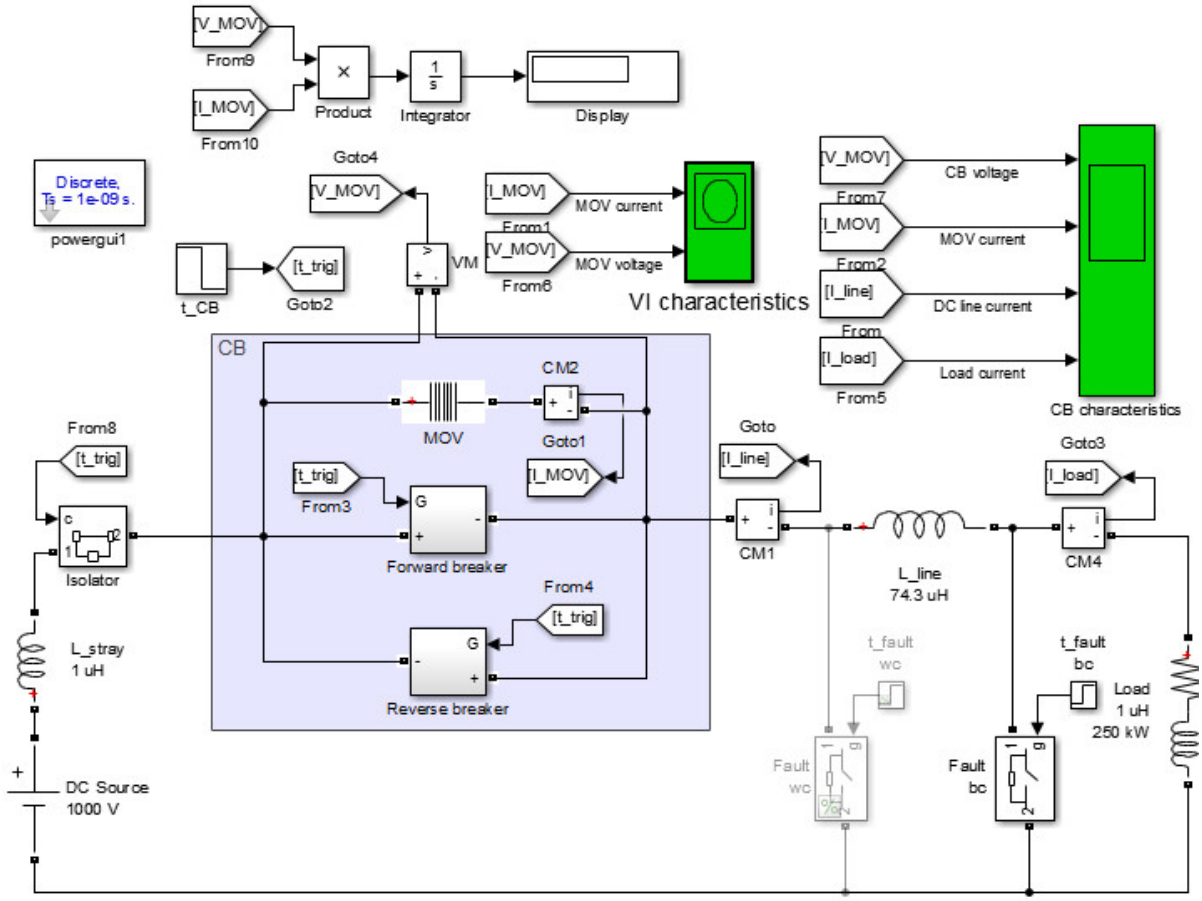

Figure 6.3 Circuit breaker standalone model

The system parameters of the simulations are given in Table 6.1. An ideal DC source block with a DC voltage of 1000 V delivers 250 kW through a line model. The load is modelled as a purely resistive Series RLC Branch block of 4 Ω, ensuring a DC line current of 250 A. Stray inductances of 1 μH are implemented as purely inductive RLC Branch Blocks, close to the source and the load, as seen in Figure 6.3. The stray inductance is chosen to be considerable small compared to the line inductance.

Table 6.1 Circuit breaker test model parameters

Parameter	Value
DC voltage source V_{DC}	1000 V
Nominal load current I_o	250 A
Total Line Inductance L_{line}	74.3 µH
250 kW Resistive Load R_{load}	4 Ω
Stray inductance L_{stray}	1 µH

6.2.1 Breaker models

Figure 6.3 shows that the CB model used for the simulations comprises two Breaker models and one MOV block. The Breaker models are connected in antiparallel to achieve bidirectional current interrupting, as described in section 4.1. Each Breaker model comprises *M*x*N* IGBT blocks. The IGBT blocks are modelled as ideal switches. During on-state mode these blocks conduct current with a simplified linear VI-characteristics, compared to that of their realistic operations, illustrated in Figure 4.3. The on-state parameters of the considered power devices are given in Table 6.2. In blocking mode, the IGBT blocks are immediately represented as an infinite resistance, completely blocking the current instantly. Figure 6.4 shows the Breaker model comprising 4x1 IGBT blocks, emulating the proposed CB based on 4.5 kV rated A-IGCTs. When simulating using the CB based on 3.3 kV IGBTs, two extra IGBT blocks are added in parallel for each Breaker model.

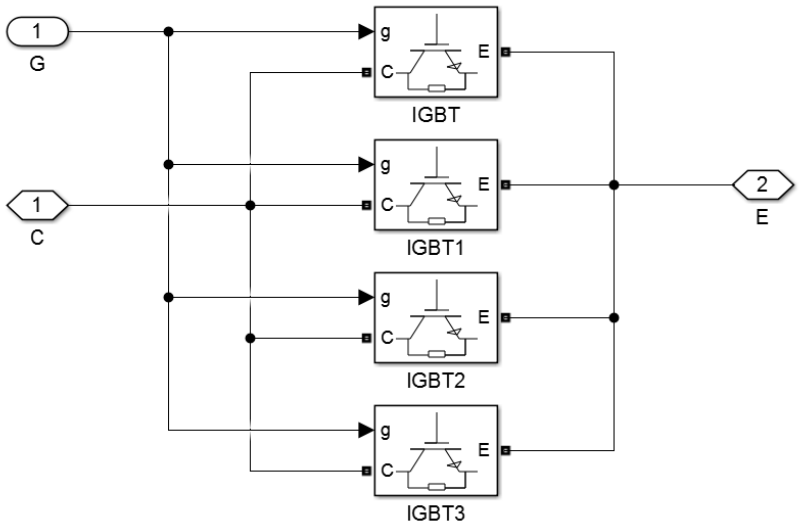

Figure 6.4 Main breaker model

Table 6.2 IGBT parameters

Type	**Voltage rating** V_{DRM} [V]	**Number of devices** MxN	**On-state resistance** R_{ON} [mΩ]	**Threshold voltage** V_{GEth} [V]	**Max. current int. capability** I_{MPC} [kA] [1]	**Max. allowed clamp. voltage** V_{max} [V]
A-IGCT	4500	4x1	4	1.12	18	3000
IGBT	3300	6x1	5	5.8	20	2200

The states of the IGBT blocks is controlled via a Pulse block providing zero gate bias to the CB after it is triggered. Due to the ideal switching performance of the IGBT blocks, the interruption period must be included in the triggering time of the Pule block. The triggering time is specific for each individual case, and is either found by calculations or pre-fault interrupting simulations given in the Appendixes.

RC-snubber circuits are initially embedded in the IGBT blocks to protect them against stress occurring during switching operations. The snubber contains a resistor R_S and a capacitor C_S, and is placed in parallel to the semiconductor [21]. The values of the snubber parameters will be selected based on simulation result, in order to sufficiently minimize the oscillations and stress of the current and voltage.

6.2.2 MOV Model

The MOV is modelled using a Surge Arrester block. The block is modelled as a non-linear resistance divided into three segments as illustrated in Figure 6.5, each with adjustable parameters, V_{ref}, I_{ref}, α_i and k_i in addition to number of columns in parallel, *n*.

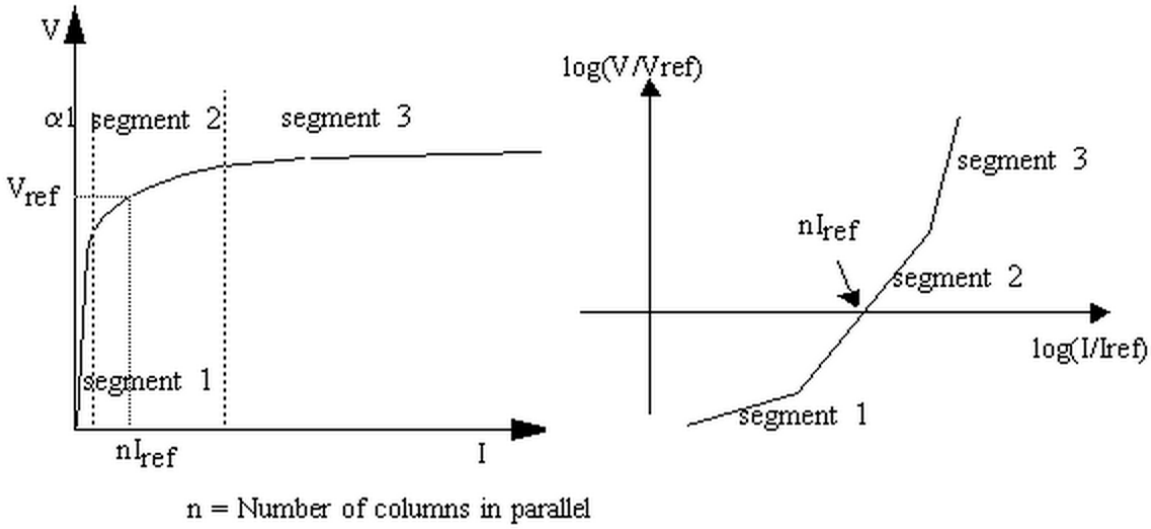

Figure 6.5 Surge Arrester block VI characteristics [74]

The relationship between these parameters per segment *i* is given in [74] as:

$$\frac{v_{MOV}}{V_{ref}} = k_i \left(\frac{i_{mov}}{I_{ref}}\right)^{\alpha_i} \tag{6.1}$$

where

v_{MOV} voltage across the MOV [V]

V_{ref} protection voltage [V];

k_i ceramic material constant of segment *i* [S];

α_i non-linearity exponent of segment *i*;

i_{mov} instant current flow in MOV [A];

I_{ref} reference current per column [A];

i segment [1-3].

Based on discussion in chapter 4.3.2, V_{ref} is the clamping voltage for one MOV column when conducting 1000 A. Accordingly, are I_{ref} and n will be selected to be 1000 A and 16, respectively. This allows the Surge Arrester block to conduct 16 kA with a maximum allowable

clamping voltage specific for each CB proposal given in Table 6.2. Adjustment of the remaining parameters will be performed through simulations, with a goal of resembling the VI-characteristics from datasheets provided by Littlefuse in [73]. A XY Graph block, able of comparing two measurements, has been implemented to the test model in order to simpler achieve this goal. The considered MOV models for each CB configuration are listed in Table 5.7.

The accumulated energy dissipated by the MOV is simply found implementing logic algorithm blocks based on equation (4.12), as shown in Figure 6.6.

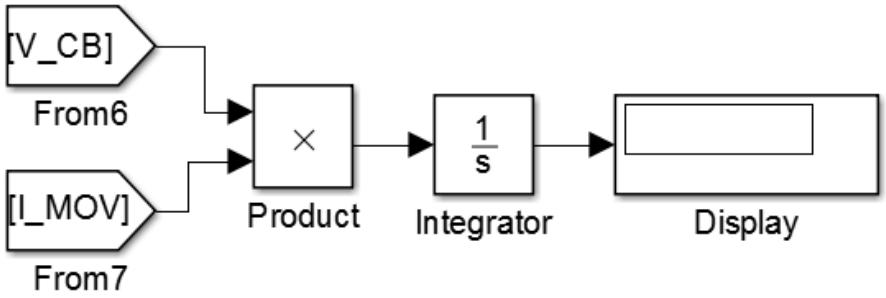

Figure 6.6 Simulation schematic of method finding the accumulated energy absorbed by MOV

6.2.3 Galvanic Isolator Model

Galvanic isolation is achieved by utilizing a Breaker block connected in series to the CB model as shown in Figure 6.3. The Breaker block is modelled as an MCB typically applied for AC applications, only capable of breaking currents if the current crosses zero. A small on-state resistance of 1 μΩ is considered for this block to obtain a considerably small conduction loss, which is found typical for MCB [1, 65]. The sequence during an interrupting process is that the MC remains closed, until the CB is triggered. The MC will not provide physical isolation instantaneously after being triggered, but conducts until the fault current crosses zero due to demagnetization of the line inductance L_{line}. Once the fault current has been reduced to zero, the MC provides adequate isolation. The triggering signal of this device is provided by the same Step Block triggering the IGBT blocks.

6.2.1 Presentation of Case Scenarios and triggering Times for the Breaker

Due to the simple circuit systems considered for the standalone test, the triggering signals of the CB and isolator is found by calculations. All calculations are presented in Appendix A, and are found by using Equation (4.2), using a threshold current of 500 A, a nominal current of

250 A, a detection period of 1 ms, an interruption time period of 150 µs and a fault initiation of 1 ms. The only variable is the inductance *L* seen between the source and the fault.

Four simulation cases will be considered for the CB standalone model. Two cases emulating a fault, where either the fault short-circuits the load or the source are studied with and without implementing CLR to the model.

Figure 6.3 shows the first test emulating a fault occurring near the load without a CLR. The CBs are parameterized for handling currents of this case. This case will mainly be used to simply optimize the values of the snubber and MOV parameters. From Appendix A, the CB is triggered at 2.16858 ms.

A worst case scenario will be implemented to the simulation, which is a fault occurring close to the voltage source. The simulation will illustrate the destructive current values the components is subjected to if worst case scenarios are not properly addressed. If the CB were to be able of breaking currents occurring during worst case, the CB is triggered at 2.15025 ms.

In order to handle the effect of worst case currents, external CLR are implemented between the CB and the DC source, as depicted in Figure 6.7. The CLR model is implemented using a purely inductive Series RLC Branch block, with a value of 65.71 µH, calculated in Chapter 5.5.2.

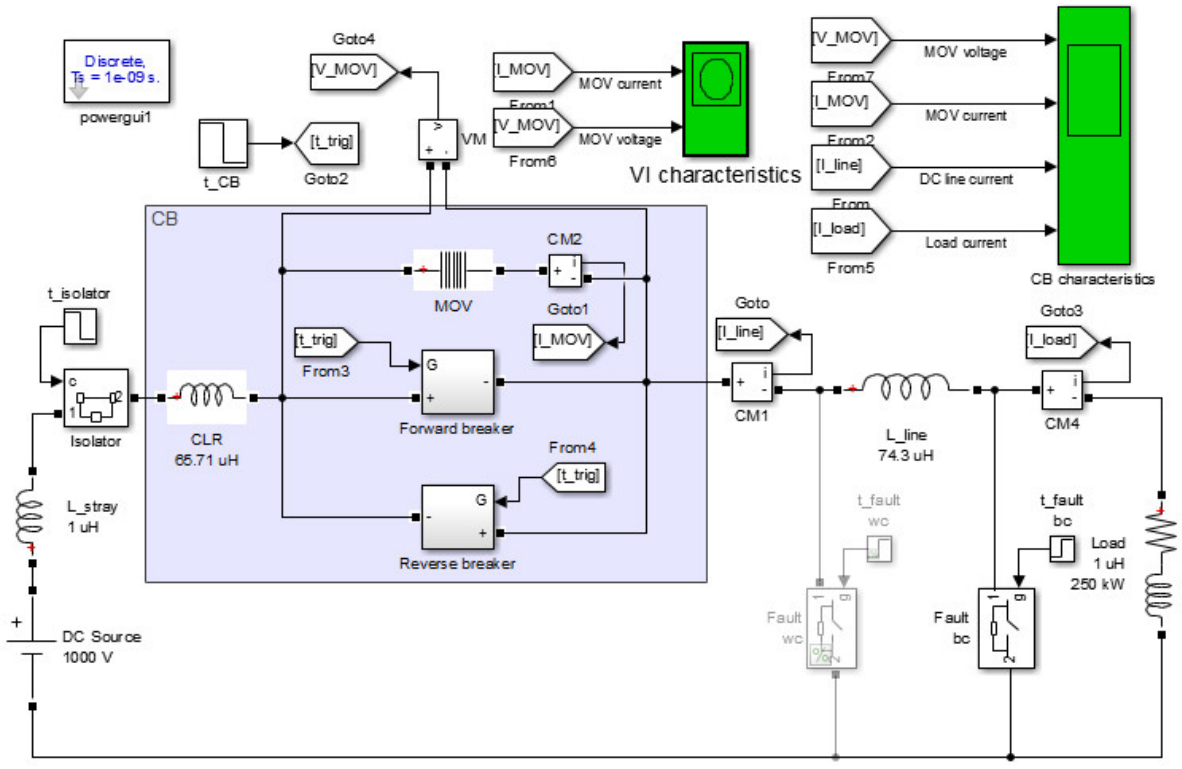

Figure 6.7 Stand-alone circuit breaker simulation model with current limiting reactor

When accounting the additional CLR, the CB are triggered at 2.16668 ms for worst case. Finally, a simulation will be performed to illustrate the breaking performance after implementing CLR for other cases than worst case. Accordingly, the CB is triggered at 2.28525 ms.

6.3 DC Microgrid Models

The performance of the best CB configuration, proposed from the CB stand-alone simulations, will be further analysed to protect a LVDC microgrid. The DC microgrid will be divided into three isolated systems, based on the systems discussed in chapter 2. Several simplifications are implemented for all systems, such as simplifying the unfocused part of the network using ideal sources and resistive elements, and considering only one point of steady state operation for all systems, eliminating the need for converter control. The model designs of the three systems are presented during this section.

6.3.1 Rectifier System Model

Figure 6.8 presents the rectifier system model. A three-phase AC source is implemented using three AC source blocks with phase voltages of 560 V. All three sources are operated with a frequency of 50 Hz, shifted 120° from each other. The AC source is interconnected to the 1000 V DC distribution network through a rectifier, which will shortly be presented. The remaining part of the network is emulated implementing a resistive load of 4 Ω, which achieves a DC line current of 250 A. The system parameters are given in Table 6.3.

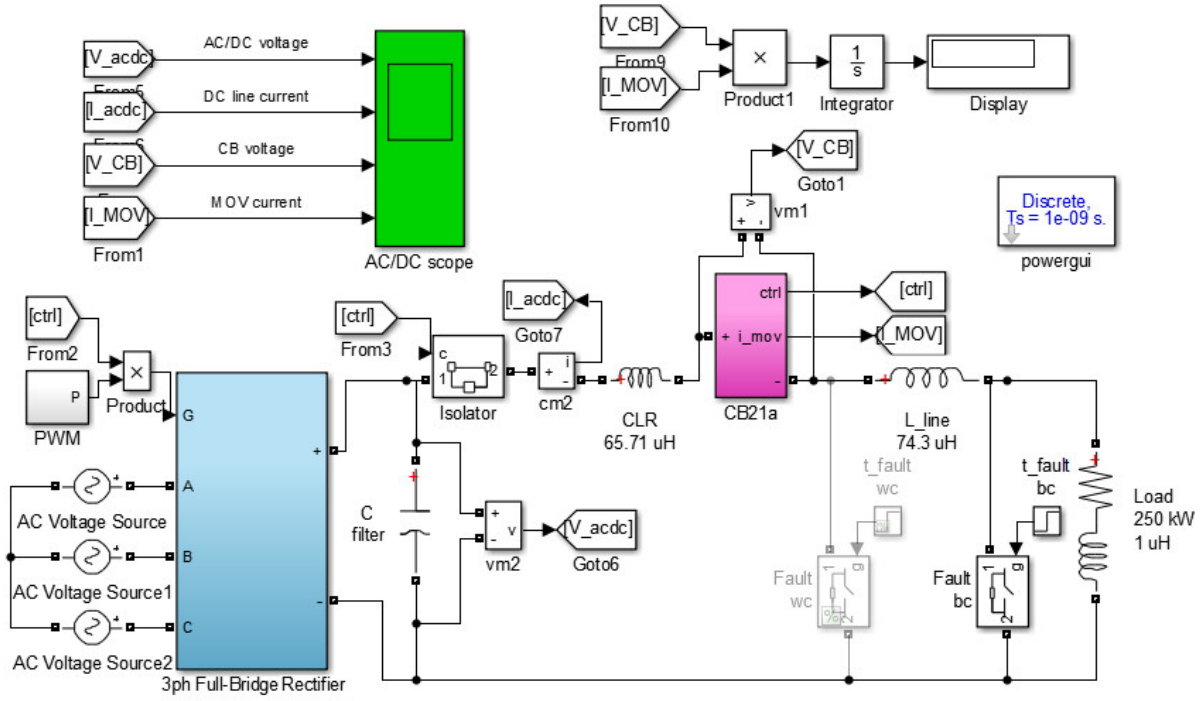

Figure 6.8 Rectifier system model

Table 6.3 Rectifier system parameters

Parameter	Value
AC source phase voltage, $V_{\varphi,source}$	520 V_{rms}
Stray inductance, L_{stray}	1 µH
Line Inductance, L_{line}	74.3 µH
Current limiting inductance, L_{CLR}	65.71 µH
Nominal load current, I_o	250 A
Resistive load, R_{load}	4 Ω
Power consumption, P_{load}	250 kW
DC link capacitor, C_L	5 mF

6.3.1.1 Rectifier Model

The rectifier was implemented using six IGBT/diode blocks to represent a three-phase two-level rectifier, as shown in Figure 6.9. The conduction and switching losses of the converters are not considered for this thesis. To guarantee satisfactorily low conduction loss, the on-state resistance of the IGBT/diode blocks are selected to be 0.1 mΩ. The PWM signal used to control the switching coordination of the IGBT valves are implemented using an embedded PWM Generator block from Simulink, depicted in Figure 6.10. This figure show how the modulation index *m* of the PWM generator is controlled by adjusting the amplitude of the reference voltage input to the PWM generator. As previously discussed, no further controllers are implemented to any of the converters. One point of operation is considered, where the line current is only determined by the DC output potential and the load resistance. From Chapter 2.2.1, a modulation index $m = 0.9$ provides an output voltage of approximately 1000 V.

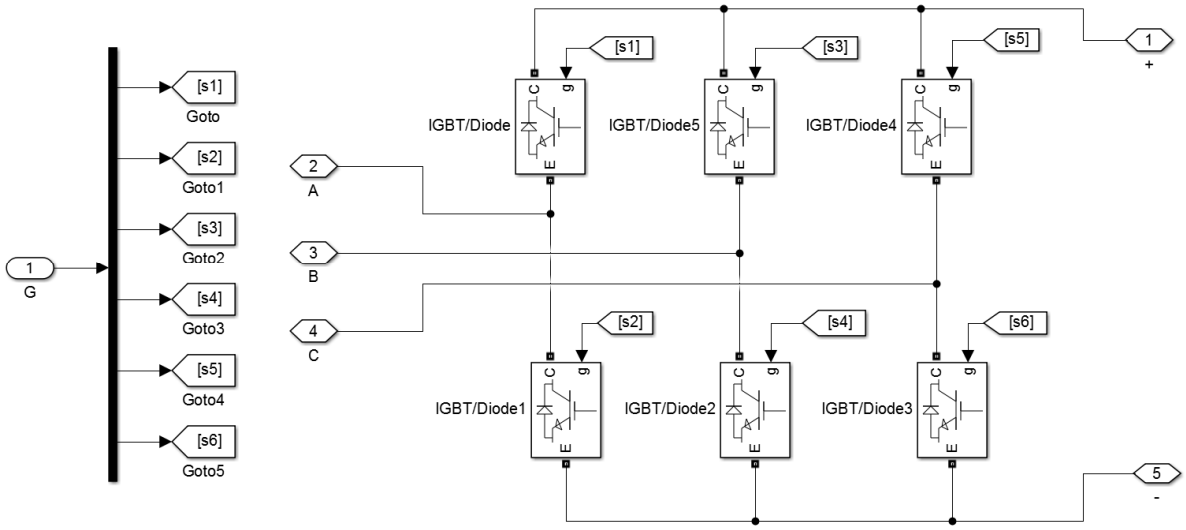

Figure 6.9 Full-bridge converter model

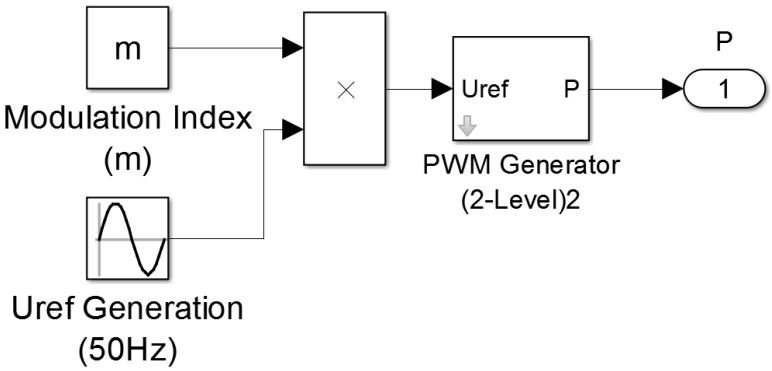

Figure 6.10 PWM signal generator model

6.3.2 Inverter System Model

Figure 6.11 presents the inverter system model. This model emphasis mainly on the inverter part of the network, allowing the remaining part of the system to be emulated using DC voltage source block of 1000 V. The load is simply modelled using a Three-Phase Parallel Resistive Branch block of 2 Ω, which assures a DC line current of 250 A. The three phase load is fed 250 kW from the DC network of 1000 V through an inverter model. The system parameters are given in Table 6.4.

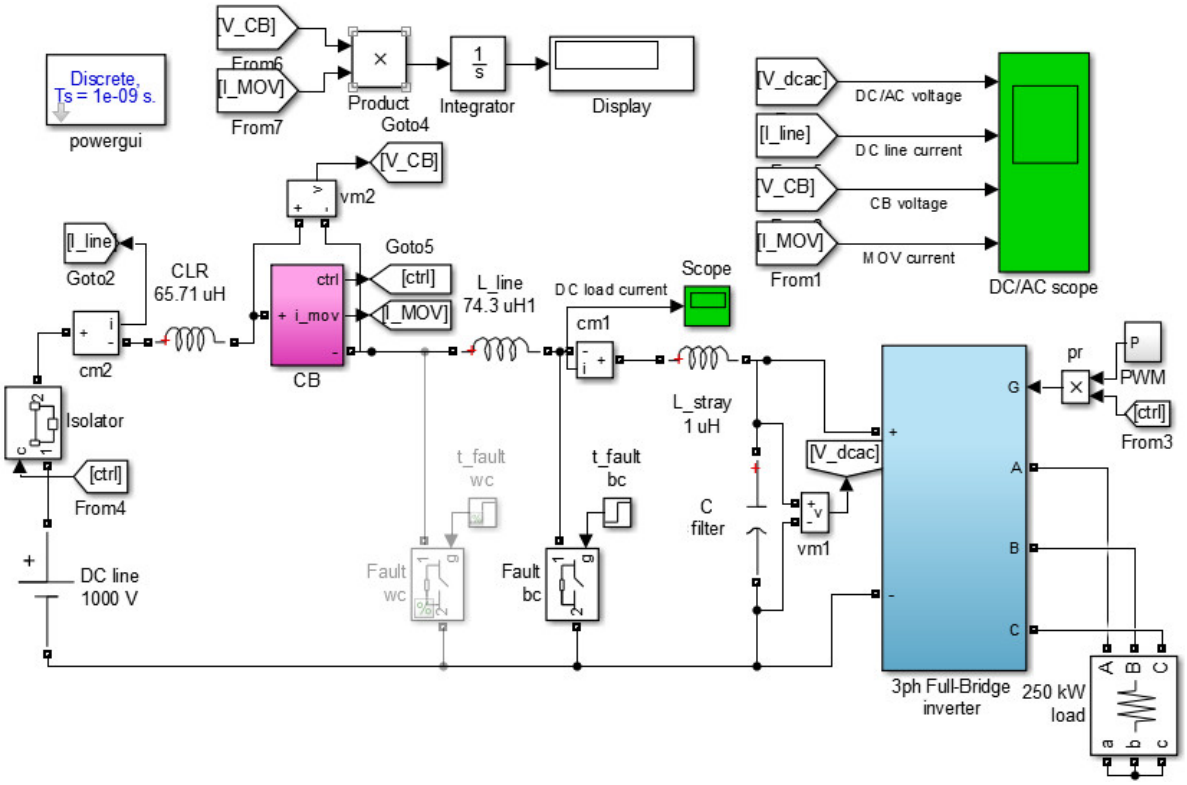

Figure 6.11 Inverter system model

Table 6.4 Inverter system parameters

Parameter	Value
AC load phase voltage, $V_{\varphi,load}$	520 V_{rms}
Stray inductance, L_{stray}	1 µH
Line Inductance, L_{line}	74.3 µH
Current limiting inductance, L_{CLR}	65.71 µH
Nominal load current, I_o	250 A
Parallel resistive load, R_{load}	2 Ω
Power consumption, P_{load}	250 kW
DC link capacitor, C_L	0.5 mF

6.3.2.1 Inverter Model

The inverter model is identical to the rectifier model utilised in the inverter system. Based on discussion on chapter 2.2.2, a modulation index m = 0.9 accounts for an output phase voltage of roughly 560 V.

6.3.3 Battery System Model

Observed in the battery system model depicted in Figure 6.12, the battery is implemented using a DC Voltage Source block of 500 V. The battery is assumed to be perfectly stiff and operate at full capacity throughout the simulation. The battery is connected to a DAB IBDC, which provides a sufficient output voltage of 1000 V. The remaining part of the network is replaced with a resistive load of 4 Ω, consuming 250 kW with a DC line current of 250 A. The system parameters are given in Table 6.5.

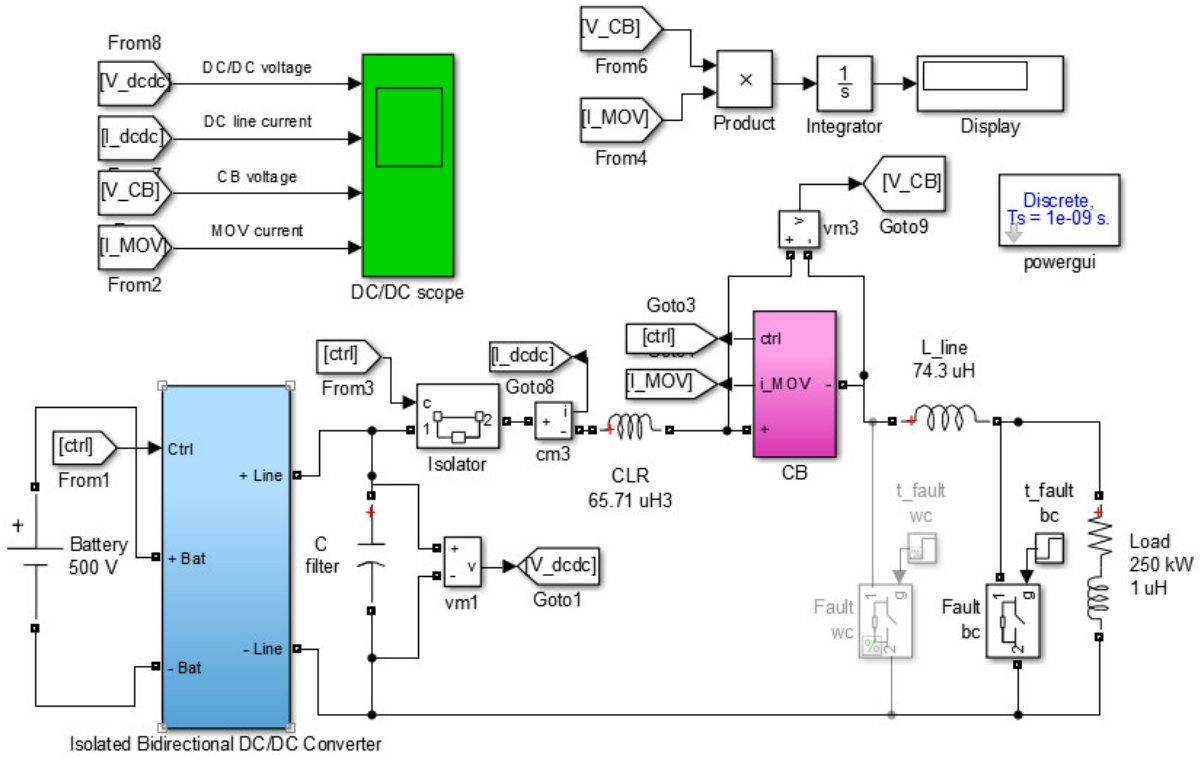

Figure 6.12 Battery system model

Table 6.5 Battery system parameters

Parameter	Value
Battery voltage, $V_{battery}$	1000 V
Stray inductance, L_{stray}	1 µH
Line Inductance, L_{line}	74.3 µH
Current limiting inductance, L_{CLR}	65.71 µH
Nominal load current, I_o	250 A
Resistive load, R_{load}	4 Ω
Power consumption, P_{load}	250 kW
DC link capacitor, C_L	30 mF

6.3.3.1 Isolated Bidirectional DC/DC Converter Model

Figure 6.13 presents the simplified simulation model of the IBDC with a full-bridge on each side of an inductance emulating the leakage inductance of the high frequency transformer.

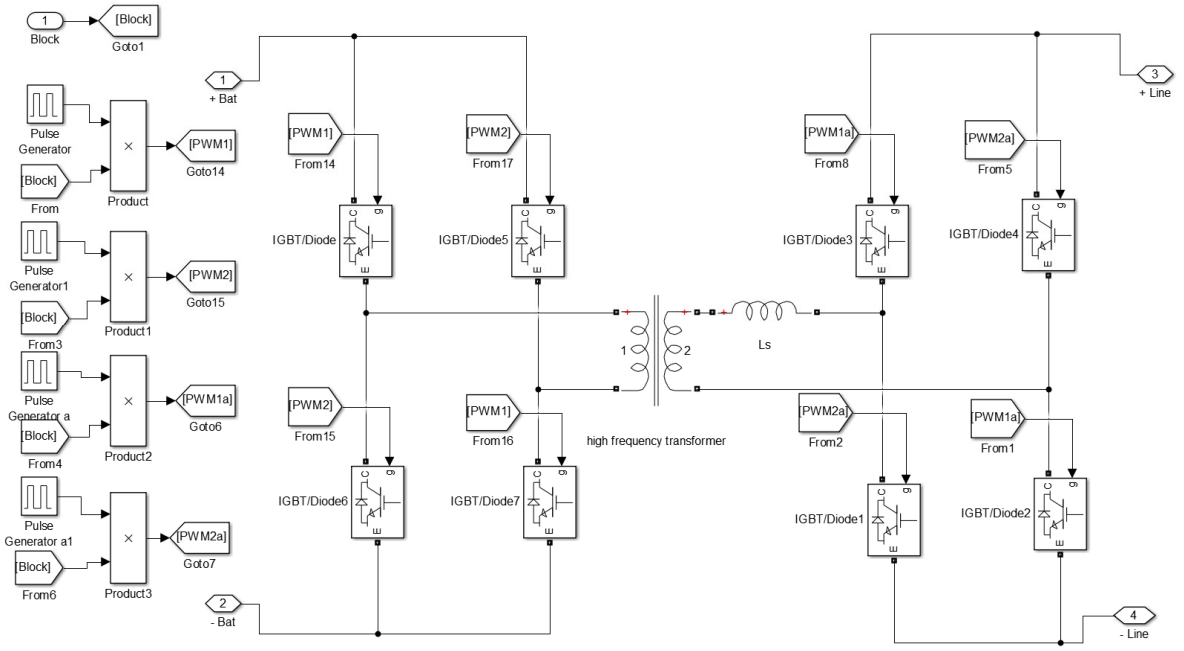

Figure 6.13 Isolated bidirectional DC/DC converter model

Power transferring is controlled by phase-shifting the triggering signals of the full-bridges, as discussed in chapter 2.2.3.

An ideal transformer is implemented as the high frequency transformer, where the inductor L_s represents the equivalent leakage inductor of the transformer. The gate signals to the active bridges were realized using two opposing pairs of Pulse Generator blocks illustrated in Figure 6.13. Each Pulse Generator block is switched with a frequency of 20 kHz, and a duty cycle D of 0.49 to eliminate deadtimes. The switching signals of the left bridge leads the switching signal of the right bridge with $\pi/2$ rad. The transformer ratio n_1:n_2 is selected to be 1:2.2 to make up for the minor voltage drop over the switches and inductor. From chapter 2.2.3, it was calculated that the external inductor is required to be 27.5 µH in order to transfer 250 kW at a phase shift of $\pi/2$ rad.

6.3.4 Implementing Protection Systems to the considered Systems

Figure 6.14 shows the schematic of the CB model found in all simulation models. It is based on the final CB found from CB standalone simulation result. The threshold time period for each system, is found by measuring the time the fault current needs to reach the threshold current of 500 A in a pre-interrupting simulation, shown in Appendix B.

As discussed in chapter 3.1, once a fault is recognized, a blocking signal is sent towards the converter, constraining the current flow through the anti-parallel diodes, in order to protect the converter. The blocking is performed by multiplying the triggering signal of the CB to the PWM switching signals of the converters, so that the IGBT valves of the converters receives zero gate bias simultaneously as the CB. The same triggering signal used to trigger the CB is utilized for the converter, in addition to the MC, as seen when comparing Figure 6.14 to Figure 6.8, 6.11 and 6.13.

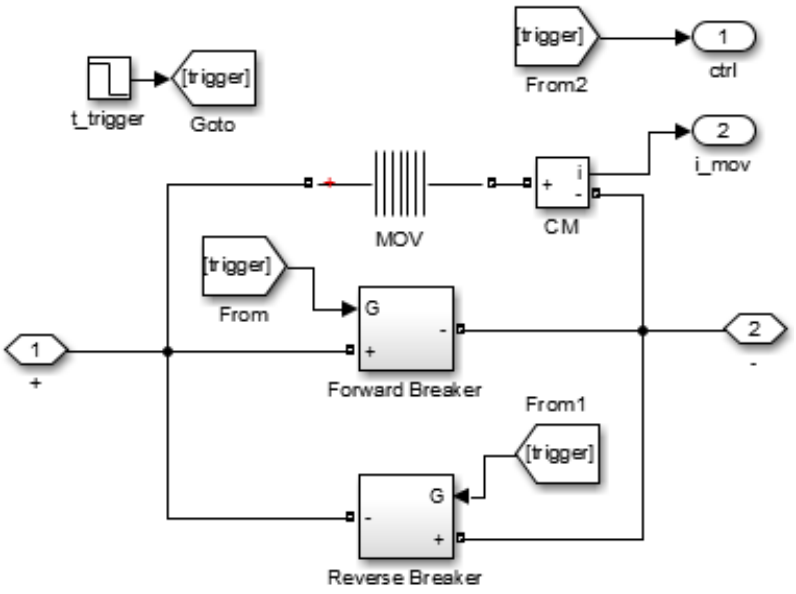

Figure 6.14 Circuit breaker model

6.3.5 Filters

Harmonic pollutions is a consequence of utilizing power electronics [1]. Converters introduces major harmonic distortions to the network, due to the IGBT valves repeatedly breaking the current, causing voltage and current ripple. A DC link capacitor connected to the DC line side of every converter is implemented in order to reduce the ripple. During faults, the capacitors are immediately discharged, and have major influence on the amount of energy magnetizing the lines, consequently effecting the level of peak currents. The selection of proper DC link

capacitors will not be investigated for this thesis. Since they have major influence on the operation of the system during faults, they are selected based on achieving preferable fault operation.

7 Results

This chapter presents the main results from simulated experiments, using the CB standalone models and the three converter systems models described in chapter 6.

7.1 Circuit Breaker Standalone Results

The breaker performance of two CB proposals, comprising either IGCTs or IGBTs, will be tested and compared against each other in this section. First, simulations selecting proper values of snubber parameters will be presented. Then, the performance of the MOV will be adjusted to have similar behaviour to that of the VI-characteristics found in component datasheets. The two CB configurations will be roughly compared against each other, based on their simulated performance, and findings from Chapter 5. Finally, the effect of implementing CLR will be evaluated for handling worst case using the most promising CB configuration.

7.1.1 Snubber Parameters Selection

The goal of adjusting the snubbers is to constrain the transient stress and oscillations occurring after the fault current has been cleared. In order to properly observe the effect of varying the snubber parameters, the MC is delayed with approximately 2 ms after the fault is applied to the simulation.

The result of the first simulation using a snubber capacitance C_s = 1 μF, and a snubber resistance R_s = 80 mΩ is presented Figure 7.1.

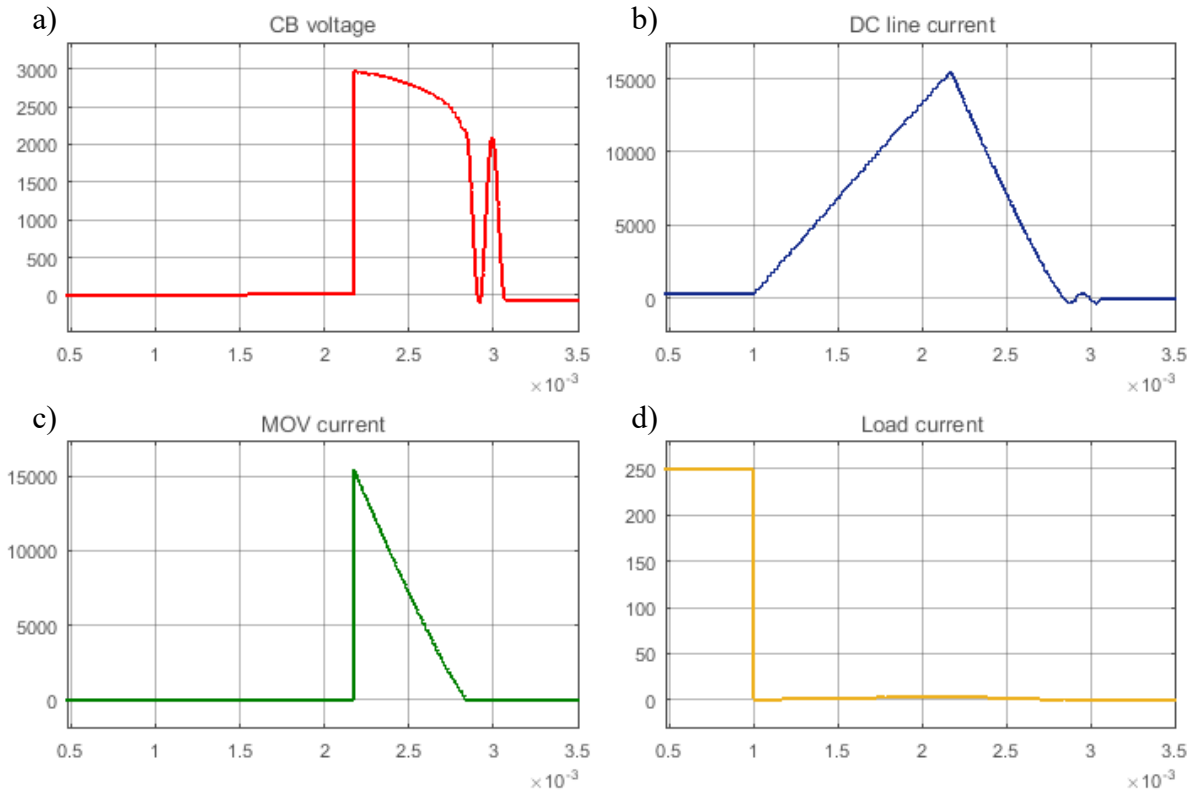

Figure 7.1 CB performance using a 4.5 kV rated IGCT based CB, C_s = 1 µF, and R_s = 80 mΩ. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

From Figure 7.1, it is notable that the waveforms looks promising according to Figure 4.2 from theory. A fault is applied to the system at t = 1 ms, and begins to rise. The current reaches a peak current value of 15.47 kA at the instant of which the CB is triggered, forcing the current to commutate towards the MOV. The MOV clamps the voltage at approximately 3000 V, forcing the current to reduce to zero. This figure show that once current is reduced to zero, the CB is subjected to voltage oscillations, with a peak-peak voltage of 2000 V. The MC properly manages to break at first zero crossing current, which is 0.2 ms after being triggered at t = 3 ms. The result indicates that the main problem for this considered CB is the excessive voltage oscillations occurring after line demagnetization. Interference between the line inductance and the parasitic capacitance of the IGBT modules might be the cause for this oscillation.

Increasing the snubber resistance R_S reduces the oscillation amplitude. Figure 7.2 shows the simulated graphs after R_s is increased to 10 Ω. The peak-peak value of the voltage oscillations is now halved, which is considered more manageable.

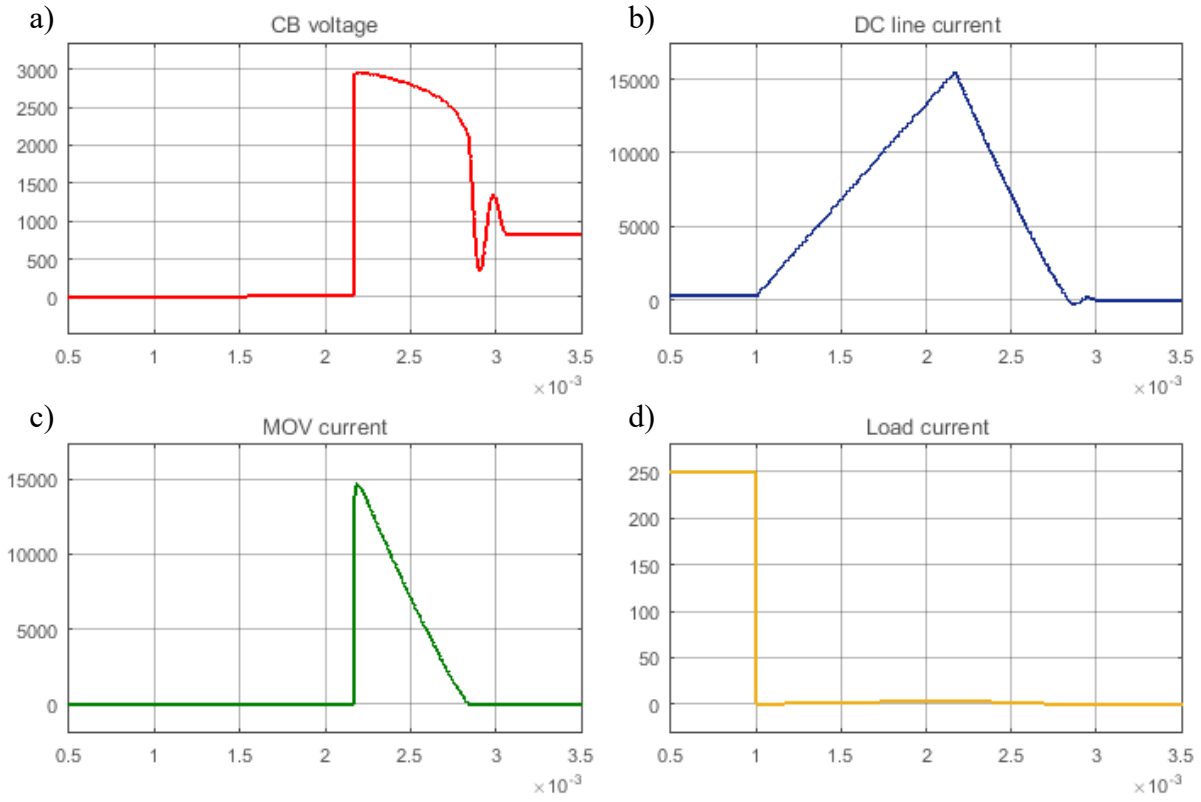

Figure 7.2 CB performance using a 4.5 kV rated IGCT based CB, C_s = 1 µF, and R_s = 10 Ω. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

Reducing the snubber capacitance *Cs* resulted in higher frequency oscillations. Since the MC is initially ignited simultaneously as the CB, high frequency oscillations may result in faster extinguishing of the arc between the contacts. This may be considered beneficial in order to limit the arcing period, which increases the expected lifetime of the MC. Figure 7.3 shows the simulated result of reducing *Cs* to 1 nF.

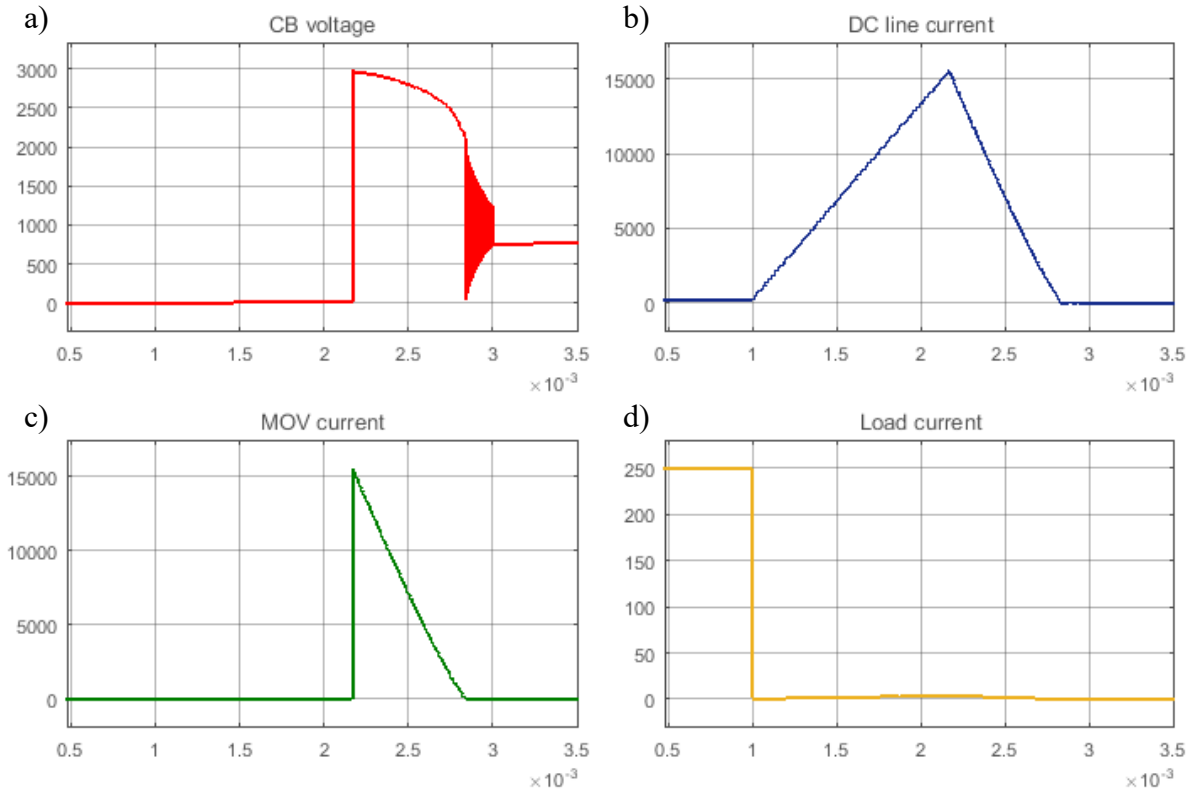

Figure 7.3 CB performance using a 4.5 kV rated IGCT based CB, C_s = 1 nF, and R_s =10 Ω. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

7.1.2 Selection of MOV Parameters

The 4.5 kV rated IGCT allows maximum clamping voltage of 3000 V. As previously discussed, it is desirable to select I_{ref}, V_{ref}, and n to be 1000 A, 3000 V, and 16, respectively. This allows the MOV, when subjected to fault currents of 16 kA, to equally share this current between the 16 columns of the MOV, such that the total MOV clamps the voltage potential to a sustainable 3000 V. The initial parameters of the Surge Arrester block utilized when analysing the snubber circuit are listed in Table 7.1.

The goal of this section is to adjust the parameters of the Surge Arrester block such that it sufficiently resemble the VI-characteristics of the MOV. When adjusting the parameters of the MOV, the MC is triggered simultaneously as the CB. The simulation result of the CB with a simultaneously triggered MC is depicted in Figure 7.4.

Table 7.1 Initial Surge Arrester block values

Parameter	Value
Protection voltage V_{ref}	3000
Number of columns n	16
Reference current per column I_{ref}	1000
Segment 1 constants $[K_1\ \alpha_1]$	[.8 50]
Segment 2 constants $[K_2\ \alpha_2]$	[1.0 12]
Segment 3 constants $[K_3\ \alpha_3]$	[0.9915 16.5]

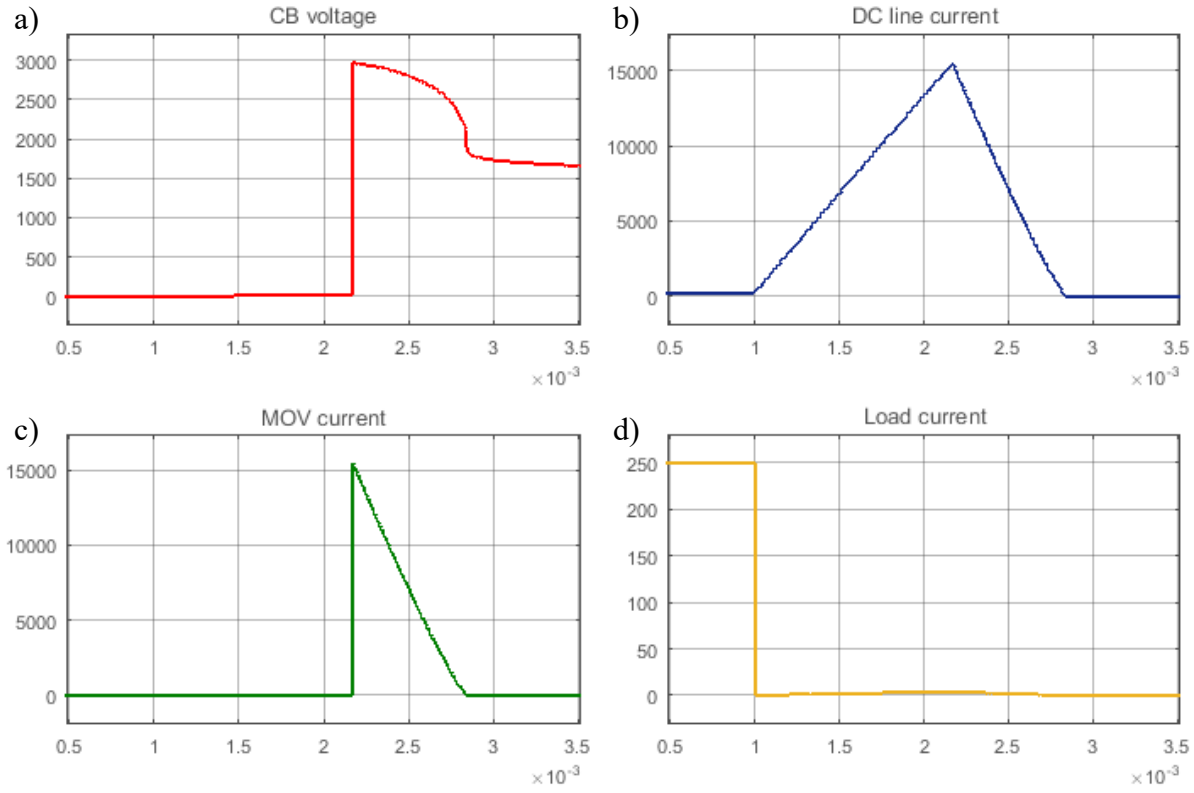

Figure 7.4 CB performance using a 4.5 kV rated IGCT based CB, K_1 = 0.8, and α_2 = 12. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

Figure 7.4 shows that the clamping voltage never reaches the intended 3000 V corresponding to the theoretical findings in Table 5.5. The slight decrease in voltage may be caused by neglecting the resistance of the fault circuit during calculations of peak current I_{fault}, resulting in the preferable MOV to have an unnecessary high current capacity. The MOV performance values collected from datasheets, were obtained through observable measurements, thus allowing the simulated waveforms to be slightly erroneous compared to the waveforms for the considered MOV found in datasheets.

Observed in Figure 7.4, the CB voltage does not instantly stabilize towards the DC source voltage. Simulation showed that the voltage potential gradually stabilizes at 1000 V after approximately 36 ms. To assure a more stable and defined performance comparable to theory, the parameters of the MOV model must be adjusted. Figure 7.5 shows the simulating result when reducing K_1 to 0.3 and α_2 to 8. From this figure, it is observed that the CB voltage waveform is more defined and stabilizes more rapidly towards the DC source voltage after the fault has been cleared. The final parameters of the MOV are listed in Table 7.2

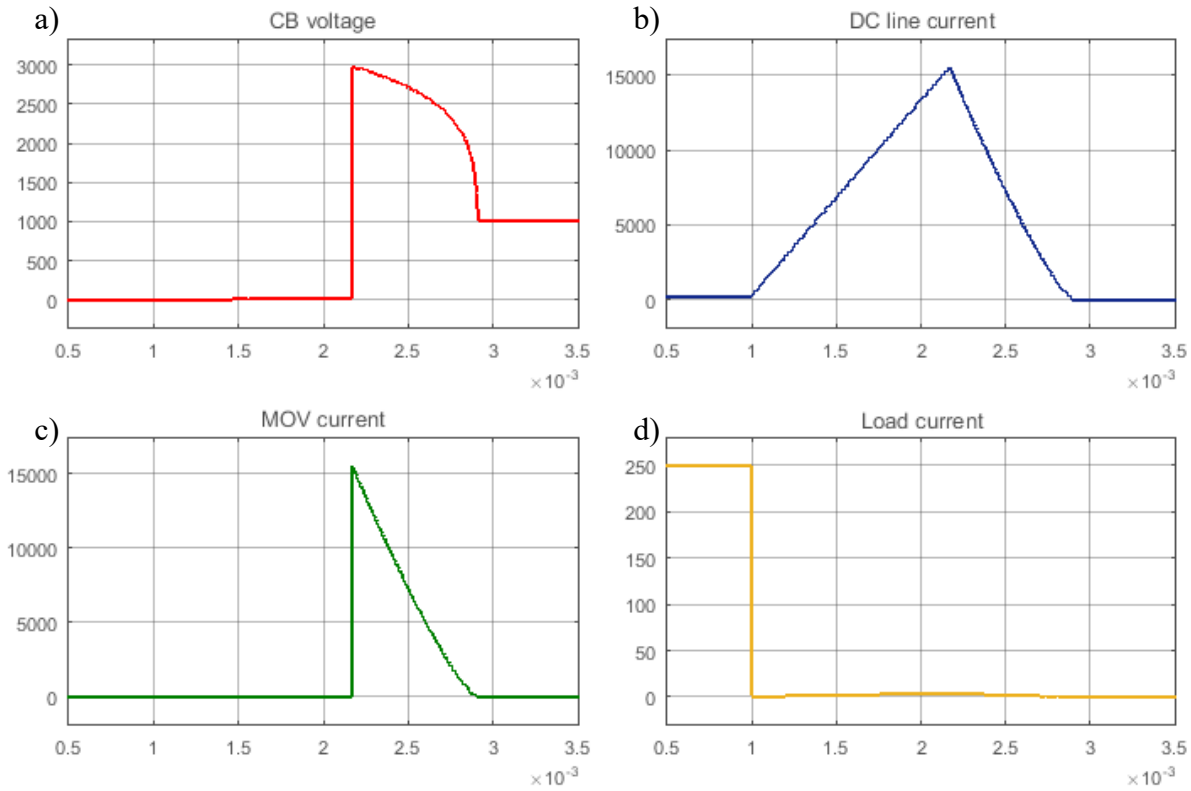

Figure 7.5 CB performance using a 4.5 kV rated IGCT based CB, K_1 = 0.3, and α_2 = 8. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

.

Table 7.2 Final Surge Arrester block parameter values

Parameter	Value
V_{ref}	3000
n	16
I_{ref} per column	1000
$[K_1\ \alpha_1]$	[0.3 50]
$[K_2\ \alpha_2]$	[1.0 8]
$[K_3\ \alpha_3]$	[0.9915 16.5]

The VI-characteristic of the final MOV is provided in Figure 7.6. The non-linear characteristics of the MOV is observable from this figure. During energy dissipation period, the current decreases with a marginal change of the CB voltage, comparable to the theoretical waveforms shown in Figure 4.4. Figure 7.6 illustrates that after the MOV has fully demagnetised the lines, and forced the current to zero, the voltage potential of the MOV drops rapidly and remains stable and equal to that of the DC source voltage of 1000 V.

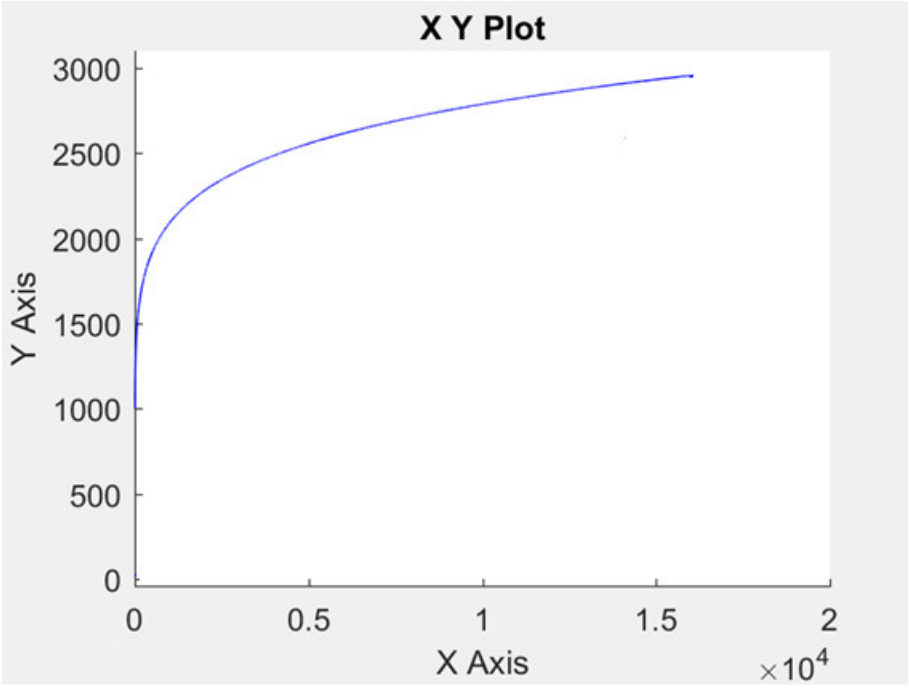

Figure 7.6 VI-Characteristics for 3000 V rated MOV, where X-axis and Y-axis correspond to current and voltage of the MOV, respectively

7.1.3 Simulated Result using the IGCT based Breaker

The final performance of the CB utilizing 4.5 kV rated A-IGCT successfully breaking a current is summarized in Table 7.3. All values are obtained from the final simulation utilizing the preferable MOV and snubber parameters, shown in Figure 7.5.

Table 7.3 IGCT based CB performance

Parameter	Value
Total fault process period, t_{tot}	1.91 ms
Peak current, I_{fault}	15.47 kA
Energy dissipation period, t_{MOV}	0.737 ms
Total energy dissipated by MOV, W_{MOV}	14.03 kJ
Conduction loss, P_{ON}[1]	0.3416 kW

1. Based on measurement and using Equation (4.10)

The conduction loss is found by measuring the voltage drop and current flow through the CB during normal operation and using Equation (4.10). Assuming uniform sharing between the 16 columns, the energy absorption per MOV device is 876.9 J, which is below the maximum energy absorbing capacity of 3800 J provided in datasheet for V112BB60 model.

7.1.4 Simulated Result using IGBT Based Breaker

Figure 7.7 shows the breaker performance of the 3.3 kV rated IGBT based CB, in the same circuit condition as of that of the IGCT based CB. Only the reference voltage V_{ref} has been adjusted such that the MOV clamps the voltage at 2000 V when conducting 16 kA. The simulated waveforms are considered sufficiently similar compared to that of the characteristic waveforms illustrated in Figure 4.2. No further adjustments of either the MOV or the snubber parameters are necessarily when simulating the IGBT based CB. Table 7.4 summarizes some performance values obtained by simulation, utilizing the 3.3 kV IGBT based CB with an MOV able of clamping the voltage at 2000 V.

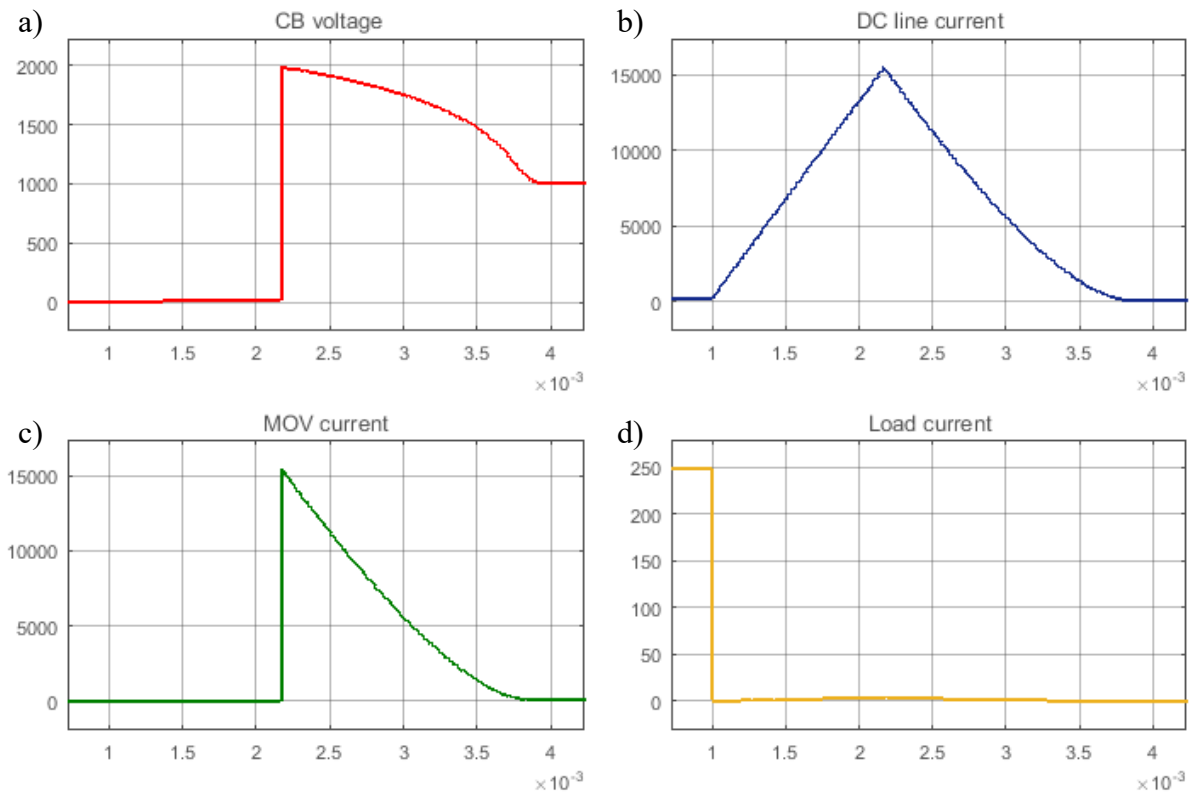

Figure 7.7 CB performance using a 3.3 kV rated IGBT based CB. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

Table 7.4 IGBT based CB performance

Parameter	Value
Total fault process period, t_{tot}	2.90 ms
Peak current, I_{fault}	15.47 kA
Energy dissipation period, t_{MOV}	1.75 ms
Energy dissipated by MOV, W_{MOV}	19.37 kJ
Conduction loss, P_{ON}[1]	1.493 kW

1. Based on measurement and using Equation (4.10)

Assuming uniform sharing between the 16 columns, the energy absorption per MOV device is 1211 J, which is below the maximum energy absorbing capacity of 2600 J given in datasheet for considered the V751BA60 model.

7.1.5 Comparison of Circuit Breaker Configurations

The comparison of the two CB configurations are based on the values obtained by simulating the CBs with their selected MOVs. Figure 7.8 compares the obtained values in a spider diagram.

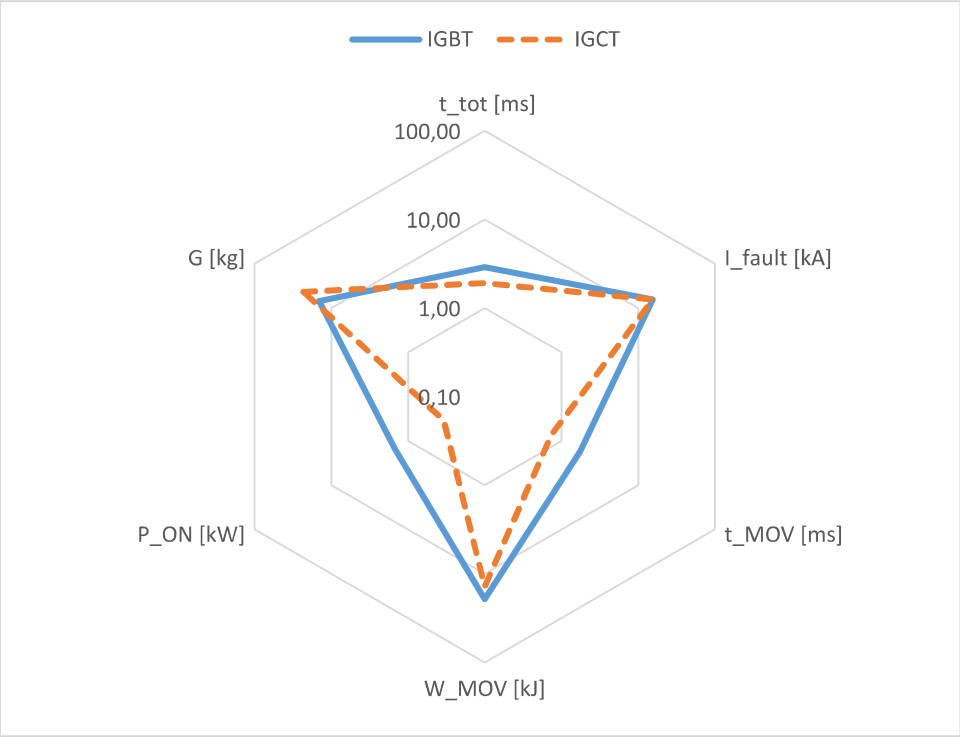

Figure 7.8 Comparison diagram of the performance IGBT and IGCT based CBs, in logarithmic scale

The high voltage rating of the CB comprising 4.5 kV rated A-IGCTs, allows utilization of MOVs with high clamping voltages. Based on theoretical discussion in section 3.2, the higher clamping voltage accounts for a more rapid fault current reduction, resulting in a shorter fault energy dissipation period. The fault energy dissipation period of the CB comprising IGCTs is 736.50 µs compared to 1.75 ms, which is the case for the CB comprising IGBTs. By allowing the clamping voltage of the MOV to increase with 1000 V, the duration of the fault process is decreased with over 1 ms. The shorter energy dissipation period, causes the energy dissipated by the MOV to be less for the IGCT based CB. Moreover, both energy dissipation periods may be considered small compared to the 38 ms energy dissipation period by the original CB concept

found in [39], indicating that both CB configurations may be overdimensioned for the considered distribution system.

Observed in Figure 7.8, the peak current values for the CB configurations are identical. The assumptions of equal detection and interruption periods of the two CB configuration results in similar interruption process prior to the breaking of the fault current. This rough assumption, cause the peak current and interruption period of the two configurations to be incomparable.

By comparing the weights of the semiconductors *G* comprising the CB configurations, it is found that the IGCT based CB is 61 % heavier than that of the IGBT based CB. Thus, a larger investment cost is indicated for the IGCT based CB. Bulky SSCB with large investment costs is found challenging for current SSCB technology. The additional weights caused by MOVs and other components are not included for this comparison. A full economical comparison is not accessible before all components of the CBs are properly selected.

The largest difference observed in Figure 7.8, considers the conduction losses of the two CB configurations. By measuring the voltage drops, and the currents through the CBs during on-state operation, the power losses of the IGCT and IGBT based CBs were obtained to be 341.6 W and 1493 W, respectively. The conduction loss of the ICBT based CB is 23 % of that of the IGBT based CB. If considering that excessive conduction losses is a major problem concerning SSCBs, the IGCT based CB seems favourable. It is beneficial to develop a CBs able of conducting with low on-state losses to ensure efficient and reliable power distribution systems. Lower conduction losses results in less heat generated on the junction of the semiconductors, which allows utilization of smaller heat sinks to sufficiently conduct the heat away from the semiconductor devices. However, the heat generated during transient events must also be considered when selecting proper heat sink.

The energy dissipated by the MOVs were found to be 14.03 kJ and 19.37 kJ for the IGCT and IGBT based CBs, respectively. As previously mentioned, the different energy dissipation periods caused by the different clamping voltage of the MOVs, impacts the energy absorbed by the MOVs. This might result in the system to be less reliable, which has to be addressed when implementing adequate heat sinks.

Based on this brief discussion, the 4.5 kV rated A-IGCT is concluded to be superior in the use of the considered CB solution, and will therefore be utilized in the following simulations.

7.1.6 Worst Case Scenario

So far, the CB has only been tested for scenarios where faults short-circuits the load. Higher currents are expected for scenarios where the fault occurs closer to the source. In cases where the fault short-circuits the source, the resulting inductance between the source and fault is considerably small. Based on Equation (3.2) the rate of rising current is expected to be significantly large. The resulting rate of rising current is found to be for the considered simulation model:

$$\frac{di}{dt} = \frac{1000\ V}{1\ \mu H} = 1\ MA/ms \tag{3.2}$$

Accounting the maximum current interrupting capability of 20 kA for the preferable CB, and the assumed constant detecting and interrupting process period of 1.15 ms, it is indicated that the proposed CB is incapable of interrupting currents occurring during worst case. Actions have to be performed such that the protection system is able to handle worst case scenarios.

Figure 7.9 illustrates the system waveforms for cases where the fault short-circuits the source.

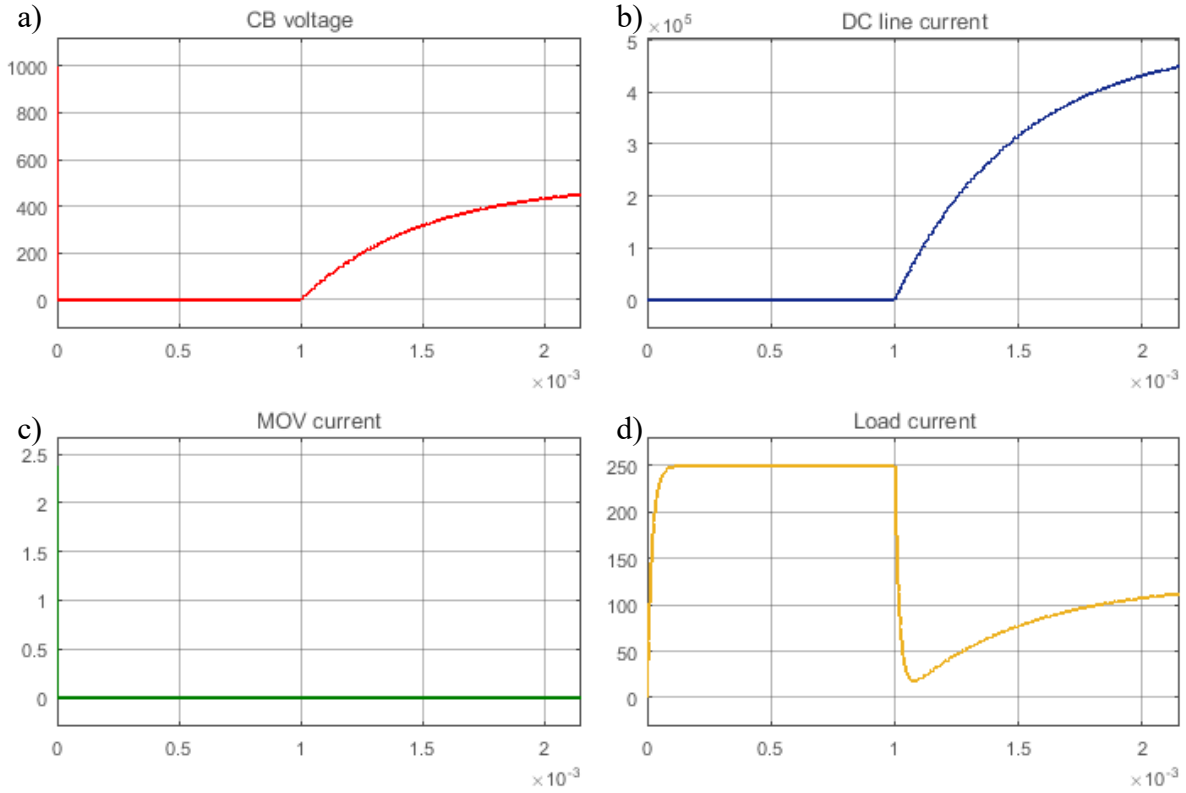

Figure 7.9 CB performance during worst case using 4.5 kV rated IGCT based CB. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

Observed in Figure 7.9, the system reaches steady state at approximately 450 kA after 1.3 ms, due to the on-state resistance of the CB and the short-circuiting resistance. The increasing voltage drop over the CB, caused by the on-state characteristics of the semiconductors in the conducting branch, accounts for excessive on-state losses, resulting in massive heat generation. The considered CB is not able to interrupt current of this level, and will most likely be thermally destroyed. If the CB was designed such that it was capable of interrupting currents of this levels, minimum 90 IGCT modules per breaker path are required in order to successfully break the current, without risking being destroyed in the process. When accounting the two breaking paths, the resulting CB is considered excessively bulky, which is considered as one of the major disadvantages regarding SSCB technology, and should therefore be avoided.

An important consideration which must be stressed when designing the system, is that all components of the system must be rated to withstand worst case peak current. This method of addressing worst case currents does not reduce the peak current, which results in excessive investment cost, due to overrated diodes in the inverter and rectifier.

The second method of addressing worst case, is by installing CLR in series to the CB. Figure 7.10 shows the CB performance when series connecting a CLR with an inductance value of 65.71 μH on the source side of the CB.

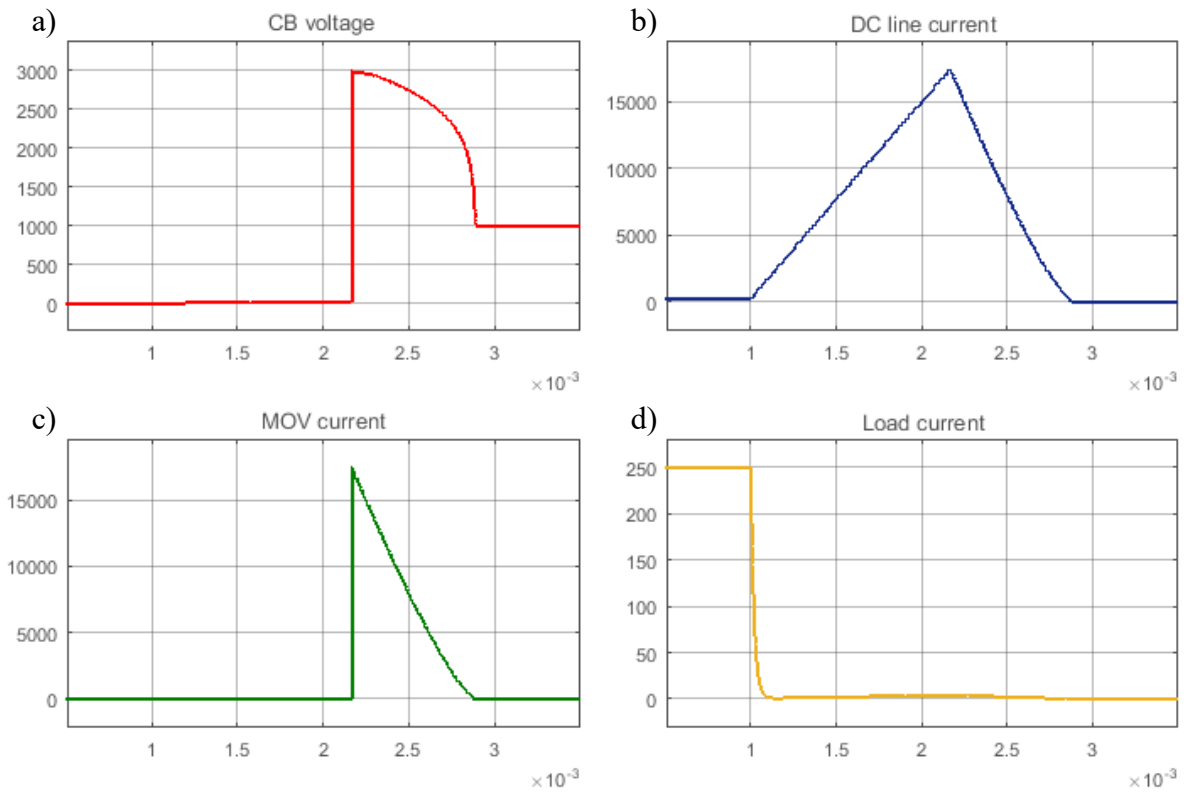

Figure 7.10 CB performance during worst case using 4.5 kV rated IGCT based CB with CLR of 65.71 µH. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

The resulting rate of rising current is slacker, providing more time for the CB to interrupt the current. The peak current is reduced to a more manageable value of approximately 17.3 kA. A protection margin of 2.7 kA is obtained during worst case, before maximum interrupting peak current of 20 kA of the CB is reached. With an energy dissipation period of 726.1 µs, and a total fault duration of 1.89 ms, the CB performance is comparable to the CB performance of the stand-alone IGCT based CB without CLR during best case scenario.

Implementing CLR limits the peak fault current for all other fault scenarios. Figure 7.11 show the result of a CB implemented with CLR, during a fault scenario where the fault short-circuits the load.

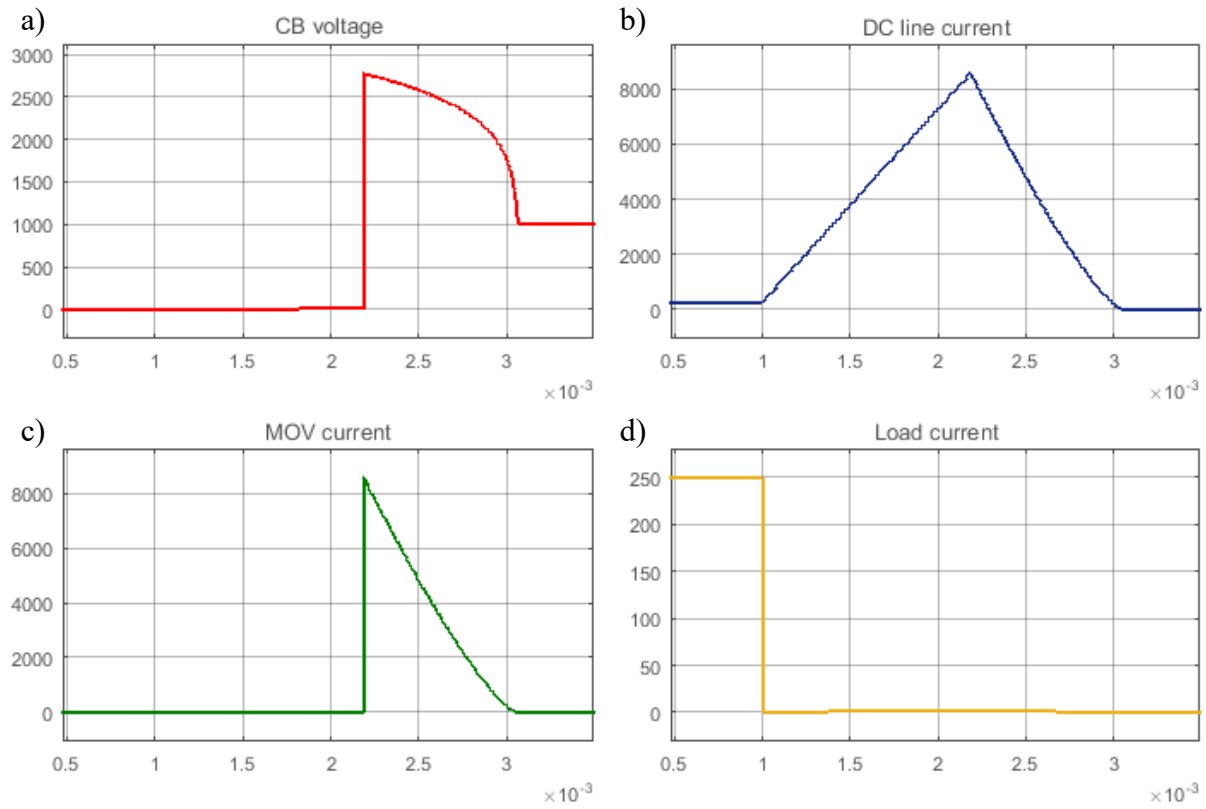

Figure 7.11 CB performance during best case using 4.5 kV rated IGCT based CB with CLR of 65.71 µH. The waveforms depicted are: a) voltage potential across the CB and MOV, b) DC line current waveform, c) current waveform through the MOV, and d) load current waveform

Compared to the simulation result of the same scenario for a system without CLR, the external inductor reduces the peak current from 15.47 kA to 8.57 kA. Due to the VI-characteristics of the MOV, the lower peak current causes the clamping voltage of the MOV to only reach approximately 2750 V. The duration of the fault energy dissipation process is therefore slightly prolonged from 736.5 µs to 882.3 µs. The marginal additional fault duration period is assumed to be manageable.

This thesis assumes the considered LVDC system to be able of withstanding fault currents of 20 kA, and will therefore continue to consider a CLR of 65.71 µH. If lower peak currents are preferable, permitting lower ratings of the system components and CBs, larger CLR may be considered.

7.2 DC Microgrid Simulation Results

This section presents the performance of the resulting CB to protect three isolated LVDC microgrid systems. The parameter values found for the standalone simulations will be used as initial values for the CB. In order to achieve the best performance, minor variations of the CB parameters were necessary in order to eliminate component stress and oscillations.

7.2.1 Rectifier System Simulation Result

The CB performance of the 4.5 kV rated A-IGCT based CB in the rectifier system, is shown for the best and worst case scenarios in Figure 7.12 and Figure 7.13, respectively. The findings obtained from the simulations are summarized in Table 7.5. The best MOV performance was achieved by increasing $\alpha_2 = 10$.

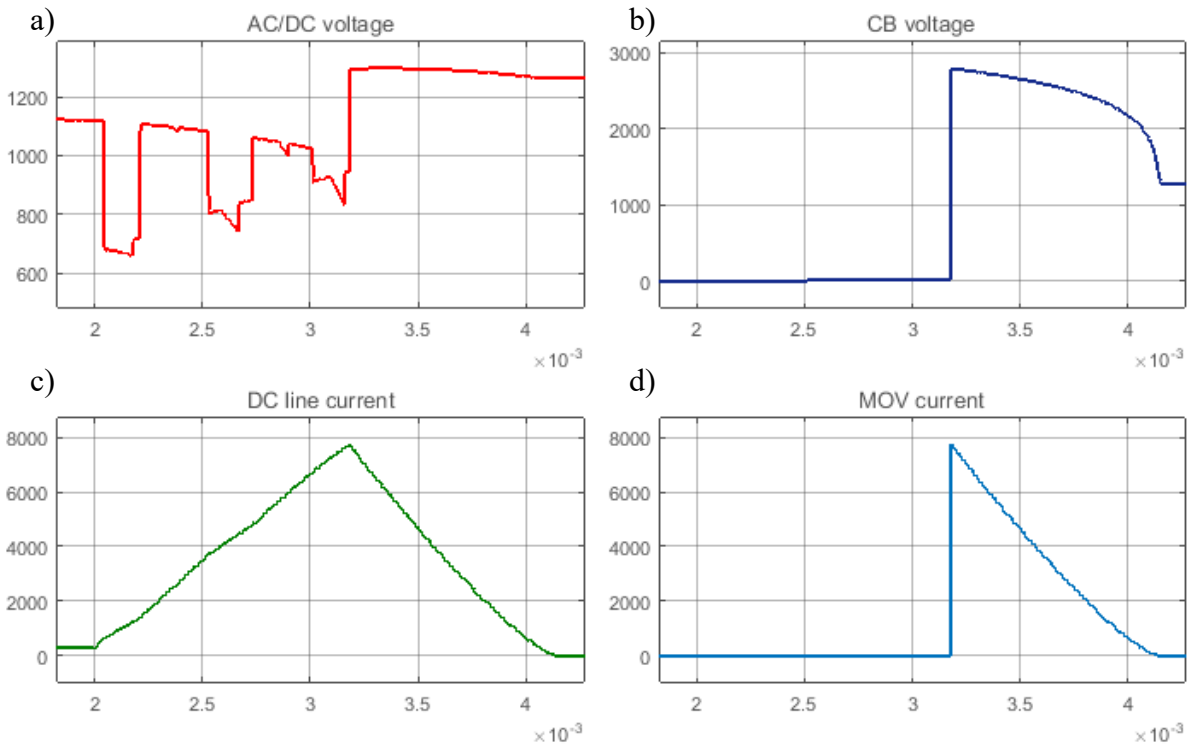

Figure 7.12 CB performance using 4.5 kV rated IGCT based CB in the rectifier system during best case. The waveforms depicted are: a) output voltage of the converter, b) voltage potential across the CB and MOV, c) DC line current waveform, and d) current waveform through the MOV

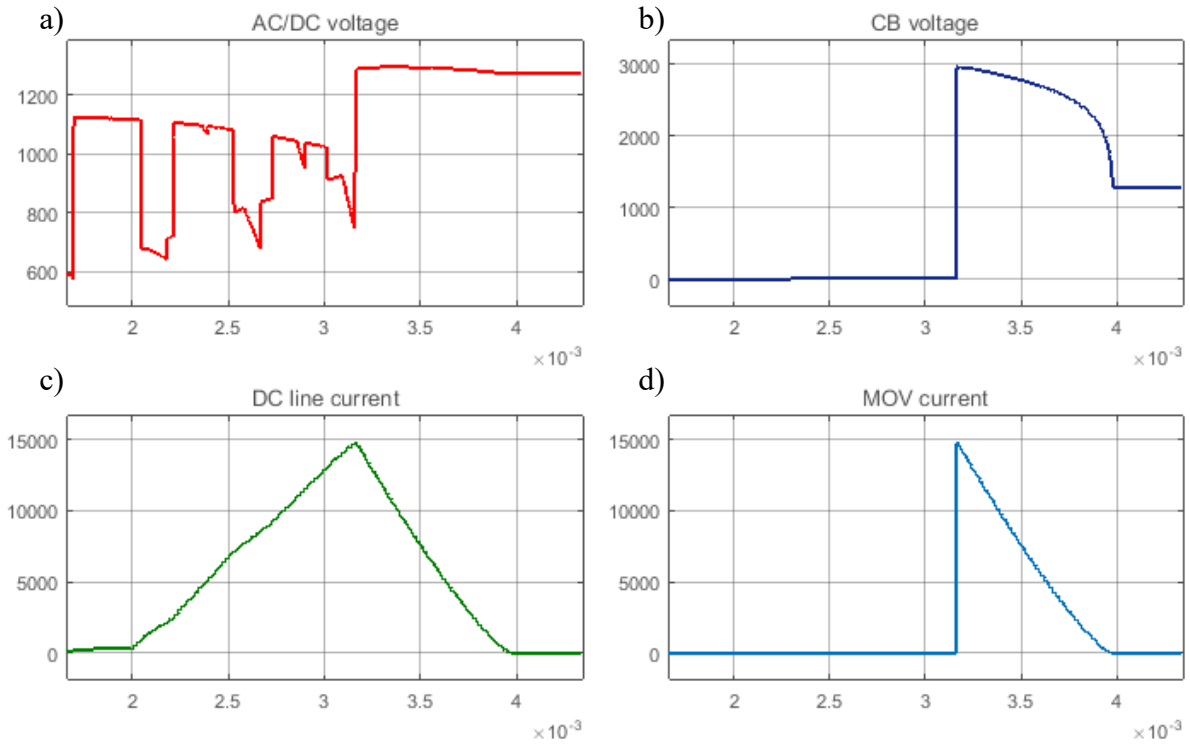

Figure 7.13 CB performance using 4.5 kV rated IGCT based CB in the rectifier system during worst case. The waveforms depicted are: a) output voltage of the converter, b) voltage potential across the CB and MOV, c) DC line current waveform, and d) current waveform through the MOV

Table 7.5 Summarized results from rectifier system simulations

Parameter	Best case result	Worst case result
Total fault process period, t_{tot}	2.17 ms	1.984 ms
Peak current, I_{fault}	7.736 kA	14.78 kA
Energy dissipation period, t_{MOV}	991.0 µs	819.32 µs
Energy dissipated by MOV, W_{MOV}	8.674 kJ	14.92 kJ

Figure 7.12 and 7.13 illustrates that the performance of the CB operates according to theory. Once the CB is triggered, the current is forced to commutate towards the MOV. The energy dissipation of the MOV for the best and worst cases are 8.647 kJ and 14.92 kJ, respectively, which are below the energy dissipation limit of 60.8 kJ. The MOV protects the CB by providing a sufficient counter voltage, influenced by the peak current, forcing the current down to zero, allowing the MC to provide galvanic isolation. The fault is totally cleared after approximately 2 ms of being initiated. From Table 7.5, it is found that the peak current does not expand beyond the current interrupting capability of 20 kA for the CB.

By observing Figure 7.12 and 7.13, the fault influence the system according to theory. The DC link capacitor begins to discharge immediately after the fault is applied to the simulation. The lines are fed inductive energy, subsequently allowing the current to increase according to equation (3.2). Due to the blocking operation of the rectifier is yet to be initiated, the inverter continues normal operation, causing the output potential to remain similar to pre-fault operations. After the IGBT valves are blocked, the converter begins to operate similar to a diode rectifier. According to theory, the output voltage of the rectifier would be:

$$V_{do} = 1.35 \cdot \sqrt{3} \cdot 560\ V = 1309\ V \tag{3.1}$$

The simulation result shows that the output voltage stabilizes at 1296 V for both cases. The slightly lower simulated output voltage of 1296 V compared to that of the theoretical value of 1309 V, is probably due to imperfections in the system, such as conduction losses of the freewheeling diodes. This voltage remains over the output of the converter after the fault has been cleared by the CB, causing a requirement for the components to withstand this voltage until normal operation can be restored. It is crucial that the selected MOV is able of clamping a larger voltage than the output potential of the diode rectifier, such that Equation (3.5) is realised, and the current is forced to zero. Based on Equation (4.3), the higher output voltage results in a slightly increased energy dissipation period.

7.2.2 Inverter System Simulation Result

The CB performance of the 4.5 kV rated A-IGCT based CB in the inverter system, during the best and worst case scenarios are shown in Figure 7.14 and Figure 7.15, respectively. The numbered findings obtained from the simulations are summarized in Table 7.6.

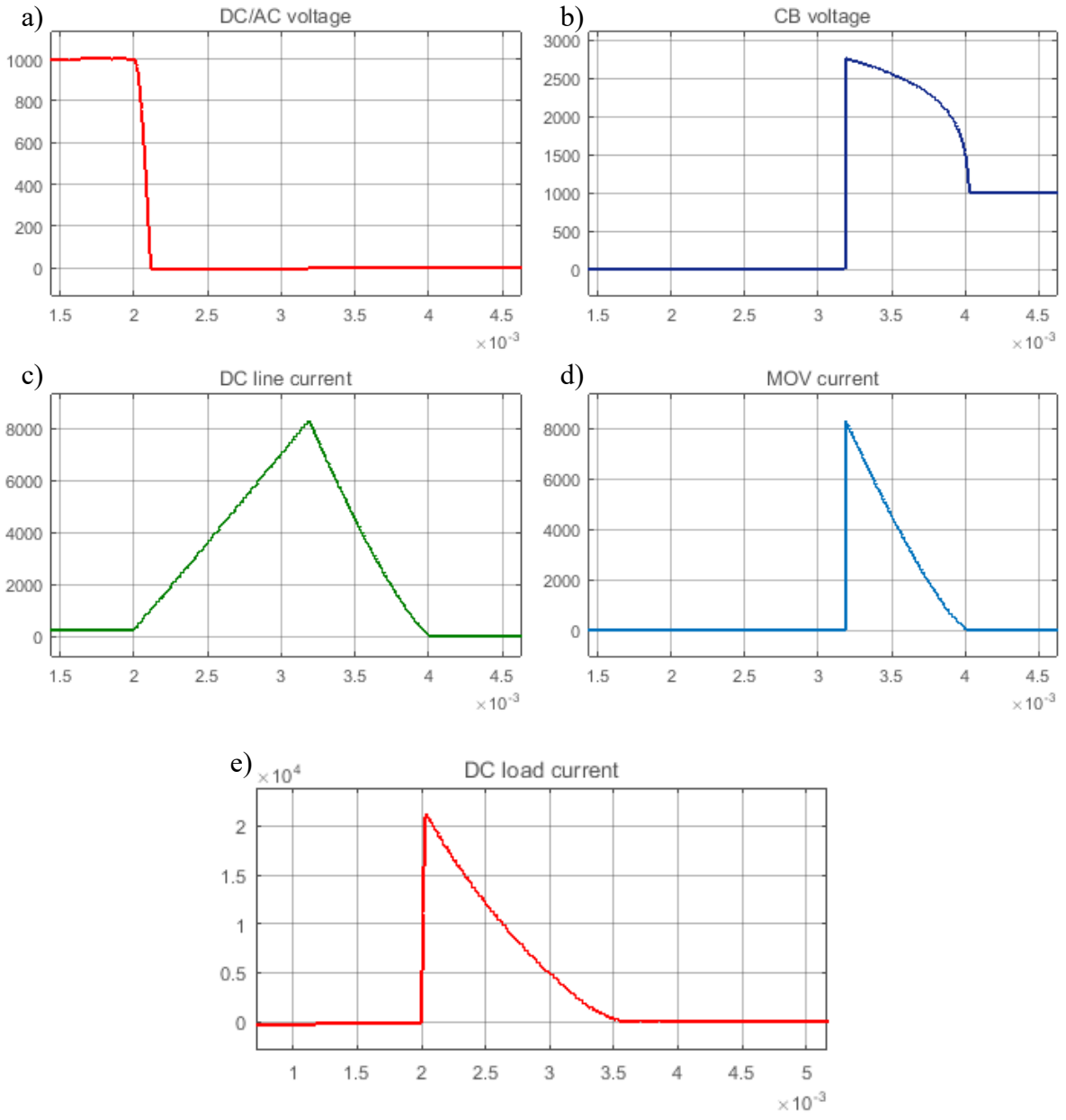

Figure 7.14 CB performance using 4.5 kV rated IGCT based CB in the inverter system during best case. The waveforms depicted are: a) output voltage of the converter, b) voltage potential across the CB and MOV, c) DC line current waveform, d) current waveform through the MOV, and e) DC load current waveform

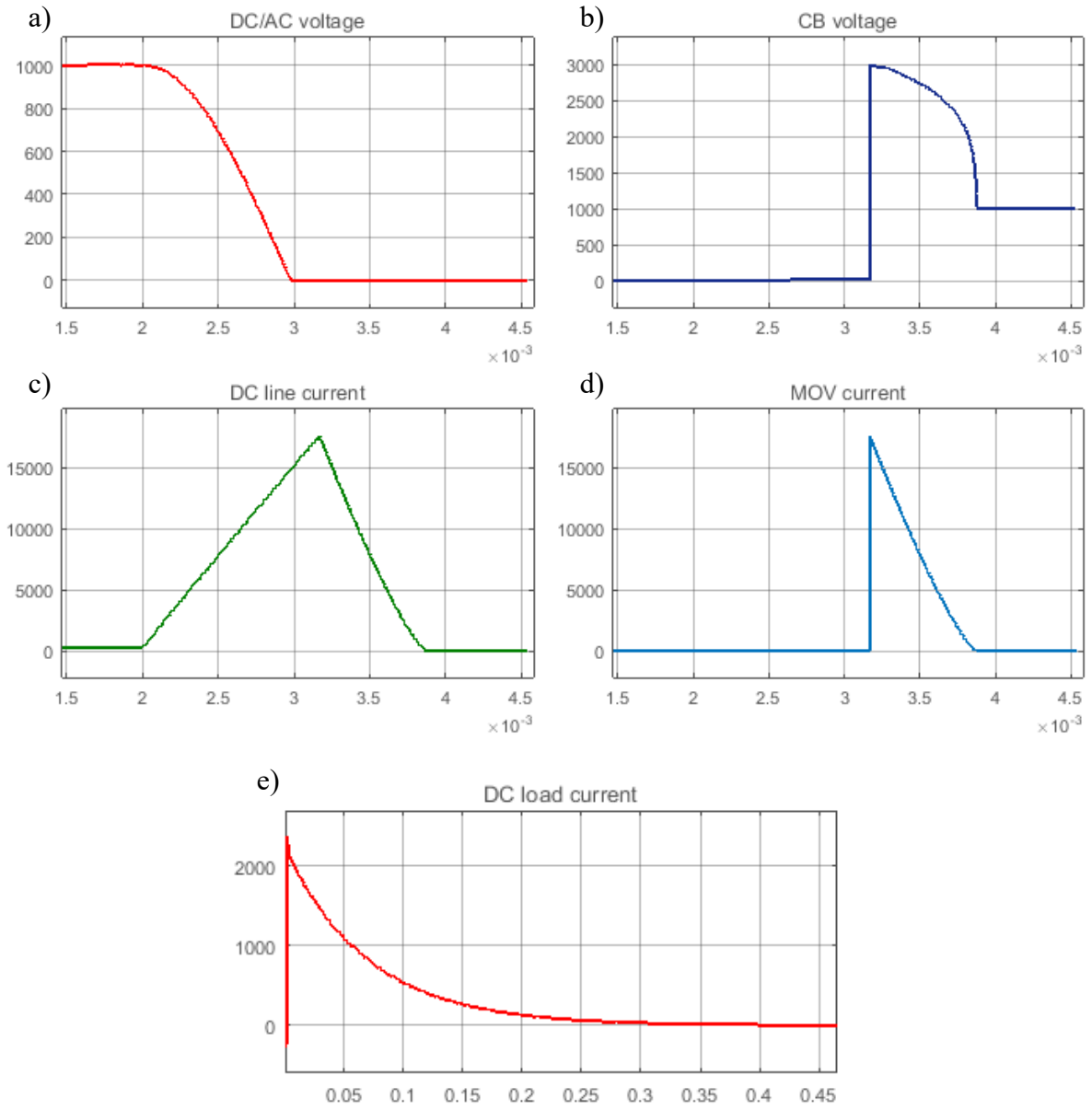

Figure 7.15 CB performance using 4.5 kV rated IGCT based CB in the inverter system during worst case. The waveforms depicted are: a) output voltage of the converter, b) voltage potential across the CB and MOV, c) DC line current waveform, d) current waveform through the MOV, and e) DC load current waveform

Table 7.6 Summarized results from inverter system simulations

Parameter	Best case result	Worst case result
Total fault process period, t_{tot}	2.04 ms	1.89 ms
Peak current, I_{fault}	8.31 kA	17.50 kA
Energy dissipation period, t_{MOV}	852.1 µs	720.73 µs
Energy dissipated by MOV, W_{MOV}	7.80 kJ	15.56 kJ
Maximum surge current, I_s	22.30 kA	2.40 kA
Residential energy dissipation period, t_s	1.67 ms	450 ms

By observing Figure 7.14 and Figure 7.15, the CB operates promising according to theory. The current commutate towards the MOV, after the CB is triggered. As seen in Figure 7.15, the worst case fault current reaches a relatively large value of 17.50 kA before being broken. The high peak current might be a result of emulating the unfocused part of the network using an ideal voltage source. This causes the CB performance of the CB in the inverter system to be comparable to that of the stand-alone system, shown in Figure 7.10 and Figure 7.11. The MOV provides a sufficient counter voltage, influenced by the current peak, forcing the current down to zero, allowing the MC to provide galvanic isolation. The two cases of faults are properly cleared within roughly 2 ms after the faults are initiated. The energy dissipated by the MOV does not reach the maximum energy dissipation limit of 60.8 kJ.

Figure 7.14 and 7.15 illustrates that once the fault is applied to the system at t = 2 ms, the DC link capacitor is completely discharged, causing the voltage potential of the inverter to drop to zero. The lack of energy absorbing devices, such as MOVs and energy absorbing snubbers, on the converter side of the fault, causes the residential energy of the capacitor to discharge though the resistive elements of the fault circuit. It is observable that the size of the inductance on the

converter side of the fault, influence the peak and duration of the discharged current. When the fault is applied close to the source, the residential dissipation period is fairly long, caused by the larger inductance limiting the rate of decreasing current. For faults applied closer to the load, the inductance is smaller, resulting in shorter residential dissipation period with a trade-off relationship of increased maximum current.

The same amount of cumulated energy is released through the line inductance such that Equation (7.1) and (7.2) applies for both scenarios:

$$W_C = \frac{1}{2} C_L \Delta V_C^2 = \frac{1}{2} L I_{peak}^2 = constant \tag{7.1}$$

$$= \int^{t_c} v_{line} i_{line} dt = \frac{1}{2} V_{line} I_{line} t_c \tag{7.2}$$

where

W_c realised energy in the DC link capacitor [J];

C_L DC link capacitance [F];

ΔV_C voltage drop of the DC link capacitor [$\Delta V_C = V_C$, when fully discharged] [V];

I_{peak} peak line current [A];

t_c residential energy absorbing period [s].

The converter may exhibit considerably large current stress. The components must be rated such that they are capable of withstanding surge currents for a longer periods of time. This problem might be addressed by utilizing energy absorbing snubbers. Due to scope limitation, this problem was to some extent managed by selecting a small DC link capacitor of 0.5 mF, restraining the maximum capacitor current to some degree.

7.2.3 Battery System Simulation Result

The CB performance of the 4.5 kV rated IGCT based CB in the battery system model, during the best and worst case scenarios are shown in Figure 7.16 and Figure 7.17, respectively. The values obtained from the simulations are summarized in Table 7.7.

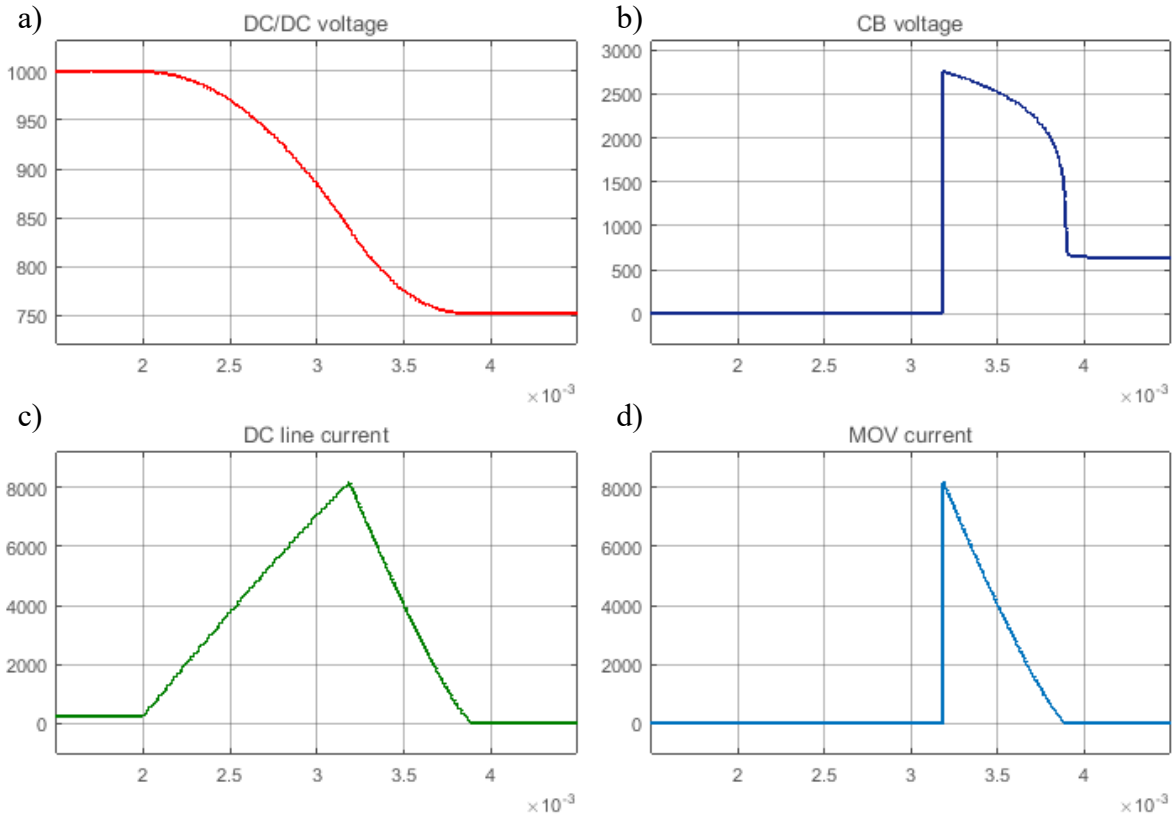

Figure 7.16 CB performance using the 4.5 kV rated IGCT based CB in the battery system during best case. The waveforms depicted are: a) output voltage of the converter, b) voltage potential across the CB and MOV, c) DC line current waveform, and d) current waveform through the MOV

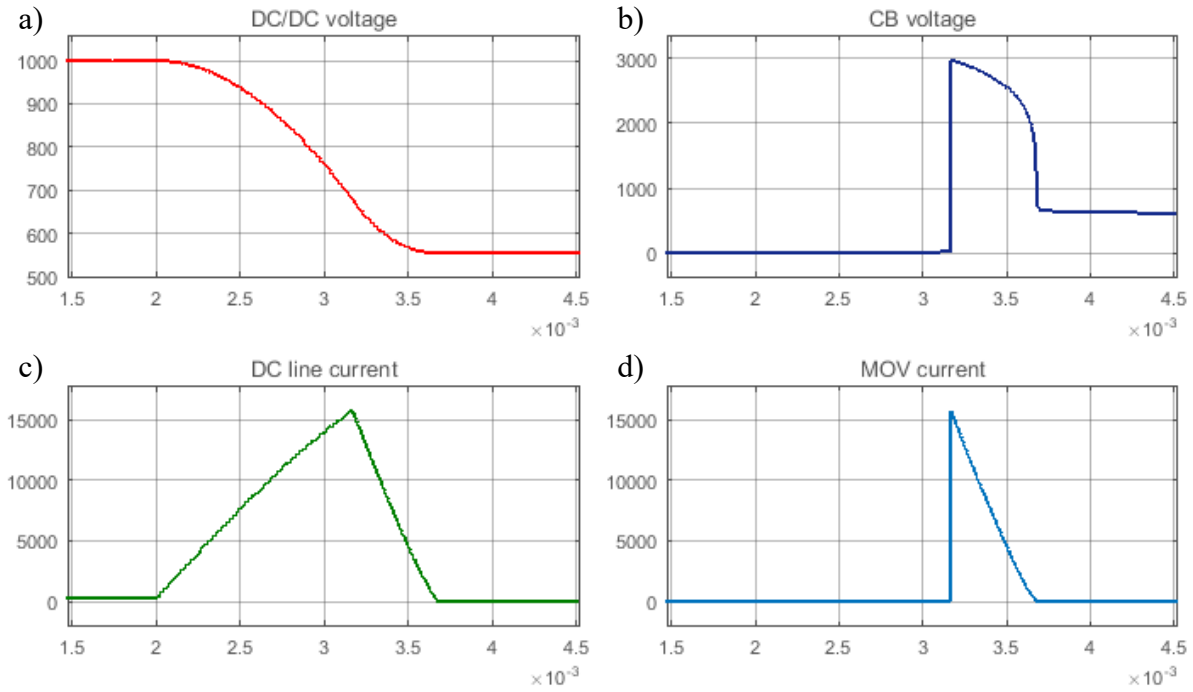

Figure 7.17 CB performance using the 4.5 kV rated IGCT based CB in the battery system during worst case. The waveforms depicted are: a) output voltage of the converter, b) voltage potential across the CB and MOV, c) DC line current waveform, and d) current waveform through the MOV

Table 7.7 Summarized results from battery system simulations

Parameter	Best case result	Worst case result
Total fault process period, t_{tot}	1.895 ms	1.679 ms
Peak current, I_{fault}	8.20 kA	15.72 kA
Energy dissipation period, t_{MOV}	709.3 µs	512.55 µs
Total energy dissipated by MOV, W_{MOV}	6.73 kJ	10.37 kJ

It is indicated in Figure 7.16 and Figure 7.17, that once the fault is applied to the simulations, the DC link capacitor discharges, consequently feeding the fault. The fault current rises with a rate related to the amount of inductance between the fault and the capacitor. After the CB has been triggered, it operates according to theory for both cases. The fault current commutates towards the MOV where the fault energy is dissipated, causing the current to reduce to zero. The energy dissipated by the MOV during best and worst case, are 6.73 kJ and 10.37 kJ respectively. Both values are below the energy dissipation limit for the MOV of 60.8 kJ.

The DAB IBDC is blocked simultaneously as the CB, only allowing the current to conduct through the freewheeling diodes. Because of this, the first full-bridge is incapable of converting DC power towards AC power, which results in no induced voltage on the primary winding of the transformer, and consequently, no induced voltage and current on the secondary winding of the transformer. After the switching signals of the DAB IBDC are blocked, the converter is unable of building up the charge of the capacitor, causing the voltage potential across the capacitor to remain constant after the fault current has been cleared.

A DC link capacitor of 30 mF was selected to avoid fast saturation of the system during worst case. The rate of which the capacitor is discharged is influenced by the line inductance. Observed by comparing Figure 7.16 and Figure 7.17, it is indicated that the capacitor discharge more rapidly through a small inductor, compared to that of a large inductor. The effect of the dropping voltage potential on the CB performance, is mainly slightly reduced energy dissipation periods, according to Equation (4.3) in theory.

8 Discussion and Conclusion

8.1 System Description and crucial Aspects of Fault

Chapter 2 presented a simple LVDC microgrid divided into three segments, comprising typical components, such as loads and sources operating at AC power, and batteries. Specific converters were selected and developed for each component, to achieve sufficient interconnection to a DC distribution network of 1000 V. Chapter 3 reviewed the theory regarding the subsequent effects a short-circuit fault has on the operation for LVDC microgrids, and developed a theoretical background for which the parameterization of the CBs would be based on, and were referred to when analysing the result from the simulations.

The major problem regarding LVDC microgrids, are their typical small system inductances compared to that of traditional HVDC and AC systems, which results in significantly steep rise of fault current. LVDC microgrids normally utilize slow operating CB based on MCB technology, with a critical consequence of excessive peak currents. All electric components of the system must be rated according to the largest possible peak current occurring during short-circuit faults, consequently resulting in expensive overdimensioned system components. It is vital to develop CBs capable of fast interruption, limiting the peak current to sustainable levels, subsequently improving the reliability of the system, and supports cost efficient LVDC microgrids.

Only minor parts of the network are usually victims of short-circuit fault simultaneously, and unnecessary power shutdowns are considered expensive, and should be avoided if possible. LVDC microgrids usually comprises several sources with inconsistent availability, which are able of cooperate with each other to supply the loads power undisturbed. To allow the healthy part of the network to continue operation undisturbed by faults, several CBs must be implemented such that the protection system is able of properly isolate the faulty part of the network. These CBs operates in the majority of time in on-state. It would be beneficial to develop CB with low conduction losses to ensure that an efficient distribution network is obtained.

8.2 CB Design and Parameterization

Based on previous work [1], a bidirectional SSCB based on two RB-IGCT connected in anti-parallel was selected as the base circuit design for this thesis. Chapter 4 presents the operation

principles for this CB, and develops design guidelines for the components comprising the considered CB, which was used for parameterization.

Thermal concerns for the considered CB were assembled in chapter 4. Semiconductor devices are provided with their maximum intrinsic temperature T_{jmax} by manufacturers. If this temperature is exceeded, important properties are lost, such as low conduction loss, and current breaking capability. Heat sinks must be properly selected to dissipate the heat away from the devices, which is generated due to on-state losses of the semiconductor devices. MOVs are provided with their maximum operating temperature T_{MOVmax} and maximum power generation P_{MOVmax} by manufacturers. The leakage current of the MOV during normal operation is negligible, due to the small voltage drop across the MOV caused by the parallel connected CB. After the fault has been successfully interrupted, the voltage potential across the MOV is equal to that of the DC source, which allows for higher leakage current due to the VI-characteristics of the MOV. MOVs have negative temperature coefficient, resulting in self-amplifying effect where more leakage currents causes higher temperatures, which again allows for higher leakage currents. Higher temperature leads to increased conduction losses, and eventually failure if P_{MOVmax} for the considered MOV, is exceeded. Therefore, it is necessary to consider MCs, which provides physical isolation between the source and the fault, and eliminates leakage currents following a fault interruption process.

Chapter 5 presents the parameterization of the CB, where IGCT and IGBT modules with sufficient ratings were considered to be used for further simulation. Selecting modules with high current interruption capability is preferred in order to restrict the size of the resulting CB. The clamping voltage of the MOVs were selected such that when conducting considered peak current, its counter voltage would never exceed 66.7 % of their rated voltage of the considered semiconductor device.

Based on low conduction losses, high current interrupting capability, the size of the resulting CB and available MOVs, a 3.3 kV rated IGBT and a 4.5 kV rated A-IGCT were chosen to be further considered for simulations. The IGCT has a higher current interrupting capability, resulting in each breaker path to require 4 parallel connected devices per breaker path to be able of interrupting the considered fault current, compared to 6 parallel connected devices per breaker path, which was necessary for the IGBT based CB.

The parametrization was not performed considering the worst case scenario, where the fault short-circuits the source, resulting in significantly small inductances, and consequently significantly steep rate of fault current. A constant detection and interruption period were

assumed for both CB configurations. Within this period of time, the worst case fault current would exceed the current interruption capability of both CB configurations. Two methods of handling worst case scenario were presented. Either the numbers of parallel connections of the CBs could be increased, such that the CBs would be able of breaking worst case currents, or CLRs could be implemented to provide a slacker rise of fault current. The first method was found to result in bulky CBs, with consequently high investment costs. Additionally, the worst case peak current would remain excessive, resulting in overdimensioned system components. Series connecting CLRs would significantly reduce the possible peak current, and were therefore considered the superior solution. The value of the CLR was based on lowest current interrupting capability resulting from the final parameterization the CBs. If lower currents are preferable, with lower system component ratings and less bulky CBs, larger CLR may be considered, with a trade-off with increased cost and mass of the CLR, and poorer power flow control due to a stiffer grid.

8.3 Modelling and Simulations

Chapter 6 described the design of the models complied for Matlab® Simulink, and chapter 7 presented the main result obtained from the simulations.

8.3.1 Stand-Alone Model and comparison of the two CB Configurations

A simple test circuit was modelled in order to compare the performance between the two considered CB configurations, comprising either a total number of 8 parallel connected 4.5 kV rated IGCTs, or 12 parallel connected 3.3 kV rated IGBTs. The test model circuit was considered very simple, comprising a stiff voltage source, a load, and a line inductance model.

The identical interruption periods assumed for both configurations resulted in identical peak currents. It would have been more accurate to assume a slightly faster interruption period for the IGBT. The higher ratings of the IGCT allowed for utilization of larger MOVs, which reduced the energy dissipation period with 1 ms. Due to the shorter dissipation period, the MOV of the IGCT based CB had to dissipate less energy. The mass of the CB comprising 3.3 kV rated IGBT was found to be 62 % of that of the CB comprising 4.5 kV rated IGCT, indicating a more economical configuration of utilizing IGBTs for the considered CB. Using on-state parameters provided by manufacturers in datasheets, the conduction loss of the IGCT based CB was found to be 23 % of that of the IGBT based CB. Due to excessive conduction loss is one of the major concerns regarding SSCB technology, the IGCT based CB appears to be the most

promising solution. Implementing CLRs to handle worst case fault scenarios were simulated and recommended for further simulations. The CLR limited the peak fault current for all cases.

8.3.2 Microgrid System Model

To limit the scope of work and focus only on what is considered most relevant for studying CB performance, it became necessary to simplify the microgrid evaluated in chapter 2. Switching and conduction losses for the converters were not considered, and no converter control were implemented for the simulations. The deep investigation of control and modulation schemes for each converter were left out of investigation for this thesis. The microgrid was divided into three isolated systems, focusing on one converter at the time, where the remaining parts of the system were simplified using resistive loads and ideal sources.

The preferred CB with CLR was shown to operate sufficiently for all simulations. After the CB was triggered, the CB forced the fault current to commutate towards the MOV where the fault energy was dissipated, causing the current to reduce to zero. The fault current interruption capability of the IGCT based CB of 20 kA was never reached. The energy dissipation never exceeded the energy dissipation limit for the selected MOV of 60.8 kJ. The MC extinguished instantly after first zero crossing of the current, providing galvanic isolation between the fault and the source. The dissipation of the fault energy was completed approximately 2 ms after the faults were applied to all systems.

To protect the IGBT valves of the considered converters during fault, they were provided blocking signals simultaneously as the CBs. This caused the converters to force the current to conduct through its anti-parallel diodes.

For the rectifier system, the full-bridge rectifier would operate similar as a diode rectifier, thus increasing the output voltage accordingly. To force the current down to zero, the counter voltage of the MOV must be greater than of that of the output of the rectifier. The resulting energy dissipation periods were slightly extended relative to that of the other systems due to the increased source voltage, but were not considered problematic due to the large energy capacity of the MOV.

The most critical problem for the inverter system, was the residential discharge of the DC link capacitor. After the fault occurred, the DC link capacitor would fully discharge, which resulted in excessive surge current for the right side of the fault, which would consequently derate the components of the inverter if not properly addressed. Implementing energy absorbing snubber

circuit for the DC link capacitor is recommended to restrict the surge current to manageable values.

The protection system of the battery system performed fault operations successfully. After the faults were applied to the simulations, the DC link capacitor discharged through the inductive elements of the circuit, contributing energy to the fault. After the converter conceived proper blocking signals, the left full-bridge of the DAB IBDC was incapable of converting the power into AC, due to the freewheeling diode path. The lack of current variations of the transformer, caused it to block power transferred between the input and output of the DAB IBDC. The converter was incapable of maintaining its voltage potential, causing the capacitor to remain at voltage potential corresponding to its level of discharge.

8.4 Main Conclusions

- The 4.5 kV rated A-IGCT based CB was considered superior to the 3.3 kV rated IGBT based CB mainly due to its high current interrupting capability and ability to conduct with 23 % of the losses of the IGBT based CB.
- Based on simulations, the 4.5 kV rated IGCT based CB is capable of successfully interrupting fault currents up to 17.5 kA at 3000 V, and clear the fault within approximately 3 ms after being initiated, for a 1000 V DC microgrid system.
- The CB was able of interrupting fault of both directions.

8.5 Potential Improvements and Errors

The parameterization may have been improved by considering the size and weight of all the components comprising the CB. Other IGBT modules with lower ratings would then have been considered for the simulations, which might have changed the outcome of this report. In this thesis, the maximum allowed MOV was selected according to the 66.7% limit for the clamping voltage and CB ratings ratio. The clamping voltage of the MOV used in the original 2.5 kV RB-IGCT based SSCB, was 1.6 kV and resulted in an energy dissipation period of 35 ms, which was found sufficient in that report. The energy dissipation period of roughly 1 ms indicates that the entire CB would have been overdimensioned for the considered 1000 V DC microgrid. A smaller MOV would increase the dissipation period, but ensure a more compact and economical CB solution.

Deviation of the simulation results and theory might be due to lack of details in the simulation model and observable data obtained from datasheets.

9 Future Work

Suggestions for future work are presented in this final chapter.

- For future work, the system models considered for this thesis, may be comprised into one model and tested properly, for various fault placements. A proposed composition of the three systems are provided in Appendix C. The fault detection method may also be considered for future work.
- Thermal equivalent models may be built for the CB and MOV to be simulated in Simulink. This allows for a better understanding of heat sink requirements, during normal and transient operations, such that the components always operate at optimal temperatures.
- Assembling a better guideline for selecting MCs for galvanic isolating purposes, studying the component stress due to arc ignition, is suggested in order to select the best MC module for the considered circuit.
- The investment costs of the resulting designs influence the selection of the most promising CB configuration. A cost study may be assembled, which considers the size and cost of the components comprising the CBs.
- Due to the indication that the most promising CB is overdimensioned, the CB may be investigated to be tested for MVDC applications.
- A derated version of the stand-alone model may also be built to be tested for laboratory experiments. The CB may be tested for heat generation due to repetitive current interruption.

Biography

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Appendix A: Calculations

Given System Parameters and Assumptions used for calculations

Table A.1 Given system parameters and assumptions

Parameter	Value
Line distance, l	40 m
Nominal current, I_o	250 A
Current density, j	6 A/mm^2
Permeability constant, μ	$4\pi \cdot 10^{-7}$ H/m
Detection time period, t_{det}	1 ms
Threshold time period, I_{th}	500 A
Interrupting time period, t_{int}	150 µs
Instant of fault injection for stand-alone model, t_{fault}	1 ms
DC source voltage, V_{DC}	1000 V
Stray inductance, L_{stray}	1 µH

Line Inductance

Known system parameters and assumptions:

Cross section area *S:*

$$S = \frac{I_o}{j} \tag{A.1}$$

$$= \frac{250A}{6\ A/mm^2} = 41.67\ mm^2$$

Based on this the wire diameter is simply calculated using following formula

$$S = \pi r^2 = \pi \left(\frac{d}{2}\right)^2 \tag{A.2}$$

The diameter *d* is derived as:

$$d = \sqrt{4 \cdot \frac{41.67mm^2}{\pi}} = 7.27\ mm \tag{A.3}$$

The diameter was rounded to nearest decimal as 7 mm.

From equation (2.5) the line inductance of a 40 m line segment can be calculated as:

$$L_{line} = 2 \cdot 4000 \left\{ \ln\left(\left(\frac{2 \cdot 4000}{0.7}\right) \left(1 + \sqrt{1 + \left(\frac{0.7}{2 \cdot 4000}\right)^2}\right)\right) - \sqrt{1 + \left(\frac{0.7}{2 \cdot 4000}\right)^2} + \frac{4\pi 10^{-7}}{4} + \left(\frac{0.7}{2 \cdot 4000}\right) \right\} = 74.3\ \mu H \tag{2.5}$$

Worst Case Peak Current Calculation

Using equation 4.2, the threshold time period is found:

$$t_{th} = \frac{(500 - 250) \cdot 1\mu H}{1000V} = 0.25\ \mu s \tag{4.2}$$

Based on this information, the peak current will

$$I_{fault} = 500A + \frac{1000V}{1\ \mu H}(1.15\ ms) = 1150.5\ kA \tag{5.1}$$

Pulse Block Times for Stand-alone Model without CLR

Best Case

Using equation (4.2), the threshold time period is found:

$$t_{th} = \frac{(500A - 250A) \cdot 74.3\mu H}{1000V} = 18.58\ \mu s \tag{4.2}$$

When a fault occurs after 1 ms, the triggering period of time for the pulse block controlling the CB is found by summarizing the different estimations such that:

$$t_{pulse} = t_{fault} + t_{th} + t_{det} + t_{int} \tag{A.4}$$

$$t_{pulse} = 1\ ms + 18.58\ \mu s + 1\ ms + 150\ \mu s = 2.16858\ ms \tag{A.4}$$

Worst Case

It is assumed that the total inductance between the fault and source is 1 µH.

$$t_{th} = \frac{(500A - 250A) \cdot 1\mu H}{1000V} = 0.25\ \mu s \tag{4.2}$$

Using Equation (A.4), the triggering signal is found to be:

$$t_{pulse} = 1\ ms + 0.25\ \mu s + 1\ ms + 150\ \mu s = 2.15025\ ms \tag{A.4}$$

Pulse Block Times for Stand-alone Model with CLR

The CLR value is 65.71 µH.

Worst Case

If utilizing a CLR, during worst case scenario, the resulting threshold time is:

$$t_{th} = \frac{(500A - 250A) \cdot (1\mu H + 65.71\mu H)}{1000V} = 16.68\ \mu s \qquad (4.2)$$

Using Equation (A.4), the triggering signal is found to be:

$$t_{pulse} = 1\ ms + \ 16.68\ \mu s + 1\ ms + 150\ \mu s = 2.16668\ ms \qquad (A.4)$$

Best Case

If the fault were to occur at the load side of the line, the line inductance prolongs the threshold current:

$$t_{th} = \frac{(500A - 250A) \cdot (1\mu H + 65.71\mu H + 74.3\mu H)}{1000V} = 35.25\ \mu s \qquad (4.2)$$

Using Equation (A.4), the triggering signal is found to be:

$$t_{pulse} = 1\ ms + \ 35.25\ \mu s + 1\ ms + 150\ \mu s = 2.18525\ ms \qquad (A.4)$$

Appendix B: Pre-Simulations of Systems finding Threshold Time Periods

Rectifier System Model

Best Case Scenario

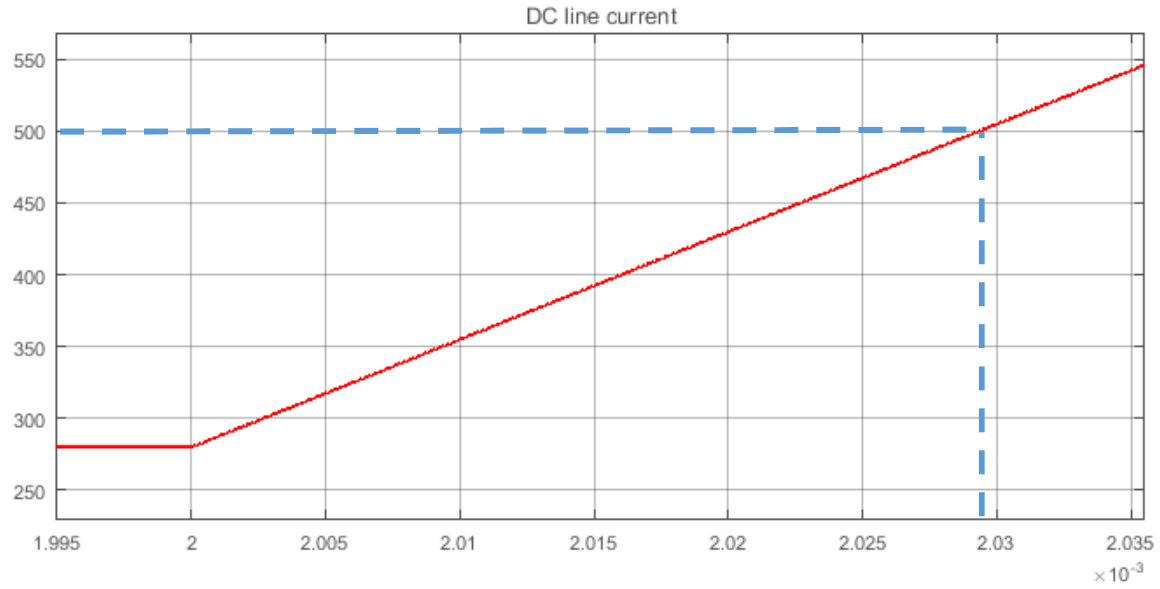

Figure B.1 Pre-fault simulation rectifier model during best case scenario

Threshold time period is found to be 29.47 µs.

Worst Case Scenario

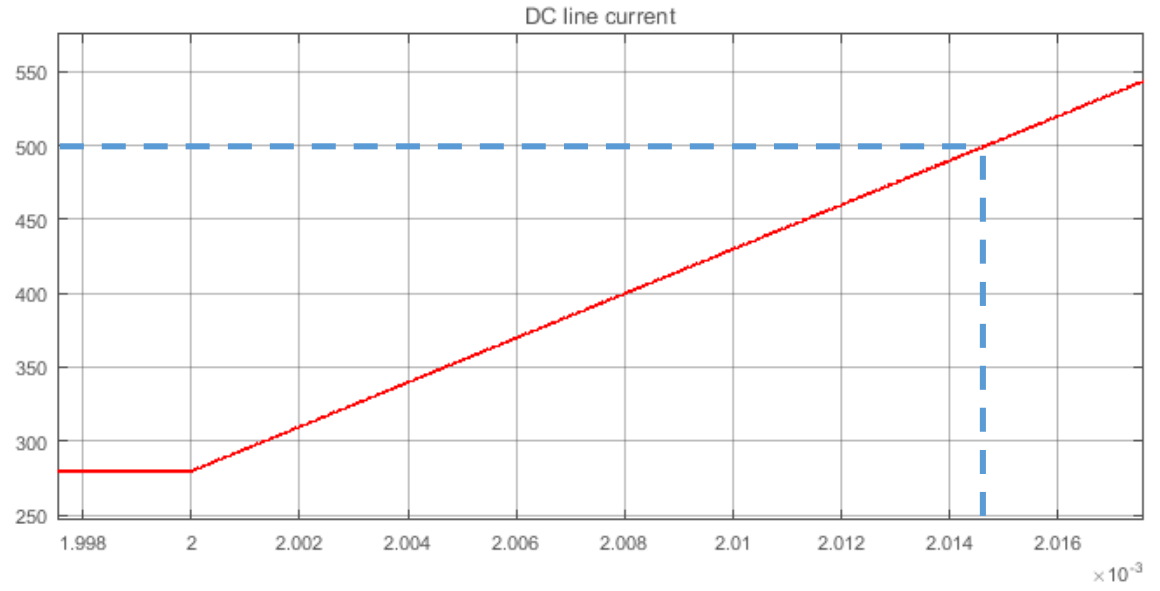

Figure B.2 Pre-fault simulation rectifier model during worst case scenario

Threshold time period is found to be 14.78 µs.

Inverter System Model

Best Case Scenario

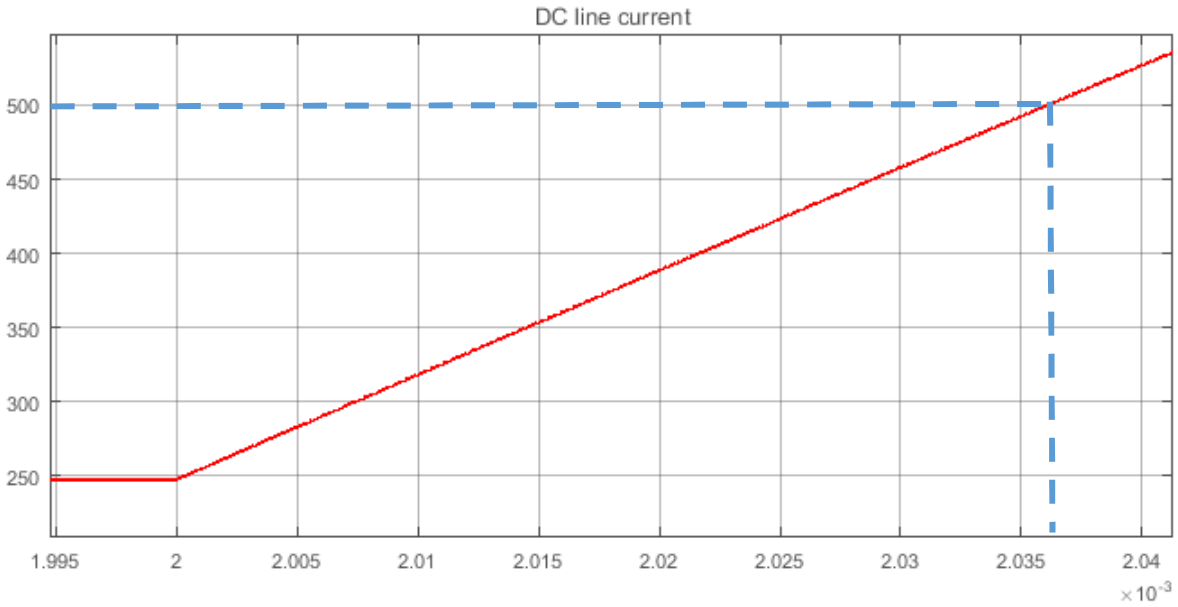

Figure B.3 Pre-fault simulation inverter model during best case scenario

Threshold time period is found to be 36.02 µs.

Worst Case Scenario

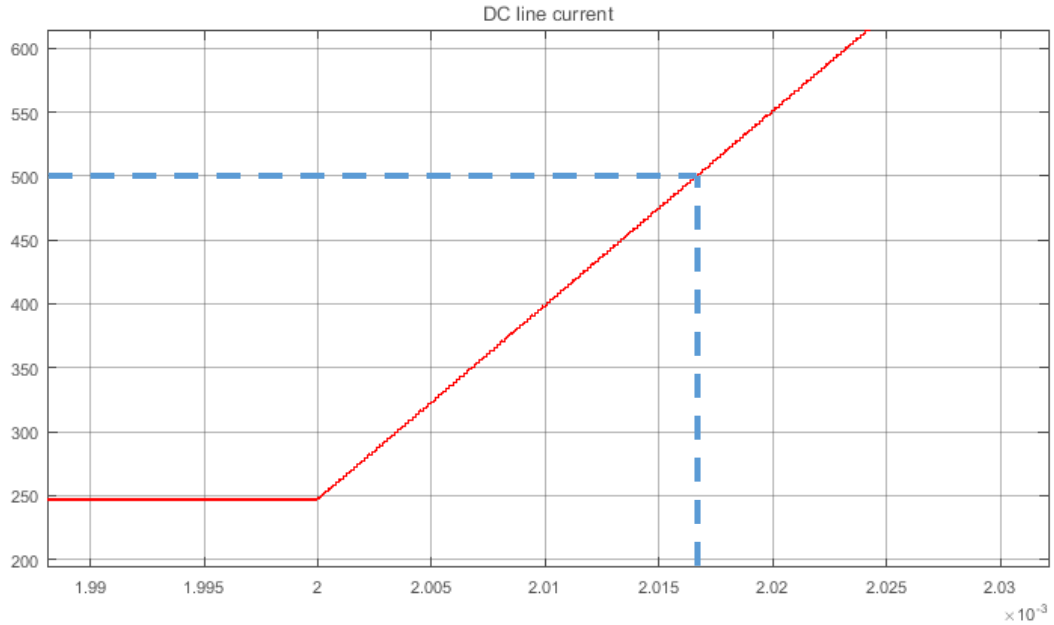

Figure B.4 Pre-fault simulation inverter model during worst case scenario

Threshold time period is found to be 16.64 µs.

Battery System Model

Best Case Scenario

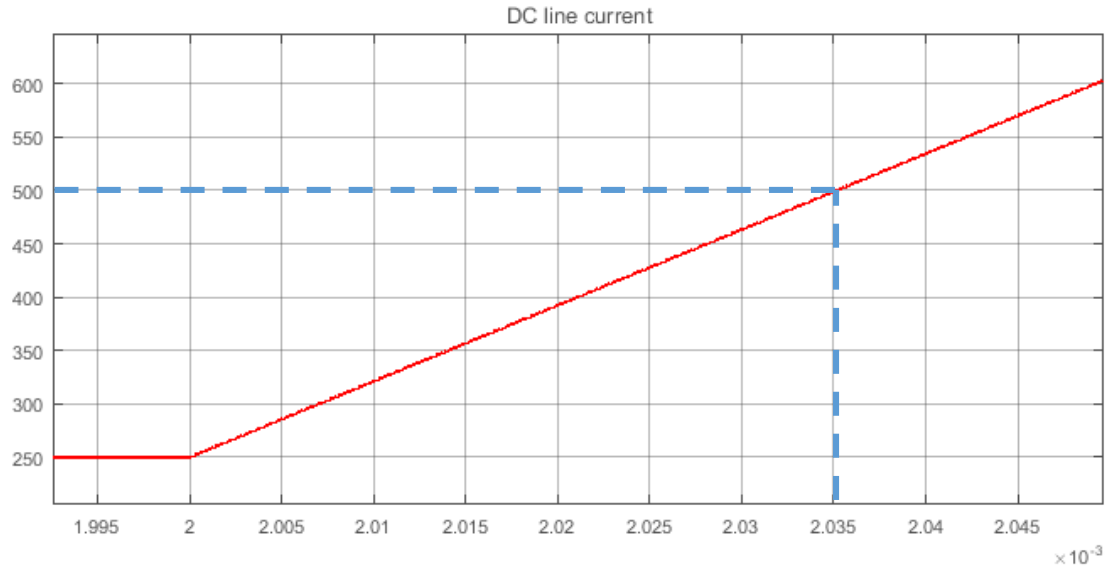

Figure B.5 Pre-fault simulation battery model during best case scenario

Threshold time period is found to be 35.40 µs.

Worst Case Scenario

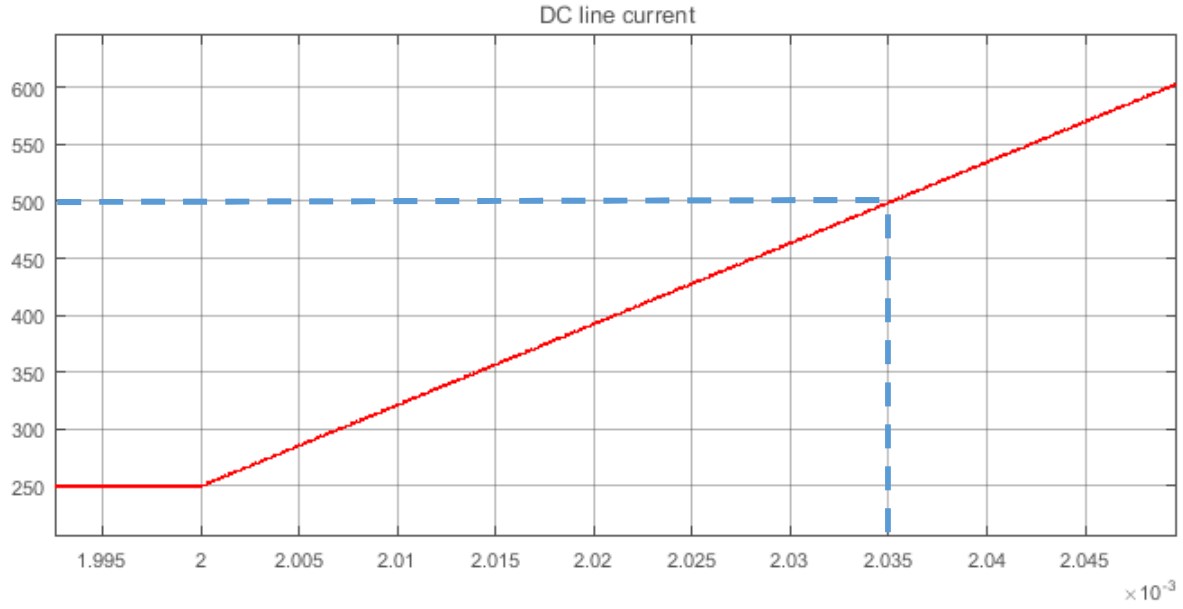

Figure B.6 Pre-fault simulation battery model during worst case scenario

Threshold time period is found to be 16.49 µs.

Appendix C: Proposed LVDC Microgrid Model for Future Work

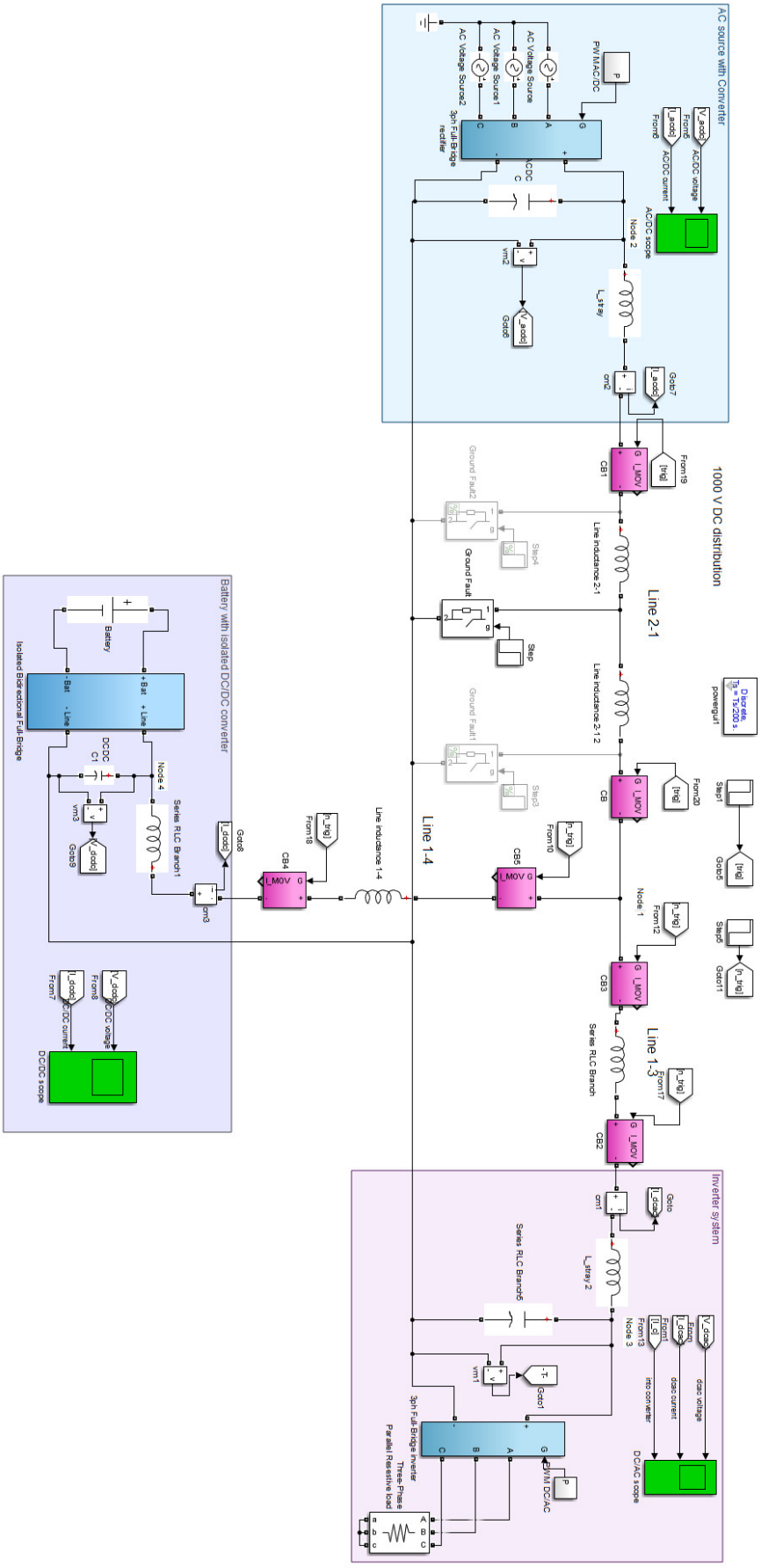

Figure C.1 Proposed LVDC microgrid model