Experimental Performance Evaluation of Two Commercially Available, 1.2 kV Half-Bridge SiC MOSFET Modules

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***Abstract*—In this paper, the switching performances of two state-of-the-art half-bridge SiC MOSFET modules are evaluated using a standard double pulse test methodology. The selected modules are commercially available, and have the same voltage and current ratings. A comparative study is carried out under various conditions such as similar dv/dt, di/dt, and current and voltage overshoots. Additionally, the lab setup is simulated in LTspice in order to investigate the impact of stray inductances in the switching performances. Both the simulations and the experimental measurements give insight in the significance of low inductive layouts to utilize the fast switching feature of SiC.**

I. Introduction

SiC devices offer several advantages such as bandgap energy and thermal conductivity of about three times higher than Si devices. The former results in a small concentration of intrinsic carriers, allowing the semiconductor devices to operate at higher junction temperature. The latter translates into reduced thermal resistance, improved heat dissipation and thereby increased power density. One of the most important features of SiC is a breakdown electric field of ten times higher than that of Si devices. This allows the use of thinner and shorter drift layer, reducing the capacitances and on-resistances. Besides, devices can be designed for higher voltage. Furthermore, the higher saturation electron drift velocity in SiC compared to Si enables higher switching speed. There are many publications explaining the aforementioned advantages of SiC devices [1], [2]. Moreover, several others have compared the switching performances of SiC devices and their Si counterparts. For example, a SiC MOSFET is compared with a Si IGBT in [3] and a SiC IGBT in [4].

However, few publications have compared SiC MOSFET modules against each other. Therefore, in this paper, two commercially available SiC MOSFET modules, from two different manufacturers, are evaluated by observing their switching performances. The selected SiC modules are CAS120M12BM2 from Cree and BSM120D12P2C005 from Rohm. Each of them have a voltage rating of 1.2 kV and a current rating of 120 A, while they have different stray inductances inside the module (L_{module}).

The paper is organized as follows. After the description of the methodology, a summary of the experimental measurements are presented. The gate resistance (R_g) is varied in order to see the impact on overshoots, ringing, slew rates, and switching energy losses. Thereafter, an LTspice simulation is presented in order to study the influence of stray inductances in the switching performances. The simulation shows that the switching speed in SiC devices are slowed down and the waveforms are more oscillating with higher values of stray inductances. Then, the comparison between the two selected SiC modules are exemplified through switching waveforms so that the differences between them can be understood easily. This comparison helps to choose an optimum value of R_g during turn-on and turn-off independently. For instance, the turn-off R_g can be selected as a trade-off between voltage overshoot (V_{os}) and turn-off energy loss. Similarly, the turn-on R_g can be selected as a compromise between current overshoot (I_{os}) and turn-on energy loss. Most importantly, the comparison between these modules illuminates the importance of having low inductive modules in order to reduce the stresses such as overshoots and switching energy losses.

II. Methodology and laboratory setup

A standard double pulse test methodology is used for evaluating the stresses such as current and voltage overshoots, ringing, dv/dt, di/dt, and switching energy losses in the device under test (DUT), as described in [5], [6]. An equivalent circuit with a clamped inductive load or with a hard switched arrangement is shown in Fig. 1. The total stray inductance in a switching loop (L_{stray}) is the sum of L_{dcbus}, L_{byp}, and L_{module} which are depicted in Fig. 1. L_{module} is the effective stray inductance which is distributed inside the module, represented by red coils.

The dc-link is realized with a planar busbar except the termination parts (needed to facilitate the module connection) so that the stray inductance in the switching loop can be kept as low as possible. A current viewing resistor (CVR) SSDN-414-01 (400 MHz, 10 $m\Omega$) from T&M research is used for measuring the drain current. The CVR replaces one of the screws in the SiC module as it is mounted directly on the screw terminal. This arrangement decreases the L_{stray} even further as one screw hole is eliminated in the busbar. L_{byp} and L_{dcbus} are calculated using Ansys Q3D extractor, and is 14 nH in total [7]. The picture illustrating the placement of the CVR in the laboratory setup is shown in Fig. 2. A detailed sketch

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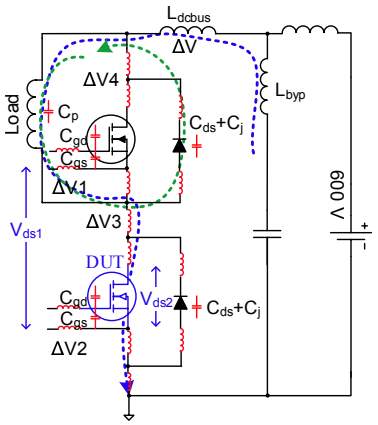


Fig. 1. Current paths show turn-on and turn-off processes in a buck converter during the double pulse test of lower MOSFET. V_{gs} of -5 V is applied in the upper side MOSFET to ensure that it is turned off all the time.

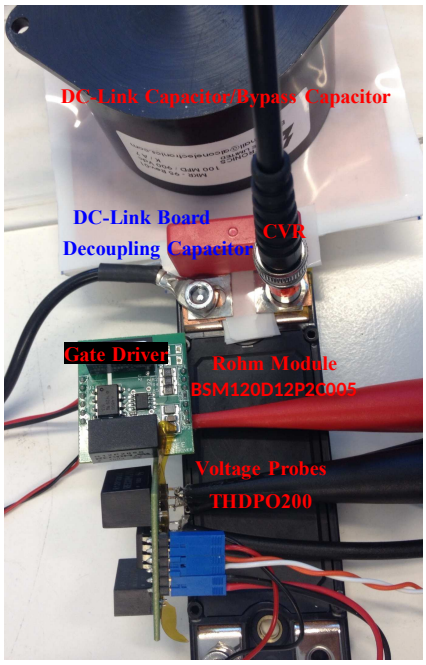


Fig. 2. Hardware setup showing a planar busbar, placement of CVR instead of a screw, several parallel capacitors in the dc-link to reduce L_{byp}, and to realize an overall low L_{stray} in the switching loop. V_{ds} of the lower side MOSFET in the half-bridge is measured across the sources of the upper and the lower MOSFETs.

for insertion of CVR between the busbar and the module is depicted in Fig. 3.

An inductive load with a single layer winding is used in order to ensure minimum stray capacitance [8]. High voltage differential probes (THDPO200, 200 MHz) are used for drain voltage (V_{ds}) and gate voltage (V_{gs}) measurements. SiC MOSFET has modest transconductance, therefore it demands V_{gs} of 20 V for acquiring optimum performance. It has a typical threshold voltage of 2.5 V but it is fully turned-on only after V_{gs} reaches 16 V. In this work, an isolated gate driver with an adjustable output voltage [9] is used for driving the SiC

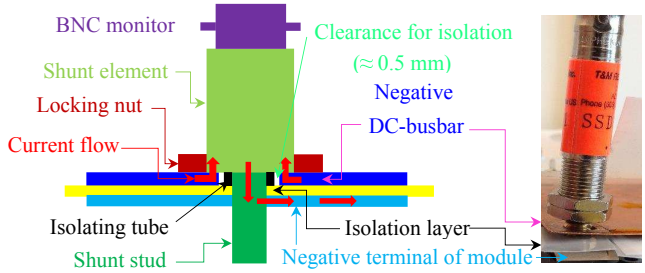
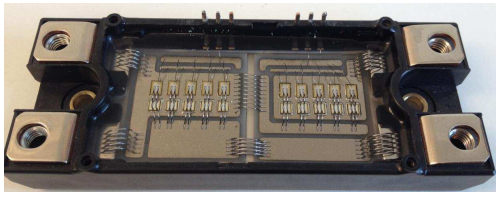


Fig. 3. Detail sketch of CVR insertion between the busbar and the module. A clearance of 0.5 mm is provided for shunt voltage drop on the DC-busbar.

(a) Internal layout of CAS120M12BM2 (Cree).



(b) Internal layout of BSM120D12P2C005 (Rohm).

Fig. 4. Picture showing the number of chips and the internal layouts.

TABLE I
NUMBER OF CHIPS, C_{iss} AND C_{oss} OF THE HALF-BRIDGE MODULES USED IN THE MEASUREMENT

Parts Half-bridge	Chips (N x $m\Omega$)	C_{iss} (nF)	C_{oss} (nF)
CAS120M12BM2 (Cree)	6x80	6.3	0.88
BSM120D12P2C005 (Rohm)	5x80	14	0.9

MOSFETs where the gate voltage is set to 20 V for turn-on and -5 V for turn-off.

Both the modules have been opened to see the internal layout and the distribution of the chips. The Cree module has 6 co-pack MOSFETs in each of the upper and the lower sides in the half-bridge configuration. A co-pack MOSFET is a MOSFET with an anti-parallel Schottky diode. In the Rohm module, there are 5 co-pack MOSFETs in each of the upper and lower side switches. The opened modules are shown in Fig. 4. The input capacitances (C_{iss}) and the output capacitances (C_{oss}) of the modules are listed in Table I [10], [11].

III. SUMMARY OF MEASUREMENTS WITH VARYING GATE RESISTANCES

All the turn-on and turn-off switching transients are evaluated for a dc-link voltage of 600 V and a drain-source current of 120 A in each of the SiC MOSFET modules at 25 °C.

TABLE II
SUMMARY OF LABORATORY MEASUREMENTS FOR CAS120M12BM2 (CREE)

R_g (Ω)	dv/dt (V/ns)	di/dt (A/ns)	V_{os} (V)	I_{os} (A)	E_{on} (mJ)	E_{off} (mJ)	di/dt_1 (A/ns)
0	34.2	9.8	215	134	0.52	0.53	1.64
1.95	26.3	7.3	185	101	0.76	1.17	1.22
3.9	19.7	5.9	156	79	1.46	1.62	0.99
6	14.8	5.8	139	67	2.08	1.67	0.98
10	10.4	3.5	106	45	3.10	2.52	0.58
12	9.4	3.1	90	43	3.83	2.90	0.51

TABLE III
SUMMARY OF LABORATORY MEASUREMENTS FOR BSM120D12P2C005 (ROHM)

R_g (Ω)	dv/dt (V/ns)	di/dt (A/ns)	V_{os} (V)	I_{os} (A)	E_{on} (mJ)	E_{off} (mJ)	di/dt_1 (A/ns)
0	35.2	7.01	295	87	0.4	1.04	1.39
1.95	23.4	3.57	264	49	2.0	1.52	0.71
3.9	17.5	2.34	212	36	3.7	1.8	0.46
6	14.26	1.92	183	31	5.0	2.17	0.38
10	10.4	1.32	147	23	7.4	3.2	0.26
12	9.4	1.15	135	21	8.6	3.6	0.23

Both the chosen SiC modules are evaluated with varying R_g. dv/dt and di/dt are measured at 50 % of the drain voltage and current as described in [3].

The summary of the measurements taken during the experiments are listed in Table II and Table III. dv/dt is the voltage slew rate during turn-off, di/dt is the current slew rate per module, while di/dt_1 is the current slew rate per chip during the turn-on of the lower MOSFET. The details are explained along with the example waveforms in Section V.

IV. ANALYSIS OF IMPACT OF STRAY INDUCTANCES BY SIMULATION IN LTSPICE

A simulation study is performed in a hard switching configuration as shown in Fig. 5 for the Rohm MOSFET module. The focus of the simulation is to study the impact of L_{stray} and stray inductance in gate side (L_g, as indicated in Fig. 5) in the switching transients.

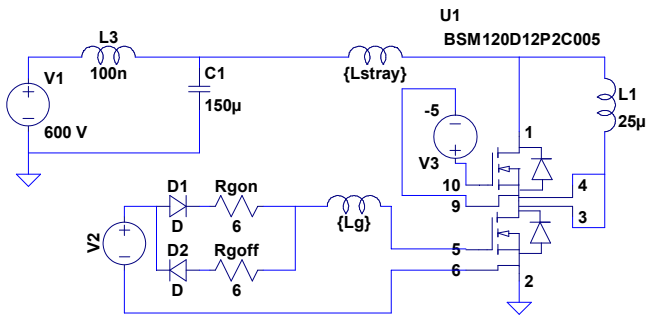
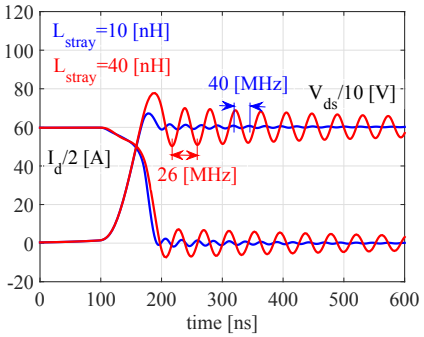


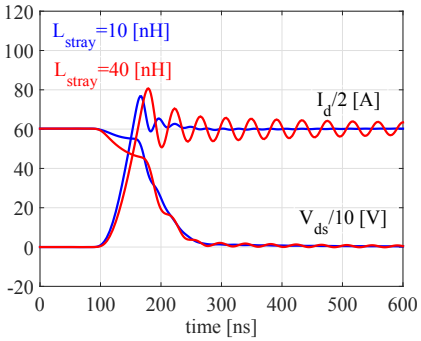
Fig. 5. Simulation model in LTspice for the study of impact of stray inductances.

A. Impact of L_{stray}

The simulated turn-off and turn-on switching transients for two different values of L_{stray} are shown in Fig. 6. With an



(a) Turn-off of BSM120D12P2C005 (Rohm). R_g = 6 Ω.



(b) Turn-on of BSM120D12P2C005 (Rohm). R_g = 6 Ω.

Fig. 6. LTspice simulation of switching transients with different L_{stray}.

L_{stray} of 10 nH, the frequency of oscillation is 40 MHz, while it is 26 MHz with an L_{stray} of 40 nH. V_{os} and I_{os} are higher and oscillations are larger and longer with higher L_{stray}. There are noticeable decrements in current slew rates both during turn-on and turn-off transients with larger L_{stray}, thereby slowing the SiC transistors.

B. Impact of L_g

Fig. 7 illustrates the switching transients with an L_{stray} of 40 nH for two different values of L_g. The impact of L_g on the oscillations and slew rates is not as significant as that with L_{stray}. Nonetheless, it slows down the device a little.

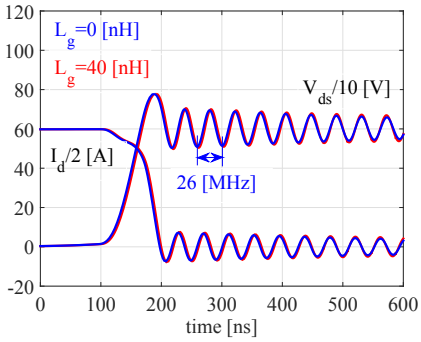
V. COMPARISON OF SIC MODULES

A. Similar dv/dt

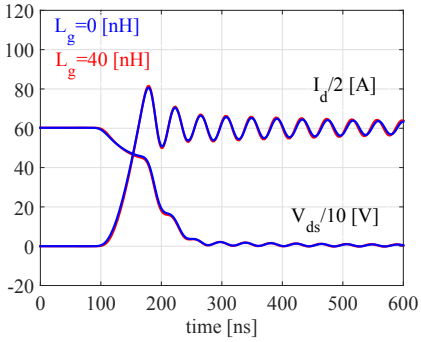
It is observed from the laboratory measurements that the variations in dv/dt with varying R_g are approximately in the same range for both modules as shown in Table II and Table III. An example of the turn-off switching transients are illustrated in Fig. 8.

It is clear from Fig. 8 that for the same R_g, the turn-off delay is longer for the Rohm device compared to the Cree. This is because of the fact that the Rohm module has a higher C_{iss} than the Cree module. The V_{os} during the turn-off is caused by switching loop inductance and di/dt at turn-off. L_{stray} can be estimated by, $V_{os} = L_{stray} \cdot di/dt$.

L_{stray} for the Cree module is 139/5.96 = 23.32 nH. Using the relation, $L_{stray} = L_{dcbus} + L_{byp} + L_{module}$, L_{module} can

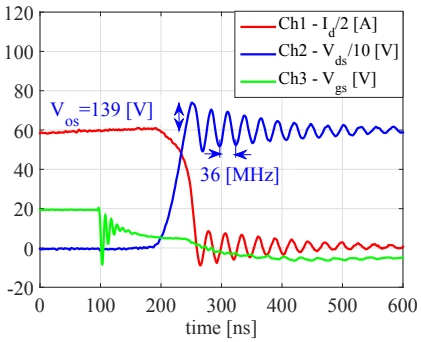


(a) Turn-off of BSM120D12P2C005 (Rohm). R_g = 6 Ω, L_{stray} = 40 nH, L_g = 10 nH and 40 nH.

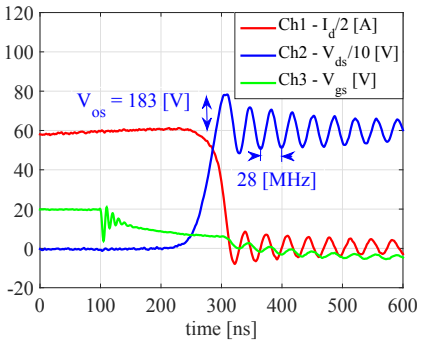


(b) Turn-on of BSM120D12P2C005 (Rohm). R_g = 6 Ω, L_{stray} = 40 nH, L_g = 10 nH and 40 nH.

Fig. 7. LTspice simulation with two L_g values; 0 nH and 40 nH.



(a) Turn-off of CAS120M12BM2 (Cree). R_g = 6 Ω, V_{os} = 139 V, dv/dt = 14.8 V/ns, E_{off} = 1.67 mJ.



(b) Turn-off of BSM120D12P2C005 (Rohm). R_g = 6 Ω, V_{os} = 183 V, dv/dt = 14.26 V/ns, E_{off} = 2.17 mJ.

Fig. 8. Illustration of switching transients for two modules at similar dv/dt.

be estimated to be 9.32 nH. The estimated L_{module} is lower than the datasheet value (15 nH). The drain voltage of the lower MOSFET is measured across the sources of the upper and lower MOSFETs indicated by V_{ds1} in Fig. 1. However, if the measurement had been done at the MOSFET chip level indicated by V_{ds2} in Fig. 1, the calculated and datasheet values would have corresponded better to each other.

Similarly, L_{stray} for the Rohm module is estimated to be 183/4.76 = 38.44 nH. L_{module} = 38.44 - 14 = 24.44 nH. The module manufacturer has measured it to be 25 nH. Since the estimated and the measured values correspond quite well, it indicates that the source pins of the upper and the lower MOSFETs in the Rohm module are very close to the chip. This can also be noticed from the layout in Fig. 4 b).

The frequency of oscillation in the Cree module is 36 MHz, while it is 28 MHz in the the Rohm module. The lower frequency of oscillation in the Rohm module is mainly because of higher stray inductance inside the module.

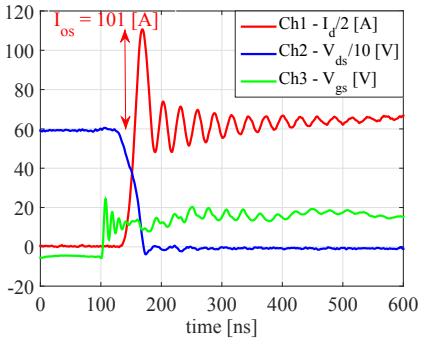
B. Similar di/dt per module

The example waveforms with similar di/dt per module for Cree and Rohm SiC MOSFETs are depicted in Fig. 9. The Cree module has 6 chips in parallel whereas the Rohm has only 5. C_{oss} is almost equal for both, which is shown in Table I. The larger I_{os} in the Cree module indicates that the effective junction capacitance of the MOSFETs and antiparallel diodes is higher compared to the Rohm module. An experiment was carried out to see the influence of varying junction capacitances in the turn-on switching waveforms in [6]. The higher the junction capacitance, the higher was the I_{os}, resulting in higher turn-on losses. This fact supports the aforementioned reasons of having higher overshoots in the Cree module compared to the Rohm. Therefore, a good way to reduce the I_{os} is by populating the chips with lower capacitances inside the module. The larger and longer amplitude of oscillations in the Rohm module imply a higher L_{stray} inside the module as calculated in Subsection A.

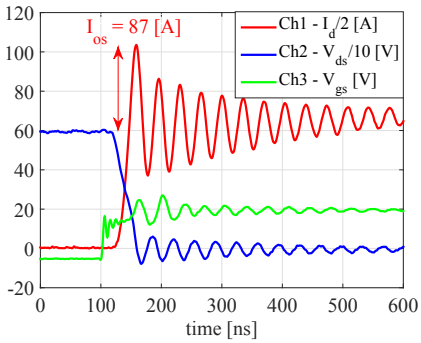
Nonetheless, the stray inductance effectively works as a turn-on snubber, which is also the reason for the lower di/dt for the same R_g in the Rohm compared to the Cree, as shown in Table II and Table III. Moreover, the simulation presented in Section IV also conforms to this fact; higher is the L_{stray}, slower is the current slew rate.

C. Similar di/dt per chip

For making a fair comparison, the waveforms with similar di/dt per chip are chosen. di/dt_1 of 0.51 A/ns can be obtained with R_g of 12 Ω for Cree and di/dt_1 of 0.46 A/ns with R_g of 3.9 Ω for Rohm, as shown in summary Table II and Table III. The waveforms for this case are shown in Fig. 10. A closer look on the oscillations of the drain currents reveals that the

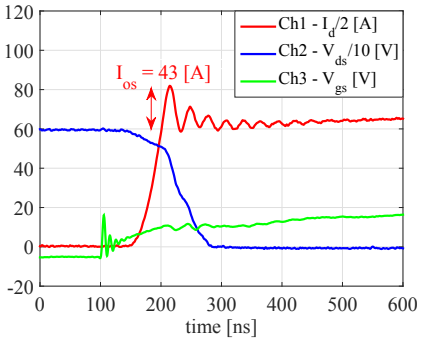


(a) Turn-on of CAS120M12BM2 (Cree). R_g = 1.95 Ω, I_{os} = 101 A, di/dt = 7.3 A/ns, E_{on} = 0.76 mJ.

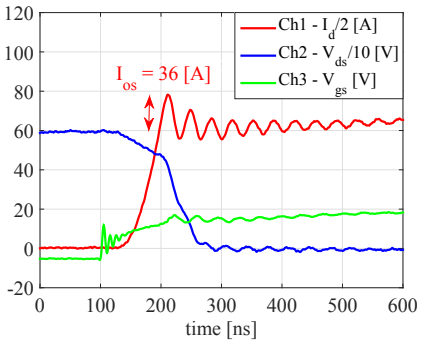


(b) Turn-on of BSM120D12P2C005 (Rohm). R_g = 0 Ω, I_{os} = 87 A, di/dt = 7.01 A/ns, E_{on} = 0.4 mJ.

Fig. 9. Illustration of switching transients for two modules at similar di/dt.



(a) Turn-on of CAS120M12BM2 (Cree). R_g = 12 Ω, I_{os} = 43 A, di/dt = 6 x 0.51 A/ns, E_{on} = 3.83 mJ.



(b) Turn-on BSM120D12P2C005 (Rohm). R_g = 3.9 Ω, I_{os} = 36 A, di/dt = 5 x 0.46 A/ns, E_{on} = 3.7 mJ.

Fig. 10. Illustration of switching transients at similar di/dt per chip.

Rohm module has a larger L_{stray} in the power loop than the Cree module.

D. Similar voltage overshoot

For comparing the case with similar V_{os}, the case with closest values are chosen from the summary Table II and Table III. The waveforms are displayed in Fig. 11. The faster rising waveforms of the Cree module compared to the Rohm clearly indicates that the turn-off losses are higher in the Rohm module for this case. From laboratory measurements, the turn-off loss for Cree is 1.17 mJ and for Rohm it is 2.17 mJ. Thus, it is desirable to have a module with lower stray inductance, otherwise it suffers from higher switching loss.

E. Similar current overshoot

R_g of 10 Ω for Cree and 3.9 Ω for Rohm modules give almost similar I_{os}. The waveforms are examplified in Fig. 12. Laboratory measurements show turn-on losses of 3.1 mJ for Cree and 2.0 mJ for Rohm.

VI. Discussion

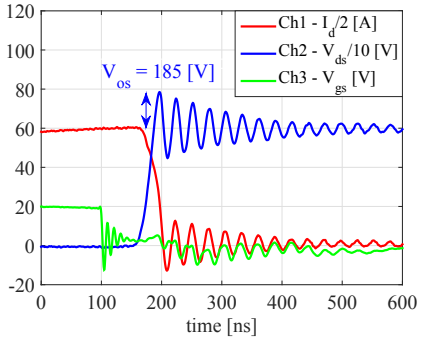
Two SiC modules with different L_{module} are compared from various perspectives. The gate resistances during the turn-on and turn-off can be selected independently, considering trade-offs between overshoots and switching losses. In any application, the V_{os} should be within some safe margin of breakdown limits, however, the I_{os} should cause no problems for the device, as long as the turn-on losses are acceptable.

The measurements show that the selected SiC modules can switch with dv/dt of about 35 V/ns with R_g of 0 Ω. When the devices switch fast, the parasitics in the circuit, i.e., stray inductances, and stray capacitances become troublesome. Therefore, the gate driver should not only switch fast, but also should be capable to handle the dv/dt and di/dt related noises. The conductive and radiative noises could cause unwanted turn-on and turn-off of the device, and eventually failure.

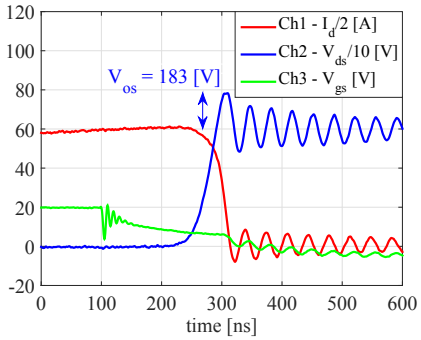
Packaging the fast switching SiC devices in a conventional plastic package and layout like in Si devices is definitely not a good solution. The companies like Vincotech and Danfoss work on low inductive packaging of SiC MOSFETs using the Cree and Rohm SiC chips, but with non-standard packages, which demands a full new design for each different case.

The layout of the circuit external to the module is important. For example, the coplanar part in the screw termination of the modules is a significant contributor to stray inductance in the switching loop. Moreover, the terminations in the dc-link capacitor also form a coplanar structure and is therefore a major contributor to the loop inductance as well [7].

Even though the physics of SiC allows switching frequencies in the range of ten's of MHz, today's limitation is given by the packaging technology and the limitations of surrounding components. Thus, SiC devices must be considered not as a

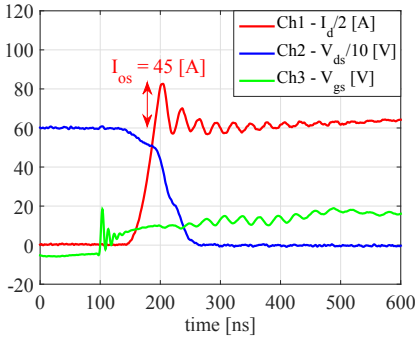


(a) Turn-off of CAS120M12BM2 (Cree). R_g = 1.95 Ω, V_{os} = 185 V, dv/dt = 26.3 V/ns, E_{off} = 1.17 mJ.

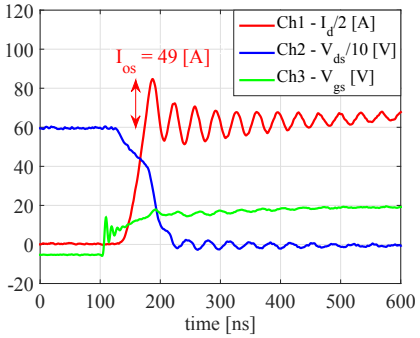


(b) Turn-off of BSM120D12P2C005 (Rohm). R_g = 6 Ω, V_{os} = 183 V, dv/dt = 14.26 V/ns, E_{off} = 2.17 mJ.

Fig. 11. Comparison of switching transients at similar V_{os}.



(a) Turn-on of CAS120M12BM2 (Cree). R_g = 10 Ω, I_{os} = 45 A, di/dt = 3.5 A/ns, E_{on} = 3.1 mJ.



(b) Turn-on BSM120D12P2C005 (Rohm). R_g = 1.95 Ω, I_{os} = 49 A, di/dt = 3.57 A/ns, E_{on} = 2.0 mJ.

Fig. 12. Comparison of switching transients at similar I_{os}.

single entity, but as a part of a system, where ancillary devices such as capacitors and magnetics need to be developed hand in hand.

VII. Conclusion

The experimental comparison between the two modules shows that the highest achievable speed is around 35 V/ns with today's SiC modules using standard plastic packages. L_{module} in the Rohm package is found to be around 25 nH and in the Cree it is about 15 nH. Both the simulation and the laboratory results illuminate that higher L_{stray} slows down SiC devices, stresses them with higher current and voltage overshoots, and higher losses. Therefore, it is crucial to reduce stray inductances both in the power and the gate loops to be able to utilize the fast switching potential of SiC.

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