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Optimal Frequency of Silicon Carbide Power Correction Circuits for On-Board Chargers

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Abstract

Compact high-efficiency power converters is a popular topic in electrical power engineering. So is also the case for electric and plug-in hybrid electric vehicle battery chargers. Increasing the switching frequency in the power converters will reduce the size of passive components, but this also results in lower efficiency. The progress being made in wide bandgap semiconductors introduce possibilities for lower loss, and thus improved efficiency at higher switching frequencies. Silicon carbide is such a semiconductor material, whose electrical and thermal capabilities trumps those of a classical silicon semiconductor.

To investigate whether utilizing a silicon carbide semiconductor in an on-board charger for electric and plug-in hybrid electric vehicles can provide lower switching loss, a silicon carbide (SiC) MOSFET is tested against a silicon (Si) MOSFET. The focus is on the hard switched application of the power supply's power factor corrector. A continuous-conduction mode DCDC boost converter is designed and used to perform the test. The converter is designed for an input voltage of 230V, output voltage of 350V and rated for 3500W. Emphasis has been made on parasitic elements and their effect on switching behavior.

Three different circuits was developed through the course of the thesis, with improvements in layout implemented for each step. Significant improvements was seen in gate drive circuitry and the overall converter from the first design to the second, and improvements in the gate circuitry was seen from the second design to the third. From this, it is concluded that for best performance, the gate driver circuit should be as compact as possible, with short conduction paths and close to the MOSFET gate pin. The return form the MOSFET source to the gate driver ground should be as large as possible, and directly underneath the gate signal path. SMD components with low parasitic inductance and capacitance should be used in the gate driver circuit.

The Si and SiC MOSFET show different switching behavior. The main difference is at turn-off, regarding delay and voltage rise waveform. At the same gate resistance and gate voltage, the turn-off delay time for the Si MOSFET is almost three times longer than the SiC MOSFET delay time. While the SiC MOSFET turn-off voltage showed a linear increase the entire rising period, the Si MOSFET voltage rise was more exponential.

Accurately determining losses in a MOSFET, and how well it is capable of operating, is a challenging exercise. Distortion caused by the probes while measuring, bandwidth limitations in the probes and oscilloscope, time delays in the probes and improper components and design can all contribute to erroneous results. Nevertheless, it was concluded that in this circuit, with these MOSFETs, the SiC MOSFET had a switching loss between 106 µJ and 138 µJ, which was between 0,7 and 0,75 times lower than the Si MOSFET switching loss. With the conduction loss for the MOSFETs taken into account, which was found to be 2,2 W for the SiC MOSFET and 7,5 W for the Si MOSFET, at nominal operation and a selected operating temperature of 125 ºC, the optimal switching frequency was found to be between 165 kHz and 215 kHz. This is based on a power loss cap of 25 W.

Preface

This Master's Thesis was prepared during the spring 2016 at the Norwegian University of Science and Technology (NTNU), Department of Electric Power Engineering. The topic of the thesis is power electronics, and is accomplished in cooperation with Valeo Powertrain Energy Conversion.

I would like to thank my supervisor, professor Ole-Morten Midtgård, for support and my co-supervisor doctoral candidate Ole Christian Spro for technical guidance through the work on this thesis. I would also like to thank Torbjørn Sørsdahl at Valeo for valuable support and constructive technical feedback. Acknowledgement also goes to the staff at the Department of Electric Power Engineering's Servicelab for technical assistance whenever needed, and to the Department of Electronics and Telecommunication's Elprolab (Electronics and Prototype Laboratory) for helpful and fast production of the printed circuit boards.

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Abbreviations

A	Ampere
AC	Alternating Current
C	Capacitance
C_{ds}	Drain-source capacitance
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{iss}	MOSFET input capacitance
C_{oss}	MOSFET output capacitance
C_{rss}	MOSFET reverse transfer capacitance (Miller capacitance)
CCM	Continuous Conduction Mode
CrM	Critical Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
E_{off}	Turn-on energy loss
E_{on}	Turn-off energy loss
E_{sw}	Total switching energy loss
ESR	Equivalent Series Resistance
EMI	Electromagnetic Interference
EV	Electric Vehicle
F	Farad
H	Henry
I	Current
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
OBC	On-Board Charger
PCB	Printed Circuit Board
PFC	Power Factor Correction

PHEV	Plug-in Hybrid Electric Vehicle
Q	Charge [Coulomb]
Q_g	Total gate charge
Q_{gd}	Gate-drain charge
Q_{gs}	Gate-source charge
SBD	Schottky Barrier Diode
Si	Silicon
SiC	Silicon Carbide
SMD	Surface Mount Device
SFR	Self-Resonant Frequency
t_{fc}	Current fall-time
t_{fv}	Voltage fall-time
t_{off}	Turn-off time
t_{on}	Turn-on time
t_{rc}	Current rise-time
t_{rv}	Voltage rise-time
V	Voltage
V_{ds}	MOSFET drain to source voltage
V_{gs}	MOSFET gate to source voltage
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1 Introduction

The master thesis is a continuation of the specialization project fall 2016. The topic is silicon carbide semiconductor for use in the on-board charger of electric and plug-in hybrid vehicles. The material properties of silicon carbide suggest faster switching and lower switching loss. Since the switching loss is proportional with the switching frequency, lower switching loss suggest the switching frequency can be increased, keeping the efficiency at an acceptable level. This is highly beneficial since a higher frequency equals smaller passive components in the circuit, which reduces the size and weight of the charger.

Electric and plug-in hybrid electric vehicles are becoming increasingly popular amongst new car buyers around the world. In Norway especially, thanks to the government incentives, sales have shot through the roof in recent years. The technology is improving rapidly, and the car manufacturers are continuously looking to increase the battery range and improve charging.

The On-Board Charger (OBC) is an essential part of the vehicle. Without it, the batteries could not be charged from your home. The AC voltage in the wall socket is converted into a regulated DC voltage that can charge the batteries in the car. The conversion is performed through power converters, and require semiconductor switches to work. These switches include loss. Apart from the voltage drop over the switch while it is conducting, high instantaneous power loss occur both then the switch turn on and off. This loss is proportional to the frequency of which the switch is operated.

Since the size of passive components is reduced, and power loss is increased, as the frequency is increased, designers must compromise between the total efficiency and the overall size of the OBC when setting the operating frequency. If the switching losses could be reduced, the frequency could be increased without compromising with efficiency. Thus, the size of the OBC could be reduced.

1.1 Scope of work

The thesis will focus on the difference between silicon and silicon carbide MOSFET in hard switch application, as the power factor corrector in the charger.

To execute this, a DCDC step-up converter will be constructed. Since a conventional PFC converter is a diode bridge rectifier followed by a boost converter, this will be sufficient to study the behavior of the MOSFETs. The ultimate goal is for the boost converter to deliver 3500W power at 350V with an efficiency of 98%. The peak-to-peak current ripple is set to be no more than 2A.

The thesis include a theoretical description of the boost converter and its modes of operation, justifying the choice of approach. The switching behavior of the MOSFET in this circuit, and considerations needed to be taken when designing it, will be explained. A theoretical presentation of silicon carbide as a semiconductor material and its applications is included, as well as a comparison between silicon and silicon carbide MOSFETs parameters and loss calculations based on these parameters. Finally, the boost converter will be tested with both silicon and silicon carbide MOSFETs, and compared.

2 On-Board Charger

An On-board Charger (OBC) is a power conversion hardware. Its purpose is to charge the vehicle batteries at the correct DC voltage when power is drawn from the AC mains. The input is converted through two stages. A power factor corrector (PFC) converts the AC input to DC while keeping the input voltage and current sinusoidal and in phase, while a DCDC converter provides the desired voltage to the battery. The PFC is a crucial part of the OBC. Without it, the harmonic distortion in the current would violate the utility grid restrictions and the converter would have to be designed for much higher peak currents. Additionally, the OBC includes, among other, controllers, soft starter, measurements and CAN (Controller Area Network) bus for communication with the vehicle. This will however not be discussed further in this thesis.

A conventional PFC consist of DCDC converter, usually a step-up converter, preceded by a diode bridge rectifier. The step-up converter is often the preferred choice in active current shaping because when the switch is off, the input directly feeds the output. Additionally, when the output voltage is higher than the peak of the input, the converter is more stable and can handle both over- and undervoltages at the input [1].

2.1 GEN2 Charger

Valeo PECs current charger, the GEN2 (generation 2), is a 3,5kW 350V output charger. Its power conversion is operated through a PFC at the input, and then through an LLC resonant converter, which outputs the desired voltage to the batteries. LLC stands for the two inductors, noted *L*, and one capacitor, noted *C*, which constitutes the resonant tank of this specific resonant converter.

The PFC in this charger is a bridgeless PFC. It utilizes two switches, one for each half cycle. This eliminates the need for a diode rectifier bridge at the input. This is beneficial in terms of efficiency, as it reduces the number of semiconductor devices in the conduction path from three to two.

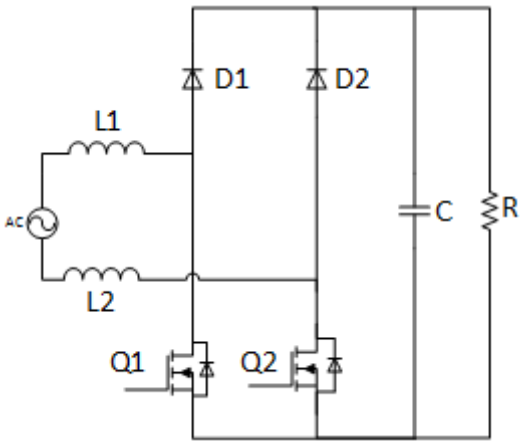


Figure 1: Bridgeless Boost PFC converter

Figure 1 shows a simple bridgeless PFC converter, patented in 1983. The switches alternate between operating as high frequency chopper and low frequency half-wave rectifier. When the sinusoidal input is on its positive half cycle, current flows from the input voltage through L1. When switch Q1 is off, current flow through D1 and to the output. When Q1 is on, current flows through it. The return path in both cases is through the antiparallel diode in Q2. When the switch is on its negative half cycle, current flow from the input through L2. When Q2 is off, the current flow through D2 to the output. When Q2 is on, the current flow through it. Here, the return path of the current is through the antiparallel diode in Q1.

After the PFC is a DCDC converter. The solution here is an LLC resonant converter, which serves two functions. The first is to provide the correct output voltage at all times for all load conditions. The second is to provide a galvanic isolation between the input and output. A simplified model of the LLC converter in the charger is shown in Figure 2

The LLC converter is a popular choice in power conversion because of its high efficiency, high power density and low electromagnetic interference (EMI). The switching bridge generates a square waveform to excite the resonant tank (Cr, Lr, Lm). The resonant tank outputs a sinusoidal current that is scaled by the transformer and rectified by the rectifier bridge. The output capacitor filters the rectified AC current and outputs a DC voltage [2].

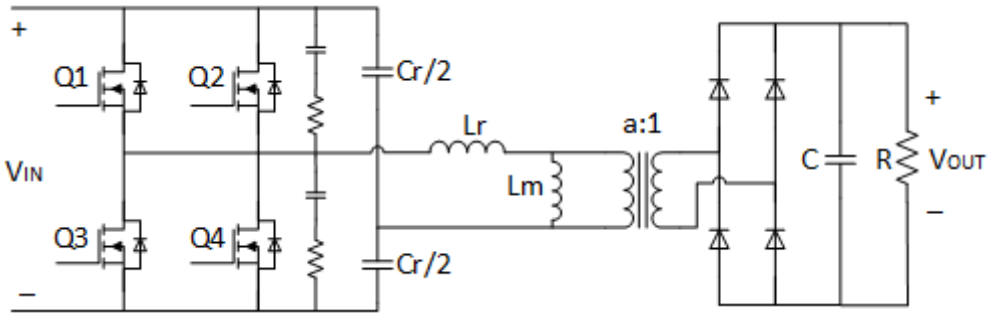


Figure 2: Half-bridge LLC resonant converter with split resonant capacitor

The specific topology used in this charger is a half-bridge resonant LLC with split resonant capacitor. This topology is especially useful at higher power levels as the current stress in each capacitor is reduced. It also makes the input current to the resonant tank look like that of a full-bridge converter. This reduces both the input differential mode noise and the stress on the input capacitor [3]. Additionally, this converter uses two parallel switches, which reduces the switching and conduction loss [4].

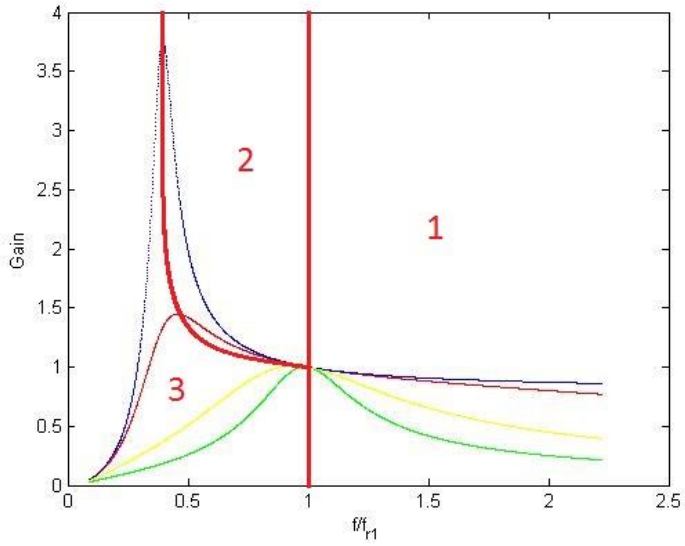


Figure 3: Frequency vs. output characteristics of an LLC resonant converter

Figure 3 show a typical gain characteristic for an LLC converter. The vertical axis show the input-to-output gain on the converter, and the horizontal axis show the normalized frequency. An LLC converter is normally designed to operate in area 1 and 2, shown in the figure. In these areas, the converter operates at zero voltage switching (ZVS), while in area 3, the converter

operates in zero current switching (ZCS). ZVS operation is usually preferred over ZCS as it shows higher efficiency and lower electromagnetic interference (EMI).

3 Boost Converter

There are several types of PFC topologies. However, the most known and used topology is the conventional PFC in Figure 4. This is a boost converter preceded by a diode bridge rectifier, creating a rectified sinusoidal input.

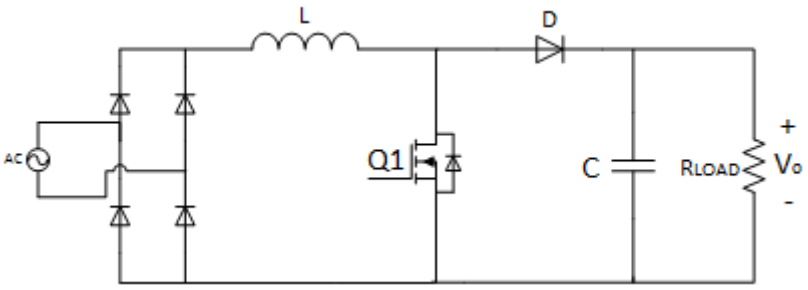


Figure 4: Conventional PFC topology

The boost converter in Figure 5, also known as a step-up converter, takes an input voltage and provide an output voltage higher than the input. How much higher the output will be compared to the input is determined by the switch duty cycle, which is defined as the on time divided by the length of the switching period. When the switch is turned on, the diode is reverse biased and the input supplies energy to the inductor. When the switch is turned off, the output receives energy from the input and the inductor. The converter has two distinct modes of operation: continuous- and discontinuous-conduction.

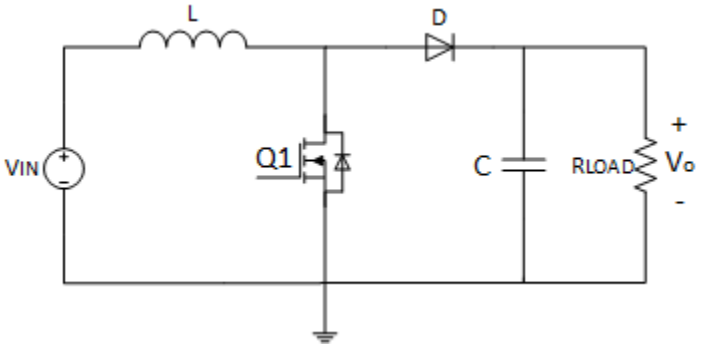


Figure 5: Simple boost converter

3.1 Continuous-conduction

In continuous-conduction mode (CCM), the current through the inductor never reaches zero in steady state. Recognizing that, in steady state, the voltage over the inductor over one switching period must be zero, then for the ideal converter the relationship between input and output voltage can be expressed as in Equation 1.

$$V_o = \frac{1}{1-d} V_{in} \tag{1}$$

Where *d* is the duty cycle, and is defined in Equation 2.

$$d = \frac{t_{on}}{T_s} \tag{2}$$

The ideal converter is also lossless in terms of energy, so the relationship between input and output current is found as in Equation 3.

$$I_o = (1-d) I_{in} \tag{3}$$

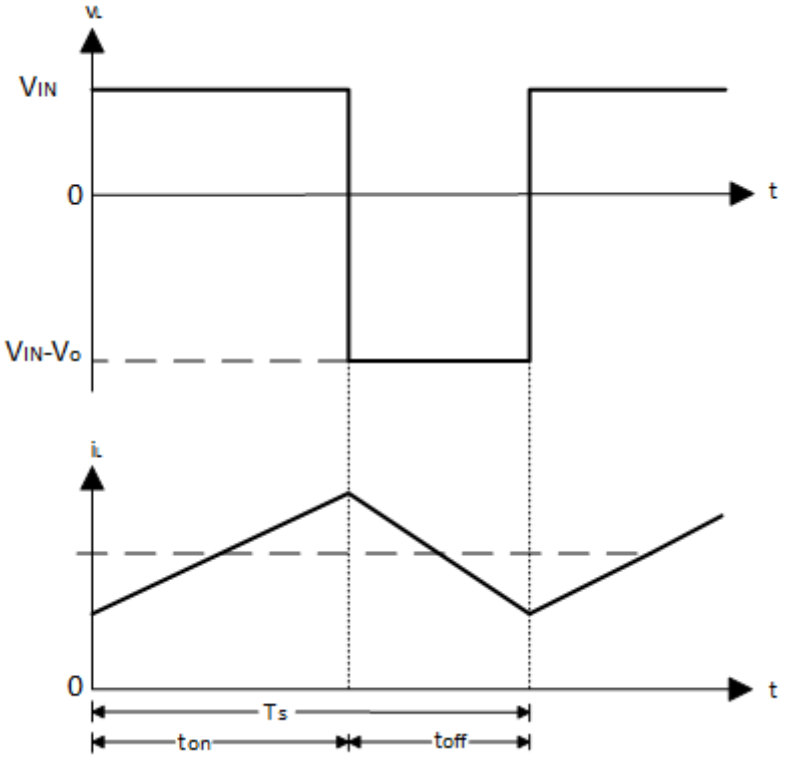


Figure 6: Boost converter inductor voltage and current waveforms in CCM

Figure 6 shows the steady state inductor waveforms for a CCM boost converter for one switching period. When the switch is on, the input voltage is applied over the inductor, and the current through the inductor rises. When the switch turn off, a negative voltage (Vin-Vo) is applied over the inductor, and the current decreases.

3.2 Border between continuous and discontinuous

This is defined as the operation mode when the inductor current just reaches zero at the end of the off interval. It is also known as critical conduction mode (CrM). Even though it is called CrM, the current does not go below zero, so this is a special case of continuous mode of operation. Figure 7 shows the steady state waveforms of the inductor voltage and current in CrM. The average inductor current in this mode can be found by Equation 4.

$$I_{LB} = \frac{V_{in}}{2L} t_{on} = \frac{V_{in} d}{2Lf_s} = \frac{V_o}{2Lf_s} d(1-d) \tag{4}$$

This equation can also be used to find the peak-to-peak current ripple, which is valid for continuous conduction as well. Since, at the border, the average current is half of the peak current, the current ripple can be expressed as Equation 5.

$$\Delta i_L = \frac{V_{in} d}{L f_s} \tag{5}$$

Since the inductor current is the same as the input current, the output current can be found using Equation 6

$$I_{oB} = \frac{V_o}{2 L f_s} d(1-d)^2 \tag{6}$$

If the load current drops below this, the inductor current drops below I_{LB}, and the converter will be in discontinuous-conduction mode.

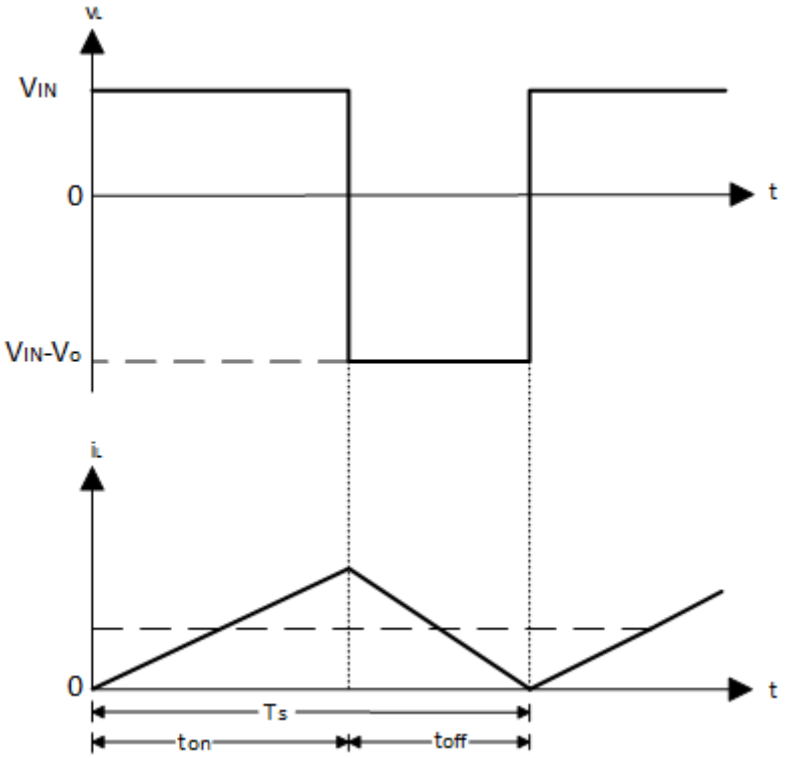


Figure 7: Boost converter inductor voltage and current waveforms in Cr

3.3 Discontinuous-conduction mode

In this mode, the inductor current drops to zero, and stays at zero for a portion of the switching interval. There are thus three stages in this mode.

- When the switch is on and the diode is reverse biased. The inductor current rises. (dT_s)
- When the switch is off and the diode is forward biased. The inductor current decreases. ($\Delta_1 T_s$)
- When the switch is off and the diode is reverse biased. The inductor current is zero. ($\Delta_2 T_s$)

Figure 8 shows the inductor voltage and current waveforms in a boost converter operating in discontinuous conduction mode (DCM).

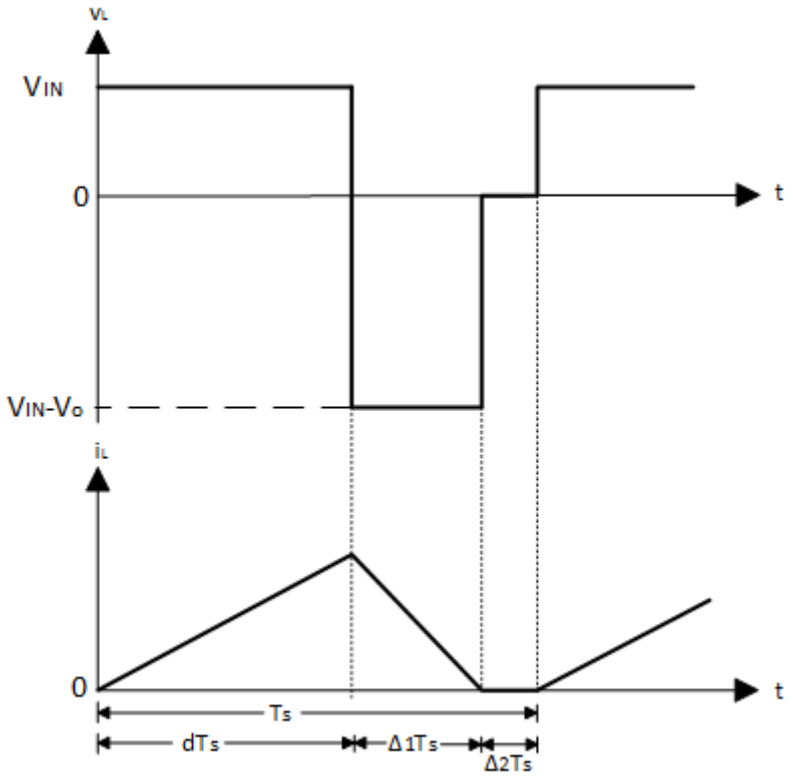


Figure 8: Boost converter inductor voltage and current waveforms in DCM

Equating the time integral of the inductor voltage over one period, the relationship between input and output voltage is expressed in Equation 7, and current in Equation 8.

$$V_o = \frac{\Delta_1 + d}{\Delta_1} V_{in} \tag{7}$$

And

$$I_o = \frac{\Delta_1}{\Delta_1 + d} I_{in} \tag{8}$$

The average input (or inductor) current is

$$I_{in} = \frac{V_d}{2Lf_s} d(d + \Delta_1) \tag{9}$$

Inserting Equation 8 in Equation 9 gives the average output current in Equation 10.

$$I_o = \frac{V_d d \Delta_1}{2Lf_s} \tag{10}$$

Looking at the above equations it is clear that a DCM converter will have a much smaller inductor than a CCM converter. This is beneficial for a compact converter. However, the ripple in the current is a concern. For a 3500W converter, the average inductor current will be 15,2A. A converter operating on the border of continuous and discontinuous would then have peak currents above 30A, and even higher for discontinuous-conduction. This will have a large impact on the peak ratings of the components and the size of the output filter. Because of this, a converter at this power level should be designed as a continuous-conduction converter.

Table 1 summarizes and compare the effects that the different operational modes of the boost converter have on the circuit. While CrM and DCM have the benefits of small inductor size and essentially no turn-on losses, they have the disadvantage of large peak currents that introduce high turn-off losses and problems with filtering these currents. Even though the CCM converter has high turn-on losses, which can be intensified by the reverse recovery loss of the boost diode, the advantages of lower peak currents, lower turn-off losses and lower high frequency ripple that must be filtered, makes it a preferred choice in high power applications [5].

Table 1: Comparison of the effects of operational mode of the boost converter.

Parameter	CCM	CrM	DCM
Current ripple	Lowest	High	Highest
Inductor size	Largest	Small	Smallest
EMI filter	Smallest	Large	Largest
Turn-on loss	Highest	Low (zero)	Low (zero)
Turn-off loss	Lowest	High	Highest

3.4 Converter Parameter setting

For proper and desired operation of the converter, the components must be properly dimensioned. The most important components are the boost inductor and the output capacitance. The main features of these are the current ripple in the converter and the output voltage ripple.

3.4.1 Output capacitance

The output capacitance is decided from the desired output voltage ripple. Assuming that the ripple component of the current through the diode flows through the capacitor and its average value flows through the load resistor, the voltage ripple can be calculated using the charge difference.

$$\Delta V_o = \frac{\Delta Q}{C} \tag{11}$$

This charge is then equal to the average output current multiplied with the on-time of the switch.

$$\Delta Q = I_o t_{on} = I_o D T_s \tag{12}$$

Inserting Equation 12 in Equation 11 and rearranging the terms, the capacitance can be found based on the desired output voltage ripple in Equation 13. This is valid for a constant output current.

$$C = \frac{I_o D T_s}{\Delta V_o} \tag{13}$$

In addition to the capacitance of the output capacitor, the equivalent series resistance (ESR) of the capacitor is an important factor to consider, which is explained in more detail in Chapter 3.6.

3.4.2 Boost inductor

The boost inductor is a crucial design step for the converter. The inductance for CCM boost converter is determined from the desired current ripple, and is calculated from Equation 5. Apart from the inductance, the inductor must be able to handle the currents without saturating the core, and its resistance should be as low as possible to minimize loss. The core material selection is also of great importance, as it must be able to operate properly at the selected frequency.

3.5 Boost Switching Basics

In order to design a good gate driver, one must understand what happens in the circuit at turn-on and turn-off of the switch. Figure 9 show a boost converter with a simplified gate driver.

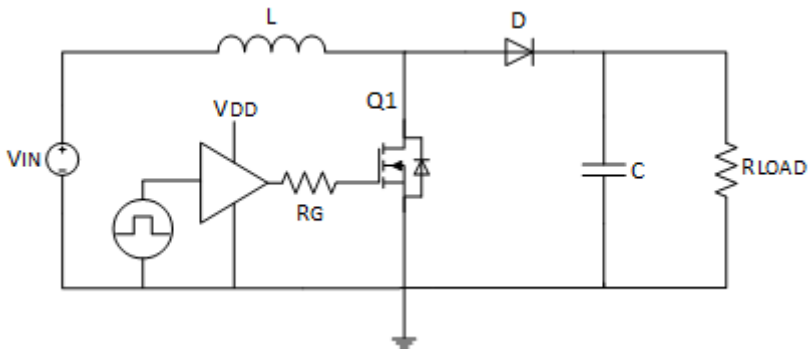


Figure 9: Boost converter with simplified gate driver

This circuitry is known as clamped inductive switching. Now the inductor L is assumed large enough to provide a constant current during the switching interval. When the MOSFET is turned on, the input voltage is applied over the inductor and the current ramps up to store energy. When the MOSFET turns off, the inductor current flows through diode D1, delivering energy to the output. The circuit waveforms at turn-on are illustrated in Figure 10 [6].

The turn-on of the MOSFET can be divided into four intervals. During the first interval, t1, the gate current charges the gate-to-source (Cgs) and gate-to-drain (Cgd) capacitances of the MOSFET to the gate threshold voltage Vth. Before these capacitances are charged to the threshold voltage, no current can flow through the MOSFET. This interval is therefore called the turn-on delay [6].

During the second interval, t2, the MOSFET start conducting current in the linear mode. Cgs and Cgd are charged to the plateau level as the drain current rises from zero to IL. The plateau level, known as the Miller plateau, is where the gate-source voltage remain constant for short time during the switching period. The drain-source voltage during this time interval is clamped at output voltage. The charge needed is Qgs, and the length of the time interval can be calculated as t2=Qgs/Ig [6].

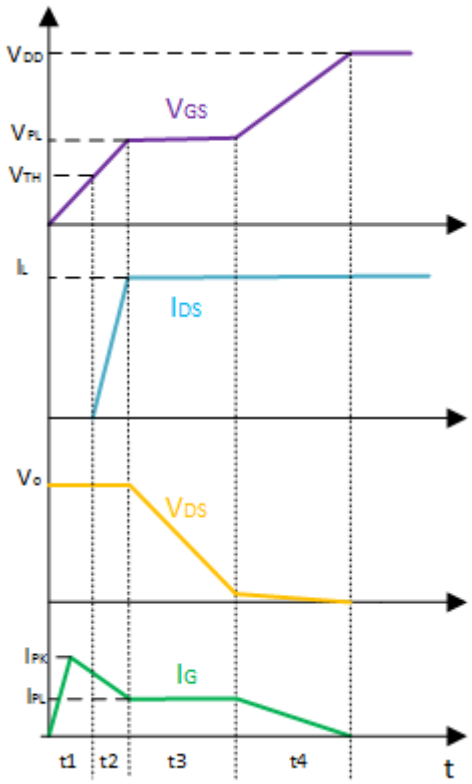


Figure 10: Waveforms at turn-on in a boost converter

The third time interval starts as the MOSFET conducts the entire inductor current. As t3 starts, the gate current flow through Cgd and the MOSFET channel. The gate current discharges Cgd as the gate-source voltage remain at the Miller plateau, and the drain-source voltage fall. This interval last until the drain-source voltage reaches zero (or near zero), and is given by t3=Qgd/Ig [6].

In interval four, the gate-source voltage rises from the plateau level to Vdd (or full driver voltage). Ig flow through a combination of Cgs, Cgd and the decreasing channel resistance. The current paths during turn-on of a MOSFET are shown in Figure 11 [6].

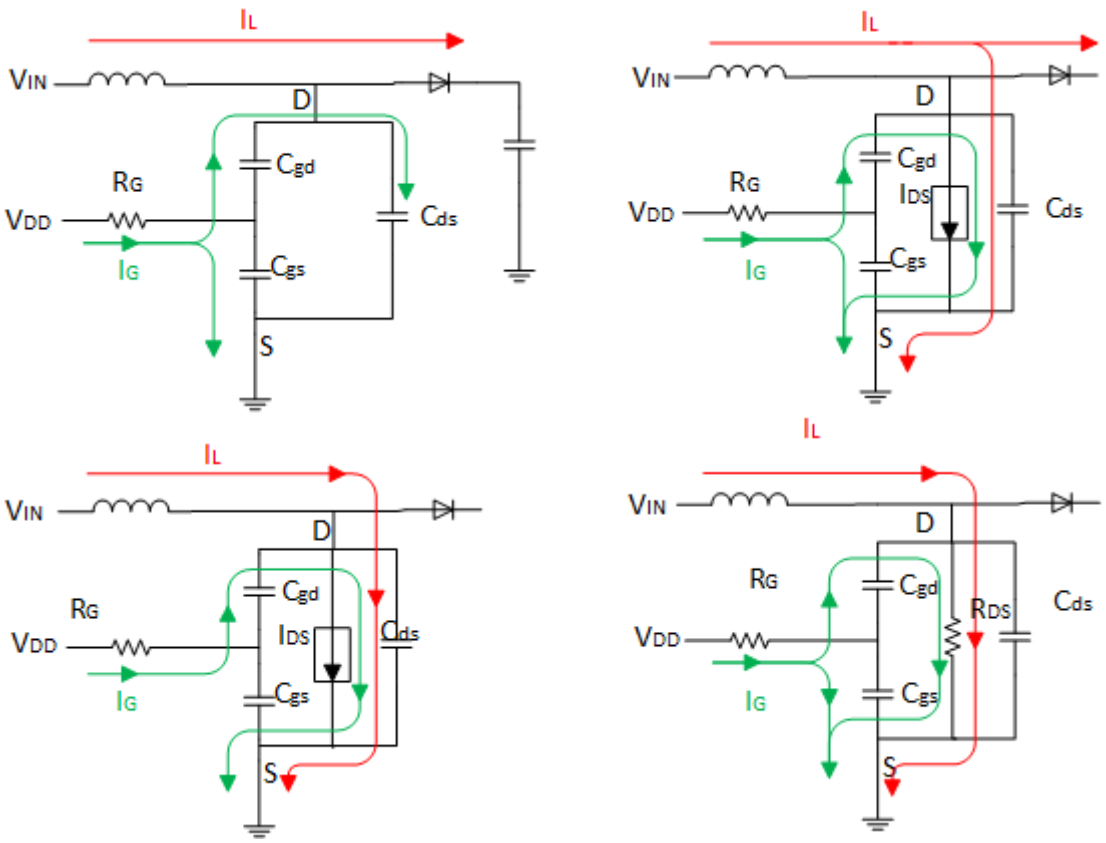


Figure 11: Current paths during the four time intervals at MOSFET turn-on. Top left: t1; top right: t2; bottom left: t3; bottom right: t4.

The switching loss during turn-on is related to time interval t2 and t3. During turn-off, the waveforms and current paths are much like the ones for turn-on, but in reverse order, as shown in Figure 12.

During interval t5, the gate current rises to discharge the gate-source voltage from Vdd to the plateau level. Vgs remain at this level during t6, while the drain-source voltage rises to the off-state voltage. The length of this time interval is found as t6=Qgd/Ig.

In t7, the drain current fall from IL to zero while the gate-source voltage falls to the threshold voltage. This time interval is calculated as t7=Qgs/Ig. During t8, the gate-source voltage is discharged to zero[6].

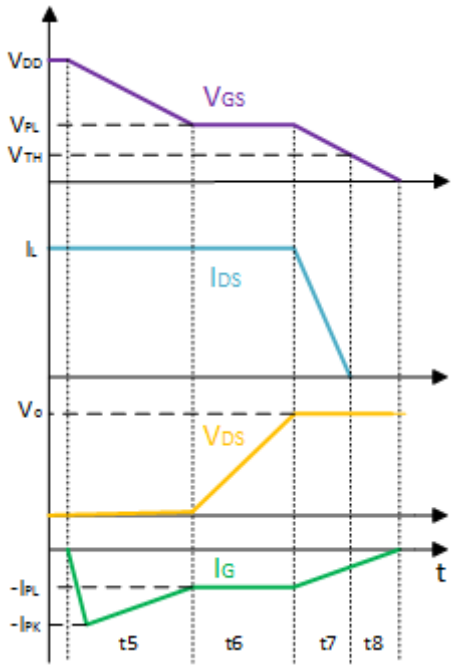


Figure 12: waveforms at turn-off in a boost converter

Turn-on or turn-off of a MOSFET can thus be divided into four time intervals. The length of these intervals is dependent on the parasitic capacitance, required voltage change across them and the available gate drive current. A thorough and careful selection of components is therefore important for a high efficiency and high frequency converter [6].

The switching loss during turn-on and turn-off can be estimated as in Equation 14 and 15 respectively [6].

$$P_{SW,ON} = \frac{V_D \cdot I_D}{2} \cdot f_s \cdot (t_2 + t_3) \tag{14}$$

$$P_{SW,OFF} = \frac{V_D \cdot I_D}{2} \cdot f_s \cdot (t_6 + t_7) \tag{15}$$

Taking into account the formulas previously stated for t2, t3, t6 and t7, the switching loss can be expressed by Equation 16 and 17.

$$P_{SW,ON} = \frac{V_D \cdot I_D}{2} \cdot f_s \cdot \left(\frac{Q_{GS}}{I_{G,t2}} + \frac{Q_{GD}}{I_{G,t3}} \right) \tag{16}$$

$$P_{SW,OFF} = \frac{V_D \cdot I_D}{2} \cdot f_s \cdot \left(\frac{Q_{GD}}{I_{G,t6}} + \frac{Q_{GS}}{I_{G,t7}} \right) \tag{17}$$

From these equations, the switching loss is dependent on the charge needed by the MOSFET and the current provided by the gate driver. Lower gate charge and higher gate current results in lower switching loss.

Using the equations for switching loss, the factor SiC switching frequency over Si switching frequency can be found, considering equal switching loss for the two MOSFETs.

$$\frac{f_{s,SiC}}{f_{s,Si}} = \frac{\frac{Q_{gs,Si}}{I_{g,t2,Si}} + \frac{Q_{gd,Si}}{I_{g,t3,Si}}}{\frac{Q_{gs,SiC}}{I_{g,t2,SiC}} + \frac{Q_{gd;SiC}}{I_{g,t3,SiC}}} \tag{18}$$

Assuming that the gate current is equal for the two cases, Equation 18 can be simplified to Equation 19.

$$\frac{f_{s,SiC}}{f_{s,Si}} = \frac{Q_{gs,Si} I_{g,t3} + Q_{gd,Si} I_{g,t2}}{Q_{gs,SiC} I_{g,t3} + Q_{gd,SiC} I_{g,t2}} \tag{19}$$

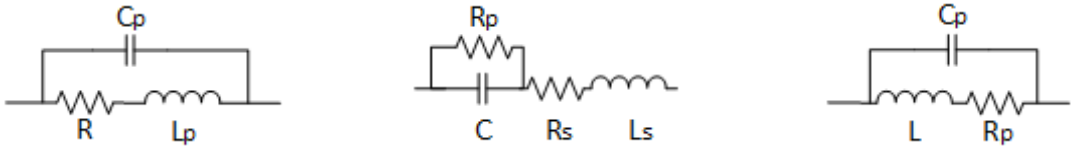
3.6 Circuit parasitic elements

There is no such thing as an ideal circuit. Any electronic circuit contain parasitic elements. These are present in both the circuit components and the physical layout of the circuit. The parasitic elements are present as either resistance, capacitance or inductance. Actually, a certain amount of all of these elements are present together. In some cases, these elements have little or no effect. In other cases, like sensitive high frequency operation, these elements can limit the performance of the circuit [7].

3.6.1 Parasitic elements in circuit components

A schematic of a resistor, capacitor and an inductor, including their parasitic elements, is shown in Figure 13. The parasitic components can cause unwanted coupling or be the cause of delayed response. The higher the frequency, the higher the influence of the parasitic components. A physical resistor can be seen as an ideal resistor with a series inductance and a parallel capacitance. For high frequency applications, metal film resistors is recommended. Metal film resistors have the lowest parasitic inductance, below 2nF. They also have the best capacitance characteristics. To minimize capacitance the capacitor should be small and compact, and have short leads. For this reason, SMD resistors are preferable [8].

A physical capacitor can be seen as an ideal capacitor with a series resistance and inductance, as well as a parallel resistance. The parallel resistance is usually a large value and only significant for small capacitance values [9]. The series inductance effectively reduces the impedance of the capacitor. The equivalent series resistance (ESR) of the capacitor is a source of loss, which inhibits the capacitors ability to source or sink charge. For a DC link, the ESR causes higher ripple. Therefore, it is a common practice to parallel capacitors, thus reducing the total ESR [10].



(a) *(b)* *(c)*

Figure 13: Equivalent schematics of circuit components including parasitic elements. (a) resistor; (b) capacitor; (c) inductor.

A physical inductor can be seen as an ideal inductor with a series resistance and a parallel capacitor. The series resistance represents the resistive copper loss in the inductor. Where the parasitic inductance in the capacitor reduces the capacitor impedance, the parasitic capacitance in the inductor increases the impedance of the inductor.

Both the capacitor and the inductor have a self-resonant frequency, determined by the capacitance and the parasitic inductance for the capacitor, and the inductance and the parasitic capacitance for the inductor. As the frequency increases towards the self-resonance frequency (SRF), the impedance of the capacitor decreases. At the SRF, the impedance is theoretically zero. Above the SRF, the impedance increases again, but the impedance of the capacitor is now inductive. As the frequency in the inductor increases towards the SRF, the impedance increases. At the SRF, the impedance is theoretically infinite. Above the SRF, the impedance decreases, but is now capacitive [9, 11].

3.6.2 Parasitic elements in physical layout

For the physical layout, parasitic resistance is usually not a problem. The copper tracks have much smaller resistance than the other components in the circuit, so the effect of this resistance is very small. One thing to be aware of however, is the size of the tracks. If these are not properly dimensioned, the copper cannot carry the current, and can overheat and destroy the circuit.

Since capacitive reactance is inversely proportional to frequency, parasitic capacitance have a large effect on high frequency circuits. This capacitance can cause unwanted coupling between two signals, resonance ringing with inductive elements and interference into high impedance circuits. Minimizing this capacitance is therefore very important. This can be achieved by either separating the copper tracks that must not be coupled as much as possible, or by putting an earthed ground plate between these tracks. In the boost converter, these tracks can be the tracks from the input to the MOSFET drain and the tracks from the output back to the MOSFET source.

Parasitic inductance can cause unwanted coupling, resonance ringing with capacitive elements or be the cause of delayed response in high frequency applications. The source of parasitic inductance is either as self-inductance or as mutual inductance. However, these are closely linked, so measures to reduce one, can also reduce the other. Self-inductance is the inductance

a current carrying loop produces and acts upon itself. Mutual inductance is the magnetic coupling between two current carrying loops.

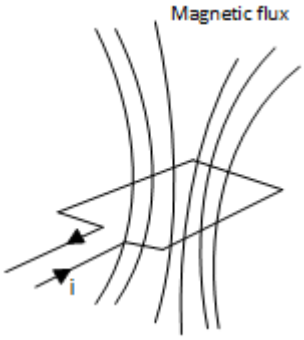


Figure 14: Self-inductance principal sketch.

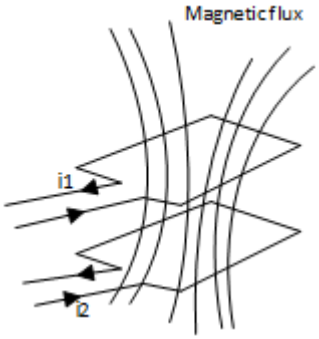


Figure 15: Mutual inductance principal sketch.

Parasitic self-inductance can be reduced by reducing the current loop area. This will limit the magnetic flux passing through the loop and thus limit the inductance. This will also have an effect on the mutual inductance, as the magnetic flux from one loop will have less influence on another. A common practice to reduce self-inductance in wiring is to twist the positive and negative wire around each other. In addition to reduce the effective area, this will also cause the direction of the magnetic field to alternate in opposite direction for each twist, cancelling each other out. Besides reducing the self-inductance of the loops, mutual inductance can be reduced by either separating the loops as far as possible, or making one loop perpendicular to the other. This will limit the effect one loop has one the other, although the latter has a practical issue on a single-board layout [7].

4 Silicon Carbide

This chapter presents the key features of silicon carbide as a semiconductor. The development of the SiC MOSFET and SiC Schottky diode is also presented. Much of the content in this chapter is obtained from the specialization project [12].

4.1 Material Properties

The theoretical limitations of Si semiconductors seem to have been reached. This has invoked a large interest in wide bandgap semiconductors, such as SiC. These have superior electrical properties compared to the standard silicon semiconductors. Table 2 compares the most important properties of SiC with Si.

Table 2: SiC properties compared to Si[13]

Property	**Si**	**4H-SiC**
Bandgap energy [eV]	1.12	3.2
Elec. mobility[$cm^2\ V^{-1}\ s^{-1}$]	1450	950
Critical elec. Field [$V\ cm^{-1}$]	$2.5 \cdot 10^5$	$2.2 \cdot 10^6$
Saturation velocity [$cm\ s^{-1}$]	10^7	$2 \cdot 10^7$
Thermal cond. [$W\ cm^{-1}\ K^{-1}$]	1.3	5

4.1.1 Bandgap energy

The bandgap energy of a semiconductor is the energy needed for an electron to break free from its bound state into a conducting state. The bandgap energy of 4H-SiC is 3.2 eV, which is about 3 times that of a Si semiconductor. Since the energy needed to break free an electron is higher, the leakage current of a SiC semiconductor is lower. It also mean that the device can handle higher temperatures than Si devices. Si MOSFETs are usually limited to operate at a junction

temperature below 150 degrees Celsius. Most SiC MOSFETs can operate at a junction temperature up to 175-200 degrees Celsius.

4.1.2 Critical electric field

The device can handle this electric field before breakdown occur. The critical electric field of a 4H-SiC is $2.2*10^6$ V cm^{-1}, which is about ten times that of a Silicon. The result of this is that the blocking layers can be thinner, with higher doping concentration, which in turn gives lower on-state resistance than for equivalent silicon devices.

4.1.3 Electron saturation velocity

This is the maximum velocity a charge carrier in a semiconductor can achieve. Therefore, it determines the frequency limitation of the semiconductor device. The SiC semiconductor has twice the electron saturation velocity than Si devices and consequently can operate at higher frequencies.

4.1.4 Thermal conductivity

The thermal conductivity of SiC is about 4 times higher than Si. This improves the heat spreading of the device. Since the heat dissipates faster from a SiC semiconductor than Si, the heatsink in the device can be smaller.

There are however, some holding points for SiC as of now. The cost/benefit factor is important for all businesses, and the cost of SiC components has been a two-digit factor higher than Si components with the same chip area. However, recent years improvements in wafer fabrication combined with higher production volume have contributed to a dramatic decline in the cost of SiC devices, making it a viable contender to Si devices [14].

In addition, the higher maximum junction temperature is of little practical use. In most packages it is the chip soldering or the wire bonding that limit the lifetime, and not the chip itself [15]. Furthermore, the electron mobility of SiC is lower than Si. This factor relates the applied

electric field and the drift velocity in the conductor. This implies that for the same electric field, the current moves faster through silicon than through silicon carbide.

4.2 SiC MOSFET

Because of its superior electrical and thermal properties, it is expected that SiC devices will replace Si in energy conversion applications. The clear benefits of SiC over Si has been known for some time now. However, problems with the reliability of gate oxide have delayed the development of the MOSFET.

A MOSFET is a unipolar semiconductor, which means that only one type of energy carrier is involved in conduction. There are two types of SiC MOSFET: UMOSFET and DMOSFET. The UMOSFET was the first type to be developed. The advantage of the UMOS is that it can be fabricated without ion implantation. The disadvantage is that its blocking voltage is limited by the oxide layer in the trench corner. In the trench corner, the electric field strength is increased, and the dielectric constant ratio increases the field further. This limited the breakdown voltage of the UMOS significantly. The advantage of the UMOS is that it have lower on-state resistance than DMOS. However, because of the issue with the breakdown of the gate-oxide layer, most manufacturers only develop DMOS, and progress is being made with lowering the conduction losses in these devices [16, 17].

In 1996, the first DMOS was introduced. This planar double-diffused MOSFET eliminated the trench problem. The first DMOS exhibited a breakdown voltage of 760 V, about three times higher than the best UMOS at the time. The cross-sectional area of the UMOS and DMOS is shown in Figure 16 [16].

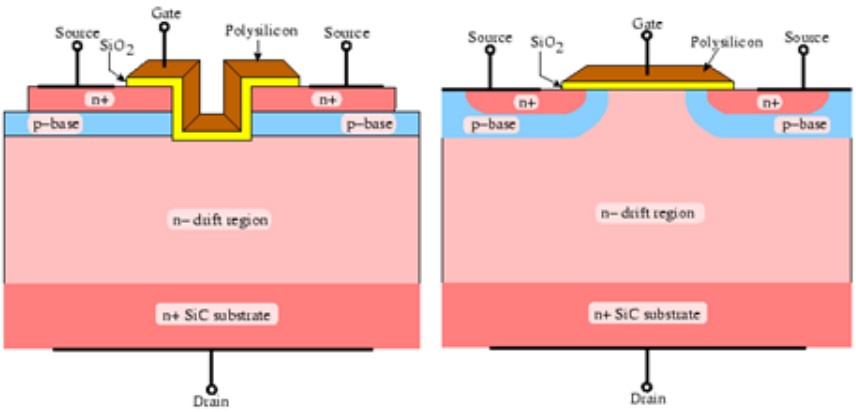


Figure 16: SiC MOSFET cross section. Left: UMOS. Right: DMOS [16].

4.3 SiC Schottky diode

A Schottky diode is formed by placing a thin metal film in direct contact with a semiconductor, usually an n-type. Compared to comparable *pn*-junction diodes, Schottky diodes have lower on-state voltage drop, faster turn-on and turn-off and much lower voltage overshoot at turn-on. The lower voltage drop in the Schottky diode is because of the significantly larger reverse saturation current. The reason for the faster turn-on and turn-off is that, in *pn*-junction diodes, stored minority carriers must be injected into, and pulled out of, the device in order to turn on and off. Schottky diodes are majority carrier devices and does not have these minority carriers. The lower voltage overshoot is a result of lower ohmic resistance in the drift region[1].

Because of these properties, SBDs may be preferable in power applications. However, because of the material properties of silicon and the geometry of the device, Si SBDs with blocking voltage over 200V cannot be reliably made [1]. The properties of SiC have proven to be nearly ideal for the SBD. The key features of the SiC SBD are higher breakdown voltage, lower leakage current, nearly no reverse recovery charge and lower forward voltage drop[15].

Unlike conventional Schottky diodes, which have reverse recovery charge, Q_{rr}, SiC Schottky diodes have capacitive charge, Q_c. The capacitive charge is low compared to the reverse recovery charge. Additionally, the capacitive charge is independent of current, *di/dt* and temperature, whereas the reverse recovery charge of a Si diode is strongly dependent of these. This consequence of this is lower recovery time and lower switching loss in the diode [5].

5 MOSFET comparison

In order to get an overview over the difference between silicon and silicon carbide semiconductors, this chapter will compare two of the top MOSFET models from STMicroelectronics. They are STW62N65M5 and STC30N120.

The STW62N65M5 is a silicon power MOSFET based on STMicroelectronics trademarked MDmesh M5 and PowerMESH technology. This MOSFET has a very low drain-source resistance, and compared to other conventional silicon based MOSFETs, low gate charge and input capacitance.

The STC30N120 is a silicon carbide power MOSFET. It thus have the benefits of low capacitance, high operating temperature capabilities and low thermal influence on switching loss and on-resistance.

Optimally, this chapter would compare the SiC MOSFET used in laboratory testing. The datasheet for this MOSFET is, however, not complete, and this chapter aims to illuminate the two MOSFETs under various conditions not yet determined for the STC90N65G2V MOSFET.

5.1 On Resistance ($R_{DS(ON)}$)

One of the first things listed for a MOSFET is the on-resistance. This corresponds to the conduction loss of the MOSFET. Because of the progress made for silicon MOSFET structure, STW62N65M5 have an on-resistance of 41-49mΩ, while STC30N120 have an on-resistance of 90-100mΩ, about twice as much. While conducting under the same conditions, the silicon MOSFET would thus be expected to have half of the power loss compared to the silicon carbide MOSFET. However, these values from the datasheets are listed for an operating temperature of 25°C, which is an unlikely operating temperature when operating in high power and frequency. The normalized on-resistance vs temperature graphs for each MOSFET is found in Figure 17.

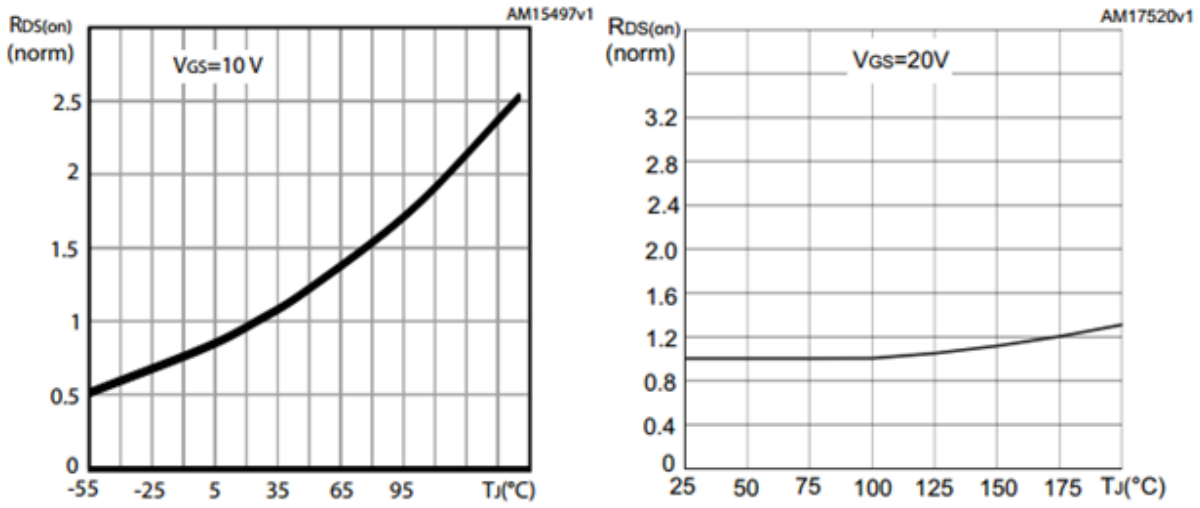


Figure 17: Normalized drain-source on-resistance vs temperature. Left: silicon. Right: silicon carbide.

From Figure 17 the difference in temperature dependency becomes clear. From 25°C to 125°C the on-resistance of the silicon MOSFET more than doubles, while the on-resistance of silicon carbide MOSFET increases with a factor of 1.1. This means that when operating at high temperatures, the on-resistance of the two MOSFETs equalizes.

5.2 Intrinsic Capacitances

MOSFETs have intrinsic capacitances between gate and source, gate and drain, and drain and source. These capacitances are dependent by the MOSFET structure, material and voltage. Since these capacitances are related to the switching speed, and are independent of temperature, the switching speed of a MOSFET is independent of temperature. Figure 18 show the locations of these capacitances in a MOSFET cross section and in a circuit perspective.

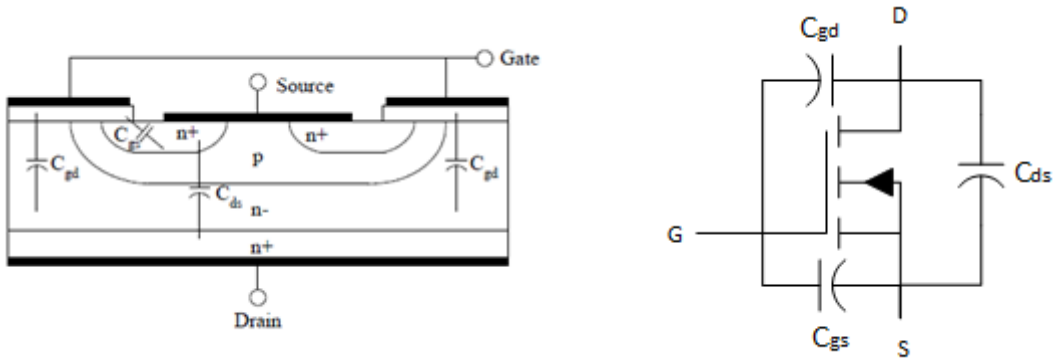


Figure 18: MOSFET intrinsic capacitance. Left: Cross-section; Right: Circuit perspective

Datasheets operate with three capacitance parameters. These are the input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}). The input capacitance is measured from gate to source with the drain shorted to source, so $C_{iss}=C_{gs}+C_{gd}$. In order for the MOSFET to turn on, the input capacitance must be charged to the threshold voltage. In order to turn off, the input capacitance must be discharged to the plateau level. Therefore, this capacitance is related to the delay time at turn-on and turn-off. The output capacitance is the capacitance measured between drain and source, with the gate shorted to source, so $C_{oss}=C_{gd}+C_{ds}$. This capacitance is mostly important in soft switching applications, as it affects the resonance of the circuit. The reverse transfer capacitance, also referred to as the Miller capacitance, is measured between the MOSFET drain and gate with source grounded, or $C_{rss}=C_{gd}$. This capacitance is one of the most important parameters affecting the rise and fall time of the voltage during switching.

5.3 Gate charge

The gate charge is often used when designing the gate drive circuit because it takes into account the changes in capacitance with changes in voltage. It reflects charge stored in the intrinsic capacitances.

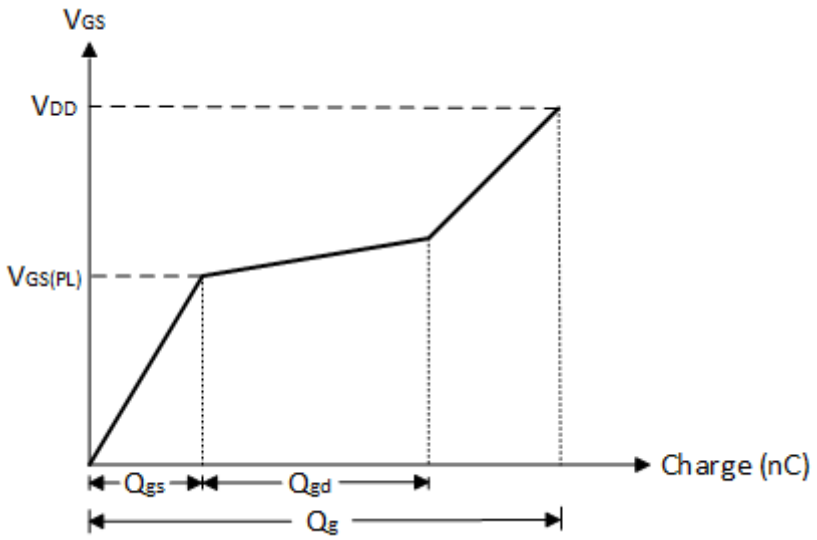


Figure 19: MOSFET gate charge vs gate-source voltage

Qgs is the charge from the origin to the first inflection in the curve. Qgd is the charge from the first to second inflection. Qg is the total gate charge, from the origin to the point where the gate voltage equals the specified gate drive voltage.

From this, it is clear that the gate charge and the intrinsic capacitance is crucial for the switching speed of the MOSFET.

Table 3: Capacitance and charge comparison of silicon and silicon carbide MOSFET

Parameter	**STW62N65M5[18]**		**SCT30N120[19]**	
Ciss	6420 pF	V_{DS}=100 V	1700 pF	V_{DS}=400 V
Coss	170 pF	V_{GS}=0	130 pF	V_{GS}=0
Crss	11 PF	f=1 MHz	25 pF	f=1 MHz
Qg	142 nC	V_{DS}=520 V V_{GS}=0/10 V I_D=23 A	105 nC	V_{DS}=800 V V_{GS}=0/20 V I_D=20 A
Qgs	34 nC		16 nC	
Qgd	58 nC		40 nC	

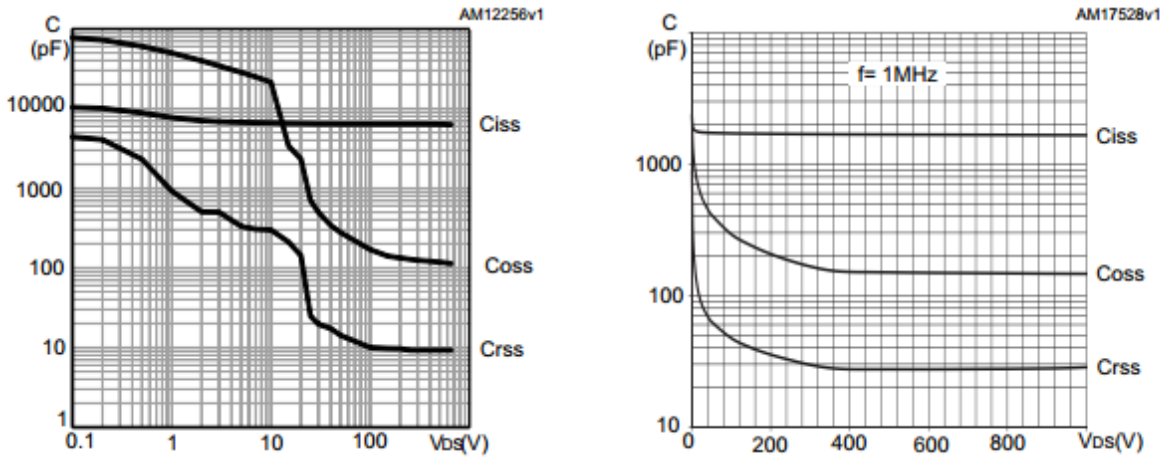


Figure 20: Input, output and Miller capacitance vs drain-source voltage. Left: silicon [18]; Right: silicon carbide [19]

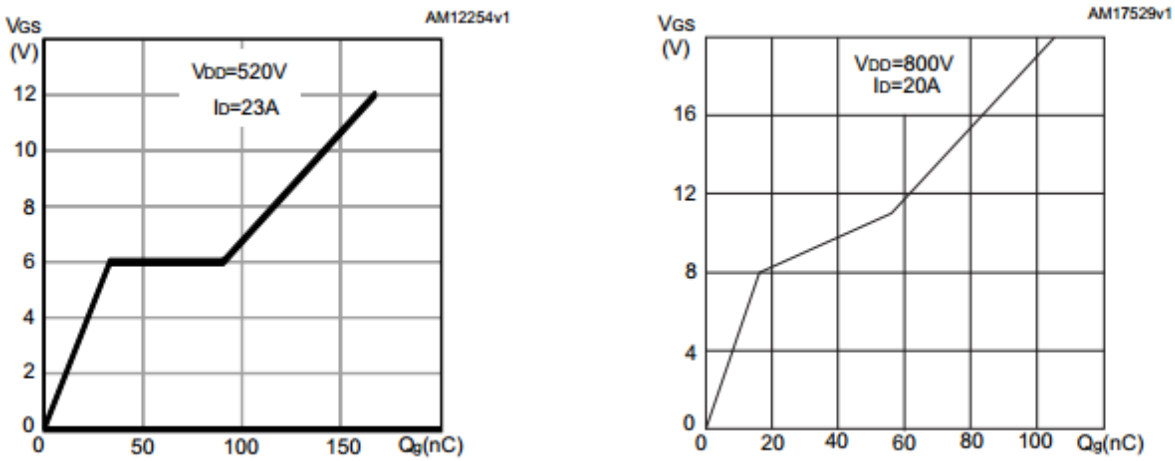


Figure 21: MOSFET gate charge vs gate voltage curve. Left: silicon [18]; Right: silicon carbide [19]

The main difference between the two with regards to the capacitance is the input capacitance, which is about 3,5 times higher for the silicon MOSFET. The silicon carbide MOSFET will therefore have much less delay time and turn on faster. The silicon MOSFET actually have a smaller reverse transfer capacitance. This suggest that the voltage rise and fall times are lower for the silicon MOSFET than for the silicon carbide MOSFET.

Looking at the gate charge for the MOSFETs, the total charge needed for the silicon carbide MOSFET is significantly smaller than the silicon MOSFET.

5.4 Loss calculations

Several different alternatives for calculating switching loss have been suggested. This chapter aims to compare the silicon and the silicon carbide MOSFETs using some of these approaches.

5.4.1 Datasheet energy loss

The first alternative is using the energy loss listed in the MOSFET datasheet. These energy losses are listed for a specific voltage and current, so they need to be scaled to the voltage and current in question. Table 4 lists the energy loss obtained from the datasheet for STW62N65M5 and SCT90N65G2V, as well as the scaled total energy loss.

Table 4: Datasheet energy loss and scaled energy loss

Energy loss	STW62N65M5	Test condition	SCT90N65G2V	Test condition
Eon	500 µJ	V_{DS} = 400 V	250 µJ	V_{DS} = 400 V
Eoff	100 µJ	I_D = 38 A	220 µJ	I_D = 50 A
Esw	600 µJ		470 µJ	
Esw, scaled	207 µJ	V_{DS} =350 V I_D = 15 A	123 µJ	V_{DS} =350 V I_D = 15 A

The scaled total energy loss is multiplied with frequency in order to obtain the power loss in Figure 22.

Figure 22: Calculated switching loss from datasheet energy loss

5.4.2 Output capacitance and gate charge

This calculation is based on a paper from Texas Instruments [20]. The equation states that the switching energy loss is the loss associated with the energy stored in the MOSFET output capacitor and the energy lost by the gate-drain charge.

$$E_{sw} = \frac{1}{2} \cdot \left(C_{OSS} \cdot (V_{DS} + V_d)^2 + (V_{DS} + V_d) \cdot \frac{I_D}{1 - d} \cdot \frac{Q_{GD} \cdot R_G}{V_{GS} - V_{TH}} \right) \quad (20)$$

Inserting the datasheet parameters for C_{OSS}, V_{TH} and Q_{GD}, as well as the circuit parameters, yields the energy losses in Table 5.

Table 5: Calculated switching energy loss from Equation 20.

	STW62N65M5	SCT90N65G2V
Esw	152,7 µJ	104 µJ

The switching energy loss in Table 5 is multiplied frequency in order to obtain power loss. The conduction loss is added to the switching loss, and the total MOSFET power loss over a frequency range is found in Figure 23.

Figure 23: Calculated MOSFET power loss from Equation 20.

5.4.3 Input and Miller capacitance

From [5] turn-on and turn-off times are calculated related to the input capacitance and the Miller capacitance.

$$t_{on} = C_{iss} \cdot R_g \cdot \ln\left(\frac{V_{gs} - V_{th}}{V_{gs} - V_{pl}}\right) + C_{rss} \cdot R_g \cdot \left(\frac{V_{ds} - V_{pl}}{V_{gs} - V_{pl}}\right) \quad (21)$$

$$t_{off} = C_{rss} \cdot R_g \cdot \left(\frac{V_{ds} - V_{pl}}{V_{pl}}\right) + C_{iss} \cdot R_g * \ln\left(\frac{V_{pl}}{V_{th}}\right) \quad (22)$$

The first part of the expression for t_{on} estimates the time it takes for the input capacitance to be charged from the threshold voltage to the Miller plateau, i.e. the current rise time. The second part for the expression estimates the time for the Miller capacitance to be charged, i.e. the voltage fall time.

The expression for t_{off} calculates the same as t_{on}, but in reverse order. First, the Miller capacitance is discharged, estimating the voltage rise time, then, the input capacitance is discharged, estimating current fall time.

In order to calculate the turn-on and turn-off times, the Miller plateau voltage must be known. This voltage is dependent on a number of factors, such as gate voltage, gate resistor and drain current. The turn-on and turn-off times are multiplied with the turn-on and turn-off conditions to obtain the energy loss, and again with the frequency to obtain the power loss. Figure 24 shows the power loss for STW62N65M5 silicon, and SCT90N65G2V silicon carbide MOSFETs with a 10Ω gate resistor.

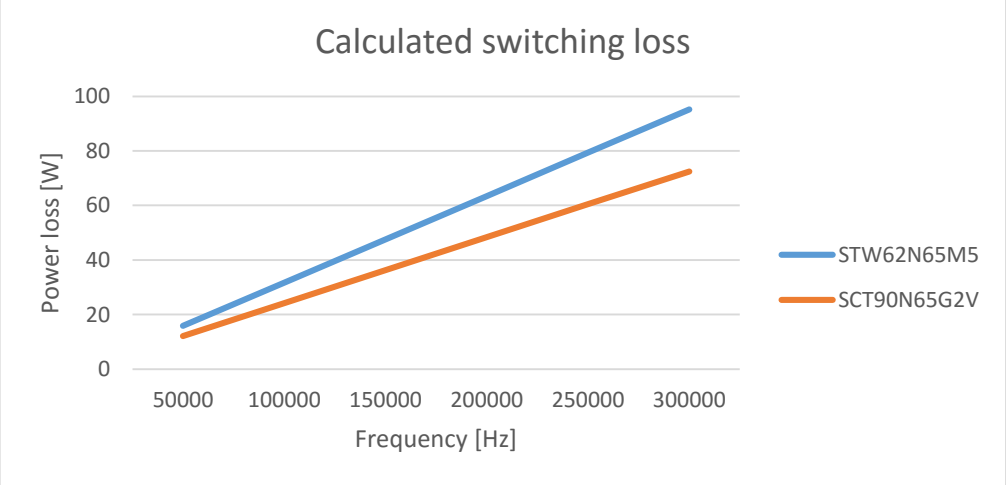


Figure 24: Calculated switching loss from [5].

5.4.4 Loss summary

Comparing the three different approaches, number one and two gives the lowest loss. The two have similar loss tendencies. Although compared to the first approach, the second gives lower loss for the SiC MOSFET and higher loss for the Si MOSFET. Approach three differ greatly from the other two, with losses more than twice as high.

Therefore, approach three seems unlikely. However, which one is more correct than the others can first be found out from the practical testing. The one thing that can be concluded from these calculations is that the SiC MOSFET is expected to experience lower loss than the Si MOSFET does. Figure 25 shows the averaged switching loss from all three approaches.

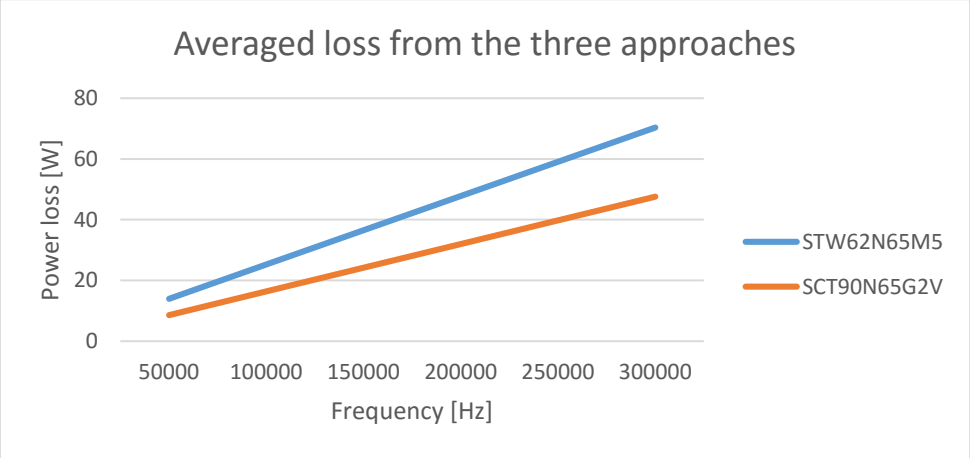


Figure 25: Averaged switching loss from the three previous approaches.

By using Equation 19, an estimation of the difference in switching frequency at equal switching loss can be calculated. Q_{gs} and Q_{gd} values for the MOSFETs are obtained from the datasheets [18, 21]. For simplicity, the gate current are assumed equal. If the maximum gate current is limited to 5A and minimum gate current 1A, then calculating through every combination, the SiC MOSFET should be able to switch between 1,2 and 1,5 times faster than the Si MOSFET with the same switching loss. Since the frequency is inversely proportional to the energy loss, the SiC MOSFET energy loss should then be between 0,67 and 0,83 times lower than the Si MOSFET.

5.4.5 Loss and switching time

According to Valeo, the MOSFET power loss is 25W in their PFC. Using Equations 14 and 15 from Chapter 3.5 estimated maximum switching time to achieve the same power loss at different switching frequency is calculated. The results are shown in Figure 26.

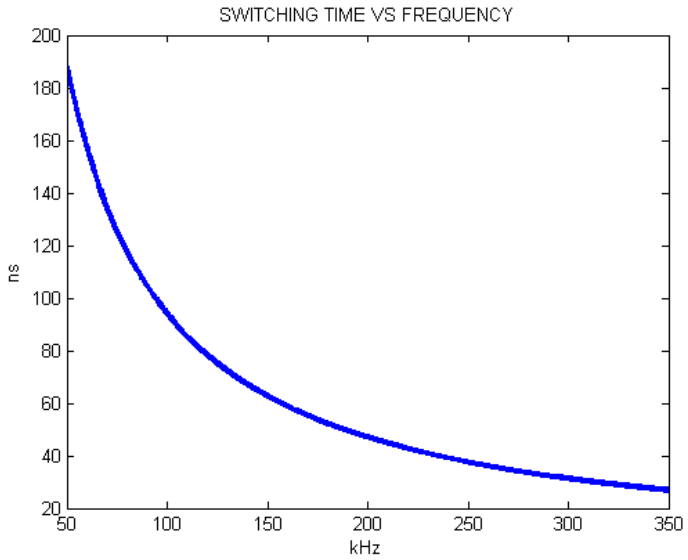


Figure 26: Calculated maximum total switching time to achieve 25W MOSFET power loss.

According to the calculations presented in Figure 26, the total switching time at 100 kHz can be in excess of 90ns to obtain a 25W power loss. In order to increase the switching frequency to 300 kHz without increasing the losses, the total switching time need to be reduced to about 30ns.

These calculations do not include the MOSFET conduction loss, so the total loss is a bit higher, and thus the frequency should be somewhat lower. How much depends on the on-state resistance of the MOSFET. At rated 3,5 kW power, the conduction loss will be between 3,4W and 7,5W for the silicon MOSFET, and 2W and 2,4W for the SiC MOSFET, depending on the temperature.

Losses in the circuit also occur in other components, predominantly in the boost inductor and diode. Expected losses in these components are calculated in Table 6.

Table 6: Expected inductor and SBD power loss at rated power.

Component	Loss
500 µH inductor	11,6 W
136 µH inductor	5,8 W
SiC SBD	13,5 W

Additional losses will occur in the converter. Capacitor losses, inductor core losses and losses in the circuit copper leads will contribute to efficiency reduction. Figures for these losses are, however, difficult to determine, and the effect of these losses are small compared to the ones previously mentioned.

In order to operate the converter at 98% efficiency, total power loss in the converter cannot exceed 70W. Using the 500 µH inductor, then the maximum total loss in the MOSFET can be 45, 9 W. This means that the switching loss for the switching loss for the Si MOSFET cannot exceed between 38,4 W and 42,5 W, and the SiC MOSFET between 43,5 W and 43,9 W, depending on the temperature. However, these losses are high, and can damage the MOSFET, so the switching loss should be well below this. Nevertheless, it shows that the SiC MOSFET can in theory have higher switching loss than the Si MOSFET, and still have the same total loss, and therefore push the frequency even higher.

6 Laboratory test

The practical part of the thesis was to build a DCDC boost converter with a simple gate driver circuit. The driver is controlled simply by a function generator, avoiding voltage and current sensing to control the output. The focus in this work is on the switching behavior of the MOSFET.

This chapter describes the practical part of the thesis. The laboratory setup is described, the equipment and measurement tools used is presented, as well as the circuit and its components.

6.1 Set-up

Figure 27 shows a simple chart overview of the test setup. The input of the step-up converter is provided by a DC voltage source, the output is a resistive load. The gate driver is driven by a separate DC source and the input signal is provided by a function generator. The desired waveforms in the converter are probed and captured on an oscilloscope. A picture of the laboratory setup is found in Appendix A.

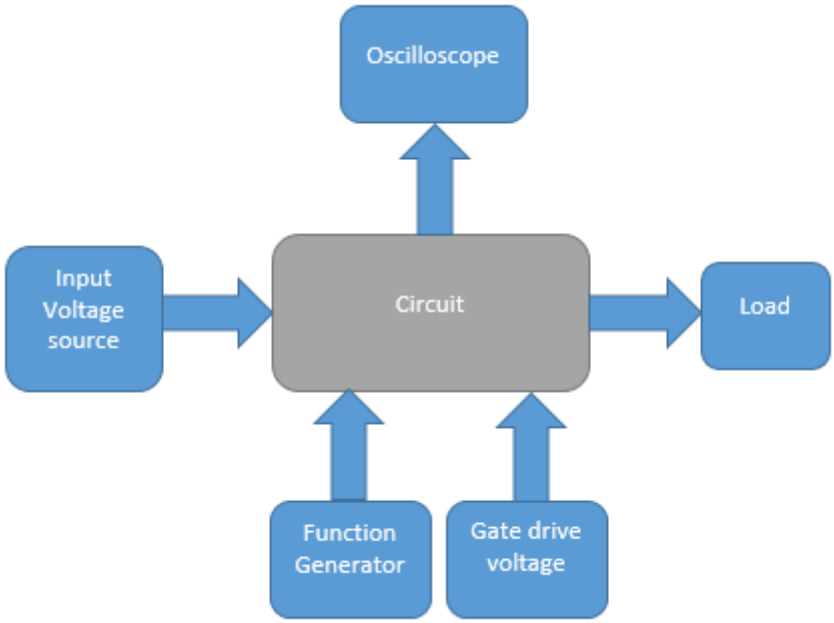


Figure 27: Chart overview of laboratory set-up.

Due to a shortage in available equipment, no voltage source with the desired ratings was obtainable initially. Therefore, the input voltage is provided through two dual voltage sources, making it four in total, in series. This however, only enabled a maximum input of 100V and 4A, drastically limiting the power capability. Eventually a DC source capable of 300V and 24A was obtained, enabling operation at rated power.

6.1.1 Equipment

Apart from the circuit itself, a substantial amount of equipment is needed to perform the necessary tests. This includes power supplies, measuring equipment and square wave generator. A complete list of the equipment used is found in Table 7.

Table 7: List of lab equipment.

Equipment	Application	Model
DC power supply	Converter input	TTi EX354RD
DC power supply	Converter input	TENMA 72-10495
DC power supply	Converter input	ETSYSTEM LAB/SM6300
DC power supply	Gate driver voltage	TTi EL303R
Differential probe	Voltage measuring	Tektronix P5200A
Function generator	Gate driver pulse	Wavetek 187
Isolation transformer	Isolate oscilloscope from grid	N/A
Multimeter	Various measurement	Fluke 175
Oscilloscope	Switching Waveforms	Tektronix TDS 2014B
Oscilloscope	Floating measurements	Tektronix TDS 2014
Rogowski coil	Current measuring	PEM CWT 6B

6.1.1.1 Oscilloscope

The waveforms measured in the circuit are captured on a Tektronix TDS2014B oscilloscope. The scope parameters are listed in Table 8. It has a 100 MHz bandwidth and a sample rate of 1 GS/s [22]. The bandwidth is the frequency at which the oscilloscope can measure a sine wave

with 70.7% accuracy. A bandwidth of 100 MHz means that it can measure a sine wave at +/- 2% accuracy at 20 MHz. Sample rate is the number of samples the oscilloscope captures per second. It determines how much waveform details the scope can capture. A higher sample rate means a better representation of the signal measured [23].

Table 8: Tektronix TDS2014B oscilloscope parameters [22].

Parameter	**Value**
Bandwith	100 MHz
Sample rate	1 GS/s
Channels	4

Floating measurements were performed on the gate voltage. The waveforms were captured on a battery-powered scope, Tektronix TDS2014. This scope is therefore disconnected from ground potential, removing fault sources. The floating measurements are done with a passive probe. This probe has a much shorter ground lead than the passive probes.

6.1.1.2 Voltage measuring

When probing in a circuit, a small signal current must go through the probes. This adds a load to the circuit, which can change the signal. The loading is defined as a resistive load in parallel with a capacitive load. For most cases, the resistive loading is negligible, as the probes resistance is much higher than the circuits. The loading of the greatest concern is the capacitive. This loading affects the measurement by reducing bandwidth and increasing rise time. For low frequency measurements, the capacitive reactance is very high, which has little effect. At high frequencies, this reactance decreases, which increases the loading. Additionally, the probe leads are wires, which has some amount of distributed inductance. This inductance interacts with the probe capacitance, causing ringing at a certain frequency that is determined by the inductance and capacitance values [24].

Tektronix P5200A differential probes are used for most of the voltage measurements. The parameters of this probe is listed in Table 9 .

Table 9: Tektronix P5200A differential probe parameters [25].

Parameter	Value
Bandwidth	50 MHz
Differential input impedance	10 MΩ||2pF

Some measurements are performed with passive probes. The passive probes have a 100 MHz bandwidth and 22pF capacitive loading. The resistive loading is the same as the differential probe.

6.1.1.3 Current measuring

The switching current is measured using a Rogowski coil, which utilizes Ampere's law to measure the current. It consist of a wire wound on an air-core, or non-magnetic core. Changes in the magnetic field caused by changes in the current induces an EMF voltage in the coil. The output of the Rogowski coil is integrated to produce an output voltage proportional to the current. Among the advantages of the Rogowski coil are that it is non-intrusive, not influenced by external magnetic fields and can measure large currents without saturating[26, 27]. The Rogowski coil used for current measurements is the CWT06 from Power Electronics Measurements Ltd. Its parameters are listed in Table 10.

Table 10: PEM CWT06 parameters [28].

Parameter	Value
Bandwidth	30 MHz
Sensitivity	50 mV/A
Peak *di/dt*	8 kA/µs
Peak current	120 A

The peak current and di/dt ratings are well within the circuit parameters. The sensitivity describes the relationship between the scope readings and measured current. 50 millivolts on the scope equals one ampere. The bandwidth could be a source of concern. A bandwidth of 30 MHz means that any oscillations above this frequency might not be accurately picked up by the probe, and not all switching transients can be trusted completely.

6.2 Measurement considerations

In order to reduce the chance of faulty measuring, efforts were made avoiding ground loops, which is the case when there are more than one path for the current to flow to ground. Every supply equipment and the oscilloscope is connected to ground through their power chord. Because of this, the circuit ground potential might be different from the oscilloscopes ground potential. When probing in the circuit, the negative probe would be connected to the circuit ground potential, through the probes galvanic isolation, then to the oscilloscopes ground. If these potentials are different, measurements of events that does not actually occur in the circuit might be observed.

This effect is avoided/reduced by creating one common ground reference for the circuit and the oscilloscope. The scopes power chord is connected through an isolation transformer, separating it from ground. One mutual grounding point is selected through one of the voltage supplies, and all supplies negative potential and the scope ground is connected to this point.

A concern when measuring fast low-voltage transients, like the gate voltage, is that the differential probes might be too influential. Long probes and probe wires cause a large area and a long path, which can have a significant impact on the measured voltage. Ideally, passive probes with a shortest possible area between the probe tip and ground should be used. However, this require a floating scope, a scope not connected to the ground potential.

6.3 Test Circuit

Figure 28 show the schematic of the final circuit. The MOSFET driver is FAN3224T/UCC27531D. The practical difference between these drivers is that FAN3224T requires an enable signal whereas UCC27531D does not. The enable signal is realized by connecting the enable pin to the driver supply voltage through a resistor. The input signal is provided by a function generator. The driver supply voltage, input signal and converter input voltage all share the same negative potential, causing the MOSFET gate to source voltage to be 0/VDD. A capacitor is placed over the driver IC between the driver supply voltage and ground. This is to create a shortest possible current path. The external voltage supply charges the capacitor and this then acts as the voltage supply to the driver. This will also reduce rippling in the supply voltage due to the switching.

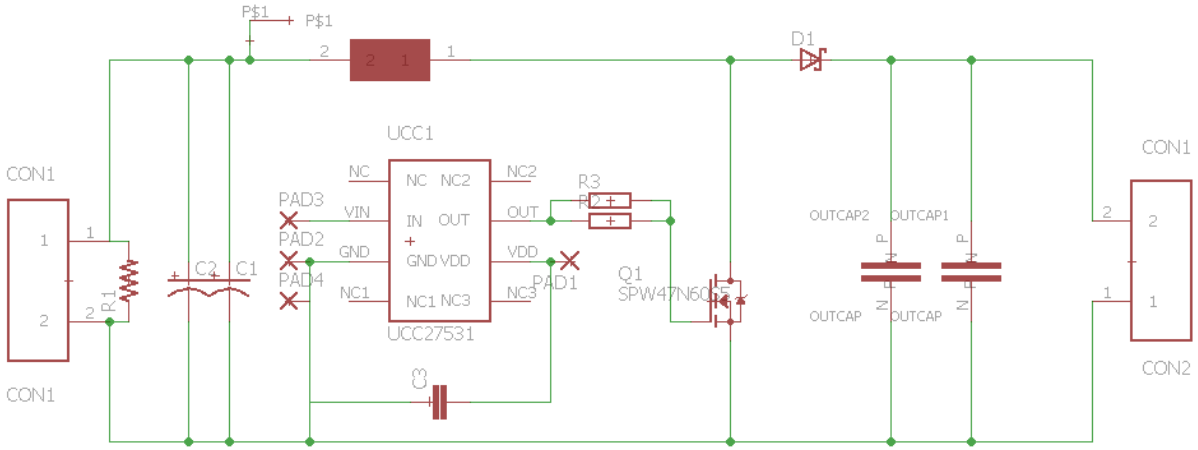


Figure 28: Boost converter schematic.

6.4 Circuit components

Three different circuit layouts have been tested, and some components have been changed throughout the testing. All circuit components used are listed in Table 11, and a more detailed description of these components are presented in the following sub-chapters.

Table 11: List of circuit components.

Component	Type
Si MOFET	STW62N65M5, ST
SiC MOSFET	SCT90N65G2V, ST
SiC Schottky diode	SCS220AE, ROHM
Boost inductor	500µH 100kHz choke 136µH 300kHz choke, PREMO
Input capacitor	33µF 350V
Input discharge resistor	25kΩ metal film resistor
Output capacitor	270µF, 450V, NIPPON CHEMI
Gate driver	FAN3224T, Fairchild UCC27531D, TI
Gate resistor	Metal film resistors Thin film SMD resistors (1206)
Gate driver capacitor	1µF through-hole tantalum 0,47µF ceramic SMD (1206)

6.4.1 Si MOSFET

The Si MOSFET used is STW62N65M5 from STMicroelectronics. The intrinsic capacitances and gate charges are discussed in Chapter 5. Other important ratings are listed in Table 12.

Table 12: SWT62N65M5 parameters [18].

Parameter	Test condition	Value	Unit
Drain-source breakdown voltage	V_{GS}=0 V I_D=1 mA	650	V
Drain current	Tc=25 ºC Tc=100 ºC	46 26	A
Gate threshold voltage	V_{DS}=V_{GS} I_D=260µA	3-5	V
Static drain-source on-resistance	Tj=25 ºC Tj=125 ºC	42 93	mΩ

6.4.2 SiC MOSFET

The SiC MOSFET tested in the converter is SCT90N65G2V from STMicroelectronics. As of now, not all characteristics of the MOSFET are yet determined, therefore the datasheet has some shortcomings. However, the most important features are listed in Table 13.

Table 13: Parameters of SCT90N65G2V SiC MOSFET [21].

Parameter	**Test condition**	**Value**	**Unit**
Drain-source breakdown voltage	V_{GS}=0 V I_D=1 mA	650	V
Drain current	Tc=25 ºC Tc=100 ºC	90 80	A
Gate threshold voltage	V_{DS}=V_{GS} I_D=1mA	1.9-3.2	V
Static drain-source on-resistance ($R_{DS(on)}$)	Tj=25 ºC Tj=150 ºC Tj=200 ºC	25 27 30	mΩ
Input capacitance (C_{iss})	V_{DS}=400 V f=1 MHz V_{GS}=0 V	3300	pF
Output capacitance (C_{oss})		320	pF
Reverse transfer capacitance C_{rss})		50	pF
Total gate charge (Q_g)	V_{DS}=400 V I_D=50 A V_{GS}=0V/20V	160	nC
Gate-source charge (Q_{gs})		32	nC
Gate-drain charge (Q_{gd})		35	nC

It is worth noticing the low temperature dependency of the MOSFET. From 25 ºC to 100 ºC the current rating is reduced 11 %, while the silicon MOSFET current rating in the same temperature range is reduced 43.5 %. The on-resistance is very low, only 25mΩ at a junction temperature of 25 ºC. At 200 ºC the on-resistance is 30mΩ, only a 20 % increase. The silicon MOSFET on-resistance doubles from a junction temperature of 25 ºC to 125 ºC, as discussed in Chapter 5.

6.4.3 SiC Schottky diode

The SiC SBD in the converter is SCS220AE from ROHM. It is rated for 650V reverse voltage and 20A forward current, and its forward voltage drop is 1,35V at the rated forward current. The forward V-I characteristics of the SiC Schottky diode is shown in Figure 29.

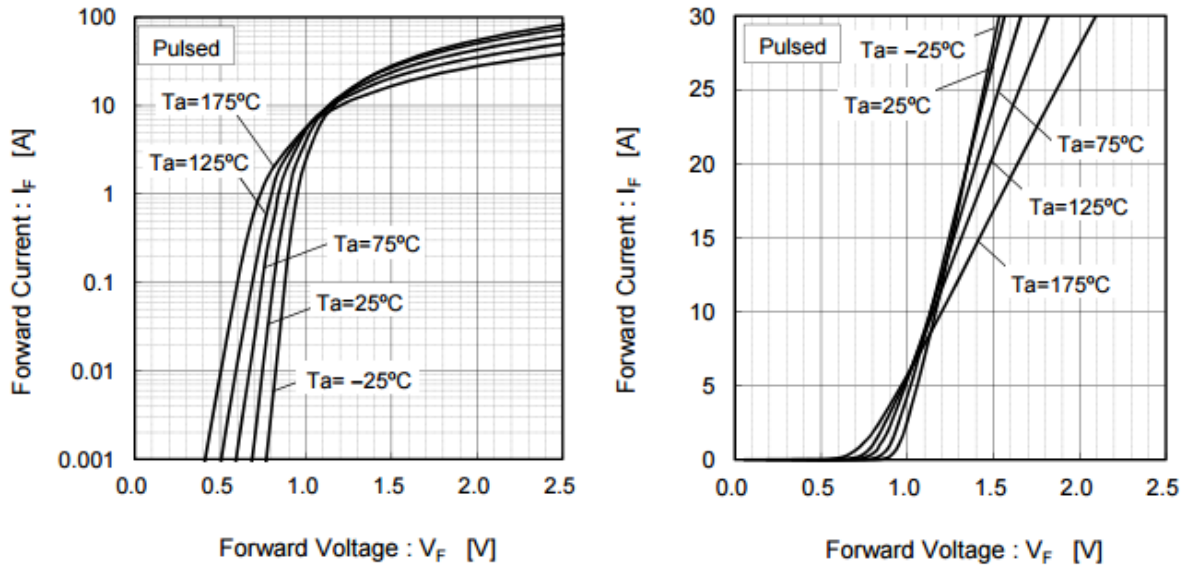


Figure 29: Forward I-V characteristic of SCS220AE SiC SBD [29].

6.4.4 Boost choke inductor:

Two different inductors was used in the boost converter. One is the original PCF choke inductor used in the GEN2 charger today, and the other is a 300 kHz inductor special ordered from PREMO.

The high frequency inductor is 136µH rated for 16Arms and 300 kHz. Its DC resistance is 25mΩ. The inductor is 33mm in diameter and 27,5mm high. The size difference of the two inductors can be seen in Figure 30. The 136µH have benefits including smaller core, reducing weight and occupied space, and fewer turns, reducing copper loss.

Figure 30: Boost choke inductor size comparison.

6.4.5 Capacitors

The input capacitors are two parallel 33µF capacitors rated at 350V. The output capacitors are two parallel 270µF capacitors rated at 450V. The capacitors are paralleled for two reasons, to obtain a suitable capacitance, and to reduce the ESR.

6.4.6 Gate driver

Two different gate driver ICs are tested. These are FAN3224T from Fairchild and UCC27531D from Texas Instruments. Both are in SOIC-8 package. The most important features of the two gate drivers are found in Table 14.

FAN3224T is the gate driver used in Valeos' GEN2 charger. The driver chosen for the SiC MOSFET should then have similar features, but higher voltage capabilities. While the FAN3224T driver have dual input/output, meaning it can switch two MOSFETs, the UCC27531D driver have a single input/output.

Table 14: Features of FAN3224T[30] and UCC27531D[31] gate driver ICs.

Parameter	FAN3224T	UCC27531D	Unit
Voltage rating	4.5-18	10-35	V
Isource/sink	5	2.5/5	A
Propagation delay	17	17	ns
Rise time	12 @2.2nF	15 @1.8nF	ns
Fall time	9 @2.2nF	7 @1.8nF	ns

The two drivers are similar in terms of delay, rise and fall time. The most important difference is that the FAN3224T gate driver is limited to 18V. This limitation makes it unideal for switching SiC MOSFETs, as the recommended gate voltage usually require 20V. The maximum voltage of the UCC27531D is safely above this requirement.

6.4.7 Gate circuit components

The gate resistor value is varied during testing. For the first two circuits, through-hole metal film resistors was used. For the third circuit layout, thin-film SMD resistors in 1206 package was used.

For the first two circuits, a 1µF through-hole tantalum capacitor was placed over the V_{DD} pin and ground pin of the gate driver. In the third circuit layout, a ceramic 0.47µF ceramic 1206 SMD capacitor was mounted on the board between these pins.

6.5 Parasitic elements in the boost converter

In Figure 31, the schematics of the setup is redrawn to include some of the parasitic inductance that occur in the circuit. These inductances influence the waveforms during switching. Especially L4 and L5 in the schematics cause voltage overshoot at turn-off. Moving the boost choke inductor as close to the MOSFET drain as possible, shortening the leads to a minimum, will reduce L4. Correspondingly, shortening the path from the source of the MOSFET to the return path will reduce L5.

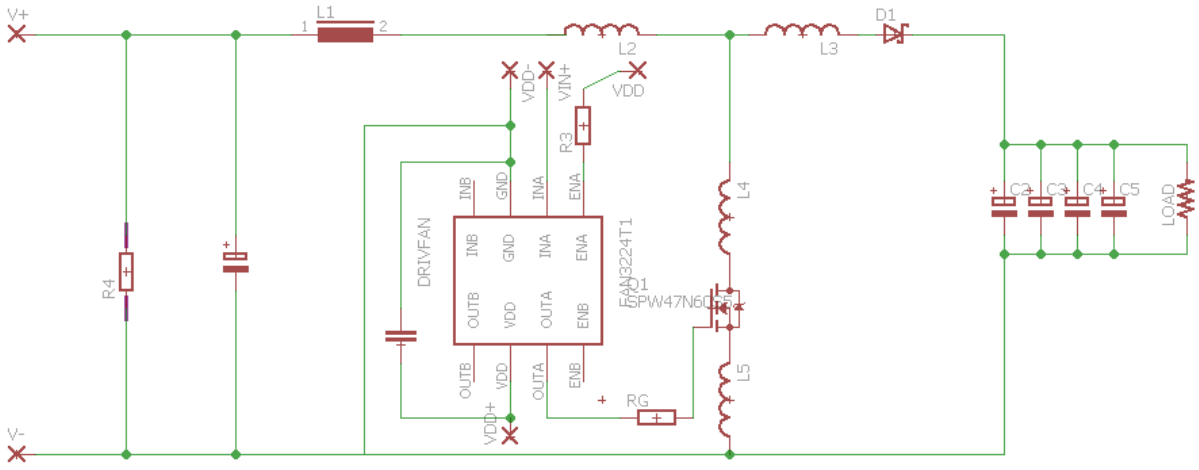


Figure 31: Parasitic inductance in the boost converter.

Parasitic inductance also occurs in the gate path. This inductance influence the switching speed and fluctuations in the gate voltage, which can cause poor switching behavior and unwanted turn-on/turn-off. The hatched area in Figure 32 is important for the parasitic inductance in the gate circuitry, represented as L1.

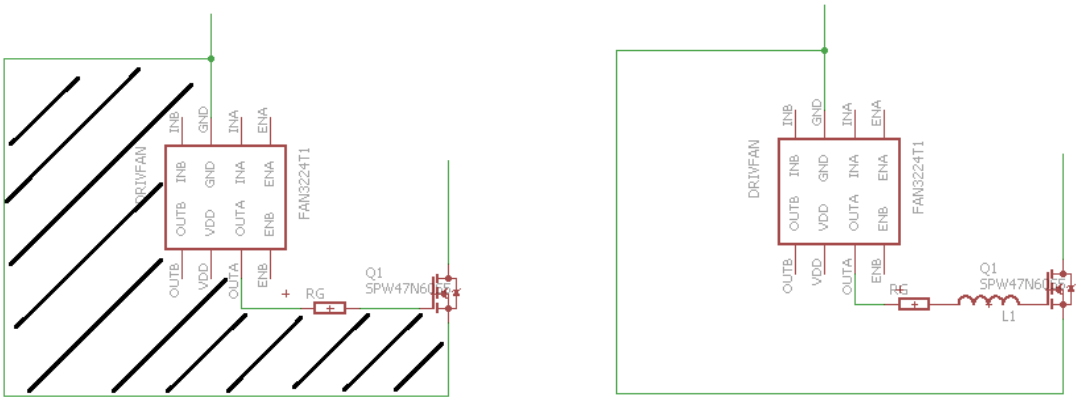


Figure 32: Parasitic inductance in the gate driver.

The size of the area influence the size of the parasitic inductance. Minimizing this area will minimize the inductance. Shortening the paths, while placing them as near to each other much as possible, as seen in Figure 33, will minimize the inductance. Ideally, the gate lead and the return lead should lie directly on top of each other, one on each side of the board.

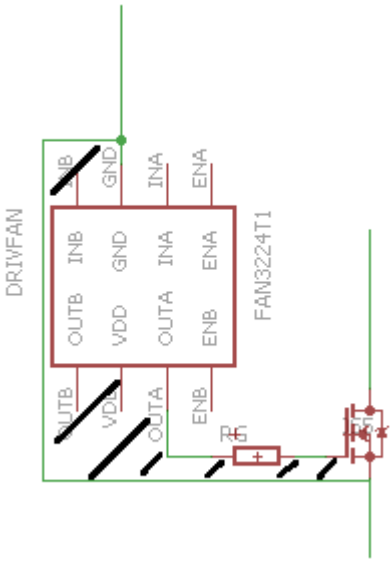


Figure 33: Minimized parasitic inductance in the gate driver.

The parasitic components in the circuit cause unideal and undesired effects, and must be eliminated as much as possible in order to obtain best possible switching behavior. An ideal circuit does not exist, and some parasitic elements is unavoidable.

7 Laboratory results

Two factors will be the focus in the laboratory testing. First, the influence of the circuit layout will be considered. Three different prototype board were tested, a veroboard, a PCB layout and an improved PCB layout. Second, the improved PCB layout will be tested at rated power, and the voltage and current switching waveforms for the Si and SiC MOSFET will be observed and compared.

Initial testing was performed on STW62N65M5 silicon MOSFET and the gate driver used in this case was FAN3224T. The purpose was to optimize the circuit parameters. To prevent overheating the MOSFET and damage it, the pulse used was set at a low frequency, about 5Hz, and the pulse width was set to 10µs so that the inductor core does not saturate.

7.1 Veroboard

For simplicity reasons, it was decided that the converter and driver was to be built on a veroboard. The veroboard is a pre-made circuit board with copper tracks on one side. Front and backside of the converter on the veroboard is depicted in Appendix B1.

The benefit of this approach is practicality. It is relatively fast to make design changes, replace components and other alterations in the circuit. The downside of using a veroboard is that, because of the voltage and current limitations of the board, wires must be used to couple the components, which increases parasitic inductance in the circuit. Difficulties with the gate driver IC also occur. This is a small surface mount device (SMD), which cannot be placed on this board. A small PCB was created to overcome this issue. This allows the gate driver to be soldered on this board and connected to the rest of the circuit through connector pins. However, this connection must again be done through wires, which have a negative influence on the parasitic inductance in the gate current path. To make it as optimal as possible, the return wire was twisted around the gate wire.

7.2 PCB Layout

It was decided, in an effort to obtain better results, to design a PCB layout of the converter including gate driver path. The layout was designed in EAGLE v7.5. EAGLE is a design software from CadSoft and stands for Easy Applicable Graphical Layout Editor. The board layout is found in Appendix B2. The benefit of the PCB layout is the elimination of wires between components, which include significantly more inductance than a PCB copper track. It also enables a more compact converter, shortening the distance between the circuit components.

7.3 Second PCB layout

The first PCB layout was made for convenience concerning changing the gate driver. This caused a long gate loop. It was also made one-sided for production convenience. This unbaled the gate ground wire from returning underneath the MOSFET gate lead. These shortcuts in design caused a significant parasitic inductance in the gate loop, which caused ringing on the Miller plateau and restricted the switching speed.

The ground return from the MOSFET source was not ideal. Long copper leads placed around and along the positive lead will have significant parasitic inductance.

These two issues with the layout restricted the gate resistor to about 20Ω, which restricts the turn-on and turn-off times of the MOSFET. A new layout was designed, trying to minimize the parasitic inductance in the PCB, and consequently allow for higher switching speed. The new layout also use SMD components instead of through-hole components in the gate driver circuit. The EAGLE layout and pictures of the PCB layout is found in Appendix B3.

7.4 Low frequency short pulse test

All three circuits are tested under the same conditions. The voltage is set to 100V and the load is 94,5Ω. The function generator provides a 5V pulse at low frequency with a 10µs pulse width. The low duty cycle makes the output equal to the input. The gate voltage is set at 16V and the gate resistance is 22Ω.

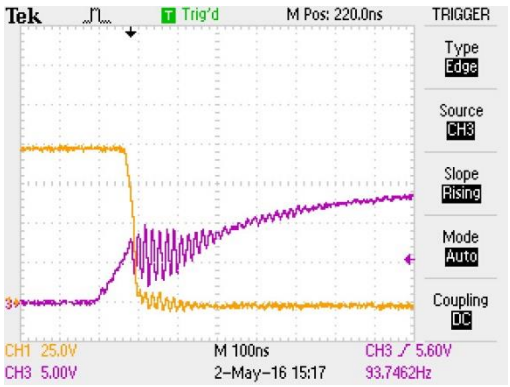


Figure 34: Veroboard LF test turn-on.

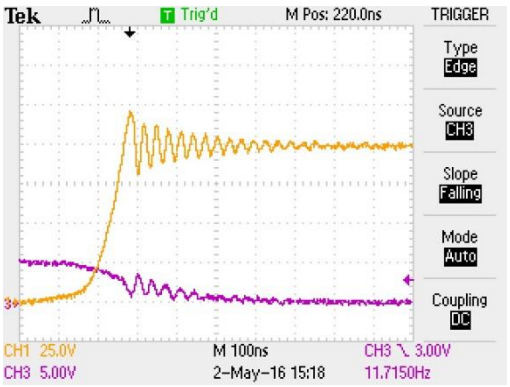


Figure 35: Veroboard LF test turn-off.

Figure 34 and Figure 35 shows the drain-source voltage (yellow) and gate-source voltage (purple), at turn-on and turn-off respectively. At turn-on, the voltage drops from 100V to 0V in 20ns. There is ringing on the gate voltage that is 8Vpk-pk at its largest. This ringing also causes ringing on the drain-source voltage. At turn-off, the drain-source voltage increases from 0V to 100V in 100ns. There is a 25% overshoot and a 40MHz ringing damping out in approximately 300 ns.

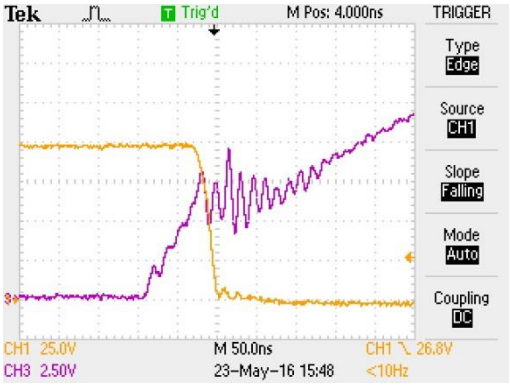


Figure 36: First PCB LF test turn-on.

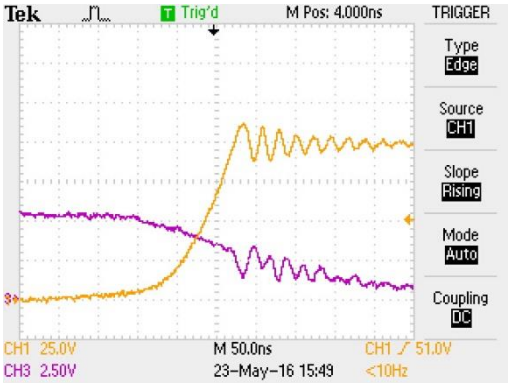


Figure 37: First PCB LF test turn-off.

Figure 36 and Figure 37 shows the turn-on and turn-off waveforms for drain-source voltage and gate-source voltage in the first PCB design. The ringing on the gate voltage is now 5Vpk-pk at its worst, otherwise around 3V. The corresponding ringing in the drain-source voltage at turn-

on is significantly reduced. The rise time at turn-off is similar to the previous case. However, the overshoot is reduced to 10%. The ringing is now at 60MHz, damping out in approximately 150 ns.

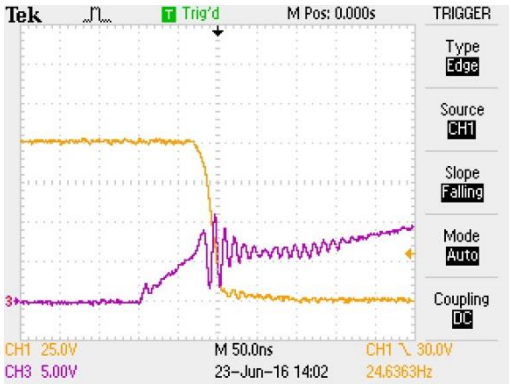


Figure 38: Improved PCB LF test turn-on.

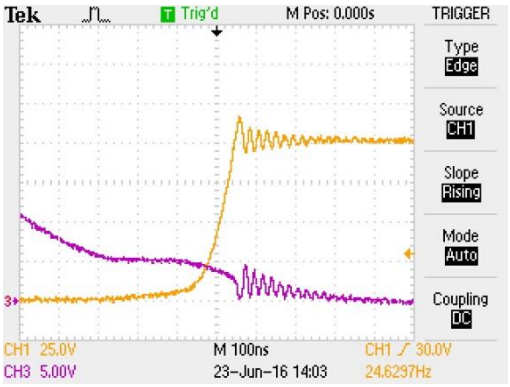


Figure 39: Improved PCB LF test turn-off.

Figure 38 and Figure 39 shows the turn-on and turn-off waveforms for drain-source voltage and gate-source voltage in the final PCB design. The drain-source voltage waveforms are similar to those of the first PCB design, with similar overshoot at turn-off and damping of the oscillations. The gate-source voltage however, is not equal. As the voltage reaches the Miller plateau, two oscillations, larger than those in the first PCB occur.

The gate voltage for the two PCB designs is also measured with a passive probe to compare with the measurements made with the differential probe. The gate voltage waveform for the first PCB is shown in Figure 40 and the waveform for the final PCB is shown in Figure 41.

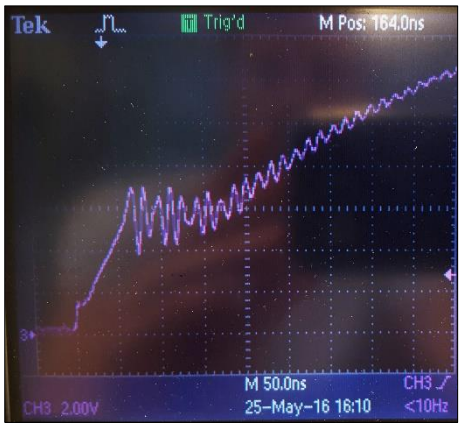


Figure 40: First PCB gate voltage at turn-on measured with passive probe.

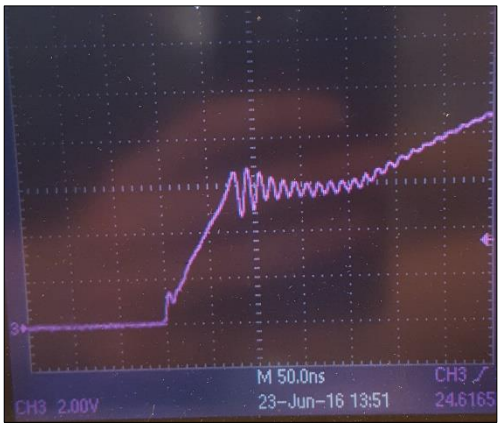


Figure 41: Final PCB gate voltage at turn-off measured with passive probe.

The passive probe measurements are performed simultaneously with the differential probe. This is to make sure the loading from the probe in the circuit is equal. Pictures of the passive probe measuring in the circuit is found in Appendix C.

These measurements show a different wave progression than the differential probe measurements. The most noticeable difference is the removal of the large spikes at the Miller plateau. With the differential probe, the high frequency oscillations seem to follow a lower frequency sinusoid, which is not present in the passive probe measurements.

7.5 Boost converter test

When operating the boost converter the goal is to map the efficiency of the converter at different loads, input voltages. The nominal converter ratings are listed in Table 15.

Table 15: Boost converter ratings.

Parameter	**Rating**
Input voltage V_{in}	230V
Input current, I_{in}	15,2A
Duty cycle, d	0,35
Output voltage, V_o	350V
Output current, I_o	10A
Output power, P_o	3,5kW

During testing, the switching frequency is set at 100 kHz with a 500µH boost inductor. According to Equation 5, this will cause a 2A input current ripple. At the rated input voltage and duty cycle, the turn-on and turn-off current will be approximately 14A and 16A respectively.

The converter is tested at rated power with the two MOSFETS and with both gate drivers, at different gate voltages and gate resistances.

Drain-source voltage and current through the MOSFET are the waveforms of interest during these tests. The voltage is measured with the differential probes directly on the MOSFET drain and source legs at 1/500 attenuation, and attenuated back 500 on the scope. The current is measured with the Rogowski coil placed around the source leg. Drain-source voltage is measured on the scopes channel 1, and is yellow, source current is measured the scope channel 2, and is turquoise/blue. Voltage is scaled at 100V per division and current is scaled at 200mV per division. With the Rogowski coils sensitivity of 50mV/A, this implies that the current is scaled at 4A per division. The time axis is set at 25 ns per division.

Each section of measurements include a table summarizing the most important factors for each case. This include delay times, voltage rise- and fall-times, current rise- and fall-times and overshoot. The delay times are measured from the gate current start flowing until the MOSFET

start conducting or start blocking. Rise-times are measured approximately from 10% to 90% of total current or voltage, and fall-times are measured from approximately 90% to 10% of total current or voltage.

Since the current through the MOSFET is measured through the source leg, gate current is also present in the measurements. This is present as an increase in current at turn-on, before the drain-source current start increasing, and as a decrease in current at turn-off, before the drain-source current start to decrease.

7.5.1 SiC with UCC27531D gate driver and 20V gate voltage

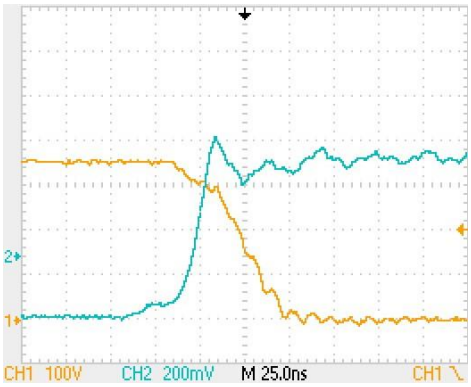


Figure 42: SiC Turn-on. UCC27531D gate driver. Rg=11Ω. Vgs=20V.

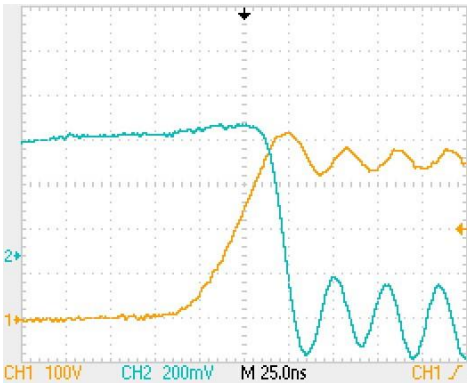


Figure 43: SiC turn-off. UCC27531D gate driver. Rg=11Ω. Vgs=20V.

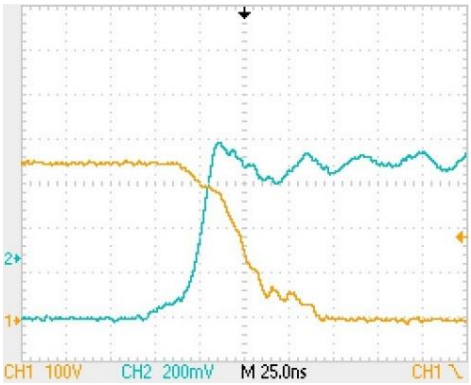


Figure 44: SiC turn-on. UCC27531D gate driver. Rg=7,5Ω. Vgs=20V.

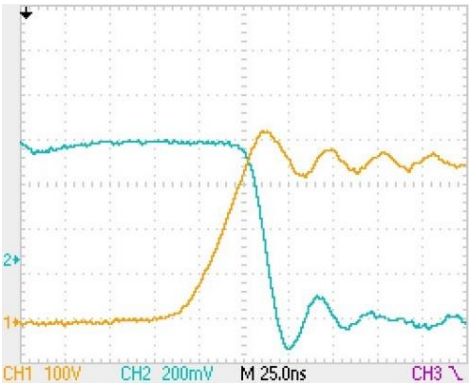


Figure 45: SiC turn-off. UCC27531D gate driver. Rg=7,5Ω. Vgs=20V.

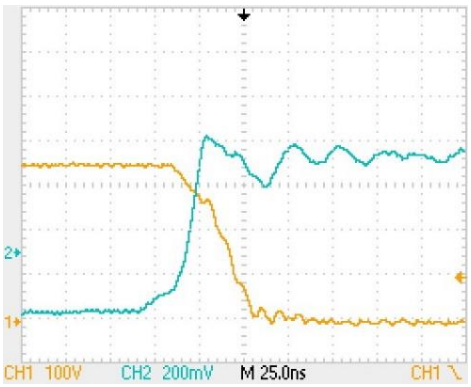


Figure 46: SiC turn-on. UCC27531D gate driver. Rg=5Ω. Vgs=20V.

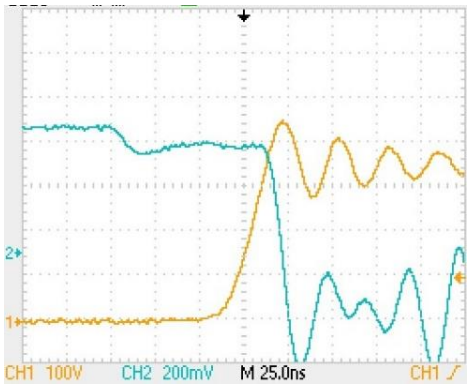


Figure 47: SiC turn-off. UCC27531D gate driver. Rg=5Ω. Vgs=20V.

Table 16: Measurements from SiC MOSFET switching transients with UCC27531D gate driver. Vgs=20V.

Period	Measurement	22||22 Ω	15||15 Ω	10||10 Ω
Turn-on	**Delay time**	20 ns	20 ns	20 ns
	Current rise time	15 ns	15 ns	15 ns
	Current overshoot	2 A	2 A	2 A
	Voltage fall time	50 ns	40 ns	35 ns
Turn-off	**Delay time**	110 ns	85 ns	50 ns
	Voltage rise time	40 ns	30 ns	22 ns
	Voltage overshoot	50 V	70 V	100 V
	Current fall time	15 ns	15 ns	10 ns

Figure 42 to Figure 47 shows the switching transients for SCT90N65G2V SiC MOSFET at 20V gate voltage, and at different gate resistance. Table 16 summarizes the most important measurements from the figures.

The first noticeable thing from these tests is the current response at turn-on, which are identical in all three cases. This be either that the gate resistance have no influence on the current at turn-on, or that the gate driver is not capable of providing more current than it does at 11Ω gate resistance so that reducing the gate resistance have no effect.

The gate resistance have some effect on the voltage fall-time, reducing it gradually from 50 ns to 35 ns at 11Ω and 5Ω gate resistance respectively.

At turn-off, the gate resistance have a more evident influence. The delay-time show a near linear relationship with gate resistance, significantly reducing with reducing resistance. The same applies to the voltage rise-time. As the voltage rise-time is reduced, the voltage overshoot increases.

The current fall-time is less influenced by the gate resistance. There are however, a slight reduction in this as well with reduced resistance. While the fall-time at 11Ω and 7.5Ω are identical, the fall-time at 5Ω is 5 ns shorter.

7.5.2 Si with UCC27531D gate driver and 11Ω gate resistance

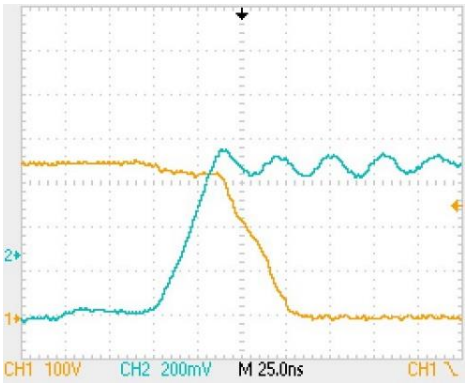


Figure 48: Si turn-on. UCC27531D gate driver. Rg=11Ω. Vgs=12V.

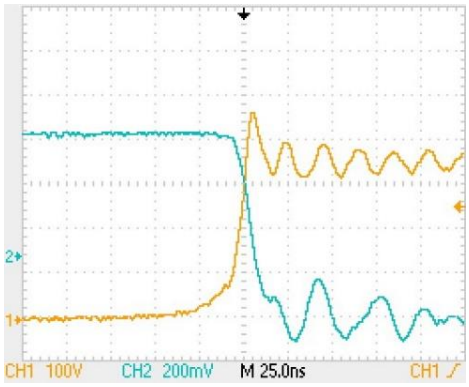


Figure 49: Si turn-off. UCC27531D gate driver. Rg=11Ω. Vgs=12V.

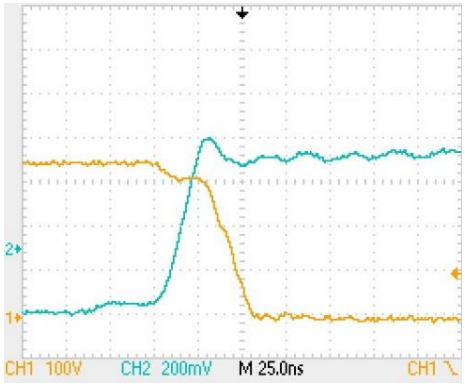


Figure 50: Si turn-on. UCC27531D gate driver. Rg=11Ω. Vgs=15V.

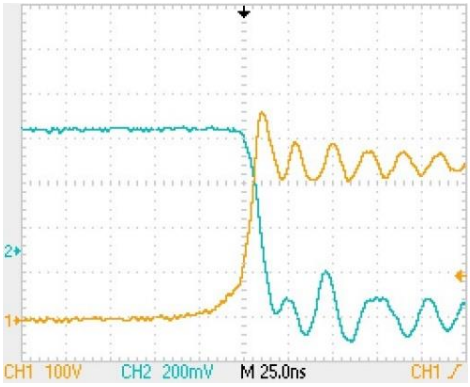


Figure 51: Si turn-off. UCC27531D gate driver. Rg=11Ω. Vgs=15V.

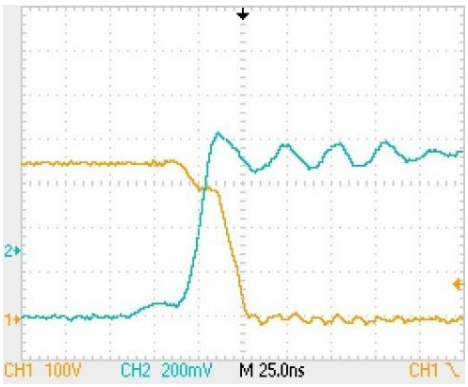


Figure 52: Si turn-on. UCC27531D gate driver. Rg=11Ω. Vgs=20V.

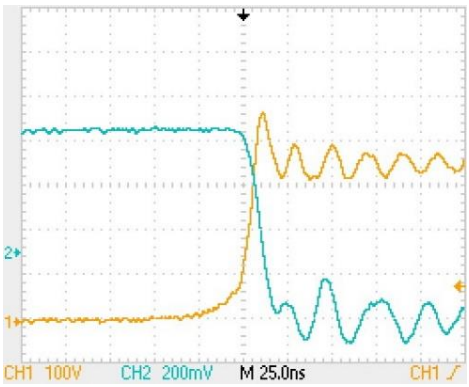


Figure 53: Si turn-off. UCC27531D gate driver. Rg=11Ω. Vgs=20V.

Table 17: Measurements from Si MOSFET switching transients with UCC27531D gate driver. Rg=11Ω.

Period	Measurement	12 V	15 V	20 V
Turn-on	**Delay time**	55 ns	40 ns	25 ns
	Current rise time	27 ns	18 ns	15 ns
	Current overshoot	2 A	2,4 A	2,4 A
	Voltage fall time	40 ns	22-30 ns	30 ns (15 280-0)
Turn-off	**Delay time**	N/A	250 ns	300 ns
	Voltage rise time	20 ns	17 ns	15 ns
	Voltage overshoot	110 V	110 V	110 V
	Current fall time	20 ns	15 ns	15 ns

Figure 48 to Figure 53 shows the switching transients for STW62N65M5 Si MOSFET at 11Ω gate resistance, and at different gate voltages, using UCC27531D gate driver. Table 17 summarizes the most important measurements from the figures.

At turn-on, the time from gate signal occur until current start flowing through the MOSFET decreases with increasing gate voltage. At turn-off, this delay time increases with the increasing gate voltage. The rest of the turn-off period is very similar in all three cases, except for the slight decrease in voltage rise-time for the increases gate voltage, and the decrease in current fall-time from 20 ns to 15 ns. The turn-off delay time was not applicable due to

The most significant effect is on the turn-on-period, with a clear reduction in both current rise-time and voltage fall-time.

7.5.3 Si with FAN3224T gate driver and 11Ω gate resistance

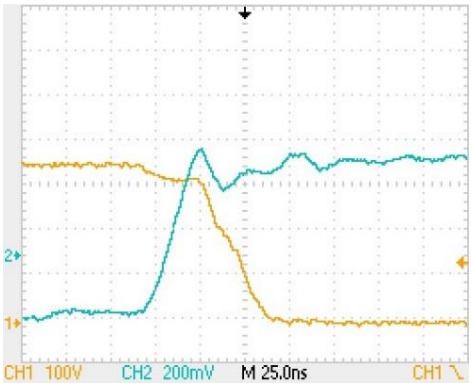


Figure 54: Si turn-on. FAN3224T gate driver. Rg=11Ω. Vgs=12V.

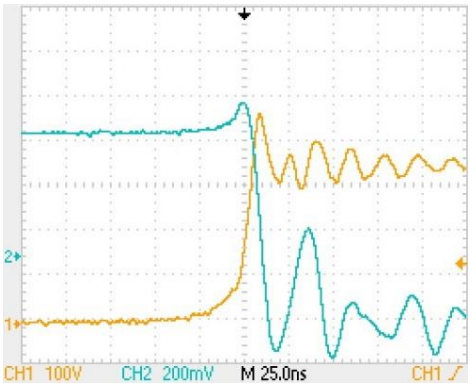


Figure 55. Si turn-off. FAN3224T gate driver. Rg=11Ω. Vgs=12V.

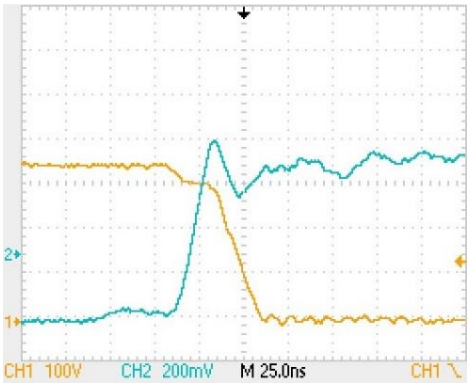


Figure 56: Si turn-on. FAN3224T gate driver. Rg=11Ω. Vgs=15V.

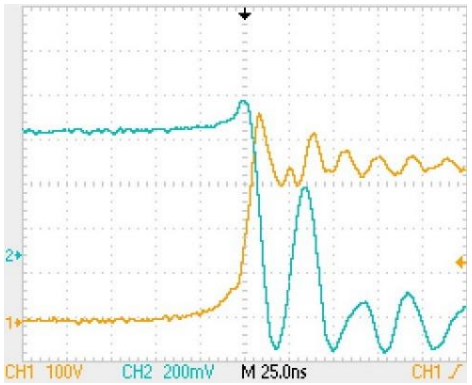


Figure 57: Si turn-off. FAN3224T gate driver. Rg=11Ω. Vgs=15V.

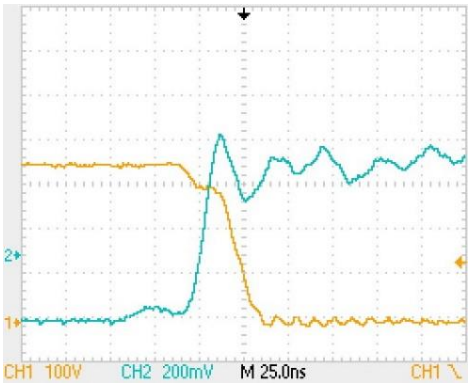


Figure 58: Si turn-on. FAN3224T gate driver. Rg=11Ω. Vgs=17,5V.

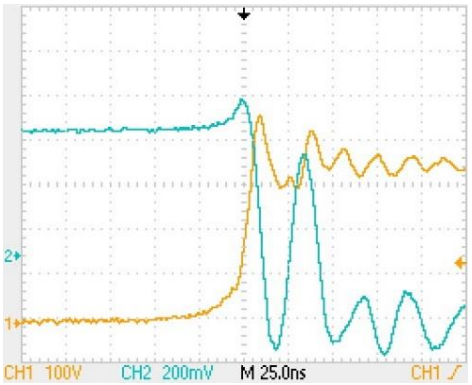


Figure 59: Si turn-off. FAN3224T gate driver. Rg=11Ω 17,5V.

Table 18: Measurements from Si MOSFET switching transients with FAN3224T gate driver. Rg=11Ω.

Period	Measurement	12 V	15 V	17,5 V
Turn-on	**Delay time**	58 ns	45 ns	35 ns
	Current rise time	25 ns	17 ns	15 ns
	Current overshoot	1,2 A	2,4 A	2,8 A
	Voltage fall time	35/65 ns	28/53ns	20/35 ns
Turn-off	**Delay time**	240 ns	275 ns	300 ns
	Voltage rise time	25/10 ns	22/10 ns	22/10 ns
	Voltage overshoot	110 V	110 V	110 V
	Current fall time	11 ns	11 ns	11 ns

Figure 54 to Figure 59 shows the switching transients for STW62N65M5 Si MOSFET at 11Ω gate resistance, and at different gate voltages, using FAN3224T gate driver. Table 18 summarizes the most important measurements from the figures.

The turn-on switching periods are quite similar to those of the case with the UCC27531D gate driver. So is the voltage rise time and overshoot at turn-off. The current at turn-off however, reaches zero faster. It also follows with a large oscillation that increases in size with higher gate voltage, while the current fall-time remains the same.

7.5.4 SiC with UCC27531D gate driver and 25V gate voltage

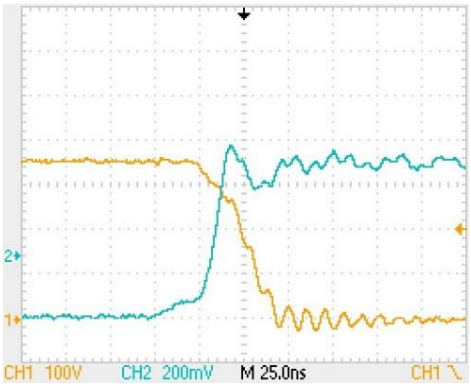


Figure 60: SiC turn-on. UCC27531D gate driver. Rg=11Ω. Vgs=25V.

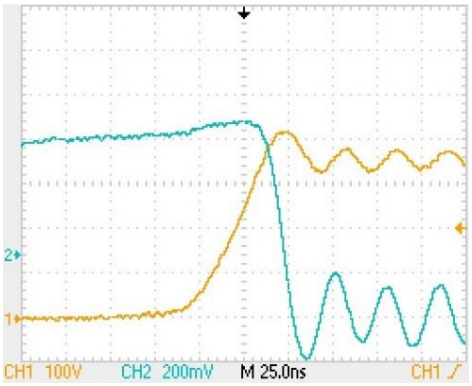


Figure 61: SiC turn-off. UCC27531D gate driver. Rg=11Ω. Vgs=25V.

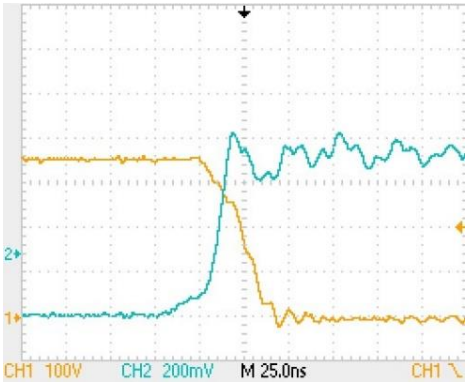


Figure 62: SiC turn-on. UCC27531D gate driver. Rg=7,5Ω. Vgs=25V.

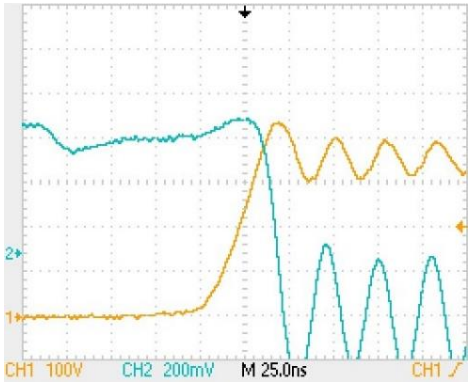


Figure 63: SiC turn-off. UCC27531D gate driver. Rg=7,5Ω. Vgs=25V.

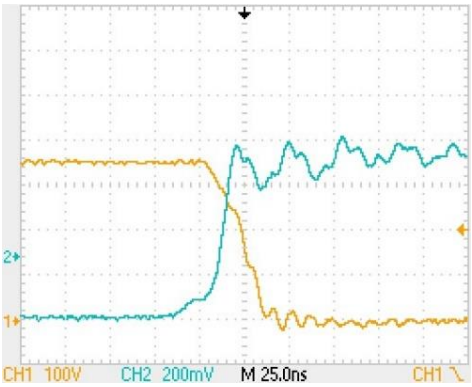


Figure 64: SiC turn-on. UCC27531D gate driver. Rg=5Ω. Vgs=25V.

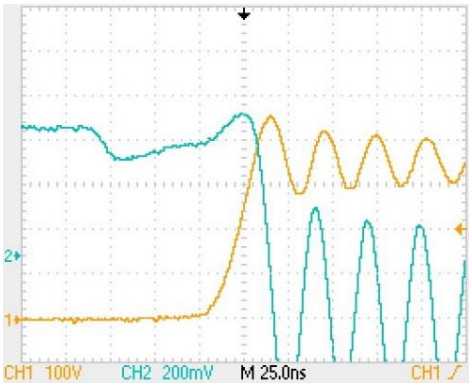


Figure 65: SiC turn-off. UCC27531D gate driver. Rg=5Ω. Vgs=25V.

Table 19: Measurements from SiC MOSFET switching transients with UCC27531D gate driver. Vgs=25V.

Period	Measurement	11 Ω	7.5 Ω	5 Ω
Turn-on	**Delay time**	30 ns	25 ns	18 ns
	Current rise time	15 ns	15 ns	15 ns
	Current overshoot	1,5 A	2,4 A	1,5 A
	Voltage fall time	35 ns	30 ns	25 ns
Turn-off	**Delay time**	130 ns	90 ns	60 ns
	Voltage rise time	40 ns	30 ns	20 ns
	Voltage overshoot	65 V	80 V	100 V
	Current fall time	15 ns	12 ns	10 ns

Figure 60 to Figure 65 shows the switching transients for SCT90N65G2V SiC MOSFET at 25V gate voltage, and at different gate resistance. Table 19 summarizes the most important measurements from the figures.

At turn-on, the increased gate voltage have the most effect on the voltage fall-time, increasing the charge into the MOSFET at the Miller plateau.

At turn-off, the delay time is increased due to a higher voltage, and thus longer time is needed to discharge the intrinsic capacitors to the Miller plateau. The current have much higher oscillations compared to the 20V gate voltage case, without any significant decrease in neither current fall-time nor voltage rise-time.

7.5.5 SiC with UCC27531D gate driver and 0Ω gate resistance

The SiC MOSFET is tested with zero gate resistance. Now, only the internal resistance of the gate driver acts in the gate circuit. This should assure maximum charge the gate driver can deliver to the MOSFET gate. Figure 66 and Figure 67 shoes the turn-on and turn-off period respectively, with 20V gate voltage.

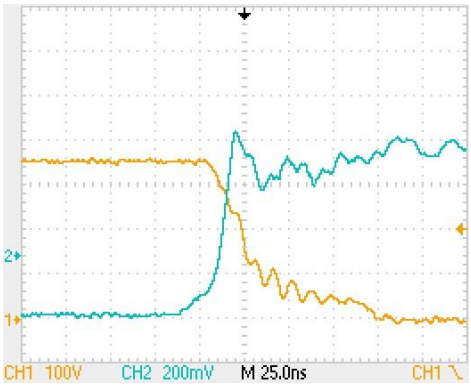


Figure 66: SiC turn-on. UCC27531D gate driver. Rg=0Ω. Vgs=20V.

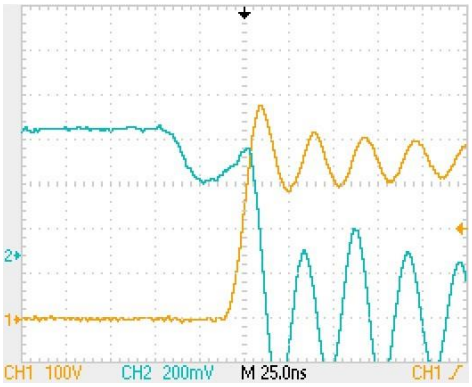


Figure 67: SiC turn-off. UCC27531D gate driver. Rg=0Ω. Vgs=20V.

At turn-on, the current rise-time is approximately equal as with gate resistance present. The voltage starts falling, reaching 100V in approximately 20 ns. However, at this point, a drastic reduction in dv/dt happens, and it takes about 65 ns for the voltage to drop completely from 100V to 0V. This is an unexpected event, as lower gate resistance should allow more charge into the MOSFET. It seems that, with no gate resistance, the MOSFET is more prone to the capacitive change that happens with lower drain-source voltage, and the Miller plateau lengthens. Increasing the gate voltage should ensure more current being inserted into the MOSFET gate over the entire switching period, and consequently shorten the length of the Miller plateau. Figure 68 shows the turn-on period with 25V gate voltage.

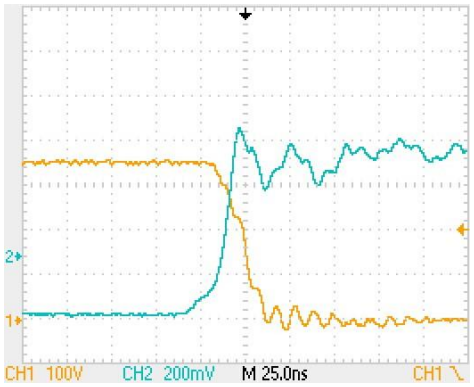


Figure 68: SiC turn-on. UCC27531D gate driver. Rg=0Ω. Vgs=25V.

The increased gate voltage ensures a shorter Miller plateau, and the drain-source voltage show a more linear drop from 350V to 0V. The voltage fall-time is just above 20 ns. The current transient remains unchanged with the increased gate voltage.

7.5.6 Increased power with SiC, UCC27531D gate driver and 0Ω gate resistance

The SiC MOSFET was tested at higher power. Input voltage was set to 260V and input current 17A. This gives an input power of approximately 4,4kW. The output voltage is 400V.

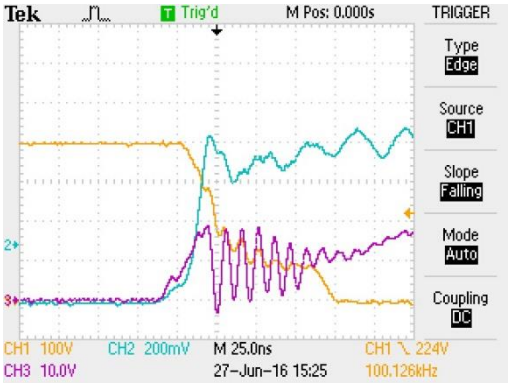


Figure 69: SiC turn-on at 4,4kW. UCC27531D gate driver. Rg=0Ω. Vgs=20V

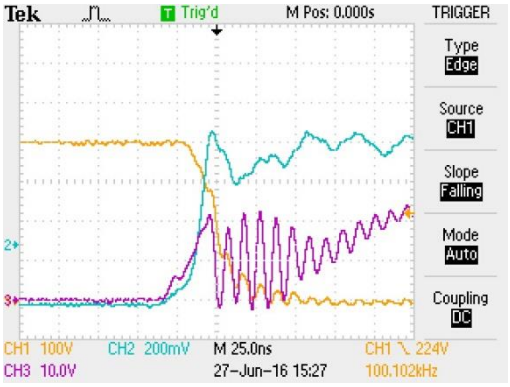


Figure 70: SiC turn-on at 4,4kW. UCC27531D gate driver. Rg=0Ω. Vgs=25V

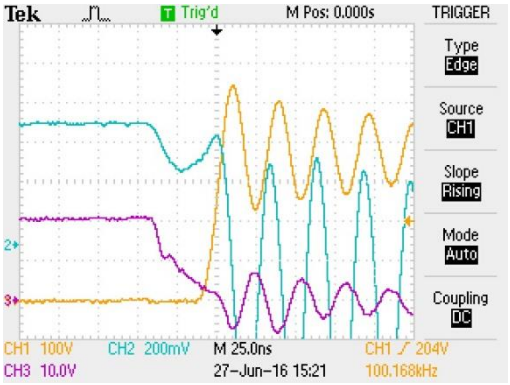


Figure 71: SiC turn-off at 4kW. UCC27531D gate driver. Rg=0Ω. Vgs=20V.

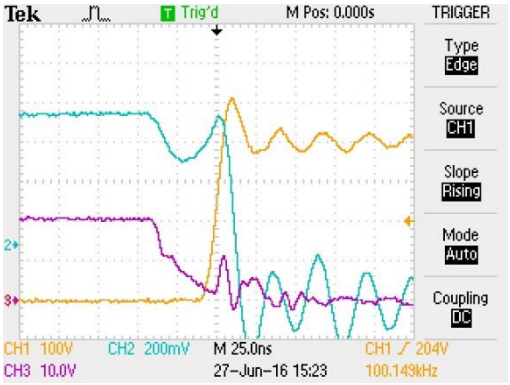


Figure 72: SiC turn-off at 4,4kW. UCC27531D gate driver. Rg=0Ω. Vgs=20V.

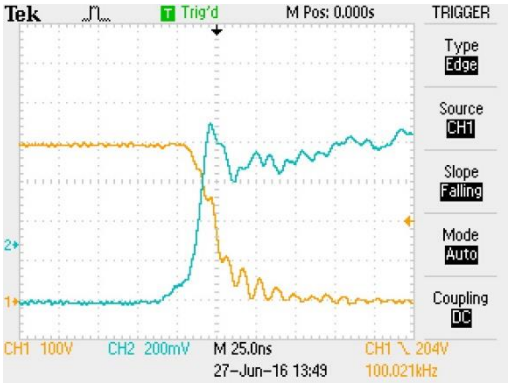


Figure 73: SiC turn-on at 4,4kW. UCC27531D gate driver. Rg=0Ω. Vgs=25V

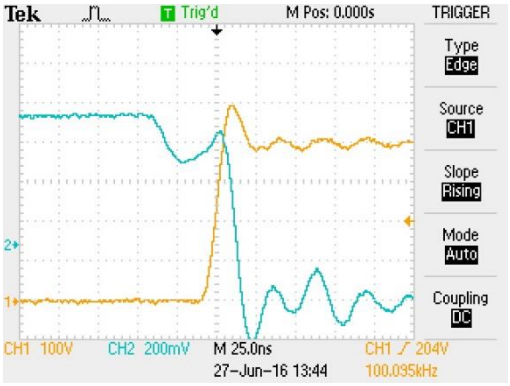


Figure 74: SiC turn-off at 4,4kW. UCC27531D gate driver. Rg=0Ω. Vgs=20V.

Table 20: SiC turn-on. UCC27531D gate driver. Vgs=25V

Period	**Measurement**	**0 Ω**
Turn-on	**Delay time**	17 ns
	Current rise time	10 ns
	Current overshoot	2 A
	Voltage fall time	25 ns

Table 21: SiC turn-off. UCC27531D gate driver. Vgs=20V.

Period	**Measurement**	**0 Ω**
Turn-off	**Delay time**	30 ns
	Voltage rise time	10 ns
	Voltage overshoot	90 V
	Current fall time	10 ns

Figure 69 show the turn on waveforms for drain-source current (blue), drain-source voltage (yellow) and gate-source voltage (purple), at 20V gate voltage. When the drain-source voltage reaches 100V, it flattens until the end of the Miller plateau. Figure 70 shows the same waveforms, with a 25V gate voltage. Because of more charge inserted into the MOSFET, the Miller plateau is shorter, and the drain-source voltage drops faster. The voltage is also has a smoother curve as it drops to zero, it does not have the same plateau as in Figure 69.

An interesting observation is the change in behavior when the power is increased. Figure 71 shows the waveforms 4kW. The input voltage is 250V and the current is 16A. Up to this power, ripple in both voltage and current increases. At this point, the voltage overshoots 170V and the current oscillates with over 10A peaks. Above this point, the rippling decreases. When the power is increased to 4,4 kW in Figure 72, the voltage overshoot is 90V and the current ripple peaks at 4A. The oscillations also damp out considerably faster. The improved turn-off is also visible in the gate voltage waveforms. The gate voltage at 4,4 kW is smoother and with substantially less ringing than the gate voltage at 4 kW.

Figure 73 and Figure 74 shows the best turn-on and turn-off obtained at 4,4kW and 0Ω gate resistance. Table 20 and Table 21 summarizes the measurements. The turn-on is similar to that of 3,5 kW. Turn-off however, show a significant improvement. Less resistance allow for a faster discharge of the intrinsic capacitors. The delay time is now 30 ns, both voltage rise-time and current fall-time approximately 10 ns, and the voltage overshoot 22,5%.

7.6 Switching loss

The energy loss is calculated from the best turn-on and turn-off switching progressions of the MOSFETs. There are many uncertainties when analyzing high frequency switching behavior, which makes coming to a definite conclusion challenging. In an effort to account for these uncertainties, the switching energy loss for the two MOSFETs was calculated with three different approaches in order to obtain a spectrum of possible loss. The loss was calculated purely based on the switching waveforms captured on the oscilloscope, by time shifting the waveforms to account for different time delays in the active probes, and by using the voltage and current fall and rise times obtained, in the theoretical switching progression of inductive switching.

7.6.1 Oscilloscope energy loss

The Si MOSFET turn-off current ramps down at a lower voltage than in the SiC MOSFET. Ignoring the initial slow start of voltage rise and interpolating the high dv/dt down, results in a total turn-off switching period of about 20 ns. The peak instantaneous power occur at 300V and

12A.The total turn-on switching period for the Si MOSFET is 40 ns. The peak instantaneous power occur at 290V and 9A.

The total turn-off switching period of the SiC MOSFET is 20 ns. The peak instantaneous power occur at 350V and 14A.The total turn-on switching period of the SiC MOSFET is 30 ns. The peak instantaneous power occur at 250V and 10A.This results in a total switching energy loss in Table 22.

Table 22: Switching energy loss based directly on oscilloscope readout.

Energy loss	**SiC**	**Si**
Eon	37,5 µJ	52,2 µJ
Eoff	49 µJ	36 µJ
Esw	86,5 µJ	88,2 µJ

7.6.2 Time-shifted waveforms energy loss

Since the measurement probes are active, some time delay is expected on the scope, and these time delays are not necessarily equal for the current probe and voltage probe. If the current and voltage waveforms are adjusted so that the voltage start falling when the current reaches its rated turn-on value, the voltage is shifted 5 ns back. This means that the turn-on period becomes 5 ns shorter and the turn-on period 5 ns longer. The peak turn-on power now is at 290V and 14A, and the peak turn-off power at 400V and 14A for the Si MOSFET. For the SiC MOSFET, the peak turn-on power becomes at 230V and 9A, the peak turn-off power occur at 400V and 16A. This results in the energy loss in Table 23.

Table 23: Switching energy loss from oscilloscope with adjusted time delay.

Energy loss	**SiC**	**Si**
Eon	26 µJ	71 µJ
Eoff	80 µJ	70 µJ
Esw	106 µJ	141 µJ

7.6.3 Loss calculated based on theoretical inductive switching.

Measurement errors and parasitic elements unique for this specific circuit might cause behavior that might not happen in other circuits. Therefore, the switching energy loss is calculated based on the theoretical switching progression of inductive switching as a worst-case scenario. This means that, at turn-on, the voltage does not start falling until the current reaches rated turn-on value, and at turn-off, the current does not start falling until the voltage reaches rated value. The fastest acceptable switching times obtained is used and is listed in along with the energy loss in Table 24.

Table 24: Fastest switching times and energy loss based on theoretical inductive switching.

Parameter	**SiC**	**Si**
Current rise-time, t_{rc}	10 ns	15 ns
Voltage fall-time, t_{fv}	25 ns	30 ns
Voltage rise-time, t_{rv}	10 ns	15 ns
Current fall-time, t_{fc}	10 ns	15 ns
Turn-on energy loss, Eon	87 µJ	112 µJ
Turn-off energy loss, Eoff	51 µJ	85,5 µJ
Total switching energy loss, Esw	138 µJ	197,5 µJ

7.6.4 Power loss

Based on the energy losses, the power loss is calculated. Figure 75 and Figure 76 shows the switching loss for the SiC and Si MOSFETs respectively, from 50 kHz to 300 kHz switching frequency.

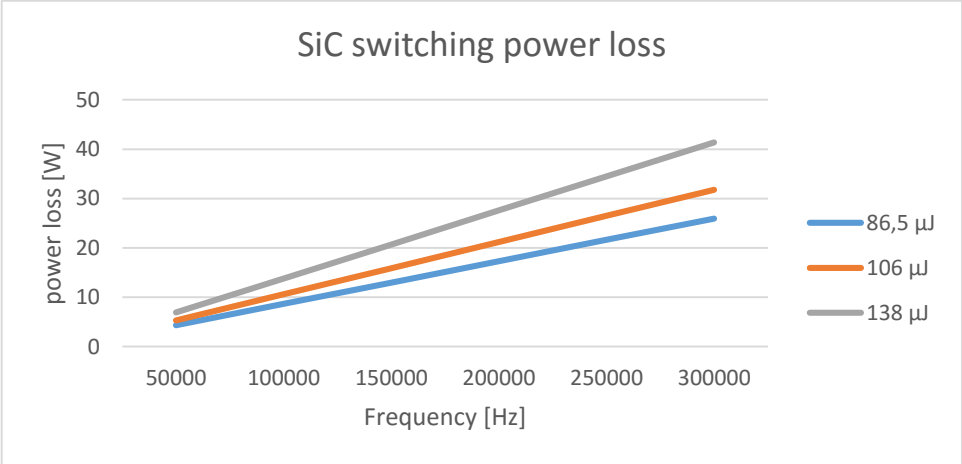


Figure 75: Switching loss for SCT90N65G2C SiC MOSFET.

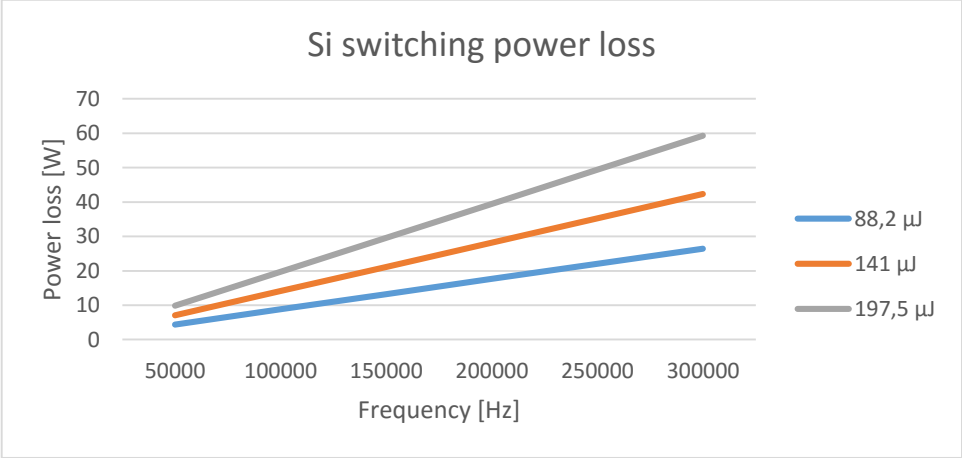


Figure 76: Switching loss for STW62N65M5 Si MOSFET.

Setting a total power loss in the MOSFET at 25W, the maximum switching frequency can be calculated. First, the conduction loss must be subtracted. For the Si MOSFET this was calculated to be between 3,4 and 7,5 W. assuming the operating temperature will be in the upper bounds, the conduction loss is set at 7,5W. The conduction loss for the SiC MOSFET is less temperature dependent and is 2,2W. The switching loss limit is thus 18W for the Si MOSFET and 23W for the SiC MOSFET. Figure 77 and Figure 78 shows the total power loss for the SiC

and Si MOSFET respectively with the 25W power limit, from 50 kHz to 300 kHz switching frequency.

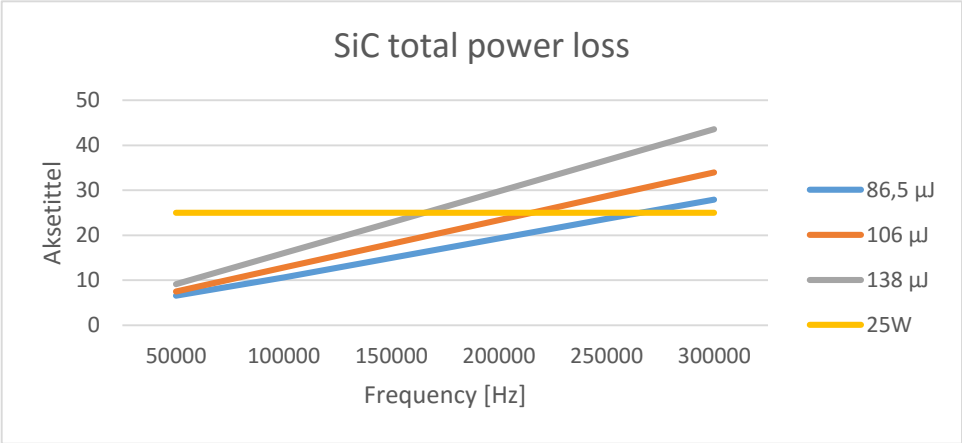


Figure 77: Total power loss for SCT90N65G2V SiC MOSFET.

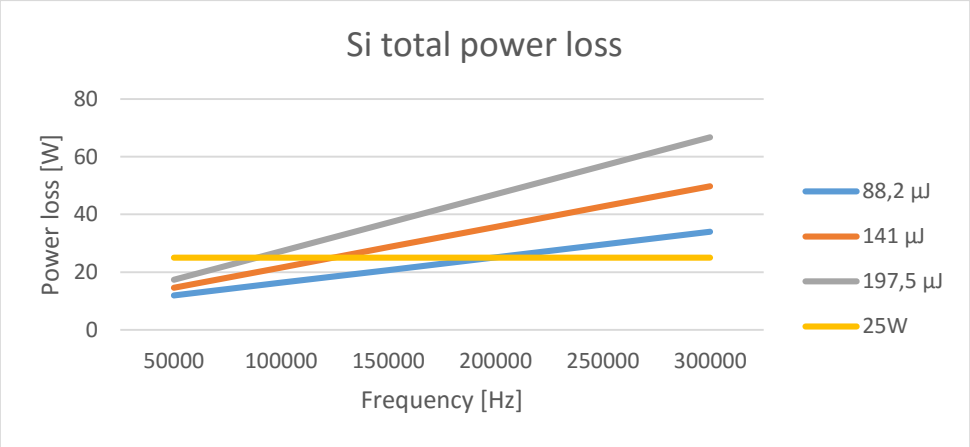


Figure 78: Total power loss for STW62N65M5 Si MOSFET.

8 Discussion

The paradox when doing circuit measurements is the inevitable extra loading imposed by the probes, which changes the behavior of the circuit. This becomes even more important when dealing with fast, high frequency switching, where every nanosecond counts. Another possible source of measurement error is the probe bandwidths. The differential probes have a 50 MHz bandwidth and the Rogowski coil have a bandwidth of 30 MHz. Ringing etc. above this frequency is not necessarily shown on the scope as it is in the circuit. Most oscillations in the measurements are around and above this frequency, and the waveforms can therefore not be trusted completely.

8.1 Circuit Layout

The three different circuit configurations all showed different switching behavior, emphasizing the importance of a good layout mitigating parasitic elements. The first layout used wires for all connections and through-hole components. This introduced too much parasitic elements in the circuit for acceptable switching at required frequency and power. A PCB layout was then designed to improve switching. Making the circuit on a PCB removes all wire connections and allows for shorter conduction paths. This reduces parasitic elements in the circuit and significantly improved switching behavior. However, the PCB was made to reuse the components from the first circuit. This caused an unnecessary long gate path and through-hole components in the gate circuitry, which have more parasitic elements than SMD components. Because of this, a third circuit layout was created. This layout was made two-sided, allowing the gate circuit return lead to return to the gate driver directly underneath the path from the gate driver to the MOSFET gate. The gate driver circuit was also made more compact, shortening all tracks. Instead of through-hole components, all components in the gate circuit was SMDs. These measures reduces both parasitic inductance and capacitance in the gate drive circuit, which was observable with passive probe measurements.

Despite several improvements, the layout is not optimal. Resources and capabilities restricted the layout. Parasitic inductance and capacitance is unavoidable, but can be significantly reduced by an optimal layout. Parasitic inductance influences the overshoot and ringing. Optimally, the lead and the corresponding return lead should be directly on top of each other on a two-sided PCB. This was not possible in this case, except for in the gate circuitry.

8.2 MOSFET switching

Overall from the tests, it can be seen that changing the gate resistance have a significant influence on the turn-off period, while the turn-on period is less influenced. Changing the gate voltage influence the turn-on period, while the turn-off period remain nearly unchanged, with the exception of delay times. This can partly be explained by that, at turn-off, the MOSFET stops conducting when the intrinsic capacitors are completely discharged. These are discharged through an RC circuitry, and a larger resistance increases the RC time constant. At turn-on, the same capacitances must be charged for the MOSFET to conduct. Increasing the gate voltage pushes more charge into the MOSFET gate, shortening the length of the Miller plateau. However, reducing the gate resistance should reduce the RC time constant and allow for faster turn-on. A possible reason that this is not considerably evident in the tests is explained through Figure 79.

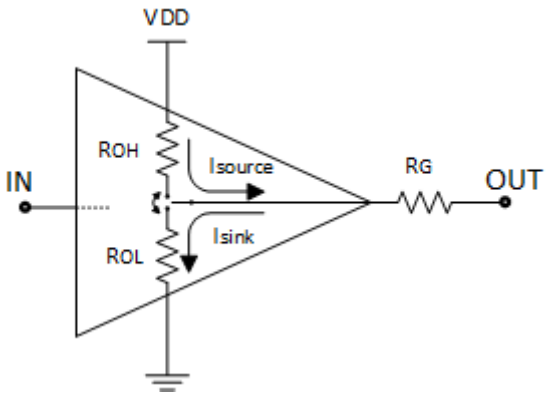


Figure 79: Conceptual sketch of a gate driver.

Figure 79 show a conceptual sketch of a gate driver. The gate driver IC have internal pull-up and pull-down resistors. These influence the switching performance. The pull-up resistor, ROH, is usually much greater than the pull-down resistor, ROL. When the switch turns on, the gate resistance, RG, and ROH forms a series resistance, effectively restricting the turn-on current, or source current. When the switch turns off, RG forms a series resistance with ROL.

In the datasheet for the UCC27531D gate driver, the pull-up resistance is listed as 12Ω and the pull-down resistance as 0,65Ω. A change in gate resistance thus have a much more significant impact on the total resistance at turn-off, than at turn-on. Another contributing factor is the source and sink current capability of this gate driver. The peak source current is given as 2,5A

and the peak source current as 5A. It is therefore a good possibility that the gate driver is not able to provide more current at turn-on than it does at 11Ω gate resistance.

Common for the Si and SiC MOSFET turn-on voltage is that it can be divided into two distinct periods, first one drop, and then another. The difference between the two is that the Si MOSFET has a small voltage drop, and then stays at this voltage until the current rise is complete, before it decreases to zero. The SiC MOSFET voltage does not have the same plateau as the Si MOSFET. The voltage decreases the entire time, but the dv/dt while the current rises is smaller than the dv/dt after the current rise is completed. The current rise progression is similar for the two MOSFETs.

The turn-off voltage progression differ for the Si and SiC MOSFET. The SiC MOSFET voltage is completely linear the entire rising period. The Si MOSFET voltage has a more modest start. It has a curved transition as it rises from zero, before the dv/dt increases drastically.

The sudden change in switching performance as the power increased to 4,4kW is difficult to comprehend. One possible explanation might lie in the intrinsic capacitances. These capacitances are, as previously stated, dependent on drain-source voltage. It could be that as the voltage increases, the capacitance changes enough to leave a capacitance area, which could be in resonance with inductive elements in the circuit. However, this is difficult to determine, especially without having the datasheet capacitance curves like the ones in Figure 20 for this MOSFET.

8.3 MOSFET power loss

The MOSFET losses are calculated from the fastest acceptable switching obtained. For the Si MOSFET this is at 20V gate voltage and 11Ω gate resistance, using the UCC27531D gate driver. The switching speed could possibly be increased by reducing the gate resistance, but that would affect the voltage overshoot negatively. At this condition, the overshoot is 31%, which is already very high. It was therefore decided not to decrease the gate resistance. For the SiC MOSFET, the fastest acceptable switching was obtained with the UCC27531D gate driver and no gate resistor. The gate voltage was 20V at turn-off, but 25V was needed in order to obtain acceptable turn-on.

Lowest switching loss was found using the oscilloscope waveform readout directly. This resulted in 86,5 µJ energy loss for the SiC MOSFET and 88,2 µJ energy loss for the Si MOSFET. The switching loss with this method is then nearly identical and significantly lower than calculated theoretically. Because the Si MOSFET have higher conduction loss than the SiC MOSFET, the total power loss is higher. An operating temperature of 125 ºC was chosen as a reasonable condition. This results in 7,5W conduction loss in the Si MOSFET and 2,2W in the SiC MOSFET. At the 25W benchmark, this results in a possible switching frequency of 198 kHz for the Si MOSFET and 264 kHz for the SiC MOSFET.

Active probes have a certain time delay before the waveforms are shown on the oscilloscope. Different probes have different time delay, so that the voltage probe and the current probe have the same time delay is highly unlikely. Based on the waveforms, the time offset between the two was set to five nanoseconds. This resulted in 141 µJ energy loss for the Si MOSFET and 106 µJ for the SiC MOSFET. Setting the same conditions as before, this gives a possible switching frequency of 124 kHz for the Si MOSFET and 215 kHz for the SiC MOSFET.

As a worst-case scenario, the voltage and current rise and fall times was used in calculating the switching loss for the theoretical switching progression for inductive switching. This resulted in 197,5 µJ energy loss for the Si MOSFET and 138 µJ energy loss for the SiC MOSFET, by far, the highest switching loss of the three approaches. The same conditions as in the previous calculations gives a possible switching frequency of 89 kHz for the Si MOSFET and 165 kHz for the SiC MOSFET.

The switching loss obtained from the time-skewed waveforms correspond really well compared to the loss calculated in 5.4.2, with the Si MOSFET energy loss 11 µJ lower and the SiC

MOSFET energy loss only 2 µJ lower. The switching loss obtained from the worst-case scenario actually correspond well to the energy loss calculated from the datasheet listed energy loss in 5.4.1. Compared to the calculations, the obtained energy loss differ 9,5 µJ for the Si MOSFET and 15 µJ for the SiC MOSFET. Although, the theoretical losses calculated was based on a 10Ω gate resistor.

The switching losses from these two approaches is also comparable to the difference in energy loss calculated in Chapter 5.4.4. From these approaches, the switching loss in the SiC MOSFET is 0,7 and 0,75 times lower than the Si MOSFET.

Based on this, it is most likely that the optimal switching frequency is between 165 kHz and 215 kHz for the SiC MOSFET. This is however, specific for this circuit, with this specific layout, MOSFET and gate driver. A different layout configuration, MOSFET and gate driver could improve on these results.

9 Conclusion

This thesis has investigated the importance of a good physical circuit for high frequency converter switching, and the switching behavior of a SiC MOSFET compared to a Si MOSFET.

Three different physical circuits was tested, with focus on the gate voltage and drain-source voltage. Significant improvements in both were observed from the first to second circuit. Both overshoot and damping of oscillations were improved, and the gate voltage showed less ringing. No significant improvement in drain-source voltage was observable from the second to third circuit. However, the ringing in the gate voltage was considerably reduced, which is important for optimal switching behavior.

There are many uncertainties when analyzing high frequency switching behavior, which makes coming to a definite conclusion challenging. In an effort to account for these uncertainties, the switching energy loss for the two MOSFETs was calculated with three different approaches in order to obtain a spectrum of possible loss. The loss was calculated purely based on the switching waveforms captured on the oscilloscope, by time shifting the waveforms to account for different time delays in the active probes, and by using the voltage and current fall and rise times obtained, in the theoretical switching progression of inductive switching.

Based on these results, the SiC MOSFET had a total power loss of 25 W at 166 kHz in the worst-case scenario and 264 kHz in the best-case scenario. The Si MOSFET had the same power loss at 89 kHz in the worst-case scenario and 198 kHz in the best-case scenario.

10 Suggestions for further work

In order to obtain more accurate results, more effort should be used in optimizing the converter and gate driver layout. Optimizing this for high frequency switching could eliminate some of the behavior problems caused by parasitic effects. Silicon Carbide MOSFETs operate optimally when the gate voltage is 20V at turn-on and -5V at turn-off. A layout with this configuration should be developed and compared to the results obtained in this thesis.

The gate driver IC has been a limiting factor. While one was limited to 18V gate voltage, the other was limited by a 2,5A source current. A gate driver capable of at least 20V and 5A source/sink current should be tested and compared to the results obtained in this thesis.

Problems with overheating the MOSFETs and boost diode occurred regularly due to too high losses and poor cooling. Therefore, a double-pulse test could be more useful in this perspective. This would enable observation of switching behavior at any desired voltage and current, without the same risk of thermal breakdown.

Comparing these Si and SiC MOSFETs directly can also be considered inaccurate. The MOSFETs have the same package size, but the SiC MOSFET have twice the current rating. This high possible load current have effect on the other parameters of the MOSFET, such as the intrinsic capacitances. For a more direct comparison, the ratings of the MOSFETs should be equal.

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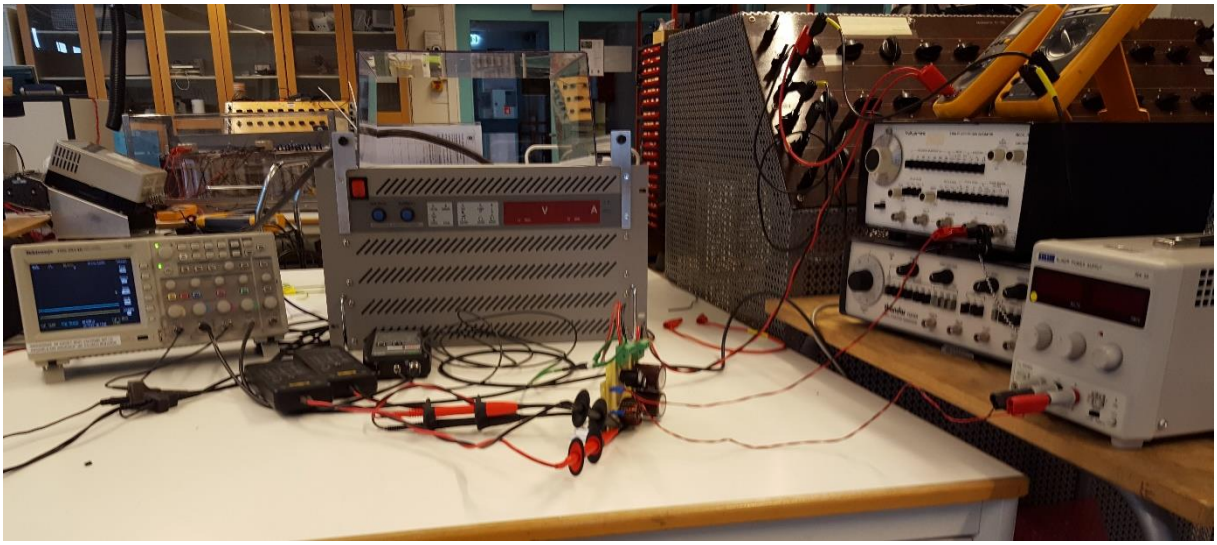
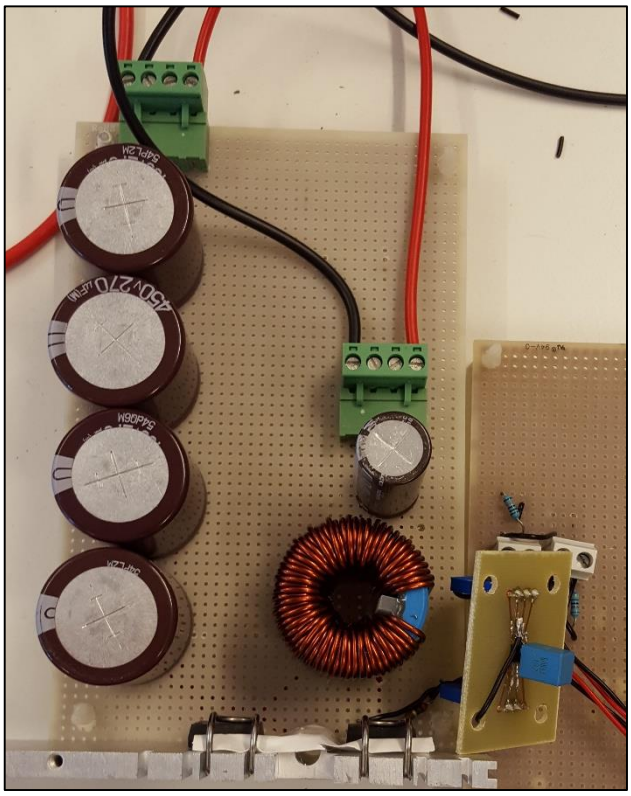
Appendix A: Laboratory setup

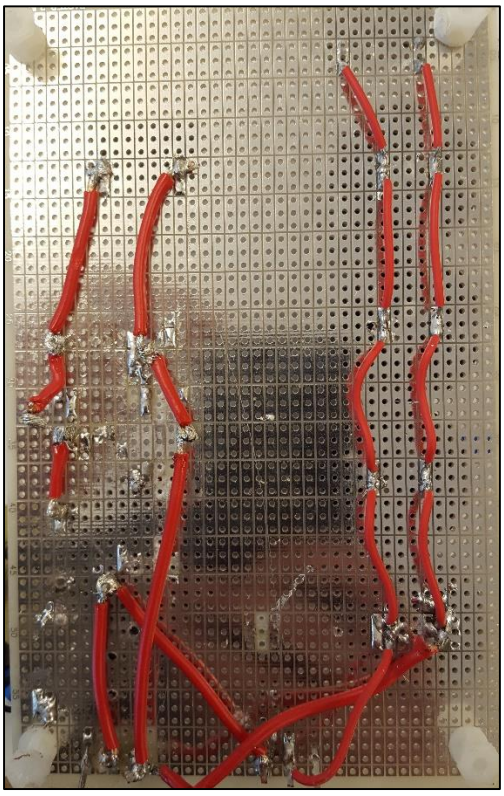


Appendix B: Circuit layouts

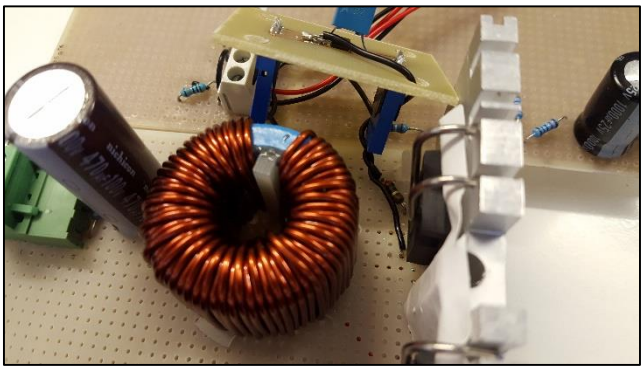
B1. Veroboard



Veroboard top side.

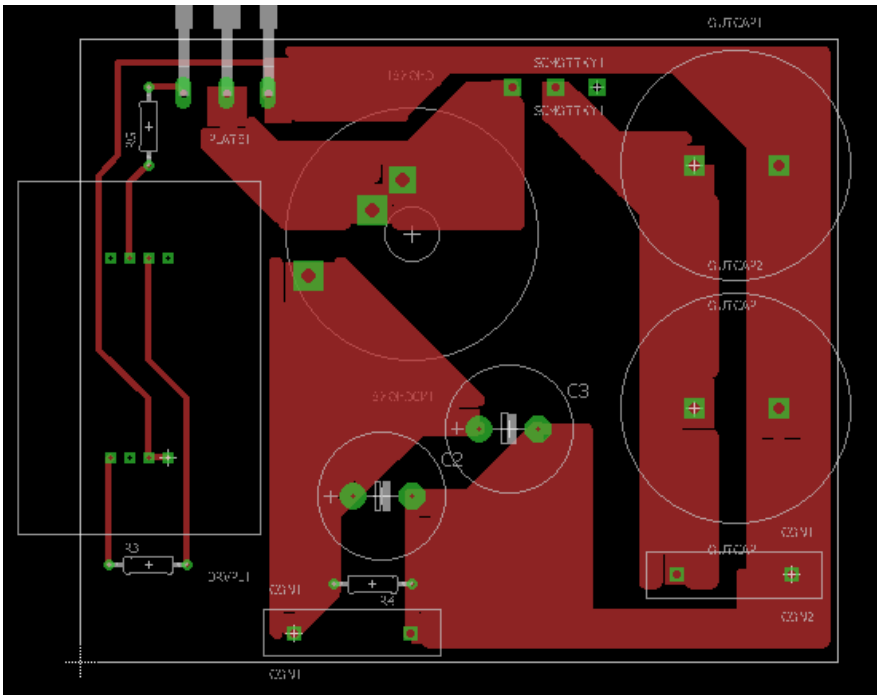


Veroboard bottom side.

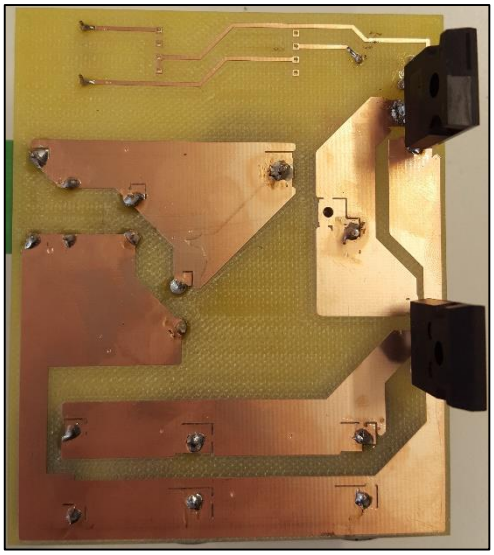


Veroboard top side and gate wires.

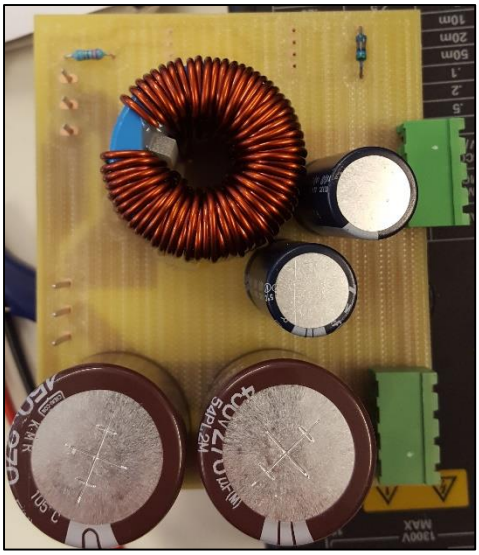
B2. PCB layout 1



EAGLE layout for first PCB.

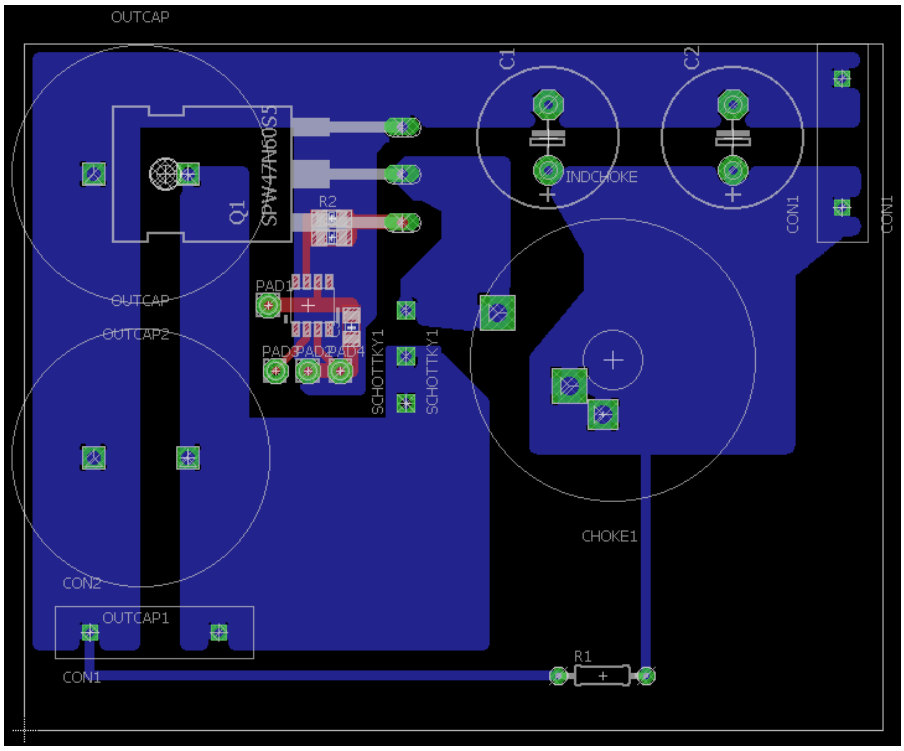


First PCB bottom side.

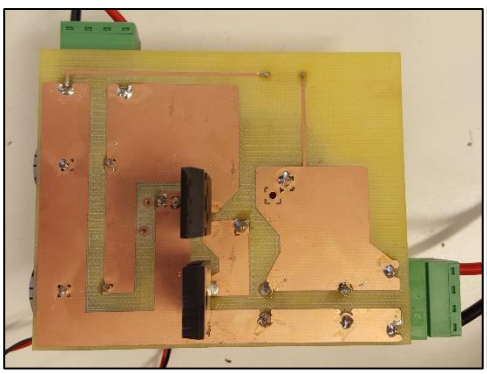


First PCB top side.

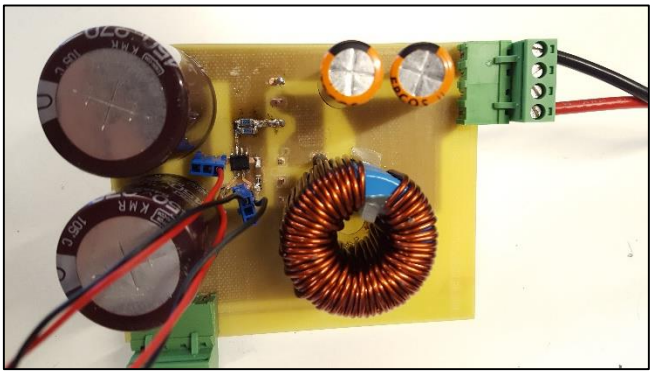
B3. PCB layout 2



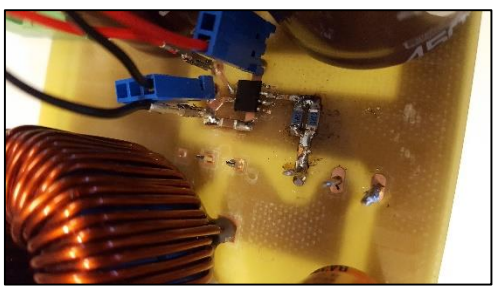
Final PCB EAGLE layout.



Final PCB bottom side.

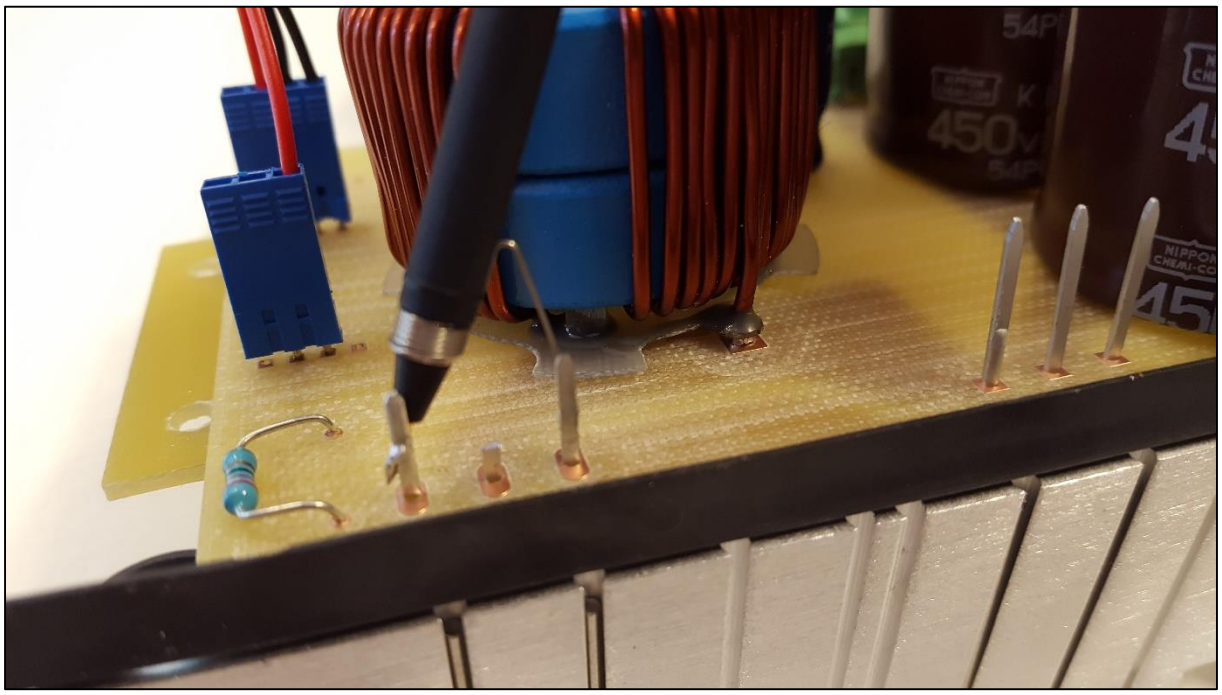


Final PCB top side.

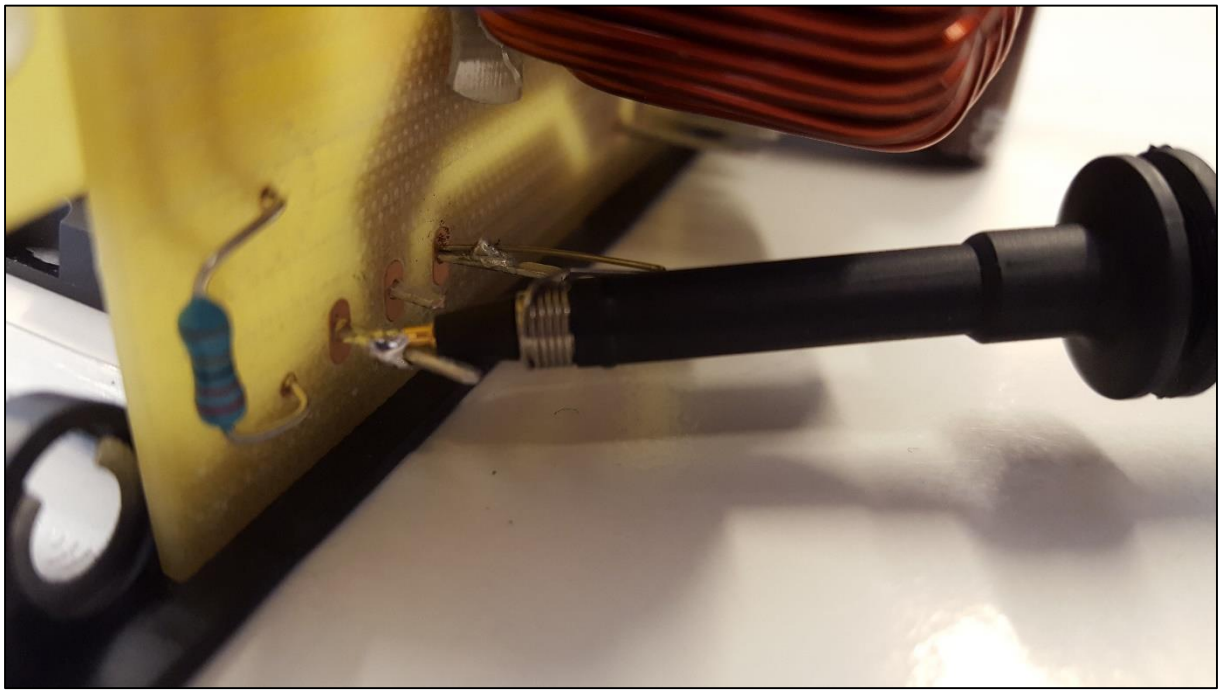


Final PCB, gate driver circuit close-up.

Appendix C: Probing with passive probe



Passive probing, front view.



Passive probing, side view.