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Ambient RF-energy harvesting at 900 MHz

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Preface and acknowledgments

This thesis is written as a part of the degree of Master of Science (MSc) at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU). The work was carried out in the spring of 2016 under the supervision of associate professor Morten Olavsbråten (NTNU) and Torolv Skjølsvik (Nordic Semiconductor). The assignment was given by Nordic Semiconductor.

First I would like to thank Morten Olavsbråten for all the help in the work of this thesis. Many hours have gone into discussing possible approaches and simulation results, and I am very thankful for all the time spent on this.

Second I want to thank Torolv Skjølsvik for giving me the opportunity to work with this RF-harvesting system. Your insight in other energy harvesting systems has been valuable. It is a shame that there was not enough time to see this harvester realised, since I know that you would appreciate it as much as I would.

I would also like to thank Professor Johannes Skaar for the help in the work leading up to this thesis.

Lastly I would like to thank my cohabitant Martine Lund Andresen for holding the fort in the writing of this and my newborn son Birk for giving me so much joy and energy in these final weeks.

Trondheim, July 2016

Fredrik Sundt Brynhildsvoll

Acronyms

ADS	Advanced design system
FET	Field-effect transistor
GSM 900	GSM frequency band from 890-960 MHz
JFET	Junction gate field-effect transistor
MESFET	Metal–semiconductor field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
RBW	Resolution bandwidth
RF	Radio frequency
RFID	Radio-frequency identification
WLAN	Wireless local area network

Abstract

In this thesis a RF-energy harvesting system able to harvest ambient power at 900 MHz (GSM band) is simulated. Especially the efficiency at low power is of interest (-19 to -23 dBm rectifier input). A rectifier and a boost converter is simulated in Advanced Design System (ADS) to determine the efficiency and output voltage. A power managing circuit able to turn the load (nRF52 chip from Nordic Semiconductor) on when sufficient power is accumulated is also presented.

Simulations show that a 3-stage rectifier is optimal to maximize efficiency. The efficiency is 32.4 % and 19.6 % at input powers of -19 dBm and -23 dBm. The output voltages are 435 mV and 184 mV respectively.

The boost converter is simulated with input powers from -24 dBm to -30 dBm (output of rectifier). It is able to charge a capacitor to 2.5 V at all simulated input powers. The efficiency with 2 V output voltage is 61.7 % and 52.2 % with input powers of -24 dBm and -30 dBm. Since the loss in the oscillation network is not included these efficiencies are overestimated.

The total efficiency is 20.0 % and 10.2 % at input powers of -19 dBm and -23 dBm. It is shown that the harvester can provide power to the nRF52 chip at input powers down to -21 dBm if the oscillation network consumes less than 733 nW. With this power consumption, estimates of the charge time reveal that the load can broadcast air temperatures at intervals of 84 seconds when the input power is -19 dBm. The interval is 188 seconds and 977 seconds (~17 minutes) at input powers of -20 dBm and -21 dBm respectively. If the oscillation loss is less than 367 nW the harvester can operate down to -22 dBm.

Sammendrag

I denne masteravhandlingen simuleres et RF-energi høstingssystem som er i stand til å høste omgivende energi ved 900 MHz (GSM bånd). Av spesiell interesse er effektiviteten ved lave effekter (-19 dBm til -23 dBm referert til inngangen av likeretteren). En likeretter og en spenningsforsterkende krets (boost converter) er simulert i Advanced Design System (ADS) for å fastslå effektivitet og utgangsspenning. En krets som gjør energi tilgjengelig for lasten (nRF52 mikrokontroller fra Nordic Semiconductor) når nok energi er akkumulert, presenteres også.

Simuleringer viser at tre steg i likeretteren er optimalt for å maksimere effektiviteten. Da er effektiviteten 32.4 % og 19.6 % ved inngangseffekter på henholdsvis -19 dBm og -23 dBm. Utgangsspenningene er henholdsvis 435 mV og 184 mV ved de samme effektene. Den spenningsforsterkende kretsen er simulert med inngangseffekter fra -24 dBm til -30 dBm (tilsvarer utgangen på likeretteren med tre steg). Den er i stand til å opp lade en utgangskondensator til 2.5 V ved alle simulerte inngangseffekter. Effektiviteten med 2 V utgangsspenning er 61.7 % og 52.2 % med inngangseffekter på henholdsvis -24 dBm og -30 dBm. Siden tap i det oscillerende nettverket ikke er tatt med i effektberegningene er dette et overestimat av den faktiske effektiviteten.

Total systemeffektivitet er 20.0 % og 10.2 % ved inngangseffekter på -19 dBm og -23 dBm. Det er vist at høstesystemet kan forsyne lasten ved inngangseffekter ned til -21 dBm dersom effektforbruket i det oscillerende nettverket er mindre enn 733 nW. Med dette forbruket viser estimater av oppladningstiden at lasten kan kringkaste lufttemperaturer med intervaller på 84 sekunder ved en inngangseffekt på -19 dBm. Intervallene er 188 sekunder og 977 sekunder (~17 minutter) med inngangseffekter på henholdsvis -20 dBm og -21 dBm. Dersom det oscillerende nettverket bruker mindre enn 367 nW kan høstesystemet forsyne lasten med inngangseffekter større enn -22 dBm.

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Chapter 1

Introduction

1.1 Development of RF-harvesting

In the beginning of the 1900s Nikola Tesla demonstrated wireless power transfer [21] and in 1969 Brown [4] showed that a small helicopter could be RF-powered when a high power transmitter is used. In recent years radio-frequency identification (RFID) have been widely deployed in numerous applications as key-cards, shoplifting alarms and as a payment method. A dedicated antenna provide power to the RFID chips by use of near field. In recent years the power consumed by microcontrollers have dropped drastic and researchers are now looking at the possibility to use far field radiation to power small electronic devices. Especially the use of ambient RF-power is interesting, as no dedicated transmitter source is needed.

1.1.1 Wireless energy transfer

Wireless energy transfer can be divided into inductive coupling, magnetic resonance coupling and electromagnetic radiation. The high efficiency of inductive coupling and magnetic resonance coupling is interesting, but the short range make them unsuitable for many applications. The focus in this thesis is electromagnetic radiation, but a short summary of the different techniques is included for comparison. The techniques are summarized in Table 1.1. Note that the efficiencies of the inductive coupling and magnetic resonance coupling is efficiency from transmitter to receiver, while the RF-energy transfer is the efficiency of only the harvesting system. Due to this the efficiencies cannot be compared directly.

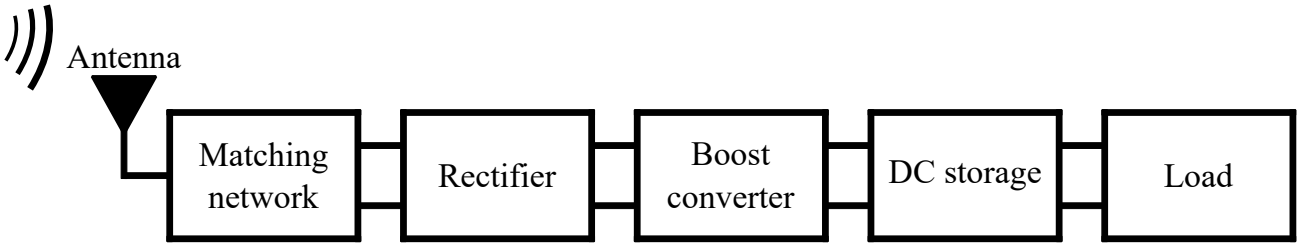


Figure 1.1: System overview of the RF-harvesting system, consisting of an antenna, matching network, rectifier, boost converter, DC storage and the load.

Inductive coupling

An electric transformer is a good example of inductive coupling. An alternating current in a primary coil generates a varying magnetic field that another coil can use to harvest power. The near field is used and the magnetic field strength decay with a factor of $1/r^3$ which strictly limit the range (typical range is less than the coil diameter). Inductive coupling is commercially used in charging of electric toothbrushes and medical implants, but the limited range make it unsuitable for power transfer over large distances [34].

Magnetic resonance coupling

Magnetic resonant coupling is an improvement of the inductive coupling. It is developed by Kurs et al. [19] and coupled coils with non-radiative magnetic resonance is utilized. An efficiency of 40 % over a distance of 8 coil radii was demonstrated with a transmitted power of 60 W. Compared to inductive coupling this is a big improvement of the range, but high power is needed. Charging of cellphones and automotive is demonstrated, at short range and with high powers.

RF-energy transfer

In RF-energy transfer the far field radiation is exploited. The far field decay with a factor of $1/r$, outperforming the other techniques over long distances. In the rest of this thesis only RF-energy transfer is considered.

1.2 Harvesting system

A system overview of a RF-harvesting system is showed in Figure 1.1. The antenna receives the RF-power, and the rectifier converts the RF-signal from the antenna to a DC voltage. Between the

Table 1.1: Comparison of different wireless energy transfer techniques. Table from[20].

Wireless energy transfer technique	Effective distance	Efficiency	Applications
Inductive coupling	From a few millimeters to a few centimeters	From 5.81 % to 57.2 % when frequency varies from 16.2 kHz to 508 kHz	Passive RF identification (RFID) tags, contactless smart cards, cell phone charging
Magnetic resonance coupling	From a few centimeters to a few meters	From above 90 % to above 30 % when distance varies from 0.75 m to 2.25 m	PHEV charging, cell phone charging
RF-energy transfer	Depend on distance and frequency and the sensitivity of RF-energy harvester (typically from several meters to several kilometers)	Depends of the input power. 0.4 % at -40 dBm, above 18.2 % at -20 dBm and above 50 % at -5 dBm	Wireless sensor network, wireless body network

antenna and the rectifier, a matching network is needed to maximize the power transfer. The output voltage of a rectifier is typically low and a boost converter is needed. The DC storage hold the amplified voltage and is a power source for the intended load. The harvesting system is presented in detail in chapter 3.

1.3 Specifications for RF-harvesting

- Provide power to the Bluetooth Low Energy chip nRF52 from Nordic Semiconductor
- Harvest ambient RF-power in the GSM 900 band (890-960 MHz)
- Efficient harvesting with input powers from -19 to -23 dBm (12.6 μW to 5 μW) at the input of the rectifier
- Provide an output voltage of 2.5 V

1.4 Commercially available RF-harvesting systems

Powercast is a commercially available RF-harvesting system operating in the GSM 900 MHz band. Both receivers (RF-harvesters) and transmitters providing RF-power of 3 W to the receivers are sold.

P2110B is a harvesting chip with a built in rectifier and boost converter with an efficiency of 10 % at an input power of -12 dBm (63 μW). The output power is stored on a capacitor with an output voltage of 3.3 V.

Another product not yet to be released is Freevolt [9] which is to operate at multiple frequencies (2G, 3G, 4G, Wifi and Digital TV). It is not stated if the harvester is to operate at these frequencies concurrently or be single band systems as Powercast. No information regarding efficiency of output voltage is available when this thesis is written.

1.5 Thesis structure

The thesis is structured as follows.

Chapter 1 provides a short introduction to the development of wireless power transfer and a comparison of different wireless power transfer techniques. A system overview of a typical harvesting system is presented together with the specifications of the harvester of interest in this thesis. Lastly two commercial RF-harvesting system are presented.
Chapter 2 includes some theory of interest. It includes how ADS calculates transient analysis, different transistor types, calculations of power density and the use of a matching network.
Chapter 3 is a through presentation of the harvesting system. All parts are presented and the rectifier, boost converter, storage capacitor and a power managing circuit is analysed in detail. This chapter provide calculations used later in the simulations.
Chapter 4 presents spectrum measurements done in the work leading up to this master thesis. Measurements are conducted at NTNU and they are compared to other results obtained in Trondheim and London. The aim of these measurements is to find the frequency band most suitable for RF-harvesting.
Chapter 5 include simulations of the rectifier and boost converter. The efficiency and output voltage of the rectifier when the number of stages are varied is simulated and an optimal input impedance is found. Different components in the boost converter are simulated to optimize the efficiency. The total efficiency and charge time of the harvester is also calculated.
Chapter 6 discuss the simulation results and compare it with other harvesting systems. Possible uncertainties in the simulation results are also discussed.
Chapter 7 summarize and concludes the thesis.

Chapter 2

Theoretical Background

2.1 Transient analysis

To analyse circuit performance with respect to time transient analysis can be performed in Advanced Design System (ADS). In transient simulations the maximum timestep is dependent on the frequency, 16 points is needed for every period. This makes the simulations time consuming, at 900 MHz (frequency of interest in this thesis) 900 million points is needed to simulate 1 second. Through the work of this thesis some attempts to reduce the computation time is conducted and the reader should have some knowledge to how the transient analysis is done. A manual describing how transient simulations are solved is available from Agilent Technologies [31] (owner of ADS at time of release). Key concepts from this manual is presented below.

The time dependency of the voltages and currents of the circuit is solved. This is done with a set of integro-differential equations. The result is a non-linear analysis with respect to time. The analysis is performed entirely in the time-domain, making it unable to account for frequency-dependent behaviour of distributed elements such as microstrip elements. Such elements need to be represented by simplified, frequency-independent models such as lumped elements, transmission lines with constant loss and no dispersion and circuits that are open or shorted. At low frequencies these simplifications are usually very reasonable.

Transient Simulation Process

The simulator operates in the following steps. Variables set by the user are in italic:

1. *Time-sweep range*, *tolerances* and *iteration limits* are specified by the user. Initial voltages in nodes in the circuit can also be specified.

2. At zero time a DC analysis is conducted.

3. The simulator set up a breakpoint table to deal with frequency-domain-devices and data. Independent source waveforms can have sharp transitions and may not coincide with the time step of the simulation. The breakpoint table is a sorted list with such transition points of the independent sources. If the next timestep is sufficiently close to a breakpoint the timestep is adjusted to land on this point. This reduce unnecessary timestep-reduction in the simulation.

4. The time is updated, and the values of independent sources are calculated at that time.

5. Through numerical integration and a finite number of Newton-Raphmsson iterations an attempt is made to solve the system of equations. If the number of iterations exceeds *Max iterations per time point* the time step is reduced by a factor of *Integration coefficient mu* divided by 8. If this time step is acceptable the analysis is repeated from step 4. If *Integration coefficient mu* is set to zero, backward-Euler numerical integration is used. Otherwise, trapezoidal numerical integration is used.

6. Following convergence, the local truncation error is calculated. The default *Integration method (IntegMethod)* to estimate the error is Trapezoidal. Another alternative is Gear's method.

7. The time step interval is calculated. The time step is computed by means of the truncation error estimate method as default.

8. The error tolerance is compared with *Local truncation error over-est factor*. If the error is within acceptable limits, the results are stored and analysis continues at the next time point. If not, the analysis is repeated at a smaller time step.

9. Steps 3 through 9 are repeated until the used-specified time-sweep range has been analysed.

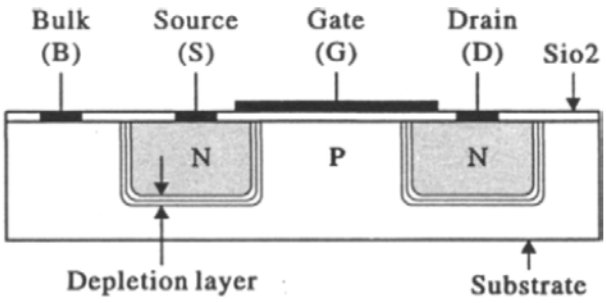


Figure 2.1: Cross section of a N-channel MOSFET. Figure from [33, p 102]

2.2 Transistor types

Numerous types of transistors exist and the two main types are Bipolar Junction Transistors (BJT) and Field Effect Transistors (FET). BJTs are current controlled transistors widely used, but since they are not a part of this thesis they are not discussed further. FET transistors are voltage controlled and due to the (very) low gate current the input impedance of these transistors is high (typically MΩ or higher). Due to this the influence of the connected circuit is low. Three types of FET transistors is the MOSFET, MESFET and JFET presented below.

The MOSFET (Metal-oxide-semiconductor field-effect transistor) can be either enhancement mode or depletion mode. An enhancement mode MOSFET is off when $V_{GS} = 0$, while a depletion mode is on at VGS=0. Only enhancement modes is discussed here. Figure 2.1 show the cross section of a N-channel MOSFET. In MOSFETs the bulk is usually connected to the gate or source (depending of N-channel or P-channel) making it a three terminal transistor. With a positive V_{GS} the gate attracts negative charge from the source and drain regions. As the voltage increase up to the threshold of the transistor a channel is formed and current will start going from drain to source. When $V_{DS} > V_{GS} - V_{th}$ (active region) a simplified current equation is

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{2.1}$$

where μ_n is the carrier mobility in bulk, C_{ox} is the gate capacitance per unit area, W is the gate width and L is the effective gate length[6, p. 20]. By putting a negative sign in front of all voltages in (2.1) the current in a P-channel MOSFET is found.

The MESFET (Metal-Semiconductor Field-Effect-Transistor) (Fig. 2.2) have a conducting channel between source and drain [35]. A Schottky metal gate is used to control the carrier flow between

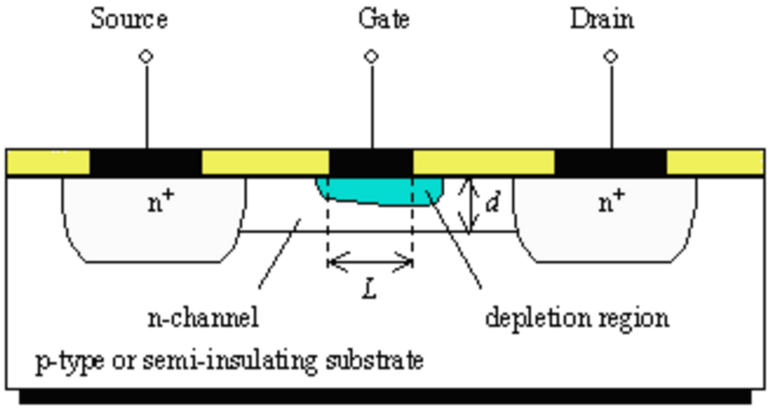


Figure 2.2: Cross section of a MESFET transistor with gate length (L) and channel thickness (d). Figure from [35, Chap. 3.6]

source and drain. The channel is controlled by varying the width of the depletion layer underneath the metal contact. The thickness of the conducting channel is then modulated, and hence the current. The key advantage over MOSFETs is the higher mobility of carriers in the channel. The result is a higher current, transconductance and that the device can operate at a (much) higher frequency. The presence of the Schottky metal gate is a disadvantage, as this limit the forward bias voltage on the gate to the turn-on voltage of the Schottky diode (typically 0.7 V for GaAs Schottky diodes). The MESFET is therefore harder to fabricate, as the voltage threshold need to be lower than this.

Figure 2.3 show the cross section of both a N-channel JFET and a P-channel JFET with corresponding symbols. The current in a JFET is maximum when V_{GS} is zero and can be controlled by applying a potential to V_{GS}. This increases the depletion layer and thus reduce the channel, called pinching off the channel. For a N-channel JFET the gate voltage need to be lower than the source voltage to reduce the current. The P-channel is opposite, when the gate voltage is higher than the source voltage the current is reduced. If g_{co} is the channel conductance when $V_{GS} = 0$ the channel current (source to drain) of a N-channel JFET is

$$I_c = \frac{-g_{co}\,(V_{GS} - V_{th})^2}{2V_{th}} \tag{2.2}$$

where V_{th} is the voltage threshold of the JFET [33, eq.10.2].

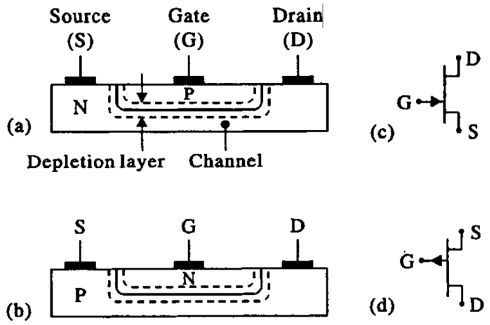


Figure 2.3: JFET cross-sections and symbols.
(a) N-channel JFET with symbol in (c)
(b) P-channel JFET with symbol in (d). Figure from [33, p 132]

2.3 Theoretical power density

The power from an antenna is distributed on a spherical shell, meaning that the power density will decrease with a rate of $1/r^2$. Under the assumption that the antenna is isotropic, the power is evenly distributed in all directions. Using Friis formula the power density a distance r away from the antenna is

$$S = \frac{P_t}{4\pi r^2} \times \frac{1}{10000} \quad \left[\frac{\mathrm{W}}{\mathrm{cm}^2}\right] \tag{2.3}$$

where P_t is the transmitter effect. The unit $\mathrm{nW/cm^2}$ is the most used in literature.

The transmitted power from GSM 900 antennas placed in urban areas is low to reduce interference. With an isotropic antenna the typical power is 0.5 W [30] from which the power density can be calculated (Tab. 2.1). The power received by an antenna with an effective area of 1000 $\mathrm{cm^2}$ (antenna assumed in this thesis) is also included to give the reader a feeling of what powers it is possible to harvest from one antenna.

Table 2.1: Theoretical power density (S_{BA}) from one antenna in the GSM 900 band and power received (P_{r}) by an antenna with effective area (A_{e}) of 1000 $\mathrm{cm^2}$. The transmitted power is 0.5 W.

r [m]	S_{BA} [$\mathrm{nW/cm^2}$]	S_{BA} [$\mathrm{dBm/cm^2}$]	P_{r} (A_{e}=1000 $\mathrm{cm^2}$) [dBm]
10	398	-34	-4
50	80	-41	-11
100	40	-44	-14
200	20	-47	-17
1000	4	-54	-24

2.4 Matching and amplification

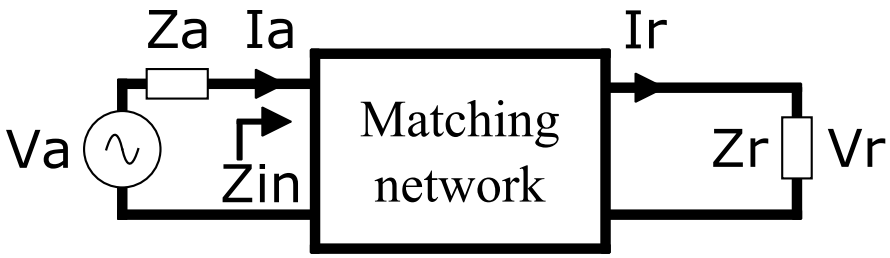


Figure 2.4: Matching network inserted between the antenna and the rectifier.

To obtain maximum power transfer between sub circuits with different impedance a matching network is needed. An example is the matching network between the antenna and the rectifier shown in Figure 2.4. Here V_a and I_a is the voltage and current from the antenna and Z_a is the antenna impedance. V_r and I_r is the voltage and current at the input of the rectifier while Z_r is the input impedance of the rectifier. Let the impedance seen looking into the matching network be Z_{in}. It is well known [22, p. 400] that maximum power transfer occurs when Z_{in} is the complex conjugated of the antenna impedance ($Z_{in} = Z_a{}^*$). Assuming a lossless matching network all power out of the antenna is transferred to the rectifier. The power in the rectifier is

$$P_r = \frac{V_r^2}{Re(Z_r)} = \frac{V_r^2}{R_r} \tag{2.4}$$

where R_r is the real value of the rectifier input impedance. The real current from the antenna is

$$I_a = \frac{V_a}{Re(Z_a + Z_{in})} = \frac{V_a}{2R_a} \tag{2.5}$$

where R_a is the real antenna impedance and it is used that Z_{in} is the complex conjugate of the antenna impedance. The power consumed by the rectifier is

$$P_r = \left|I_a^2\right| Re\left[Z_{in}\right] = \frac{V_a^2}{4R_a}. \tag{2.6}$$

By comparing equation 2.4 and 2.6 and by defining the voltage gain as the ratio of V_r to V_a the voltage gain of the matching network is found

$$A_v = \frac{V_r}{V_a} = \frac{1}{2}\sqrt{\frac{R_r}{R_a}}. \tag{2.7}$$

From equation 2.7 it is evident that the voltage gain of the impedance transformation network increases with the square-root of the load impedance. This voltage gain can be used to overcome the voltage threshold of the diodes in the rectifier circuit.

Chapter 3

The harvesting system

A system overview of the RF-harvester presented in this thesis is shown in Figure 3.1. A circuit diagram of the complete harvesting system with components can be found in Appendix A. The **antenna** capture the power and make it available to the rest of the circuit. The antenna is not a focus in this thesis, but it is crucial that it work well for the complete frequency band the harvester is to operate at. It is here assumed that the antenna covers the GSM band at 900 MHz and that the effective area of the antenna is 1000 cm^2. The effective area of the antenna is discussed in Section 5.1.4.

The **matching network** is needed to transfer the power captured by the antenna to the rectifier without loss. Since the input impedance of the rectifier is higher than that of a typical antenna it will also contribute to a voltage gain as discussed in Section 2.4. The matching network is not a part of this thesis, but simulations (Sec. 5.1.4) will show that the matching network need to match the antenna to 1000 Ω.

The **rectifier** transform the input RF-signal to a DC voltage. The efficiency of the rectifier is

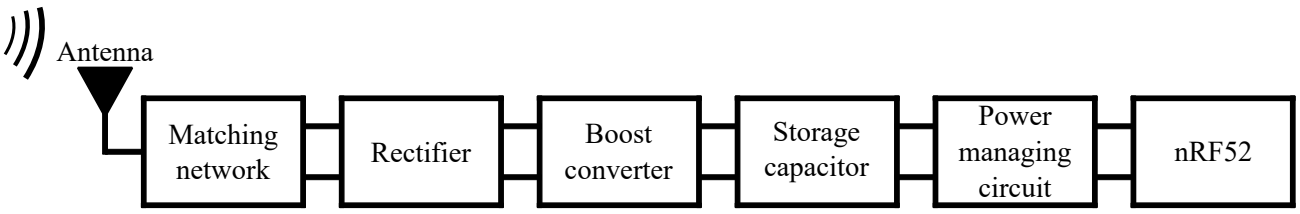


Figure 3.1: System overview of the RF-harvesting system presented in this thesis, consisting of an antenna, matching network, rectifier, boost converter, storage capacitor, power managing circuit and nRF52.

important and is defined as

$$\eta = \frac{P_{\mathrm{DC}}}{P_{\mathrm{RF}}} \tag{3.1}$$

where P_{DC} is the DC power out of the rectifier and P_{RF} is the power available at the input of the rectifier. The rectifier is described in Section 3.1.

It will be shown that the output voltage of the rectifier does not fulfil the specifications, therefore a **boost converter** is needed. Two boost converter topologies is presented in Section 3.2. In addition, a commercially available boost converter for low power applications is presented. The output power of the boost converter is charged onto a storage element. The energy can be accumulated on a capacitor of a battery, depending on the application. In this thesis a **storage capacitor** is assumed, since it can be charged and discharged an infinite number of times. Section 3.3 show how the capacitor value can be calculated.

The power consumed by the load (nRF52) is higher than the expected power from the harvester. Due to this a **power managing circuit** is needed. When sufficient energy is accumulated on the storage capacitor this circuit make the energy available for the load. A power managing circuit is presented in Section 3.4.

nRF52 is the intended load for the RF-energy harvester. This microcontroller is a low power System on Chip with Bluetooth Low Energy (BLE). Calculations of the needed power to do temperature measurements with an external sensor and send it over BLE is done in Section 3.4.

3.1 Rectifier

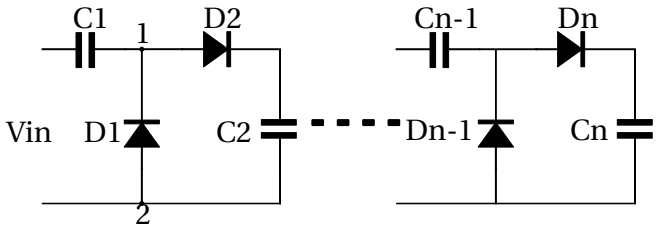


Figure 3.2: Full wave Villard voltage doubler.

The Villard voltage doubler (Fig. 3.2) is a rectifier which also amplify the input voltage. A 1-stage Villard voltage doubler (left part of Figure) can be made with two diodes and two capacitors. With ideal components the output voltage is twice the input voltage, hence the name. First assume that the diodes are ideal (no threshold voltage or loss) and that the capacitor values is so high that when they are charged or discharged the change in capacitor charge will not significantly change the voltage across them. Let the peak voltage of V_{in} be V_{m}. In the negative half cycle V_2 is larger than V_1 and a current is going through D_1 charging up C_1. At the peak negative amplitude $V_{\text{c1}} = V_{\text{m}}$. When the amplitude of the voltage starts increasing V_2 is less than V_1 making D_1 reverse biased so no current is going through it. In the positive half cycle V_{c1} is added to the input voltage forward biasing D_2 and charging up C_2. When the input voltage is at the maximum amplitude $V_{\text{c2}} = 2V_{\text{m}}$. This is repeated in the next negative half cycle. After enough cycles the output voltage will be twice the input voltage.

Multiple voltage doubler can be added in cascade to increase the voltage further. In the ideal case, by adding n voltage multipliers the voltage on the last capacitor (V_{out}) will be $2V_{\text{m}} \times n$. This is not achievable in practice due to loss in the circuit and non-ideal diodes. By taking the threshold voltage V_{th} into account Karthaus and Fischer [17] showed that the output voltage of a n-stage Villard voltage rectifier is

$$V_{\text{out}} = n(V_m - V_{\text{th}}). \tag{3.2}$$

3.2 Boost converter

The boost converter will amplify the voltage from the rectifier to a voltage the load can operate from. Three different approaches to this is presented, a simple boost converter, a self-oscillating boost converter and a commercially available boost converter.

3.2.1 Simple boost converter

A boost converter can be constructed with an inductor, a switch and a diode (Fig. 3.3). It also consists of two capacitors, C_{in} (holding the input energy) and C_{out} (storing the output energy). An oscillation network to switch the transistor is also needed. The frequency of the oscillation network is $f = 1/T$ and the on time is set by t_{on}. First assume that the switch and diode is ideal, short circuit when on (3.3b) and open circuit when off (3.3c).

Figure 3.4 show the currents and voltages in the boost converter. When the switch turns on at t=0 the diode voltage (V_{D}) is -V_{out}, making the diode reverse biased. The inductor voltage (V_{L}) change from 0 to V_{in}, increasing the current in the inductor. The current increase with a slope of V_{in}/L until the switch is turned off at time t=t_{on}. The current is then I_1=$V_{\text{in}} \times t_{\text{on}}/L$. When the switch is turned off current is still flowing in the inductor since it cannot change abruptly. The inductor is now working as a current source for the diode, forcing current to run through it and thus charging the output capacitor. The current is decreasing with a slope of $(V_{\text{in}} - V_{\text{out}})/L$ down to zero at time T. At this time the switch is turned on again and the process repeats itself.

In this ideal case all the magnetic energy stored in the inductor is transferred to the output capacitor. The stored magnetic energy is

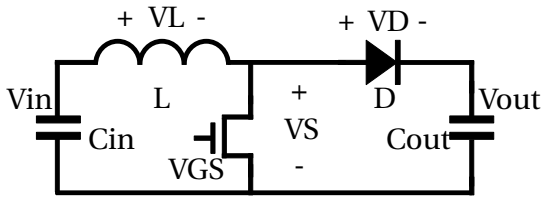
$$\triangle W_{\text{L}} = \frac{1}{2} L[I_{\text{L}}^2(t_{\text{on}}) - I_{\text{L}}^2(t_0)] \tag{3.3}$$

where $I_{\text{L}}(t_0)$ is zero in this example.

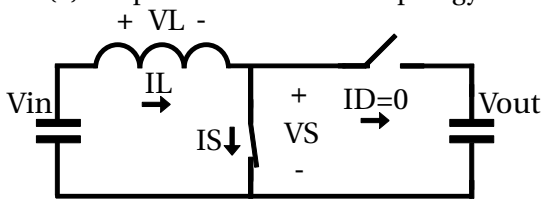
Loss in the boost converter when switching

When loss is taken into account the inductor value L will influence the efficiency. Figure 3.5 show the boost converter with losses included. Let us first consider the circuit when the switch is closed. The equivalent resistance in the circuit is then

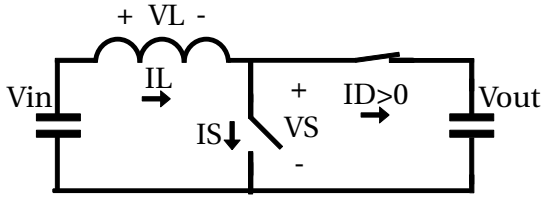
$$R_{\text{eq}} = R_{\text{in}} + R_{\text{L}} + R_{\text{S}}. \tag{3.4}$$



(a) Simple boost converter topology.



(b) Ideal boost converter circuit with switch closed.



(c) Ideal boost converter circuit with switch open.

Figure 3.3: Boost converter topology consisting of one inductor, a diode and a n-channel MOSFET transistor and the resultant ideal circuits with switch open and closed.

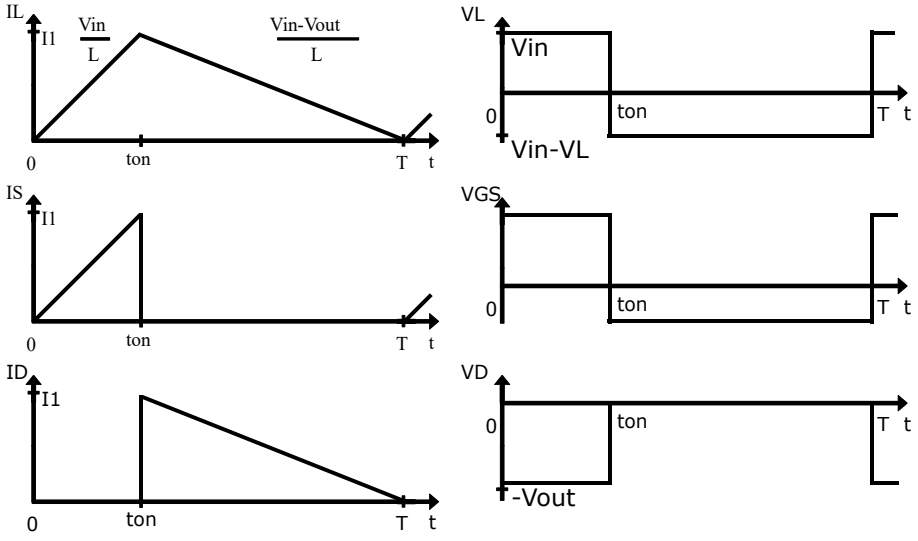


Figure 3.4: Currents and voltages in the inductor, switch and diode in the boost converter with ideal components.

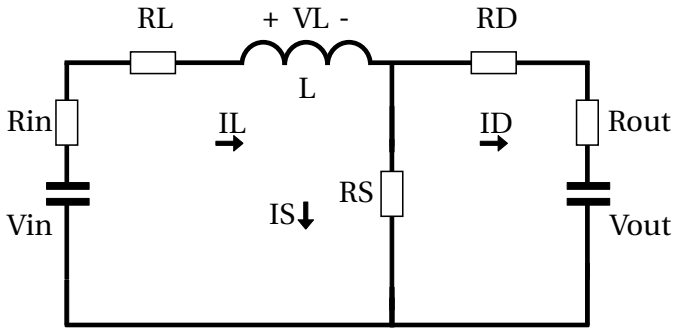


Figure 3.5: Boost converter circuit with the losses of the inductor (R_L), switch (R_S), diode (R_D), input capacitor (R_{in}) and output capacitor (R_{out}).

This is now RL circuit with the current

$$I_L(t) = \frac{V_{in}}{R_{eq}}\left(1 - e^{\frac{-R_{eq}t}{L}}\right) \tag{3.5}$$

and

$$P_{Loss} = \int R_{eq} I_L^2 = R_{eq} \int_0^{t_{on}} \left(\frac{V_{in}}{R_{eq}}\left(1 - e^{\frac{-R_{eq}t}{L}}\right)\right)^2 \mathrm{dt} \tag{3.6}$$

where P_{Loss} is the loss in the circuit which can be solved to

$$P_{Loss} = \frac{V_{in}^2}{2R_{eq}^2}\left(4Le^{\frac{-Rt_{on}}{L}} - Le^{\frac{-2Rt_{on}}{L}} - 3L + 2Rt_{on}\right) \tag{3.7}$$

If R_{eq}, V_{in} and t_{on} are assumed constant the loss can be found to be

$$P_{Loss} = \begin{cases} \frac{V_{IN}^2 t_{on}}{R_{eq}} & L = 0 \\ 0 & L = \infty \end{cases} \tag{3.8}$$

in the extreme values of L. As long as L is a positive number (all inductor values are) the loss is strictly decreasing with increasing L. The same procedure can be used to show that the loss is minimized with increasing L also when the switch is open.

The assumption to threat R_{eq}, V_{in} and t_{on} as constants might not hold. It holds for V_{in} as the input voltage is independent of L. When L is increasing R_{eq} is also assumed to increase since the number of turns in the inductor is generally higher with a high inductor value. This will increase R_L. The optimal pulse length t_{on} with a set L inductor is unknown and might change with increasing L value.

From this is seems like a big inductor value is preferable to minimize the loss, but simulations

should be done to see if this is the case.

3.2.2 Self oscillating boost converter

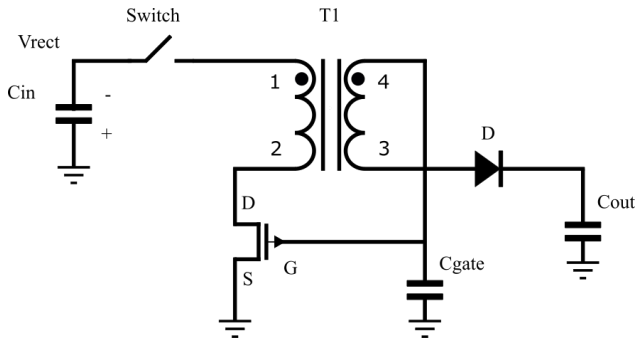


Figure 3.6: Circuit diagram of a self-oscillating boost converter consisting of two coupled inductors, a p-channel JFET and a diode. It also includes a capacitor modelling gate capacitance of the JFET, input and output capacitors and a pushbutton switch.

The self-oscillating boost converter (Fig. 3.6) consists of two coupled inductors, a p-channel JFET, a diode, a capacitor modelling the gate capacitance of the JFET (C_{gate}), an input capacitor and an output capacitor. A switch is also included between the input capacitor and the boost converter. This is because the boost converter need a startup voltage before the oscillation can start. When the voltage is high enough the switch is shut.

A p-channel JFET have three regions

$$\begin{aligned} &\text{off}: -V_{\text{GS}} < -V_{\text{th}} \\ &\text{linear}: 0 < -V_{\text{DS}} < -V_{\text{GS}} + V_{\text{th}} \\ &\text{saturated}: 0 < -V_{\text{GS}} + V_{\text{th}} < -V_{\text{DS}} \end{aligned} \tag{3.9}$$

where V_{th} is the voltage threshold of the JFET. In this explanation it is assumed that the JFET behaves ideally: in the off region no current is running through it, in linear region it behaves as an variable resistor and in the saturated region is behaves as a short circuit. Also remember the dot convention of coupled inductors, when the current enters the dotted terminal on the primary inductor the voltage is positive at the dotted terminal on the secondary inductor.

Initially assume that the circuit is completely discharged. After some time, the voltage on the input capacitor is sufficient to run the circuit and the pushbutton switch is pushed. Since the gate voltage of the JFET is zero a current start running from ground through the primary inductor (V_{in} is negative). By the dot convention the voltage on node 3 is positive and a current will go

through the diode charging up the output capacitor. V_{GS} becomes negative due to dot convention and the current going through the JFET starts decreasing until it is pinched off completely. The magnetic energy stored in the secondary inductor is drawn to charge the output capacitor, making the voltage on V_{GS} increase and eventually become zero. Then the cycle repeats itself.

With this boost converter Gudan et al. [10] were able to harvest energy and charge a battery at input powers down to -25 dBm, proving the concept of this boost converter. The author of this thesis have tried to replicate these simulations results in both ADS and LTspice (simulation tool provided by Linear technology). Many days have gone into making the simulations work, but it has not been possible to get the boost converter to oscillate. The reason for this is unknown, but one possibility is inaccuracy in the spice model provided by the manufacturer. The JFET used is MMBFJ270 manufactured by Fairchild Semiconductor. This is a new revision of their old JFET J270, but a new spice model is not provided and the old model have been used. Numerous inquiries towards the manufacturer have not resulted in a new model. Other JFETs are also simulated, with no resulting oscillation. Still, this boost converter is presented as a future solution, since it does not need extra switching circuitry to function.

3.2.3 Commercially available boost converters

Low power boost converters are commercial available, since they are used by other energy harvesting techniques like solar panels and Thermal Electric generators. BQ25570 [16] from Texas Instruments is a boost converter able to function at input voltages down to 100 mV. The efficiencies at different input voltages with an input current of 10 μA and output voltage of 2 V is shown in Table 3.1 where the input power is also calculated. The author of this thesis have not been able to find a boost converter with higher efficiencies at these powers.

Table 3.1: Efficiency of the commercially available boost converter (BQ25570 [16]) from Texas Instruments at different input voltages. The input current is 10 μA and the output voltage is 2 V.

V_{in} [V]	P_{in} [μW]	P_{in} [dBm]	Efficiency
0.1	1	-30.0	0.00
0.2	2	-27.0	0.06
0.3	3	-25.2	0.40
0.4	4	-24.0	0.51
0.5	5	-23.0	0.60

3.3 Storage capacitor

With the suggested power managing circuit, the attached load (nRF52) is disconnected from the harvesting circuit when the harvester accumulate energy, and is turned on when sufficient power is available. The time between the active periods can be minimized by carefully selecting the size of the storage capacitor. The do this measurements of the current consumption of the nRF52 is needed.

The supervisor from Nordic Semiconductor have designed a solar panel harvesting system which measure the air temperature with an external sensor and broadcast it once every second. The average current consumption at an input voltage of 2 V is found to be 19 μA. It is desirable to send the data two times, and in addition some additional energy is needed to turn the chip on. The startup energy is assumed to be equal to one additional second making the needed energy

$$U_{\text{cycle}} = I \times V \times t = 19\mu\text{A} \times 2\text{V} \times 3\text{s} = 114\mu\text{J}, \tag{3.10}$$

where t is the time used. On a capacitor the energy stored is

$$U = \frac{CV^2}{2}\,[\text{J}]\,, \tag{3.11}$$

which can be used to find the value of C which will draw U_{cycle} from the capacitor as the voltage change from V_{high} to V_{low}. The minimum capacitance value is

$$C_{\text{min}} = \frac{2U_{\text{cycle}}}{V_{\text{high}}^2 - V_{\text{low}}^2} = \frac{2 \times 114\mu}{2.3^2 - 1.84^2} \approx 111\mu\text{F} \tag{3.12}$$

where V_{high} and V_{low} is the calculated voltages the power managing circuit switch on and off (Sec. 3.4)

3.4 Power managing circuit

The available power from the harvesting circuit is expected to be less than what the load consumes while operating. Due to this the load need to be turned off while the system accumulated enough energy for it to operate. Figure 3.7 show a circuit which makes power available to the load when sufficient energy is harvested. It consists of two p-mos transistors (Q_1 and Q_2), one n-mos transistor (Q_3), five resistors and C_{out} which is the last capacitor of the harvesting circuit (the storage capacitor). This circuit is not simulated in this thesis, but the power managing circuit is together with nRF52 treated as the load for the harvesting system. Losses in this circuit is calculated and included when the total system performance is evaluated in Section 5.3.1.

The circuit is described thoroughly below, but the summary of the functionality is as follows: when V_{out} is increased above 2.3 V power is delivered through Q_1 to the load. The energy is taken from C_{out}, thus reducing its voltage. When the voltage falls below 1.8 V Q_1 it turned off and no power is delivered to the load. C_{out} is then recharged and the cycle start over.

Component	Value
R_1	2.2 MΩ
R_2	2.2 MΩ
R_3	6.8 MΩ
R_4	3.9 MΩ
R_5	30 MΩ
$R_{Q1/Q2}$ (p-mos)	1.5 Ω
R_{Q3} (n-mos)	500 Ω
$V_{\text{th, p-mos}}$	-0.86 V
$V_{\text{th, n-mos}}$	1.4 V

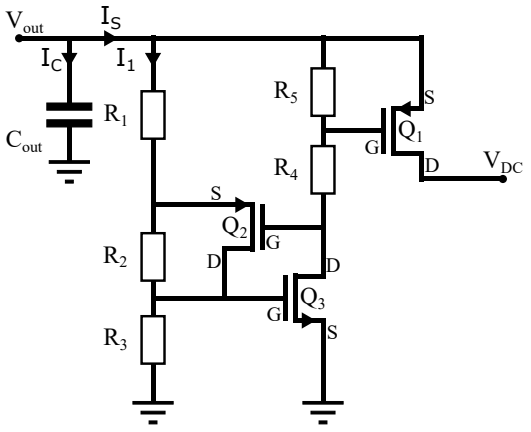


Figure 3.7: Power managing circuit used to turn the load on when sufficient energy is harvested. Q1/Q2: FDC6304P [26], Q3: ALD110914 [2].

To describe the functionality of the circuit a simple MOSFET transistor model is used. The transistor is either on (state on) or off (state off). In the different states the transistors can be substituted with the internal resistance R_{Qx}

$$R_{\text{eq}} = \begin{cases} R_{\text{Qx}} & \text{on state} \\ \infty & \text{off state} \end{cases}, \tag{3.13}$$

where R_{Qx} is stated in Figure 3.7. The condition for a transistor to be in on state is given by the gate-source voltage and the voltage threshold of the transistor (V_{th}). For a p-mos transistor (Q_1 and Q_2)

the condition is $V_{GS} > V_{th}$ and for a n-mos transistor (Q_3) it is $V_{SG} > |V_{th}|$. since power is supplied to the load through Q_1, a reasonable starting point will be to investigate this transistor.

$$V_{SG1} = V_S - V_{G1} = V_{out} - V_{out}\frac{R_4 + R_{Q3}}{R_5 + R_4 + R_3} = V_{out}\left(1 - \frac{3.3M + R_{Q3}}{33.9M + R_{Q3}}\right) \tag{3.14}$$

so in the different states og Q_3

$$V_{SG1} \approx \begin{cases} 0.9V_{out} & Q_3 \text{ on} \\ 0 & Q_3 \text{ off} \end{cases}. \tag{3.15}$$

The condition for delivering power to the load (Q_1 on) is

$$V_{SG1} > |V_{th}| = 0.86\text{V}. \tag{3.16}$$

By comparing (3.15) and (3.16) it is clear that Q_1 is always off when Q_3 is off. When Q_3 is on there is a minimum voltage V_{out} to turn Q_1 on, and it is found by rearranging (3.15) and using the value from (3.16)

$$V_{out} > \frac{0.86}{0.9} \approx 0.96\text{V}. \tag{3.17}$$

As we will see, V_{out} is always greater than 0.96 V as long as Q_3 is on. This means that Q_1 is in the same state as Q_3, they are either both on or off.

The analysis of Q_2 is similar, but a bit more complicated. This is because the gate-source voltage of both Q_2 and Q_3 is dependent on the state of the other. Since both transistors can be in on or off state, four different combinations are possible.
The internal resistance (R_{Q2}) of Q_2 is in parallel with R_2. Let

$$R_x = R_{Q2} \parallel R_2 \approx \begin{cases} 0 & Q_2 \text{ on} \\ R_2 & Q_2 \text{ off} \end{cases}, \tag{3.18}$$

then (since $R_{Q2} \approx 0$)

$$V_{SG2} = V_{S2} - V_{G2} = V_{out}\frac{R_x + R_3}{R_1 + R_x + R_3} - V_{out}\frac{R_{Q3}}{R_5 + R_4 + R_{Q3}} \tag{3.19}$$

where

$$V_{S2} \approx \begin{cases} 0.80V_{out} & Q_2 \text{ on} \\ 0.76V_{out} & Q_2 \text{ off} \end{cases} \tag{3.20}$$

and

$$V_{G2} \approx \begin{cases} 0 & Q_3 \text{ on} \\ V_{out} & Q_3 \text{ off} \end{cases}. \tag{3.21}$$

Table 3.2 summarize V_{GS1} for the four different states. From V_{GS1} and with (3.16) the needed voltage V_{out} to have Q_2 in the on state is also calculated.

Table 3.2: V_{SG1} at in the different states and needed $V_{\mathbf{out}}$ have Q_2 in on state.

	Q_3 on		Q_3 off	
	V_{SG2}	V_{out} [V]	V_{SG2}	V_{out}[V]
Q_2 on	$0.76V_{out}$	> 1.14	$-0.24V_{out}$	< -3.52
Q_2 off	$0.80V_{out}$	> 1.07	$-0.20V_{out}$	< -4.38

First notice that when Q_3 is off, a negative V_{out} is needed to put Q_2 into on state. A negative voltage from the boost converter is impossible, meaning that whenever Q_3 is off, Q_2 is also off. If Q_3 is in the on state the voltage needed to put Q_2 in on state depends on the state of the transistor. When Q_2 is on $V_{out} > 1.14$ V, and when it is off $V_{out} > 1.07$ V. As will be shown when Q_3 is investigated V_{out} is always above 1.14 V when Q_3 is on. This means that whenever Q_3 is on, Q_2 is also on. From this it is clear that the state of Q_2 is always the same as the state of Q_3.

Q_3 is a n-mos transistor, meaning that it is on when $V_{GS} > V_{th} = 1.4$V.

$$V_{GS3} = V_G - V_S = V_{out}\frac{R_3}{R_1 + R_x + R_3} \approx \begin{cases} 0.61V_{out} & Q_2 \text{ on} \\ 0.76V_{out} & Q_2 \text{ off} \end{cases}, \tag{3.22}$$

and from V_{GS3} the voltage of V_{out} to put Q_3 in on state will be

$$V_{out} > \begin{cases} 2.30\text{V} & Q_2 \text{ on} \\ 1.84\text{V} & Q_2 \text{ off} \end{cases}. \tag{3.23}$$

It is now possible to describe how the circuit works. Initially assume that $V_{out} < 1.84$V and that the harvesting circuit is charging the capacitor and therefore increasing the voltage. When $V_{out} <$ 1.84V, Q_3 is in off state, meaning that Q_1 and Q_2 also are off. Since Q_2 is off V_{out} need to increase up to 2.30V to turn Q_3 on. When this happens Q_1 and Q_2 turns on, delivering power to the load. This power comes from V_{out}, and if the power delivered to the load is greater than the power from the harvesting circuit, V_{out} will decrease. All transistors will be on until $V_{out} < 1.84$V, which is the minimum voltage needed to have Q_3 on when Q_2 is also on. Q_3 is then turned off, resulting in

Q_1 and Q_2 also turning off. With all transistors off the harvesting circuit will charge up V_{out} once more, and the cycle repeats itself.

The loss when all transistors is off is important, since it will draw energy from the output capacitor when the harvester is accumulating energy. The equivalent resistance seen looking into the circuit is then

$$R_{\text{eq}} = (R_1 + R_2 + R_3) \parallel (R_4 + R_5 + R_{\text{Q3}}) = R_1 + R_2 + R_3 \tag{3.24}$$

since $R_{\text{Q3}} = \infty$ when the transistor is off. Then

$$P_{\text{Power managing loss}} = \frac{V_{\text{out}}^2}{R_{\text{eq}}} = \frac{V_{\text{out}}^2}{11.2M} \approx 357\text{nW}. \tag{3.25}$$

Chapter 4

Spectrum measurements

The author of this master thesis wrote a project report [5] in December 2015. It was a study of already published literature and how they compare. This report also included spectrum measurements to find the available power in different frequency bands and compared this to other studies conducted other places. Based on these measurements it was concluded that the harvesting system should be created to function in the GSM 900 band. This full chapter is included in this thesis for completeness.

Measurements were performed with the spectrum analyzer Spectrum Master MS2721A from Anritsu [3] together with a log-periodical antenna from ETS-Lindgren, model 3142B [8]. This antenna is very directional therefore measurements have been taken in three directions in the horizontal plane (120 ° between each measurement). The spectrum analyser sweep the frequency band and take measurements at 551 points in the selected bandwidth. At each of these points the power is measured using a filter with a bandwidth given by the resolution bandwidth (RBW), which means the measured power (P_r) is the power with bandwidth RBW. The sweep time and frequency resolution of the measurements depend on RBW, a high RBW give short sweep time and poor frequency resolution.

The interesting property is the power density per Hz (S_Hz) thus the effective area of the antenna need to be removed. The relationship between the effective area and received power is [25, p. 119]

$$S_\mathrm{Hz} = \frac{P_\mathrm{r} 4\pi e_\mathrm{rad}}{G\lambda^2 \mathrm{RBW}} \quad \left[\frac{W}{\mathrm{Hz\,cm^2}}\right], \tag{4.1}$$

where G is the gain of the antenna provided by the manufacturer (Appendix F). The radiation efficiency e_rad of the antenna is unknown and assumed to be 1.

A measurement with bandwidth from 60MHz to 3GHz was taken at the lab (location 1) and in a typical office environment (location 2). The measurements are conducted with a high RBW to decrease the sweep time (RBW = 100kHz at the lab, RBW = 30kHz at the office environment). At each location measurements are taken in three directions and the data is processed to find the average. S_{Hz} of the two measurements is shown in Figure 4.1. A RF-harvester can make use of the input power in a band of frequencies. Therefore, one important parameter is the power density across different bands, denoted S_{BA} (W/cm^2) which will be

$$S_{\mathrm{BA}} = \sum S_{\mathrm{Hz}} M_{\mathrm{BW}} \quad [W/cm^2], \tag{4.2}$$

where M_{BW} is the spacing between the measurement points (frequency resolution). For the 7 bands with promising characteristics new measurements was taken with lower RBW (10kHz), at the same two locations. RBW was set to 10kHz to give a good resolution and S_{BA} was calculated using equation (4.2). The results are shown in Table 4.1. The resulting power density in all bands is low which might be because the network activity is low at the time of the measurements. The results suggest that the most suitable band is 4G (790-862 MHz) and GSM (890-960).

Table 4.1: Measurements of S_{BA} at two locations at NTNU. Three measurements are taken at each band in each location. (Measurements taken between 09.00 and 11.00 Tuesday 25.11.15.)

		Lab		Office		total
Band	Frequency MHz	Average S_{BA} (nW/cm^2)	Max S_{BA} (nW/cm^2)	Average S_{BA} (nW/cm^2)	Max S_{BA} (nW/cm^2)	Average S_{BA} (nW/cm^2)
DTV	470-790	0.001	0.001	0.004	0.008	0.003
4G	790-862	0.052	0.077	0.022	0.048	0.037
P-GSM	890-960	0.008	0.014	0.005	0.008	0.007
GSM&3G	1710-1930	0.003	0.003	0.002	0.003	0.002
3G	2120-2160	0	0	0	0	0
WLAN	2400-2484	0.007	0.018	0.0013	0.002	0.004
4G	2520-2655	0.001	0.001	0	0	0.001

The density of WLAN transmitters (phones, computers and routers) is very high, which might make the available power more evenly distributed compared to other bands. Measurements of S_{BA} in the WLAN band at four different locations (the lab, and three typical office environments) is therefore taken. Table 4.2 summarize S_{BA} at the different locations. The power density deviates with a factor of four from the highest to the lowest, therefore the theory of even distributed power does not hold.

Pinuela et al. [24] measured the input RF-power density at all the London underground net-

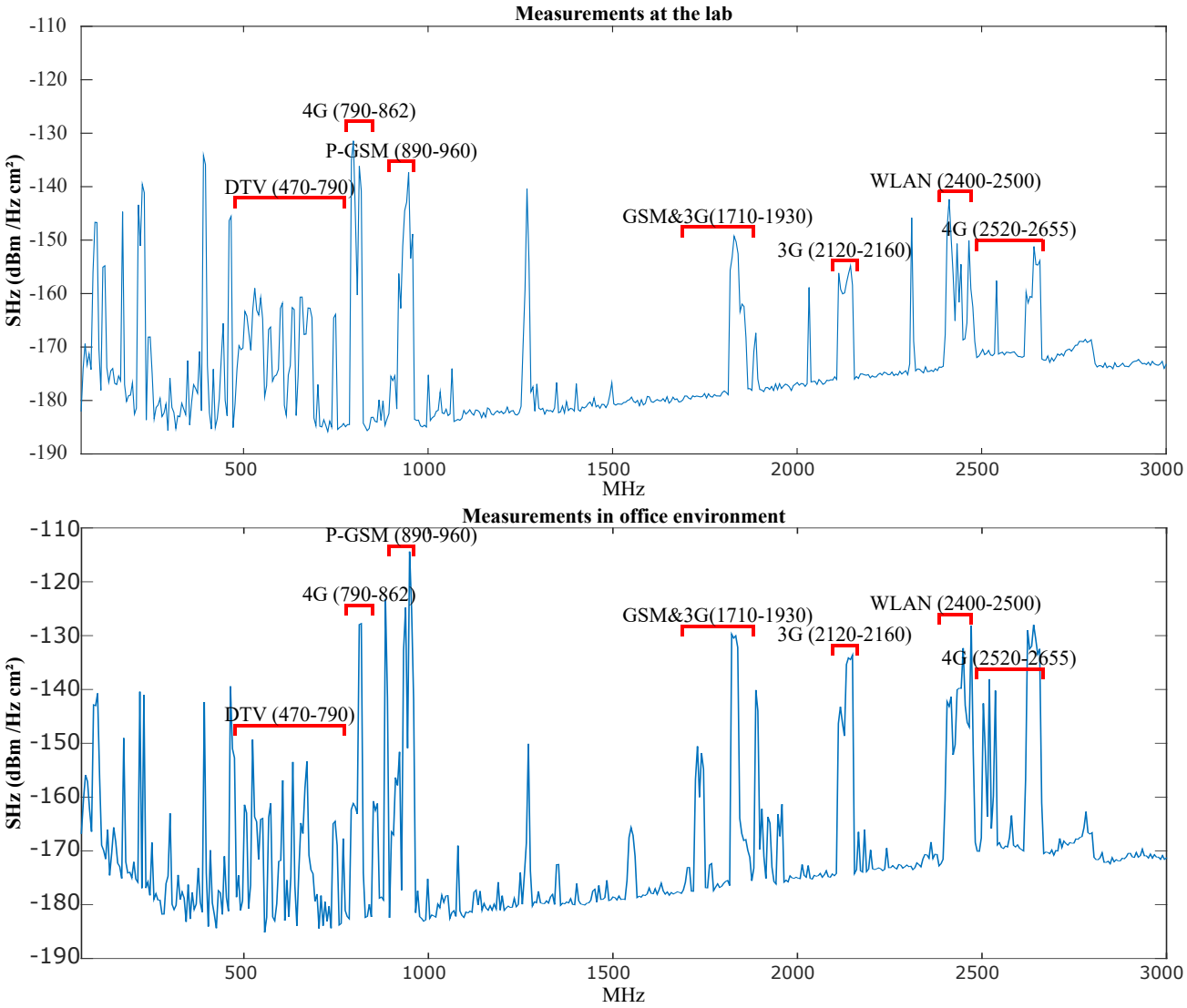


Figure 4.1: Measured power density at the lab (location 1) and office environment (location 2). 7 promising bands is marked in the figure.

Table 4.2: Average S_{BA} at four locations. Location 1 is the lab, while location 2,3 and 4 is typical office environments.

	Location 1	Location 2	Location 3	Location 4	Average
SBA $\left[\frac{nW}{cm^2}\right]$	0.003	0.006	0.0122	0.003	0.006

works (270 locations) and calculated S_{BA} in 8 bands (Table 4.3). All measurements are taken between 10.00 and 15.00 on weekdays since they expect the power be different from day time to evening time. This way they make sure comparison between measurements are valid. Each measurement is taken over 1 minute with multiple sweeps and max-hold meaning that the maximum power at each frequency is logged. Due to this, the reported band power density is overestimated. Also note that the survey is conducted before the full switch-over to digital tv and 3G making the measurements in these band an underestimate (4G not included in the survey). Table 4.3 show the results, and the GSM (1800) and GSM (900) is the most promising bands for RF-harvesting.

Table 4.3: Measured band power input in London underground network. MTx is mobile transmitter band and BTx is base station transmitter band [24].

Band	Frequencies (MHz)	Average S_{BA} (nW/cm^2)	Maximum S_{BA} (nW/cm^2)
DTV (during switch over)	470-610	0.89	460
GSM900 (MTx)	880-915	0.89	39
GSM900 (BTx)	925-960	36	1930
GSM1800 (MTx)	1710-1785	0.5	20
GSM1800 (BTx)	1805-1880	84	6390
3G (MTx)	1920-1980	0.46	66
3G (BTx)	2110-2170	12	240
WiFi	2400-2500	0.18	6

To determine if the electromagnetic radiation is a health hazard to humans, Post- og teletilsynet (now Nasjonal kommunikasjonsmyndighet) measured the power density at different locations in Norway [18]. The measurements were taken with max-hold over a period of 6 minutes at five different locations in Trondheim. The measured places can be found in Figure 4.2, and the results is shown in Table 4.4. The reports are available from the web page of Nasjonal kommunikasjonsmyndighet, see [18]. From these results it seems that GSM (900) and GSM (1800) bands is most suitable for RF-harvesting.

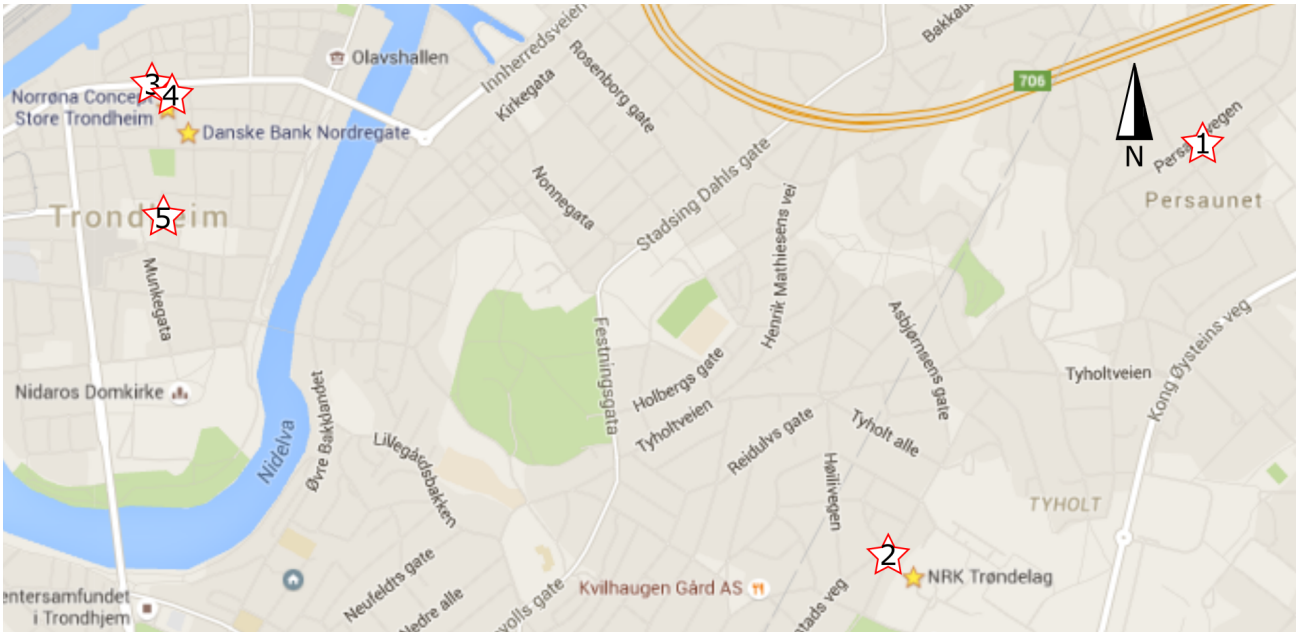


Figure 4.2: Map showing locations where the measurements of Post- og teletilsynet is taken. Map from google maps.

Table 4.4: Measurements by Post- og Teletilsynet conducted in Trondheim 2010. Na. means no measurement were conducted in the band. Measurements are from [18].

Report name	Bolig Trondheim	Bedrift Trondheim	Gatemåling Trondheim		
Location on map	1	2	3	4	5
Power density	S_{BA} (nW/cm^2)	S_{BA} (nW/cm^2)	S_{BA} (nW/cm^2)	S_{BA} (nW/cm^2)	S_{BA} (nW/cm^2)
FM (87.5-108MHz)	1.25	25	0	0	0
DAB (223-237MHz)	10	65	0.2	0.3	0.2
DTV (470-790MHz)	Na.	2.9	0.01	0.04	0.1
GSM (876-960)	12500	105	65.6	5880	135
GSM (1710-1875)	650	0.83	82.9	5436	67
WLAN (2400-2485)	Na.	0	0.4	0.13	0.8

Chapter 5

Simulations

5.1 Rectifier

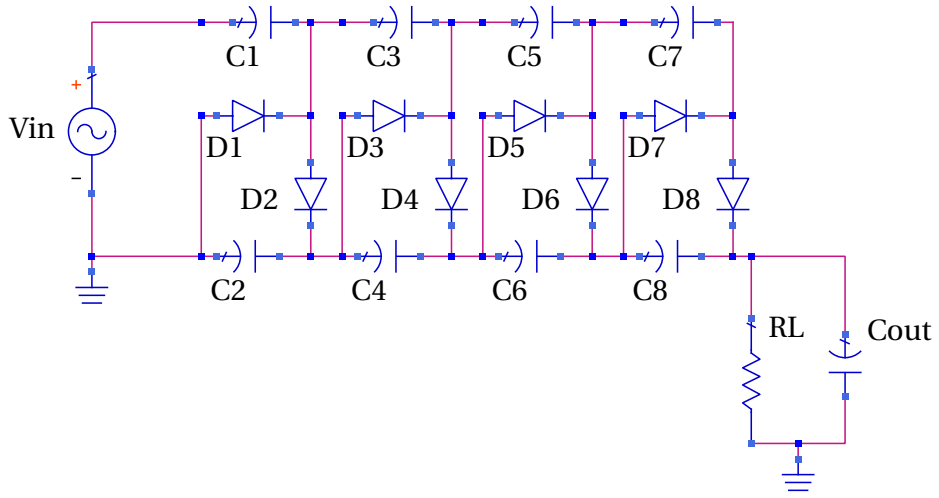


Figure 5.1: Circuit used in simulation of rectifiers, here shown with the 4-stage rectifier. The simulations are done with a sinusoidal source with frequency of 900 MHz, ideal capacitors and model of the HSMS-2850 diode manufactured by Avago Technologies[32].

The rectifier circuit is simulated in ADS to determine the behaviour. Simulations are done with transient analysis and the number of stages are varied from one to eight. As an example the 4-stage simulation circuit is shown in Figure 5.1. C_{out} is the capacitor storing the rectified energy and R_{L} model an attached load. The input of the rectifier is a sinusoidal voltage source with an impedance of 900 MHz. The diodes are HSMS-2850 from Avago Technologies and ideal capacitors are used because it reduces the simulation time. Components and values are stated in Table 5.1.

Table 5.1: Components used in simulations of n-stage rectifiers.

Frequency	900MHz
C1-C8	0.33 nF
Cout	6 nF
D1-D8	HSMS-2850

5.1.1 Capacitor values

The capacitor values are not arbitrary. A high capacitance value will give a low output ac voltage from one stage, a low capacitance value will result in a voltage drop during switching with the result of the rectifier not functioning properly. The value is also dependent on the choice of diode since the ac voltage is used to excite the diodes. Several capacitor values are simulated and the capacitor values that maximize the rectifier efficiency is found to be 0.33 nF. It is also found that the output capacitor need to be big enough to not have a big voltage swing during simulations. Increasing the value further lead to no change in the efficiency. A value of 6 nF is chosen since it is found to be just high enough to avoid an efficiency degrading voltage swing. By minimizing the value, the charging of this capacitor is reduced and therefore the simulation time is minimized.

5.1.2 HSMS-2850 linear circuit model

The diode used in the rectifier is HSMS-2850 manufactured by Avago Technologies. It is chosen due to the low forward voltage drop. A s-parameter model of this diode is provided in the HFDiode library which can be found in the component folder when ADS is installed. This model is used when simulating, but a linear circuit model is also useful to describe the behaviour of the rectifier. The model and parameters is shown in Figure 5.2 and is based on the datasheet provided by the manufacturer[32]. The equivalent impedance of the circuit is

Parameter	Units	HSMS-2850
R_x	Ω	25
C	pF	0.18
n		1.06
I_s	μA	3
T	°Kelvin	

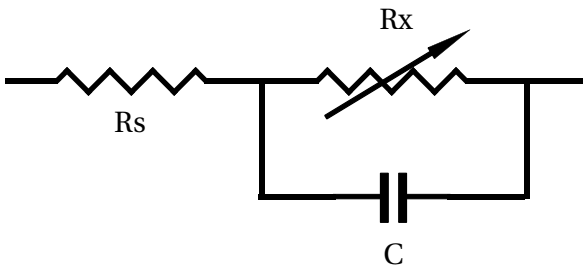


Figure 5.2: Equivalent linear circuit model of diode HSMS-2850 used in the rectifier[32].

$$R_{eq} = R_S + R_x \parallel C = R_S + \frac{R_x / j\omega C}{R_x + 1/j\omega C} = R_S + \frac{R_x}{1 + jR_x\omega C} = (R_s + \frac{R_x}{1 + (R_x\omega C)^2}) - j\frac{R_x^2\omega C}{1 + (R_x\omega C)^2} \quad (5.1)$$

where R_j is a variable resistor given by

$$R_j = \frac{8.33 \times 10^{-5} nT}{I_b + I_s}. \quad (5.2)$$

Here I_b is the bias current and the other variables is as stated in Figure 5.2. From this equation it is clear that when the current decreases the resistance increases and there is a higher loss in the diodes.

5.1.3 Maximum theoretical voltage gain

The maximum voltage gain of the rectifier can be simulated by deactivating the load resistor ($R_L = \infty$) while sweeping the input voltage. Since no power is dissipated in the load the output voltage will increase up to a maximum value. The resulting voltage with varying number of stages is shown in Figure 5.3 where input voltage is swept from 0 to 1 V. As can be seen there is a linear relationship between the input voltage and the output voltage of the rectifiers. To have some margin to the 2.5 V in the speciticationsan output voltage of 3 V is needed, and the input voltage to obtain this is shown in Table 5.2. With 7-stages the needed input voltage is 0.29 V, and for a 1-stage rectifier the input voltage need to be higher than 1 V. Please note that there is no restriction on the input power in these simulations. When there is limited input power these voltages are probably not obtainable.

Table 5.2: Needed input voltage to obtain 3 V output voltage for the different number of stages in the rectifier with ideal capacitors and resistors.

Number of stages	1	2	3	4	5	6	7
Input voltage [V]	>1	0.83	0.58	0.46	0.38	0.33	0.29

5.1.4 Input impedance of the rectifier

Between the antenna and the rectifier, a matching network is inserted to maximize the power transfer. To obtain maximum power transfer the output impedance of the matching network should be matched to the input impedance of the rectifier. But the impedance is not a constant, it varies with input voltage, input power, number of stages and the value of the output resistor. A through simulation is necessary in order to decide the optimal matching impedance.

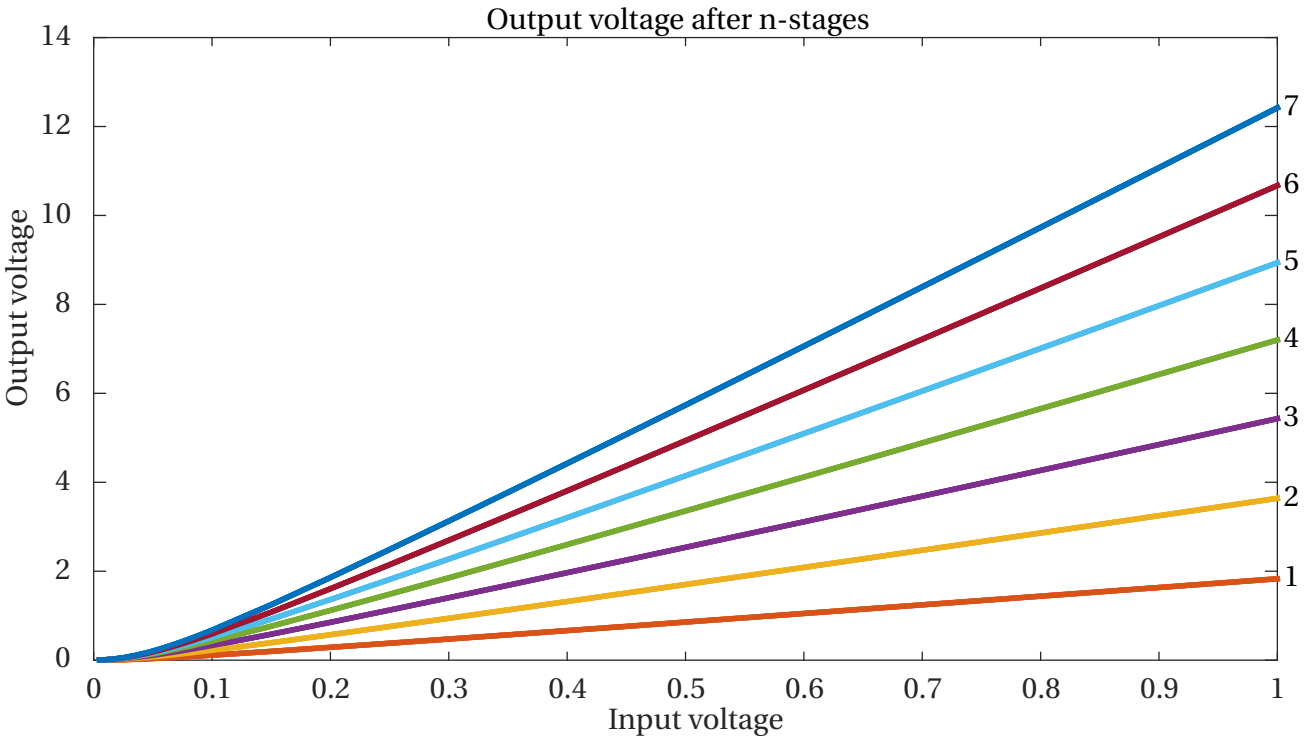


Figure 5.3: Maximum voltage of rectifier circuit with $R_L = \infty$.

The rectifier is simulated with transient analysis in ADS. The input voltage is swept from 0.1 to 0.5 V with the number of stages varying from one to eight. In addition to the input impedance the efficiency and output voltage is of interest.

A drastic change in the rectifier behaviour is expected with changing power at the input terminals. In measurements of the available power at underground stations in London [24](see also Chapter 4) the average power density in GMS900 band is found to be 36 nW/cm^2. As a starting point an antenna with effective area of 1000 cm^2 is assumed, giving an average power from the antenna of 36 μW. The harvesting system is designed to function at input powers below this since it then can function a larger portion of the time. It is simulated with input powers varying from 3 μW (-25 dBm) to 31 μW (-15 dBm), but with a focus on high efficiency at the lowest input powers.

There is a relationship between the load resistor (R_L), the output voltage (V_{out}), efficiency (η) and input power

$$R_L = \frac{V_{out}^2}{\eta P_{in}} \, [\Omega] \, . \tag{5.3}$$

By guessing the efficiency and output voltage of the rectifier at the different input powers the load resistor value is calculated and simulations are carried out. If these initial guesses give an input power within the range the result is used, otherwise a new resistor value is calculated and the sim-

ulation is restarted.

The relationship between the input impedance (R_{in}), input voltage (V_{in}) and input power (P_{rms}) is

$$R_{\text{in}} = \frac{V_{\text{in}}^2}{2 \times P_{\text{rms}}}, \tag{5.4}$$

showing that different combinations of input voltage and input power can give the same input impedance. To see how this effect the efficiency the input voltage is set constant and the input power is swept. The simulation data can be found in Table B.1 and B.2 in Appendix B.

Figure 5.4 show the resulting efficiency of the 8-stage rectifier. The input impedance is also measured and marked in each point (they will be discussed later). First look at the efficiency with input voltage set to 100 mV. With increasing input power the efficiency increases while input impedance decrease as expected from (5.4). This is shown in all measurements with constant input voltage. From the figure it is also evident that with decreasing input power a low input voltage is needed, otherwise the efficiency collapses. This is because the loss in the diodes increase when the currents decrease, as discussed in Section 5.1.2. Also note that the efficiencies are quite low, from 0.22 and down towards zero.

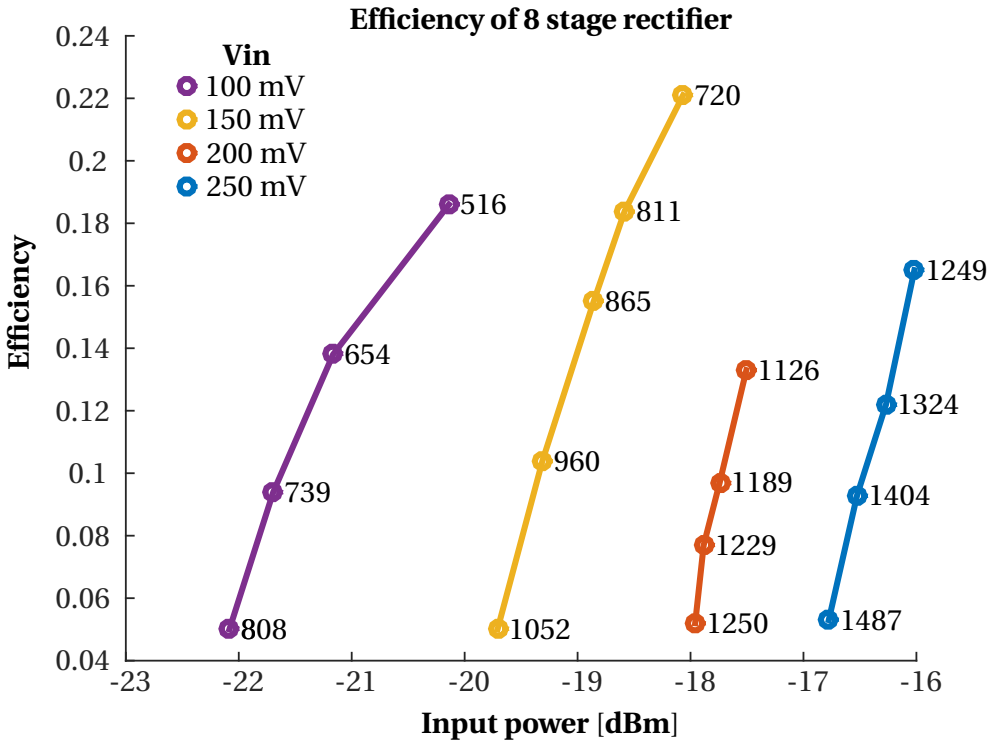


Figure 5.4: Efficiency of 8-stage rectifier with varying input power and input voltage set from 100mV to 250 mV. The measured input impedance [Ω] in each point is shown in the figure.

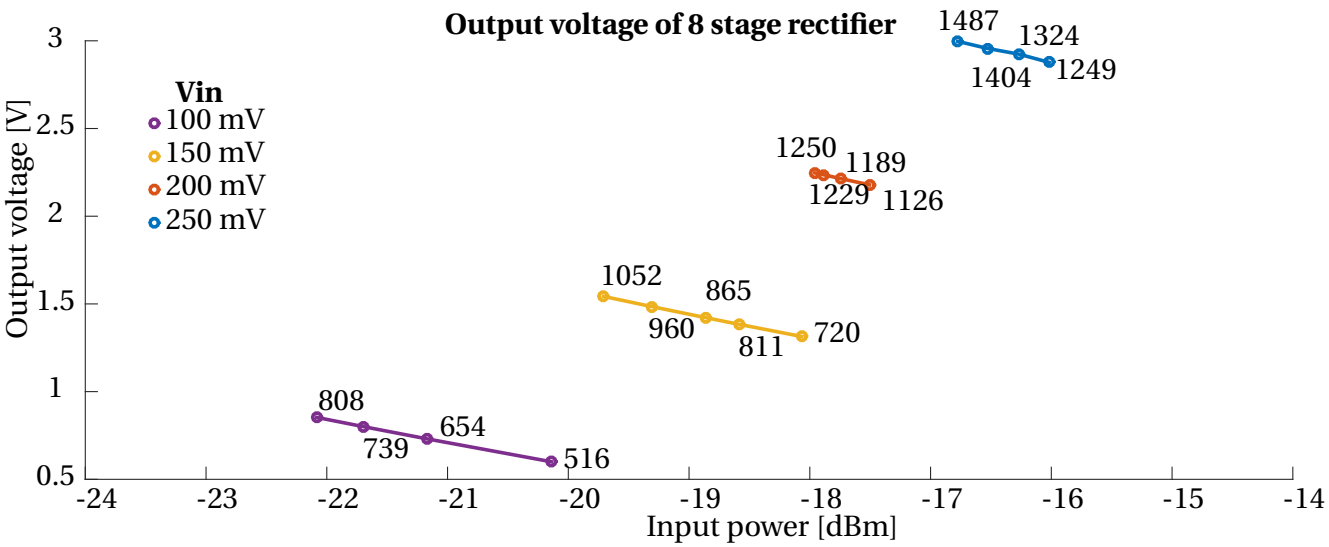


Figure 5.5: Output voltage of 8-stage rectifier with varying input power and input voltage set from 100 mV to 250 mV. The measured input impedance [Ω] in each point is shown in the figure.

The output voltage of the 8-stage rectifier is also simulated (Fig. 5.5). With increasing input voltage the output voltage also increase. This is expected since the rectifier works as a voltage amplifier. But this figure also shows the relationship between the input power and input voltage, with increasing input voltage the needed input power to rectify is higher. This is because the currents need to be high enough to overcome the diode threshold and with a set input voltage this can only be achieved by increasing the input power.
Another interesting observation from this figure is that for a given input voltage the output voltage increases when the input power decreases. The output voltage is given by

$$V_{\text{out}} = \sqrt{P_{\text{out}} \times R_{\text{L}}}, \tag{5.5}$$

and the voltage increase because R_{L} increase more than P_{out} decrease when the input power is lowered. High output voltage is desirable, but one must keep in mind that this comes at a high cost, the efficiency of the rectifier drop drastic at lower input power.

The 3-stage rectifier efficiency and output voltage is shown in Figure 5.6 and 5.7. Many simulations are done with Vin set to 150 mV to see how the curve develops over many input powers. It is interesting that the curve has a maximum between -20 and -19 dBm and decrease as the input power gets higher. Also note that the efficiency curve with Vin set to 250 mV show the same trend and that this also can be seen in the 8-stage rectifier. With more simulation points it is likely that they will also flat out before they decay. It is also seen that the output voltage increase (nearly)

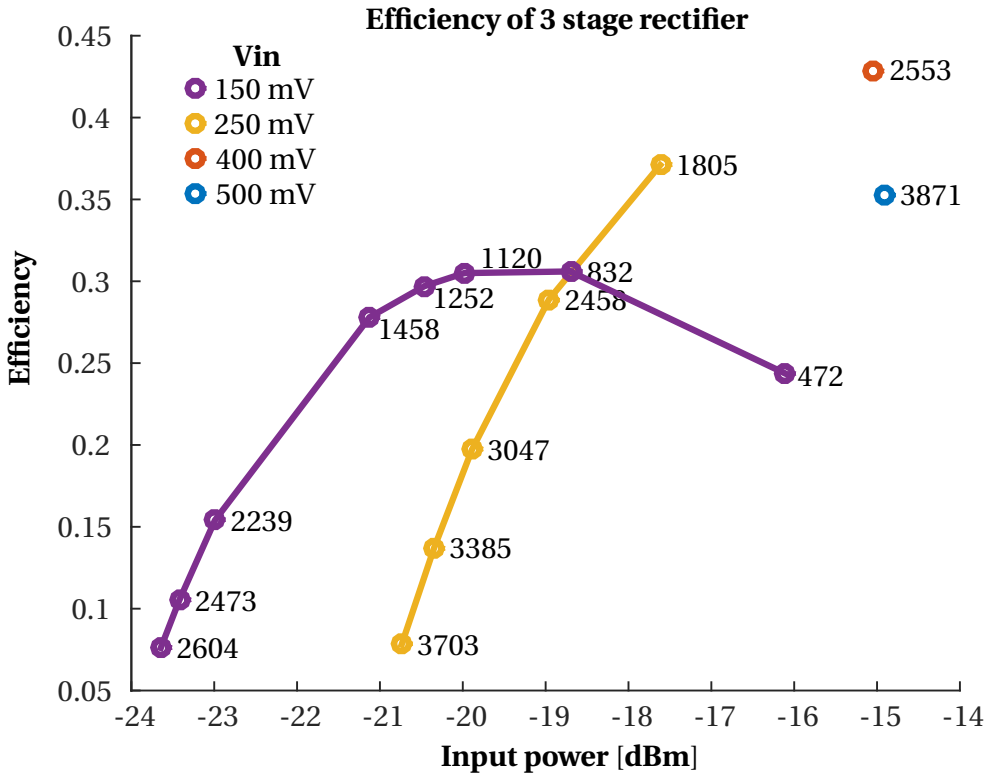


Figure 5.6: Efficiency of 3-stage rectifier with varying input power and input voltage set from 150mV to 500 mV. The measured input impedance [Ω] in each point is shown in the figure.

linearly when input power is decreased.

The main reason behind these simulations is to decide an input impedance for further simulations. With a set input voltage, the efficiency of the rectifiers increase when impedance is lowered, but the output voltage decrease. A tradeoff between efficiency and voltage amplification is needed. Another concern with input impedance is the impedance transformation (matching) network between the antenna and the rectifier. In general impedance matching is good at a (small) band around the center frequency and the farther the matching impedances is a part, the smaller the band. Since there is power available in a *band* around 900 MHz it is crucial that the band is wide enough.

The rectifier is simulated with the number of stages varied from 1 up to eight, but only a few simulations is done with other stages than 3 and 8. The results are summarized in Appendix B (Tab. B.1 and B.2). As a compromise between efficiency, output voltage and impedance transformation an input impedance of 1000 Ω is chosen for the rectifier. This is achievable in the matching network and should give both high voltages and efficiencies.

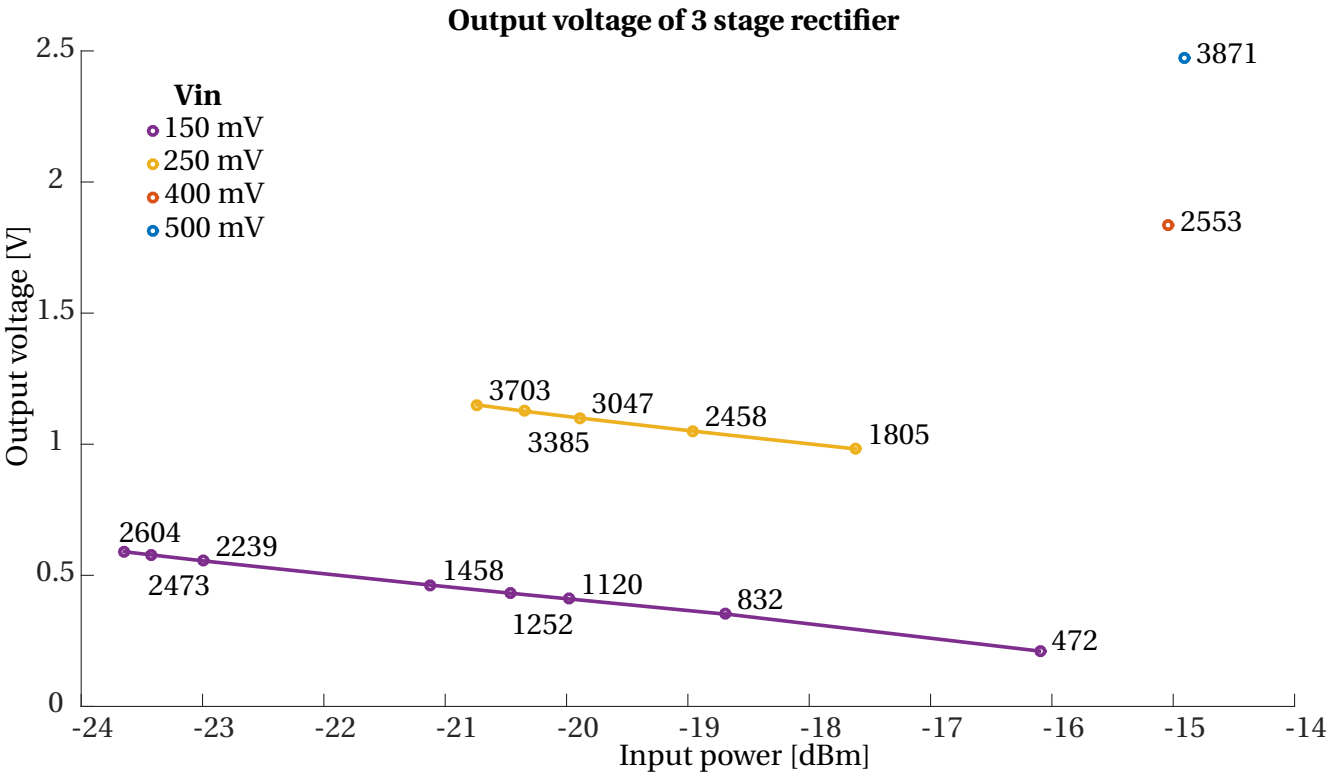


Figure 5.7: Output voltage of 3-stage rectifier with varying input power and input voltage set from 150 mV to 500 mV. The measured input impedance [Ω] in each point is shown in the figure.

5.1.5 Simulations with set input impedance

With the impedance set to 1000 Ω the rectifier is simulated again and a Thevenin equivalent circuit can be used to simplify simulations. The input voltage source is transformed to the equivalent circuit with an impedance set to 1000 Ω, as shown in Figure 5.8. By setting $V_{th} = 2V_{in}$ and $R_{th} = 1000\Omega$ it follows from Thevenin's theorem that maximum power is delivered if the impedance seen looking into the rectifier is 1000 Ω. Simulations are now done by finding the output resistor that give an input impedance of 1000 Ω. A 5 % deviation from the input resistance is allowed since these simulations are time consuming.

With the input impedance set there is now a constant relationship between input voltages and input powers, given by $P_{rms} = V_{in}^2 / 2R_{in}$. The voltages used and corresponding average input power is listed in Table 5.3.

The efficiency of the rectifiers with varying input power is shown in Figure 5.9 (the simulation data is found in Appendix C, Tab. C.1 and C.2). First notice that the efficiency with a 1-stage and 2-stage rectifier is lower than that of the 3-stage rectifier when the input power is below -16 dBm.

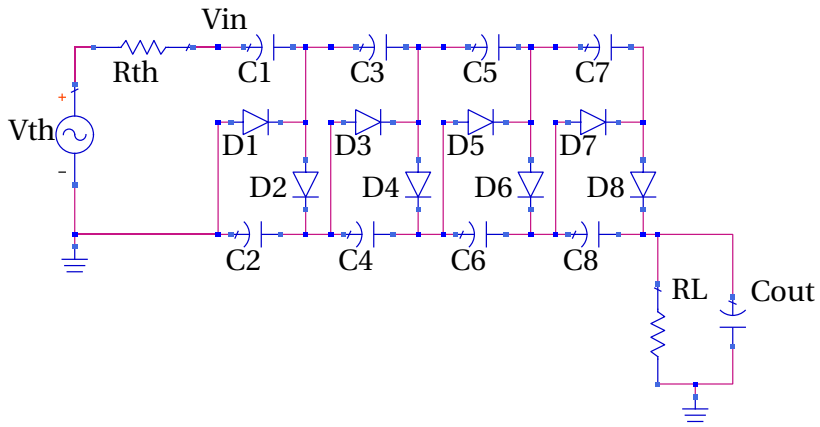


Figure 5.8: Thevenin equivalent of rectifier. R_{th} is set to 1000 Ω and other components as previously stated.

Table 5.3: Relationship between input voltage and average input power with input impedance set to 1000 Ω.

V_{in}	P_{rms} [dBm]	P_{rms} [μW]
0.100	-23	5.00
0.126	-21	7.94
0.159	-19	12.64
0.200	-17	20.00
0.282	-14	39.76

When the number of stages is increased from 3 up to 8 the efficiency drops again. It can also be seen that the efficiency is approximately linear in the different cases. Figure 5.10 show the output voltages when the input power is varied. As expected the output voltage increase when additional stages are added to the rectifier. As mentioned earlier an output voltage of 3 V is desired. The 8-stage rectifier can provide this voltage only above -15 dBm, but this is higher than the expected power available. With fewer stages this voltage is not obtainable.

A solution is to increase the number of stages, but how many stages would be needed? At -19 dBm the additional voltage when increasing the number of stages from 7 to 8 is 0.238 V (from Fig.5.10). Assume that the voltage gain by adding another one extra stage is 0.275 V. This is more than what can be expected and will provide an overestimate. The additional number of stages (m) to reach 3 V would be

$$m = \frac{3\text{V} - V_{\text{8-stage}}}{0.275} = \frac{1.4}{0.275} \approx 5, \tag{5.6}$$

where $V_{\text{8-stage}}$ is the output voltage of the 8-stage rectifier at -19 dBm. A 13-stage rectifier is needed

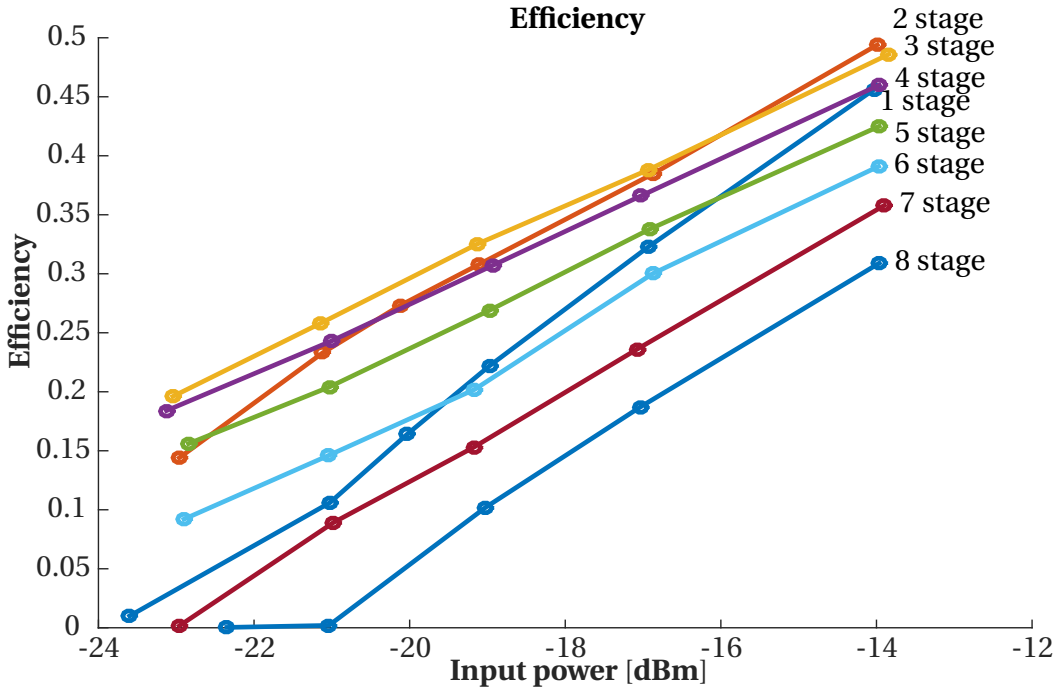


Figure 5.9: Efficiency of n-stage rectifiers with input impedance of 1000 Ω.

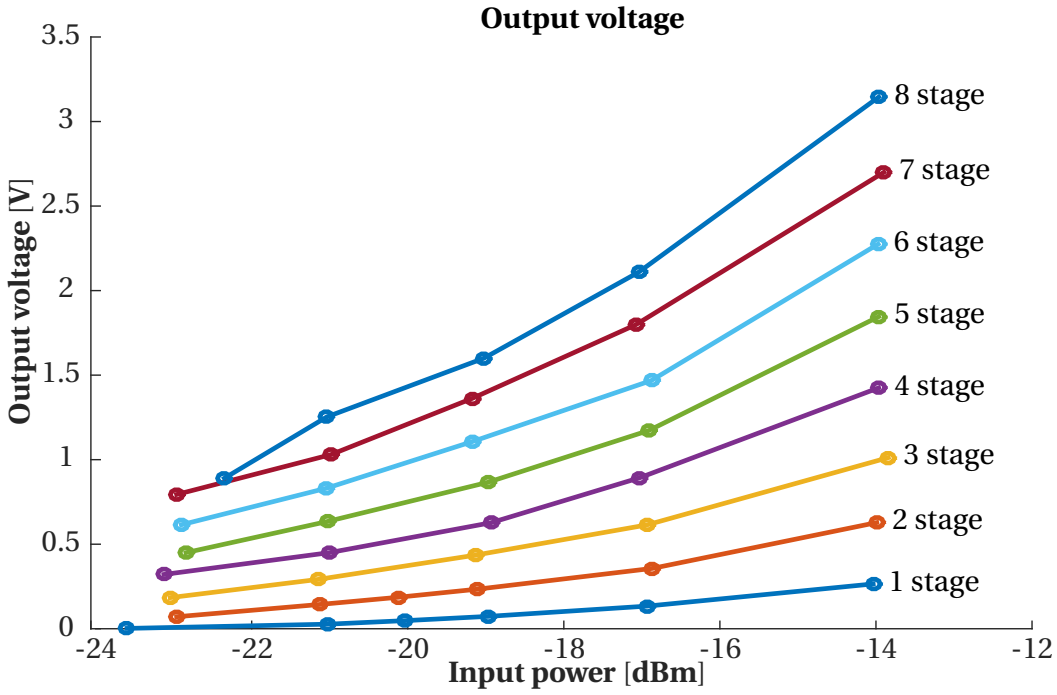


Figure 5.10: Output voltage of n-stage rectifiers with input impedance of 1000 Ω.

and assuming that additional stages would show the same trend in efficiency it is clear that the efficiency would be very low. And if the input power drop below -19 dBm it can not provide the needed output voltage. From this it is obvious that another voltage amplification is needed to amplify the voltage to a usable value. This can be done by a boost converter, discussed later.

The performance of a boost converter depends on how much it need to amplify the voltage. When the amplification increase the efficiency decrease. Figure 5.9 also show that the efficiency of the rectifier decrease when the amplification (number of stages) increase. It is important to see where voltage should be amplified to maximize the total efficiency. It is evident that the 1- and 2-stage rectifiers should not be used since a 3-stage rectifier is better with both higher output voltage and efficiency. Therefore the 1- and 2-stage rectifiers is discarded.

Figure 5.11 show the efficiency of the rectifiers from 3- to 8-stages, with the measured output voltage in each point added. Deciding the number of stages that should be used is as before a trade-off between output voltage and efficiency and will depend on the efficiency of the boost converter.

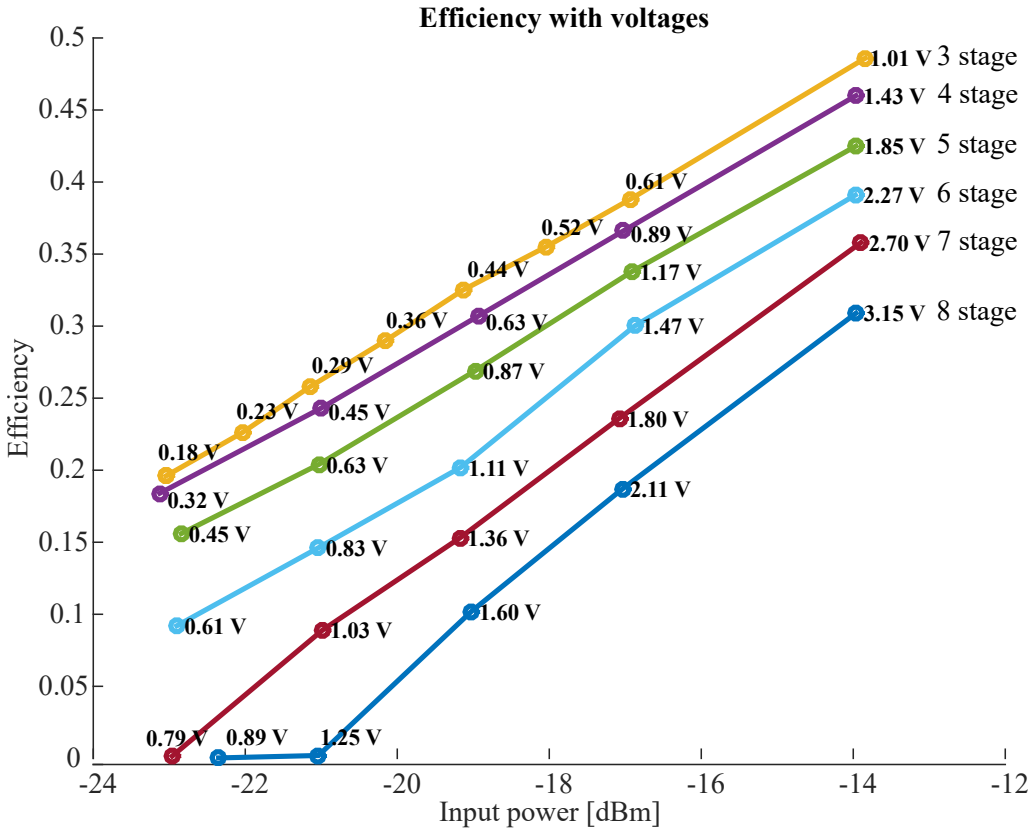


Figure 5.11: Efficiency of n-stage rectifiers with output voltages in each point. The input impedance is 1000 Ω.

5.2 Simple DC-DC boost converter

The rectifier simulations revealed that the 3-stage rectifier yield the highest efficiency and the output of this rectifier is chosen as the input to the boost converter. The working principle of the boost converter shown in Figure 5.12 is described in Section 3.2.1. Figure 5.13 show the voltage on the input and output capacitor over five charge cycles (left) and a close up of the voltages in the switching period (right). This is a simulation of the boost converter with the Thevenin equivalent of the 3-stage rectifier with input power of -19dBm. Other simulation parameters can be found in the caption of the figure. First have a look at what happens in the time around the switching period. When the switch turns on a current starts going from the input capacitor to ground, discharging the input capacitor. This can be seen as a voltage drop on the input capacitor. When the switch turns off the voltage over the output capacitor starts increasing, since the current that was flowing in the inductor is now charging it up. But note that the charge time of the input capacitor is large compared to the on time of the switch, due to the low input power. The ratio of on time versus period is called the duty cycle and is here

$$D = \frac{t_{\text{on}}}{T} = \frac{2.1\mu\text{s}}{9930\mu\text{s}} \approx 0.00021, \tag{5.7}$$

in other words, the time spent charging up the input capacitor is around 5000 times longer than the time it actually amplify the voltage. This is something that need to be considered when choosing components for the circuit.

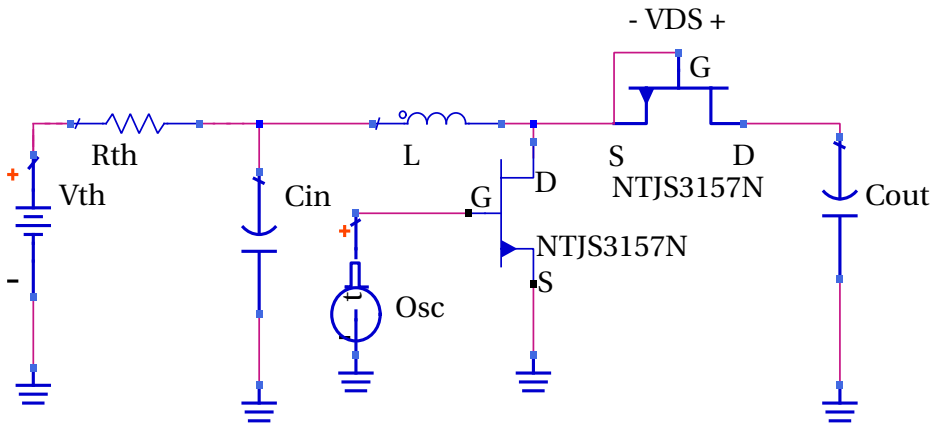


Figure 5.12: Simple DC-DC boost converter.

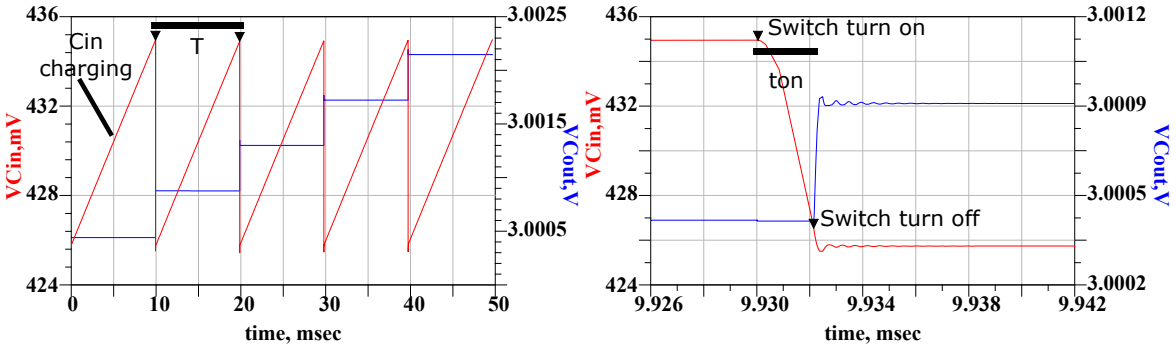


Figure 5.13: The voltages on the input and output capacitor in the boost converter. Right show a close up of the voltages around t_{on}. The period T and on time t_{on} is marked in the figure. (Simulated in ADS with L=8.2μ, $t_{on} = 2.1\mu$s, T = 9930μs, $V_{th} = 2 \times 0.435$ and R_{th}=47.6kΩ.)

5.2.1 Selection of components

Selection of switching transistor

Two main concerns are considered for the switching transistor, switching time and on resistance (R_{on}). The switching time is important since the resistance in the transistor changes between infinity and R_{on}, giving high loss under transitions. R_{on} is the loss in the circuit when the switch is on. The transistor chosen is NTJS3157N manufactured by On Semiconductor, which is an n-channel enhancement mode MOSFET [28]. During simulations the on resistance is found to be less than 10mΩ, and the switching time stated in the datasheet is 12ns and 11ns for the rise and fall time respectively (at $V_{GS} = 4.5$ V).

Oscillating circuit

The oscillating circuit that control the switch is beyond the scope of this thesis and will need to be designed in order to have a standalone system. It is simulated with a step voltage source with amplitude of 1.5V, rise- and fall time of 30ns, on time set by t_{on} and period of T. Please note that losses in the oscillating circuit is not considered when efficiency is simulated, making the efficiencies of the boost converter an overestimate of actual performance with an oscillating circuit.

Selection of diode

As stated previously the boost converter will spend most of its time in idle mode, charging up the input capacitor. A critical aspect in this mode is to preserve the energy stored on the output capacitor. In idle the voltage on the output capacitor is charged above the input voltage, reverse biasing

the diode ($V_{DS} > 0$). Although the diode is reverse biased a small current will go from the output capacitor and back into the boost converter. This current will go through the switch and is a loss. It is important to minimize this leakage current, therefore different diodes are simulated.

Five candidates is simulated, two Schottky diodes and three n-channel enhancement mode MOSFETs diode connected. The simulations is done by reverse biasing the diodes and measuring the currents. The simulations (Tab. 5.4) show that diode coupled transistors have much lower leakage current than Schottky diodes. NTJS3157N is the best transistor at all voltages except 0.8 V, with ZXMN2AMC as the next best choice. Based on this NTJS3157N manufactured by Diodes Incorporated is chosen.

Table 5.4: Leakage currents of different diodes, both Schottky diodes and diode connected transistors. NTJS3157N have the lowest leakage current at all voltages except V_{DS} = 0.8 V. This is used in the design. Manufacturers: BAT43W (Diodes Incorporated [14]), HSMS-2850 (Avago Technologies [32]), DMN2300UFB4 (Diodes Incorporated [15]), NTJS3157N (ON Semiconductor [28]) and ZXMN2AMC (Diodes Incorporated [13])

	Leakage current [nA]				
V_{DS}[V]	BAT43W	HSMS-2850	DMN2300UFB4	NTJS3157N	ZXMN2AMC
0.8	-80139.47	-3002.50	-13.80	-0.30	-0.27
1.4	-80167.18	-3005.50	-16.76	-0.31	-0.48
2.0	-80191.39	-3008.51	-20.32	-0.33	-0.68
2.6	-80215.60	-3011.51	-24.60	-0.34	-0.88
3.2	-80239.81	-3014.51	-29.76	-0.36	-1.08
3.4	-80247.89	-3015.56	-31.70	-0.36	-1.15

Selection of inductor

Boost converter efficiency and output voltage is the two main concerns when selection the inductor. The size of the inductor is discussed in 3.2.1 where it is assumed that a big inductor value will minimize the loss (3.8).

Ferrite chip inductors manufactured by Coilcraft (1008AF 2520) is tested with the boost converter due to their high inductance to frequency ratio. Inductance values ranging from 1.1 μH up to 8.2 μH is simulated. Simulations are first carried out with the output capacitor charged to 2.5 V. The efficiency at this voltage is especially important since the load is assumed to work around this voltage.

With a set inductor value the efficiency of the boost converter is found by finding the best switch on time (t_{on}) and the switch period (T) that corresponds to this value. But since these two

variables are dependent on each other one would need to simulate each inductor value a number of times to be sure that the best solution is found. These simulations are (very) time demanding, so another simulation scheme is developed.

The switching can be calculated with

$$T_{\text{calc}} = \frac{E_{\text{used}}}{P_{\text{in}}} \tag{5.8}$$

where E_{used} is the power drawn from the input capacitor in the switching period and P_{in} is the input power. The efficiency (η) is calculated from

$$\eta = \frac{E_{\text{Cout}}}{E_{\text{in}}} \tag{5.9}$$

where E_{in} is the energy going into the circuit and E_{Cout} is the net energy charged onto C_{out}. (both when switching and loss in idle mode). It is given by

$$E_{\text{Cout}} = E_{\text{charged}} - E_{\text{loss}} = E_{\text{charged}} - V_{\text{DS}} \times \grave{\text{I}}_{\text{DS}} \times T_{\text{calc}} \tag{5.10}$$

where V_{DS} is the voltage over the diode, I_{DS} is the leakage current and T is the period calculated above. The simulations are done by setting a short period T (much smaller than in the final design) and sweeping t_{on}. The energy drawn from the capacitor (E_{used}) and input power (P_{in}) is measured and T_{calc} is calculated from (5.8). T_{calc} can then be used to calculate the efficiency when the energy charged into the capacitor is measured.

The simulated efficiencies (Tab. 5.5) indeed show that the highest inductor values indeed yield the highest efficiencies. Especially 8.2, 6.8 and 5.8 μH show promising characteristics, each having the highest efficiency at different input powers. New simulations of these three inductor values is done with an initial output voltage of 3 V (Tab. 5.6). These simulations show that the 5.8 μH inductor give slightly lower efficiency, and that 6.8 μH and 8.2 μH show very low variations. Based on these simulations both inductors will be a good choice and the highest value is chosen. By choosing this the current is kept at a minimum.

5.2.2 Boost converter simulation results

The boost converter is simulated to determine the performance. The 8.2 μH inductor previously discussed is used, together with the NTJS3157N used as both a transistor and as diode. Ideal capac-

Table 5.5: Simulated efficiency of boost converter with different size inductors from Coilcraft (1008AF 2520[7]). The simulation circuit is shown in Fig 5.8. Initial output voltage of the boost converter is 2.5 V. Highest efficiencies at different input powers is marked in bold.

			Inductor value [μH]								
V_{Cin} [mV]	R_{th} [kΩ]	dBm	8.2	6.8	5.8	4.7	3.9	3.3	2.7	1.5	1.1
184	35.0	-30.12	54.3	**57.9**	54.0	52.3	52.9	45.6	50.2	40.0	42.2
232	38.0	-28.50	58.9	60.0	**62.2**	55.7	56.3	50.0	54.1	46.2	45.8
292	43.0	-27.03	62.9	62.2	**66.5**	62.3	59.7	54.1	58.7	49.9	49.4
357	45.5	-25.53	64.5	**70.4**	62.2	60.6	61.5	56.0	60.1	53.4	51.9
435	47.6	-24.02	**72.3**	65.7	64.6	63.7	63.7	58.6	61.0	53.9	54.7

Table 5.6: Simulated efficiency of boost converter with most promising inductors from Coilcraft (1008AF 2520[7]). The simulation circuit is shown in Fig 5.8. Initial output voltage of the boost converter is 3.0 V. Highest efficiencies at different input powers is marked in bold.

			Inductor value [μH]		
V_{Cin} [mV]	R_{th} [kΩ]	dBm	8.2	6.8	5.8
184	35.0	-30.12	**55**	54.69	53.89
232	38.0	-28.50	56	**57.81**	56.34
292	43.0	-27.03	60	**60.9**	57.37
357	45.5	-25.53	**62**	61.83	60.38
435	47.6	-24.02	63	**63.81**	62.63

itors are used since the capacitors are not a part of the boost converter. Their values are $V_{in} = 10\mu$F and $C_{out} = 20\mu$F. Ideal capacitors also shortens the simulation time. The simulation scheme described in Section 5.2.1(Selection of diode) is used to find t_{on}.

As an input to the boost converter the output voltage and output power of the 3-stage rectifier is used (Tab. 5.7). The efficiency of the boost converter (Fig. 5.14) is highly dependent on the voltage charged onto the output capacitor. When the voltage is below 1 V the efficiency is low (less than 51%). When the output voltage is increased up to 2 V the efficiency increase, beyond this the increase in efficiency is marginal. At an output voltage of 2 V the efficiency varies from 52% at -30 dBm input power up to 61% at -24.02 dBm. Please note that this efficiency does not take into account the loss in the oscillating circuit needed to run the transistor, making it an overestimate of the net performance. The interested reader is referred to Appendix D for simulation data and simulation parameters. The boost converter is able to charge the output capacitor up to 2.5 V at all input powers investigated.

Figure 5.15 show currents and voltages in the boost converter during switching. Input power to the rectifier is -27 dBm, which corresponds to the output of the 3-stage rectifier with input power

Table 5.7: Thevenin voltage V_{th} and Thevenin resistance R_{th} and corresponding power used as input to the boost converter. These values correspond to the output values of the 3-stage rectifier when the input is between -19 and -23 dBm.

Input power [dBm]	V_{th} [V]	R_{th} [kΩ]
-24.02	0.435	47.6
-25.53	0.357	45.5
-27.03	0.292	43.0
-28.50	0.232	38.0
-30.12	0.184	35.0

of -21 dBm. At t=0 the switch opens and a current start going through the inductor (5.15a). After 2.7 μs the switch closes and the current is forced through the diode (I_{out}) resulting in a voltage over the switch (V_{DS}). This is charging up the output capacitor. A ringing voltage is also observed after the switch is closed. The gate current of the switch (5.15b) suggest that this comes from discharging the parasitic capacitances of the switch. When the switch is open energy is drawn from the input capacitor, resulting in a voltage drop (5.15c). Between switching the input capacitor is charged up

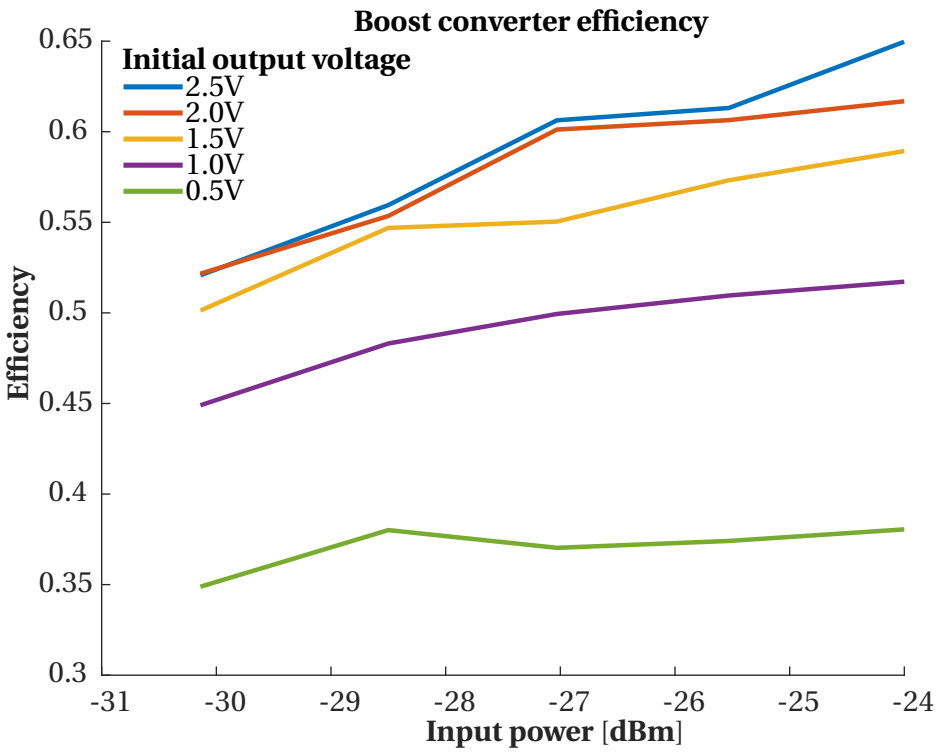
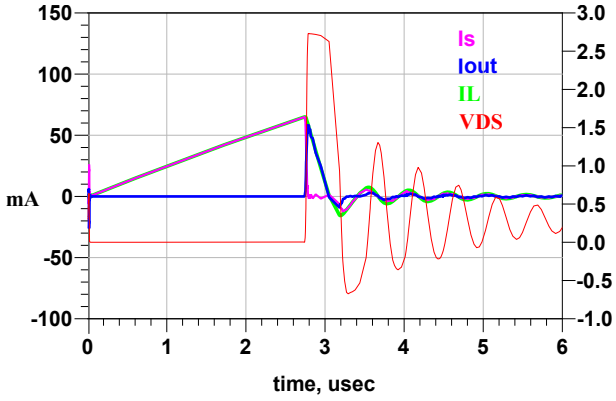
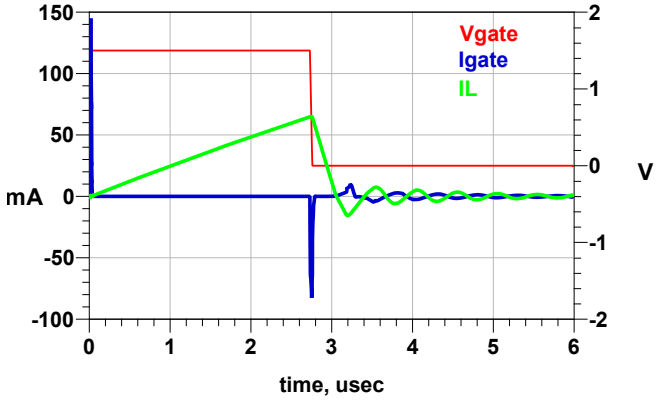


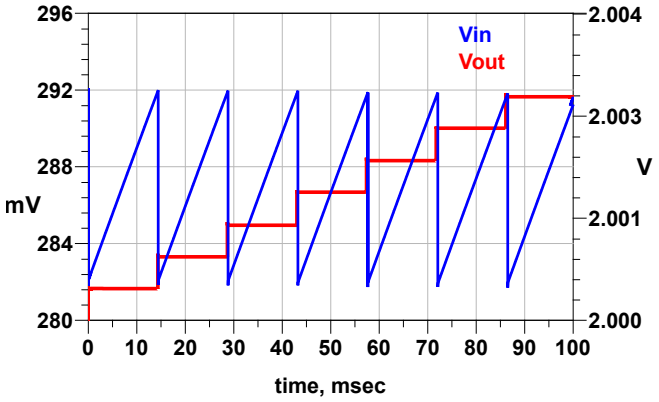
Figure 5.14: Efficiency of boost converter at different input powers. The boost converter is simulated with different voltages charged onto the output capacitor.



(a) Current in switch, inductor, into output capacitor and voltage over switch.



(b) Transistor gate voltage, transistor gate current and inductor current.



(c) Voltage on input and output capacitors.

Figure 5.15: Currents and voltages in the boost converter during switching. Ringing in the currents is due to charging of parasitic capacitances. Input power is -27 dBm with input voltage of 0.292 V and initial output voltage is 2 V.

to the initial voltage again. Charging of the output capacitor is also shown as an increase in the voltage.

5.2.3 Loss analysis

Simulations are done to analyse the loss in the boost converter. The boost converter is simulated with an input power of -25.5 dBm and an initial output voltage of 2 V. The loss in the inductor, switch and diode is measured through an entire cycle. Also of interest is the loss when switching, in the region where the current is ringing and the leakage after the ringing dies out. The different regions is marked in Figure 5.16. The total efficiency of the boost converter is 58.49 %. Simulations reveal (Tab. 5.8) that the diode is the lossiest component. 21.23 % of the total power is lost in the

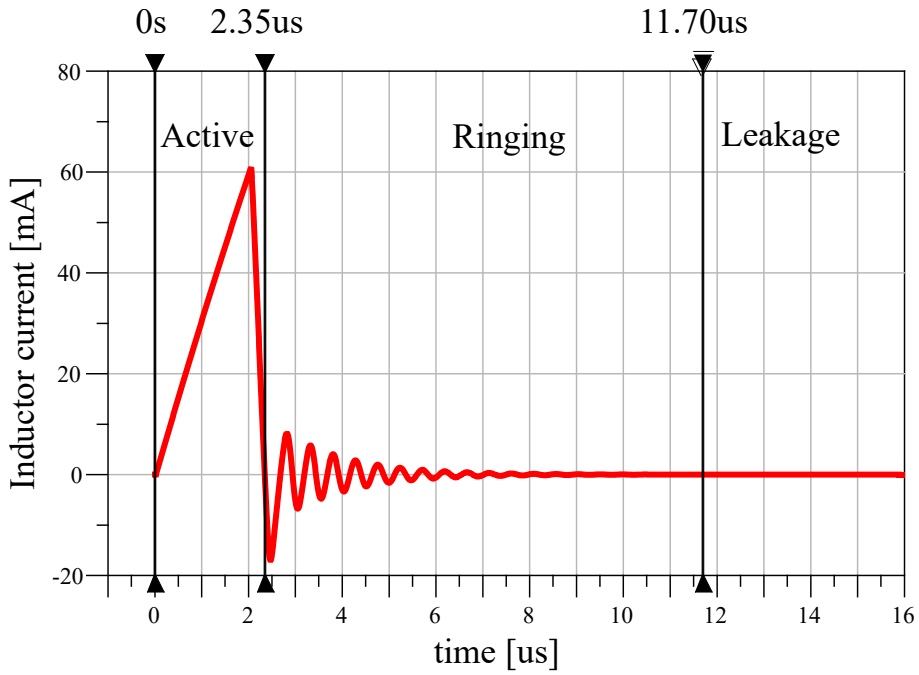


Figure 5.16: Figure showing the current in the inductor with the three regions of interest in the loss analysis is marked. Active region is the ideal charge and discharge of the inductor, ringing region is the current due to discharging of parasitic capacitors and leakage region is the region with leakage losses when the ringing stops. This region lasts until the next cycle start after 8.91 ms.

diode, 16.24 % in the inductor and 4.03 % in the switch. It is also found that 4.14 % of the total power is lost in the ringing region. The loss in the leakage region is less than 0.02 %.

Table 5.8: The amount of the input power lost in the different components of the boost converter. Both the total loss and the loss in the different regions is listed. Boost converter efficiency: 58.49 %, input power: -25.5 dBm, initial output voltage: 2 V.

	Total [%]	Active	Ringing	Leakage
Inductor	16.24	12.97	3.27	0.00
Switch	4.03	3.82	0.20	0.01
Diode	21.23	20.56	0.67	0.01

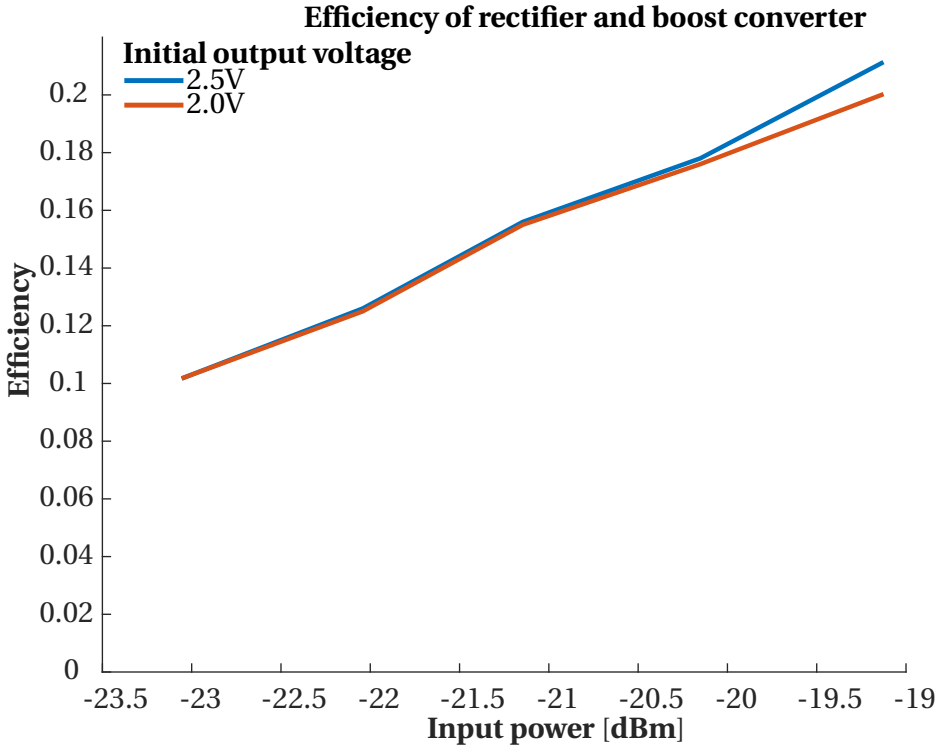


Figure 5.17: The total efficiency of the rectifier and boost converter with varying input power. Efficiency calculated by multiplying the efficiencies of the rectifier and boost converter in the different data points.

5.3 Rectifier and boost converter performance

The efficiency of the 3-stage rectifier and boost converter (Fig. 5.17) is found by multiplying the efficiency of the rectifier with the efficiency of the boost converter. Efficiencies at output voltages of 2.0 and 2.5 V are shown since this is the voltage a typical load will use. Total efficiency at lower voltages can be found in Appendix E. The efficiency is increasing approximately linear with increasing input power, and there is little deviation between the efficiency with the two output voltages, except at -19 dBm. The efficiency is 21.1 % at -19 dBm and decreasing to 10.2 % at -23 dBm (with an output voltage of 2.5 V). The output power at different input powers is shown in 5.18. The output power is 0.5 μW at -23 dBm and increasing up to 2.5 μW at -19 dBm.

5.3.1 Charge time with rectifier, boost converter and power managing circuit

A microcontroller from Nordic Semiconductor (nRF52) is used as a load for the harvesting system. The energy needed to send two packets of data over Bluetooth Low Energy (including turning the

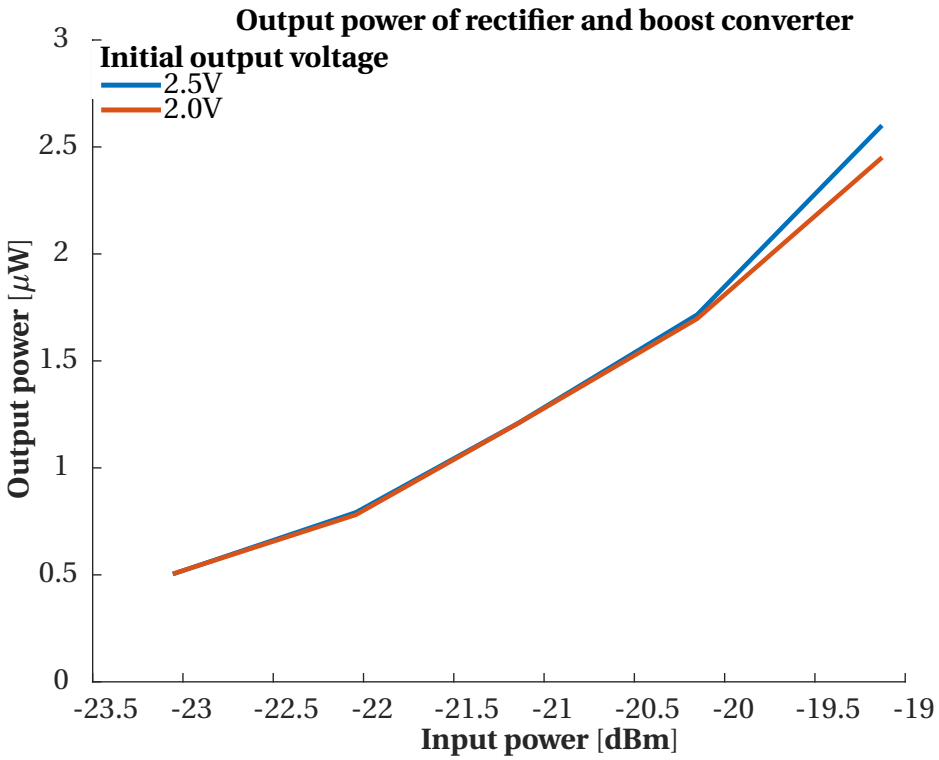


Figure 5.18: Charged power onto the output capacitor from the rectifier and boost converter at different input powers. Input power is calculated by multiplying the efficiency with the input power.

chip on) is calculated in Section 3.3 and found to be 114 μJ (3.10). The charge time can be calculated with

$$t_{\text{charge}} = \frac{U_{\text{cycle}}}{P_{\text{out}} - P_{\text{oscillator}} - P_{\text{Power managing loss}}} \tag{5.11}$$

where U_{cycle} is the energy needed, P_{out} is the harvested power without oscillator loss, $P_{\text{oscillator}}$ is the power consumption on the oscillator and $P_{\text{Power managing loss}}$ is the loss in the power managing circuit found to be 357 nW (3.25). The loss in the oscillator network will here be modelled as a percentage of the total harvested power at -19 dBm input power. The loss in the oscillator is then

$$P_{\text{oscillator}} = P_{\text{out at -19 dBm}} \times L_{\text{Loss factor}}. \tag{5.12}$$

The charge time with different losses is shown in Table 5.9 (calculated with an output voltage of 2 V). With no loss the charge time is 55 seconds at -19 dBm and increasing up to almost 13 minutes at -23 dBm. With a 5 % loss the charge time is increased up to 66 minutes at -23 dBm. The oscillation network power consumption that gives a net charge of zero to the load is also calculated (Tab. 5.10).

Table 5.9: Charge time needed at different input powers to the rectifier before the load (nRF52) can send two packets of data with Bluetooth Low Energy. The loss in the oscillator circuit is modelled with $L_{\text{Loss factor}}$, see (5.12). Simulation results with 2 V output voltage is used.

		Charge time [min:sec] at different input powers				
$L_{\text{Loss factor}}$)	$P_{\text{oscillator}}$ nW	-19 dBm	-20 dBm	-21 dBm	-22 dBm	-23 dBm
1.00	0	00:55	01:25	02:14	04:29	12:36
0.95	122	00:58	01:34	02:37	06:18	66:18
0.90	240	01:02	01:44	03:08	10:35	∞
0.85	367	01:06	01:57	03:56	33:11	∞
0.80	489	01:11	02:14	05:16	∞	∞
0.70	733	01:24	03:08	16:17	∞	∞
0.60	978	01:43	05:15	∞	∞	∞
0.50	1222	02:12	16:07	∞	∞	∞

Table 5.10: Power consumption in the oscillation network which give a net charge of zero delivered to the load at different input powers. Calculated with an output voltage of 2 V.

Input power	-19 dBm	-20 dBm	-21 dBm	-22 dBm	-23 dBm
$P_{\text{oscillator}}$ nW	2087	1340	850	424	151

5.4 Number of rectifier stages to maximize efficiency

From the rectifier simulations it was implied that a 3-stage rectifier would be the best tradeoff between efficiency and input power. Due to this the output of the 3-stage rectifier was used as an input to the boost converter. But could another number of stages be a better solution?

The total efficiency of the rectifier and boost converter is

$$\eta_{\text{Tot}} = \eta_{\text{Rect}} \times \eta_{\text{Boost}} \tag{5.13}$$

where η_{Rect} and η_{Boost} is the efficiency of the rectifier and boost converter respectively. Simulations of the boost converter efficiency with input voltage and input power corresponding to the output of the 4- and 5-stage rectifiers are done to compare the total efficiency (Tab. 5.11). With input power of -19 dBm and -21 dBm the 3-stage rectifier give the highest efficiency, while at -23 dBm the 4-stage rectifier show slightly better performance. The 5-stage rectifier have the lowest efficiency at all input powers. It is assumed that adding more stages will result in even lower efficiencies, so they are not simulated.

Table 5.11: Efficiency of rectifier and boost converter with the number of stages in the rectifier varied from 3 to 5.

Number of stages (n)	Input power [dBm]	$\eta_{\text{Rect n-stage}}$	$\eta_{\text{Boost n-stage}}$	$\eta_{\text{Tot n-stage}}$
3	-19	0.325	0.617	0.200
	-21	0.258	0.601	0.155
	-23	0.196	0.522	0.102
4	-19	0.307	0.646	0.198
	-21	0.243	0.633	0.154
	-23	0.184	0.599	0.110
5	-19	0.269	0.664	0.179
	-21	0.204	0.653	0.133
	-23	0.156	0.625	0.098

Chapter 6

Discussion

Performing transient analysis is time consuming at high frequencies and different approaches to reduce the computation time is taken. This will affect the simulation results. Charging the minimum calculated storage capacitor (111 μF) up to 2 V will take 17 seconds if the input power is -19 dBm and the efficiency is 100 %. To simulate this at 900 MHz the minimum simulation points is 15.3 billion and the stored simulation data will be much higher. It is obvious that the computation time need to be reduced drastic which will introduce uncertainty in the simulations. One way of doing this is to reduce the frequency of the input signal, as is done in the boost converter.

In the rectifier the frequency cannot be reduced since the diodes are frequency dependent. The capacitor values used in the rectifier is chosen as low as possible to reduce the charge time needed. The values are reduced until the behaviour of the rectifier change, which was observed with capacitor values of 0.1 nF. Capacitor values of 0.33 nF is chosen for some margin. It is possible that higher capacitor values yield better performance, but it is assumed that the deviation will be low. Initial voltages in all nodes of the rectifier is also included in simulations. It is done by guessing the initial voltages in each node and evaluating how they change when the simulation is started. By doing this until there is no change in any node the steady state is found. It is possible that these initial conditions put the rectifier in a state that cannot be reached if all voltages initially are zero, but it is considered unlikely.

The boost converter is simulated with a DC source as input, thus reducing the simulation frequency. This is a simplification since the output of the rectifier will have a small AC voltage in addition to the DC contribution. It is assumed that only minor changes will occur if the AC voltage is included, since the input of the rectifier is actually varying due to charge and discharge of the input capacitor. A simulation scheme is also used to find the optimal on time (t_{on}) of the boost converter switch without the need to find the period of all values of t_{on}. This will introduce uncer-

tainty that cannot be disregarded, as other values of t_{on} could yield better results. Since t_{on} is also simulated with steps of 0.1 μs it is likely that the maximum efficiency is not found. This element of uncertainty is accepted since it is expected that the accuracy in a realized oscillation network will be limited. If the precision in the oscillation network is higher than 0.1 μs the simulations should be recalculated with a higher resolution.

6.1 Rectifier

A matching network is needed between the low impedance antenna (~50 Ω) and the high impedance rectifier. The rectifier is simulated with the number of stages varied from one to eight to determine the impedance. Based on these simulations it was found that the input impedance of the rectifier should be 1000 Ω. They showed that a higher impedance might be preferable for the rectifier efficiency, but a suitable match between the antenna and the rectifier is hard to accomplish at impedances above 1000 Ω. If there is to big difference between the antenna and rectifier impedance power can be lost. This is due to the low bandwidth of the matching, which might be lower than the bandwidth of the signal of interest. In that case some of the power in the band is lost. Also, if the bandwidth is low problems might occur when manufactured. Due to imperfections in the components and substrate there might be a drift in the matching frequency and the harvester can miss the wanted frequency band.

With an impedance of 1000 Ω the rectifiers was simulated again. The 3-stage rectifier yield the highest efficiency from 48.6 % at -14 dBm to -19.6 % at -23 dBm. The output voltage varied from 1.01 to 0.18 V at input powers of -14 and -23 dBm respectively. With an input power of -20 dBm the efficiency and output voltage is 29 % and 0.357 V. Compared to similar rectifiers these results are good, [23] reported an efficiency of 13.6 % with an output voltage of 0.2 V, [29] reported 33.6 % with an output voltage of 0.15 V, both with an input power of -20 dBm at 900 MHz. Note that the loss in the matching network is included with these rectifiers, which is not a part of this thesis. With the loss in the matching network included the results the results in this thesis is lower. The output of the 3-stage rectifier was later used as the input of the boost converter since it yield the highest efficiency.

Simulations with set impedance of 1000 Ω revealed that the output voltage of a rectifier is not sufficient to run a suitable load. At input powers expected (below -19 dBm) the maximum voltage was 1.6 V (8-stage rectifier), well below the 2.5 V set as a minimum. With less stages the output voltage is found to be less. Another voltage amplification is therefore needed after the rectifier.

The rectifier is simulated with ideal capacitors to reduce the computation time. This will introduce some uncertainty in the simulations results. Using non ideal capacitors will introduce loss in the rectifier and thus the lower the efficiency. It is assumed that the loss will be low compared to the diode loss and that the relative performance of the rectifiers will remain the same, making the 3-stage rectifier the most efficient.

The rectifier is simulated with a sinusoidal voltage source with a frequency of 900 MHz. The RF-signal captured by an antenna is a modulated signal with a frequency varying from 890-960

MHz. The effect of a modulated signal is not considered in this thesis but some deviations are expected. It is not known if this will increase or decrease the rectifier efficiency. It is expected that the efficiency of the rectifier will be lower when the input frequency deviates from the simulated 900 MHz, but how much is not known. As the maximum change in frequency is 6 % it is assumed that the impact will be small.

6.2 Simple boost converter

A simple boost converter is simulated to determine the output voltage and efficiency. It was assumed that a big inductor value would maximize the efficiency, since the current will be smaller to store the needed magnetic energy. Simulations support this, as higher inductor values indeed give a higher efficiency. Due to this an inductor value of 8.2 μH was used in the rest of the simulations.

The oscillation network needed to switch the MOSFET is not a part of this thesis. It is replaced by a voltage source and the loss in this network is not considered. The efficiencies of the boost converter is therefore an overestimate. It was shown in simulations that by carefully selecting the switching period and on time of the switch the efficiency is 65 % at an input power of -24 dBm. The efficiency decrease with decreasing input power, at -30 dBm the efficiency is 52 %. It is also shown that the boost converter can charge the output capacitor to 2.5 V at all simulated input powers (above -30 dBm). Simulations of voltages above this is not considered since the load is to operate at this voltage and the loss in the power managing circuit following the boost converter will increase at increasing output voltages.

[11] used the same boost converter topology and the efficiency and output voltage was 62.86 % and 1.5 V at an input power of -25.7 dBm. Compared to the boost converter presented here the efficiency improvement is 2.76 % but with a lower output voltage. With a higher voltage amplification, it is believed that the boost converter performances will be similar. Note that the loss in the oscillation circuit is not included in their paper either, making it a fair comparison.

The use of the previous mentioned self-oscillating boost converter for energy harvesting is new and the efficiency is still low at low input powers. Another disadvantage is also that the output voltage varies with input power and is generally low. [1] obtained an efficiency of 8.43 % and an output voltage below 1 V at an input power of -24 dBm. The output voltage of this kind of boost converter is to low for the load used in this thesis.

The commercially available boost converter (BQ25570) yield an efficiency of 60 % at an input power of -24 dBm. This is 2 % less than that obtained by the simulated boost converter, but it includes all losses. It is likely that when the loss in the oscillation network is included the commercially available boost converter will yield higher efficiency. At -25 dBm and -27 dBm the efficiency of the commercial boost converter is 40 % and 6 % respectively. Since the efficiency of the simulated boost converter is 61 % and 60 % at these input powers it is likely that the simulated boost converter will yield higher efficiency, especially at -27 dBm.

The efficiency of the boost converter is highly dependent on the voltage charged onto the output capacitor. When the output voltage decrease the efficiency also decrease, at voltages below 1

V the efficiency is less than 51 %. This is not critical since the total system is to be operated with output voltages around 2 V. When the output capacitor is charged to 2.3 V the load starts to operate and the voltage will always between 1.8 and 2.3 V as long as power is available in the frequency band. Low efficiency at low output voltages will only result in a longer start up time of the harvesting circuit.

A loss analysis is performed to determine the loss contribution of the different components. First notice that the efficiency of the boost converter was found to be 58.49 % with an input power of -25.5 dBm and an output voltage of 2 V. This is not the same efficiency as found previously with the same parameters (60.64 % in Sec. 5.2.2). In the loss analysis the resolution is set higher (changed from 150 ns to 4.5 ns) and it is believed that the difference in the efficiencies is due to this. This reveals that there is uncertainty in the simulation results of the boost converter. It can be re simulated with a higher accuracy, but the computation time will be 33 times higher. In this master thesis there is not enough time to do this.

Both the total loss and the loss in the three different regions active (ideal inductor switching), ringing (due to parasitic capacitances) and leakage (when the input capacitor is charging) is simulated. The diode is the lossiest component, 21.23 % of the total power is lost here. Since 96.8 % of the diode loss is dissipated in the active region it might be that another diode can yield a lower loss. But keep in mind that this diode is chosen due to the low leakage and that the total diode loss can increase if another diode with a higher loss is chosen. The diode leakage loss is only 0.01 %. The total inductor loss is 16.24 % where 79.86 % is in the active region. This is due to internal resistance in the inductor and can only be reduced by switching to a better (less lossy) inductor, but the author of this thesis have not been able to find one. The inductor loss in the ringing region contributes to a total loss of 3.27 %. This loss can be reduced by reducing the ringing in the inductor current and will be discussed later. The loss in the switch is 4.03 %, a low percentage in the authors opinion. Also note that the total loss in the leakage region is 0.02 % of the total power. This is due to the low leakage current in the diode and the switch.

After the switch turn off there is a ringing current in the inductor. It is assumed that this comes from discharging parasitic capacitances in the switch. The loss analysis revealed that 4.14 % of the total power is dissipated in the components due to this. It is anticipated that this loss can be reduced if the oscillation network is carefully designed with the parasitic capacitances of the switch taken into consideration. By doing this the switch can be completely shut faster and some of the loss can be reduced. Since the oscillation network is not a part of this thesis this is not done here.

6.3 Rectifier and boost converter performance

The total efficiency of the rectifier and boost converter is found to be 21.1 % with an input power of -19 dBm. At -23 dBm the efficiency falls to 10.2 %. The harvester is able to provide an output voltage above 2.5 V at input powers above -23 dBm. Powers below this is not considered.

Since the oscillation circuit is not a part of this thesis the total efficiency is an overestimate. To see how a loss in the oscillation network affects the performance an analysis of the charge time needed to operate a Bluetooth Low Energy microcontroller from Nordic Semiconductor (nRF52) is done. It was shown that when the oscillation network consumes 151 nW the harvester cannot function at an input power of -23 dBm. It is unlikely that an oscillation network that consumes less than this can be designed, making the harvester unable to harvest power at -23 dBm. At an input power of -19 dBm the oscillation network can consume 2087 nW. With -19 dBm input power and a oscillation power loss of 1220 nW (50 % loss) the charge time is found to be just over 2 minutes.

The available power varies from location to location. It is also expected that the power will vary by the time of the day, especially in the GSM 900 band which is dependent on user traffic. In periods with no available RF-power the system need another energy source to operate, for instance a coin cell battery. An RF-harvester can then be used to power the system when sufficient power is available, prolonging the lifetime of the battery.

6.4 Number of rectifier stages to maximize efficiency

After the simulations of the rectifier it was assumed that the 3-stage rectifier was the best choice to be used together with the boost converter. To support this choice, the boost converter was simulated again with input corresponding to the output of the 4-stage and 5-stage rectifier. The simulations showed that the total performance with a 5-stage rectifier was lower than that of the 3-stage rectifier. Based on this it was assumed that adding more stages would degrade the performance further, so no simulations with more stages are conducted. The total efficiency with a 4-stage rectifier showed little deviation from the 3-stage rectifier. As the difference is small a conclusion based on these simulations cannot be made. It is possible that the 4-stage rectifier can yield the same results or slightly better.

Chapter 7

Conclusion

The aim of this thesis is to design a harvesting system able to harvest ambient power available in the GSM 900 MHz band. Measurements show that the average power in the GSM 900 band is higher than other frequency bands. The focus is on designing an efficient system at low input powers (-19 to -23 dBm) able to power a Bluetooth Low energy (nRF52) microcontroller as a load. These input powers correspond to the power from an antenna with an effective area of 1000 cm^2 and the average power density in the GSM 900 MHz band measured at London underground stations.

A rectifier and a boost converter is simulated with the aim of maximizing the efficiency. A power managing circuit which is able to turn the load off during charging is also presented.

Through simulations it was shown that a voltage multiplier with 3-stages yield the highest efficiency and should be used as a rectifier. With -19 dBm input power the simulated efficiency is -32.5 % while it decrease to 19.6 % at an input power of -23 dBm. The output voltage of the rectifier is 435 mV and 184 mV at an input power of -19 dBm and -23 dBm respectively. As this is not sufficient for the intended load a boost converter is needed.

A simple boost converter with only an inductor, a transistor switch and a diode is simulated. The oscillation network of the boost converter is not a part of this thesis, making the efficiency results an overestimate. It was shown that by carefully selecting the frequency and on time of the switch efficiencies from 65 % to 52 % can be obtained at input powers of -24 dBm and -30 dBm respectively. This power corresponds to the output powers of the 3-stage rectifier. The boost converter is able to provide an output voltage of 2.5 V at all input frequencies simulated.

The total efficiency of the rectifier and boost converter is found to be 21.1 % and 10.2 % with input powers of -19 dBm and -23 dBm respectively. Analysis of the needed charge time of the rectifier to operate the load reveals that a very efficient oscillation network is needed for the harvester to work at input powers down to -23 dBm. It is believed that the power consumed by this network will

be higher than the harvested power making the harvester unable to function at input powers below -22 dBm. The expected charge time at an input power of -19 dBm is below 2 minutes if the oscillation network consumes 733nW. With this power consumption the harvester is able to function at input power down to -21 dBm.

When the loss in the oscillation network is not considered the harvester is able to power the intended load (nRF52) at input powers down to -23 dBm. As the output voltage is 2.5 V it fulfil the specifications stated. Since the oscillation network is not designed it is not possible to conclude how low the input power can be before the harvesting stops. It is shown that with a power consumption of 733nW the harvester is functioning down to -21 dBm. It should be possible to design an oscillation network consuming less than this, making the harvester fulfil the specifications down to -21 dBm.

Further work

The focus in this thesis is to simulate the performance of a rectifier and boost converter to maximize the efficiency at low input powers. The rectifier and boost converter should be manufactured and tested to verify the simulation results. This is especially important due to the mentioned methods to reduce the computation time of the transient analysis which introduce uncertainties in the simulation results. An oscillation network for the boost converter also need to be designed to have a standalone harvesting system.

The bottle neck of the harvesting system is the rectifier where the efficiencies is low. Since the efficiency of the proposed boost converter is much higher than that of the rectifier most of the voltage amplification should be done here. In simulations the 1-stage and 2-stage rectifiers yield lower efficiencies than the 3-stage rectifier, but higher efficiencies should be obtainable. The use of high impedance antennas is interesting since higher rectifier input impedances is then possible (due to lower demands on the matching network). The work of Hucheng et al. [12] showed that this is possible as the efficiency of a half wave rectifier was found to be 25 % at -25 dBm input power. This efficiency should be higher if a full wave (1-stage) rectifier with a high impedance antenna is utilized, but simulations are needed to verity this. Also of importance is the rectifier efficiency when the frequency deviates from 900 MHz and the effect of a modulated RF-signal. When the matching network is designed a simulations of the efficiency with varying frequency and modulation should be conducted.

The self-oscillating boost converter is an interesting boost converter as there is no need for an oscillation network. More research should be put into this to lower the input powers this boost converter can function from.

More research should also be put into designing rectifier able to harvest power in multiple bands. This is especially interesting since the efficiency of rectifiers is low at low input powers. A multi-band system should therefore be able to both capture more power and rectify this power in a more efficient manner.

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Appendix A

Complete circuit diagram with components

Table A.1: Components used in the RF-harvesting system (circuit diagram in Fig. A.1).

Component	Description
C	0.33nF
D	HSMS-2850 [32]
C1	6nF
L	8.2 uF (1008AF[7])
T1	NTJS3157N [28]
T2	FDC6304P [26]
T3	ALD110914 [2]
R1/R2	2.2 MΩ
R3	6.8 MΩ
R4	3.9 MΩ
R5	30 MΩ
nRF52	Bluetooth Low Energy System on Chip [27]

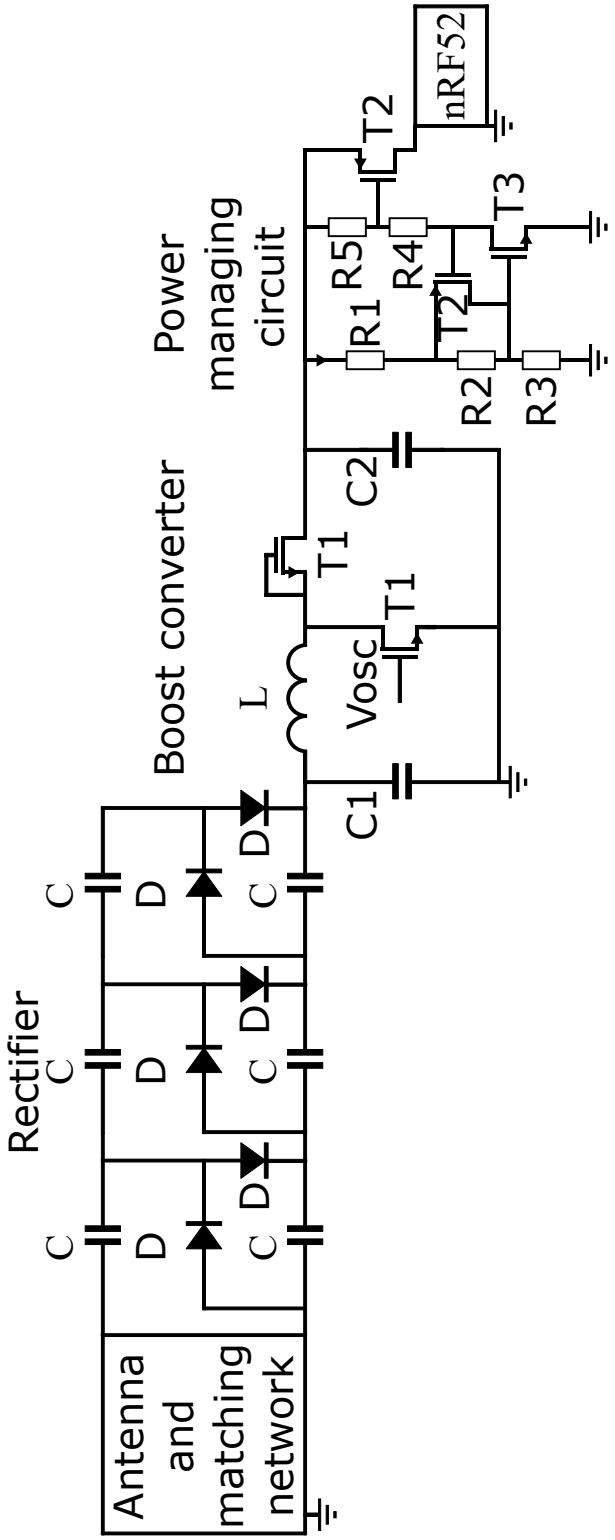

Figure A.1: Circuit diagram of the complete RF-harvesting system. For a standalone system an oscillation network connected to V_{osc} is needed (components in Tab. D).

Appendix B

Rectifier simulations to find input impedance

Table B.1: Rectifier simulation data with no restrictions of the input impedance, part 1/2.

Number of stages	V_{in} [mV]	R_{in} [Ω]	R_L [MΩ]	P_{in} [dBm]	V_{out} [V]	Efficiency [%]
1	500	3758.3	0.027	-14.78	0.744	0.61
2	500	3866.4	0.158	-14.90	1.593	0.497
	150	2429.8	0.089	-23.34	0.326	0.258
3	150	2604.2	1.060	-23.65	0.59	0.076
	150	2473.3	0.700	-23.42	0.578	0.105
	150	2239.3	0.400	-22.99	0.555	0.154
	150	1457.8	0.100	-21.13	0.463	0.278
	150	1251.8	0.070	-20.46	0.432	0.297
	150	1120.3	0.055	-19.98	0.41	0.305
	150	832.5	0.030	-18.69	0.352	0.306
	150	471.8	0.010	-16.23	0.242	0.246
	250	3702.8	2.000	-20.74	1.15	0.078
	250	3385.0	1.000	-20.35	1.126	0.137
	250	3047.0	0.600	-19.89	1.1	0.197
	250	2457.9	0.300	-18.96	1.05	0.289
	250	1804.7	0.150	-17.62	0.982	0.371
	400	2552.6	0.251	-15.04	1.836	0.429
4	150	1933.0	1.215	-22.35	0.777	0.085
	400	2739.7	0.770	-15.35	2.546	0.288
	400	2630.0	0.700	-15.17	2.532	0.301
	500	3876.0	1.820	-14.91	3.383	0.195
	500	3685.1	1.500	-14.70	3.365	0.225
	500	3680.8	1.500	-14.69	3.364	0.222

Table B.2: Rectifier simulation data with no restrictions of the input impedance, part 2/2.

Number of stages	V_{in} [mV]	R_{in} [Ω]	R_L [MΩ]	P_{in} [dBm]	V_{out} [V]	Efficiency [%]
	150	1621.0	2.300	-21.59	0.981	0.06
	150	1510.1	1.200	-21.28	0.953	0.102
5	350	2568.1	2.250	-16.23	2.796	0.146
	350	1821.8	0.652	-14.73	2.652	0.32
	500	3871.2	0.538	5.88	2.475	0.353
	300	1764.7	1.400	-15.93	2.722	0.208
6	300	1666.0	1.170	-15.68	2.693	0.229
	300	1470.6	0.800	-15.14	2.633	0.283
	300	1933.8	10.120	-16.33	3.304	0.046
7	300	1875.0	6.340	-16.20	3.283	0.071
	300	1638.2	2.310	-15.61	3.198	0.161
	100	807.8	2.370	-22.08	0.853	0.05
	100	738.6	1.000	-21.69	0.8	0.094
	100	653.6	0.500	-21.17	0.73	0.138
	100	516.2	0.200	-20.14	0.6	0.186
	150	1052.1	4.410	-19.71	1.543	0.05
	150	959.9	1.800	-19.31	1.485	0.104
	150	864.7	1.000	-18.86	1.421	0.155
8	150	811.4	0.750	-18.58	1.383	0.184
	150	720.5	0.500	-18.07	1.314	0.221
	200	1250.0	6.000	-17.96	2.247	0.052
	200	1228.5	4.000	-17.88	2.236	0.077
	200	1189.1	3.000	-17.74	2.214	0.097
	200	1126.1	2.010	-17.51	2.179	0.133
	250	1487.4	8.000	-16.78	2.997	0.053
	250	1403.9	4.200	-16.52	2.956	0.093
	250	1323.6	3.000	-16.27	2.924	0.122
	250	1248.7	2.000	-16.02	2.877	0.165

Appendix C

Rectifier simulation with input impedance set to 1000 Ω

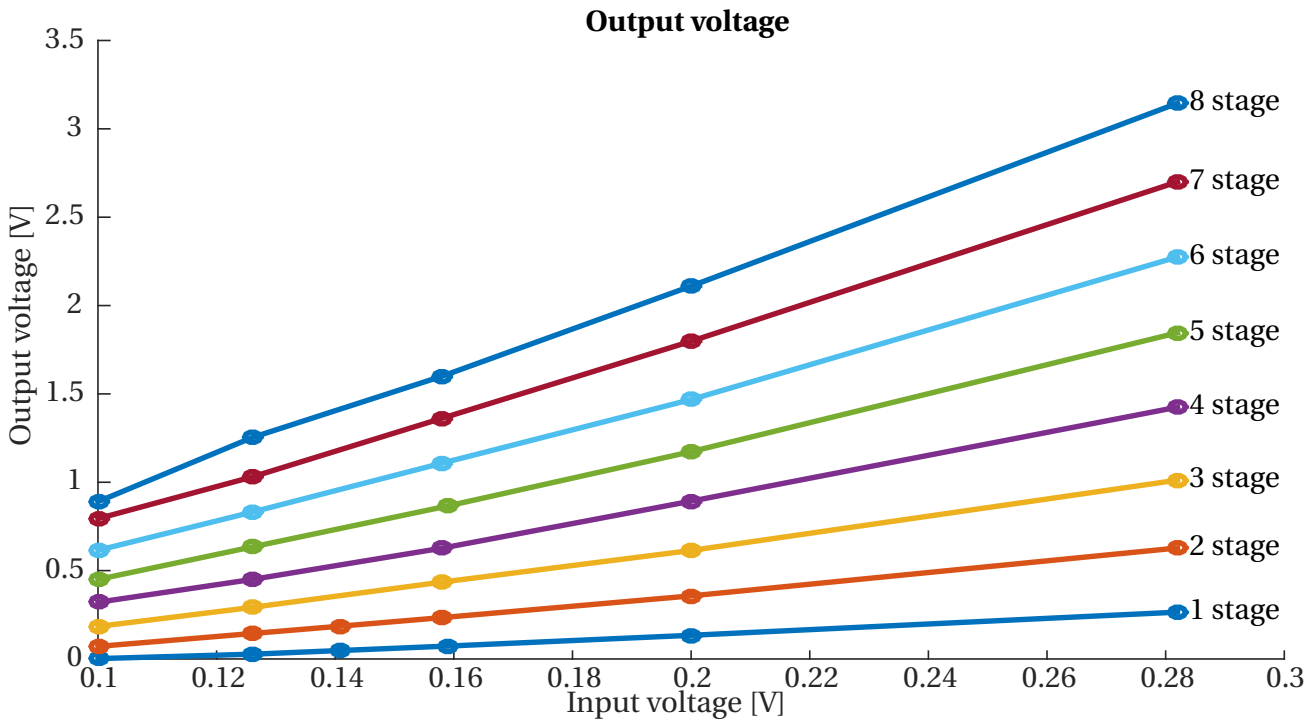

Figure C.1: Output voltage of n-stage rectifiers with input impedance of 1000 Ω and varying input voltage.

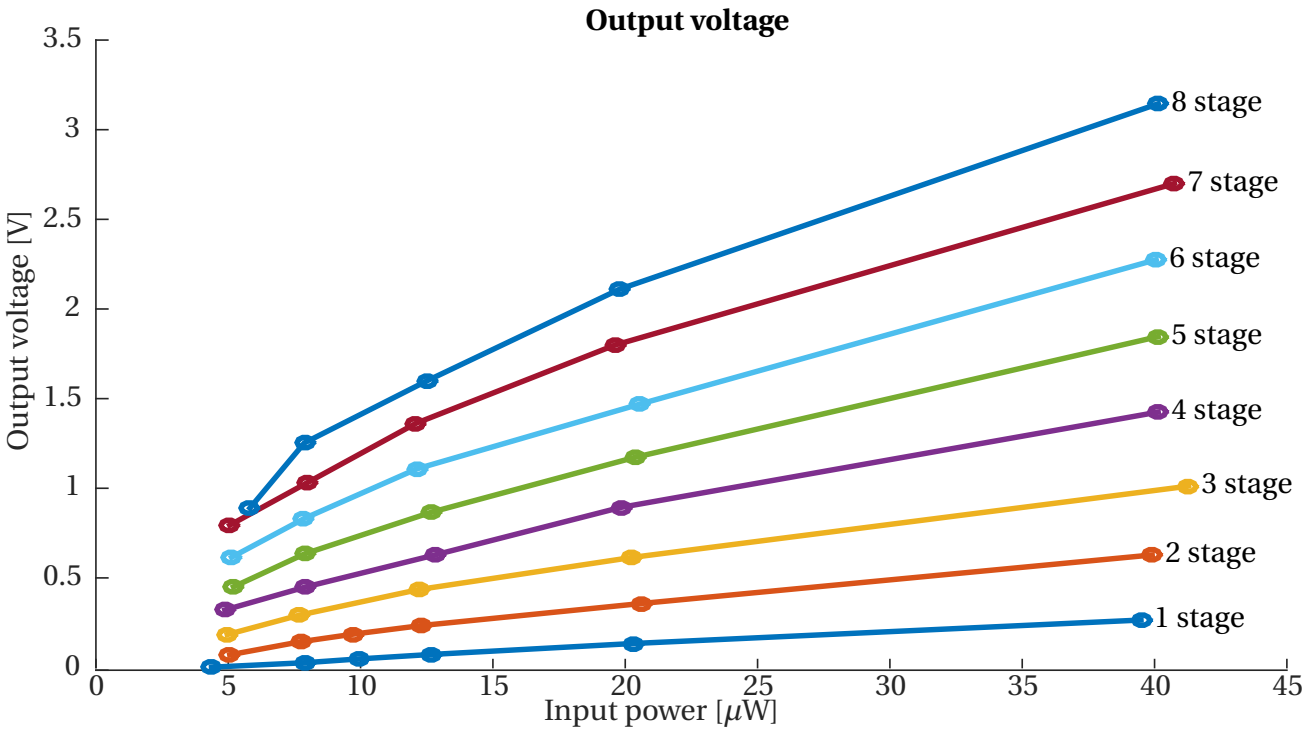

Figure C.2: Output voltage of n-stage rectifiers with input impedance of 1000 Ω and varying power.

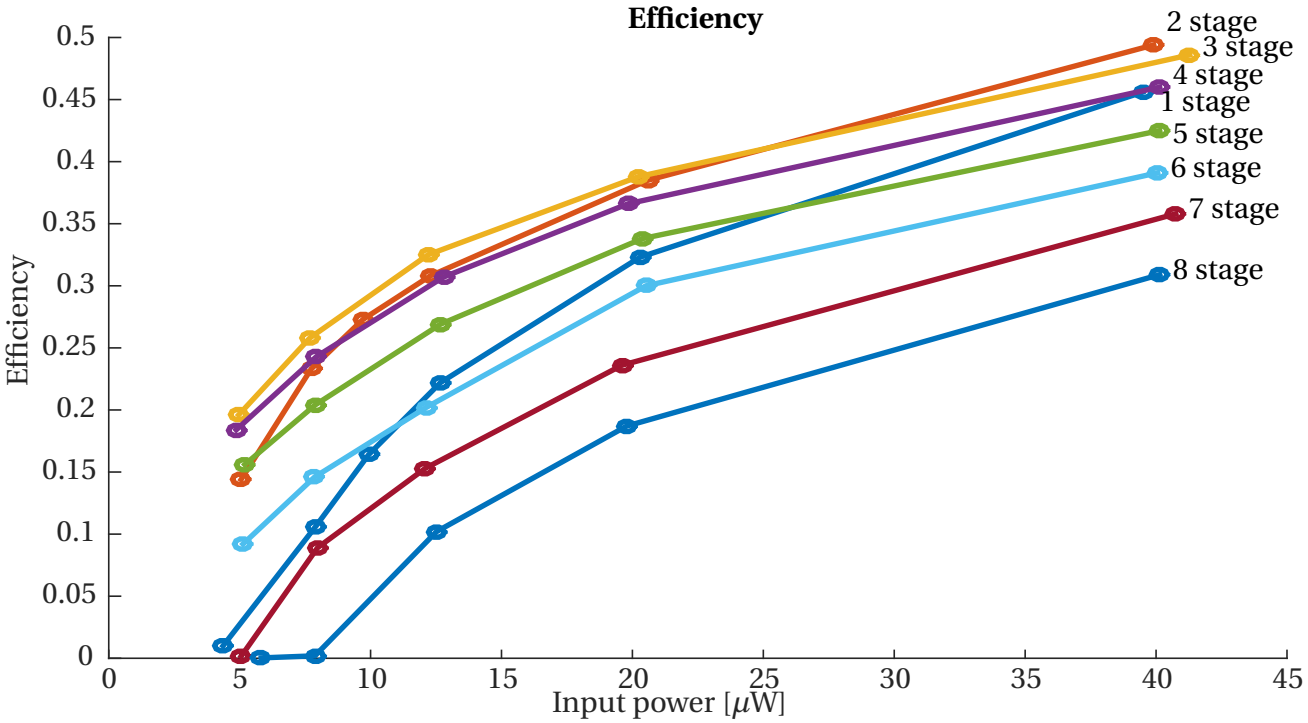

Figure C.3: Efficiency of n-stage rectifiers with input impedance of 1000 Ω and varying power.

Table C.1: Data from simulations of n-stage rectifiers with input impedance set to 1000 Ω. This data is used to plot figures in Section 5.1.5. This Table is part 1/2.

Number of stages	V_{in} [V]	R_{in} [Ω]	P_{in} [μW]	P_{in} [dBm]	V_{out} [V]	Efficiency [%]
1	0.100	1145.0	4.37	-23.60	0.002	0.010
	0.126	1006.1	7.90	-21.03	0.027	0.106
	0.141	1002.3	9.93	-20.03	0.048	0.164
	0.159	998.8	12.67	-18.97	0.073	0.222
	0.200	986.8	20.29	-16.93	0.134	0.323
	0.282	1007.9	39.49	-14.04	0.265	0.456
2	0.100	989.7	5.06	-22.96	0.071	0.144
	0.126	1028.8	7.73	-21.12	0.144	0.233
	0.141	1024.2	9.71	-20.13	0.186	0.273
	0.158	1017.4	12.28	-19.11	0.234	0.308
	0.200	972.4	20.59	-16.86	0.357	0.385
	0.282	997.5	39.91	-13.99	0.628	0.494
3	0.100	1008.6	4.96	-23.04	0.184	0.196
	0.112	1009.0	6.25	-22.04	0.232	0.226
	0.126	1037.4	7.68	-21.15	0.292	0.258
	0.141	1035.4	9.66	-20.15	0.357	0.290
	0.158	1036.3	12.20	-19.14	0.435	0.325
	0.178	1009.0	15.69	-18.04	0.516	0.355
	0.200	988.8	20.25	-16.94	0.614	0.388
	0.282	964.1	41.29	-13.84	1.012	0.486
4	0.100	1027.9	4.87	-23.13	0.321	0.184
	0.126	1001.5	7.93	-21.01	0.450	0.243
	0.158	977.6	12.78	-18.93	0.627	0.307
	0.200	1010.1	19.83	-17.03	0.893	0.366
	0.282	991.7	40.14	-13.96	1.425	0.460
5	0.100	963.1	5.20	-22.84	0.450	0.156
	0.126	1008.3	7.88	-21.03	0.634	0.204
	0.159	999.3	12.67	-18.97	0.866	0.269
	0.200	982.7	20.38	-16.91	1.173	0.338
	0.282	990.8	40.14	-13.96	1.846	0.425
6	0.100	976.4	5.13	-22.90	0.615	0.092
	0.126	1010.5	7.87	-21.04	0.831	0.146
	0.158	1026.0	12.12	-19.16	1.108	0.202
	0.200	976.2	20.52	-16.88	1.468	0.300
	0.282	994.3	40.06	-13.97	2.275	0.391

Table C.2: Data from simulations of n-stage rectifiers with input impedance set to 1000 Ω. This data is used to plot figures in Section 5.1.5. This Table is part 2/2.

Number of stages	V_{in} [V]	R_{in} [Ω]	P_{in} [μW]	P_{in} [dBm]	V_{out} [V]	Efficiency [%]
7	0.100	990.1	5.06	-22.96	0.794	0.002
	0.126	996.8	7.97	-20.98	1.030	0.089
	0.158	1033.8	12.09	-19.18	1.362	0.153
	0.200	1022.1	19.60	-17.08	1.798	0.236
	0.282	977.1	40.75	-13.90	2.700	0.358
8	0.100	860.5	5.82	-22.35	0.890	0.000
	0.126	1009.2	7.88	-21.04	1.253	0.002
	0.158	998.4	12.52	-19.02	1.600	0.102
	0.200	1010.8	19.78	-17.04	2.110	0.187
	0.282	992.4	40.14	-13.96	3.145	0.309

Appendix D

Boost converter simulation data and simulation parameters

Table D.1: Boost converter simulation data and simulation parameters (t_{on} and period T). The simulation circuit is shown in Figure 5.12. Input to the boost converter is the output of the 3-stage rectifier. Components used: 8.2 μH inductor (1008AF from Coilcraft[7]), NTJS3157N (On Semiconductor [28]) used as transistor and diode, C_{in} = 10μF and C_{out} = 20μF (ideal capacitors). The circuit is simulated in ADS.

P_{in} [dBm]	Initial V_{out} [V]	Period (T) [μs]	t_{on} [μs]	Efficiency	P_{out} [μW]
	2.5	10215	2.1	0.649	2.59
	2.0	7070	1.7	0.617	2.44
-24.02	1.5	7380	1.7	0.589	2.36
	1.0	5545	1.4	0.517	2.06
	0.5	3445	1.0	0.380	1.51
	2.5	16360	2.8	0.613	1.72
	2.0	8910	2.0	0.606	1.70
-25.53	1.5	6755	1.7	0.573	1.61
	1.0	5720	1.5	0.510	1.43
	0.5	3595	1.1	0.374	1.05
	2.5	26625	3.8	0.606	1.21
	2.0	14345	2.7	0.601	1.21
-27.03	1.5	12830	2.5	0.550	1.09
	1.0	8040	1.9	0.499	0.99
	0.5	4315	1.3	0.370	0.74
	2.5	31380	4.5	0.560	0.79
	2.0	22440	3.7	0.554	0.78
-28.5	1.5	15490	3.0	0.547	0.78
	1.0	11480	2.5	0.483	0.68
	0.5	5915	1.7	0.380	0.51
	2.5	36490	5.2	0.521	0.51
	2.0	33280	4.9	0.522	0.51
-30.12	1.5	18390	3.5	0.502	0.49
	1.0	9380	2.4	0.449	0.44
	0.5	4640	1.6	0.349	0.34

Appendix E

Simulation data of rectifier and boost converter

Table E.1: Total efficiency of the 3-stage rectifier and boost converter at different output voltages.

		η_{Tot} at Output voltage				
Pin [dBm]	η_{Rect}	0.5	1.0	1.5	2.0	2.5
-19.10	0.325	0.124	0.168	0.191	0.200	0.211
-20.10	0.290	0.108	0.148	0.166	0.176	0.178
-21.10	0.258	0.096	0.129	0.142	0.155	0.156
-22.00	0.226	0.086	0.109	0.124	0.125	0.126
-23.00	0.196	0.068	0.088	0.098	0.102	0.102

Appendix F

Gain of log-periodic antenna

Frequency (MHz)	Gain (dBi)	Frequency (MHz)	Gain (dBi)	Frequency (MHz)	Gain (dBi)
26	-23,93	190	3,85	625	4,01
28	-22,09	200	3,50	650	5,07
30	-19,49	225	3,80	675	4,54
40	-11,15	250	3,85	700	4,85
50	-5,16	275	3,94	725	4,93
60	-3,42	300	4,55	750	5,46
70	-3,50	325	4,46	775	5,20
80	-4,48	350	4,33	800	4,93
90	-3,62	375	4,40	825	5,31
100	-1,90	400	3,94	850	5,54
110	-0,15	425	4,84	875	6,22
120	1,75	450	4,70	900	5,58
130	1,64	475	4,88	925	5,36
140	1,49	500	4,16	950	5,53
150	0,12	525	4,29	975	6,05
160	1,26	550	4,27	1000	6,73
170	2,50	575	5,31	>1000	6,00
180	2,75	600	4,34		

Table F.1: Antenna gain of log-periodical antenna from ETS-Lindgren (model 3142B) [8].