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Evaluation of Switching Characteristics, Switching Losses and Snubber Design for a Full SiC Half-Bridge Power Module

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Problem Description

Renewable energies and environmental consideration have made electric propulsion systems increasingly popular in marine industry and applications. In order to achieve an efficient and high-quality electric propulsion system, well-performing and reliable power electronic converters are necessary. Power electronics in marine vessels are indispensable because of multiple power sources and loads. This increasing demand for electric power systems and power converters in marine vessels increases the volume and weight that they occupy. In order to minimize the space occupied by such systems, it is desirable to minimize losses and hence cooling systems needed. Using power converters with high switching frequency is another way of reducing the converter size, as the dimensions of passive components can be smaller.

Currently, the best-developed power converters consist of Silicon (Si) IGBT transistors and Si power MOSFET transistors. Unfortunately, converters based on Si technology are reaching their theoretical limits and are not as efficient as desired in high-power application. This is why there is an interest in the opportunities of Silicon Carbide (SiC) technology as Si's successor. SiC is a wide-bandgap semiconductor with superior material properties compared to Si.

As part of my master's thesis at NTNU, in collaboration with Rolls-Royce Marine AS Trondheim (formerly known as SmartMotor AS), the aim is to double-pulse test the performance of a full SiC half-bridge power module consisting of SiC MOSFETs and SiC SBDs. Thus, a double-pulse test circuit has to be designed and built. The double-pulse test makes it possible to analyze the switching transients and the switching power losses of the SiC module. LTspice IV will be used as simulation tool in order to design the double-pulse test circuit in a suitable way, as well as to take adequate precautions. The aim will be to obtain and investigate the switching characteristics of the SiC module in both simulation and experiment.

The fast switching transients of SiC MOSFETs can cause high switching stresses on the transistor, such as current and voltage overshoot and ringing. A short-circuit protection system should be designed and implemented in the gate driver in order to avoid dangerous short-circuit currents. Suitable snubbers should be designed and implemented in order to obtain acceptable switching transients and switching losses. This should result in a conclusion on whether SiC modules could help give a more compact converter design in high-frequency applications.

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Preface

The fourth year of my university education was spent abroad at INP ENSEEIHT in Toulouse, France. As they are prominent within power electronics, it was a natural choice for me to specialize within this subject. During the summer of 2015, I had a summer job at SmartMotor AS. This made it possible for me to start learning about the subject before the beginning of the fifth year. This was followed by the specialization project, which was carried out as a part of the ninth semester during the fifth year at NTNU, in collaboration with SmartMotor.

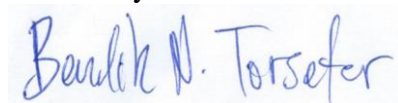
The master's thesis is a continuation of the specialization project. It has been very exciting to have such an innovative and practical subject in my master's thesis. New and creative solutions had to be found when challenges arose during the laboratory work. As this was the first time I worked with power converters without supervision, it was very challenging at times. Luckily, I had very competent people around me who were willing to share their knowledge. I would like to thank Prof. Ole-Morten Midtgård for his valuable advice and suggestions during the thesis. His guidance was essential in leading the thesis in the right direction and in sticking to the plan. I would like to express my sincere gratitude to Dr. Richard Lund from Rolls-Royce Marine AS Trondheim for always finding time in his busy schedule to help me move forward with my thesis. His competent advice was essential when difficulties arose during the laboratory work. He also gave valuable analysis of results from the laboratory work. I would also like to thank Subhadra Tiwari, a PhD student working with SiC power converters, for sharing her laboratory experience throughout the project. Her guidance at the laboratory was essential. I would like to thank all my supervisors encouraging me to write a scientific paper on the results from my master's thesis for the PEDG 2016 conference.

Finally, I would like to thank the staff working at the service lab at NTNU for helping me with the laboratory equipment and always finding solutions to problems. The Elprolab at NTNU also deserves a big thank you for manufacturing PCBs for my laboratory circuit. Amund Gjersvik at the Elprolab did an extremely important work during the semester, using numerous hours troubleshooting the laboratory setup when it did not function as desired. I would not have been able to finish all the goals of the master's thesis without his help.

Rolls-Royce Marine Trondheim and NTNU deserve a big thank you for providing me with everything I needed throughout my laboratory work.

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Abstract

In this thesis, the performance of the full Silicon Carbide (SiC) half-bridge power module BSM120D12P2C005 from Rohm Semiconductor is investigated. A laboratory circuit enabling double-pulse tests of the half-bridge module is designed and built. Building such a laboratory circuit demands careful analysis of the challenges and dangerous aspects that might arise. Consequently, the first part of the thesis discusses relevant background theory on SiC material properties, SiC MOSFETs and SiC SBDs. This is followed by general theory on different power converters, as well as analysis of switching transients and power losses in MOSFETs and SBDs. A theoretical efficiency comparison of three-phase inverters consisting of eight different state-of-the-art SiC half-bridge modules and one state-of-the-art Si IGBT half-bridge module is provided. It is shown in this comparison that all the SiC modules achieve an efficiency of 98 %, while the Si IGBT module gives an efficiency of approximately 93 % at 50 kHz.

Subsequently, general theory on important considerations when designing a converter circuit for hard-switching SiC modules is presented. This is followed by a detailed description of the laboratory setup, the measuring instruments and other important considerations in this thesis.

The next part presents an analysis of the SiC module performance through simulations in LTspice IV. The simulation circuit design and decisions are justified. The simulations are used as basis to investigate the switching characteristics of the SiC module, in addition to testing the impact of changes in the laboratory circuit. It is found through simulations that the combination of a DC snubber and a turn-off snubber could help improve the switching characteristics.

Finally, results from the laboratory experiments are presented. Firstly, it is shown that the bandwidth and stray inductance of the measuring instruments influence the switching characteristics. This is followed by a discussion on the selection of gate resistance and its influence on the switching speed. A short-circuit protection (SCP) is added to the gate driver of the SiC MOSFET, and its practical operation is proven successful. The switching characteristics and switching losses are obtained through double-pulse tests of the SiC MOSFET, and are presented for different drain-to-source voltages and drain currents. The switching characteristics show high switching stresses on the SiC module. Thus, snubber circuits are added to the laboratory circuit. The addition of a DC snubber and a turn-off snubber results in 40 % reduction in voltage overshoot and 85 % reduction in ringing duration. This improvement is achieved with an increase in total switching losses of 24 %. It is found that an Si IGBT switching at 600 V 120 A and a switching frequency of 50 kHz dissipates four times more energy than a SiC MOSFET including snubbers at equal conditions.

Sammendrag

Denne masteroppgaven analyserer ytelsen til halvbro-modulen BSM120D12P2C005 fra Rohm Semiconductor. Halvbro-modulen er «full SiC», noe som betyr at den kun inneholder silisiumkarbid (SiC) transistorer og dioder. En laboratoriekrets er designet og bygget slik at dobbepulstesting av SiC-modulen kan utføres. Å bygge en slik omformer-krets krever nøye planlegging og analyse av potensielle utfordringer knyttet til laboratorieforsøk. Av den grunn presenterer rapporten teori knyttet til silisiumkarbid som materiale, SiC MOSFET og SiC SBD. Deretter presenteres generell teori knyttet til kraftomformere, i tillegg til svitsjetransienter og effekttap i MOSFET og SBD. Dette følges av en teoretisk sammenligning av trefase vekselrettere bestående av åtte ulike SiC MOSFET-halvbro-moduler og én Si IGBT-halvbro-modul. Det er vist at alle SiC-modulene oppnår en virkningsgrad på 98 % i en trefase omformer, mens Si IGBT-modulen oppnår omtrent 93 %.

Neste del presenterer generell teori om hva som må tas hensyn til når man lager en elektrisk omformer med transistorer som svitsjer ekstremt raskt. Dette følges av en detaljert beskrivelse av laboratorieoppsettet, måleutstyret og andre hensyn knyttet til laboratorieforsøkene i denne rapporten.

LTspice IV brukes som simuleringsverktøy for å undersøke svitsjekarakteristikken til SiC-modulen. Simuleringskretsen og alle dens spesifikasjoner er nøye beskrevet. Simuleringene brukes til å undersøke hvilken påvirkning ulike endringer i simuleringskretsen har på svitsjekarakteristikken til SiC-modulen. Det er vist i simulering at en kombinasjon av en DC-snobber og en turn-off-snobber forbedrer svitsjingen.

Til slutt i rapporten presenteres resultatene fra laboratorieforsøkene. Det er først vist at båndbredden og strøinduktansen til måleutstyret kan ha stor innvirkning på svitsjekarakteristikken til SiC-modulen. Dette følges av en diskusjon rundt gate-motstanden, og dens innvirkning på hastigheten til svitsjetransientene. Et kortslutningsvern (SCP) er implementert i driverkretsen, og det er bekreftet at det fungerer som det skal ved høye strømmer. Eksperimentell dobbepulstesting gir svitsjekarakteristikken til SiC MOSFET-transistoren ved ulike drain-til-source-spenninger og drain-strømmer. Det er vist at svitsjebelastningen på SiC-modulen er veldig stor. For å unngå slik belastning brukes snobber-kretser. En kombinasjon av DC-snobber og turn-off snobber resulterer i 40 % reduksjon i overspenning og 85 % reduksjon i ringevarighet. Dette er oppnådd med en økning av totale svitsjetap på 24 %. En Si IGBT-transistor som svitsjer med en frekvens på 50 kHz har fire ganger høyere tap enn en SiC MOSFET-transistor, inkludert snobbere, ved samme betingelser.

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Abbreviations

| Acronym | Definition |
|----------------|---|
| AC | Alternating Current |
| BJT | Bipolar Junction Transistor |
| BOM | Bill of Materials |
| DC | Direct Current |
| DER | Distributed Energy Resources |
| DPT | Double-Pulse Test |
| DUT | Device Under Test |
| EMI | Electromagnetic Interference |
| ESR | Equivalent Series Resistance |
| FRD | Fast-Recovery Diode |
| IGBT | Insulated-Gate Bipolar Transistor |
| JFET | Junction Gate Field-Effect Transistor |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| PCB | Printed Circuit Board |
| PM | Permanent Magnet |
| PWM | Pulse-Width Modulation |
| RMS | Root Mean Square |
| SBC | Synchronous Buck Converter |
| SBD | Schottky Barrier Diode |
| SCP | Short-Circuit Protection |
| Si | Silicon |
| SiC | Silicon Carbide |
| SIT | Static Induction Transistor |
| SMD | Surface-Mount Device |
| SPWM | Sinusoidal Pulse-Width Modulation |

1. Introduction

1.1 Problem Background

Renewable energies and environmental consideration have made electric propulsion systems increasingly popular in marine industry and applications. In order to achieve an efficient and high-quality electric propulsion system, well-performing and reliable power electronic converters are necessary. Power electronics in electrified marine vessels are essential because of multiple power generation sources and multiple loads with different ratings. The increasing demand for electric power systems and power converters in marine vessels increases the volume and weight that they occupy [1]. In order to minimize the space occupied by such systems, it is desirable to minimize losses and hence the cooling systems needed. The size of a power converter can also be reduced by switching the transistors at higher frequencies, as this reduces the size of all passive components [2].

The power quality in a distribution system with high penetration of distributed energy resources (DER) highly relies on power converter switching transients with low voltage and current overshoot, low EMI and little ringing. The implementation of suitable snubber circuits can reduce such switching stresses and increase the output power quality from power converters [3] [4] [5] [6].

A great challenge in today's medium and low voltage power systems is the power converters and their considerable power losses during high-frequency switching. Currently, the best-developed power converters consist of Silicon (Si) IGBTs and Si power MOSFETs. Unfortunately, converters based on Si technology are reaching their theoretical limits and are not as efficient as desired and required [7]. This is why there is an interest in Silicon Carbide (SiC) technology as replacement for Si. SiC is a wide-bandgap semiconductor that has superior material properties compared to Si in high-power applications [8]. SiC technology can contribute to decreasing power losses in power converters, which makes it possible to reduce their size. That is, SiC technology could help minimize the power losses in large-scale power systems [9]. A performance evaluation from Cree Inc. states that the power losses in a DC/DC boost converter with SiC MOSFET had 99,3 % efficiency at 100 kHz, reducing the losses by 18% from the best Si IGBT solution at 20 kHz [10].

The master's thesis is conducted at NTNU in collaboration with Rolls-Royce Marine AS Trondheim, formerly known as SmartMotor AS. Rolls-Royce Marine Trondheim is a company offering compact, efficient and high-torque permanent magnet (PM) machines with integrated

drive and control systems for different applications. As a part of their desire to develop even better solutions, SiC technology is investigated as a replacement to their current technology in drive and control systems. The Hugin AUV, presented in Figure 1.1, was made by Kongsberg Maritimes in collaboration with SmartMotor.



Figure 1.1: The Hugin AUV – Developed by Kongsberg Maritimes and SmartMotor AS [11]

1.2 Objective

The objective of the master's thesis is to obtain, analyze and improve the switching characteristics of the full SiC half-bridge power module BSM120D12P2C005 from Rohm Semiconductor, by building a laboratory test setup. The switching characteristics should be obtained both through simulations in LTspice IV and through laboratory experiments. Thus, the aim is to investigate the influence of different aspects of the simulation circuit and the laboratory circuit on the switching characteristics of the SiC module.

As SiC MOSFETs have faster switching transients than Si IGBTs, they introduce challenges related to voltage and current overshoot and parasitic ringing during hard-switching transients. Such overshoot and ringing can cause high electrical stresses on the power device, which at worst could be damaging. These switching stresses can be as extensive that they could cause shoot through and short circuits. Thus, a short-circuit protection (SCP) system based on drain-to-source voltage measurement should be implemented in the gate driver circuit, in order to protect the SiC MOSFETs [12]. In order to reduce the high stresses on the transistor during switching, snubber circuits should be designed and implemented [6].

In [13], a C-CR DC snubber is used to suppress voltage ringing in a full-SiC half-bridge configuration. This solution, however, might not always be sufficient in cases with half-bridge power modules, as significant amounts of stray inductance could be located inside the module package. An RC turn-off snubber could help reduce switching stresses on the power device to an acceptable level [14] [15]. The master's thesis investigates if the combination of a DC snubber and a turn-off snubber could help reduce the electrical stresses on hard-switching SiC modules to an acceptable level during switching.

1.3 Scope of Work and Report Outline

The goal of the master's thesis is to build and test a power converter consisting of only SiC devices, analyze the switching characteristics and try to improve the transients by implementing snubber circuits. Eventually, the main goal of Rolls-Royce Marine Trondheim is to obtain a full SiC three-phase inverter. In order to accomplish this, it was initially determined to test and analyze the performance of a SiC half-bridge module from Rohm Semiconductor. A three-phase inverter would consist of three such half-bridge modules. The double-pulse test was chosen as evaluation basis for its performance. The master's thesis is a continuation of the specialization project, which focused on building a laboratory circuit and conducting double-pulse tests to obtain the switching characteristics of the SiC module.

The switching characteristics obtained in the specialization project were not as good as desired. Switching stresses such as extensive voltage overshoot and long-lasting ringing were some of the drawbacks that were found. Due to this, the switching transients in the specialization project had to be slowed down by increasing the gate resistance, in order to obtain switching stresses within acceptable limits.

In the master's thesis, the main goal is to exploit the advantages of SiC power devices as much as possible. This means that the switching transients have to be made as fast as possible. This will cause extensive switching stresses on the SiC module. Thus, snubber circuits and short-circuit protection must be implemented in order to operate safely.

The master's thesis is structured into seven chapters, where Chapter 1 is an introduction to problem background, objective and report outline. In Chapter 2, the technology and advantages of Silicon Carbide (SiC) and state-of-the-art SiC power devices are presented.

Chapter 3 presents general theoretical background that is important to have as basis in the continuation of the thesis. This chapter presents a thorough analysis of different converters, important parameters in MOSFET switching transients and an analysis of power losses in

switching devices. As the main goal of Rolls-Royce Marine Trondheim and NTNU is to build and test a three-phase inverter consisting only of SiC devices, a theoretical efficiency comparison of three-phase inverters consisting of eight different state-of-the-art SiC half-bridge modules is conducted. This comparison also includes a three-phase inverter consisting of state-of-the-art Si IGBT half-bridge modules.

In this thesis, much time is spent on theoretical background and converter design. This is done in order to understand all considerations that have to be made in order to conduct a safe and structured laboratory work. Thus, Chapter 4 presents general theory on converter design and considerations.

The thesis is composed in such a way that the reader should be able to conduct the exact same laboratory test without difficulty. Thus, the laboratory setup and measurement methods are thoroughly explained and discussed in Chapter 5. Snubber design based on theoretical calculations is presented.

Chapter 6 presents the switching characteristics of the SiC module obtained through simulations in LTspice IV. The simulations circuit design and considerations are explained in order to understand how the results are obtained. Switching characteristics, switching times and switching losses both with and without snubber circuits are investigated.

Chapter 7 presents switching characteristics obtained through laboratory experiments. The influence of the measuring instruments on the test results is explained, in addition to the impact of change in gate resistance in the gate driver. The implementation of a short-circuit protection (SCP) system in the gate driver is explained and tested through laboratory experiments. The continuation of Chapter 7 has a similar structure to that of Chapter 6, with double-pulse tests of the SiC module both with and without snubbers. This is followed by a comparison of the results obtained in simulation and experiment, compared to the datasheet values of the SiC module. The chapter ends with an analysis of the total switching losses in a high-frequency switching SiC MOSFET compared to the losses in a high-frequency switching Si IGBT.

The appendices are added as a supplement to what is presented in the thesis. They provide information that was not found necessary to include in the main parts of the thesis.

As earlier mentioned, the master's thesis is a continuation of the specialization project that was conducted during the autumn of 2015 [16]. It was found necessary to include parts of the theory from the specialization project in the master's thesis, as this theory gives an important basis for understanding the results of the master's thesis.

During the work with the thesis, LTspice simulations and laboratory experiments gave innovative and promising results. Encouragement from my supervisors resulted in writing a scientific paper on our findings for the PEDG 2016 conference in Vancouver, Canada. The paper was written in collaboration with Ole-Morten Midtgård and Subhadra Tiwari from NTNU, and Richard Lund from Rolls-Royce Marine Trondheim, who are also the supervisors in my master's thesis. Some of the results that are presented in the master's thesis were also presented in the paper. However, the scientific paper is written in the IEEE format, which is much more compact. While the scientific paper only focuses on snubber design and the advantage of implementing snubbers in simulations and laboratory experiments, the master's thesis goes more in detail on important aspects of the gate driver and measuring instruments. The scientific paper, with the title "Experimental Evaluation of Switching Characteristics, Switching losses and Snubber Design for a Full SiC Half-Bridge Power Module", is attached in Appendix H.

1.4 References

The reference list in this thesis mostly consists of well-known books, scientific IEEE papers, application notes and datasheet. These references are a combination of new and relatively old publications. As SiC technology still is quite new in the world of semiconductor devices, most of the references are from the last decade.

It is chosen to trust application notes from semiconductor manufacturers, as these often include information on semiconductors and switching devices that is not found elsewhere. However, such information should only be trusted when general information on switching devices is presented, as application notes often include hidden advertising for the manufacturers' own products.

2. Silicon Carbide

This chapter presents the material properties of SiC, and the advantages of SiC compared to Si. A brief explanation of bipolar and unipolar semiconductor devices is followed by a thorough analysis to the state-of-the-art SiC semiconductor devices.

2.1 Material Properties and Advantages of SiC

SiC is a wide-bandgap semiconductor with interesting properties when compared to Si semiconductor. The material properties of SiC and Si are presented in Table 2.1.

Table 2.1: Main properties of Si and SiC [17]

| Properties | Si | 4H-SiC |
|--|-----------------|------------------|
| Energy bandgap [eV] | 1.12 | 3.26 |
| Thermal conductivity [W/cm°C] | 1.5 | 3.7 |
| Saturated electron drift velocity [cm/s] | 1×10^7 | 2×10^7 |
| Electron mobility [cm ² /Vs] | 1400 | 1000 |
| Electric breakdown field [V/cm] | 2×10^5 | 20×10^5 |
| Dielectric constant | 11.7 | 9.7 |

The material properties listed in Table 2.1 are important when it comes to SiC's role in making power converters smaller and more efficient. The wide energy bandgap that SiC provides leads to lower leakage current in blocking mode and a higher junction temperature [18]. The energy bandgap of SiC, which is more than three times wider than the Si energy bandgap, means that it takes a lot more energy for the electrons to free themselves from their valence bands. This means that SiC devices can operate at a significantly higher junction temperature than Si devices, without risking high leakage currents.

The thermal conductivity is about three times higher in SiC than in Si. This leads to a much better thermal capability and the possibility of removing a lot more heat from the junction [19]. That is, SiC devices are able to operate at a lower temperature than Si devices for the same switching voltage and current, thus a smaller heatsink can be used. Thus, the risk of thermal runaway is smaller in SiC devices due to good thermal conductivity.

The advantage of a higher saturated electron drift velocity is that the electrons are able to move faster than in SiC devices than in Si devices. As a result, the switching speed increases and thereby introduces the possibility of having a higher switching frequency.

The breakdown electric field of SiC is 10 times higher than that of Si. That is, 1cm of SiC semiconductor can block 10 times higher voltage than 1cm of Si semiconductor. Consequently, the drift region in a SiC MOSFET with 600 V rating can theoretically be 10 times smaller than in an Si MOSFET with the same voltage rating. As a result, the on-state resistance in SiC devices is much lower due to a much shorter drain-to-source region. Equation (2.1) expresses the specific on-resistance in the doped semiconductor layer [20]:

$$R_{\text{on,sp}} = \frac{4V_B^2}{\epsilon \cdot \mu \cdot E_c^3} \quad (2.1)$$

V_B is the breakdown voltage [V], E_c is the critical electric breakdown field [V/cm], ϵ is the dielectric constant and μ is the mobility [cm^2/Vs]. From (2.1), the on-state resistance decreases with the cube of the critical electric breakdown field. A faster switching transition combined with lower on-state resistance reduces both the switching power losses as well as the conduction power losses [9].

In a power converter based on SiC components there are even more advantages related to the topology of the converter. As SiC transistors are able to operate at higher frequencies than their Si counterparts at high voltage levels, this means that all passive components can be smaller [2]. The reduced power losses in SiC devices lead to additional downsizing of all passive components. All this eventually leads to a more compact power converter design.

A drawback of SiC is that the electron mobility is lower than in Si. From (2.1) it is clear that a lower electron mobility causes higher on-state resistance in the drift region. This is why the 4H-SiC polytype is chosen in this evaluation, as it has higher electron mobility than other SiC polytypes [21].

2.2 Unipolar and Bipolar Power Devices

In bipolar devices, minority carriers are injected during the on state of the device. These minority carriers must be removed from the device at turn off. This charge removal is done either via electron-hole recombination or via the base drive current [17]. Such a removal process leads to critical switching power losses in the device during turn off. This phenomenon is often referred to as a tail current. The IGBT and the BJT are bipolar devices.

Unipolar devices are majority carrier devices with no minority carrier injection. This is due to an insulated gate terminal, i.e. no charge flows from gate to source/drain in a majority carrier device. This is advantageous, as there are no power losses due to minority charge removal

during turn off, and thus no tail current. Because of this, unipolar current conduction is often preferred in power semiconductor devices. The Schottky barrier diode (SBD) is such a device. The SiC revolution has led to SBDs becoming dominant in power devices, as bipolar Si/SiC PN-junction diodes have significant power losses compared to SiC SBDs.

SiC devices are often unipolar devices, due to a low hole mobility [22]. Unipolar device topologies include MOSFET, JFET and SIT. The MOSFET is the most common unipolar power device, as it has normally-off behavior [17]. This is a very important property in terms of security in power converters.

2.3 State-of-the-art SiC Devices

The SiC devices that will be thoroughly described in this thesis are the SiC Schottky Barrier Diode (SBD) and the SiC MOSFET.

2.3.1 SiC Schottky Barrier Diode (SBD)

Schottky barrier diodes (SBD) are extremely fast diodes with good reverse recovery dynamic and low threshold voltage [23]. The cross-sectional view of an SBD is presented in Figure 2.1.

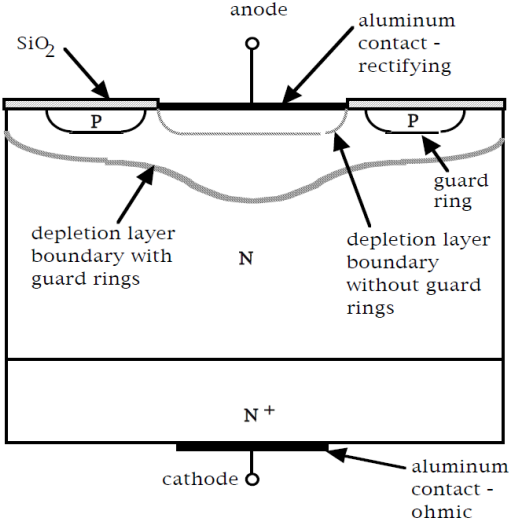


Figure 2.1: Cross-sectional view of an SBD [6]

The SBD is formed by a thin aluminum contact that is in direct contact with an n-type semiconductor. The thin aluminum metal film is the anode, while the n-type semiconductor is the cathode [6]. The metal-to-semiconductor interface forms a depletion layer, similar to that of a pn junction, due to electrons that travel across the interface in both directions during the formation of the depletion layer. However, most of the electrons travel from the semiconductor to the metal film. This happens because the electrons in the semiconductor have higher absolute potential energy than the electrons in the metal film. The depletion layer is finished forming

when thermal equilibrium is reached, that is, when the flow of electrons is equal in both directions. As electrons are the only carriers that take part in the transition, the SBD is called a majority carrier device [6].

If a positive voltage is applied at the anode with respect to the cathode, the barrier potential formed by the depletion layer is reduced. This allows current to flow. If a negative voltage is applied, on the other hand, the potential barrier is increased, making it more difficult for current to flow. The I-V characteristics of the SBD is presented in Figure 2.2.

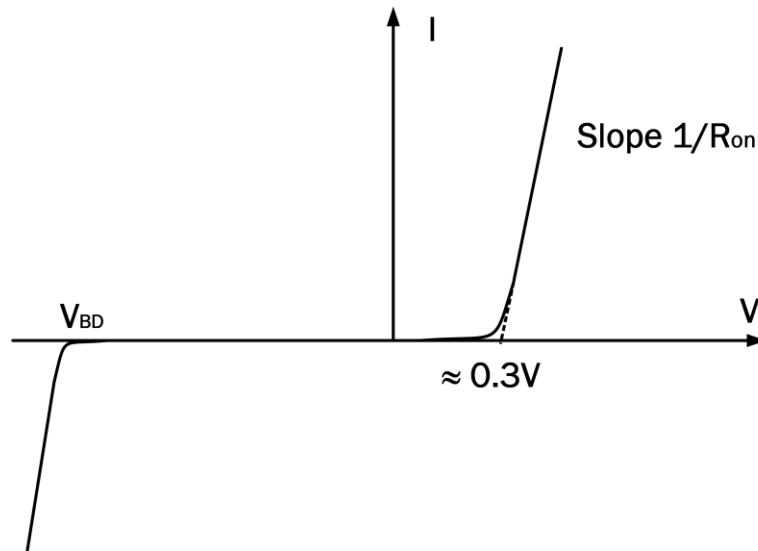


Figure 2.2: I-V characteristics of the Schottky Barrier Diode

R_{on} is the on-state resistance and V_{BD} is the reverse breakdown voltage of the SBD. As the SBD does not include any pn junction, the on-state voltage threshold $V_{th} \approx 0.3 V$ is less than that of a pn-junction diode. Traditional Si pn-junction diodes also have excessive reverse recovery, which results in higher switching losses. This is because pn-junction diodes are minority carrier devices that need to remove stored charge from the drift region when switching off the diode. In contrast, SBDs are majority carrier devices with no stored minority carriers during conduction mode, due to the lack of pn-junction in the drift region. When turning off the SBD, the only reverse recovery current is due to discharge of the junction capacitance [24].

When using SBDs as freewheeling diodes, the reverse recovery of SBDs is almost independent of the transistor drain current. This leads to lower turn-off power losses in SBDs than in pn-junction diodes, as well as a quicker turn-off transient. The typical turn-off reverse-recovery transient of an Si fast-recovery pn-junction diode (FRD) compared to a SiC SBD is given in Figure 2.3.

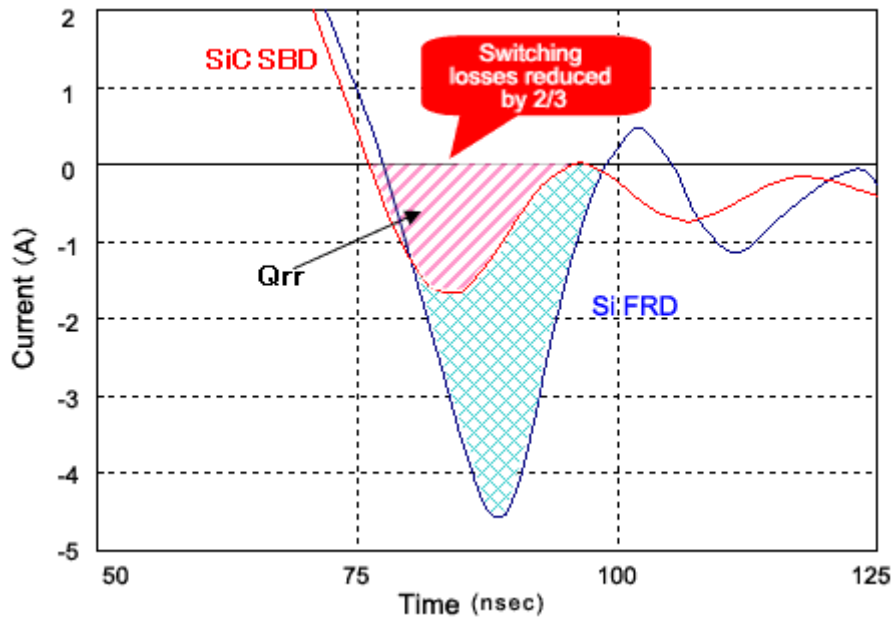


Figure 2.3: Comparison of Si FRD and SiC SBD reverse recovery [25]

Q_{rr} is the total reverse-recovery charge stored in the diodes, which is discharged as the reverse-recovery current I_{rr} during the turn-off transient. According to [25], the reverse-recovery switching losses due to Q_{rr} can be reduced by $2/3$ by using a SiC SBD instead of a Si FRD. This could also be achieved by implementing Si SBDs instead of Si FRDs. However, while Si SBDs have low voltage ratings and high leakage currents due to the material properties of silicon, state-of-the-art SiC SBDs have voltage ratings up to 1200V and current ratings up to 40A [24]. The SiC SBD has excellent high-temperature performance due to the thermal properties of SiC. Thus, the current switching transients and reverse-recovery time are close to independent of temperature. This is a huge advantage compared to Si SBDs. The material properties of SiC make SiC SBDs more efficient, smaller and able to operate at higher frequencies than Si SBDs. In addition, thermal properties lead to a smaller heat sink. All the above-mentioned advantages make SiC SBDs an important part of future compact power converters.

2.3.2 SiC MOSFET

Si power MOSFETs have the disadvantage that the on-state resistance of the device increases significantly for higher voltage ratings. This is why the IGBT, which is a minority carrier device, until now have been prominent for high-voltage applications. As IGBTs are minority carrier devices, they introduce a tail current during the turn-off transient of the device due to minority carriers in the drift region, as explained in Section 2.2. This increases the switching time and the switching losses of the device at turn off.

SiC MOSFETs have superior properties compared to Si devices, both when it comes to high blocking voltage, low on-state resistance, fast switching transients, low switching losses and good thermal properties [26]. As opposed to IGBTs, SiC MOSFETs are majority carrier devices with no tail current and thus lower switching times and switching losses [27]. The wide bandgap of SiC makes the on-state resistance in SiC MOSFETs much lower than in Si power MOSFETs, due to a much shorter drift region for the same voltage rating (Section 2.1). While the on-state resistance of Si power MOSFETs increases rapidly at high temperatures, SiC MOSFETs have low on-state resistance also at high temperatures [24]. As for SiC SBDs, SiC MOSFETs can be much smaller than Si power MOSFETs and Si IGBTs, hence their advantage in future compact power converters.

The drawback of SiC MOSFETs is that they currently experience some problems related to voltage overshoot and ringing caused by parasitic capacitance and inductance in the converter circuit [28]. This drawback exists because SiC MOSFETs have faster switching transients than Si IGBTs, and thus give more oscillating transients with the same amount of parasitics. Because of this, parasitics in a laboratory test circuit of SiC MOSFETs have to be minimized. Figure 2.4 depicts the high frequency and high power capability that the SiC MOSFET possesses.

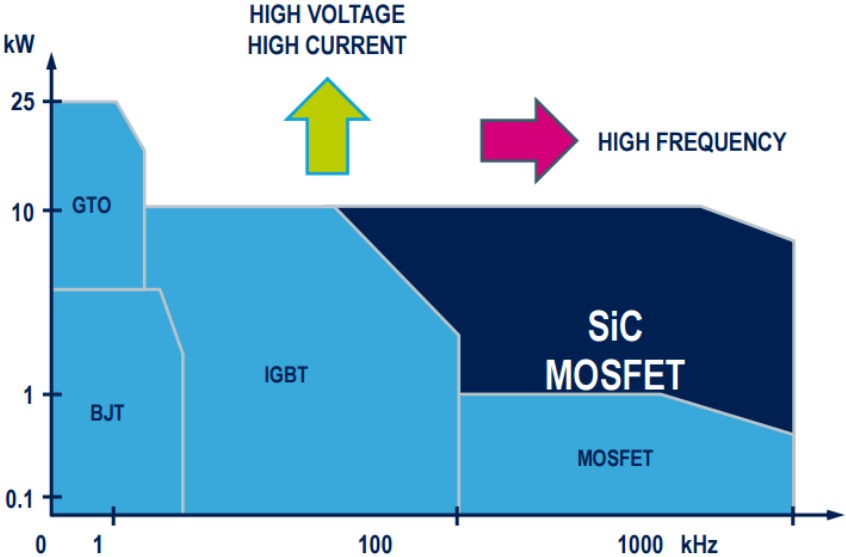


Figure 2.4: Advantages of the SiC MOSFET [23]

2.3.2.1 Basic Structure

The SiC MOSFET has three external terminals called drain (D), source (S) and gate (G). It is constructed in such a way that the current flowing from drain to source is controlled by the voltage applied between gate and source. The basic structure and the symbol of an n-channel DMOS MOSFET is given in Figure 2.5 [29].

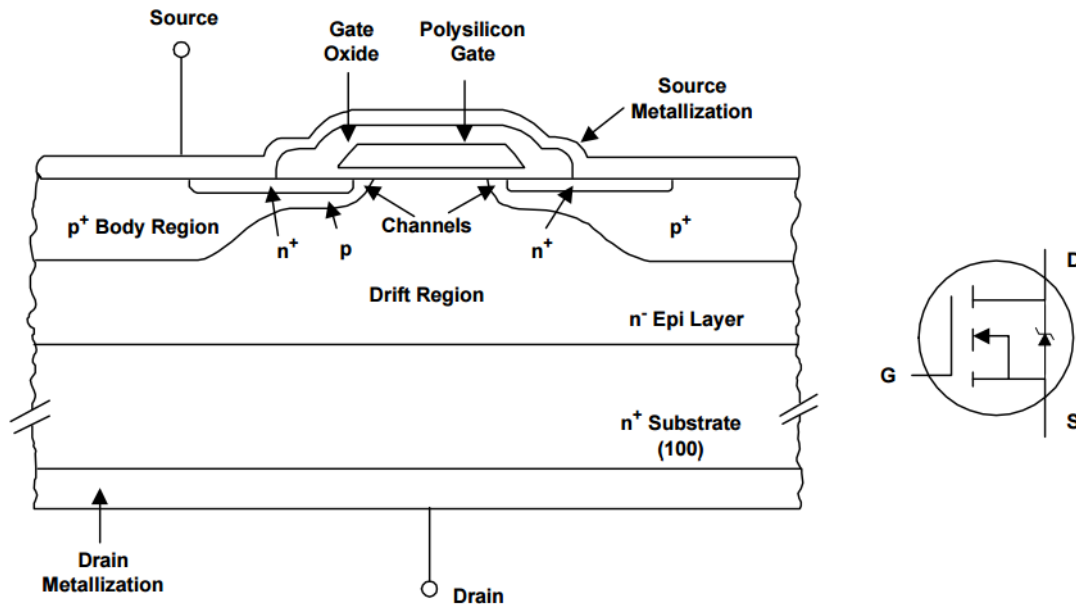


Figure 2.5: Basic structure of the n-channel DMOS MOSFET [29]

At first glance, it seems as this structure would never be able to conduct any current between the drain and source terminals. As there are two opposite pn junctions in the structure (drain-to-body junction and source-to-body junction), it seems as at least one of them has to be blocking if a voltage is applied between drain and source. Bipolar devices, e.g. BJTs, inject minority carriers through their base terminals in order to enhance conduction between collector and emitter. This would not be possible in MOSFETs, as the gate terminal is insulated from the channel due to the gate oxide (SiO_2 material). However, if a positive voltage is applied on the gate terminal with respect to source in Figure 2.5, the negative charges will start to accumulate on the surface of the channel in the body region. Thus, a conducting channel will form in the body region. This will allow current to flow between the drain and source terminals [6].

The structure in Figure 2.5 is called n-channel, as the source and drain regions are n-type regions, while the body region is a p-type region [6]. A p-channel MOSFET has the exact opposite structure. P-type and n-type regions are explained in the following manner:

- **P-type semiconductor:** Semiconductor with higher concentration of holes than electrons. Thus, electrons are minority carriers and holes are majority carriers.
- **N-type semiconductor:** Semiconductor with higher concentration of electrons than holes. This means that holes are minority carriers and electrons are majority carriers.

Both types of semiconductors are created through doping. An n-channel MOSFET can be either enhancement-mode or depletion-mode. This is explained in the following manner:

- **Enhancement-mode:** An n-channel enhancement-mode MOSFET does not have a conductive channel naturally. This means that a positive gate-to-source voltage has to be applied in order to create a conductive channel.

- **Depletion-mode:** An n-channel depletion-mode MOSFET has a conductive channel when a gate-to-source voltage is not applied. This means that an increased positive gate-to-source voltage narrows the channel, which denies channel conduction.

There are different types of structures used in SiC MOSFETs, which will be discussed in the next section.

2.3.2.2 DMOS and UMOS

The most common power MOSFET structure is called VDMOS (vertical-diffused metal-oxide-semiconductor) or simply DMOS (double-diffused metal-oxide-semiconductor). Other structures including VMOS and UMOS are also available on the market. The DMOS and UMOS structures are depicted in Figure 2.6.

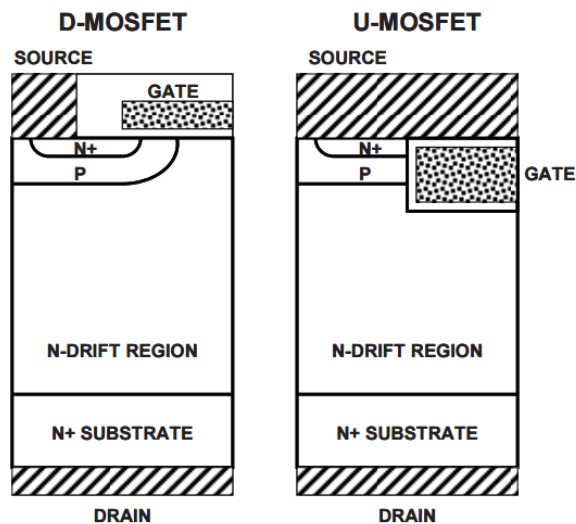


Figure 2.6: Power MOSFET structures [17]

The DMOS structure was the first available Si power MOSFET structure, which was made available in the 1970s. In the 1990s, the UMOS was introduced in order to reduce the on-state resistance in the Si power MOSFET [17]. The MOSFET structure in Figure 2.5 is DMOS.

The first available SiC power MOSFET was introduced in 1994 and had UMOS structure, also called vertical trench MOSFETs [30]. In the development of SiC MOSFETs in high power applications, the UMOS structure encountered problems related to increasing the voltage rating. Because of the trench-positioned gate layer, the peak voltage across the SiO_2 insulation layer (gate oxide) can become so high that it causes breakdown of the oxide layer at the trench corners. This problem was solved by removing the trenches and using the planar DMOS structure, even though this increases the on-state resistance of the SiC power MOSFET. By this transition from UMOS to DMOS, the blocking capability of the MOSFET was tripled [30]. The DMOS structure is the dominating topology in SiC power MOSFETs.

2.3.2.3 Intrinsic Resistance and Capacitance in DMOS Structure

The detailed n-channel DMOS structure including all intrinsic resistances is presented in Figure 2.7:

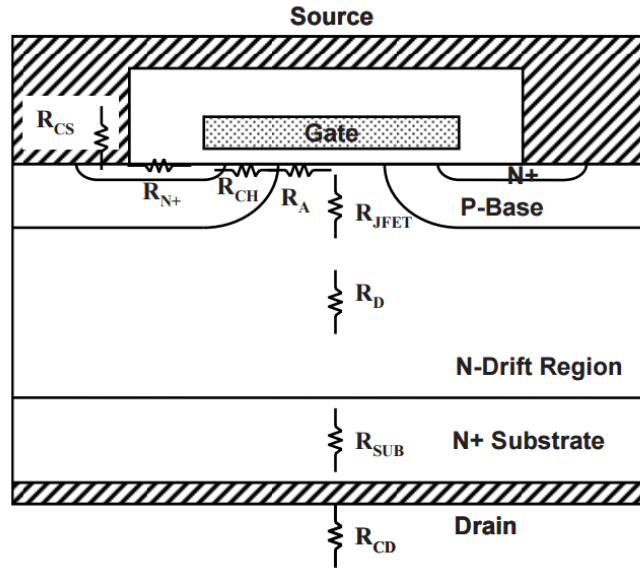


Figure 2.7: Intrinsic resistance in the n-channel DMOS MOSFET [17]

The total on-state drain-to-source resistance $R_{ds(on)}$ of the device is the sum of all the intrinsic resistances, as shown in (2.2).

$$R_{ds(on)} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD} \quad (2.2)$$

It can be calculated by using the expression for specific resistance in a uniformly doped semiconductor, given in (2.1).

The equivalent circuit describing the intrinsic capacitances in an n-channel DMOS MOSFET is depicted in Figure 2.8.

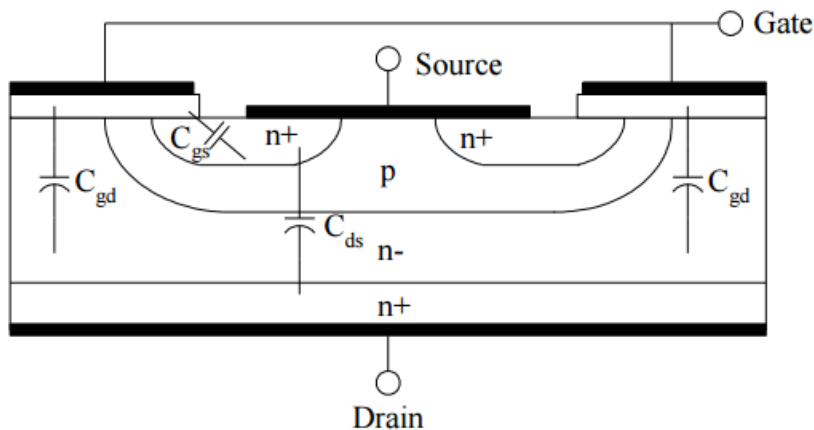


Figure 2.8: Intrinsic capacitance in the n-channel DMOS MOSFET [31]

The intrinsic capacitances are independent of temperature. This means that the switching speed of MOSFETs is independent of temperature, as switching speed is related to the charging of the input capacitance $C_{iss} = C_{gs} + C_{gd}$. However, the gate-to-source capacitance C_{gs} and the gate-to-drain capacitance C_{gd} vary with the voltage applied [31]. There are three important terms describing the intrinsic capacitances and their influence on power MOSFET switching:

- **Input Capacitance** $C_{iss} = C_{gs} + C_{gd}$. The input capacitance is measured between gate and source when drain-to-source is shorted. Thus, C_{iss} has direct influence on the switching speed, as this capacitance has to be charged to the threshold voltage to turn on the device. It also needs to be discharged in order to turn off.
- **Output Capacitance** $C_{oss} = C_{ds} + C_{gd}$. The output capacitance is measured between drain and source when gate-to-source is shorted. C_{oss} can affect the resonance of the circuit, as it together with stray inductance form an LC resonant circuit.
- **Reverse Transfer Capacitance** $C_{rss} = C_{gd}$. The reverse transfer capacitance is measured between drain and gate with source connected to ground. This is often referred to as the Miller capacitance. It affects the voltage rise time and fall time during switching.

These capacitances are easy to measure experimentally, and are therefore often listed in MOSFET datasheets.

2.3.2.4 I-V Characteristics

The I-V characteristics of a SiC MOSFET are presented in Figure 2.9.

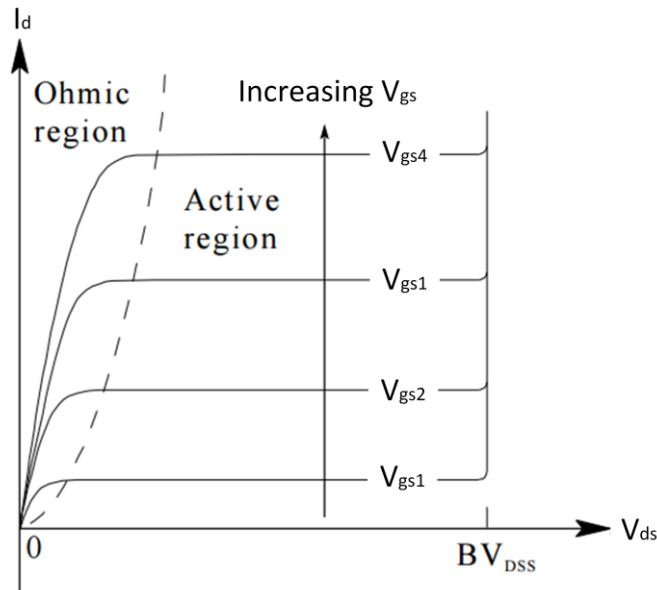


Figure 2.9: I-V characteristics of the MOSFET [31]

The gate-to-source voltage V_{gs} has a great impact on the on-state drain-to-source resistance $R_{ds(on)}$ of the MOSFET, and thus the drain current I_d , as can be seen in Figure 2.9. This is

because an increased gate-to-source voltage increases the field effect of the gate. Thus, the on-state resistance of the MOSFET is inversely proportional to the magnitude of the positive bias gate-to-source voltage $V_{gs(on)}$. The MOSFET is said to be in its *ohmic region* when the magnitude of the drain-to-source voltage V_{ds} influences the drain current, which is only the case for low drain-to-source voltages. The ohmic region gets wider when the gate-to-source voltage increases. In the *active region* of the MOSFET, the drain current is independent of drain-to-source voltage. In this region, the drain current only depends on the gate-to-source voltage. The last region is called the *cutoff region*, which is the region where the MOSFET is blocking all drain current. This region is explained using Figure 2.10.

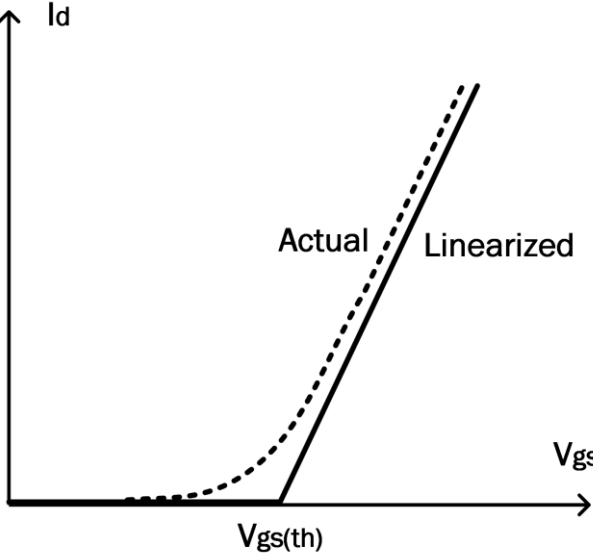


Figure 2.10: Gate-to-source voltage transfer characteristics

For low gate-to-source voltages, there is no drain current flowing. This is because the field effect from the gate terminal is not high enough to induce conduction in the channel between drain and source. The region with no conduction is called the cutoff region. At the threshold voltage $V_{gs(th)}$, the gate-to-source voltage gets high enough to form a conducting channel between gate and source. Figure 2.10 presents the actual and the linearized transfer characteristics.

2.3.3 SiC MOSFET Switching Characteristics

The switching characteristics of SiC MOSFETs are very similar to that of Si MOSFETs. This section presents the switching transients of SiC MOSFETs, and includes information on important events during turn-on and turn-off switching. The switching transients will be examined in a step-down (Buck) converter design, depicted in Figure 2.11. This converter design will be explained in Section 3.1.

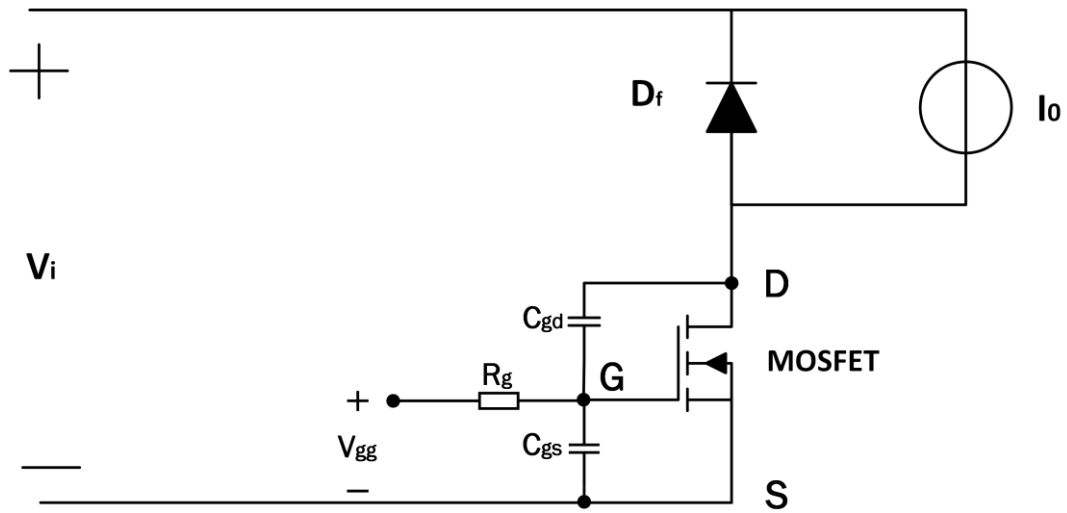


Figure 2.11: Step-down converter with MOSFET including intrinsic capacitances

2.3.3.1 Turn-On Switching Characteristics

Firstly, the turn-on switching transient will be investigated. It is assumed that the MOSFET in Figure 2.11 is in its off state, and that the load current I_0 is freewheeling through the freewheeling diode D_f . The load is assumed to be purely inductive, thus the load is represented by the current source I_0 . If now the input voltage V_{gg} is increased in order to turn on the MOSFET, a turn-on switching transient will initiate. This is depicted in Figure 2.12.

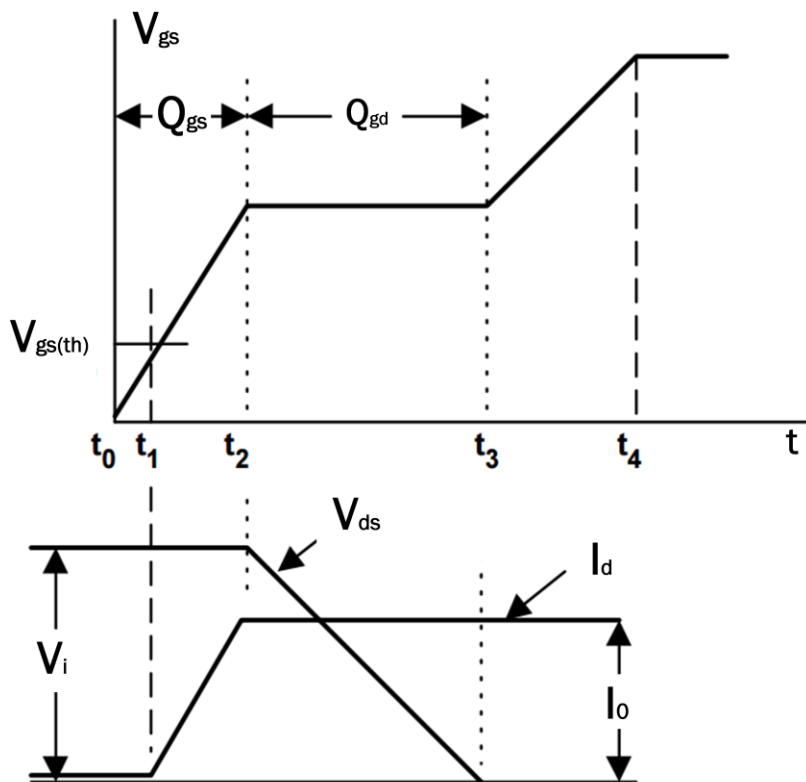


Figure 2.12: Turn-on transient without diode reverse recovery [29]

For the gate-to-source voltage V_{gs} to start rising, the gate-to-source capacitance C_{gs} in Figure 2.11 has to be charged. Thus, a gate current will start to flow from V_{gg} , through the external gate resistor R_g , to the capacitor C_{gs} . The charge supplied to C_{gs} makes the gate-to-source voltage V_{gs} rise, with the MOSFET being in its cutoff region. At time t_1 in Figure 2.12, the threshold voltage $V_{gs(th)}$ is reached. At this point, the field effect from the gate is high enough to induce a conducting channel from drain to source. Thus, the drain current I_d can start to increase while the gate-to-source voltage increases further. The MOSFET is now in its active region. The drain current will continue to rise along with V_{gs} (as $R_{ds(on)}$ decreases), until it reaches the load current I_0 at time t_2 . For as long as the drain current is lower than the load current, all the DC voltage V_i must lie across the MOSFET, as the freewheeling diode is still conducting. However, at time t_2 , the voltage across the MOSFET can start to decrease. At this point, the capacitance C_{gs} is completely charged. Thus, the gate-to-source voltage is clamped at what is called the *Miller plateau*. In this period, the gate current charges the gate-to-drain capacitance C_{gd} , also called the Miller capacitance (Section 2.3.2.3). Thus, the gate-to-source voltage is constant while the drain-to-source voltage V_{ds} decreases towards zero. The voltage at which the Miller plateau is found increases with drain current [32].

At time t_3 , the MOSFET enters its ohmic region. Now, the drain-to-source voltage only depends on the on-state gate resistance. The gate-to-source voltage continues to rise until it reaches the voltage V_{gg} [6] [29].

In a realistic MOSFET turn-on transient, the reverse recovery of the diode must be considered. The modified switching characteristics are shown by the red line in Figure 2.13.

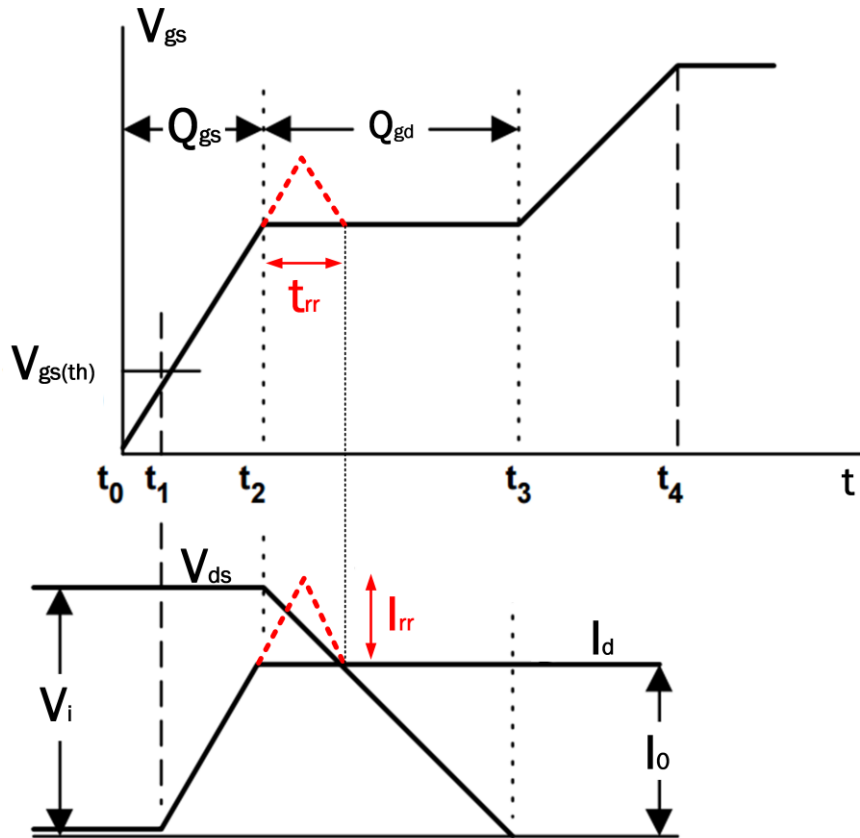


Figure 2.13: MOSFET turn-on transient including diode reverse recovery

The reverse recovery makes the drain current increase beyond I_0 at the time t_2 , due to the reverse-recovery current I_{rr} at diode turn off (Figure 2.3). The increased drain current leads to an increased gate-to-source voltage in the time interval t_{rr} . This diode reverse recovery has an influence on the turn-on switching losses of the MOSFET.

2.3.3.2 Turn-Off Switching Characteristics

This chapter investigates the turn-off transient of the MOSFET. It is assumed that the load current I_0 in Figure 2.11 is flowing through the MOSFET, and that the freewheeling diode is reverse biased. If now the voltage V_{gg} is pulled down to zero (or negative biased in order to speed up the turn-off transient), the turn-off transient of the MOSFET will initiate. The turn-off transient will involve the exact same events as in Figure 2.12, but in reverse order. This gives the turn-off transient in Figure 2.14.

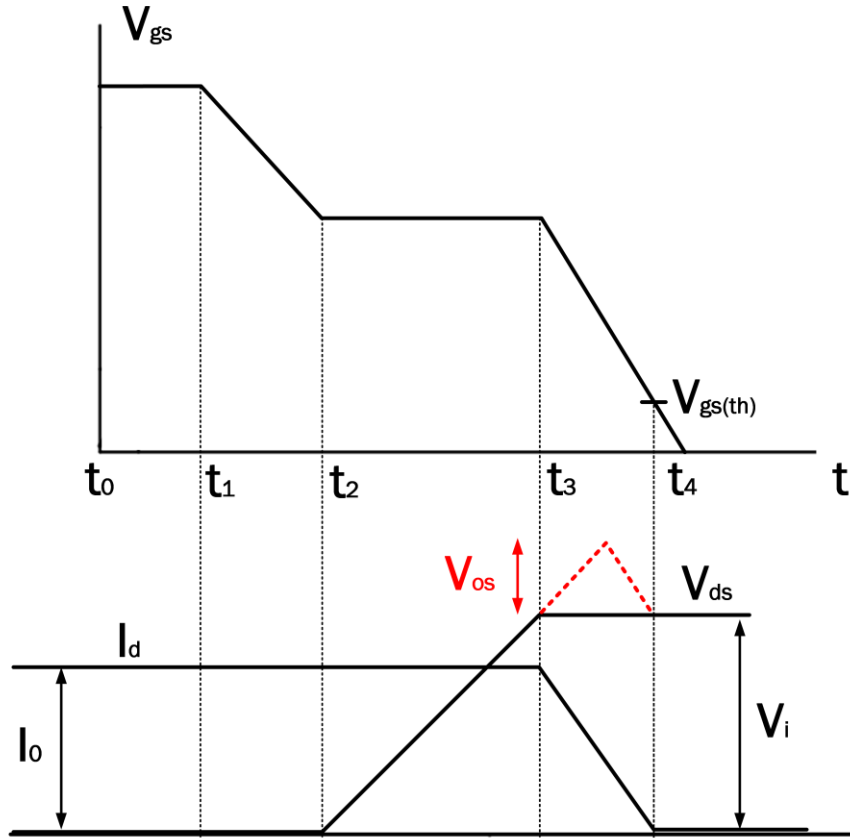


Figure 2.14: MOSFET turn-off transient including voltage overshoot

The ideal switching characteristics is shown in black. However, the actual turn-off switching characteristics often include a considerable voltage overshoot at the time t_3 due to stray inductance L_s in the circuit, and a high drain current derivative di/dt ($V_{os} = L_s \cdot di/dt$). This gives the drain-to-source voltage overshoot given in red. Such a voltage overshoot influences the turn-off switching losses significantly.

2.4 High-Temperature Operation of SiC devices

Section 2.1 discussed the advantages of SiC devices compared to traditional Si devices. It was explained that the wide bandgap of SiC devices makes it possible to operate them at higher junction temperatures than Si devices. In addition, the high thermal conductivity of SiC material is advantageous in high-temperature applications. SiC MOSFETs have proven stable operation at temperatures up to 500 °C [33]. Such extensive temperatures, however, introduce great challenges related to packaging. Improving packages in order to exploit the high-temperature properties of SiC MOSFETs is an ongoing process [34].

3. Theoretical Background

This chapter presents general theory on power converters that is important to have as basis in order to understand the rest of the thesis. The first sections cover different converter designs, including properties and advantages. The last sections present methods on how to analyze switching transients and calculate the power losses in power converter circuits. The chapter ends with a theoretical efficiency comparison of state-of-the-art SiC modules and Si IGBT modules used in a three-phase inverter.

3.1 Step-Down Converter

A step-down converter, also known as a Buck converter, is a DC/DC converter that steps down/reduces the voltage of a DC power supply by the use of switches [6]. A simple step-down converter design is presented in Figure 3.1.

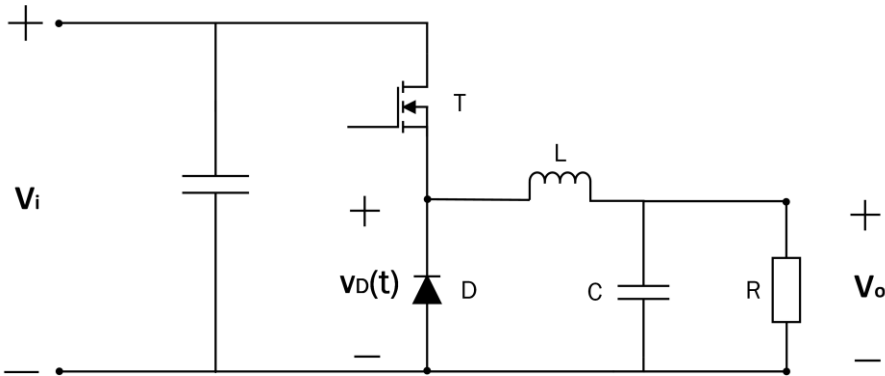


Figure 3.1: Step-down converter

In this step-down converter, the average output voltage V_o across the load is lower than the input voltage V_i at all times. The voltage across the freewheeling diode, $v_D(t)$, is presented as a function of time in Figure 3.2.

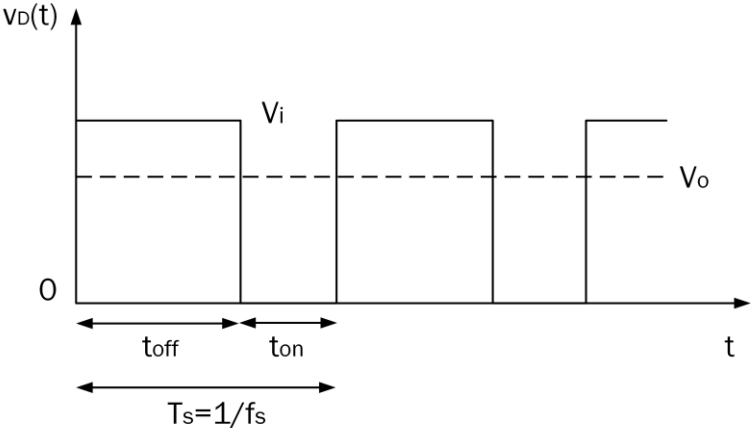


Figure 3.2: Voltage waveforms of step-down converter

The transistor controls the output voltage V_o in the following manner:

$$V_o = D \cdot V_i \quad (3.1)$$

D is the duty ratio, which is defined below:

$$D = \frac{t_{on}}{T_s} \quad (3.2)$$

The duty ratio expresses the time ratio of the switching period that the upper transistor is conducting. The lower diode acts as a freewheeling diode. Thanks to this freewheeling diode, the current can continue to flow through the load even when the upper transistor does not conduct.

Instead of the converter topology in Figure 3.1, the step-down topology in this report will consist of two transistors and two freewheeling diodes by using a half-bridge module. This is called a half-bridge converter.

3.2 Half-Bridge Converter and Synchronous Buck Converter (SBC)

In Figure 3.1, the step-down converter consists of one transistor and one freewheeling diode. A similar step-down behavior can be achieved with a half-bridge module consisting of two transistors and two freewheeling diodes, as depicted in Figure 3.3.

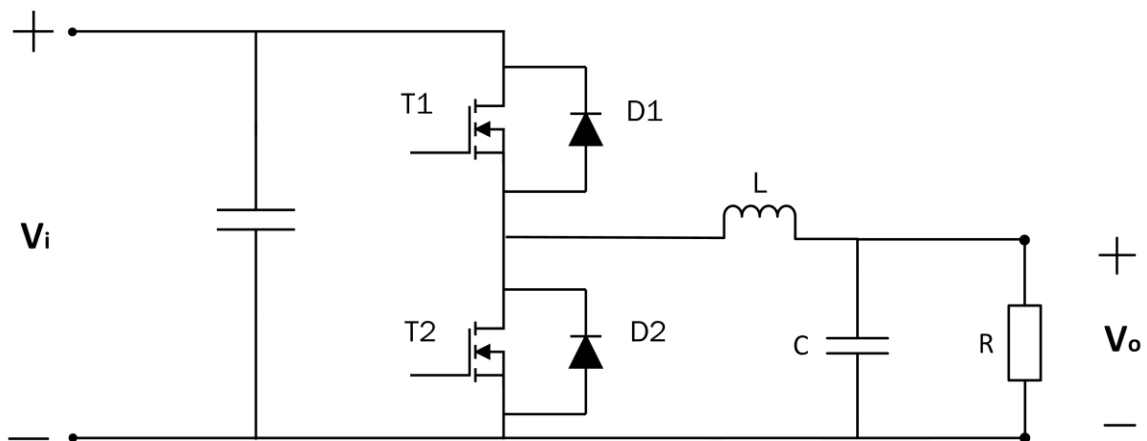


Figure 3.3: Half-bridge converter

In this topology, only one of the two transistors will be switching. The other transistor will always be off. In Figure 3.3, the desired step-down DC/DC conversion is achieved by connecting the load in parallel with the transistor that is off at all times. The corresponding anti-parallel diode will act as a freewheeling diode. If the load is connected in parallel with T2 and D2 as in Figure 3.3, T1 will be the switching transistor. T2 will never conduct, and D2 will be

the freewheeling diode. As the only operating devices are T1 and D2, this type of operation is similar to the one in Figure 3.1.

The half-bridge topology can be exploited even further by means of a synchronous buck converter (SBC). An SBC extends the step-down conversion by exploiting both transistors [35]. In order to operate the circuit in Figure 3.3 as an SBC, the load is connected in parallel with T2 and D2 (Figure 3.3). T1 switches and gives the desired duty cycle and output voltage. Opposite to earlier, T2 will also be switching. The reason for this is that the load current in the SBC freewheels through T2 instead of through D2. Thus, T2 will be on whenever T1 is off. This means that the transistor T2 has to be able to conduct current in both directions, as is the case with MOSFETs [36] [37]. This type of operation reduces the power losses in the step-down conversion, as MOSFETs often have lower on-state losses than diodes, and no threshold voltage. To operate the half-bridge as an SBC demands a more complex control circuit. Blanking time and dead time must be implemented in order for the SBC to operate safely. The diode D2 will conduct only during the short blanking time and dead time when both T1 and T2 are off.

3.3 Three-Phase Voltage Source Inverter

The purpose of a three-phase voltage source inverter is to transform DC voltage in order to supply three-phase AC loads. Such applications can be uninterruptable AC power supplies (UPS) and AC motor loads [6]. A three-phase voltage source inverter consists of three half-bridges, which in total include six transistors and six freewheeling diodes. The three-phase inverter design is presented in Figure 3.4.

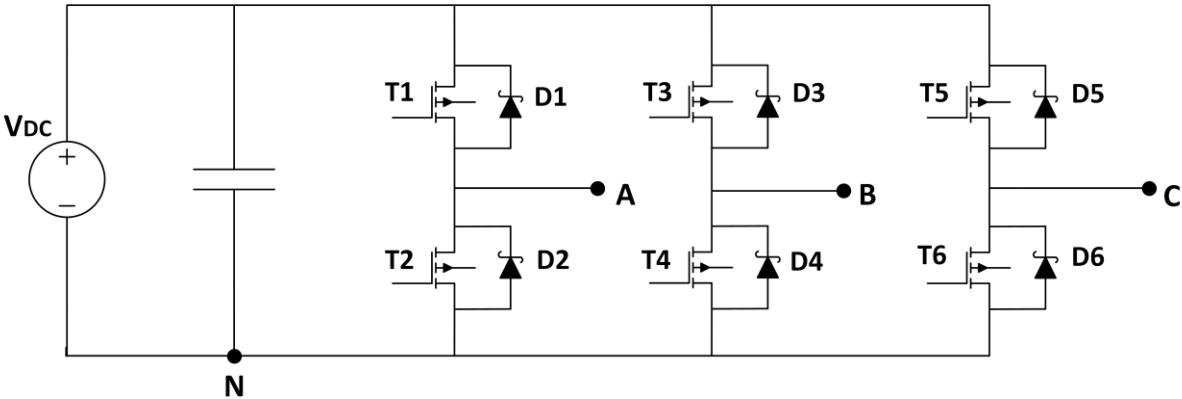


Figure 3.4: Three-phase inverter

The converter design in Figure 3.4 permits to create AC voltages across the loads through the control of the six transistors. In Section 3.1 and 3.2, there were only one or two switching

transistors needed in the converter operation. Thus, the control system in a three-phase inverter is much more complex, as six transistors must be controlled simultaneously. Three balanced AC voltages can be obtained at the output of the three-phase inverter by using square-wave operation or pulse-width modulation (PWM). This section presents the inverter operation of the latter. There are different methods that can be used in order to pulse-width modulate three-phase inverters. The simplest manner is presented in Figure 3.5. In this figure, the PWM signal controlling the six transistor in the three-phase converter is obtained by comparing a triangular voltage v_{tri} with three sinusoidal control voltages with 120° phase shift [6]. Such a PWM operation is called sinusoidal pulse-width modulation (SPWM).

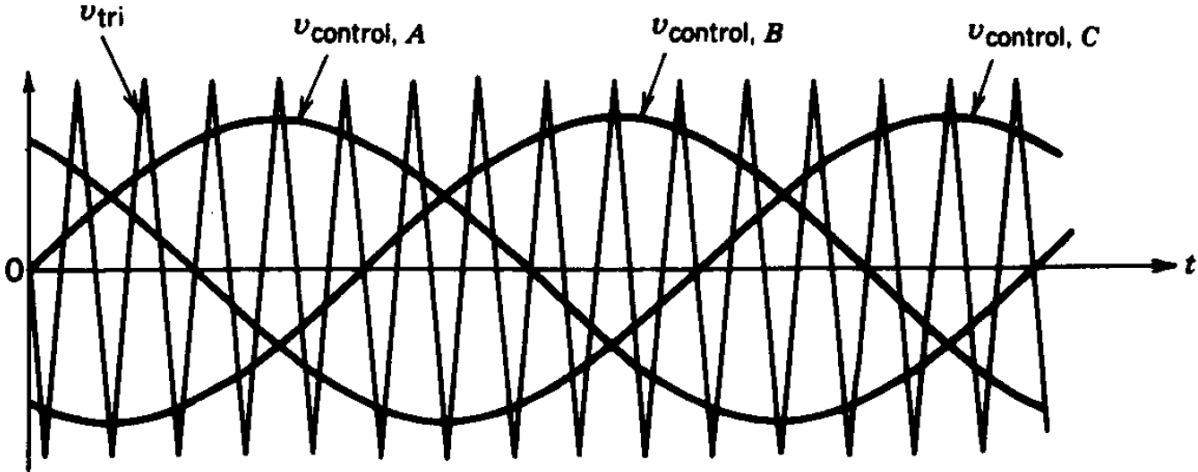


Figure 3.5: Pulse-width modulation [6]

The voltages $v_{control,A}$, $v_{control,B}$ and $v_{control,C}$ are reference voltages determining the control of the three phase legs in Figure 3.4. Thus, they control the output voltages of the inverter. If $v_{control,A}$ exceeds the triangular voltage v_{tri} , transistor T1 is on. Thus, when T1 is in its on state, the voltage between the point A and neutral N v_{AN} will be equal to the input voltage V_{DC} . As long as T1 is on, T2 will be off. However, if $v_{control,A}$ is lower than v_{tri} , T2 will be in its on state. When T2 is on, T1 is off and $v_{AN} = 0$. The same principle holds for the control of the two other phase legs. Thus, the resulting voltages v_{AN} , v_{BN} and $v_{AB} = v_{AN} - v_{BN}$ will be as presented in Figure 3.6 for the same time scale as in Figure 3.5.

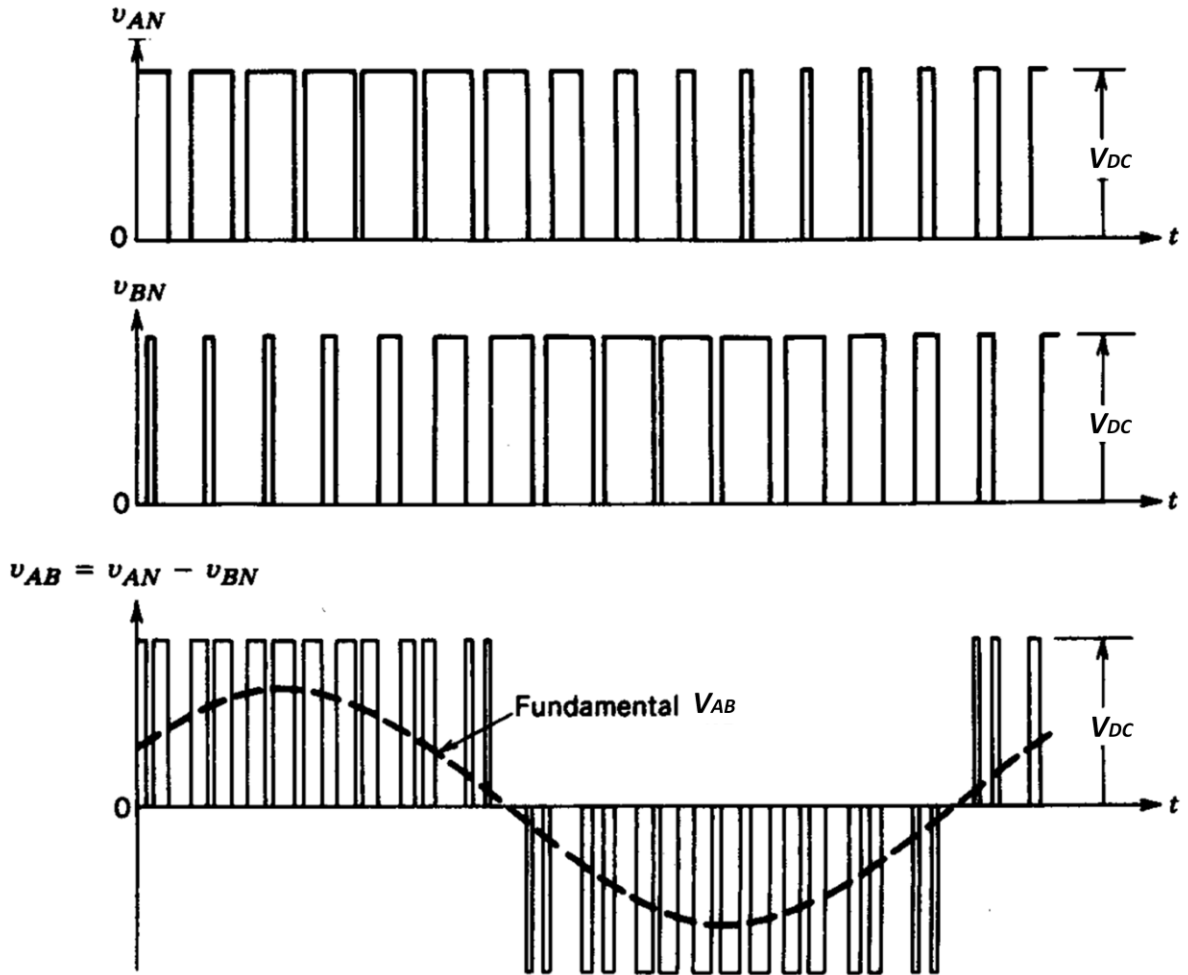


Figure 3.6: Resulting voltages in PWM modulation [6]

Thus, the fundamental of the voltage v_{AB} across the terminals A and B is an AC voltage. It is important to notice that the fundamental of the voltage v_{AB} has the same frequency as the control voltage $v_{control.A}$. Thus, $v_{control.A}$ determines the fundamental frequency f_1 , while the triangular voltage v_{tri} determines the switching frequency f_{sw} of the transistors. The voltages v_{BC} and v_{CA} will be similar to v_{AB} , but 120° and 240° shifted, respectively. This results in the possibility of connecting a balanced AC load across the terminals A, B and C.

The ratio between the peak of the control voltage $v_{control}$ and the peak of the triangular voltage v_{tri} is the modulation depth m . Thus, the following relation holds [6]:

$$m = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \quad (3.3)$$

Thus, if $m = 1$, the amplitude of $v_{control}$ and v_{tri} is the same.

The modulation depth controls the peak of the fundamental-frequency component of the voltage v_{AN} in a three-phase inverter in the following manner [6]:

$$(\hat{V}_{AN})_1 = m \cdot \frac{V_{DC}}{2} \quad (3.4)$$

Thus, the magnitude of the output voltage is controlled by the modulation depth. Having a modulation depth higher than one, $m > 1.0$, is called overmodulation. This would increase the amplitude of the fundamental $(\hat{V}_{AN})_1$. In this area, however, the relation in (3.4) does no longer hold, as the voltage amplitude does not vary linearly with the modulation depth. Overmodulation also causes an increased number of harmonic components in the output voltage.

The line-to-line rms voltage V_{AB} and the phase load rms voltage $V_{A,load}$ across the terminal A and the load neutral n are given by the following relations, which are deduced in [6]:

$$V_{AB} = \frac{\sqrt{3}}{\sqrt{2}} \cdot (\hat{V}_{AN})_1 = \frac{\sqrt{3}}{\sqrt{2}} \cdot m \cdot \frac{V_{DC}}{2} \quad \leftrightarrow \quad V_{A,load} = m \cdot \frac{V_{DC}}{2\sqrt{2}} \quad (3.5)$$

The voltage $v_{A,load}$ has a harmonic spectrum with dominant high-frequency components. Such harmonic components can cause problems related to output power quality. It is possible to eliminate harmonics by [6]:

- Controlling the switching frequency f_{sw} of the transistors
- Combining PWM and square-wave switching in “programmed harmonic elimination switching”

Even though methods of eliminating harmonics are important to consider when designing a three-phase inverter, this will not be further discussed in this thesis.

The control system of a three-phase inverter must include a way of generating blanking time between turn off and turn on of the two transistors in the same phase leg. Such a blanking time is crucial for avoiding shoot through of the DC link, which can occur if both transistors in the same bridge leg are in their on state simultaneously. During this short blanking time, the freewheeling diodes will conduct.

The diode conduction intervals in a three-phase inverter depend on the power factor of the load. With an inductive load, the diodes must conduct whenever the transistor is not able to conduct the inductive current. An example of this is presented in Figure 3.7 and Figure 3.8.

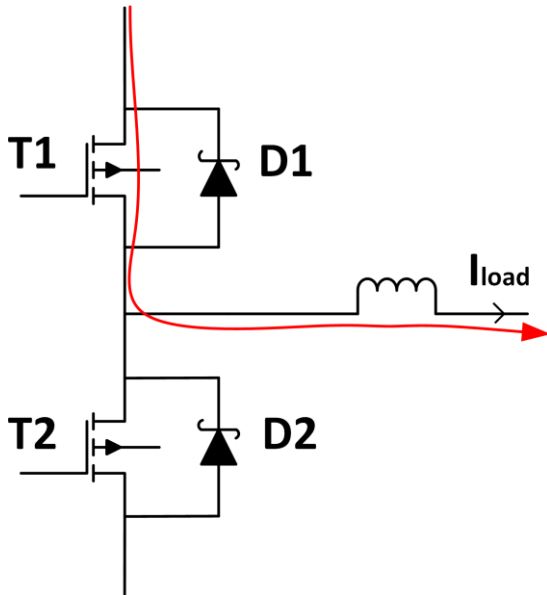


Figure 3.7: Transistor conduction with inductive load

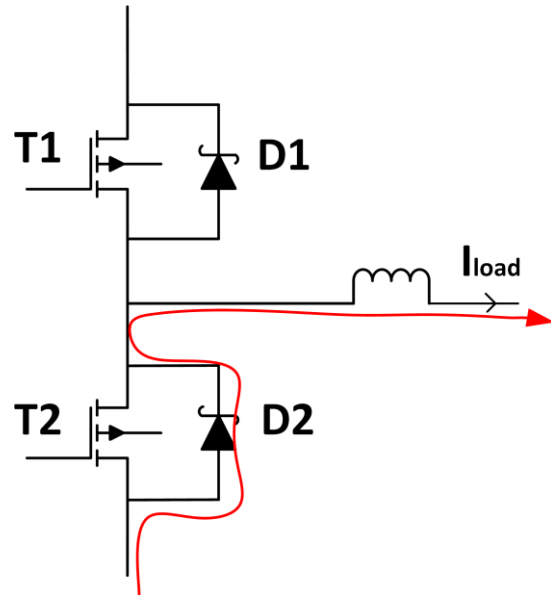


Figure 3.8: Diode conduction with inductive load

It is now assumed that T1 and T2 are IGBTs. In Figure 3.7, the inductive current is flowing through the transistor T1. If T1 is turned off, T2 is turned on after a short blanking time. Due to the inductive load, the load current still has the same direction. As IGBTs are bipolar devices, T2 will not be able to conduct this current. Thus, as shown in Figure 3.8, the diode D2 must conduct this current for as long as the load current is flowing in this direction.

As opposed to bipolar transistors, e.g. IGBTs, unipolar transistors, e.g. MOSFETs, are able to conduct current in both directions. Thus, if a MOSFET is positive biased, both forward conduction and reverse conduction are possible [36] [37]. This means that if T1 and T2 were MOSFETs, some of the current in Figure 3.8 would be able to flow through T2. The current distribution between the diode and the MOSFET would depend on the on-state resistance of the two devices at the given load current.

3.4 Double-Pulse Test

In the experimental part of this report, a double-pulse test (DPT) is conducted in order to obtain and analyze the switching characteristics of the device under test (DUT). A double-pulse test circuit is depicted in Figure 3.9.

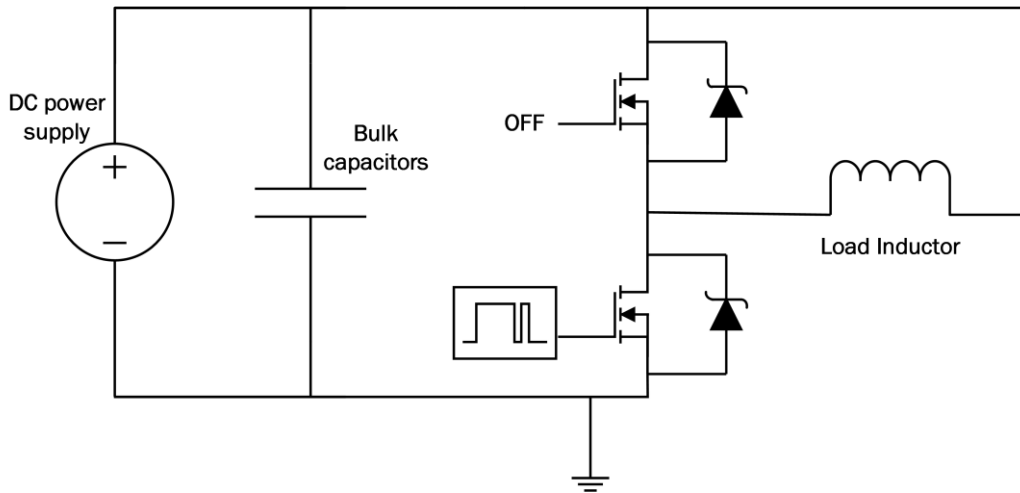


Figure 3.9: Double-pulse setup – Inductive load

The double-pulse test is used to observe the switching transients of a transistor without having to heat the device. The double-pulse test is normally done with a purely inductive load, i.e., a load inductor [24]. The first pulse should turn on the lower transistor in Figure 3.9, and charge a current through the inductor. This means that the first pulse should be a wide pulse, which charges the load current to the magnitude that is interesting to analyze. Then, a short break followed by a second short pulse should appear. Such a double pulse gives the possibility of analyzing the rising edge (turn on) and the falling edge (turn off) of a hard-switching transient of the transistor at the exact transistor current that is desired. A double-pulse signal is depicted in Figure 3.10.

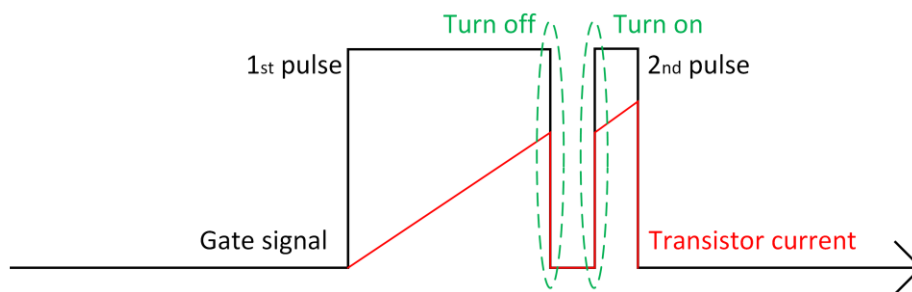


Figure 3.10: Double-pulse signal

By adjusting the pulse width of the first pulse supplied to the gate driver, it is possible to adjust the transistor current magnitude. The double pulses are supplied at a very low frequency, e.g. 1 Hz. This gives the transistor time to remove the generated heat, and the load inductor time to discharge between the double pulses. The transistor current will have a waveform similar to the red signal in Figure 3.10, with a purely inductive load.

3.5 MOSFET Switching Transients

The switching transients of SiC power MOSFETs are very similar to the switching transients of Si Power MOSFETs. This section explains the basic rules that are used when analyzing the switching transients in this thesis.

3.5.1 Switching Times and Derivatives

The general and simplified hard-switching transients of a double-pulse test setup similar to the one in Figure 3.9, with an inductive load, is depicted in Figure 3.11. This figure presents the turn-on and turn-off transients of the drain-to-source voltage V_{ds} , the drain current I_d and the gate-to-source voltage V_{gs} , in addition to important switching time parameters.

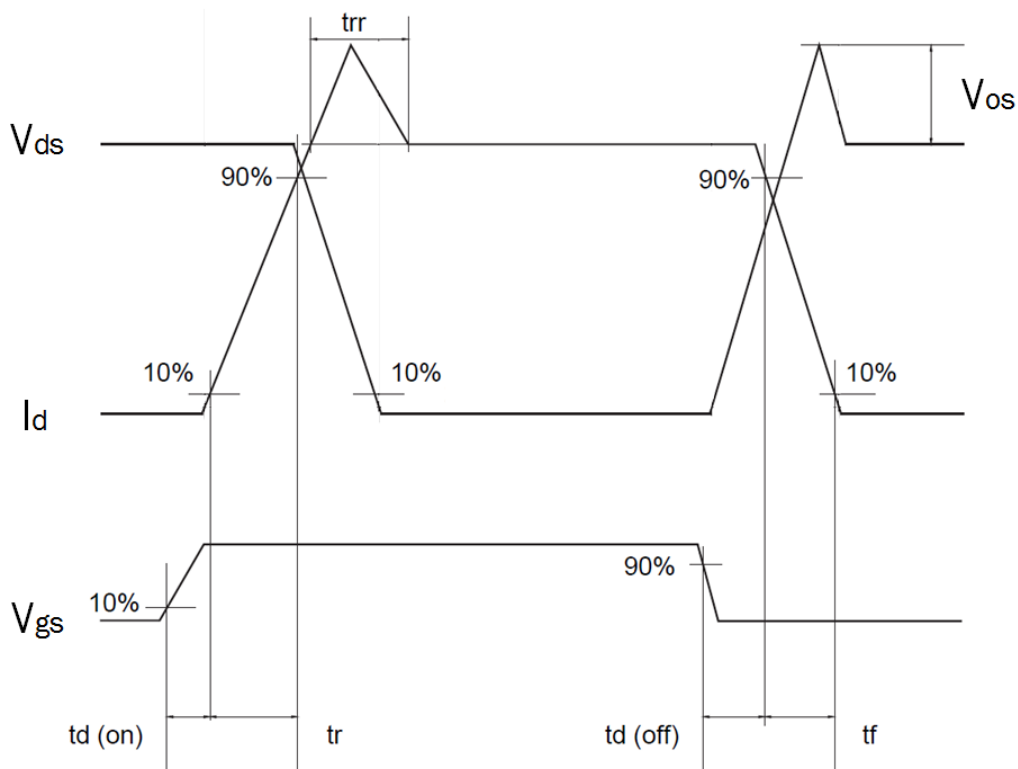


Figure 3.11: SiC MOSFET switching transient [38]

The switching time parameters in Figure 3.11 are [31]:

- $t_{d(on)}$ – **Turn-on delay time.** This is the period from when the gate-to-source voltage reaches 10 % of its final value, to when the drain current reaches 10 % of its final value during turn on.
- $t_{d(off)}$ – **Turn-off delay time.** This is the period from when the gate-to-source voltage drops to 90 % of its on-state voltage, to when the drain current drops to 90 % of its on-state value during turn off.
- t_r – **Current rise time.** The current rise time is the period when the drain current rises from 10 % to 90 % of its final on-state value during turn on.

- **t_f – Current fall time.** The current fall time is the period when the drain current drops from 90 % to 10 % of its on-state value during turn off.
- **t_{rr} – Diode reverse recovery time.** The time it takes the diodes to discharge the stored reverse recovery charge.

The total turn-on and turn-off switching times are denoted as:

$$t_{on} = t_{d(on)} + t_r \quad \text{and} \quad t_{off} = t_{d(off)} + t_f \quad (3.6)$$

The two following parameters are also commonly used:

- **t_{rv} – Voltage rise time.** The voltage rise time is the period when the drain-to-source voltage rises from 10 % to 90 % of its final off-state value during turn off.
- **t_{fv} – Voltage fall time.** The voltage fall time is the period when the drain-to-source voltage drops from 90 % to 10 % of its off-state value during turn on.

The voltage derivative dv/dt and the current derivative di/dt during switching are often used when comparing the switching speed of transistors. In this report, dv/dt and di/dt are measured between 10% and 90% of nominal values of voltage and current respectively. Thus, for a given drain-to-source voltage V_{ds} , the voltage rise time during MOSFET turn off is given as:

$$\frac{dv}{dt_{off}} = \frac{0.9 \cdot V_{ds} - 0.1 \cdot V_{ds}}{t_{rv}} = \frac{0.8 \cdot V_{ds}}{t_{rv}} \quad (3.7)$$

di/dt is calculated in the same manner during MOSFET turn on.

$$\frac{di}{dt_{on}} = \frac{0.9 \cdot I_d - 0.1 \cdot I_d}{t_r} = \frac{0.8 \cdot I_d}{t_r} \quad (3.8)$$

This report only includes calculations on dv/dt during MOSFET turn off and di/dt during MOSFET turn on. The reason for this is that the voltage waveform during turn off and the current waveform during turn on are easiest to compare for different conditions, as the development of these waveforms is the same for different conditions. The switching speeds and derivatives, however, change significantly for different conditions, which makes these waveforms well suited for comparison. This is illustrated in Figure 3.12 and Figure 3.13, which are turn-off transients obtained in laboratory experiments at 600 V drain-to-source voltage and 30 A and 120 A drain currents respectively.

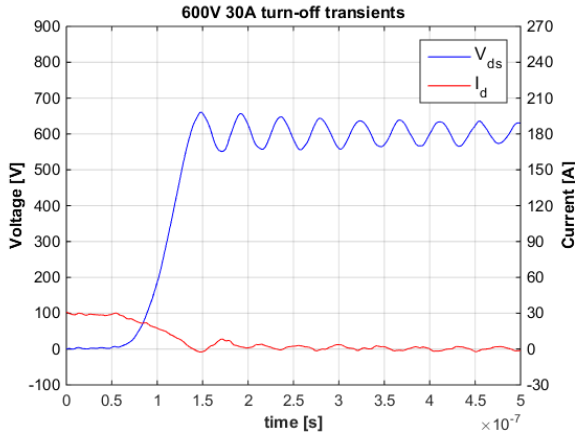


Figure 3.12: 600 V 30 A turn off

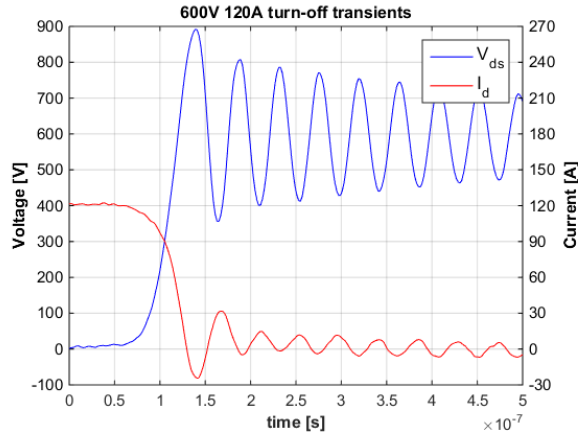


Figure 3.13: 600 V 120 A turn off

While the voltage transients have very similar development in the two figures, the current transients are very different. This is why it is chosen to investigate the voltage transient during turn off. The turn-on transients for the same conditions are presented in Figure 3.14 and Figure 3.15.

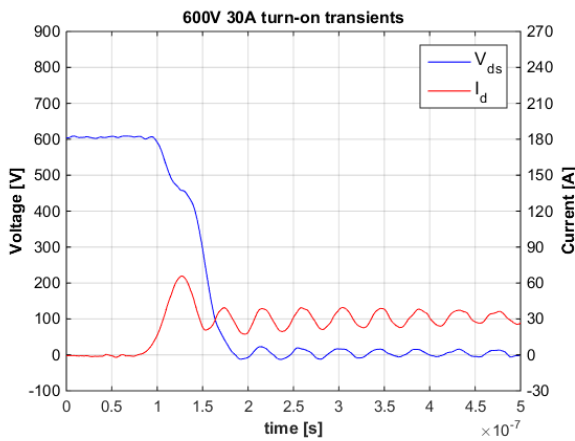


Figure 3.14: 600 V 30 A turn on

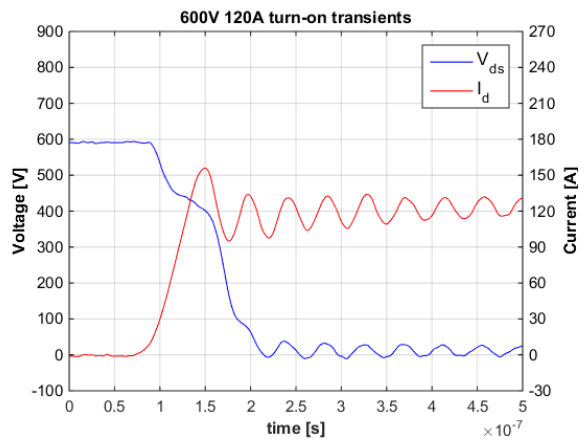


Figure 3.15: 600 V 120 A turn on

At MOSFET turn on, the current transients have similar development for different drain currents. The drain-to-source voltage, on the other hand, has very different development for different drain currents. Thus, it is chosen to examine mainly the drain current at MOSFET turn on, and the drain-to-source voltage at MOSFET turn off.

3.5.2 Electromagnetic Interference

The switching transients of SiC MOSFETs can be very fast, leading to high voltage and current derivatives. Due to parasitics in the circuit, the fast transients can lead to high overshoots, long-lasting ringing, power losses and other switching stresses. Such effects of switching can lead to electromagnetic interference (EMI) in the control circuit and other electronics located close to

the switch. EMI is normally noise that occurs in electrical signals due to inductive coupling between conductors [39] [40].

EMI-caused noise can be avoided by using decoupling (bypass) capacitors across all voltage inputs that must be stable. Other solutions reducing EMI-caused noise are EMI filters and shielding [39].

3.5.3 Hard Switching and Soft Switching

The switching transients in Figure 3.11 are denoted as hard-switching transients. Switching in this manner causes transistor stresses such as extensive power losses and current- and voltage spikes during the switching transients. These stresses could be dangerous and in worst case destroy the transistor. The high di/dt and dv/dt could also cause long-lasting parasitic ringing and EMI, as explained in the previous section. Even though hard switching could cause high switching stresses and increased power losses, hard switching gives low switching times and the possibility of switching at high frequencies. The switching stresses caused by hard switching can be minimized by [41]:

- Reducing parasitic inductance and capacitance in the circuit layout
- Reducing di/dt and dv/dt by implementing snubbers
- Reducing di/dt and dv/dt by modifying the gate driver
- Soft switching

To reduce parasitic inductance and capacitance is always an important part of designing a circuit layout. Implementing snubbers and modifying the gate driver, on the other hand, can cause new switching stresses. Soft switching can be a solution to reducing switching stresses without causing any new problems. The aim of soft switching is to reduce power losses and EMI by forcing zero-voltage or zero-current switching transients [40] [41]. Thus, the aim is to have zero overlap between current and voltage during switching. Zero-voltage and zero-current switching can be obtained by modifying the converter layout. Soft-switching technology can be smart to implement in both DC and AC conversion.

As an example, soft switching can be obtained in the half-bridge converter in Figure 3.3 by implementing the modifications shown in Figure 3.16.

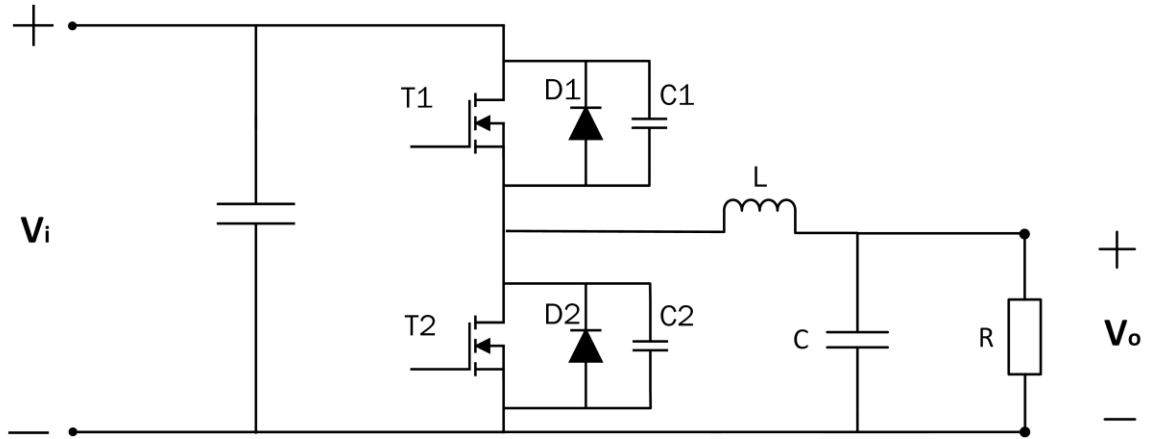


Figure 3.16: Soft switching half-bridge converter

The addition of the capacitors C1 and C2 makes it possible to achieve zero-voltage switching in both T1 and T2 in SBC mode. The capacitors C1 and C2 slow down the voltage transients, which makes it possible for the current to finish its transients with zero voltage across the transistor [41].

It is possible to achieve a soft turn-off transient of a transistor by implementing a turn-off snubber. This will be explained in Section 4.7.1.

3.6 Power Losses in Single MOSFETs and SBDs

A double-pulse test of a MOSFET makes it possible to determine the switching power losses of a high-frequency switching MOSFET. In a double-pulse test, it is possible to analyze both the turn-on and the turn-off transients of the transistor at a given drain-to-source voltage and drain current. This makes it possible to determine the total switching power losses in the transistor. The power loss $p_{T,loss}$ in a single MOSFET is given by [42]:

$$p_{T,loss}(t) = v_{ds}(t) \cdot i_d(t) \quad (3.9)$$

v_{ds} is the drain-to-source voltage and i_d is the drain current of the switching transistor. When the transistor is off, i_d is close to zero, due to very low leakage current. The off-state conduction losses are thus negligible. When the transistor is on, there are conduction power losses due to the on-state drain-to-source resistance $R_{ds(on)}$ of the transistor. The conduction power losses are given by [42]:

$$p_{T,cond}(t) = R_{ds(on)} \cdot i_d^2(t) \quad (3.10)$$

The conduction losses are not easily found through the double-pulse test, as the drain current is constantly increasing due to the purely inductive load. Thus, the double-pulse test does not

represent the transistor conduction losses in a good way. However, for a high-frequency switching transistor, the average value during one switching period T_{sw} can be found using (3.11) [42]:

$$P_{T,cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{ds(on)} \cdot i_d^2(t) dt = R_{ds(on)} \cdot I_{d,rms}^2 \quad (3.11)$$

$I_{d,rms}$ is the RMS drain current in the transistor.

On the other hand, the transistor switching losses are easily determined using the double-pulse test. The switching losses in the transistor occur during turn on and turn off. The ideal switching transients of the MOSFET are depicted in Figure 3.17.

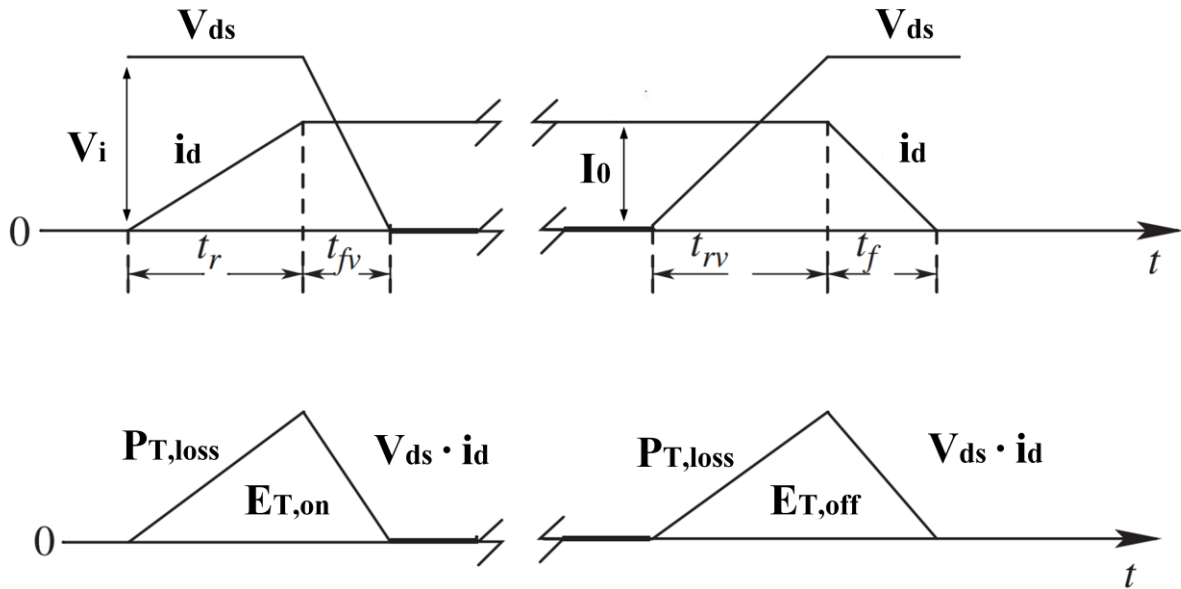


Figure 3.17: Switching power losses in a MOSFET [41]

The ideal switching energy losses during turn-on and turn-off respectively can be found using the following equations [42]:

$$E_{T,on} = \int_0^{t_r+t_{fv}} p_{T,loss}(t) dt = \int_0^{t_r+t_{fv}} v_{ds}(t) \cdot i_d(t) dt \quad (3.12)$$

$$E_{T,off} = \int_0^{t_f+t_{rv}} p_{T,loss}(t) dt = \int_0^{t_f+t_{rv}} v_{ds}(t) \cdot i_d(t) dt \quad (3.13)$$

However, the switching transients obtained in laboratory experiments are not ideal. Thus, the total turn-on and turn-off switching times might be different from $t_r + t_{fv}$ and $t_f + t_{rv}$. If this

is the case, (3.12) and (3.13) do not hold. Thus, $E_{T,on}$ and $E_{T,off}$ should be calculated by investigating the power waveform $P_{T,loss}$ directly.

$E_{T,on}$ and $E_{T,off}$ can be found in a double-pulse test, using the integration feature of the oscilloscope. These energy losses will remain the same independently of the switching frequency of the transistor. Assuming that the transistor is switching at a frequency f_{sw} , the total switching power losses in the transistor are given by [42]:

$$P_{T,sw} = f_{sw} \cdot (E_{T,on} + E_{T,off}) \quad (3.14)$$

The freewheeling SBD in Figure 3.9 will also contribute to the power losses in a double-pulse test setup. By using the same principle as in (3.11), the diode conduction losses are given by:

$$P_{D,cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} (V_{F0} \cdot i_F(t) + R_F \cdot i_F^2(t)) dt = V_{F0} \cdot I_{F,av} + R_F \cdot I_{F,rms}^2 \quad (3.15)$$

V_{F0} is the diode threshold voltage and R_F is the SBD on-state resistance. $I_{F,av}$ is the average diode current and $I_{F,rms}$ is the RMS diode current. The diode conduction losses at a given current are normally not determined in a double-pulse test. However, they are quite easily determined using the diode freewheeling current during the off state of the transistor, which is equal to the load current.

The switching losses in an SBD occur mainly at diode turn off, due to the reverse recovery of the charge stored in the junction capacitance (Section 2.3.1). The diode turn-on losses are negligible in comparison [43]. Thus, the total switching losses in the diode are given by:

$$P_{D,sw} = f_{sw} \cdot E_{D,off} \quad (3.16)$$

The turn-off reverse recovery of the diode also affects the turn on of the MOSFET, as the reverse-recovery current increases the turn-on power losses of the transistor [36] [44].

3.7 Power Losses in a PWM Modulated Power Inverter

The power losses in a power converter can be divided into three categories: gate driver, conduction and switching power losses. These losses are located in different parts of the circuit and in different devices. This section discusses the losses in a three-phase voltage source inverter, consisting of three MOSFET phase legs. Such a voltage source inverter is depicted in Figure 3.18:

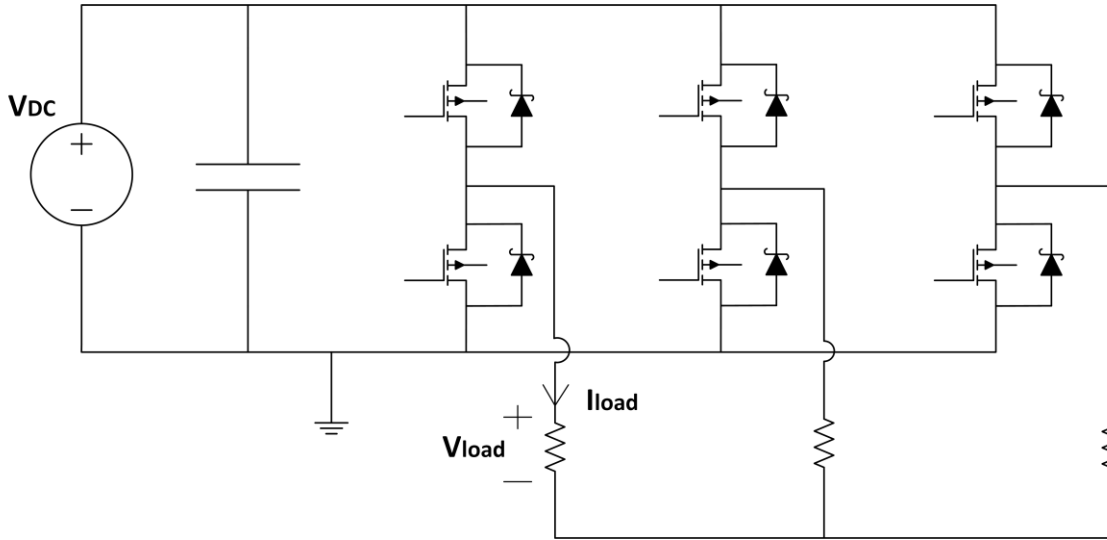


Figure 3.18: Three-phase inverter with load

In this section, it is assumed SPWM modulation. This mode of operation was thoroughly explained in Section 3.3. It is also assumed that the three-phase inverter is full SiC consisting of SiC MOSFETs and SiC SBDs.

3.7.1 Gate Driver Losses

The gate driver losses of a MOSFET are directly related to charging and discharging of the gate input capacitance, C_{iss} [45]. The gate charge losses in each gate driver circuit can be calculated as:

$$P_{GATE} = V_{DRV} \cdot Q_G \cdot f_{DRV} \quad (3.17)$$

V_{DRV} is the gate drive voltage of the MOSFET, Q_G is the total gate charge required to charge C_{iss} and f_{DRV} is the gate driver frequency. Q_G is the integral of the gate charge current during turn on, or the gate discharge current during turn off. In datasheets, total gate charge is normally given as a function of gate-to-source voltage. Total gate charge varies slightly with drain current and drain-to-source voltage [31]. As SiC MOSFETs only need short current pulses in order to turn on or off, it is assumed that there are no conduction losses in the gate driver circuit.

3.7.2 Conduction Losses

The conduction losses in a three-phase inverter are related to the conduction losses in the SiC MOSFETs and the SiC SBDs. In [6], it is stated that nearly all the conduction losses in a MOSFET at normal operating conditions are dissipated when the MOSFET is in its on state, since the leakage current in its off state is extremely low.

By using [46] and [47], and the fact that the MOSFET is a unipolar device with only resistive losses (as opposed to bipolar devices such as BJTs, which also have losses related to the threshold voltage), the following on-state conduction losses $P_{T,cond}$ in the MOSFET can be derived:

$$P_{T,cond} = \frac{1}{2} \cdot \frac{R_{ds(on)}}{4} \cdot \hat{I}_{load}^2 + m \cdot \cos \varphi \cdot \frac{R_{ds(on)}}{3\pi} \cdot \hat{I}_{load}^2 \quad (3.18)$$

The parameters in Figure 3.18 and (3.18) are given below:

- $R_{ds(on)}$ – The total on-state drain-to-source resistance
- \hat{I}_{load} – The amplitude of the load current fundamental (Figure 3.18)
- $\cos \varphi$ – The power factor of the inverter
- m – The modulation depth, given by the relation in (3.6)
- \hat{V}_{load} – The amplitude of the fundamental output phase voltage across the load, given by the relation in (3.5)
- V_{DC} – The input DC voltage.

The same line of thought can be used to derive the conduction losses in the SBD. The following equation represents the conduction losses $P_{D,cond}$ in the SBD [46] [47]:

$$P_{D,cond} = \frac{1}{2} \cdot \left(\frac{V_{F0}}{\pi} \cdot \hat{I}_{load} + \frac{R_F}{4} \cdot \hat{I}_{load}^2 \right) - m \cdot \cos \varphi \cdot \left(\frac{V_{F0}}{8} \cdot \hat{I}_{load} + \frac{R_F}{3\pi} \cdot \hat{I}_{load}^2 \right) \quad (3.19)$$

V_{F0} is the diode threshold voltage and R_F is the total on-state resistance between the anode and the cathode of the SBD. The off-state conduction losses in SBDs (due to leakage current) are negligible, as they are in MOSFETs.

3.7.3 Switching Losses

The switching losses in an inverter are the losses related to changing the state of a device. During a switching transient the drain current i_d and drain-to-source voltage v_{ds} will both be higher than zero and overlap for some period, as depicted in Figure 3.11. This causes a power dissipation in the MOSFET, due to $p_{T,loss} = v_{ds} \cdot i_d$. The transistor switching losses occur during both turn-off and turn-on switching. In addition, the SBD has switching losses related to the reverse-recovery current during diode turn off, as explained in Section 3.6. The averaged switching loss in an SPWM controlled transistor $P_{T,sw}$ is [46]:

$$P_{T,sw} = \frac{1}{\pi} \cdot f_{sw} \cdot (E_{T,on} + E_{T,off}) \quad (3.20)$$

f_{sw} is the switching frequency, $E_{T,on}$ is the turn-on switching energy loss and $E_{T,off}$ is the turn-off switching energy loss. $E_{T,on}$ and $E_{T,off}$ vary with both the load current \hat{I}_{load} and the DC voltage V_{DC} . These values can be measured directly in the laboratory, or they can be found as a function of \hat{I}_{load} in the datasheet. The problem with this approach is that the values of $E_{T,on}$ and $E_{T,off}$ often are given at a fixed DC voltage V_{DC} . This means that it is not possible to find the switching energy loss at a certain operating point. In order to solve this difficulty, the following approximation can be used in order to calculate $P_{T,sw}$ [47]:

$$P_{T,sw} = \frac{1}{\pi} \cdot f_{sw} \cdot (E_{T,on} + E_{T,off}) \cdot \frac{V_{DC} \cdot \hat{I}_{load}}{V_{ref} \cdot \hat{I}_{ref}} \quad (3.21)$$

V_{ref} and \hat{I}_{ref} are the DC voltage and load current amplitude at which the switching energy losses given in the datasheet were measured. In the same manner as in (3.20) and (3.21), the averaged switching loss of the diode $P_{D,sw}$ can be found. As explained in Section 3.6, the diode turn-on switching losses are neglected:

$$P_{D,sw} = \frac{1}{\pi} \cdot f_{sw} \cdot E_{D,off} \cdot \frac{V_{DC} \cdot \hat{I}_{load}}{V_{ref} \cdot \hat{I}_{ref}} \quad (3.22)$$

By using (3.21) and (3.22), an expression of the total switching losses in one diode-transistor pair is found:

$$P_{sw} = P_{T,sw} + P_{D,sw} = \frac{1}{\pi} \cdot f_{sw} \cdot (E_{T,on} + E_{T,off} + E_{D,off}) \cdot \frac{V_{DC} \cdot \hat{I}_{load}}{V_{ref} \cdot \hat{I}_{ref}} \quad (3.23)$$

In this expression, $E_{T,on}$, $E_{T,off}$ and $E_{D,off}$ are measured at the reference load current \hat{I}_{ref} and reference DC voltage V_{ref} .

3.7.4 Total Inverter Losses and Efficiency

By using Sections 3.7.1, 3.7.2 and 3.7.3, the total power losses in a SPWM modulated SiC inverter can be calculated as:

$$P_{loss} = 6 \cdot (P_{GATE} + P_{T,cond} + P_{D,cond} + P_{T,sw} + P_{D,sw}) \quad (3.24)$$

The three-phase output power of the inverter is given in (3.25) [6]. The substitution for V_{load} comes from (3.5).

$$P_{out} = 3 \cdot V_{load} \cdot I_{load} = 3 \cdot m \cdot \frac{V_{DC}}{2\sqrt{2}} \cdot \frac{\hat{I}_{load}}{\sqrt{2}} \quad (3.25)$$

The total efficiency of the three-phase inverter is given by:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \quad (3.26)$$

3.8 Theoretical Efficiency Comparison of State-of-the-art Half-Bridge Modules

This section covers eight different SiC half-bridge modules from four different manufacturers and a comparison of their performances. All of them are full SiC half-bridge modules consisting of SiC MOSFET transistors. In order to test the modules on different grounds, three different power loss comparisons will be conducted. Some of the modules include SiC SBD freewheeling diodes, while others only include the intrinsic SiC body diodes. Consequently, this comparison will only investigate the switching and conduction losses in the SiC MOSFETs. The diode losses are ignored due the fact that not all of the modules include SiC SBDs. Gate driver losses are neglected due to their low value compared to the losses in the power circuit. A state-of-the-art Si IGBT half-bridge module is also added to the comparison in order to compare with the SiC modules. The three-phase inverter that will be investigated is given in Figure 3.18.

3.8.1 Fixed Operating Point – Total Power Losses and Efficiency

The first comparison will be conducted at a fixed operating point. The following specifications are made on the DC voltage V_{DC} , the load current RMS value I_{load} and junction temperature T_j :

- $V_{DC} = 600 \text{ V}$
- $I_{load} = 100 \text{ A}$
- $T_j = 150 \text{ °C}$

These conditions will be satisfied for as long as the datasheets have sufficient data. Disregarding the diode losses and the gate driver losses, the total inverter losses consist only of switching losses and conduction losses in the SiC MOSFETs. By using (3.18) and (3.21), the total losses in one transistor is given by (3.27):

$$\begin{aligned} P_{T,tot} &= P_{T,cond} + P_{T,sw} \\ \Rightarrow P_{T,tot} &= \frac{1}{2} \cdot \frac{R_{ds(on)}}{4} \cdot \hat{I}_{load}^2 + m \cdot \cos \varphi \cdot \frac{R_{ds(on)}}{3\pi} \cdot \hat{I}_{load}^2 \\ &+ \frac{1}{\pi} \cdot f_{sw} \cdot (E_{T,on} + E_{T,off}) \cdot \frac{V_{DC} \cdot \hat{I}_{load}}{V_{ref} \cdot \hat{I}_{ref}} \end{aligned} \quad (3.27)$$

There are only three of the parameters above that vary from module to module and need to be found in the datasheet. They are $R_{ds(on)}$, $E_{T,on}$ and $E_{T,off}$. In order to find the values of these parameters, each module's datasheet and the specified values for V_{DC} , I_{load} and T_j are used. The eight chosen SiC modules and the Si IGBT module are presented together with their relevant electrical properties and ratings in Table 3.1:

Table 3.1: Electrical properties of the eight chosen SiC Modules and the Si IGBT

| Manufacturer | Part number | I_D [A] | V_{DSS} [V] | $R_{ds(on)}$ [m Ω] | $E_{T,on}$ [mJ] | $E_{T,off}$ [mJ] |
|---------------|-----------------------|-----------|---------------|----------------------------|-----------------|------------------|
| Rohm | BSM120D12P2C005 | 120 | 1200 | 25 | 2.8 | 1.8 |
| Rohm | BSM180D12P2C101 | 180 | 1200 | 17.5 | 5 | 3.5 |
| Rohm | BSM300D12P2E001 | 300 | 1200 | 11 | 4.5 | 2.5 |
| Microsemi | APTMC120 AM08CD3AG | 250 | 1200 | 16 | 2.4 | 1 |
| Microsemi | APTMC120 AM09CT3AG | 295 | 1200 | 11 | 2.7 | 1.2 |
| Cree | CAS300M17BM2 | 225 | 1700 | 8* | 6* | 2.4* |
| Cree | CAS300M12BM2 | 404 | 1200 | 5** | 2.9** | 1.2** |
| Semikron | SKM500MB120SC | 541 | 1200 | 5.7*** | 10.3*** | 4.7*** |
| Semikron IGBT | SKM 400GB125D | 400 | 1200 | 7.6 ($R_{ce(on)}$) | 17 | 18 |

* Values for $T_j = 25$ °C and $V_{DC} = 900$ V

** Values for $T_j = 25$ °C

*** Values for $I_{load} = 250$ A

This comparison does not consider neither the gate resistances $R_{g,on}$ and $R_{g,off}$, nor the gate-to-source voltage V_{gs} at which the information in the datasheets was obtained. The reason for this is that these parameters vary a lot from datasheet to datasheet. Nevertheless, these three parameters would normally affect the total conduction losses and switching losses in the modules, and should be considered if possible.

Connecting three SiC half-bridge modules in parallel, as depicted in Figure 3.18, forms a 3-phase inverter. Thus, such a circuit consists of six SiC MOSFETs. The total power losses in a three-phase inverter, disregarding diodes and gate drivers, are from (3.24):

$$P_{loss} = 6 \cdot P_{T,tot} \quad (3.28)$$

Modulation depth and power factor are set to $m = 1$ and $\cos \varphi = 0,9$ respectively. The total inverter losses are calculated for frequencies in the range $f_{sw} \in [5, 50] \text{ kHz}$. The calculations and figures are done in Microsoft Excel. The results for all eight modules are presented in Figure 3.19. As mentioned, a state-of-the-art Si IGBT module is added to the figure in order to compare with the SiC modules. It is important to note that all switching energy losses presented in the module datasheet are given at $T_j = 125 \text{ }^\circ\text{C}$ and $T_j = 150 \text{ }^\circ\text{C}$, except for in the Cree module datasheet, where the information is given at $T_j = 25 \text{ }^\circ\text{C}$.

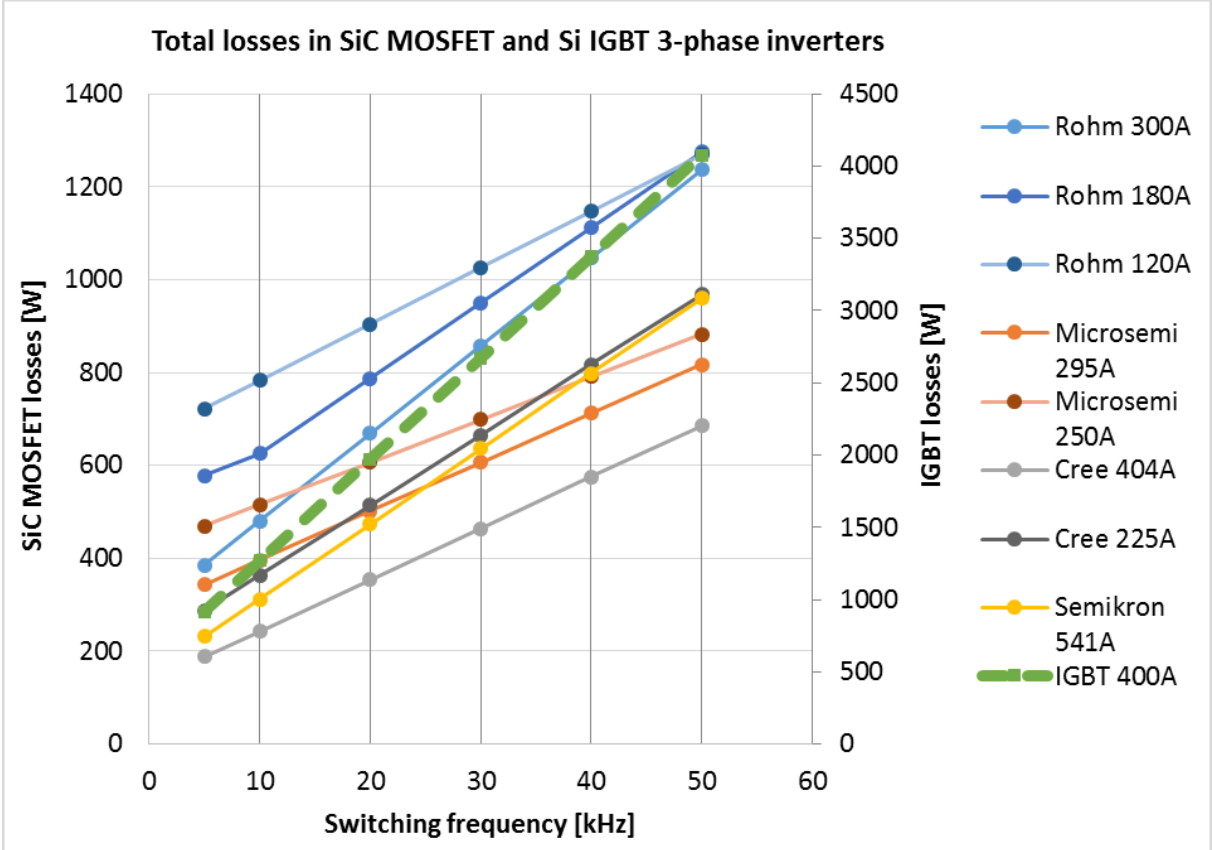


Figure 3.19: Total losses in SiC MOSFET and IGBT three-phase inverters

It is apparent that the IGBT 3-phase inverter (secondary y-axis) has much higher power losses than all the SiC MOSFET 3-phase inverters (primary y-axis) at equal conditions. Due to high switching losses in the IGBT module, this is particularly true at high frequencies. The three SiC MOSFET modules from Rohm (in blue) have the highest power losses compared to the other manufacturers. The reason for this might be that all the full SiC modules from Rohm have a lower current rating than the other modules included in this note. Thus, the on-state resistance is higher in these modules. In Figure 3.20, the efficiency of the three-phase inverters is presented as a function of switching frequency.

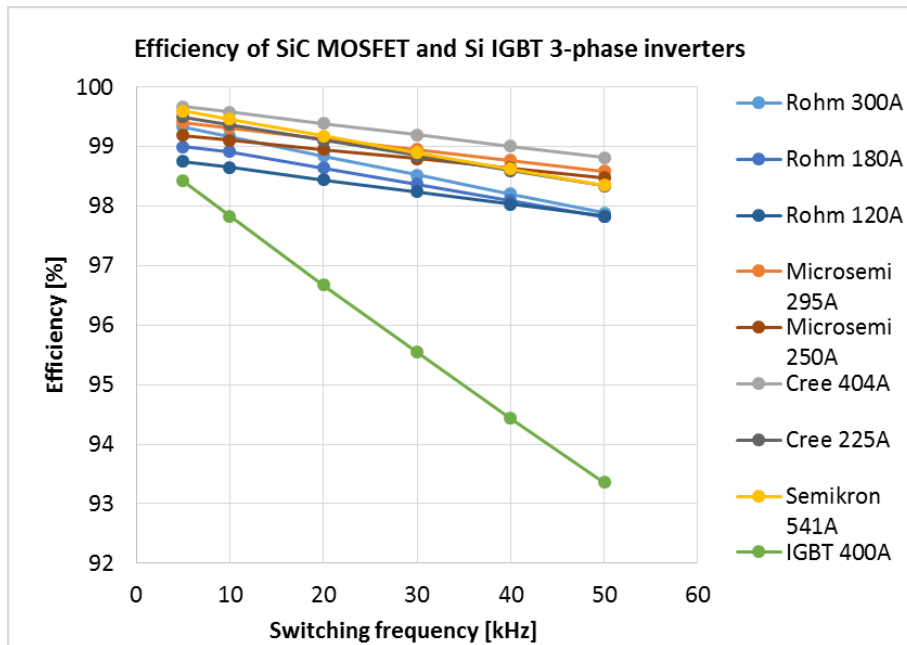


Figure 3.20: Efficiency of SiC MOSFET and IGBT three-phase inverters

The equations (3.25), (3.26) and (3.28) were used in the calculation. It is found that nearly all the SiC three-phase inverters have more than 98 % efficiency for all frequencies. The Si IGBT three-phase inverter has a much lower efficiency of about 93 % at $f_{sw} = 50 \text{ kHz}$.

3.8.2 Fixed Inverter Power Losses – Maximum Drain Current

The total power loss in the 3-phase inverter is now fixed at $P_{loss} = 1000 \text{ W}$. I.e., the total power loss is not allowed to exceed this value. By iterating over the load current I_{load} , the maximum load current for a given switching frequency is obtained. This gives the result in Figure 3.21.

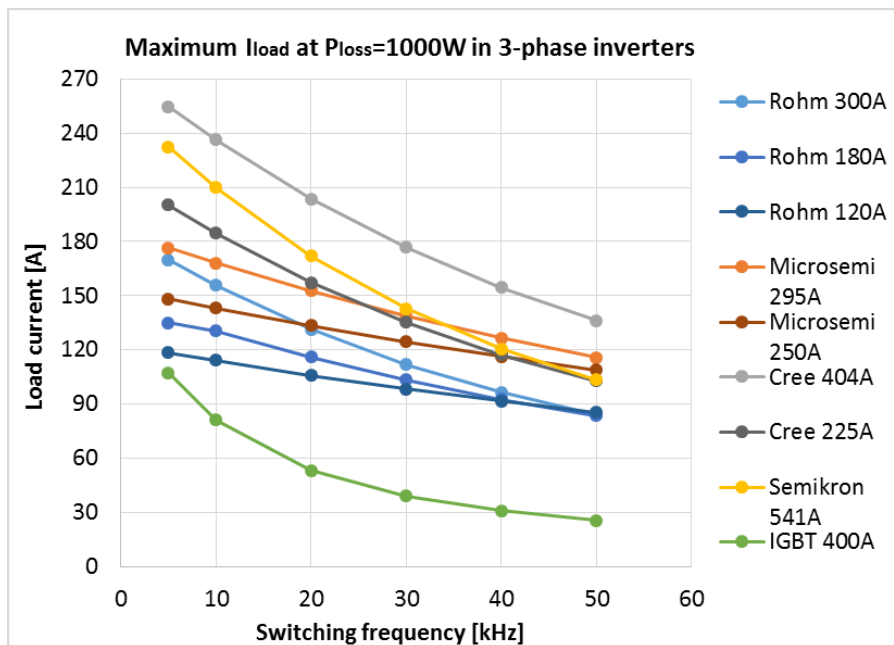


Figure 3.21: Maximum load current at $P_{loss} = 1000 \text{ W}$ in three-phase inverters

At $P_{loss} = 1000\text{ W}$, Cree’s 404 A module gives the highest load current for all test frequencies. Semikron’s 541 A module also gives a high load current, especially at low frequencies. It is clear that this comparison accentuates the modules with high current ratings, as they achieve higher load currents at $P_{loss} = 1000\text{ W}$. Once more, the IGBT module performs badly compared to the other modules. At 1000 W power dissipation, it is only able to switch about 25A at 50 kHz. All of the SiC modules are able to switch more than 80 A load current at 50 kHz.

3.8.3 Fixed Inverter Power Losses – Maximum Switching Frequency

Once more, the total inverter power loss is fixed at $P_{loss} = 1000\text{ W}$. It is desired to iterate over the switching frequency in order to obtain the modules’ switching capabilities. By fixing the load current RMS value at $I_{load} = 100\text{ A}$ and the total power losses at $P_{loss} = 1000\text{ W}$, the maximum switching frequency $f_{sw,max}$ is obtained in Table 3.2.

Table 3.2: Maximum switching frequency at $P_{loss} = 1000\text{ W}$ and $I_{load} = 100\text{ A}$

| Module | Rohm 300A | Rohm 180A | Rohm 120A | Microsemi 295A | Microsemi 250A | Cree 404A | Cree 225A | Semikron 541A | IGBT 400A |
|-----------------------|--------------|--------------|--------------|-------------------|-------------------|--------------|--------------|------------------|--------------|
| $f_{sw,max}$ [kHz] | 37.5 | 33.1 | 27.9 | 67.3 | 62.8 | 78.4 | 52.1 | 52.5 | 4.3 |

From Table 3.2, the advantage of a SiC MOSFET power module compared to an Si IGBT power module becomes evident. All the tested SiC MOSFET modules outperform a state-of-the-art IGBT module at high frequencies, by a wide margin.

This comparison could be more realistic by adding the power losses of the freewheeling diodes, by including similar anti-parallel SiC SBDs in all the three-phase inverters. Nevertheless, this would only decrease the maximum possible switching frequency for all modules and would not change which module that performs the best. The gate driver losses could easily be added by using (3.17), but they are negligible compared to the conduction losses and switching losses in the three-phase inverter.

4. Converter Design and Considerations

This chapter discusses general practical considerations when designing a converter laboratory setup. The considerations covered in this chapter include minimization of parasitics, choice of load inductor, choice of measuring instruments, PCB design, gate driver design and snubber design.

4.1 Parasitic Inductance and Capacitance

When conducting laboratory experiments on a switching device, e.g. a SiC MOSFET, there will always be a struggle to minimize the parasitic stray inductance of the test jig. Both the driver circuit and the power circuit can have high stray inductance due to long cables and wires. From [6], it is known that 1 cm of unshielded lead has about 5 nH of series inductance. In addition, parasitic capacitance exists as a part of all power devices. This parasitic capacitance can be significant. SiC-based converters are able to switch much faster than Si-based converters, which means that di/dt and dv/dt are much higher. Thus, the parasitics could cause an undesired resonant behavior in the series LC resonant circuit that they constitute [6]. This could cause high-frequency ringing on output current and voltage. Such ringing could introduce problems related to EMI (Section 3.5.2). In order to prevent this parasitic oscillation, it is important to minimize the stray inductance by making all leads in the power and driver circuits as short as possible, without causing danger. It is a good measure to twist all cables or wires of significant lengths [6]. A simplified figure of the laboratory setup used in this report is presented in Figure 4.1.

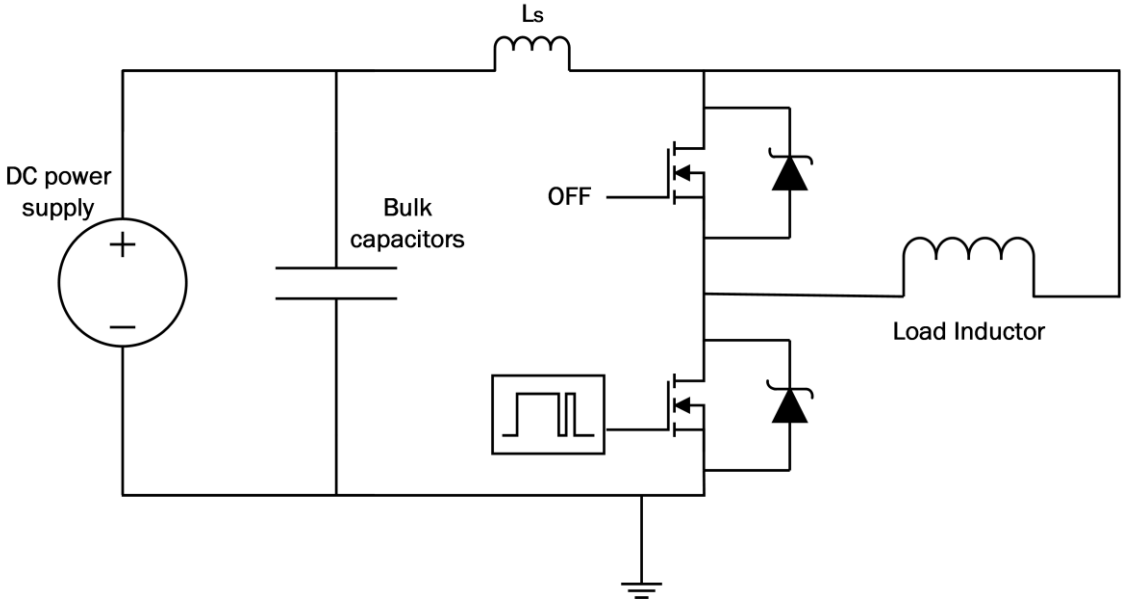


Figure 4.1: Simplified double-pulse laboratory setup

The total loop stray inductance in the circuit presented in Figure 4.1 is lumped and denoted as L_s . The stray inductance of a loop configuration such as the one in Figure 4.1 can be calculated by using Figure 4.2 and (4.1):

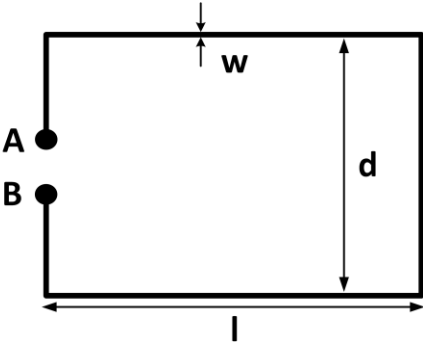


Figure 4.2: Stray inductance of loop configuration [48]

$$L_{AB} = \frac{\mu_0}{\pi} \cdot \left(l \cdot \ln \frac{2d - w}{w} + d \cdot \ln \frac{2l - w}{w} \right) \tag{4.1}$$

μ_0 is the permeability of air, l is the length of the loop, d is the width of the loop and w is the trace width. From (4.1), the loop inductance increases with loop length and loop width, and decreases with the trace width. This means the loop configuration should be as small as possible, with a minimal $l \cdot d$ area. A smart method, which reduces the loop stray inductance in bus bars, is to use thin copper plates instead of wires or cables when possible [6]. Whenever using this solution, it is important to have a thin insulation layer between the copper plates (e.g. Lexan plate). It is also important to have a sufficient creepage distance in order to avoid an undesired shoot through at the bus bar. When applying this solution, the loop width d is reduced to the width of the insulation. Thus, the loop stray inductance is greatly reduced. A possible solution is presented in Figure 4.3:

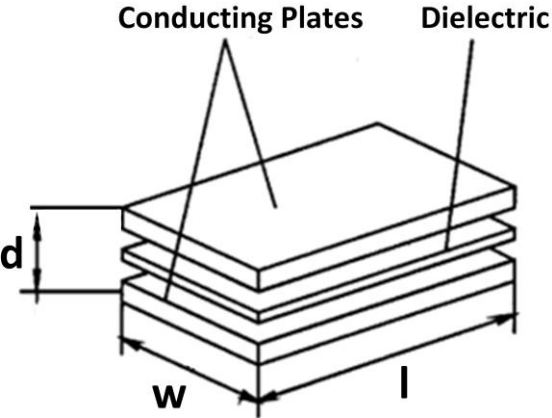


Figure 4.3: Bus bar to minimize stray inductance [49]

The total loop stray inductance in a circuit similar to the one in Figure 4.1 is [49]:

$$L_s = L_{\text{bus bar}} + L_{C1} \parallel \dots \parallel L_{Cn} + L_{\text{screws}} + L_{\text{SiC module}} \quad (4.2)$$

It is therefore crucial to carefully choose a bus bar topology and input and bulk capacitors C_1, \dots, C_n that minimize the total stray inductance. L_{screws} represents the stray inductance caused by screws and nuts in the circuit.

4.2 DC Link

In a switch-mode DC/DC converter, it is essential that the input DC voltage after the rectifier stage of the DC power supply remains constant independent of the transients that develop during switching. In order to achieve this, a DC-link stage consisting of both input and bulk capacitors is used [50]. These capacitors control the voltage at the input when there is a current transient in the circuit. The input capacitors are large capacitors with good stabilizing properties. These capacitors are often implemented as a part of the rectifying power supply. In addition to the input capacitors, there is also a need for bulk capacitors. These are placed very close to the device under test (DUT) and are capable of supplying the demanded energy more quickly than the power supply and the input capacitors. The bulk capacitors are often much smaller than the input capacitors. By having a DC-link stage with bulk capacitors close to the DUT, input voltage deviations during switching are minimized. The minimum required bulk capacitance can be calculated in the following manner [50]:

$$C = \frac{1.21 \cdot I_{tr}^2 \cdot L}{\Delta V^2} \quad (4.3)$$

I_{tr} is the load current change (transient) and ΔV is the maximum allowed voltage dip. L is the filter inductor. If no filter inductor is used, this inductor should be set to $L = 50nH$ to account for stray inductance. It is important to choose bulk capacitors with low equivalent series resistance (ESR), as ESR can cause voltage drops during transients due to the current flowing through the capacitors [50].

The DC-link stage with bulk capacitors is indispensable for stabilizing the input voltage to the converter. Nevertheless, the connection of bulk capacitors increases the total stray inductance in the converter circuit. Thus, low-inductive bulk capacitors should be used. A good measure for reducing stray inductance and ESR caused by bulk capacitors is to connect several capacitors in parallel.

4.3 Choice of Load Inductor

In a double-pulse test, the load is purely inductive, as shown in Figure 4.1. The reason for this is that an inductor can behave as a current source for a short period. The inductance of the load inductor determines the time it takes to charge the inductor and how long it is able to operate as a current source. In a double-pulse test, it is interesting to switch an inductive current as this makes it possible to hard-switch the transistor. Thus, the “worst-case” turn-on and turn-off transients at a given current can be analyzed in detail at a given drain current.

In [51], it is shown that a single-layer air-core inductor is most suitable in a double-pulse test. This is because it has less parasitic capacitance than an iron-core inductor, which is an important property to avoid resonance effects during high-frequency switching.

The most important property of the load inductor is its inductance. A large inductor with high inductance is slow, and can store large amounts of energy. This means that the first pulse of the DPT needs to be a long pulse in order to charge the inductor current to a given level. It also discharges more slowly than a smaller inductance, which could be a safety issue if the double pulses come with high frequency. A large inductor can also have high DC resistance due to a long wire. This could potentially degrade the test conditions. This will be thoroughly discussed in Section 5.4. The inductance L of a single-layer air-core inductor can be calculated as [52]:

$$L = \frac{d^2 \cdot n^2}{45d + 100l} \quad (4.4)$$

d is the coil diameter, l is the coil length and n is the number of turns of the single layer coil.

4.4 Measuring Instruments

A laboratory experiment involving SiC MOSFETs requires well-adapted measuring instruments. As the transients in a double-pulse test have high-frequency information, it is important to use voltage probes with high bandwidths, as well as voltage ratings that exceed the measured voltage. The current measuring instruments should also be able to measure high-frequency transients, as well as having high current ratings. A high-bandwidth oscilloscope should be used. It is crucial that the oscilloscope has a higher bandwidth than the measuring instruments, in order not to lose valuable information [53].

Differential voltage probes should be considered in cases where the oscilloscope and the measured voltage do not share the same ground potential. If the desired measurement is the gate-to-source voltage of the transistor in Figure 4.1, then the probe reference is different from

the oscilloscope ground. In this case, it is important to use a differential probe, which has the property of providing galvanic isolation. If not, ground current loops could occur, which at worst could destroy the oscilloscope or cause other types of danger.

4.5 PCB Design

The design of a power electronic circuit often includes designing a PCB. PCBs in power electronics are most importantly designed in order to minimize wire lengths and thus reduce stray inductance and EMI efficiently [54] [55]. Designing PCBs also helps to obtain a more practical design, and solves challenges such as soldering of small components and lack of space. PCBs can be designed using computer software, e.g. CadSoft Eagle and Altium. Many layout considerations have to be taken into account when designing a PCB. Firstly, the component package footprints have to be designed and drawn with uppermost care. Then, the electrical equivalent must be made in the computer software. Finally, the PCB itself with real component sizes can be designed, and wires between the components can be routed. The computer software includes tools that make it easy to minimize distances. However, considerations such as minimum clearance and creepage must be input to the design rules manually (Appendix A). The trace thickness and width must be selected with great care. This must be selected based on maximum current flow and noise sensitivity. Different trace widths are needed for different signals [56]. Considerations such as number of layers, use of vias, etc., must be based on what optimizes the PCB and what minimizes distances. Soldering components onto PCBs with large copper conduction planes can be very difficult, as copper conducts heat very well. This challenge can be solved by including pads with thermal relief [57]. Implementation of thermal reliefs reduces the thermal conduction from the pad to the copper plane, without decreasing the current conduction capability considerably. Vias can also contribute to making soldering easier. When a PCB design is ready for manufacturing, it can be manufactured through different methods. Popular solutions are etching and milling. PCB milling often gives the most accurate result for small and detailed PCBs.

4.6 Gate Driver Circuit

This section presents important considerations and requirements in gate driver circuits for SiC MOSFETs. In the following, considerations such as required gate-to-source voltage, galvanic isolation, Miller clamp and short-circuit protection (SCP) will be discussed.

4.6.1 Gate Driver Requirements

Driving SiC MOSFETs is somewhat similar to driving Si IGBTs. As earlier mentioned, a SiC MOSFET driver circuit should be low-inductive in order to reduce ringing and EMI caused by stray inductance [6].

Another important aspect is that SiC MOSFET gate drivers should have a high current capability. As SiC MOSFETs are able to switch faster than Si IGBTs, this means that SiC MOSFET gate drivers need to be quicker than Si IGBT gate drivers in order to exploit this property. In order for the SiC MOSFET to switch fast, the gate-to-source voltage of the MOSFET needs to increase quickly. Consequently, a higher gate current is needed in order to charge the input capacitance C_{iss} more quickly [58]. The same current capability is needed at MOSFET turn off. A higher gate current capability can be obtained by reducing the external turn-on and turn-off gate resistors $R_{g,on}$ and $R_{g,off}$. In addition, the stray inductance in the gate driver must be minimized in order for the gate current rise to be as fast as desired.

As for IGBTs, SiC MOSFETs also require a negative gate-to-source voltage, often referred to as active turn-off, in order to have a quick and safe turn-off transient. Normally, a SiC MOSFET driver provides a positive bias gate-to-source voltage $V_{gs(on)}$ of +20 V, and a negative bias gate-to-source voltage $V_{gs(off)}$ of -5 V [23]. The negative bias voltage of $V_{gs(off)} = -5 V$ prevents any false (undesired) turn on of the MOSFET. It also forces a quicker turn-off, as the input capacitance C_{iss} gets discharged much more quickly [58]. This leads to lower turn-off switching losses. The high positive bias voltage of $V_{gs(on)} = 20 V$ reduces the on-state resistance in the SiC MOSFET [58]. It also leads to a faster turn-on transient, i.e., lower turn-on switching losses.

4.6.2 Galvanic Isolation of Signal Supply and DC Power Supply

4.6.2.1 Signal Supply

Galvanic isolation is a very important safety measure when designing gate driver circuits for MOSFETs. In a half-bridge configuration there are two different gate drivers controlling the upper and the lower transistor. The upper transistor source jumps in potential during switching. This means that the gate-to-source voltage reference of the upper transistor is floating. It is thus required to provide galvanic isolation on the upper gate signal supply. Galvanically isolated input signal to the upper transistor provides a necessary level shift. In addition, the gate-to-source voltage of the lower transistor might also be floating if the output from the rectifier is not grounded. If so, galvanic isolation of the signal supply should be included also here. There are three ways of obtaining signal isolation; fiber optics, optocouplers and transformers [6].

4.6.2.2 DC Power Supply

Most gate drivers require a DC power supply on the output side. Using the same arguments as for signal supplies, DC power supplies should also be galvanically isolated. Galvanic isolation of DC power supplies can be provided by high-frequency DC/DC converters, which give a very compact design. Other popular solutions are bootstrap supplies and auxiliary supplies [45].

In order to prevent undesired ground current loops from the power circuit through the driver circuit, all signal and power supplies in the driver circuit should be galvanically isolated [23]. A ground current loop through the driver could possibly destroy it, as the current rating in the driver circuit is very low compared to that of the power circuit.

4.6.3 Miller Clamp

The switching of SiC MOSFETs in half-bridge configurations introduces challenges due to extremely fast switching transients. Such a challenge could be a false (undesired) turn on of both transistors simultaneously, causing a short circuit or shoot through across the DC power supply. The short circuit could be caused by a Miller current flowing through the gate driver during transistor turn off. This is explained using Figure 4.4.

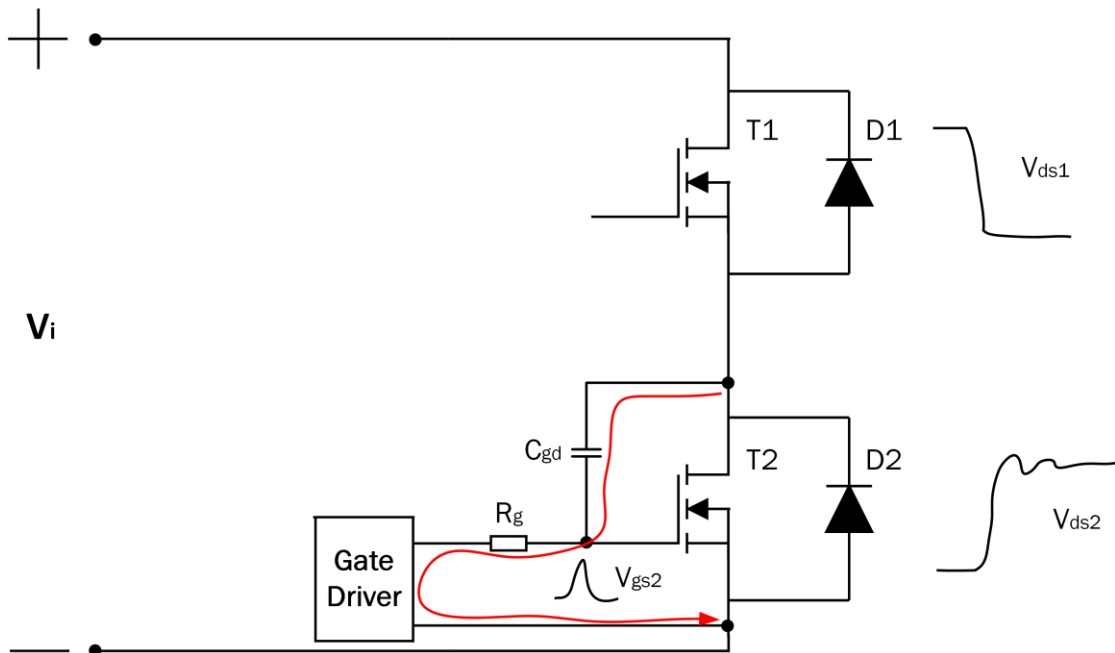


Figure 4.4: Miller current explanation

Initially, switch T1 is off and switch T2 is conducting. If now T2 is turned off, and T1 is given a turn-on signal, the drain-to-source voltages will be as depicted by V_{ds1} and V_{ds2} . This switching transient causes very high dv/dt across T2. Due to this high dv/dt , current is able to

pass through C_{gd} . This current is called the Miller current, as it is flowing through the Miller capacitance (Section 2.3.2.3), and is given by the following equation [59]:

$$I_{gd} = C_{gd} \frac{dv}{dt} \tag{4.5}$$

The Miller current is depicted by the red line in Figure 4.4. This current passing through the driver circuit could cause the gate-to-source voltage to increase for a short period, depicted by V_{gs2} . If this gate-to-source voltage rises high enough to exceed the threshold voltage of the transistor, this could cause a dangerous turn on of T1. This would make T1 and T2 conduct simultaneously, causing a short circuit across the DC voltage.

There are different ways of solving this problem during transistor turn off. One solution is to divide the gate resistor R_g into a turn-on gate resistor $R_{g,on}$ and a turn-off gate resistor $R_{g,off}$. By reducing $R_{g,off}$ to a lower value than the original R_g , the gate-to-source voltage during transistor turn off will not increase as much as in Figure 4.4. Such a solution is presented in Figure 4.5, where the red line is the turn-off current including Miller current, and the green line is the turn-on current from the gate driver.

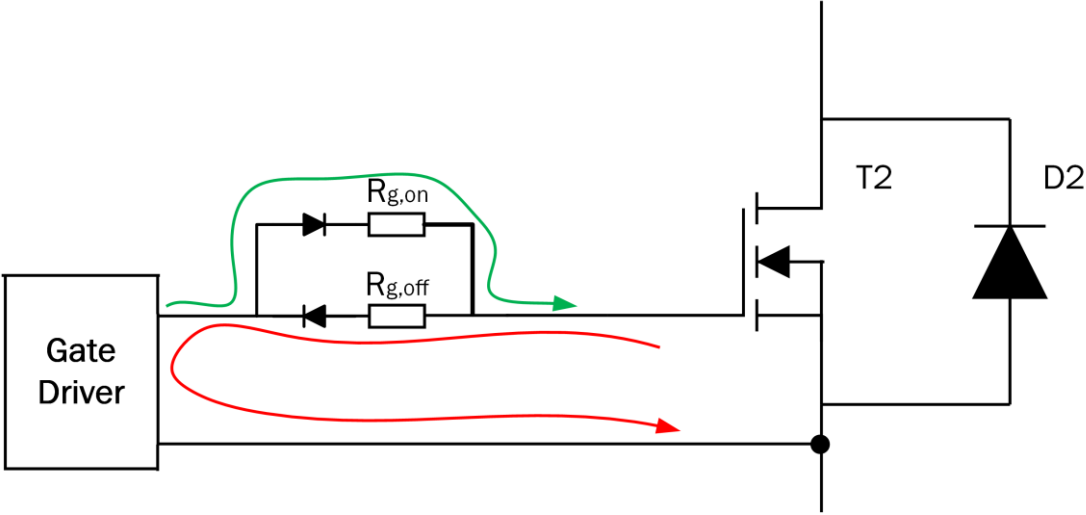


Figure 4.5: Solution 1 – Reduction of turn-off gate resistance

The reduction of $R_{g,off}$ solves the problem to some extent. If the turn-off gate resistance is too low, however, this could lead to extremely fast switching and a too high dv/dt across T2.

A second solution is to add a transistor to the driver circuit that can bypass the Miller current during turn off. Such a solution is called an active Miller clamp. Figure 4.6 presents the active Miller clamp.

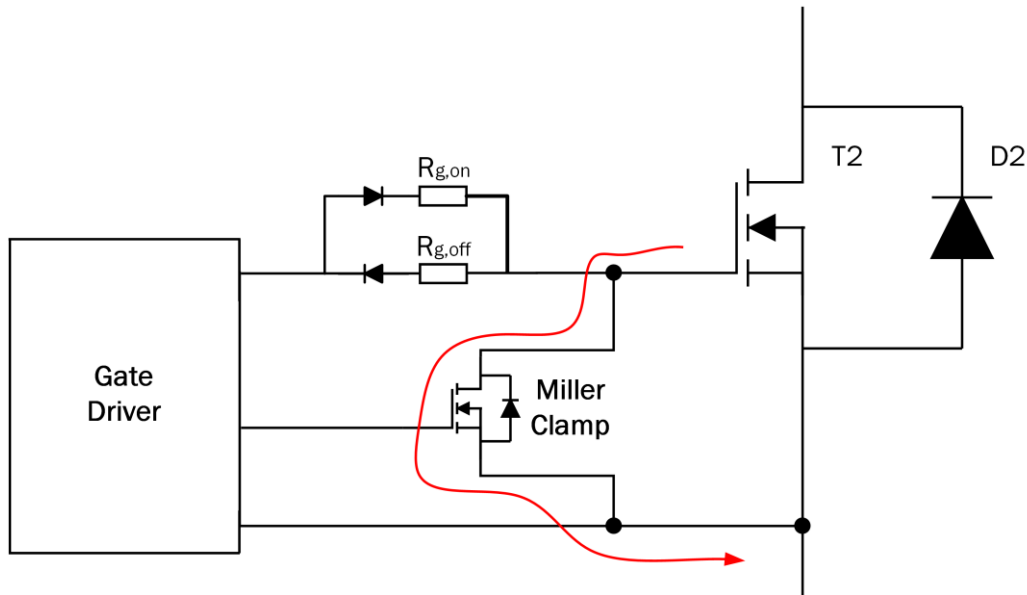


Figure 4.6: Solution 2 – Active Miller clamp

The Miller clamp consists of a MOSFET that bypasses the Miller current (depicted by the red line) during T2 turn off. The Miller clamp is controlled by the gate driver IC. Normally, the bypass MOSFET is turned on by the gate driver when the gate-to-source voltage V_{gs2} across T2 is reduced to the threshold voltage during turn off [59]. In this way, the Miller clamp does not affect the dv/dt of V_{gs2} nor the turn-off switching time. This is a very effective way of avoiding undesired effects of Miller current. The bypass MOSFET turns off when V_{gs2} reaches the threshold voltage during turn on. Thus, the active Miller clamp does not affect the turn on of T2.

4.6.4 Short-Circuit Protection

The gate driver circuit of a transistor, e.g. a SiC MOSFET, should always include a short-circuit protection (SCP) system [12]. Such an SCP system should be able to turn off the transistor if the current through it exceeds a given limit. This is particularly important in a half-bridge configuration, as the one depicted in Figure 4.1. If both transistors should turn on simultaneously, this would create a dangerous short circuit across the half bridge. An SCP system would protect the converter against such faults, and similar faults that create too high currents through the transistors. It is important to design the SCP to be fast and able to force a turn off at high currents without destroying the device. Thus, the SCP should include features that limit the current derivative di/dt and the voltage derivatives dv/dt . This means that the SCP should compel a soft turn off. The most usual SCP system is based on drain-to-source voltage measurement of the protected MOSFET. The SCP system and its complete design will be discussed in Section 5.1.3.

4.7 Snubber Circuits for MOSFETs

Snubber circuits should be implemented in power converters including MOSFETs and other transistors. As transistors can cause high overvoltages and overcurrents during switching, this might be dangerous and could destroy the power devices. Snubber circuits are designed to reduce these switching stresses to safe levels. A snubber can reduce switching stresses on transistors by [6]:

- Limiting voltage spikes across transistors during turn-off transients
- Limiting current spikes through transistors during turn-on transients
- Limiting di/dt during transistor turn on and dv/dt during transistor turn off
- Reducing total power losses during switching

There are three basic types of snubber circuits that are used to protect single transistors [6]:

1. Turn-off snubbers
2. Turn-on snubbers
3. Overvoltage snubbers

The converter topology in Figure 4.7 will be used in order to explain the different snubbers.

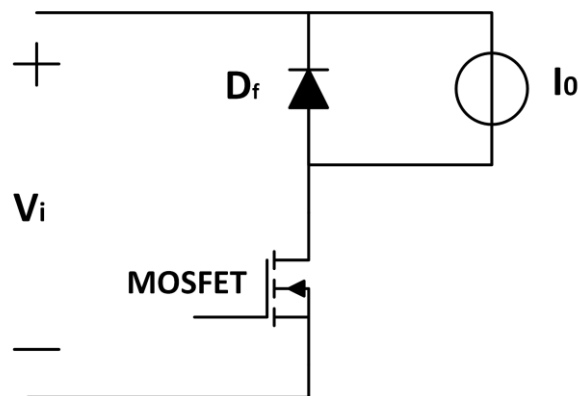


Figure 4.7: Simple converter circuit without snubber

4.7.1 Turn-Off Snubber

Turn-off snubbers are essentially used in order to limit turn-off switching losses by limiting the voltage rise across the transistor during the turn-off transient. In a converter configuration as the one depicted in Figure 4.7, the aim is to keep the voltage across the MOSFET as low as possible until the drain current has shifted to the freewheeling diode D_f . By doing this, the switching power losses during transistor turn off is limited. Figure 4.8 depicts a possible turn-off snubber layout.

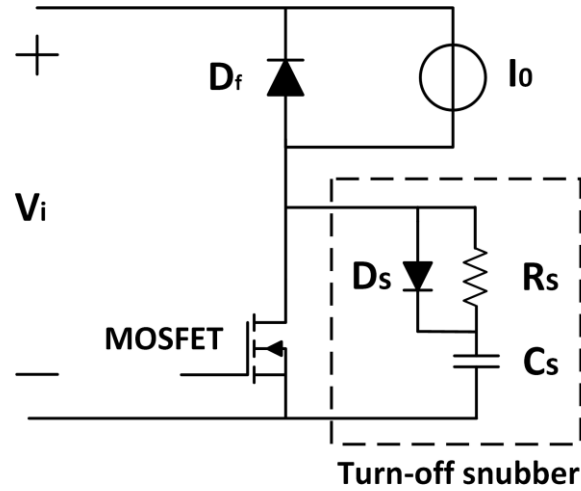


Figure 4.8: Turn-off snubber

In Figure 4.8, a snubber capacitor C_s is connected across the MOSFET. During the turn-off transient of the MOSFET, the current I_o will start to shift from the transistor and start to flow through D_s and C_s . This will charge the snubber capacitor C_s , which will help limit the voltage rise across the MOSFET while the drain current decreases. Normally, turn-off snubbers are RCD circuits including a diode in parallel to the snubber resistor, as shown in Figure 4.8. Such a diode helps to achieve a higher current flowing into the snubber capacitor (faster charging of C_s) during DUT turn off, as the current would flow through the diode instead of through the resistor [6]. Thus, an RCD snubber would reduce the power dissipation compared to an RC snubber, as no power is dissipated in R_s during MOSFET turn off. However, by not including the diode, the turn-off snubber would also be suitable for limiting the voltage overshoot across the MOSFET, as the drain current derivative is more restricted than with an RCD snubber [14]. Such a snubber would also reduce ringing efficiently.

The turn-off snubber capacitor can be calculated by using the following relation [6].

$$C_s = \frac{I_d \cdot t_f}{2 \cdot V_{ds}} \quad (4.6)$$

I_d is the drain current, t_f is the current fall time and V_{ds} is the drain-to-source voltage.

The turn-off snubber affects the turn-on transient and turn-on switching losses in a negative manner, as the current overshoot height and width increase due to discharge of the snubber capacitor through the snubber resistor during transistor turn on. The snubber resistor R_s helps reduce this current overshoot by limiting the current discharge from C_s . The turn-off snubber resistor should be chosen so that the peak current through it is less than the reverse-recovery

current of the freewheeling diode during turn on. That is, the reverse-recovery current should be limited to $\frac{V_{ds}}{R_s} < I_{rr} = 0.2 \cdot I_0$ [6]. This gives the following relation for calculating the turn-off snubber resistor.

$$R_s > \frac{V_{ds}}{0.2 \cdot I_0} \quad (4.7)$$

When designing a suitable turn-off snubber, it is of great interest to keep the switching losses as small as possible in both the switch and the snubber. An increased capacitance C_s in the turn-off snubber would help reduce the voltage overshoot and ringing. However, this would lead to higher losses, as this slows down both the turn-on transient and the turn-off transient. In addition, the capacitor energy, which is dissipated in the snubber resistor, is given by [6]:

$$E_{R_s} = \frac{C_s \cdot V_{ds}^2}{2} \quad (4.8)$$

Thus, a higher capacitance C_s implies higher losses dissipated in the snubber resistor R_s .

4.7.2 Turn-On Snubber

It is assumed that the load current I_0 in Figure 4.7 is freewheeling through the diode D_f , and that the MOSFET is off. If the MOSFET is given a turn-on signal, the current through it starts to increase. Thus, I_0 will commute from the freewheeling diode to the transistor. When the freewheeling diode ceases to conduct, it reverse recovers the charge stored in the pn junction. If this transition happens without a turn-on snubber, a high drain current derivative di/dt can cause high peak reverse-recovery current through the MOSFET. If this reverse-recovery current gets too high, it can cause unsafe stresses on the MOSFET. A turn-on snubber topology solving this issue is presented in Figure 4.9.

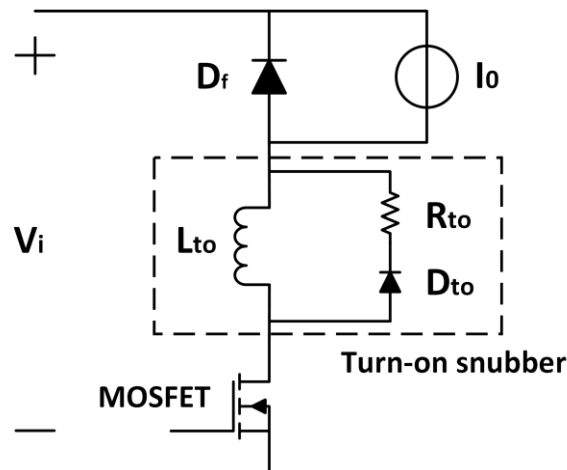


Figure 4.9: Turn-on snubber

By increasing the snubber inductance L_{to} between the diode and the MOSFET, the rate of rise of the drain current is limited. This limitation reduces the peak reverse-recovery current flowing to the MOSFET. During the turn-on transient, the voltage across L_{to} is given by $V = L_{to} \cdot \frac{di}{dt}$. Thus, the voltage across the MOSFET is lower than V_d during the turn-on transient, depending on the size of L_{to} . This leads to lower turn-on switching losses.

Before the MOSFET turn off, the energy $E_{L_{to}} = \frac{1}{2} \cdot L_{to} \cdot I_0^2$ is stored in the snubber inductor. In order to avoid overvoltages across the MOSFET during turn off, this energy is dissipated through the diode D_{to} and the resistor R_{to} at turn off.

4.7.3 Overvoltage Snubber

It is now assumed that the MOSFET in Figure 4.7 is on, and that load current I_0 flows through it. If the MOSFET is given a turn-off signal, the voltage across it starts to increase. This voltage increases until the freewheeling diode starts to conduct and the current through the transistor starts to decrease (Figure 3.11). The drain-to-source voltage V_{ds} across the MOSFET during the turn-off transient can be expressed as:

$$V_{ds} = V_i - L_s \cdot \frac{dI_d}{dt} \quad (4.9)$$

L_s is the lumped stray inductance of the loop, depicted in Figure 4.10. The drain current I_d will decrease very quickly during the turn-off transient. This causes a negative di/dt and thus an overvoltage across the transistor that exceeds the DC voltage V_i . This overvoltage across the MOSFET can reach unsafe levels if the product of di/dt and L_s is too high. Thus, an overvoltage snubber is needed in order to limit this overvoltage to an acceptable level. The overvoltage snubber limits the overvoltage by leading the energy stored in the stray inductance to a snubber capacitance instead of to the drain node of the transistor. Figure 4.10 depicts the alternative current path during switching, through the diode D_{ov} and the snubber capacitor C_{ov} .

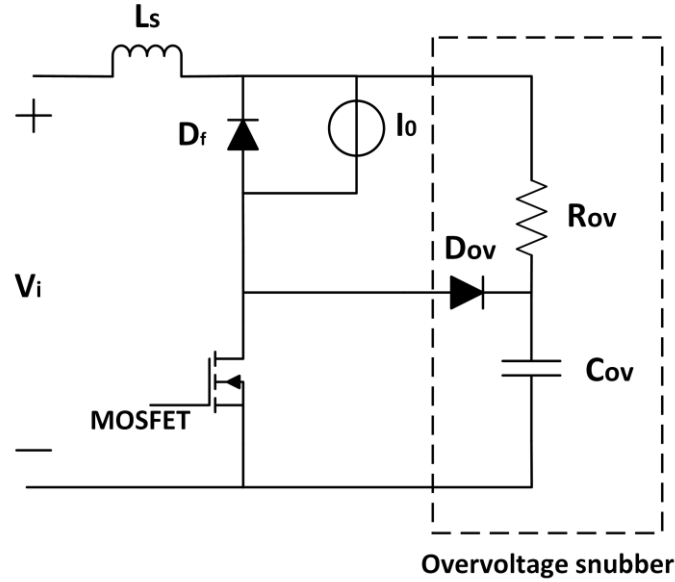


Figure 4.10: Overvoltage snubber

Assuming that all the energy stored in the stray inductance goes to the snubber capacitor, the snubber capacitance C_{ov} can be calculated as [6]:

$$\frac{1}{2} \cdot C_{ov} \cdot \Delta V_{ds,max}^2 = \frac{1}{2} \cdot L_s \cdot I_0^2 \quad (4.10)$$

$\Delta V_{ds,max}$ is the maximum allowed drain-to-source overvoltage and L_s is the total lumped stray inductance. As can be seen from (4.10), an increased snubber capacitance reduces the overvoltage at turn off.

A snubber resistor R_{ov} is connected across the freewheeling diode D_f to avoid long-lasting ringing between the snubber capacitor and the stray inductance, by dissipating the energy in the snubber resistor. An increased snubber capacitance C_{ov} will lead to higher losses in the snubber resistor, as the energy stored in the snubber capacitor will increase. This can be seen from (4.10).

4.7.4 DC Snubber

The DC snubber is a variation of the overvoltage snubber, which can be used in half-bridge module configurations. The DC snubber is depicted in Figure 4.11.

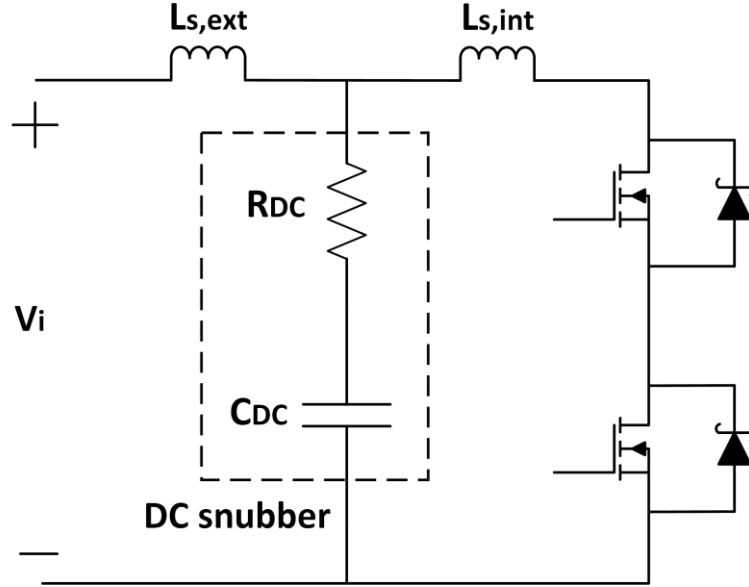


Figure 4.11: DC snubber

This DC snubber topology, in the same way as the overvoltage snubber, creates an alternative path for the inductive current during turn off, which reduces the turn-off surge voltage and the parasitic oscillation [60]. Half-bridge power modules often make it more difficult to connect the snubber exactly on the desired location. As big parts of the stray inductance can be located inside the module package, depicted by $L_{s,int}$ in Figure 4.11, the connection of the overvoltage snubber in Figure 4.10 can be difficult to achieve. Due to this, the DC snubber is connected in parallel to the module, as close to it as possible. The DC snubber should be able to attenuate ringing caused by stray inductance outside the module, depicted by $L_{s,ext}$. Thus, the effectiveness of a DC snubber highly relies on the connection points in the converter circuit, and the location of the stray inductance.

A DC snubber can be designed based on the turn-off voltage waveform of a switching device. Fast-switching transients often show long-lasting and high-frequency voltage ringing. This ringing is caused by a resonance between the parasitic capacitance C_p of the power devices and the total stray inductance L_s in the test circuit. Thus, the ringing frequency can be expressed in the following manner [13]:

$$f_r = \frac{1}{2\pi \cdot \sqrt{L_s \cdot C_p}} \leftrightarrow L_s = \frac{1}{(2\pi)^2 \cdot f_r^2 \cdot C_p} \quad (4.11)$$

If f_r is known, this equation makes it possible to calculate the total stray inductance L_s in the entire test circuit. The damping coefficient ζ of such a parallel RLC resonant circuit can be expressed in the following manner, where R_{DC} is the DC snubber resistor [14]:

$$\zeta = \frac{1}{2 \cdot R_{DC}} \cdot \sqrt{\frac{L_s}{C_p}} \leftrightarrow R_{DC} = \frac{1}{2 \cdot \zeta} \sqrt{\frac{L_s}{C_p}} \quad (4.12)$$

Thus, the DC snubber resistor R_{DC} can be calculated by choosing a damping coefficient ζ . For the DC snubber to be effective at the ringing frequency, the following equation must be true [14]:

$$f_r = \frac{1}{2\pi \cdot R_{DC} \cdot C_{DC}} \leftrightarrow C_{DC} = \frac{1}{2\pi \cdot R_{DC} \cdot f_r} \quad (4.13)$$

Thus, the DC snubber capacitor C_{DC} can be calculated using the values for R_{DC} and f_r . DC snubbers often consist only of the snubber capacitor C_{DC} . Even though the snubber capacitor alone efficiently reduces the voltage overshoot, it would not be suitable for damping parasitic ringing. Thus, the snubber resistor R_{DC} should be included in order to reduce long-lasting ringing in half-bridge configurations.

4.7.5 Calculation of Snubber Losses

The switching power losses in an RC snubber circuit can be considerable, thus, it is important to calculate them. All the switching energy losses E_R in an RC snubber are dissipated in the snubber resistor, and can theoretically be calculated in the following way.

$$E_R = \frac{C \cdot V^2}{2} \quad (4.14)$$

R is the snubber resistor, C is the snubber capacitor and V is the voltage across the snubber capacitor before discharge. This is a generalization of (4.8). However, as snubber capacitors can be charged and discharged multiple times during switching, this relation does not always hold in laboratory experiments.

The switching losses in the snubber resistor can be measured and calculated more accurately in laboratory experiments by measuring the current flowing through the snubber resistor. Thus, the resistive power losses p_R are given below.

$$p_R(t) = R \cdot i_R^2(t) \quad (4.15)$$

i_R is the current flowing through the snubber resistor. This current will be zero at all times, except during switching. Thus, by integrating p_R during the switching transients, it is possible to calculate the switching energy losses E_R in the snubber resistor very accurately.

5. Laboratory Setup and Measurement

This chapter is a complete description of the laboratory setup and measuring instruments used in the laboratory experiments in Chapter 7. The implementation of short-circuit protection in the gate driver is explained in detail. Considerations regarding PCB design, choice of load inductor, measurement delay and snubber design are thoroughly discussed. The complete bill of materials (BOM) for the laboratory setup is presented in Appendix C.

5.1 Laboratory Setup

5.1.1 Device Under Test

The device under test (DUT) in this laboratory experiment is the lower transistor of the BSM120D12P2C005 SiC Power Module from Rohm Semiconductor [38]. The module is a full SiC half-bridge module consisting of SiC MOSFET transistors with DMOS structure and SiC Schottky Barrier diodes (SBD). The voltage rating of the module is 1200 V, and the current rating is 120 A. A detailed figure of the module is presented in Figure 5.1:

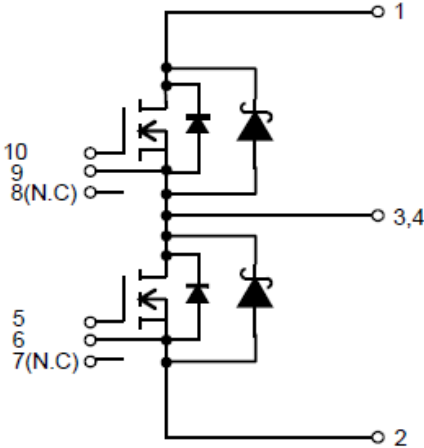


Figure 5.1: Half-bridge module with SiC MOSFETs and SiC SBDs [38]

As seen from Figure 5.1, SiC MOSFETs include intrinsic pn-junction body diodes. These diodes are fast and have a good reverse recovery response. Unfortunately, these diodes have a high on-state resistance for continuous current as well as a high threshold voltage [24]. Thus, anti-parallel SiC SBDs are included in the module in order to minimize the on-state losses of the power circuit. SiC SBDs normally have low on-state resistance as well as low threshold voltage and fast recovery characteristics, as explained in Section 2.3.1. Unfortunately, detailed electrical properties of the SiC SBD are not given in the SiC module datasheet.

Electrical properties of the DUT are listed in Table 5.1:

Table 5.1: Electrical properties of the DUT [38]

| SiC Module | V_{DSS} | I_D | $R_{ds,on} (25^\circ\text{C})$ | $V_{gs(th)}$ | C_{iss} | E_{on} | E_{off} |
|------------------------|-----------|-------|--------------------------------|--------------|-----------|----------|-----------|
| BSM120D12P2C005 (Rohm) | 1200 V | 120 A | 20 m Ω | 2.7 V | 14 nF | 4 mJ* | 2 mJ* |

*Switching losses are given at $I_d = 120\text{ A}$ and $T_j = 25\text{ }^\circ\text{C}$

The DUT has the following I-V characteristics, which are given in the SiC module datasheet.

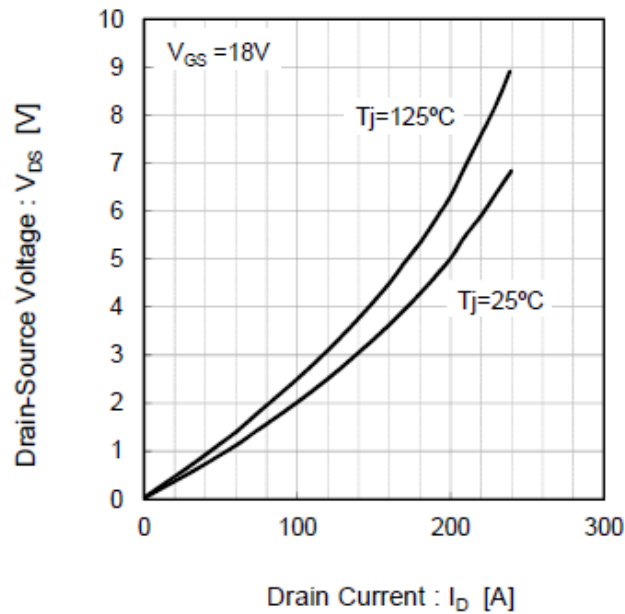


Figure 5.2: I-V characteristics of the DUT [38]

Figure 5.3 presents a simplified electrical equivalent of the laboratory setup, including the DUT, the gate driver circuit, the load inductor and the bulk capacitors. All the aspects of the laboratory setup will be explained in detail in the continuation.

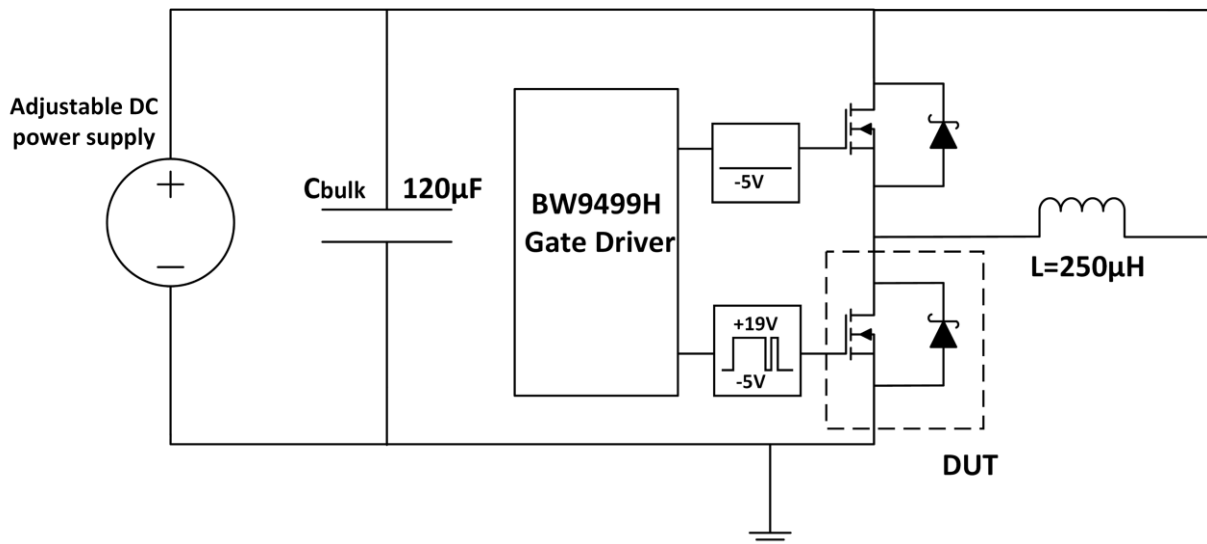


Figure 5.3: Simplified electrical equivalent of the laboratory Setup

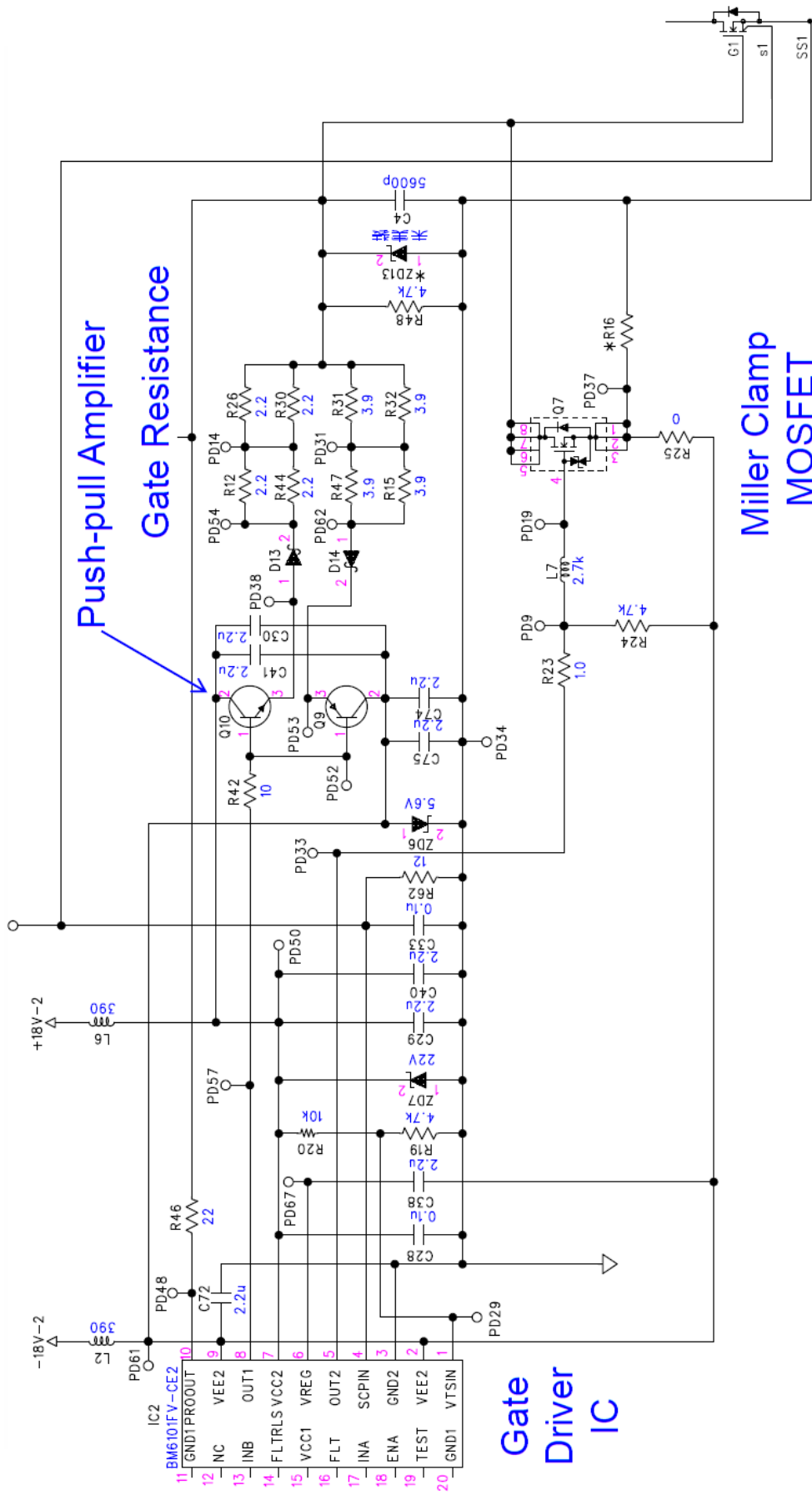


Figure 5.4: Circuit diagram of the BW9499H – Upper gate driver [61]

5.1.2 Gate Driver Circuit Board

In order to drive the SiC module, the BW9499H “Gate driver circuit board for SiC Power Modules” from Rohm Semiconductor is used [61]. The gate driver circuit board includes two separate gate drivers, which means that it is able to drive both the upper and the lower transistor of the half-bridge module simultaneously. The circuit diagram of the upper gate driver is presented in Figure 5.4. The circuit diagram of the lower gate driver is similar to that of the upper gate driver.

This is a gate driver circuit made especially for evaluation purposes of SiC power modules. It actually fits directly on top of the SiC Module, which means that the stray inductance is minimized due to the short distance between the SiC module and the driver. The gate driver IC in Figure 5.4 provides galvanic isolation of the gate signal. Unfortunately, the gate driver circuit board does not provide galvanic isolation of the output-side DC power supply, which was found necessary in Section 4.6.2.2. Because of this, the gate driver supply voltages are fed through external DC/DC converters from Recom, providing galvanic isolation [62]. It is desired that the DC-voltage supply from the DC/DC converters have three output levels: +19 V, 0 V and -5 V. This is in order to provide plus bias gate voltage, reference and minus bias gate voltage respectively. This is accomplished by using one dual output ± 12 V and one single output +5 V DC/DC converter in the manner depicted in Figure 5.5:

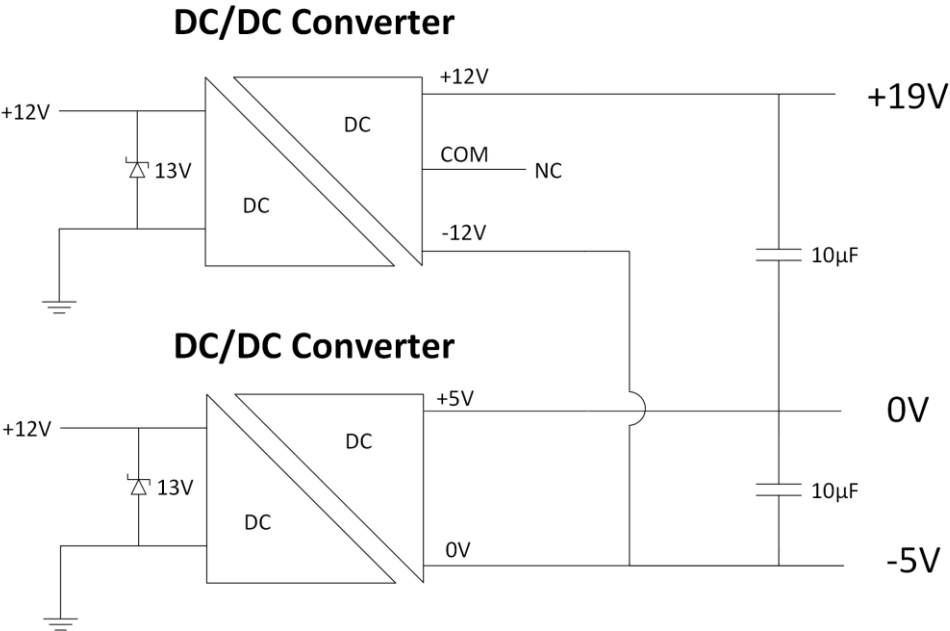


Figure 5.5: DC/DC converter design providing galvanic isolation

For security reasons, Zener diodes are connected across the DC power supply. These Zener diodes have a voltage rating of 13 V. Thus, if the input to the DC/DC converters exceeds 13 V,

then the Zener diodes will start to conduct and maintain the voltage at 13 V [63]. This solution helps to ensure that the voltage input to the gate driver never is too high. In addition, 10 μ F electrolytic capacitors are connected across the output from the DC/DC converters. This is done to ensure that the voltage input to the gate driver circuit is as stable as possible, without fluctuations [62]. The importance of such decoupling capacitors was explained in Section 3.5.2. Both the upper and the lower driver have this design. The PCB design including the electrical circuit in Figure 5.5 will be presented in Figure 5.9.

By using (3.17), it is in (5.1) verified that the driving power requirements at a switching frequency of 50 kHz are lower than the DC/DC converter power rating, which is 2 W.

$$P_{GATE} = V_{DRV} \cdot Q_G \cdot f_{DRV} = 24 V \cdot 700 nC \cdot 50 kHz = 0.84 W < 2 W \quad (5.1)$$

The driving charge Q_G is found using the SiC module datasheet.

The gate driver circuit board includes a Miller Clamp MOSFET that bypasses Miller current during DUT turn off, in order to avoid false turn on. The importance of such a feature in the gate driver was explained in Section 4.6.3.

The circuit board also has separate turn-on and turn-off external gate resistors. This makes it easy to control the switching speed at turn on and turn off separately, in addition to investigating the influence of the external gate resistance during switching. The external gate resistors are 0612 surface-mount (SMD) resistors with higher current capability than normal 1206 SMD resistors.

5.1.3 Short-Circuit Protection

The importance of a short-circuit protection (SCP) feature in the gate driver was explained in Section 4.6.4. The SCP system should detect a short-circuit fault, or overcurrents, by measuring the drain-to-source voltage of the DUT. As the DUT has an on-state drain-to-source resistance of $R_{ds(on)} = 20 m\Omega$, it is easy to calculate for which current/voltage the SCP should intercept. E.g., a drain current of 200 A gives a drain-to-source voltage of 4 V according to Ohm's law.

The gate driver circuit board BW9499H does not include any SCP feature that is ready for use. However, it is possible to implement an SCP by exploiting the in-built features of the gate driver integrated circuit (IC) BM6101FV [64]. The gate driver IC has an output called SCPIN, which is pin number 4 in Figure 5.4. If the voltage potential of this pin relative to the ground potential exceeds $V_{SCPIN} = 0.74 V$, then the gate driver IC sends a turn-off signal to the SiC MOSFET. This property can be utilized in order to implement the SCP. This is done by using voltage

division, as explained in the BM6101FV datasheet. Figure 5.6 depicts the SCP circuit for the upper gate driver, made in LTspice IV.

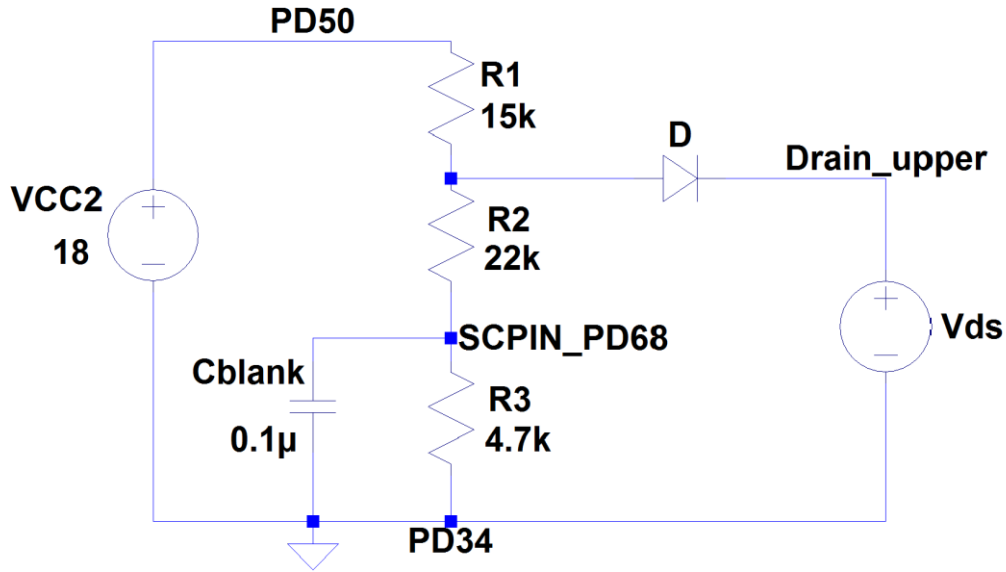


Figure 5.6: SCP circuit for upper driver

The desired voltage division is obtained by connecting three resistors between PD50 and PD34 in Figure 5.4. One of the resistors, R_3 , is connected across SCPIN (PD68) and ground (PD34) along with a capacitor C_{blank} . These two components replace R62 and C33 in Figure 5.4. By adjusting the resistors R_1 , R_2 and R_3 , it is possible to determine for what drain-to-source voltage V_{ds} the voltage potential on SCPIN exceeds 0.74 V, and thus the upper MOSFET turns off. The capacitor C_{blank} determines the blanking time of the SCP. A diode is connected to the drain of the MOSFET to be able to measure the drain-to-source voltage. The purpose of the diode is to block current from flowing from drain to gate during the off state of the MOSFET. This diode should therefore be able to block more than 600 V in addition to having a fast recovery. Thus, the UF4007 ultrafast-recovery diode from Vishay is chosen [65], which has a breakdown voltage of 1000 V.

In such a circuit, the drain-to-source voltage at which the SCP will intervene is given by [64]:

$$V_{ds,SCP} = V_{SCPIN} \cdot \frac{R_3 + R_2}{R_3} - V_{FD} \quad (5.2)$$

$V_{FD} = 1.7 V$ is the forward voltage of the diode and $V_{SCPIN} = 0.74 V$ is the voltage limit at SCPIN at which the SCP is activated. The values in Figure 5.6 should therefore give $V_{ds,SCP} = 2.50 V$, which corresponds to a drain current of approximately 125 A. This is just above the drain current rating.

In order for this to work, the following relation must hold [64]:

$$V_{CC2} > V_{SCPIN} \cdot \frac{R_3 + R_2 + R_1}{R_3} \quad (5.3)$$

If not, the SCPIN voltage will not be able to reach the voltage limit of $V_{SCPIN} = 0.74 V$. The blanking time t_{blank} of the SCP can be calculated in the following manner [64]:

$$t_{blank} = -\frac{R_2 + R_1}{R_3 + R_2 + R_1} \cdot R_3 \cdot (C_{blank} + 27 \cdot 10^{-12}) \cdot \ln\left(1 - \frac{R_3 + R_2 + R_1}{R_3} \cdot \frac{V_{SCPIN}}{V_{CC2}}\right) + 0.65 \cdot 10^{-6} \quad (5.4)$$

The blanking time of the SCP, increases when the blanking capacitor C_{blank} increases. Thus, a higher blanking capacitance leads to slower reaction.

Unfortunately, the BW9499H gate driver circuit board does not have any space available for the implementation of the SCP. Thus, a new PCB containing the components needed for the SCP has to be made. The SCP circuit diagram implemented in CadSoft Eagle is presented in Figure 5.7.

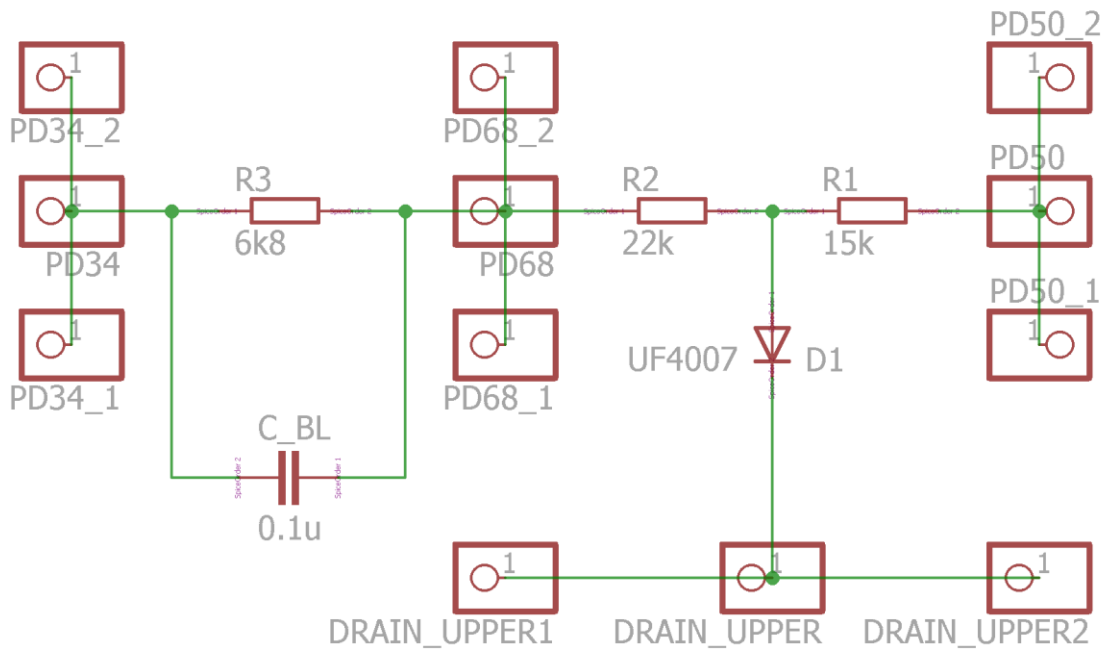


Figure 5.7: CadSoft Eagle – SCP for upper driver

The same PCB also includes the DC/DC converters providing galvanic isolation to the power supplies, which was explained in Figure 5.5. The circuit diagram for the DC/DC converters is presented in Figure 5.8.

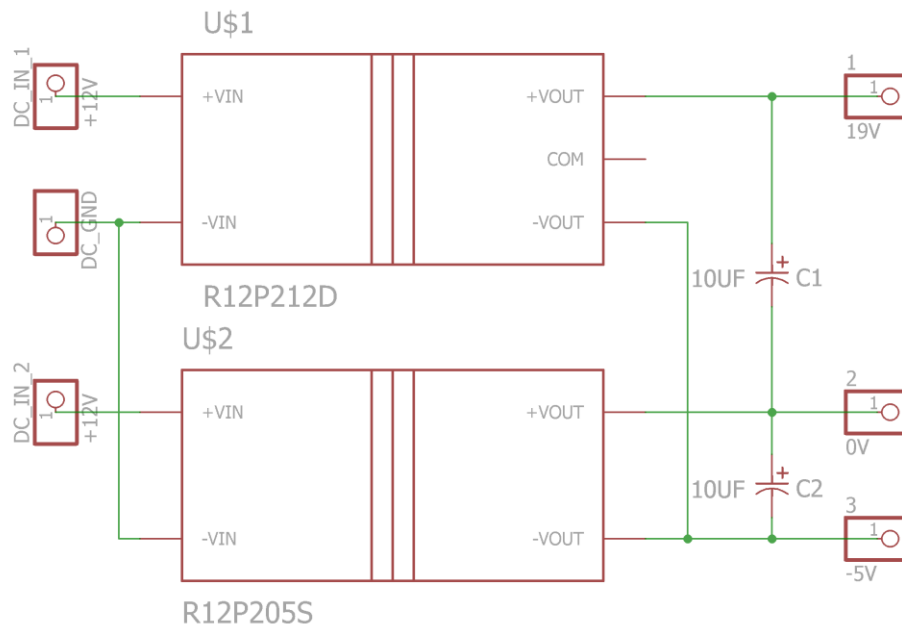


Figure 5.8: CadSoft Eagle – DC/DC converters for upper driver

This circuit provides galvanic isolation for the upper driver. The circuit diagrams for the lower driver are similar to the ones in Figure 5.7 and Figure 5.8, and are presented in Appendix B. Note that the Zener diode protecting the DC/DC converter voltage inputs were not considered in the PCB design. However, these were soldered onto the board after PCB manufacturing, as depicted in Figure 5.5.

Figure 5.9 presents the final PCB design in CadSoft Eagle for the circuits providing galvanic isolation and SCP. This PCB includes the SCP circuits for both the upper and the lower driver on the right hand side, as well as the DC/DC converter design on the left hand side. The 16 pins in the middle of the board make it possible to connect the PCB directly on top of the 16 connection pins on the gate driver circuit board. The different PD nodes in the SCP circuit are connected through short wires to their respective connection points on the gate driver circuit board. The connection points drain_lower and drain_upper are connected to their respective drain power terminals on the SiC module. All these connection points have three pads each for mechanical stability.

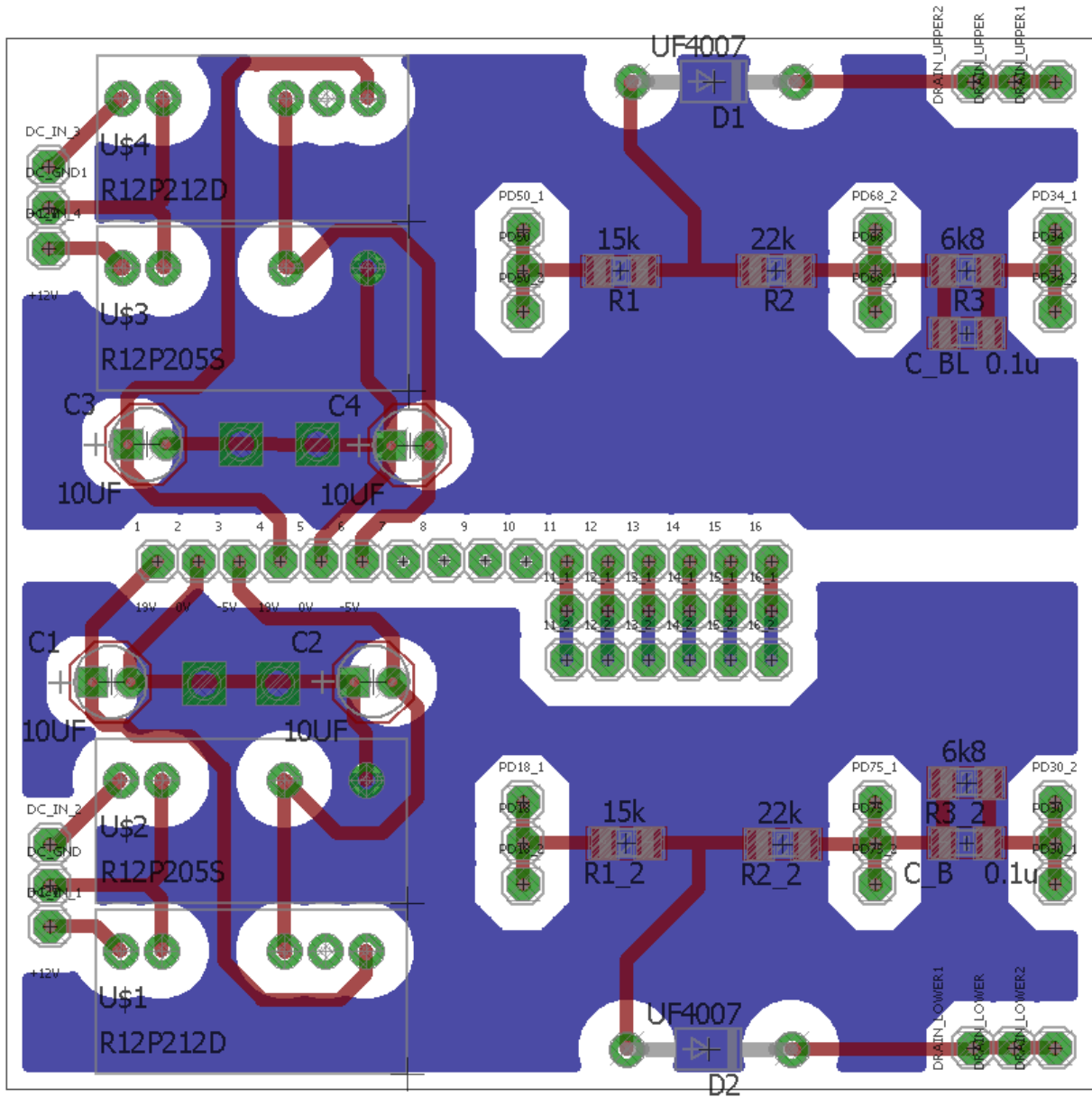


Figure 5.9: CadSoft Eagle – PCB design with SCP and galvanic isolation

5.1.4 Bus Bar Design

The bus bar is a two-sided machine-made printed circuit board (PCB) consisting of two 0.035 mm thick copper layers and one 1.5 mm thick insulation layer (lexan). The 1.5 mm thick insulation layer has a breakdown voltage of about 100 kV [66], which is more than sufficient in this experiment as the maximum voltage never exceeds 1000 V. The two 0.035 mm thick copper plates are able to conduct the currents in this experiment without difficulty, as the currents are only fed through the bus bars over a very short period of time [67]. Such a bus bar design should theoretically give a low-inductive loop configuration (Section 4.1).

DC-link bulk capacitors are connected to the bus bar in parallel to the output from the rectifier stage. Six 20 μF MKP-series capacitors from Vishay with low ESR and high voltage and current

ratings are used (Section 4.2) [68]. The paralleling of six bulk capacitors reduces the stray inductance, as explained in Section 4.2. The bus bar is designed using the CadSoft Eagle software, and the circuit diagram is presented in Figure 5.10.

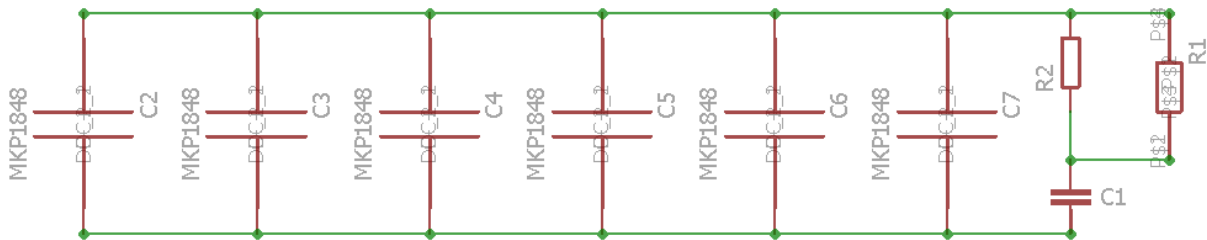


Figure 5.10: CadSoft Eagle – Bus bar with bulk capacitors and snubber

C2-C7 are the MKP-series bulk capacitors, while R1, R2 and C1 are different connection possibilities for a DC snubber circuit. The final bus bar PCB design is presented in Figure 5.11.

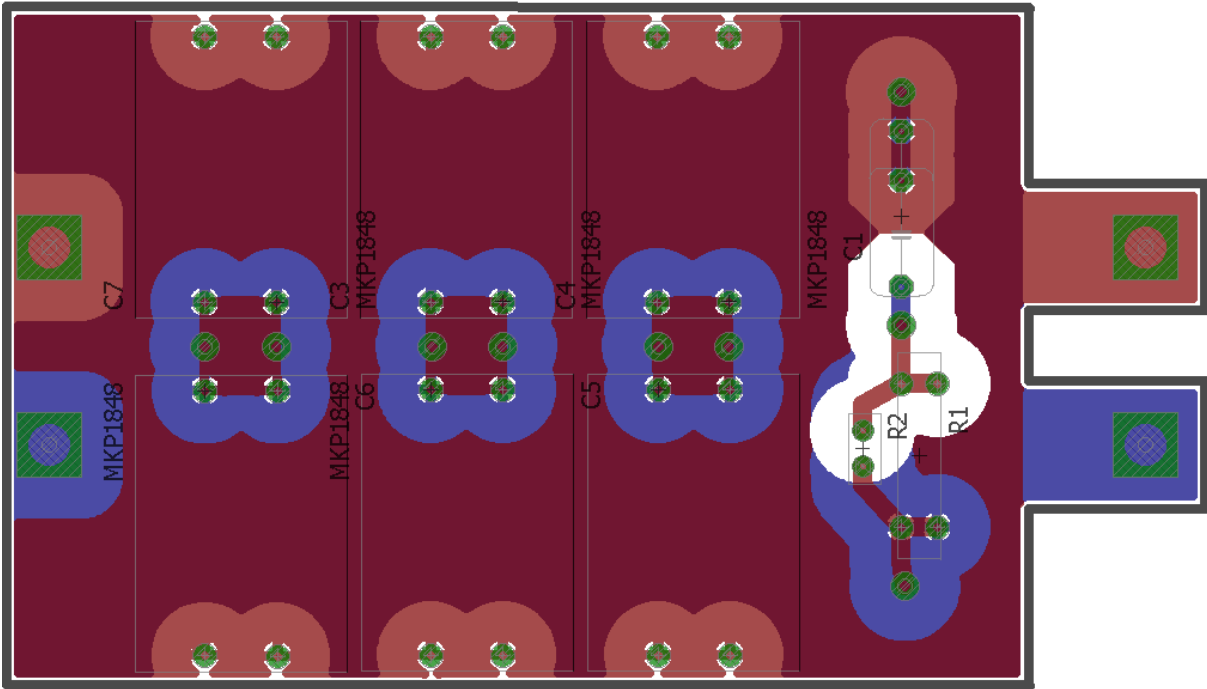


Figure 5.11: CadSoft Eagle – PCB design for bus bar

The area covered in blue and dark red is the DC- node, which is the bottom layer. The area covered in light red and dark red, except the three squares in the middle, is the DC+ node, which is the upper layer. The bus bar is designed so that it connects directly to the SiC module, which minimizes the distance between them. This design minimizes the stray inductance. Electrical clearance has to be considered, as the voltage potential between DC+ and DC- is 600 V. It is shown in Appendix A that an electrical clearance of 5 mm is more than sufficient for this kind of laboratory experiment. The bus bar includes the possibility of adding a DC snubber circuit

close to the SiC module, where R1, R2 and C1 are located. This will be further discussed in Section 5.6. All pads have thermal relief, as this makes it easier to solder components onto such a PCB with large copper planes (Section 4.5). The three dark red squares in the middle of the PCB are connected to the bottom layer (DC-) through vias, so that all the capacitor pins can be soldered from the same side of the board.

5.1.5 Electrical Equivalent of the Laboratory Setup

In this laboratory experiment, the upper SiC MOSFET will be off at all times. That is, the gate driver circuit will always output a negative biased gate-to-source voltage to the upper transistor. This means that the only switching transistor in this experiment will be the DUT.

The load inductor is a 250 μ H air-coil inductor manufactured at NTNU by using the relation in (4.4). Considerations regarding the choice of load inductor will be discussed in Section 5.4. The load inductor is connected in parallel with the upper SiC MOSFET. This means that when the DUT is on, there will be a current flowing from the rectifier stage through the load inductor and the DUT. When the DUT is off, the inductive load current will freewheel through the upper SiC SBD. This topology gives the desired step-down conversion of the voltage at the load terminals (Section 3.2).

As a safety measure, the minus side of the output from the rectifier stage is grounded. The heatsink of the SiC Power module is also grounded. This measure helps to reduce noise in voltage and current measurements on the oscilloscope. A detailed electrical equivalent of the full laboratory setup is presented in Figure 5.12.

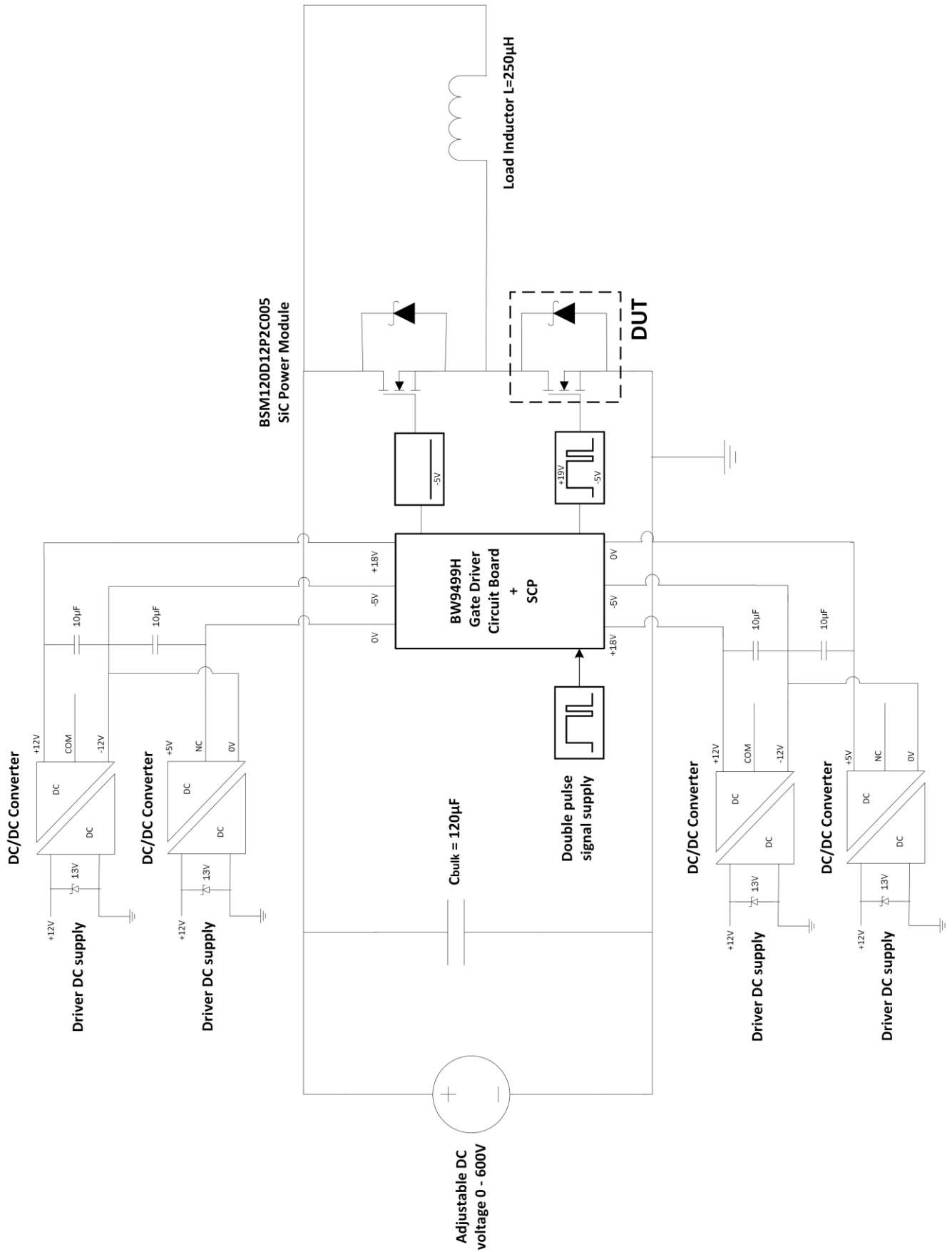


Figure 5.12: Electrical equivalent of the laboratory setup

5.2 Measuring Instruments

In the laboratory experiments, it is of interest to measure the drain-to-source voltage and the drain current of the DUT, as this is the switching component in the double-pulse test. The gate-to-source voltages of both transistors should also be monitored.

5.2.1 Oscilloscope

A MSO5104 high-bandwidth oscilloscope from Tektronix is used to capture all waveforms. The bandwidth of the oscilloscope is 1 GHz and it is able to capture 10 GS/s. It has some impressive features, including well-adjusted triggering features and complex mathematical operations. This makes it possible to analyze the high-speed transients and the power losses during switching.

The oscilloscope has four channels, making it possible to measure the drain-to-source voltage, the drain current and both the gate-to-source voltages simultaneously. By using the “math” feature, the power losses in the DUT can be calculated by multiplying the drain-to-source voltage and the drain current. Unfortunately, the drain current measuring instrument has different measurement delay than the drain-to-source voltage probe. This means that the deskew feature of the oscilloscope must be used in order to get correct power loss measurements. This will be carefully discussed in Section 5.5. It is possible to calculate the energy loss during switching directly on the oscilloscope by calculating the time integration of the power waveform.

5.2.2 Current Measurement

Two different current measuring instruments were used to measure drain current in the laboratory experiments. These were the CWT 6B high-current Rogowski Current Waveform Transducer from PEM [69] and the SSDN current shunt from T&M Research products. These two current measuring instruments have completely different working principles.

5.2.2.1 Rogowski Coil

The Rogowski coil is an air-core coil, which encloses the desired current lead. By Ampère’s law, a change in current through the coil induces a voltage. The Rogowski coil contains an integrator circuit, which provides an output that is proportional to the current through the coil [69]. As the coil has an air core, the Rogowski coil will not saturate. The CWT 6B Rogowski coil is able to measure currents up to 1200 A and it has a maximum bandwidth of 20 MHz. As the working principle of the Rogowski coil is Ampère’s law, it is not able to measure DC currents with this equipment. Thus, the lower bandwidth of the Rogowski coil is 1Hz.

For the Rogowski coil to be able to measure the drain current of the DUT, it must be connected to the circuit as depicted in Figure 5.13.

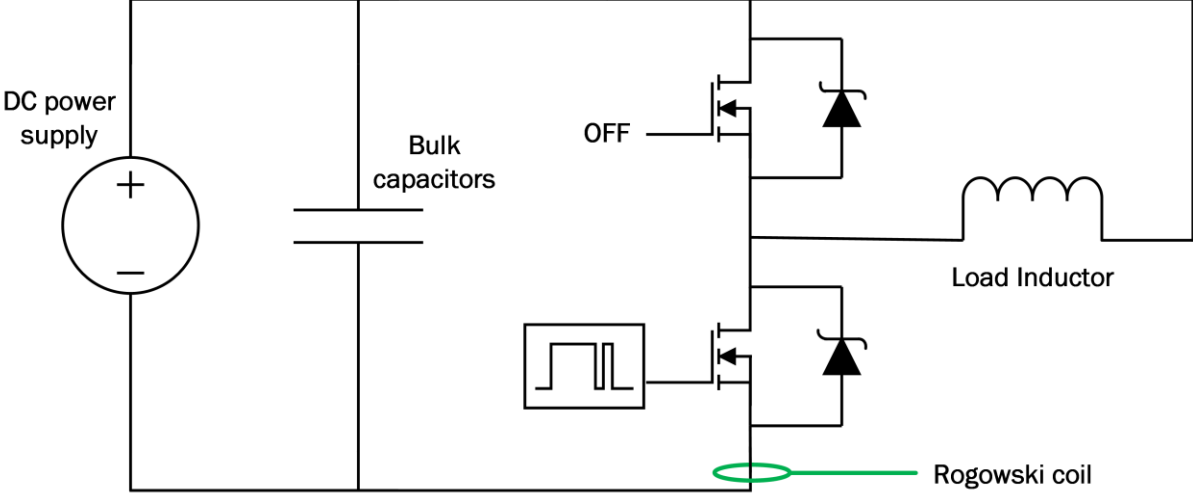


Figure 5.13: Rogowski coil placement

By placing the Rogowski coil in this manner, the drain current flowing through the DUT can be measured directly. A picture showing the placement of the Rogowski coil in the laboratory circuit is presented in Appendix G. After the connection of snubbers, the placement of the Rogowski coil gets even more important. If the Rogowski encloses the wrong lead, it could measure a different current than the drain current. This will be discussed in Section 7.7.

5.2.2.2 Current Shunt

A current shunt consists of a shunt resistor and two connection terminals. The working principle of the current shunt is to measure the voltage across its shunt resistor when current is flowing through it. As the shunt resistance is known, the current is also known. The SSDN series current shunt has a bandwidth of 400 MHz and maximal power of 2 W. The current shunt is not as practical to use as the Rogowski coil. While the Rogowski coil can measure current in almost every location, by enclosing the desired wire/cable, the current shunt must be connected in series with the current it is supposed to measure. This makes current measuring with a current shunt a little more challenging. Figure 5.14 presents the placement of the current shunt in the laboratory circuit.

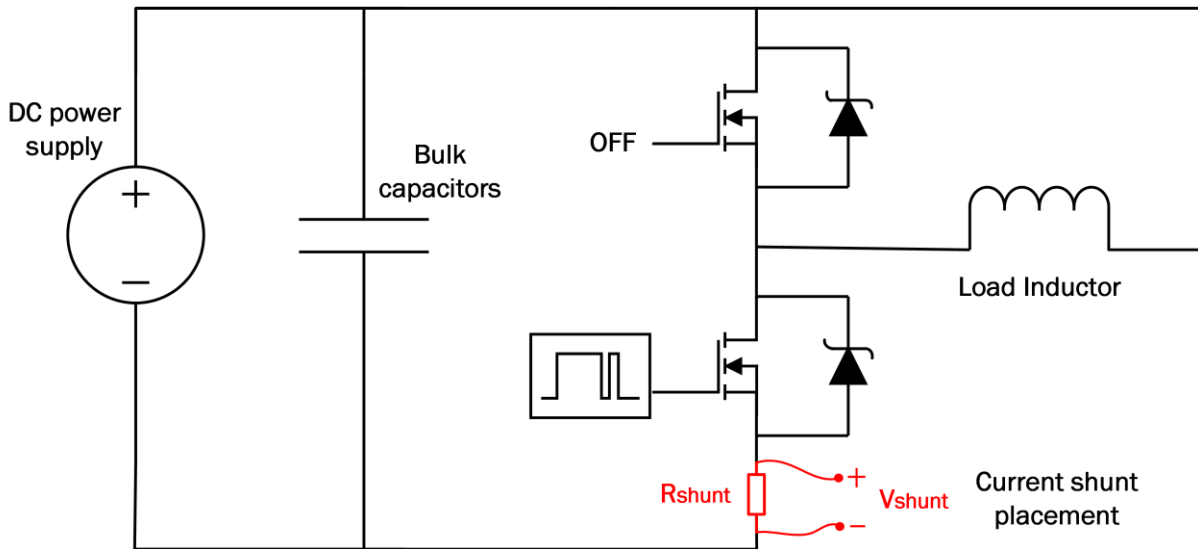


Figure 5.14: Current shunt placement

It is clear that the laboratory circuit must have a location where it is possible to connect the current shunt in series with the drain current, without influencing any part of the design. The SSDN series current shunt is well suited for current measurements in this kind of laboratory experiment, as it has low resistance and high bandwidth.

A measurement comparison of the two current measuring instruments presented in this section will be presented in Section 7.2.2.

5.2.3 Voltage Measurement

The drain-to-source voltage of the DUT is measured with the THDP0200 200 MHz differential high-voltage probe from Tektronix [70]. V_{ds} is measured across the terminals SS1 (pin 9) and SS2 (pin 6) of the SiC power module [38], as these terminals are closest to the DUT. The gate-to-source voltages are measured with the P5200A 50 MHz differential high-voltage probe, also from Tektronix [70]. V_{gs2} of the DUT is measured across the terminals G2 (pin 5) and SS2 (pin 6). These probes were chosen due to low stray inductance compared to other probes, as well as voltage ratings above 1000 V. A measurement comparison of the two voltage probes will be presented in Section 7.2.1.

5.3 List of Laboratory Equipment

A complete list of the equipment used in the laboratory experiments is provided in Table 5.2:

Table 5.2: List of laboratory equipment

| Application | Equipment | Name | Manufacturer |
|--------------------------------------|---------------------------------|-----------------|-----------------------|
| Drain current measurement | Rogowski coil | CWT 6B | PEM |
| Drain current measurement | Current shunt | SSDN series | T&M Research Products |
| Turn-off snubber current measurement | Rogowski coil | CWT 06B | PEM |
| Gate-to-source voltage measurement | Differential high-voltage probe | P5200A | Tektronix |
| Drain-to-source voltage measurement | Differential high-voltage probe | THDP0200 | Tektronix |
| Waveform analysis | Oscilloscope | MSO5104 | Tektronix |
| Double-pulse supply | Pulse/function generator | Model 187 | Wavetek |
| DC power supply | 600 V–10 A DC power supply | SM6000-series | Delta Elektronika |
| Driver DC supply | DC supply | 72-8345 | Tenma |
| Driver DC supply | DC supply | 72-10495 | Tenma |
| Gate drivers | Gate driver circuit board | BW9499H | Rohm |
| Device under test | SiC Power Module | BSM120D12P2C005 | Rohm |

Table 5.2 does not include the components used in the converter design. Thus, the complete BOM is given in Appendix C.

5.4 Load Inductor Considerations

In Figure 5.12, a 250 μH load inductor is connected in parallel with the upper transistor. This is chosen to be an air-core inductor because this results in lower parasitic capacitance at high frequencies and thus less ringing (Section 4.3). Initially, an inductance of $L = 900 \mu\text{H}$ was chosen because this was the only suitable air-core inductor available at the laboratory. As this inductance is quite high, the di/dt through the load inductor is lower than with a smaller inductor. This can be seen from the definition of inductance (DC resistance of the inductor neglected):

$$V = L \cdot \frac{di}{dt} \Rightarrow \frac{di}{dt} = \frac{V}{L} \quad (5.5)$$

V is the voltage applied across the inductor, During initial laboratory experiments, problems related to a slow di/dt were experienced. For high drain currents, the DC-link voltage from the rectifier stage dropped substantially after the double pulse. The voltage drop at the DC link for a double-pulse test at 600 V drain-to-source voltage and 120 A drain current with $L = 900 \mu H$ is depicted in Figure 5.15:

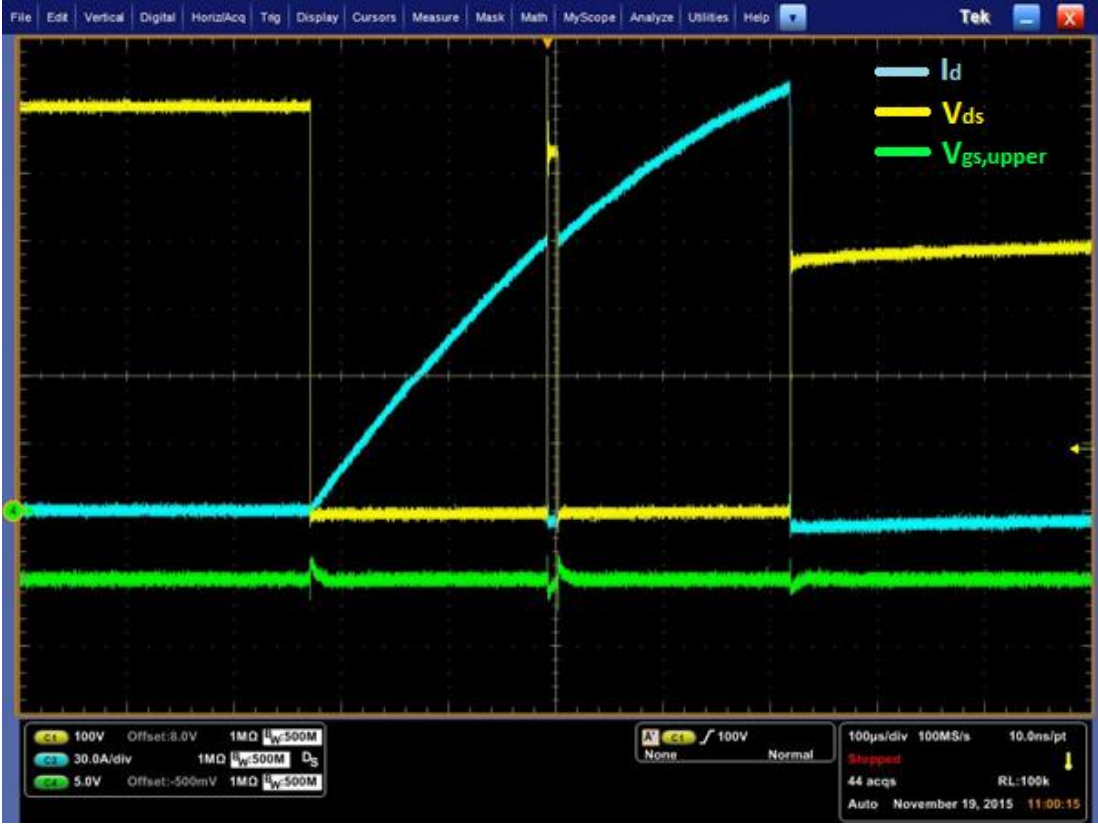


Figure 5.15: 600 V 120 A double-pulse test with $L = 900 \mu H$

The drain-to-source voltage drops down to less than 400 V after the double pulse. This is probably due to the current limitation in the 600 V-10 A DC power supply, as the DC current limit of the DC power supply is 10 A and the output power limit 6000 W. However, double-pulse tests can be done at a much higher output power from the rectifier stage. This is because the double pulses normally are very short, which means that the overcurrent protection system in the DC power supply does not have the time to react and intervene during the double pulse. In Figure 5.15 however, the first pulse needs to be quite wide in order to reach 120 A drain current. As the output power from the rectifier stage is $120 A \cdot 600 V = 72000 W$ and higher for a significant period, the overcurrent protection has the time to intervene. Since the output power is too high, the power supply intervenes by lowering the output voltage.

This problem can easily be solved by using a smaller load inductor, as explained in Section 4.3. A smaller load inductor gives a higher di/dt and thus a much shorter pulse for a given drain

current. By using (4.4), the dimensions of a smaller air-core inductor can be found. It was decided to make a 250 μH single-layer air-core inductor with $n = 70$ turns. By substituting the old 900 μH load inductor with the new 250 μH load inductor, the double-pulse test response in Figure 5.16 was obtained:



Figure 5.16: 600 V 120 A double-pulse test with $L = 250 \mu\text{H}$

The voltage drop in Figure 5.16 is much lower than in Figure 5.15. As opposed to earlier, turn-on and turn-off transients at 600 V 120 A can be analyzed. An even better response could be obtained by lowering the load inductance even further.

At high load currents, the di/dt starts to decrease substantially. It seems as the inductor current reaches some sort of saturation. As the load inductor has an air core, a saturation is not possible. The reason that the di/dt decreases, is that the resistive conduction losses in the inductor coil become significant for high currents. Thus, equation (5.5) describing the voltage across the load inductor becomes:

$$V = L \cdot \frac{di}{dt} + R_{DC} \cdot i \Rightarrow \frac{di}{dt} = \frac{1}{L} \cdot (V - R_{DC} \cdot i) \tag{5.6}$$

R_{DC} is the DC resistance of the load inductor. At high drain currents, the product $R_{DC} \cdot i$ becomes significant, leading to a lower di/dt in the load inductor. The 900 μH inductor has a DC resistance of $R_{DC,900} = 1.1 \Omega$, while the 250 μH inductor has a lower DC resistance of approximately $R_{DC,250} = 0.5 \Omega$. This is less than half the resistance of the 900 μH inductor. Because of this, the di/dt does not decrease as significantly in Figure 5.16 as in Figure 5.15. Thus, the experimental part will be conducted with the 250 μH load inductor.

5.5 Measurement Delay

In order to calculate the power losses in the DUT, it is important to use probes and other measuring instruments with high bandwidths. As voltages and currents are measured on a scale of a few nanoseconds, the probes will have significantly different measurement speeds. That is, the drain current measured through the transistor will have a delay relative to the drain-to-source voltage measured across the transistor. The measurement delay of different measuring instruments increases with the length of the cables.

In order to compensate for this delay between the instruments, it is important to find the measurement delay in the different measuring instruments so that that the deskewing feature of the oscilloscope can synchronize the signals. To determine this measurement delay, the following circuit is used [71]:

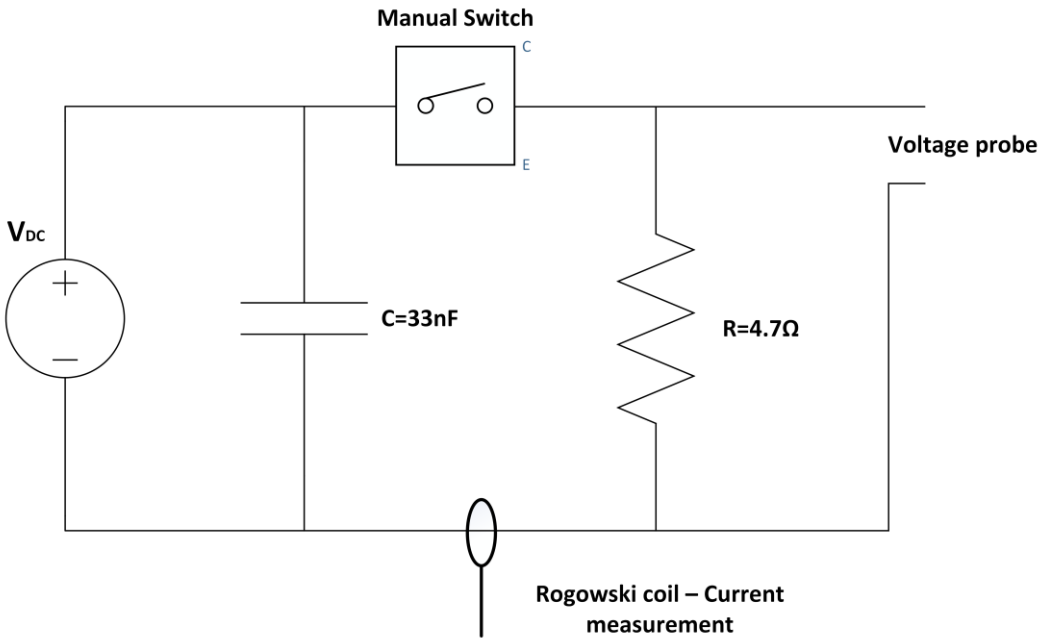


Figure 5.17: Determination of measurement delay

When the switch is off, the DC voltage source charges the capacitor. When the manual switch is turned on, a current will start to flow in the resistor and the voltage across the resistor will

rise to the DC voltage. By measuring the voltage across, and the current through, the resistor, it is possible to measure the propagation delay that the Rogowski coil has relative to the voltage probe. In this test, a DC voltage of $V_{DC} = 10\text{ V}$ is used. This gives a current of just above 2 A through the resistor when the switch is on.

The following probes are tested:

- CWT 6B, 20 MHz Rogowski coil
- THDP0200, 200 MHz differential high-voltage probe
- P5200A, 50 MHz differential high-voltage probe

PEM Ltd states that the measurement delay of CWT 6B is 50 ns [69]. Unfortunately, it is not known what is used as reference in this test. As there are three different measuring instruments with three different measurement delays, a test of these delays needs to be done. As the THDP0200 probe is the fastest one, this is set as reference probe. The measurement delays are measured at the rising edge of the current and the voltage of the resistor when the manual switch is closed. The results are presented in Figure 5.18 and Figure 5.19:

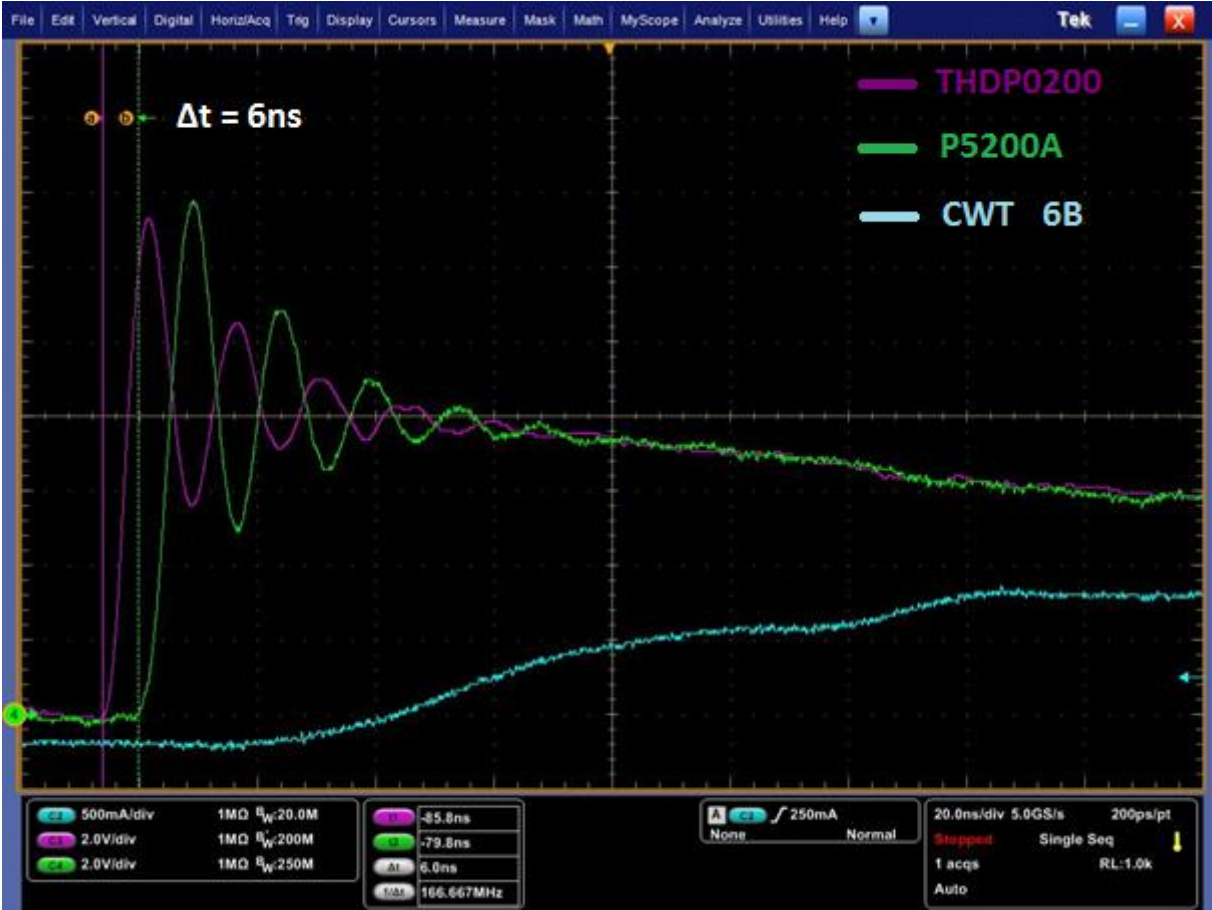


Figure 5.18: Measurement delay between THDP0200 and P5200A

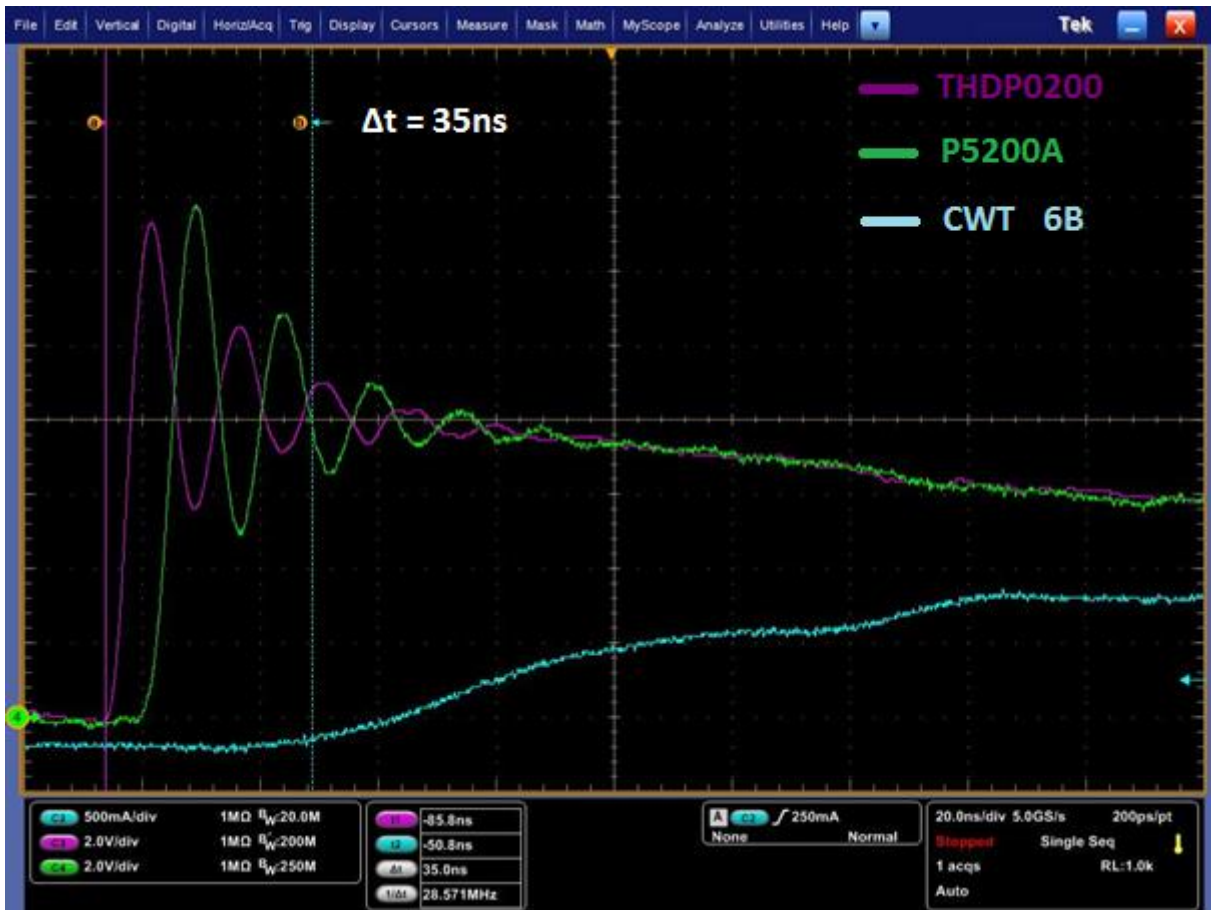


Figure 5.19: Measurement delay between THDP0200 and CWT 6B

The bandwidth limit of CWT 6B was set to 20 MHz on the oscilloscope, in order to avoid the high-frequency noise on the current signal. This can be done without slowing down the current rise time, as the bandwidth of the Rogowski actually is 20 MHz. From Figure 5.18, the P5200A differential probe reacts about 6 ns slower than the THDP0200 differential probe. From Figure 5.19, the CWT 6B Rogowski coil reacts about 35 ns slower than the THDP0200 differential probe. This means that the measurement delay of CWT 6B relative to P5200A is 29 ns. These measurements were verified with different voltages and currents through many tests. In all oscilloscope measurements, the CWT 6B Rogowski coil is deskewed 35 ns in order to be synchronized with THDP0200. P5200A is deskewed 6 ns relative to THDP0200.

5.6 Theoretical Snubber Design

The switching characteristics of the DUT show extensive voltage overshoot and long-lasting ringing due to parasitic inductance and capacitance inside the module itself and in other parts of the test circuit. In order to reduce this parasitic oscillation, snubber circuits can be designed and implemented. There are different ways of implementing snubbers in power circuits,

depending on what kind of snubber that is needed. Two possible solutions that can be implemented in the laboratory circuit are presented in Figure 5.20.

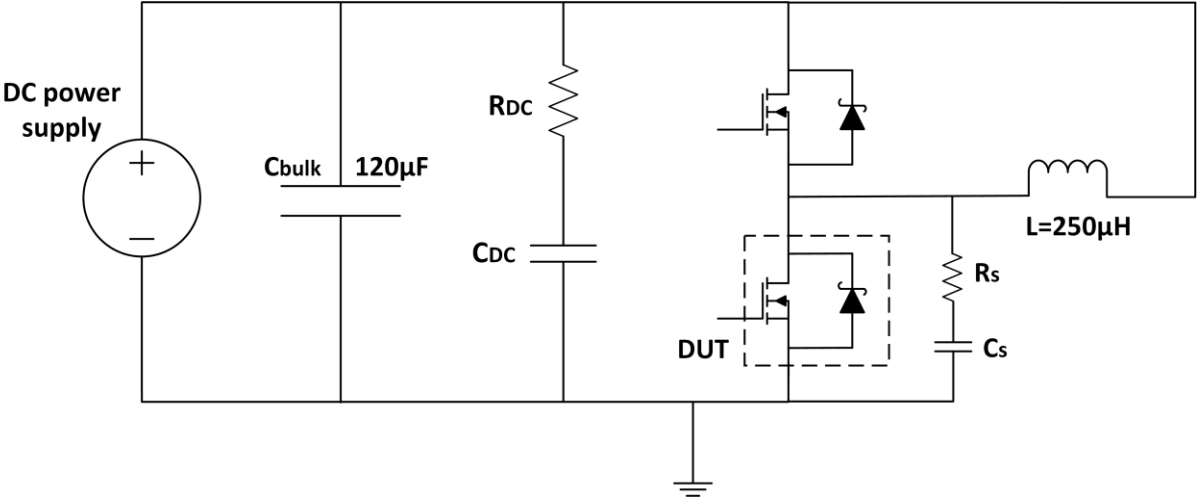


Figure 5.20: Implementation of DC snubber and turn-off snubber

A DC snubber is connected in parallel with the half-bridge module, depicted by R_{DC} and C_{DC} . The snubber connected in parallel with the DUT, depicted by R_s and C_s , is called a turn-off snubber. These two snubbers have different properties and advantages, explained in Section 4.6. Both snubber configurations are RC snubbers. As for all other passive components discussed in Chapter 5, snubber capacitors and resistors introduce parasitic inductance. This stray inductance should be minimized in order not to introduce new problems during switching. Thus, low- or non-inductive components should be chosen in the snubber configurations.

The optimal theoretical values of the DC snubber and the turn-off snubber will be calculated in the following, using Section 4.7.4 and Section 4.7.1 respectively.

5.6.1 DC Snubber Calculation

In order to be able to design a suitable DC snubber, the DUT turn-off voltage waveform is needed. This was explained in Section 4.7.4. Thus, a double-pulse test without snubber is conducted at 600 V 90 A. This gives the DUT turn-off voltage waveform in Figure 5.21:

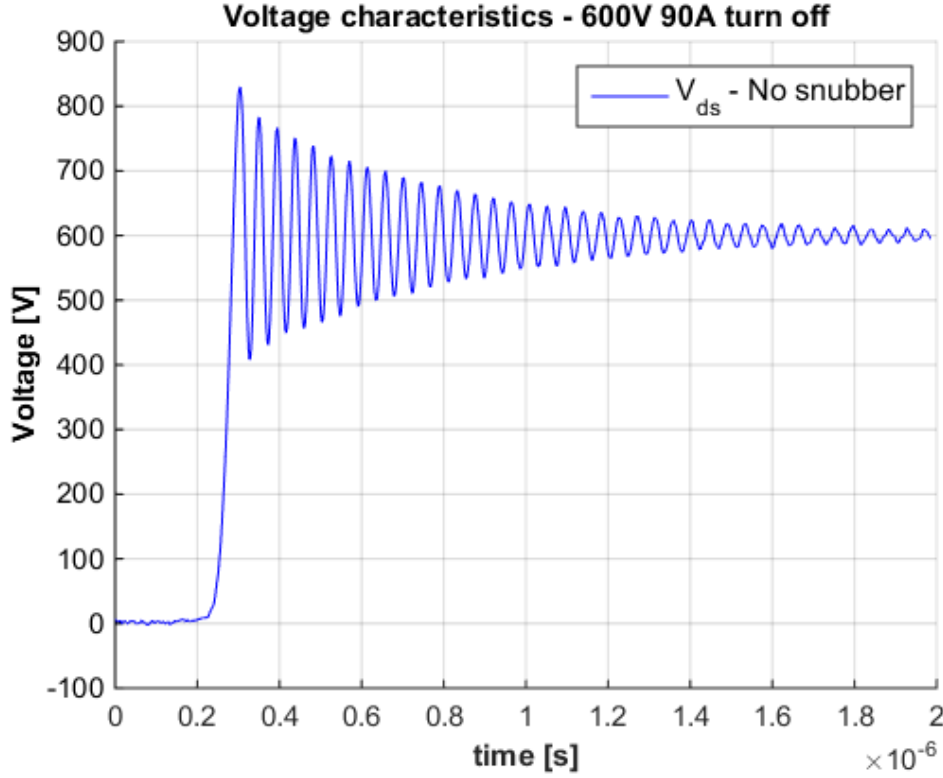


Figure 5.21: DUT turn-off voltage characteristics at 600 V 90 A

The DC snubber will be designed based on the DUT turn-off voltage characteristics. The extensive ringing in Figure 5.21 has a frequency of $f_r = 22.7 \text{ MHz}$. This ringing is caused by a resonance between the parasitic capacitance C_p of the SiC power devices (SiC MOSFET and SiC SBD) and the stray inductance L_s in the test circuit. From [38], $C_p = 1.45 \text{ nF}$. Thus, by using (4.11), the following can be found:

$$L_s = \frac{1}{(2\pi)^2 \cdot f_r^2 \cdot C_p} = \frac{1}{(2\pi)^2 \cdot (21.3 \text{ MHz})^2 \cdot 1.45 \text{ nF}} = 34 \text{ nH} \quad (5.7)$$

This is the total stray inductance in the entire test circuit, where about 20 nH is placed inside the module itself. By choosing the damping coefficient in order to obtain critical damping of the ringing, i.e. $\zeta = 1$, the DC snubber resistor R_{DC} can be calculated using (4.12).

$$R_{DC} = \frac{1}{2 \cdot \zeta} \sqrt{\frac{L_p}{C_p}} = \frac{1}{2 \cdot 1} \sqrt{\frac{34 \text{ nH}}{1.45 \text{ nF}}} = 2.4 \Omega \quad (5.8)$$

By using (4.13), the DC snubber capacitor can be found.

$$C_{DC} = \frac{1}{2\pi \cdot R_{DC} \cdot f_r} = \frac{1}{2\pi \cdot 2.4 \Omega \cdot 22.7 \text{ MHz}} = 2.9 \text{ nF} \quad (5.9)$$

This theoretical DC snubber calculation will be tested in both simulation and experiment. The bus bar PCB, shown in Figure 5.11, includes the possibility of connecting such a DC snubber close to the SiC module, which makes it possible to test the DC snubber experimentally.

5.6.2 Turn-Off Snubber Calculation

The turn-off snubber capacitor can be calculated from the DUT turn-off characteristics, by using (4.6). From the 600 V 90 A DUT turn-off characteristics in Figure 5.21, the current fall time is $t_f = 42 \text{ ns}$. This gives the following turn-off snubber capacitor.

$$C_s = \frac{I_d \cdot t_f}{2 \cdot V_{ds}} = \frac{90 \text{ A} \cdot 42 \text{ ns}}{2 \cdot 600 \text{ V}} = 3 \text{ nF} \quad (5.10)$$

The turn-off snubber resistor can be calculated by using (4.7). At the DUT drain current rating of 120 A, the following snubber resistor can be calculated.

$$R_s = \frac{V_{ds}}{0.2 \cdot I_0} = \frac{600 \text{ V}}{0.2 \cdot 120 \text{ A}} = 25 \Omega \quad (5.11)$$

As the main purpose of the turn-off snubber is to reduce voltage overshoot and ringing, the snubber diode is not included as a part of the turn-off snubber in Figure 5.20. This, however, leads to higher switching losses, as explained in Section 4.7.1. The turn-off snubber will be tested in both simulation and experiment.

6. Simulations in LTspice IV

6.1 Introduction

In order to investigate and test the converter design and the switching characteristics of the DUT in simulation, LTspice IV is used as simulation tool. An LTspice model of the SiC power module was provided by Rohm Semiconductor. In order to make the simulation as realistic as possible, many considerations had to be taken into account. Stray inductance and gate driver circuit layout are some of the important and challenging aspects that had to be realized in the simulation circuit. The circuit implemented in LTspice is a double-pulse test circuit of the performance of the DUT, which is made as similar to the laboratory setup as possible. This chapter presents the LTspice circuit design and the DUT switching characteristics obtained through simulation. Subsequently, snubber design in order to improve the switching characteristics is discussed and tested.

In the simulation and laboratory results of this thesis, it was decided to focus on the current waveform during turn on and the voltage waveform during turn off. This was done in order to present the switching characteristics and improvements in the most transparent manner possible, without having too many waveforms in the same figure. This choice was explained in Section 3.5.1.

An example of a double-pulse test at 600 V drain-to-source voltage and 120 A drain current, obtained through simulations in LTspice IV, is presented in Figure 6.1.

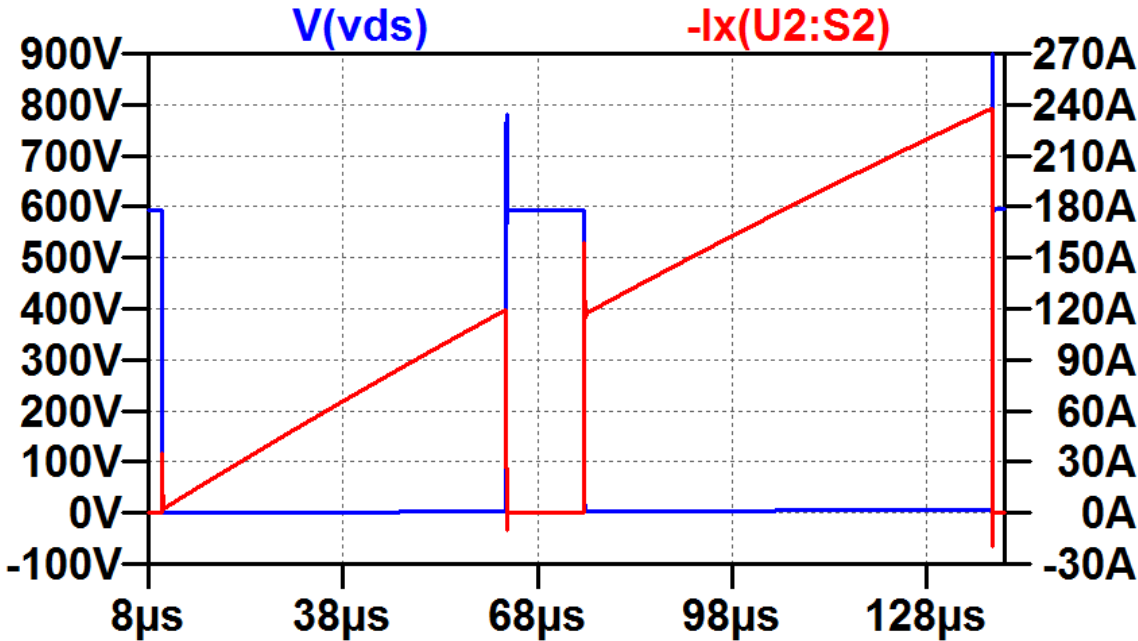


Figure 6.1: Simulation – Double-pulse test

6.2 LTspice IV Circuit Design

The simulation circuit in LTspice is designed to be as realistic as possible. That is, the circuit design should have the same parameters as the laboratory setup. The SiC power module is represented by an LTspice model provided by Rohm Semiconductor. This model includes parasitic inductance and capacitance. Some parts of the circuit, such as the load inductor and the DC-link capacitors, are easily implemented. Other parts of the circuit, such as the loop stray inductance and the gate driver circuit, are more challenging to design. Due to this, laboratory experiments are used in order to improve the simulation circuit in order for the simulation results to be as close as possible to the laboratory results. This method makes it possible to include stray inductance in the simulation circuit that is somewhat similar to that of the laboratory setup. The LTspice simulation circuit is presented in Figure 6.2.

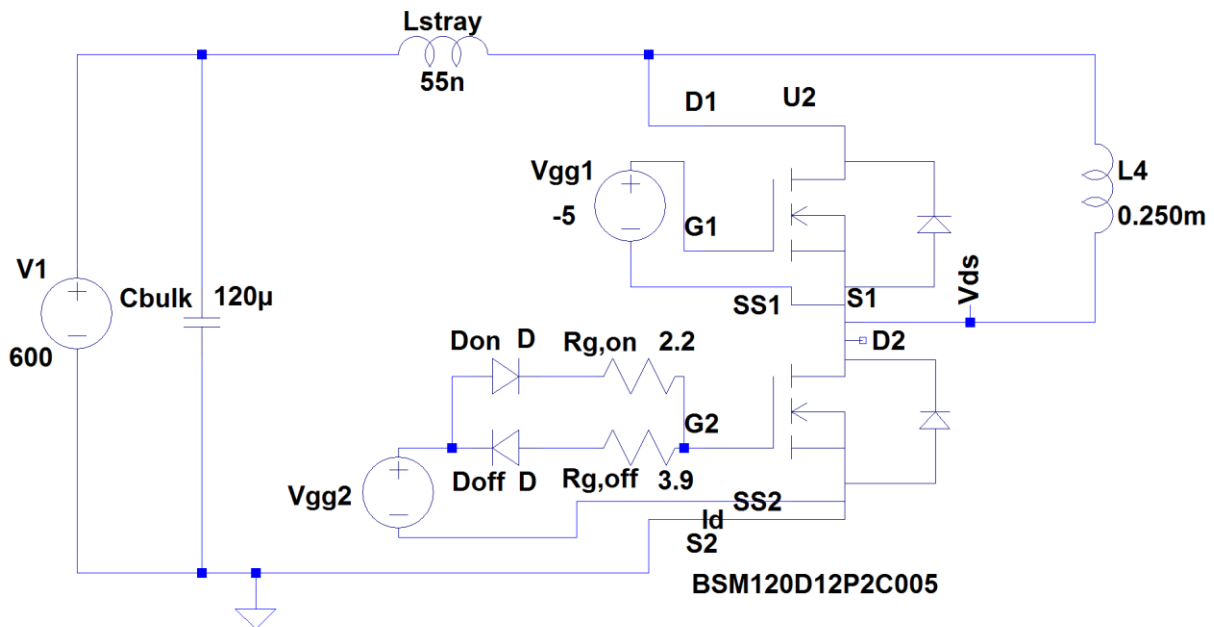


Figure 6.2: Simulation circuit in LTspice IV

The total stray inductance outside the SiC power module is lumped and placed in the inductor L_{stray} . In addition, the LTspice model of the SiC module includes some stray inductance. The total stray inductance in Figure 6.2 is higher than what was calculated in (5.7). However, this amount of inductance is needed in order to obtain similar voltage overshoot in simulation and laboratory experiment. The influence of stray inductance on the simulation results will be thoroughly discussed in Section 7.9.

The load inductor $L_4 = 0.250mH$, with a DC resistance of 0.5Ω (Section 5.4), is connected across the upper switch of the module. This switch is always off, due to the negative biased gate voltage V_{gg1} . The DUT (lower transistor), however, is given a double pulse signal through the voltage V_{gg2} . The use of two separate turn-on and turn-off gate resistors, $R_{g,on}$ and $R_{g,off}$ in Figure 6.2, makes it possible to investigate the influence of the gate-to-source voltage rise time and fall time on the DUT switching characteristics. The six parallel $20 \mu F$ DC-link capacitors are lumped and implemented as $C_{bulk} = 120 \mu F$. V_1 is the DC power supply from the rectifier stage.

6.3 Switching Characteristics and Switching Losses

The switching characteristics of the DUT are investigated at 600 V drain-to-source voltage for four different drain currents. This is done in order to analyze the influence of drain current on the DUT switching transients. Only the 600 V 120 A switching characteristics are presented in the simulation part. The switching characteristics at 30 A, 60 A and 90 A drain currents are given in Appendix D.

6.3.1 Turn-Off Switching Characteristics

Firstly, the DUT turn-off switching characteristics are investigated at 600 V drain-to-source voltage. The turn-off switching characteristics at 120 A drain current are presented in Figure 6.3. Switching characteristics for 30 A, 60 A and 90 A drain currents are given in Appendix D.1.

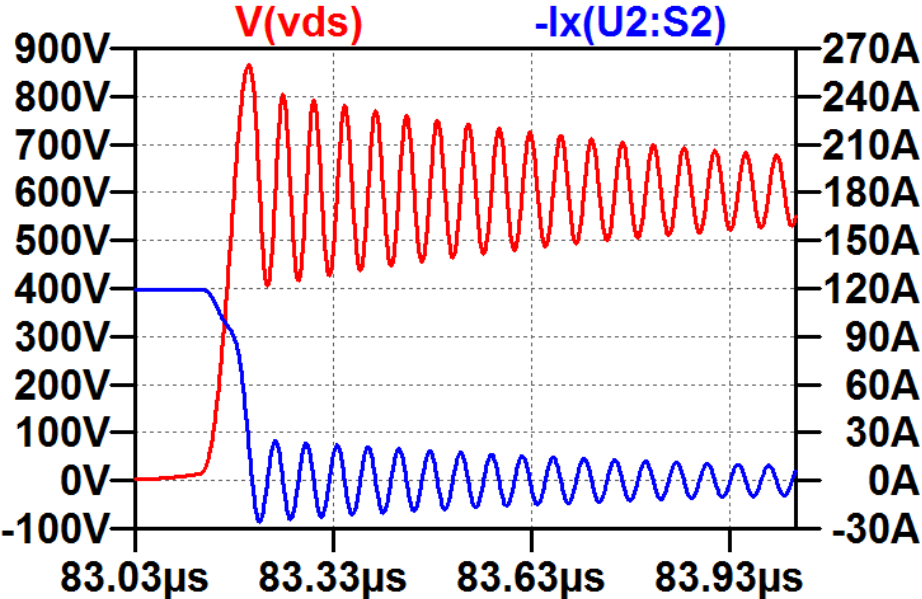


Figure 6.3: Simulation – Turn-off characteristics at 600 V 120 A

The turn-off switching characteristics show extensive voltage overshoot and ringing at all drain currents. In order to compare the switching transients at different drain currents, voltage rise time t_{rv} , voltage derivative dv/dt current fall time t_f and voltage overshoot V_{os} are found during DUT turn off, and are presented in Table 6.1. These parameters are measured by using the method described in Section 3.5.1.

Table 6.1: Simulation – Turn-off switching characteristics

| I_d [A] | Turn off | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{rv} [ns] | t_f [ns] | dv/dt [V/ns] | V_{os} [V] |
| 30 | 50 | 65 | 9.60 | 56 |
| 60 | 39 | 55 | 12.3 | 147 |
| 90 | 35 | 51 | 13.7 | 214 |
| 120 | 33 | 49 | 14.5 | 265 |

The di/dt-caused voltage overshoot increases for increased drain current. This is because the current fall time decreases. The voltage rise time also decreases with drain current, which leads to an increase in voltage derivative dv/dt .

6.3.2 Turn-On Switching Characteristics

In the same manner, the DUT turn-on characteristics are investigated at 600 V drain-to-source voltage. The turn-on switching characteristics at 120 A drain current are presented in Figure 6.4. Turn-on switching characteristics at 30 A, 60 A and 90 A drain currents are presented in Appendix D.2.

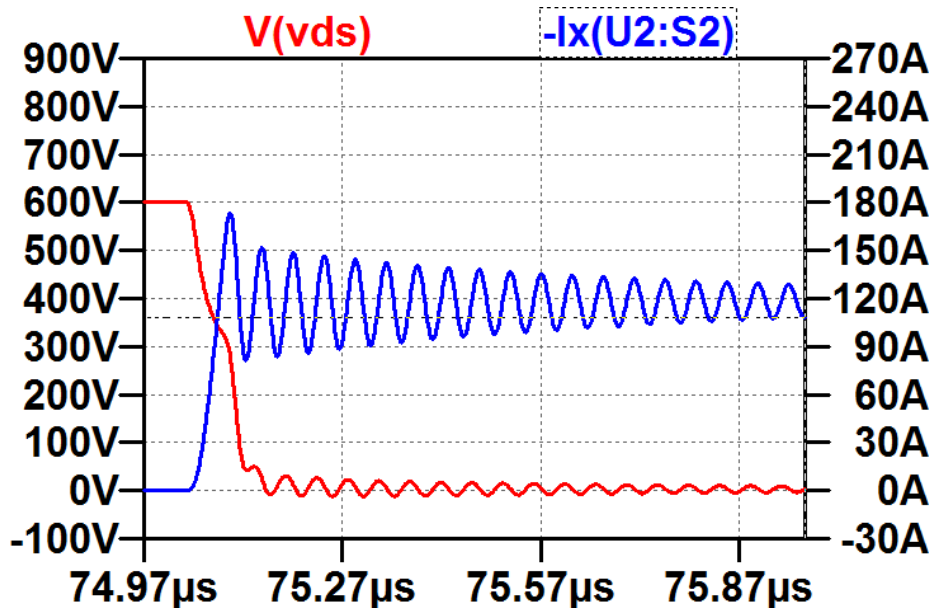


Figure 6.4: Simulation – Turn-on characteristics at 600 V 120 A

The current transient at DUT turn on has extensive current overshoot and long-lasting ringing. The voltage transient, on the other hand, has negligible ringing. The turn-on switching transients

are inspected by measuring current rise time t_r , current derivative di/dt , voltage fall time t_{fv} and current overshoot I_{os} during DUT turn on (Section 3.5.1). This is presented in Table 6.2.

Table 6.2: Simulation – Turn-on switching characteristics

| I_d [A] | Turn on | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{fv} [ns] | t_r [ns] | di/dt [A/ns] | I_{os} [A] |
| 30 | 49 | 13 | 1.85 | 52 |
| 60 | 56 | 19 | 2.52 | 52 |
| 90 | 63 | 25 | 2.88 | 53 |
| 120 | 72 | 29 | 3.31 | 53 |

It is found that that the switching times increase with drain current. It is clear that the current overshoot is very little affected by the increase in drain current, as it is close to constant. This is as expected, as the reverse-recovery current of the diode consists of discharge of its junction capacitance during turn on. As explained in Section 2.3.1, the charge stored in the junction capacitance is close to independent of drain current. Thus, the reverse-recovery current is also close to independent of drain current.

6.3.3 Switching Times

Figure 6.5 presents the switching times of the DUT, which were obtained in Table 6.1 and Table 6.2, in a graphical manner. The switching times are given as a function of drain current.

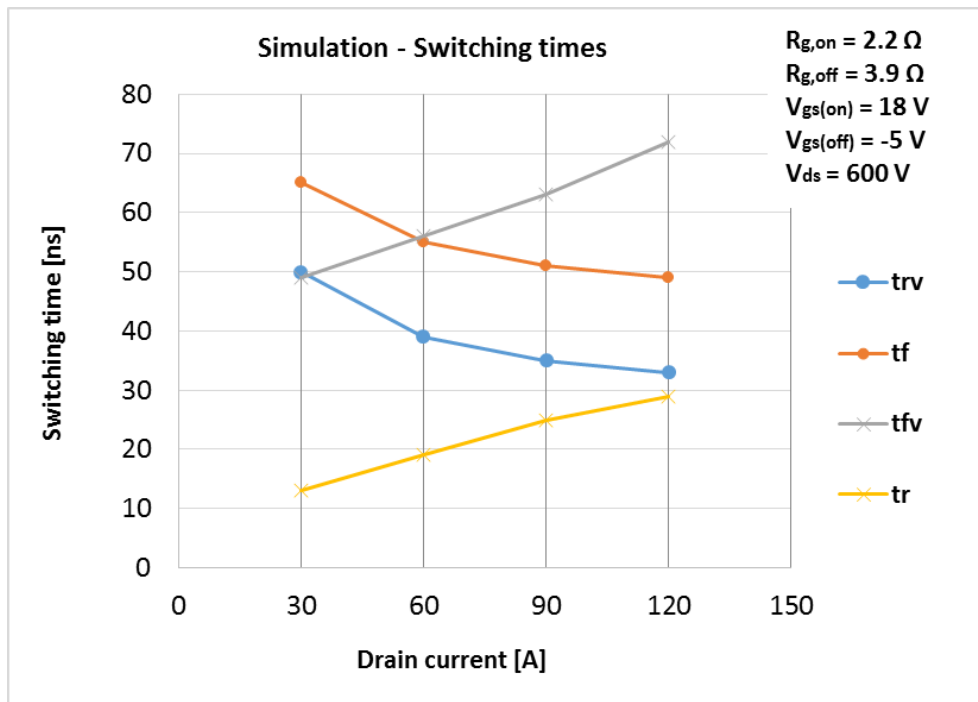


Figure 6.5: Simulation – Switching times as a function of drain current

It is observed that the turn-off switching times decrease with drain current, while the turn-on switching times increase.

6.3.4 Switching Losses

The DUT switching losses can be calculated by using the method described in Section 3.6. This is presented as a function of drain current in Figure 6.6. The parameters in the figure are:

- E_{on} – Turn-on switching losses in the DUT
- E_{off} – Turn-off switching losses in the DUT
- $E_{tot} = E_{on} + E_{off}$ – Total switching losses in the DUT

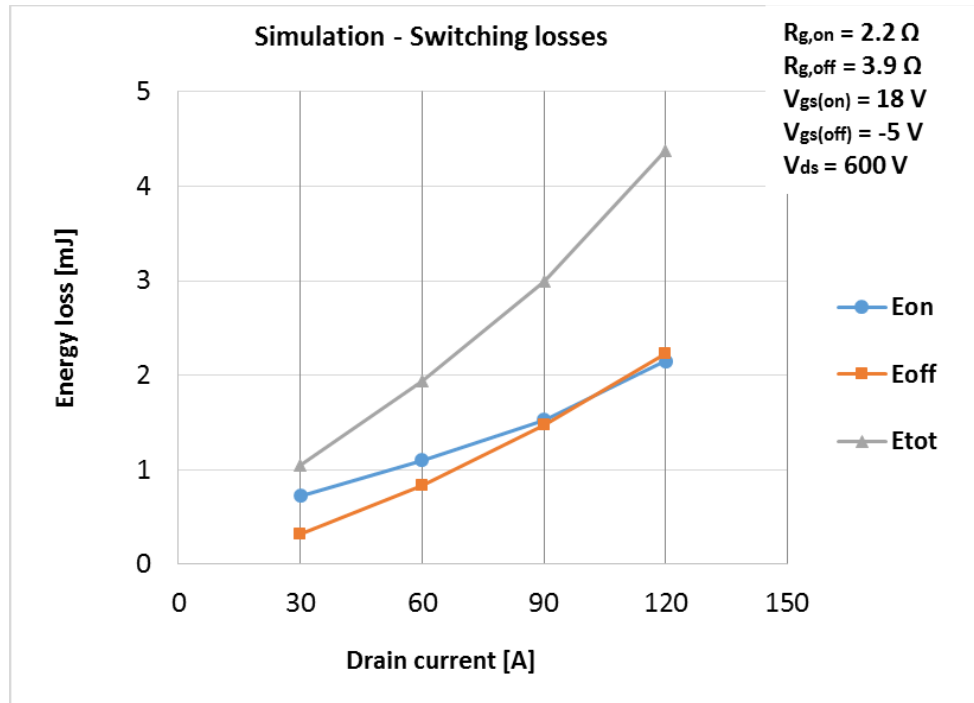


Figure 6.6: Simulation – Switching losses as a function of drain current

An extremely fast turn-on transient causes very low turn-on switching losses, which gives similar losses at turn on and turn off. Normally, the turn-on switching losses are higher than the turn-off switching losses [72]. Both the turn-on and the turn-off switching losses increase with drain current.

6.4 Influence of Gate Resistor on Switching Times and Switching Losses

In order to investigate the influence of the gate resistance on the DUT switching characteristics, the switching time and the switching losses will be analyzed for different gate resistance. Thus, the turn-on and turn-off gate resistors $R_{g,on}$ and $R_{g,off}$ are combined in one single gate resistor R_g . Firstly, the switching times are found as a function of gate resistance in Figure 6.7. These results are obtained at 600 V drain-to-source voltage and 120 A drain current.

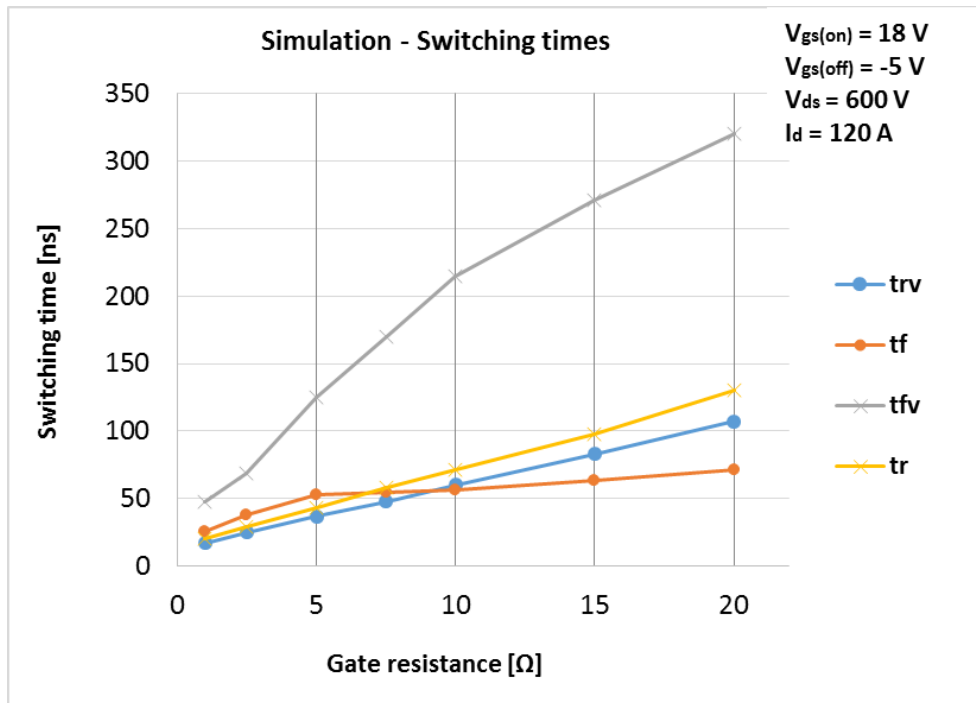


Figure 6.7: Simulation – Switching times as a function of gate resistance

It is clear that all switching times increase with increased gate resistance. However, the slope of the voltage fall time is much higher than for all the other switching times.

The switching losses are presented as a function of gate resistance in Figure 6.8. These results are also obtained at 600 V drain-to-source voltage and 120 A drain current.

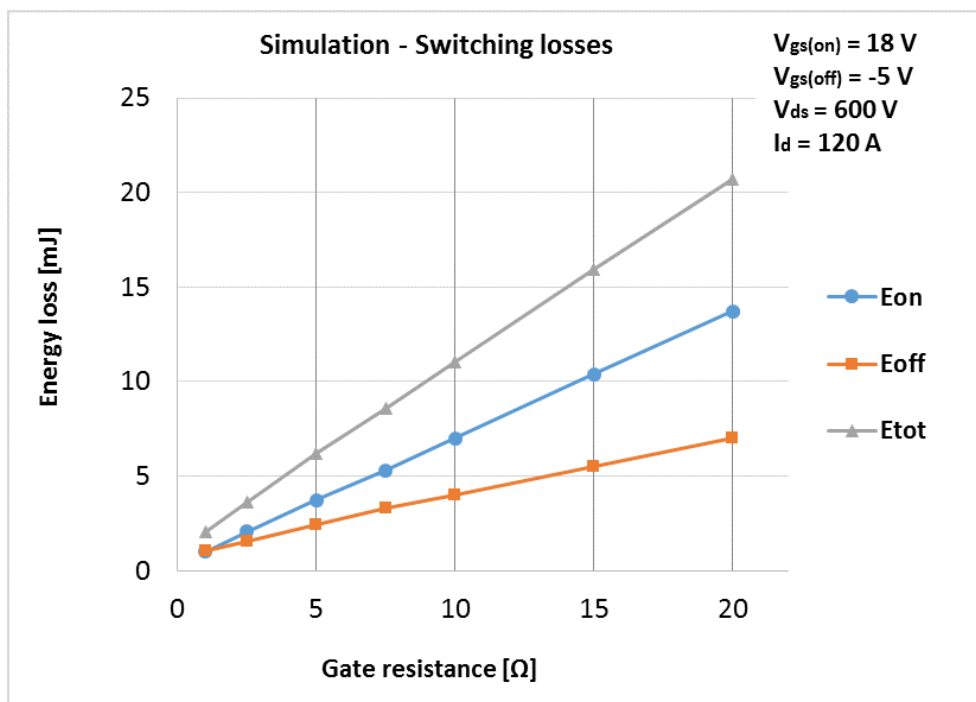


Figure 6.8: Simulation – Switching losses as a function of gate resistance

The switching losses increase with increased gate resistance, as the switching transients are slowed down. This leads to a wider “overlap” between current and voltage. The turn-on switching losses has a higher slope than the turn-off switching losses.

The switching times in Figure 6.7 are much lower for low gate resistance, as the gate driver current capability is much higher. Thus, the gate-to-source voltage rise time and fall time are much faster, as explained in Section 4.6.1. This influences the switching times of the DUT.

6.5 Snubber Design

It was shown in Section 6.3.1 and Section 6.3.2 that the DUT turn-off and turn-on transients are extremely fast, causing high overshoots and long-lasting ringing. In order to improve the DUT switching characteristics, snubber circuits can be designed and added to the simulation circuit. This section presents the effects of adding RC snubber circuits to the LTspice simulation circuit. These snubber designs were thoroughly explained in Section 4.6 and designed in Section 5.6.

6.5.1 DC Snubber

The DC snubber designed in Section 5.6.1 will be tested through simulations in LTspice. The resulting simulation circuit including DC snubber is presented in Figure 6.9.

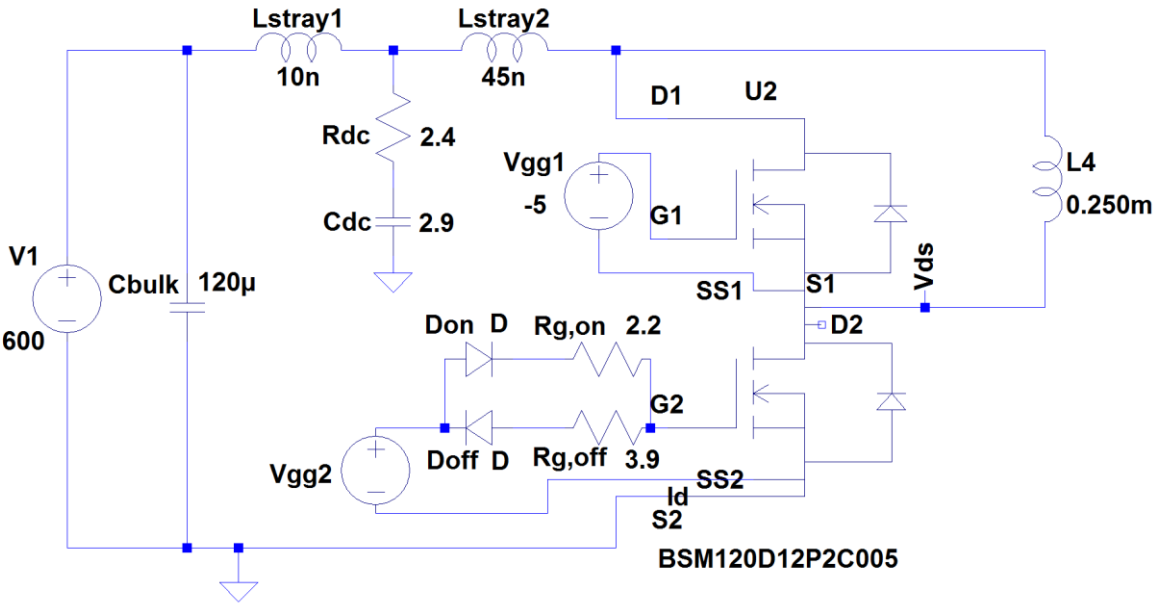


Figure 6.9: Simulation circuit including DC snubber

The DC snubber is depicted by the resistor R_{dc} and the capacitor C_{dc} . The values of these components were calculated in Section 5.6.1 to be $R_{DC} = 2.4 \Omega$ and $C_{DC} = 2.9 nF$. It is important to notice that the stray inductance in Figure 6.9 is different from what was presented

in Figure 6.2. The stray inductance is now split into two different inductances. The reason for this is that there is a lot of inductance close to, and inside, the SiC module. From the comparison of simulation results and laboratory results, there is reason to believe that the real stray inductance inside the SiC module is higher than what was provided in the LTspice simulation model. Thus, a big part of the stray inductance must be placed between the DC snubber and the module. This is depicted by the inductor L_{stray2} . This stray inductance represents the inductance in the connection points between the bus bar and the module, in addition to the stray inductance that was not included in the module simulation model. The inductance of the bus bar, however, seems to be very low. Thus, this inductance is represented by the inductor L_{stray1} .

The DUT turn-off switching characteristics at 600 V 120 A after the connection of the optimal DC snubber are presented in Figure 6.10. The switching characteristics for 30 A, 60 A and 90 A drain currents are given in Appendix D.3.

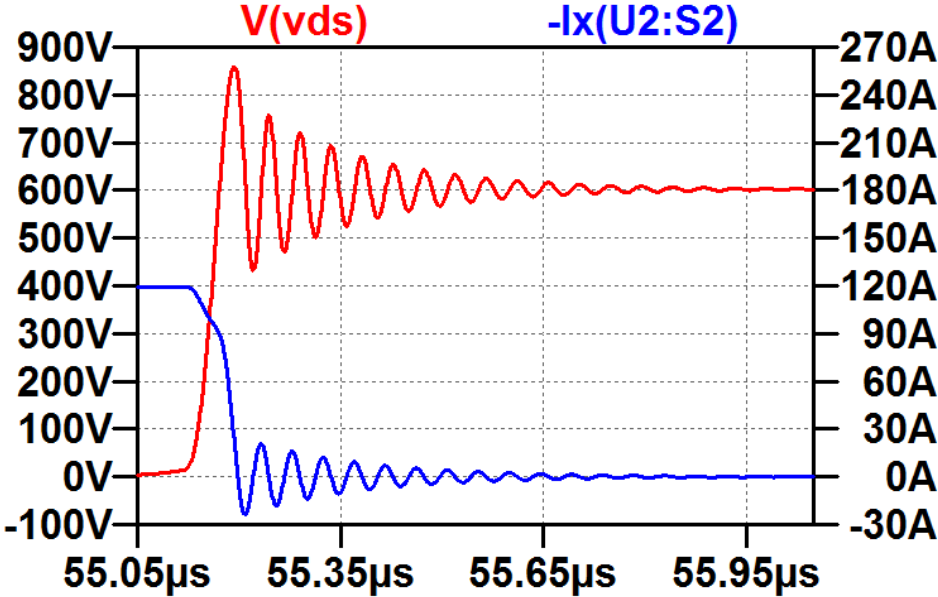


Figure 6.10: Simulation – Effect of DC snubber at 600 V 120 A turn off

The turn-off switching characteristics with DC snubber show improvement with significant reduction of the long-lasting ringing compared to without snubber, in Figure 6.3. The voltage overshoot during turn off, however, is close to unchanged. Similar improvement in ringing duration is found at DUT turn on. The turn-on switching characteristics at 30 A, 60 A, 90 A and 120 A drain currents with DC snubber are presented in Appendix D.4.

The fall times and rise times of current and voltage during switching are close to unaffected after the addition of DC snubber. It is also found that the losses in the DC snubber are negligible compared to the losses in the DUT. Thus, the implementation of a DC snubber improves the

switching transient significantly without influencing the switching times and the switching losses.

6.5.2 Turn-Off Snubber

In order to improve the DUT switching characteristics even further, a turn-off snubber is added to the simulation circuit. This is presented in Figure 6.11.

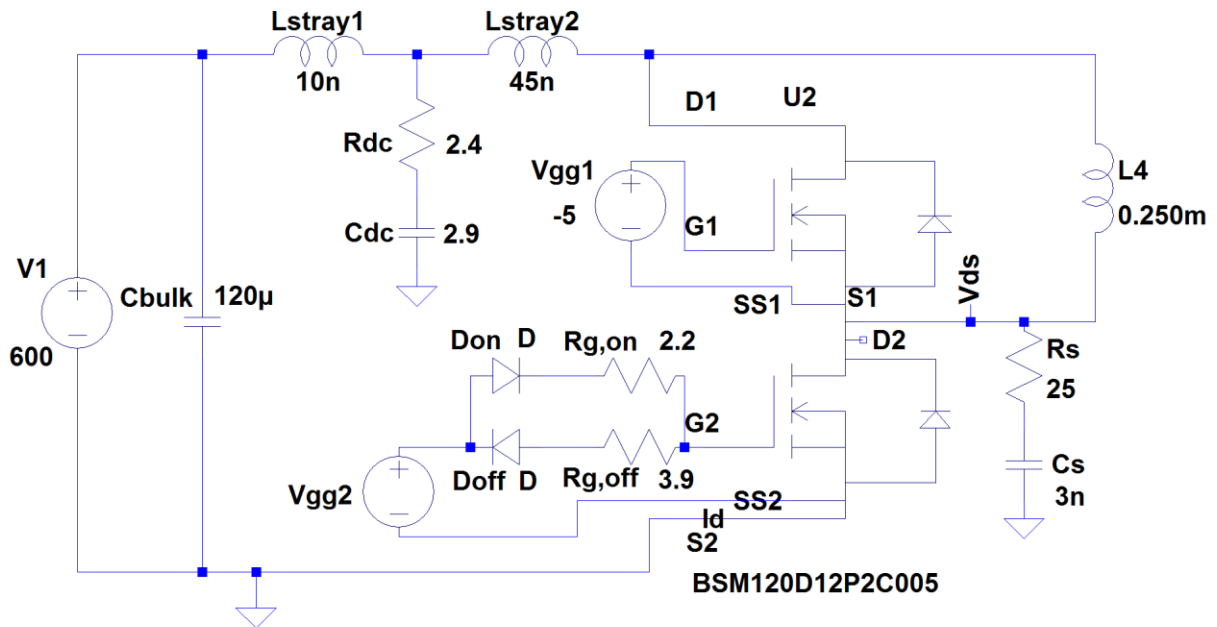


Figure 6.11: Simulation circuit including DC snubber and turn-off snubber

The turn-off snubber is depicted by the resistor R_s and the capacitor C_s . The values of these components were calculated in Section 5.6.2 to be $R_s = 25 \Omega$ and $C_s = 3 \text{ nF}$. Such a snubber design should help reduce the voltage overshoot during turn off, as well as reducing ringing even more. This was thoroughly discussed in Section 4.6. The DC snubber from the previous section is kept part of the simulation circuit, as it helped improve the switching transients.

6.5.2.1 Influence of Snubber Capacitor on Turn-Off Transient

The influence of the snubber capacitor on the turn-off transient is investigated by varying the snubber capacitance C_s and holding the snubber resistance R_s constant. Figure 6.12 presents the DUT turn-off transients at 600 V 120 A with two different snubber capacitors, and constant snubber resistance.

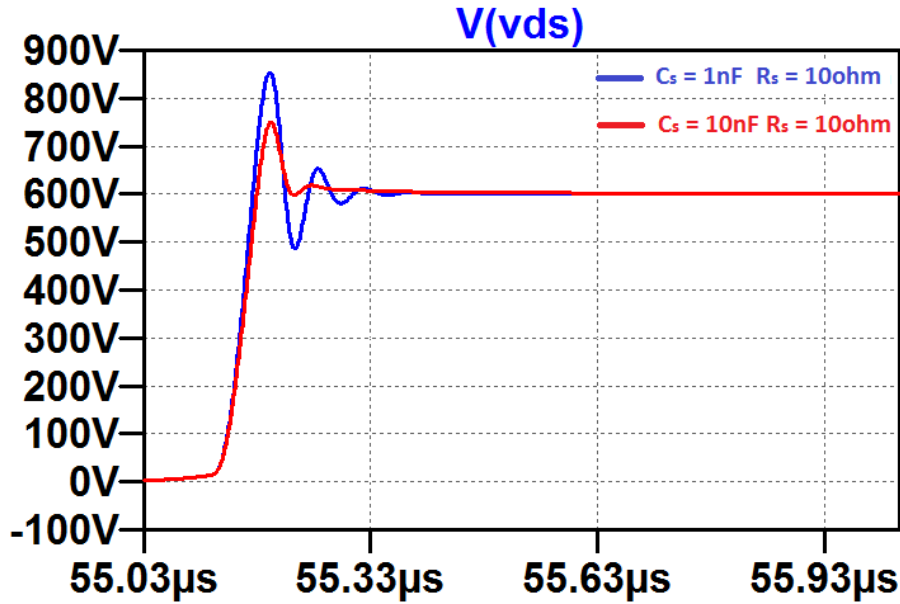


Figure 6.12: Simulation – Influence of snubber capacitor at 600 V 120 A turn off

It is clear that an increased capacitance gives higher damping if the resistance is held constant. This is because the voltage rise is limited and slowed down by the higher capacitance. In addition, this leads to lower voltage overshoot. However, slower turn-off switching leads to higher turn-off losses. The total switching losses with the two turn-off snubbers in Figure 6.12 are presented in Table 6.3. The switching losses in the DC snubber are negligible compared to the losses in the transistor and the turn-off snubber. Thus, the switching losses denoted as $E_{snub,on}$ and $E_{snub,off}$ are dissipated in the turn-off snubber. The parameters describing the switching losses after the addition of snubbers are explained below:

- $E_{snub,on}$ – Turn-on switching losses dissipated in the turn-off snubber
- $E_{snub,off}$ – Turn-off switching losses dissipated in the turn-off snubber
- $E_{trans,on}$ – Turn-on switching losses dissipated in the DUT
- $E_{trans,off}$ – Turn-off switching losses dissipated in the DUT
- $E_{tot,on} = E_{trans,on} + E_{snub,on}$ – Total turn-on switching losses
- $E_{tot,off} = E_{trans,off} + E_{snub,off}$ – Total turn-off switching losses
- $E_{tot} = E_{tot,on} + E_{tot,off}$ – Total switching losses

The same definition will hold for similar tables and figures in Chapter 6 and Chapter 7.

Table 6.3: Simulation – Influence of snubber capacitor on switching losses with $R_s = 10 \Omega$

| C_s [nF] | Turn on | | | Turn off | | |
|------------|---------------------|--------------------|-------------------|----------------------|---------------------|--------------------|
| | $E_{trans,on}$ [mJ] | $E_{snub,on}$ [mJ] | $E_{tot,on}$ [mJ] | $E_{trans,off}$ [mJ] | $E_{snub,off}$ [mJ] | $E_{tot,off}$ [mJ] |
| 1 | 2.26 | 0.034 | 2.29 | 1.91 | 0.13 | 2.04 |
| 10 | 2.95 | 1.19 | 4.14 | 1.38 | 1.68 | 3.16 |

It is clear from Table 6.3 that the total switching losses increase with the snubber capacitance at both turn on and turn off. However, the turn-off losses $E_{trans,off}$ dissipated in the DUT decrease when the snubber capacitance increases. This happens because when the snubber capacitance increases, the turn-off transient approaches zero-voltage switching. This phenomenon was explained in Section 3.5.3. Even though the turn-off losses in the DUT are reduced, the switching losses in the turn-off snubber increase significantly. This leads to a significant increase in total switching losses at both turn on and turn off. Thus, the capacitance of the turn-off snubber should be limited.

6.5.2.2 Influence of Snubber Resistor on Turn-Off Transient

In the same manner, the influence of the snubber resistor is analyzed. Thus, C_s is held constant, while R_s is varied. The influence of R_s at 600 V 120 A turn off is presented in Figure 6.13.

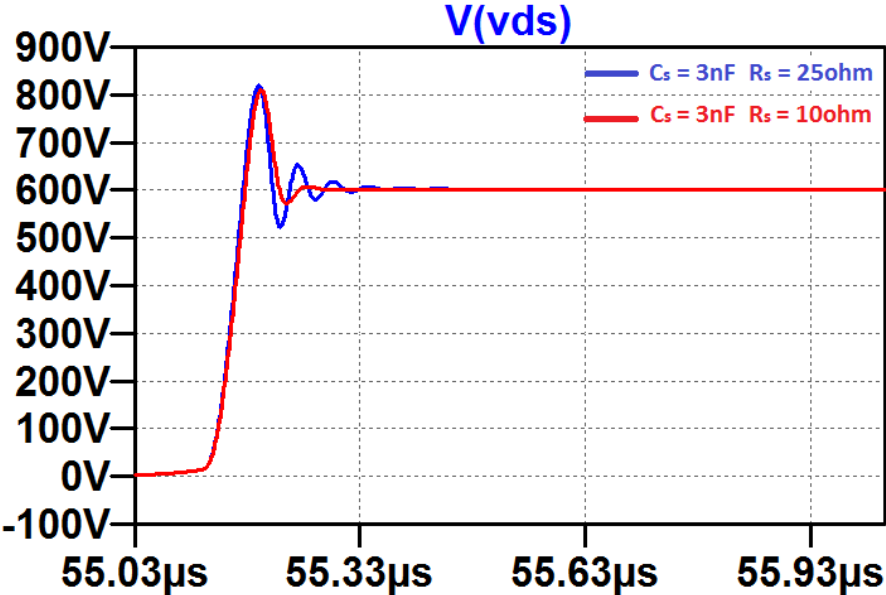


Figure 6.13: Simulation – Influence of snubber resistor at 600 V 120 A turn off

If the snubber resistance is reduced, the damping increases if the snubber capacitance is held constant. In (4.12), it was shown that a reduction in resistance leads to higher damping in a parallel RLC circuit. Thus, the theory is consistent with the simulation results. The influence of the snubber resistor on the total switching losses are presented in Table 6.4. The definition of the switching loss parameters was given in Section 6.5.2.1.

Table 6.4: Simulation – Influence of snubber resistor on switching losses with $C_s = 3 \text{ nF}$

| R_s [Ω] | Turn on | | | Turn off | | |
|--------------------|---------------------|--------------------|-------------------|----------------------|---------------------|--------------------|
| | $E_{trans,on}$ [mJ] | $E_{snub,on}$ [mJ] | $E_{tot,on}$ [mJ] | $E_{trans,off}$ [mJ] | $E_{snub,off}$ [mJ] | $E_{tot,off}$ [mJ] |
| 10 | 2.54 | 0.21 | 2.75 | 1.58 | 0.48 | 2.06 |
| 25 | 2.39 | 0.34 | 2.73 | 1.83 | 0.53 | 2.36 |

The total switching losses in Table 6.4 are not much affected by the snubber resistance. The biggest difference is seen in the DUT at turn off. The DUT turn-off losses $E_{trans,off}$ decrease when the snubber resistance decreases. Thus, in the comparison in Table 6.4 and Figure 6.13, a smaller snubber resistor has the advantage of improving the switching transients in addition to reducing the total switching losses. Thus, it is in this section found that the optimal turn-off snubber is $C_s = 3\text{ nF}$ and $R_s = 10\ \Omega$. However, in the rest of this chapter the turn-off snubber will be as calculated in Section 5.6.2 and depicted in Figure 6.11. Thus, all results are obtained with $C_s = 3\text{ nF}$ and $R_s = 25\ \Omega$.

6.5.2.3 Turn-Off Switching Characteristics with $C_s = 3\text{ nF}$ and $R_s = 25\ \Omega$

The DUT turn-off switching characteristics at 600 V 120 A after the addition of the turn-off snubber found in Section 5.6.2 ($C_s = 3\text{ nF}$ and $R_s = 25\ \Omega$) are presented in Figure 6.14. Turn-off switching characteristics for 30 A, 60 A and 90 A drain currents are attached in Appendix D.5.

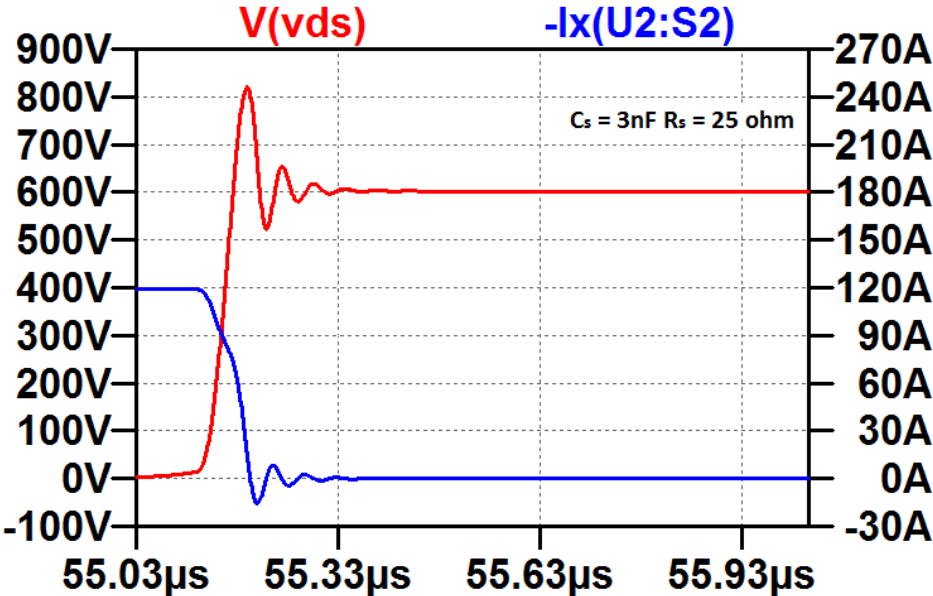


Figure 6.14: Simulation – Effect of turn-off snubber at 600 V 120 A turn off

The addition of a turn-off snubber reduces the voltage overshoot and the ringing duration significantly, when comparing with Figure 6.3. The turn-off snubber influences the switching transients by increasing the switching times. In order to investigate this influence, the DUT turn-off switching times, voltage derivative and voltage overshoot are presented in Table 6.5.

Table 6.5: Simulation – Turn-off switching characteristics with snubbers

| I_d [A] | Turn off | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{rv} [ns] | t_f [ns] | dv/dt [V/ns] | V_{os} [V] |
| 30 | 67 | 86 | 7.16 | 25 |
| 60 | 43 | 60 | 11.2 | 92 |
| 90 | 38 | 56 | 12.6 | 163 |
| 120 | 35 | 54 | 13.7 | 220 |

When comparing these results with what was presented in Table 6.1, it is clear that the turn-off transient gets slower due to the addition of snubbers. However, the increase in switching time is only marginal. The voltage overshoot is reduced significantly, leading to lower switching stresses on the DUT.

6.5.2.4 Turn-On Switching Characteristics with $C_s = 3\text{ nF}$ and $R_s = 25\ \Omega$

The DUT turn-on switching characteristics at 600 V 120 A after the addition of the turn-off snubber are presented in Figure 6.15. The turn-on switching characteristics for 30 A, 60 A and 90 A drain currents are presented in Appendix D.6.

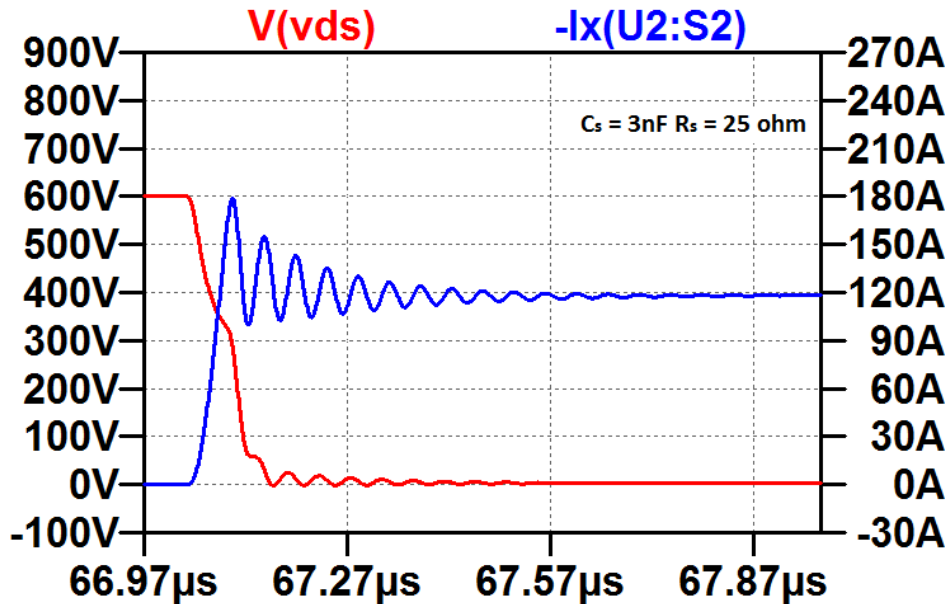


Figure 6.15: Simulation – Effect of turn-off snubber at 600 V 120 A turn on

When comparing these results with the turn-on switching characteristics without snubber in Figure 6.4, it is found that the turn-on switching characteristics are improved significantly. In particular, the ringing duration is reduced. The DUT turn-on switching times, current derivative and current overshoot with snubbers are presented in Table 6.6.

Table 6.6: Simulation – Turn-on switching characteristics with snubbers

| I_d [A] | Turn on | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{fv} [ns] | t_r [ns] | di/dt [A/ns] | I_{os} [A] |
| 30 | 51 | 14 | 1.71 | 56 |
| 60 | 59 | 20 | 2.40 | 58 |
| 90 | 67 | 25 | 2.88 | 59 |
| 120 | 78 | 30 | 3.20 | 59 |

The current overshoot increases due to the addition of a turn-off snubber, compared to what was presented in Table 6.2. In addition, the switching times increase marginally.

6.5.3 Switching Characteristics Improvement

The improvements of the DUT switching transients due to the addition of DC snubber can be investigated by plotting the switching transients with and without DC snubber in the same diagram. This is done for the DUT turn-off voltage transient at 600 V 120 A in Figure 6.16.

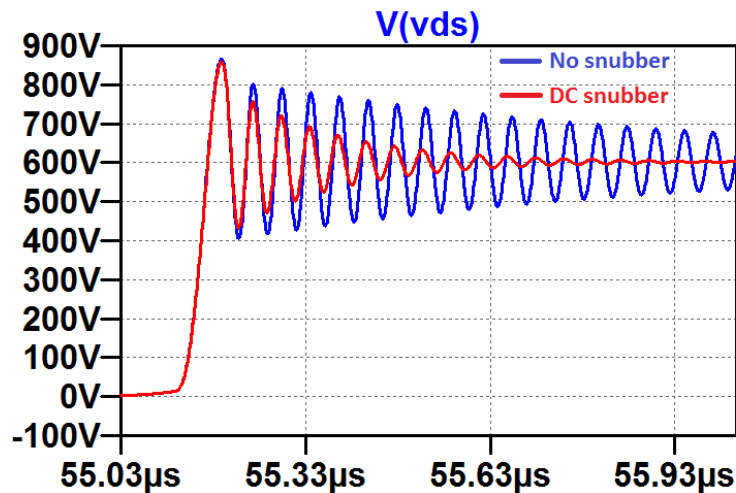


Figure 6.16: Simulation – Turn-off voltage improvement after addition of DC snubber

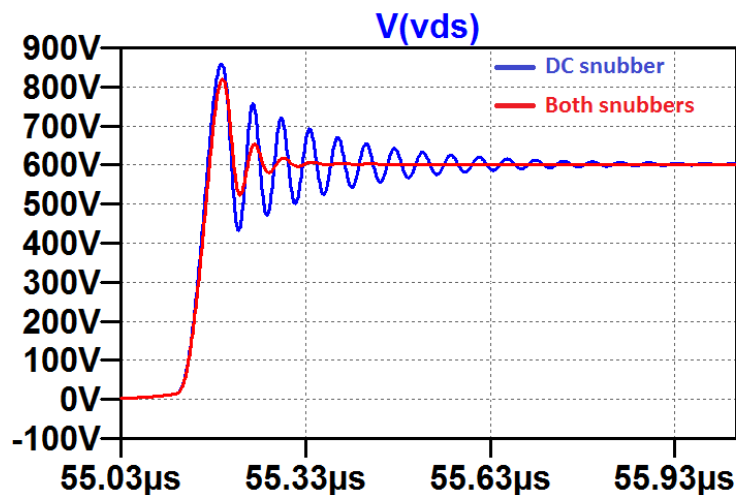


Figure 6.17: Simulation – Turn-off voltage improvement after addition of both snubbers

The improvements due to the addition of both DC snubber and turn-off snubber can be found in the same way. This is done for the DUT turn-off transient at 600 V 120 A in Figure 6.17.

It is shown through simulation that the addition of a DC snubber and a turn-off snubber improves the turn-off voltage waveform significantly. In particular, the long-lasting ringing is removed from the turn-off transient of the DUT. In addition, the voltage overshoot is reduced.

The same comparison can be conducted for the current transient for a DUT turn on at 600 V 120 A. This is presented in Figure 6.18 and Figure 6.19.

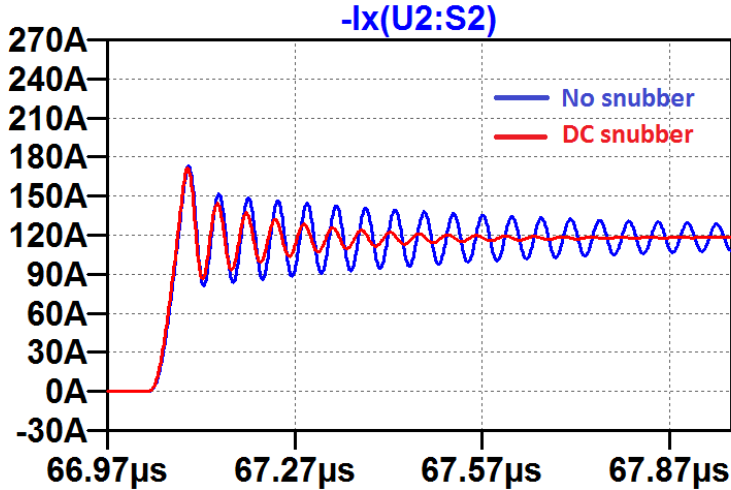


Figure 6.18: Simulation – Turn-on current improvement after addition of DC snubber

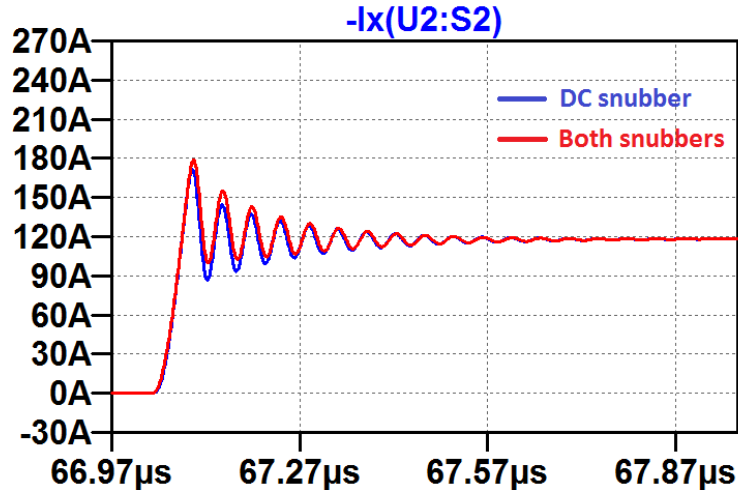


Figure 6.19: Simulation – Turn-on current waveform after addition of both snubbers

It is clear from Figure 6.18 that the DC snubber has a good influence on the DUT turn on, as it reduces the ringing duration. The turn-off snubber, however, influences the turn on in a bad manner. It can be seen from Figure 6.19 that the addition of a turn-off snubber increases the current overshoot, which also increases the turn-on switching losses. This is due to discharge of the turn-off snubber capacitor during turn on. However, the increase is only marginal.

6.5.4 Switching Times with Snubbers

The addition of snubber circuits changes the structure of the simulation circuit. Thus, changes in switching time are experienced. Figure 6.20 presents the switching times from Table 6.5 and Table 6.6 as a function of drain current after the addition of snubbers.

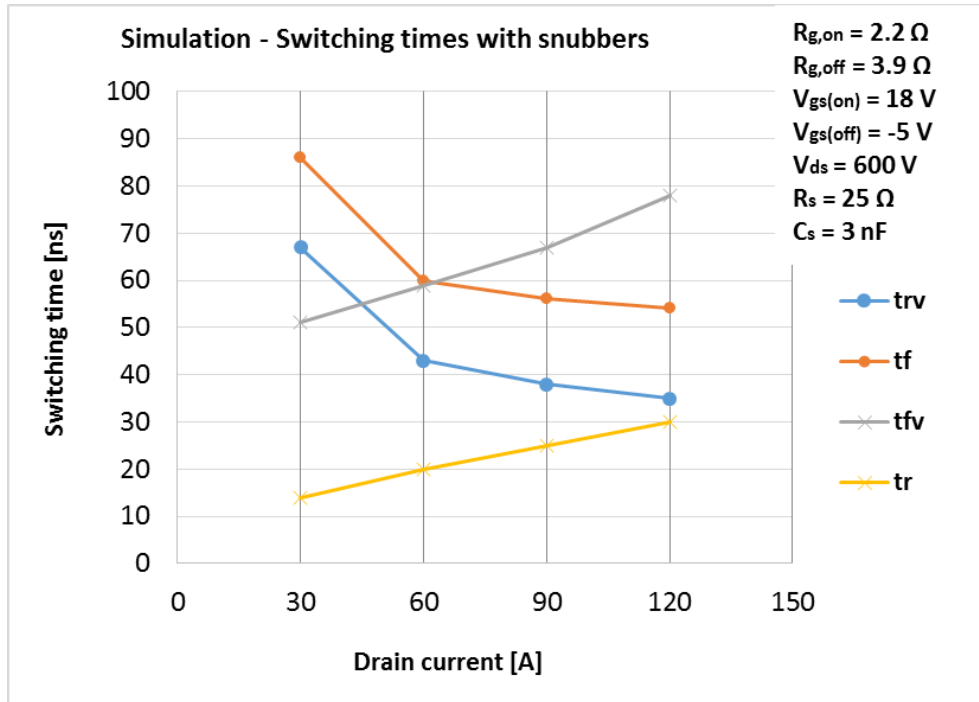


Figure 6.20: Simulation – Switching times as a function of drain current with snubbers

When comparing Figure 6.20 with Figure 6.5, it is clear that the switching times only increase marginally due to the addition of snubbers. Thus, it seems in simulation as the snubbers can influence the switching characteristics in a very positive way, without influencing the switching times significantly.

6.5.5 Switching Losses with Snubbers

The addition of snubber circuits changes the DUT switching characteristics, and this change will therefore influence the switching losses. The DUT switching losses are calculated by using the method described in Section 3.6. In addition, the switching snubber losses are calculated by integrating the resistive power losses in the turn-off snubber during switching. This was explained in Section 4.7.5. The total losses as a function of drain current are presented in Figure 6.21, including information on where in the simulation circuit the losses are dissipated. The definition of these parameters was presented in Section 6.5.2.1.

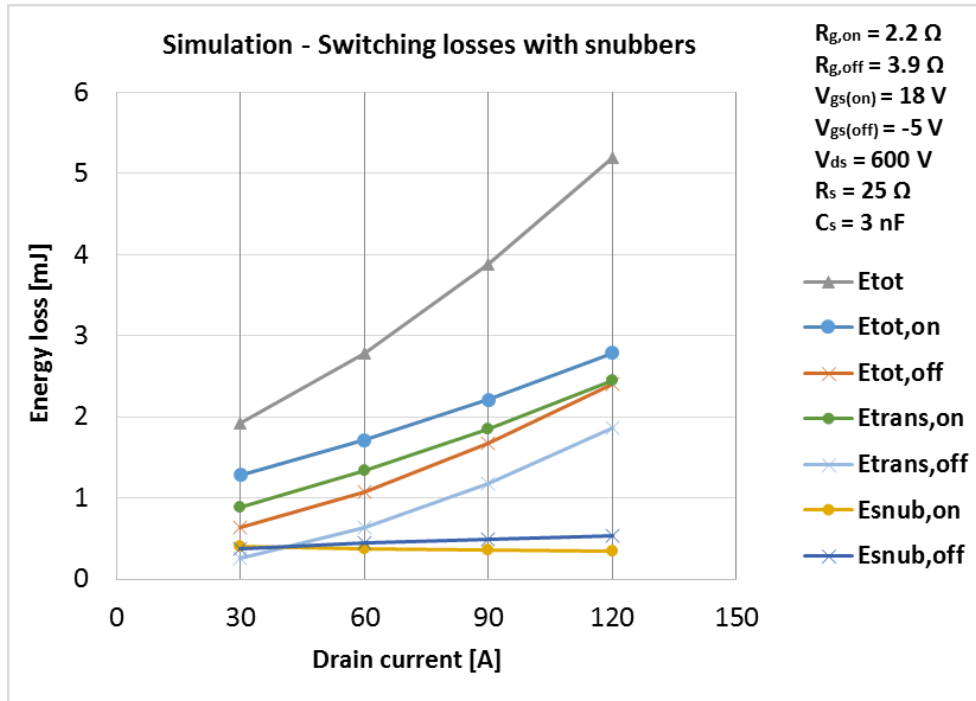


Figure 6.21: Simulation – Switching losses as a function of drain current with snubbers

The snubber switching losses are low compared to the transistor snubber losses, especially for increased drain currents. When comparing the results in Figure 6.21 with what was presented in Figure 6.6, it is found that the total switching losses only increase marginally due to the addition of snubbers. The switching characteristics, however, have improved significantly because of the snubbers. The switching losses in Figure 6.21 are lower than what was presented in the SiC module datasheet [38], even after the addition of snubbers. In order to verify the accuracy of the simulation results, the same kind of test will be conducted in the experimental part.

7. Laboratory Experiments and Discussion

7.1 Introduction

This chapter presents an analysis of the most important results from the laboratory experiments, including a thorough discussion on parameters that can have great influence on the switching characteristics of the DUT. The accuracy of the LTspice simulations in the previous chapter will be tested.

Firstly, the influence of the current and voltage measuring instruments on the switching characteristics will be investigated. Secondly, the influence of the external gate resistance in the gate driver will be discussed. Thirdly, the implementation and the effect of the short circuit protection (SCP) in the gate driver will be studied. Then, the switching characteristics and switching losses of the DUT will be analyzed. Finally, the impact of adding suitable snubber circuits to the laboratory setup will be explained and analyzed. The influence of snubber circuits on switching characteristics and switching losses will be investigated with the same structure as in Chapter 6. This winds up in a comparison of results obtained in simulation and experiment, compared to the values given in the SiC module datasheet.

The switching characteristics will be obtained by the use of double-pulse tests at different test conditions. This gives the basis for investigating the switching transients in laboratory experiments, as explained in Section 3.4. Figure 7.1 presents a picture of the laboratory setup, showing an ongoing double-pulse test on the oscilloscope (waveforms in Appendix E).

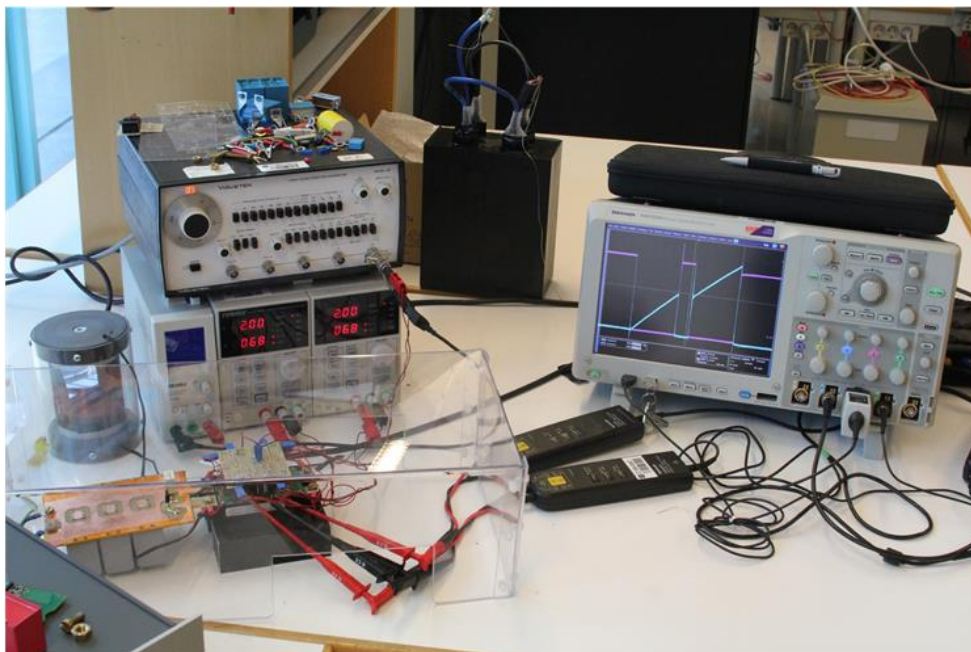


Figure 7.1: Picture of the laboratory setup

7.2 Influence of Measuring Instruments on Switching Characteristics

When conducting tests on hard-switching devices with fast switching transients, accurate measurements rely on using suitable measuring instruments. The measuring instruments can influence the measurements in different ways. E.g., the connection of voltage probes can change the conditions of the test circuit by adding parasitic inductance or capacitance to the circuit, which can reduce the accuracy of the measurements considerably. The bandwidth of the measuring instrument is another important aspect when choosing the most suitable ones. This was explained in Section 5.2. As the switching transients are fast with high-frequency ringing, it is important to determine whether the bandwidth limits the accuracy of the measurement.

7.2.1 Voltage Measurement

Firstly, the influence of the voltage probes is investigated. This is done by measuring the drain-to-source voltage of the DUT with two different voltage probes simultaneously. The first voltage probe, the P5200A differential high-voltage probe from Tektronix, has a bandwidth of 50 MHz. The second probe, the THDP0200 differential high-voltage probe from Tektronix, has a higher bandwidth of 200 MHz. By measuring the drain-to-source voltage with both probes simultaneously, these two voltage probes can be compared through a 90 A 600 V double-pulse test. The voltage waveforms at DUT turn off are presented in Figure 7.2. MATLAB is used in order to filter and plot the waveforms from the oscilloscope in a transparent manner. The script that was used in Figure 7.2 is presented in Appendix F.

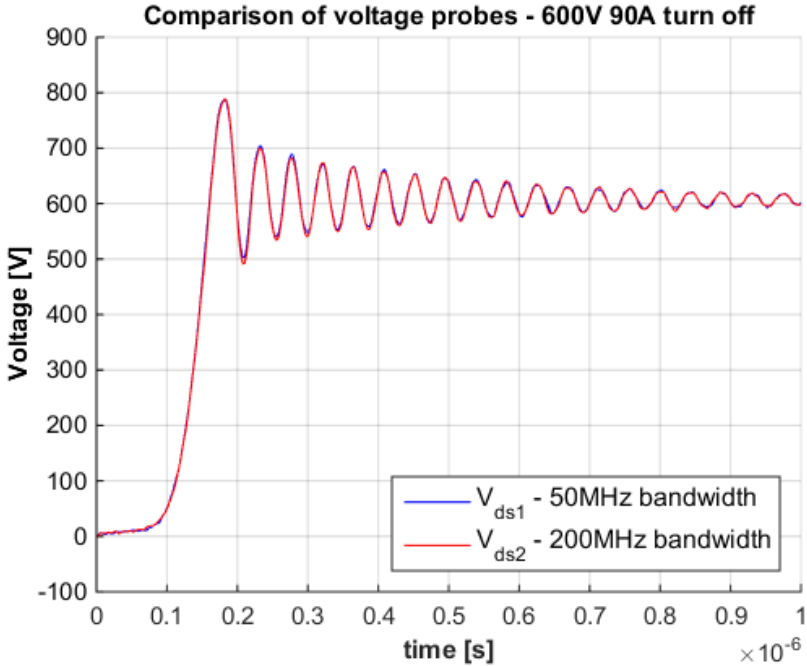


Figure 7.2: Voltage probe comparison – DUT turn off at 600 V 90 A

V_{ds1} is the drain-to-source voltage measured with the 50 MHz probe, while V_{ds2} is measured with the 200 MHz probe. The voltage measurements with the two voltage probes are very similar at DUT turn off, thus both measurements should be accurate. The same kind of comparison is done at DUT turn on. This is presented in Figure 7.3.

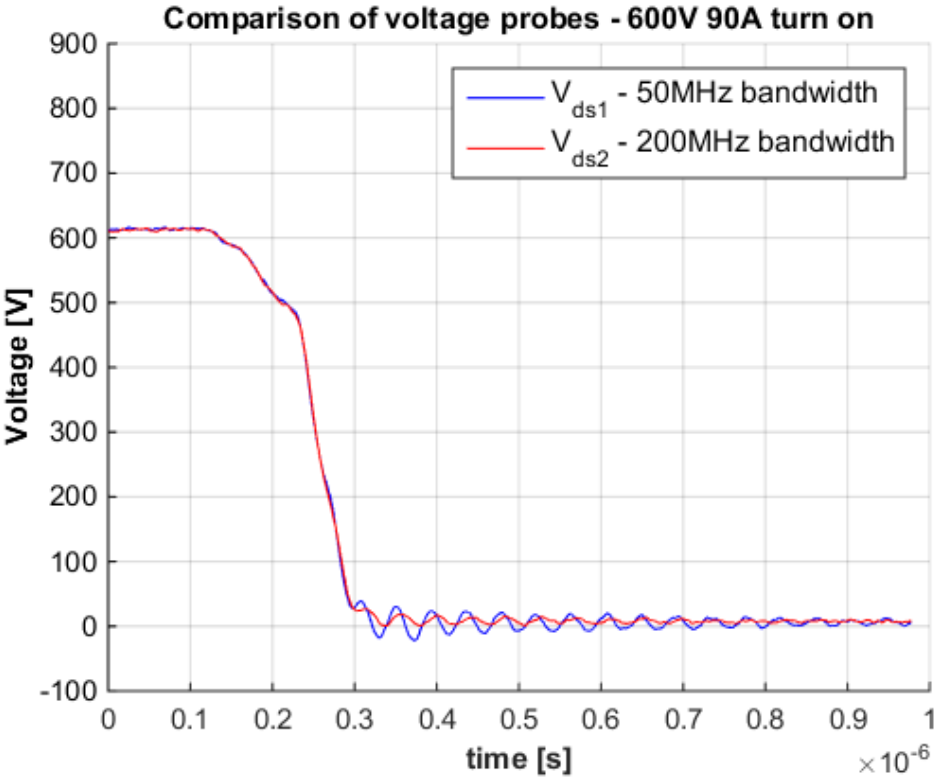


Figure 7.3: Voltage probe comparison – DUT turn on at 600 V 90 A

At DUT turn on, the difference is more significant. The 50 MHz voltage probe introduces a turn on with more ringing than the 200 MHz voltage probe. This is probably caused by higher inductance in the 50 MHz voltage probe. Thus, the 200 MHz probe should be the most accurate. However, the voltage fall time is similar with both probes. In the continuation, drain-to-source voltage measurements will be conducted with the 200 MHz voltage probe, and gate-to-source voltage measurements will be conducted with the 50 MHz voltage probe.

7.2.2 Current Measurement

In this section, the influence of the current measuring instruments on current measurements is investigated. The current measurement during fast transients relies on having the right measuring instrument. If high-frequency ringing occurs, the current measuring instrument should have higher bandwidth than this frequency in order to obtain accurate results. If not, this high-frequency ringing will be attenuated and the switching characteristics will be somewhat

inaccurate. This is illustrated in Figure 7.4, which is a comparison of drain current measurement with two different measuring instruments for a DUT turn on at 600 V 90 A.

I_{d1} is the drain current measured with a CWT Mini 6B Rogowski coil, which has a bandwidth of 20 MHz. I_{d2} is the drain current measured with an SSDN series shunt from T&M Research Products, with a bandwidth of 400 MHz. The placement of these current measuring instruments in the laboratory circuit was explained in Section 5.2.2.

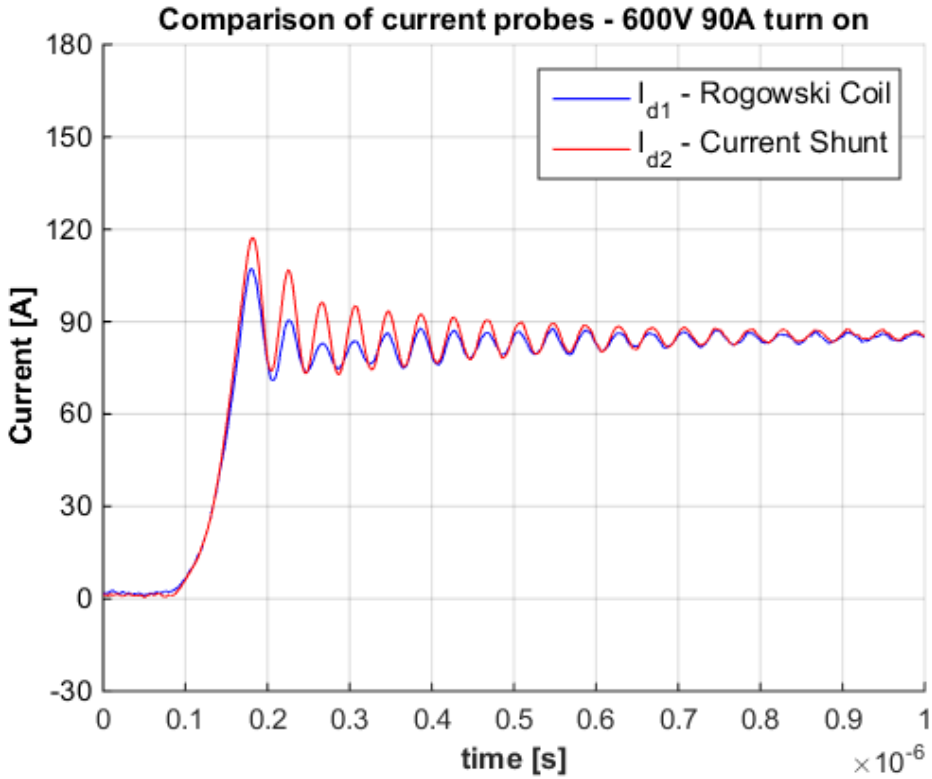


Figure 7.4: Current measurement comparison – DUT turn on at 600 V 90 A

The shunt measurement gives a little higher current overshoot during DUT turn on as well as ringing with higher amplitude than with the Rogowski coil. Thus, it is probable that the current measurement in the Rogowski coil is attenuated due to lower bandwidth. The high-frequency ringing has a frequency of approximately 24 MHz, which is higher than the bandwidth of the Rogowski coil. The same phenomenon is depicted in Figure 7.5, which is the DUT turn off at 600 V 90 A.

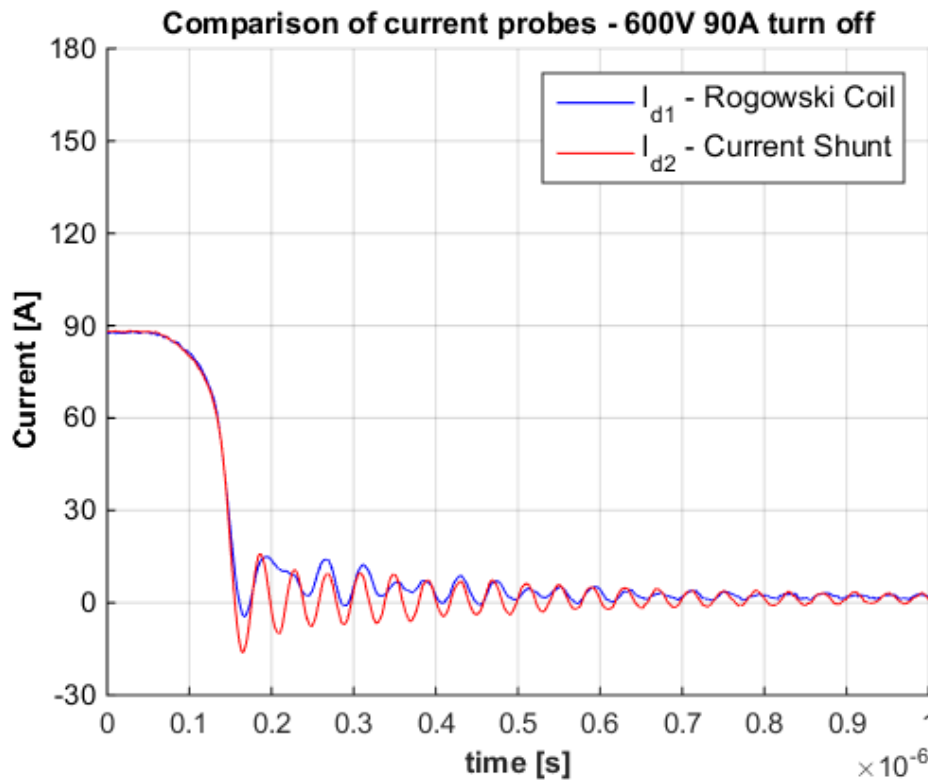


Figure 7.5: Current measurement comparison – DUT turn off at 600 V 90 A

Once more, the shunt measurement has higher oscillation amplitude. Even though the current shunt gives the most accurate current measurement, from this point onwards current will be measured with the Rogowski coil. This current measuring method is chosen because it is much more practical in laboratory experiments than using the current shunt. In addition, as can be seen in Figure 7.4 and Figure 7.5, the current rise time and fall time are not influenced considerably by using the Rogowski coil. Thus, the switching time measurements should be close to accurate.

7.3 Influence of Gate Resistor on Switching Characteristics

The gate resistance in the gate driver influences the switching time of a MOSFET. A lower gate resistance leads to higher charging current flowing to and from the gate terminal of the MOSFET. This means that the rise time and fall time of the gate-to-source voltage decrease. This again leads to faster MOSFET turn-off and turn-on switching transients. However, even though faster switching gives many advantages, this also leads to higher switching stresses on the switching device. Thus, a tradeoff must be made. In order to investigate the influence of the gate resistance on the switching characteristics of the DUT, double-pulse tests (DPT) with different external gate resistors are conducted. As explained in Section 5.1.2, the gate drivers

have two different gate resistors for turn off and turn on, denoted as $R_{g,off}$ and $R_{g,on}$ respectively.

7.3.1 Influence of Turn-Off Gate Resistor

Firstly, the influence of the turn-off gate resistance is analyzed. One DPT is conducted with the original external gate resistance $R_{g,off} = 3.9 \Omega$, while the other DPT is conducted with $R_{g,off} = 7.8 \Omega$. The turn-off switching characteristics at 600 V 120 A with different external gate resistors are presented in Figure 7.6.

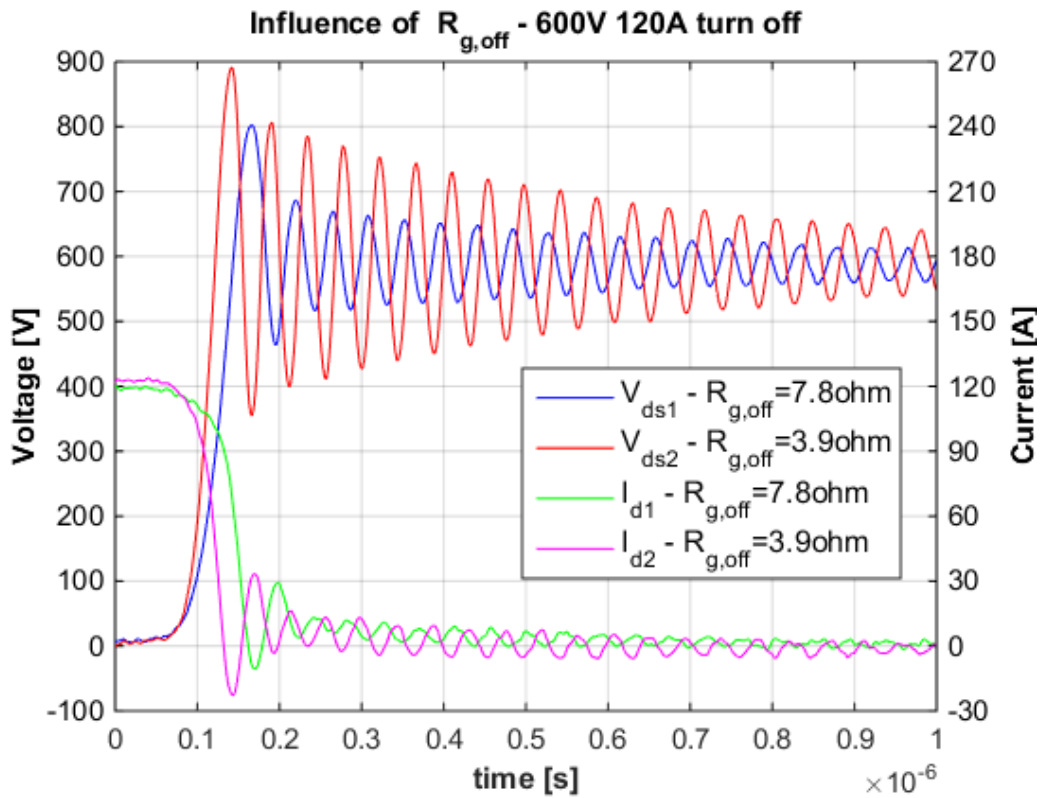


Figure 7.6: Influence of turn-off gate resistance – Switching characteristics

As can be seen in Figure 7.6, using a smaller external gate resistor results in much faster switching. The switching times are significantly reduced with $R_{g,off} = 3.9 \Omega$. However, even though faster switching leads to lower switching losses, it is clear that the switching stresses on the DUT increase considerably. The voltage overshoot and ringing is much more significant with $R_{g,off} = 3.9 \Omega$. The current ringing also increases when the switching time goes down.

In the same manner, Figure 7.7 presents the influence of the turn-off gate resistance on the gate-to-source voltage V_{gs} at 600 V drain-to-source voltage and 120 A drain current.

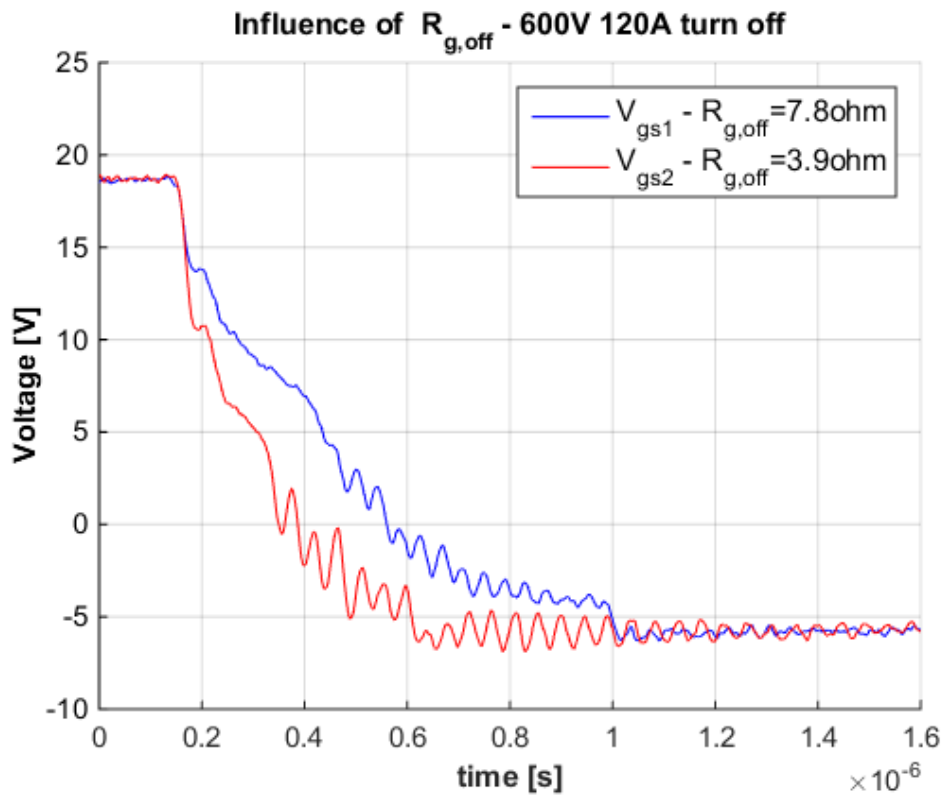


Figure 7.7: Turn-off gate resistance comparison – Gate-to-source voltage

It is clear that the gate resistance influences the fall time of the gate-to-source voltage during turn off significantly. This is why the switching times in Figure 7.6 are reduced. This was explained in Section 4.6.1. It is interesting to notice that the Miller plateau, which was explained in Figure 2.14, is not very clear in the waveform due to the oscillations.

The instantaneous power dissipation in the DUT during the turn-off transient at 600 V 120 A is presented with different gate resistance in Figure 7.8. The power dissipation is simply found by multiplying the DUT drain-to-source voltage with the drain current, as explained in Figure 3.17.

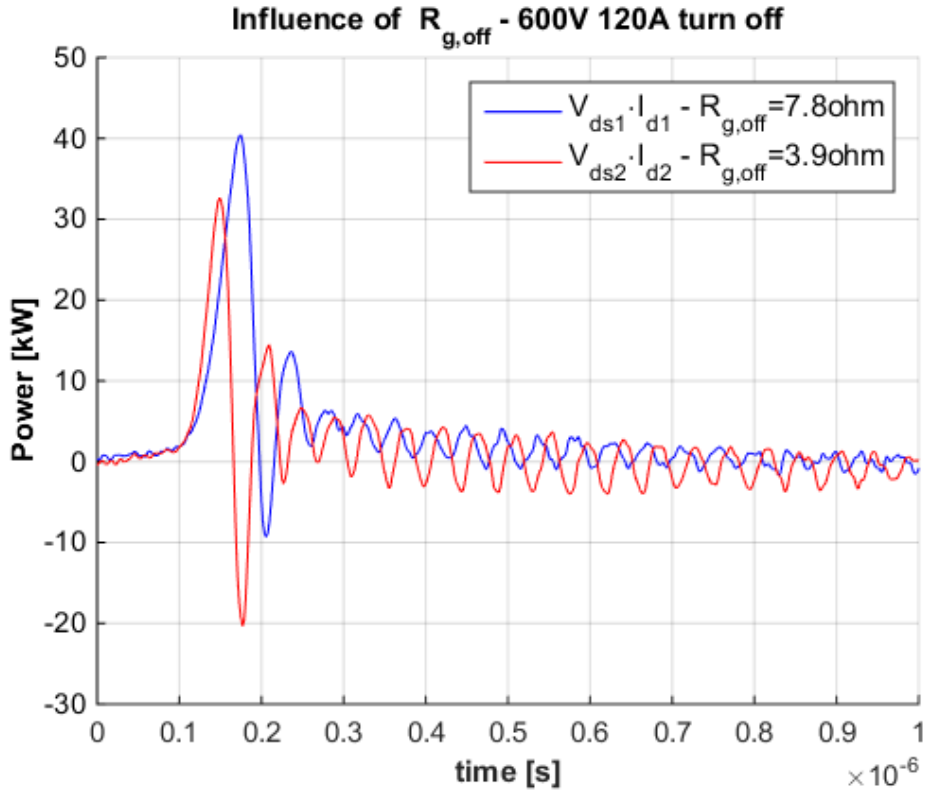


Figure 7.8: Influence of turn-off gate resistance – Power dissipation

This shows that $R_{g,off} = 3.9 \Omega$ gives lower power dissipation, but the ringing increases significantly. The turn-off switching losses and switching times at 600 V 120 A with different turn-off gate resistance are presented in Table 7.1. E_{off} is found by integrating the waveforms in Figure 7.8, as explained in Section 3.6.

Table 7.1: Experiment – Switching times and losses with different turn-off gate resistance

| $R_{g,off} [\Omega]$ | $t_{d(off)} [ns]$ | $t_f [ns]$ | $t_{off} [ns]$ | $t_{rv} [ns]$ | $E_{off} [mJ]$ |
|----------------------|-------------------|------------|----------------|---------------|----------------|
| 3.9 | 115 | 34 | 149 | 39 | 0.97 |
| 7.8 | 205 | 52 | 256 | 52 | 1.80 |

It is clear that the turn-off gate resistance has a big influence on turn-off switching time t_{off} and turn-off switching loss E_{off} . If $R_{g,off}$ is doubled, t_{off} increases by 72 % and E_{off} increases by 86 %. Thus, in order to minimize the turn-off switching losses, the turn-off gate resistance should be held as low as possible without causing dangerous switching stresses.

7.3.2 Influence of Turn-On Gate Resistor

The same kind of comparison as in the previous section is conducted in order to investigate the influence of the turn-on gate resistance. The first DPT is conducted with turn-on gate resistance of $R_{g,on} = 4.4 \Omega$, while the second DPT is conducted with the original turn-on gate resistance

of $R_{g,on} = 2.2 \Omega$. The turn-on switching characteristics at 600 V 120 A are presented in Figure 7.9.

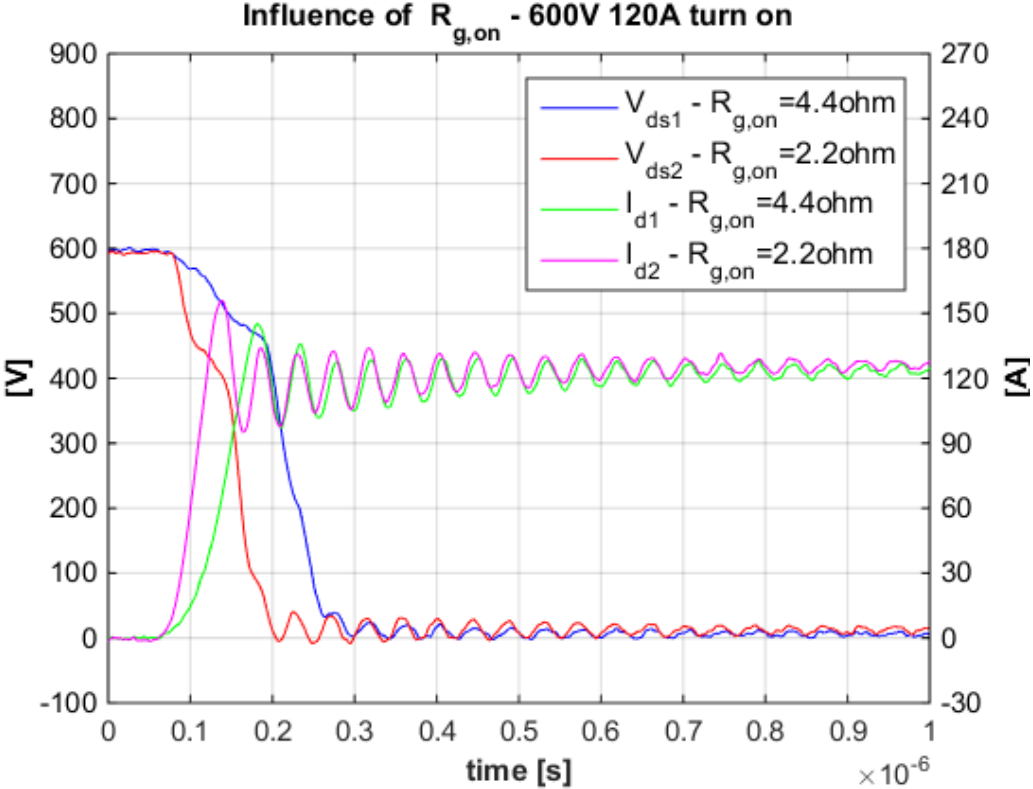


Figure 7.9: Influence of turn-on gate resistance – Switching characteristics

The switching times during turn on are reduced significantly due to the reduction in turn-on gate resistance. This leads to a marginal increase in ringing amplitude in the current and voltage waveforms. The current overshoot increases for lower turn-on gate resistance.

A comparison of gate-to-source voltage V_{gs} at DUT turn on with different gate resistance is given in Figure 7.10.

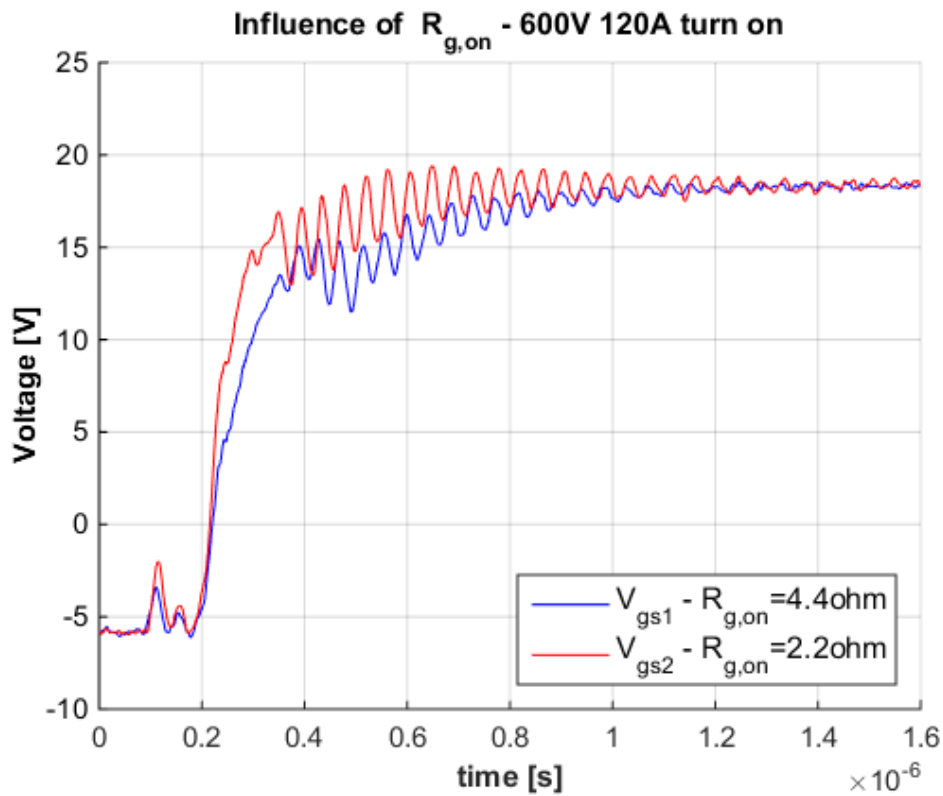


Figure 7.10: Turn-on gate resistance comparison – Gate-to-source voltage

The faster switching transients in Figure 7.9 are a consequence of the faster gate-to-source voltage rise time in Figure 7.10. The Miller plateau, which was explained Figure 2.13, is found at a high voltage of approximately 15 V. As explained in Section 2.3.3.1, the voltage at which the Miller plateau is found increases with drain current. However, the Miller plateau is not easily noticeable due to an oscillating waveform.

The instantaneous power dissipation during DUT turn on at 600 V 120 A is presented with different turn-on gate resistance in Figure 7.11.

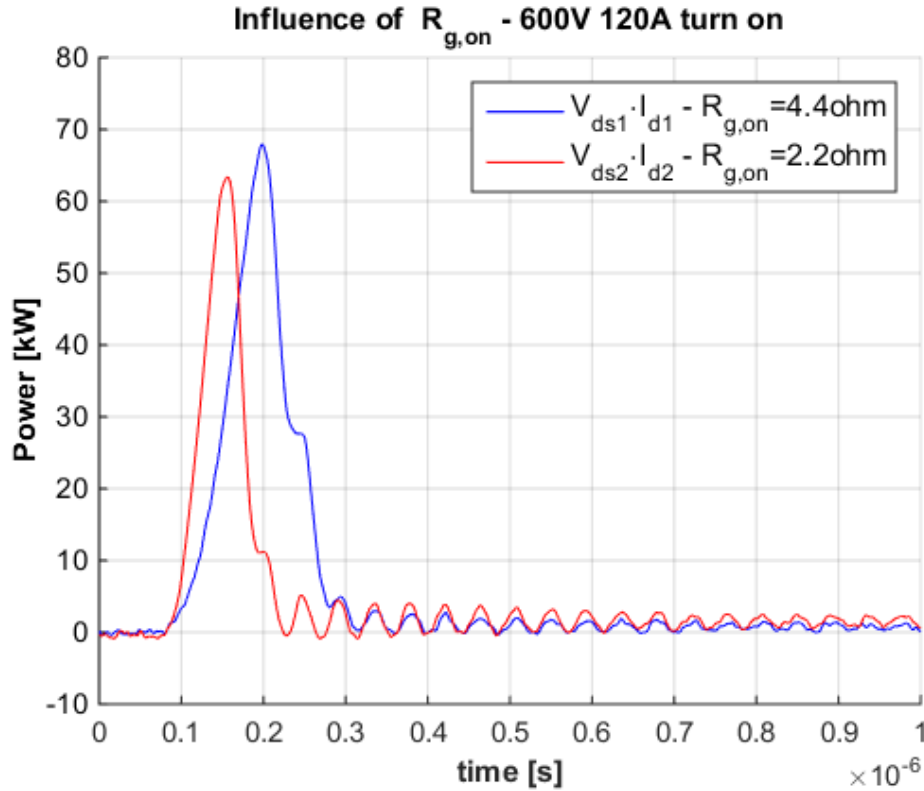


Figure 7.11: Turn-on gate resistance comparison – Power dissipation

It is clear that a lower turn-on gate resistance $R_{g,on}$ leads to lower DUT power dissipation at turn on. The turn-on switching losses and switching times at 600 V 120 A with different turn-on gate resistance are given in Table 7.2. E_{on} is found by integrating the waveforms in Figure 7.11, as explained in Section 3.6.

Table 7.2: Experiment – Switching times and losses with different turn-on gate resistance

| $R_{g,on}$ [Ω] | $t_{d(on)}$ [ns] | t_r [ns] | t_{on} [ns] | t_{fv} [ns] | E_{on} [mJ] |
|-------------------------|------------------|------------|---------------|---------------|---------------|
| 2.2 | 41 | 39 | 80 | 99 | 3.41 |
| 4.4 | 66 | 65 | 131 | 126 | 5.49 |

It is found that if $R_{g,on}$ is doubled, t_{on} increases by 64 % and E_{on} increases by 61 %. Thus, in order for the turn-on switching losses to be minimized, the turn-on gate resistance should be as low as possible without causing dangerous switching stresses.

7.4 Experimental Test of Short-Circuit Protection

The performance of the short-circuit protection (SCP) system described in Section 5.1.3 will be tested in this section. Modifications to the setup presented in Figure 5.6 will be carried out in order to obtain the desired behavior. Note that the test of the SCP is conducted with a turn-off gate resistance of $R_{g,off} = 7.8 \Omega$.

The first test of the SCP is a single-pulse test at 400 V drain-to-source voltage. This is conducted with $R_1 = 15 \text{ k}\Omega$, $R_2 = 22 \text{ k}\Omega$, $R_3 = 6.8 \text{ k}\Omega$ and $C_{blank} = 0.1 \mu\text{F}$. This should theoretically give activation of the SCP at the following drain-to-source voltage (5.2):

$$V_{ds,SCP} = 0.74 \text{ V} \cdot \frac{6.8 \text{ k}\Omega + 22 \text{ k}\Omega}{6.8 \text{ k}\Omega} - 1.7 \text{ V} = 1.43 \text{ V} \quad (7.1)$$

A drain-to-source voltage of $V_{ds,SCP} = 1.43 \text{ V}$ corresponds to an activation of the SCP at a drain current of $I_{d,SCP} = 71.7 \text{ A}$, which is much lower than the drain current rating of the DUT. The 400 V single-pulse test of the SCP is given in Figure 7.12.

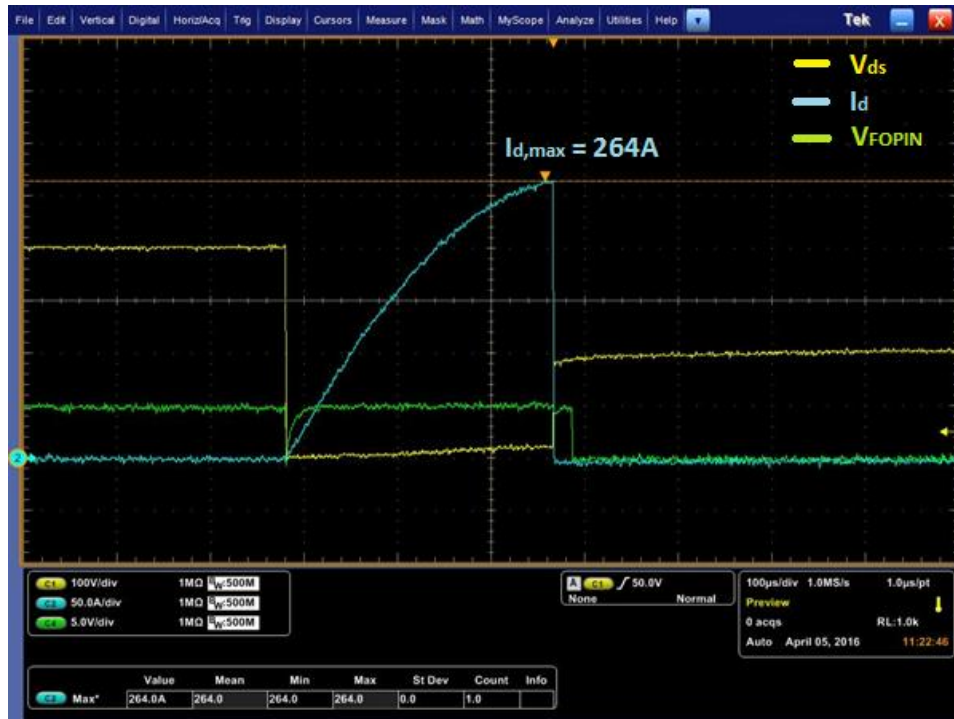


Figure 7.12: 400 V single-pulse SCP test

In Figure 7.12, the yellow waveform is the drain-to-source voltage V_{ds} , the blue waveform is the drain current I_d and the green waveform is the signal from the Fault Output Pin of BW9499H V_{FOPIN} . As long as everything works as normal, the Fault Output Pin outputs 5 V. If there is an SCP fault, however, the Fault Output Pin is pulled down to 0 V. In Figure 7.12, the SCP intervenes and turns off the DUT at 264 A drain current. This is a much higher drain current than what was calculated theoretically in (7.1). The reason for this might be that the current through the DUT increases very rapidly due to a load inductor with relatively low inductance. Thus, the SCP might be too slow to react as rapidly as desired.

In order to obtain an SCP that intervenes at an even lower drain current, modifications have to be made. The resistor R_2 is now chosen to be much lower, thus $R_2 = 6.8 \text{ k}\Omega$. This means that

a bigger part of the voltage in the voltage division will lie across R_3 . Thus, the voltage on SCPIN that activates the SCP, $V_{SCPIN} = 0.74 V$, will be reached much faster. The results from single-pulse tests at 400 V and 600 V drain-to-source voltages are presented in Figure 7.13 and Figure 7.14.

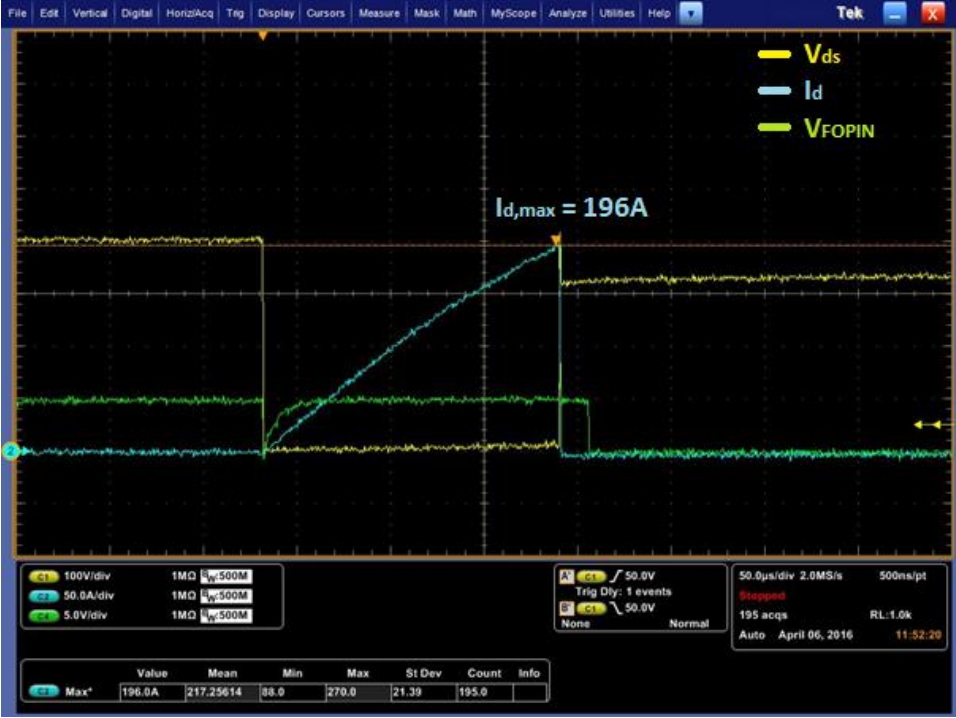


Figure 7.13: 400 V SCP test with $R_2 = 6.8 k\Omega$

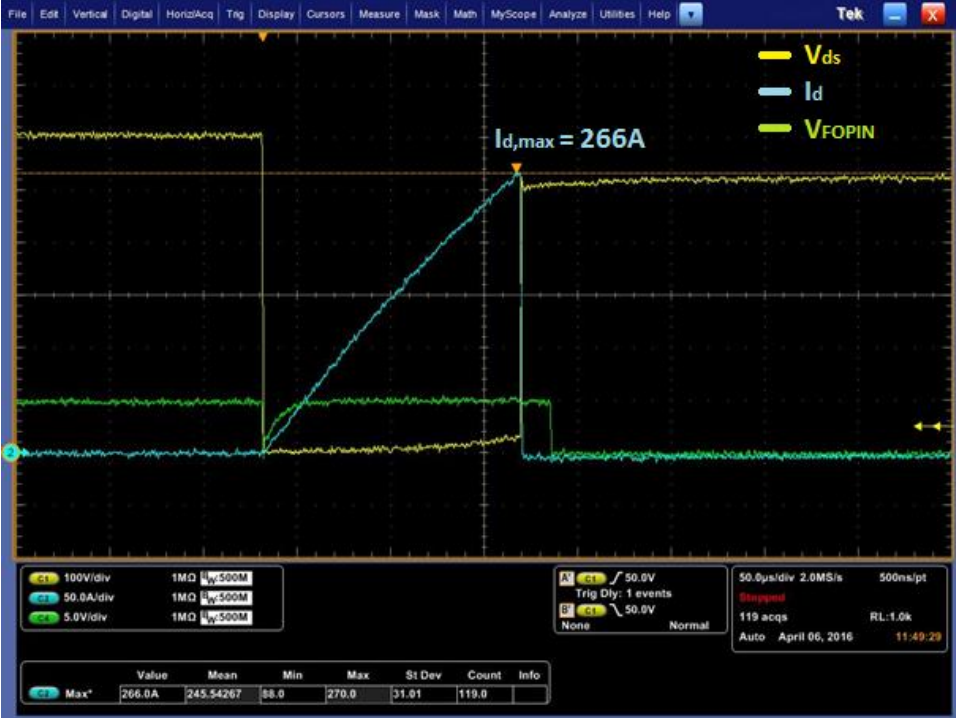


Figure 7.14: 600 V SCP test with $R_2 = 6.8 k\Omega$

The result in Figure 7.13 shows that the reduction of R_2 leads to lower maximum drain current, as the DUT now turns off at 196 A at 400 V drain-to-source voltage. In Figure 7.14, however, the DUT turns off at 266 A. Thus, an increase in drain-to-source voltage from 400 V to 600 V leads to an even higher drain current gradient, as the voltage across the load inductor is given by $v = L \cdot \frac{di}{dt}$. This means that the current through the DUT increases even more rapidly. It should be noted that Figure 7.13 and Figure 7.14 have the same time scale. As the desired test voltage is 600 V, the SCP must be modified even further.

The next SCP test will be done with $R_2 = 4.7 \text{ k}\Omega$. In addition, in order to obtain an even faster SCP, the blanking time is reduced by reducing the blanking capacitance to $C_{blank} = 68 \text{ nF}$. This gives a more rapid charging of the blanking capacitor and thus the SCPIN voltage (Section 5.1.3). The result from a single-pulse test at 600 V is presented in Figure 7.15.

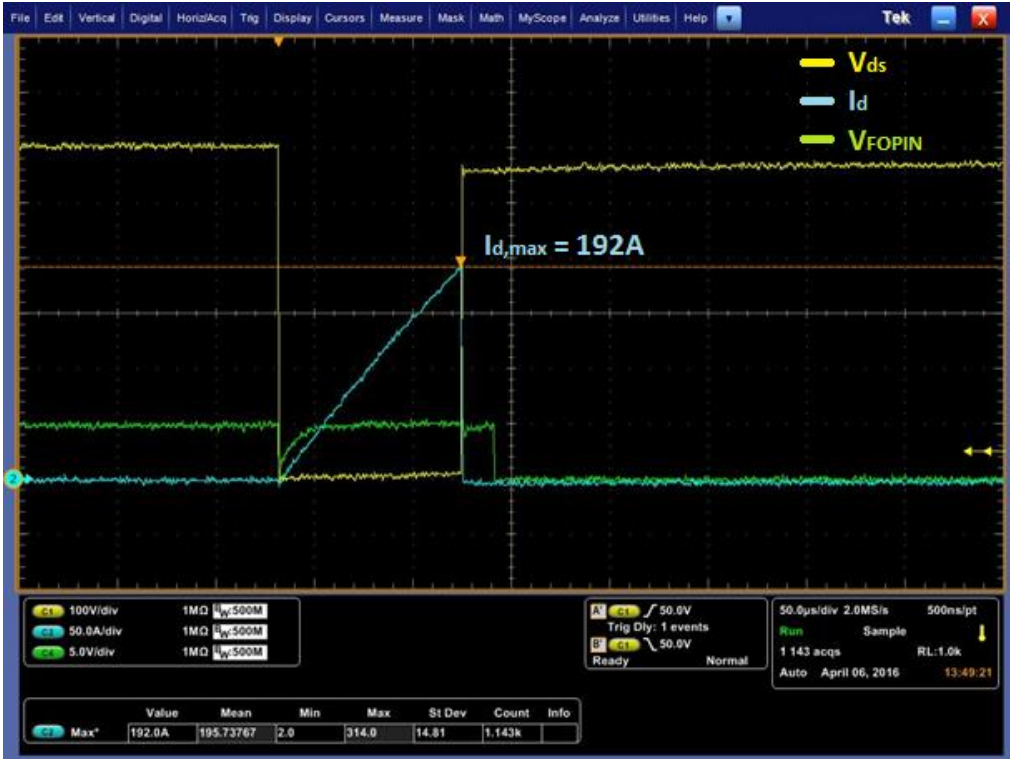


Figure 7.15: 600 V single-pulse SCP test with $R_2 = 4.7 \text{ k}\Omega$ and $C_{blank} = 68 \text{ nF}$

The DUT now turns off at 192 A drain current. This is a sufficient SCP for these short current pulses, as the DUT can handle 240 A for a period of maximum 1 ms [38]. The result from a 600 V double-pulse test with the same SCP is presented in Figure 7.16.

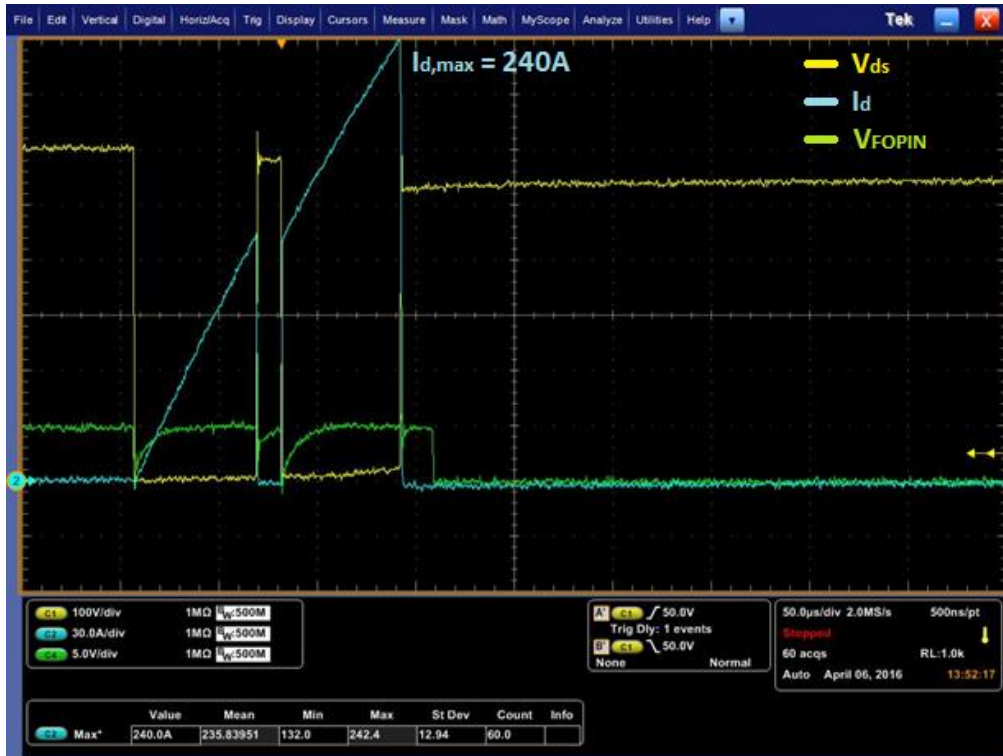


Figure 7.16: 600 V double-pulse SCP test with $R_2 = 4.7 \text{ k}\Omega$ and $C_{\text{blank}} = 68 \text{ nF}$

For the double-pulse test in Figure 7.16, the DUT turns off at 240 A. If the first pulse is not wide enough for the drain current to reach the single-pulse limit of 192 A, the SCP will not intervene during first pulse. Thus, as the load is inductive, the current is able to continue to increase during the second pulse. This leads to a much higher maximum drain current in double-pulse tests. However, the SCP is able to limit the current to safe levels also here.

As the SCP should be able to force a safe turn off at high drain currents, the gate driver needs to slow down the turn off in order not to cause too high switching stresses on the DUT. Thus, the gate driver should conduct a soft turn-off switching of the DUT if the SCP is activated. The concepts of soft switching and hard switching were explained in Section 3.5.3. Figure 7.17 presents a normal hard-switching turn-off transient of the DUT at 600 V 120 A.



Figure 7.17: Hard-switching DUT turn off at 600 V 120 A

This turn-off transient has high voltage overshoot and extensive ringing. When increasing the pulse width in order to reach the SCP drain current activation limit of 192 A, the result in Figure 7.18 is obtained.

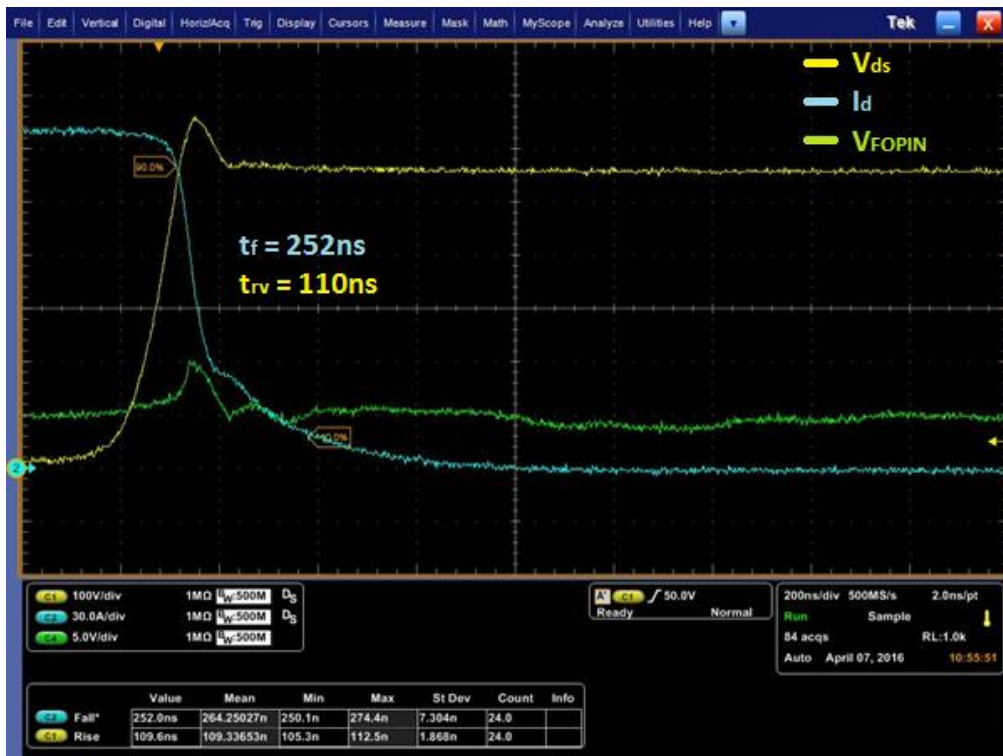


Figure 7.18: Soft turn off at 600 V 192 A to reduce switching stresses

This is not zero-voltage soft switching, as the voltage and current overlap for a wide period. However, it is clear that the activation of the SCP leads to a much slower turn-off transient than without the SCP, as the switching times increase significantly. The total turn-off time $t_{off} = t_{d(off)} + t_f$ increases by approximately 400 % from Figure 7.17 to Figure 7.18. This results in a voltage overshoot that is limited to a safe level, as well as no ringing. The turn-off function that slows down the switching is a feature provided by the BM6101FV-C gate driver IC. Such a feature is crucial for an SCP system to operate safely.

7.5 I-V Characteristics of the DUT

The I-V characteristics of the DUT can be found by conducting a double-pulse test. During the first pulse of the double pulse in Figure 7.1, the drain current of the DUT increases from 0 A to 120 A. By investigating the drain-to-source voltage across the DUT, it is possible to obtain its I-V characteristics in this particular drain current interval. It is known that the on-state drain-to-source resistance $R_{ds(on)}$ varies with the positive bias voltage $V_{gs(on)}$, as this influences the field effect of the gate. This was explained in Section 2.3.2.4. Thus, the I-V characteristics of the DUT are obtained with $V_{gs(on)} = 18\text{ V}$, which is the same value as in the SiC module datasheet. This is presented in Figure 7.19.

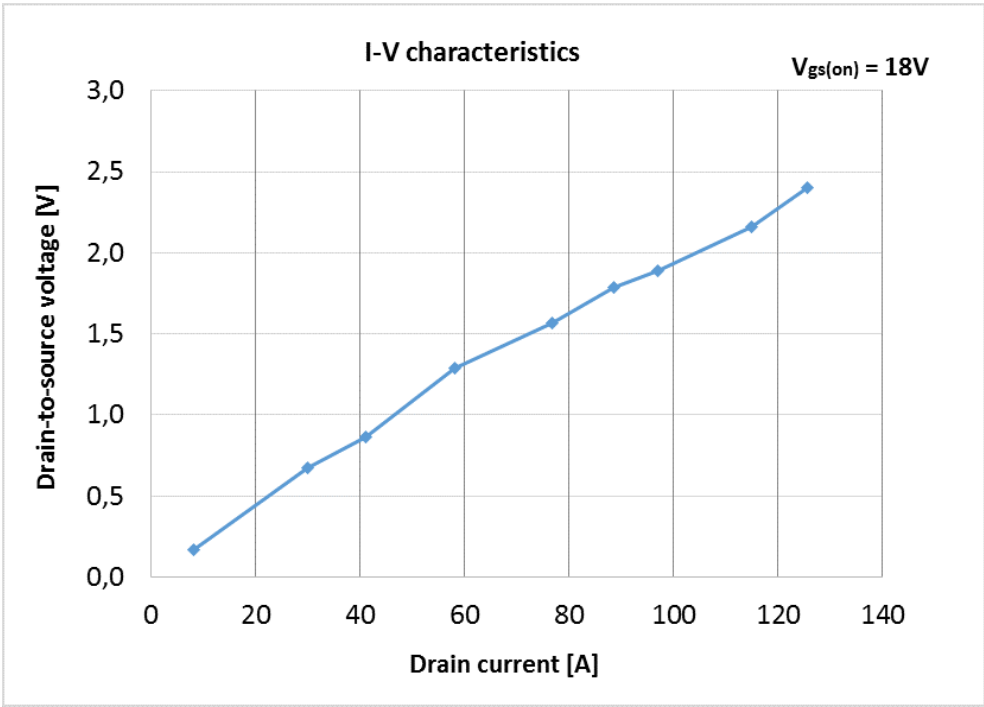


Figure 7.19: DUT I-V characteristics

The I-V characteristics in Figure 7.19 are very similar to the I-V characteristics given in the datasheet, which was presented in Figure 5.2 of this report. The I-V characteristics give an on-state drain-to-source resistance of $R_{ds(on)} = 19 \text{ m}\Omega$ for a drain current of $I_d = 120 \text{ A}$.

7.6 Switching Characteristics and Switching Losses

The switching characteristics of the DUT are obtained by conducting double-pulse tests (DPT) at 600 V drain-to-source voltage for four different drain currents, as was done in Chapter 6. The original external gate resistances are chosen in order to obtain as fast switching as possible. Thus, $R_{g,on} = 2.2 \text{ }\Omega$ and $R_{g,off} = 3.9 \text{ }\Omega$ (Section 7.3). In addition, the positive bias voltage is +18 V and the negative bias voltage is -5 V at the gate terminal of the DUT in all experiments. The switching losses in the DUT can be calculated by using (3.12) and (3.13), and are obtained by using the integration feature provided by the oscilloscope.

7.6.1 Turn-Off Switching Characteristics

The turn-off switching characteristics are investigated through double-pulse tests of the DUT at 600 V drain-to-source voltage. The DUT turn-off characteristics at 30 A, 60 A, 90 A and 120 A drain currents are given in Figure 7.20, Figure 7.21, Figure 7.22 and Figure 7.23 respectively. The MATLAB script used in Figure 7.23 is presented in Appendix F.

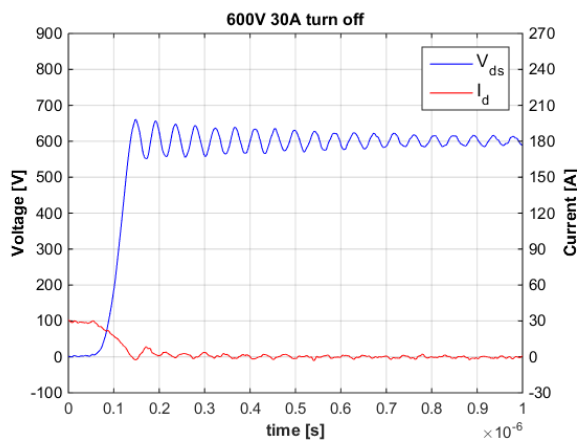


Figure 7.20: Experiment – Turn-off characteristics at 600 V 30 A

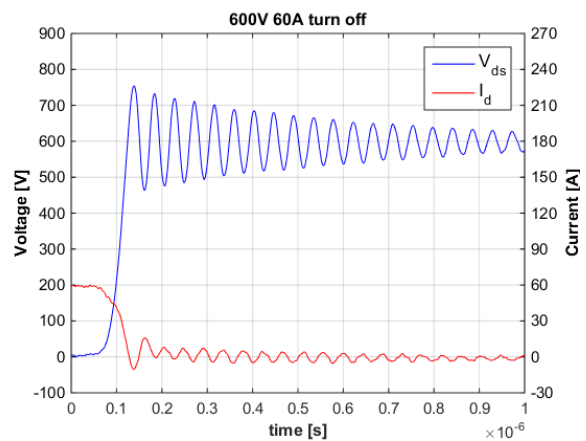


Figure 7.21: Experiment – Turn-off characteristics at 600 V 60 A

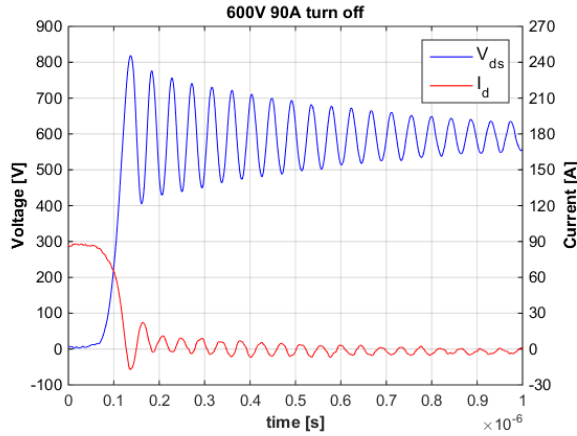


Figure 7.22: Experiment – Turn-off characteristics at 600 V 90 A

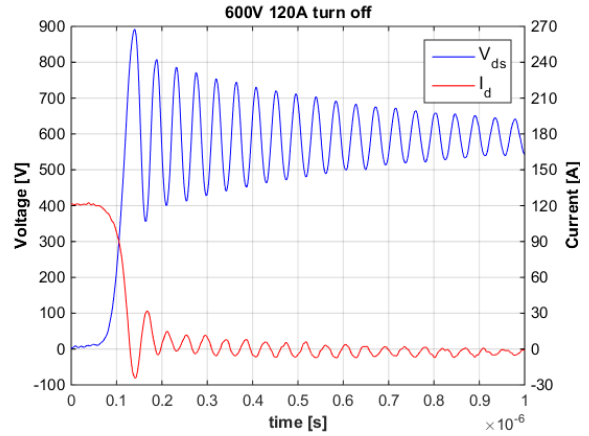


Figure 7.23: Experiment – Turn-off characteristics at 600 V 120 A

The turn-off transient is very fast, leading to high voltage overshoot and long-lasting ringing due to the stray inductance in the test circuit. It is clear that the voltage overshoot and ringing increase significantly with increased drain current. By using the information in Section 3.5.1, it is possible to find and compare the switching times of the DUT at different drain currents. Voltage rise time t_{rv} , voltage derivative dv/dt , current fall time t_f and voltage overshoot V_{os} are found during DUT turn off, and are presented in Table 7.3.

Table 7.3: Experiment – Turn-off switching characteristics

| I_d [A] | Turn off | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{rv} [ns] | t_f [ns] | dv/dt [V/ns] | V_{os} [V] |
| 30 | 50 | 62 | 9.60 | 64 |
| 60 | 37 | 50 | 12.7 | 160 |
| 90 | 35 | 42 | 13.7 | 220 |
| 120 | 34 | 39 | 14.2 | 292 |

It is evident that the turn-off transient is very fast with extremely low switching times at 120 A drain current. The turn-off switching times decrease with drain current. The voltage overshoot, however, increases with drain current due to lower current rise time as drain current increases. Thus, due to the stray inductance L_s in the circuit, and increased current derivative di/dt , $V_{os} = L_s \cdot \frac{di_d}{dt}$ increases.

7.6.2 Turn-On Switching Characteristics

The turn-on switching characteristics are investigated in the same manner through double-pulse tests of the DUT at 600 V drain-to-source voltage. The DUT turn-on characteristics at 30 A, 60 A, 90 A and 120 A drain currents are given in Figure 7.24, Figure 7.25, Figure 7.26 and Figure 7.27 respectively.

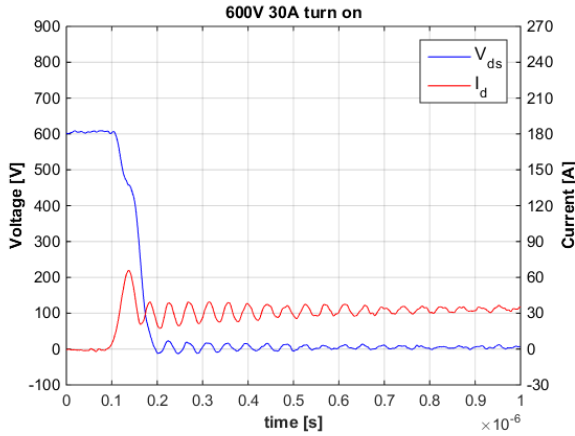


Figure 7.24: Experiment – Turn-on characteristics at 600 V 30 A

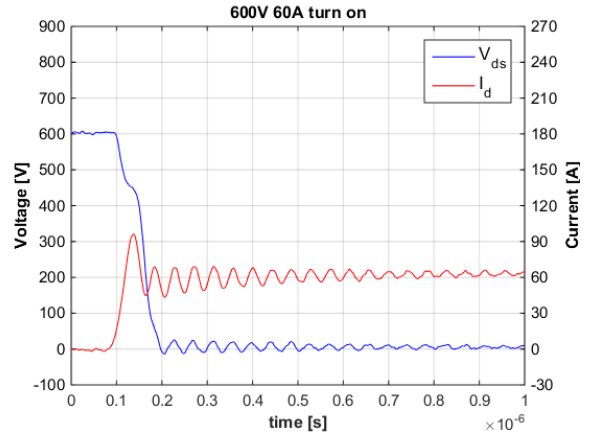


Figure 7.25: Experiment – Turn-on characteristics at 600 V 60 A

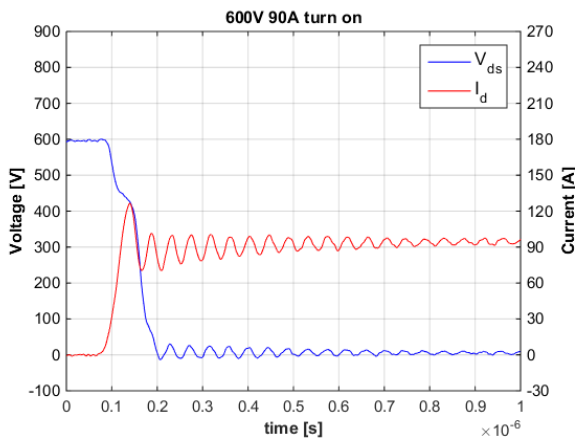


Figure 7.26: Experiment – Turn-on characteristics at 600 V 90 A

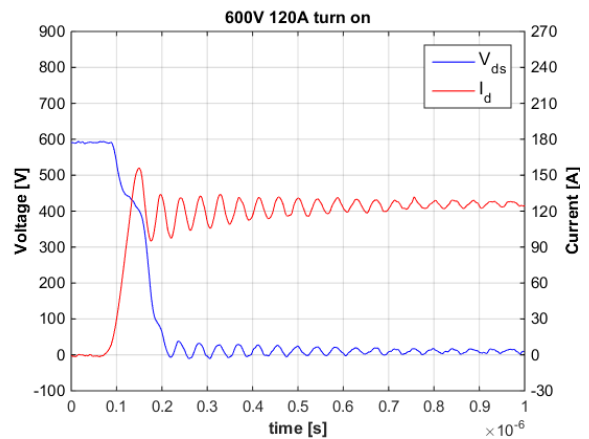


Figure 7.27: Experiment – Turn-on characteristics at 600 V 120 A

Current rise time t_r , current derivative di/dt , voltage fall time t_{fv} and current overshoot I_{os} are found during DUT turn on.

Table 7.4: Experiment – Turn-on switching characteristics

| I_d [A] | Turn on | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{fv} [ns] | t_r [ns] | di/dt [A/ns] | I_{os} [A] |
| 30 | 61 | 19 | 1.26 | 31 |
| 60 | 75 | 24 | 2.00 | 32 |
| 90 | 87 | 31 | 2.32 | 32 |
| 120 | 99 | 39 | 2.46 | 31 |

The current rise time is found to be very low, even at high drain currents. The turn-on switching times increase with drain current, as opposed to the turn-off switching times. It is found that the current overshoot in the laboratory experiments is close to independent of drain current. This is expected, as the current overshoot is caused by the discharge/reverse recovery of the junction capacitance of the freewheeling diode. As this junction capacitance does not change with drain

current, the current overshoot is constant. This was explained in Section 2.3.1. The current overshoot was found to be constant also in the simulations in Table 6.2. However, the current overshoot was significantly higher in simulation than in experiment.

7.6.3 Switching Times

The switching times in Table 7.3 and Table 7.4 are presented as a function of drain current in Figure 7.28.

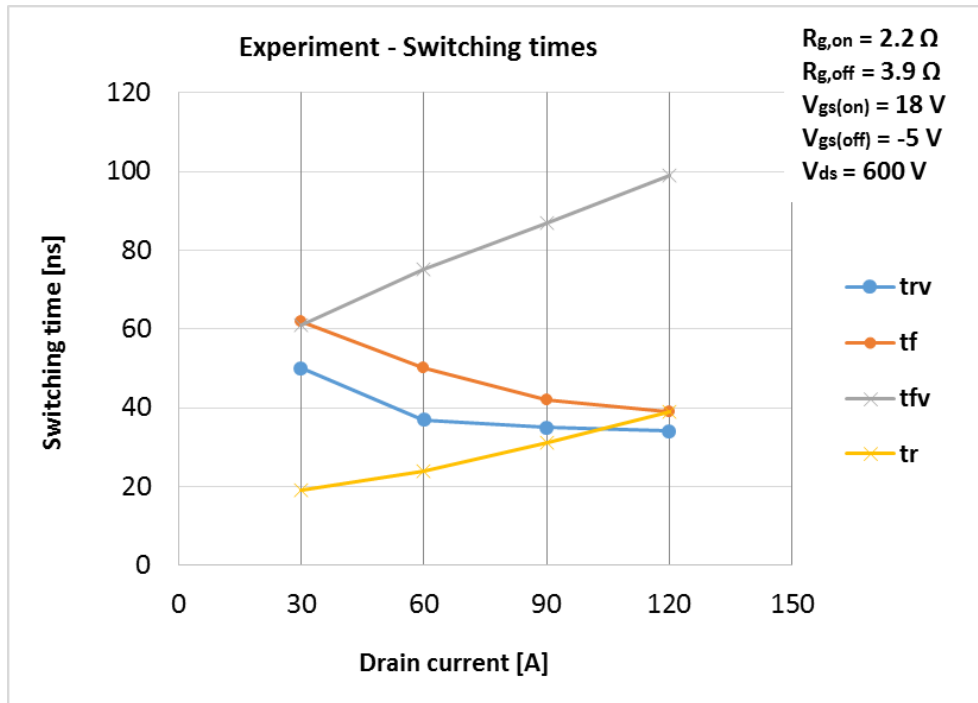


Figure 7.28: Experiment – Switching times as a function of drain current

This can be compared with Fig. 7 in the SiC module datasheet [38]. It is clear that both t_r and t_f are lower than what was presented in the datasheet. The current rise time is most likely lower due to lower turn-on gate resistance $R_{g,on}$ in Figure 7.28. The current fall time is probably lower due to the negative bias voltage $V_{gs(off)} = -5 V$ at turn off in Figure 7.28. The results in the SiC module datasheet, on the other hand, were obtained with $R_{g,on} = R_{g,off} = 3.9 \Omega$ and $V_{gs(off)} = 0 V$.

The results in Figure 7.28 can also be compared with what was found in simulation, and presented in Figure 6.5. It is found that the turn-off switching times are very similar, while the turn-on switching times are somewhat lower in the simulation results.

7.6.4 Switching Losses

The turn-on and turn-off switching losses can be calculated by using the method described in Section 3.6. The switching losses as a function of drain current are given in Figure 7.29.

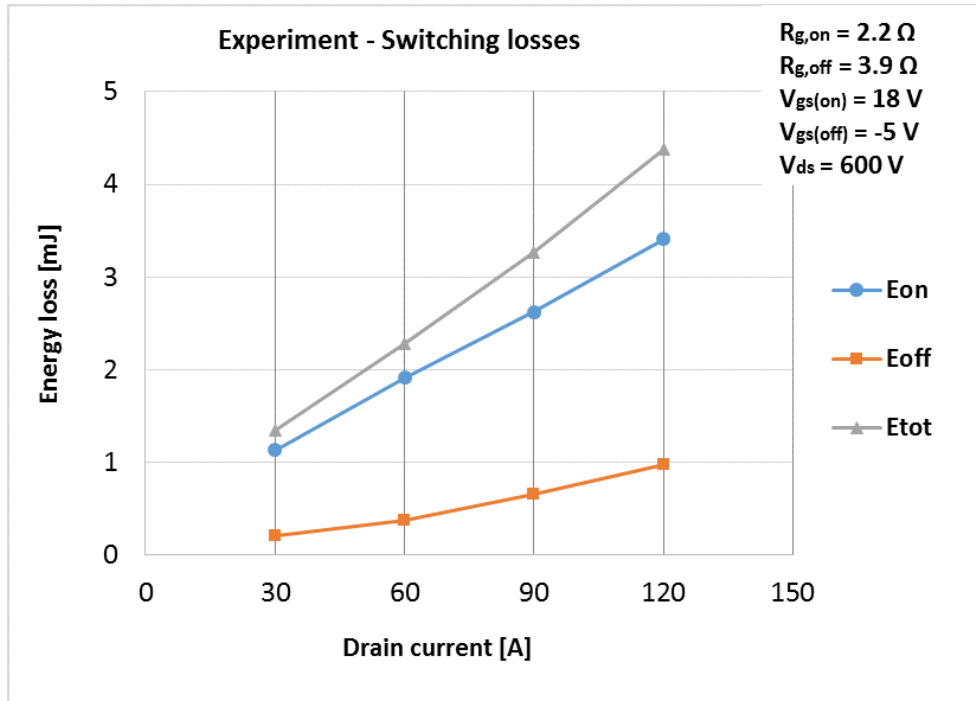


Figure 7.29: Experiment – Switching losses as a function of drain current

When comparing this result with Fig. 9 in the datasheet [38], it is clear that the turn-off switching losses are very similar. However, as the turn-on gate resistor is higher ($R_{g,on} = R_{g,off} = 3.9 \Omega$) in [38] than in Figure 7.29, this leads to higher turn-on switching losses in the datasheet.

A similar study is conducted in [73], where the same SiC module is double-pulse tested. It is clear that the switching losses in Figure 7.29 are very low in comparison. This might be due to a more suitable gate driver, as well as a more optimized test circuit layout.

Figure 7.29 can also be compared with the switching losses obtained in simulation, which were presented in Figure 6.6. It is found that the switching losses in simulation and experiment are somewhat different, especially at DUT turn on. This is probably due to an unrealistically fast turn-on transient in the simulation part. The turn-off switching losses, on the other hand, are lower in Figure 7.29.

7.7 Snubber Design

The results presented in the previous section show switching characteristics with extensive voltage overshoot and long-lasting ringing. Such DUT switching stresses would not be acceptable in a power converter, as this could wear out and destroy the transistors. In addition, the power quality of the power conversion would not be as good as desired. This problem can be solved by implementing snubber circuits, as explained in Section 4.6. In Section 6.5, it was

shown through simulation that two simple snubber circuits could be the solution to reducing voltage overshoot and ringing. In this section, the influence of these two snubbers will be tested through laboratory experiments.

7.7.1 DC Snubber

Firstly, a DC snubber is connected to the test circuit. The DC snubber is connected directly to the bus bar PCB in Figure 5.11, which places it close to the SiC module. The resulting laboratory circuit layout is depicted in Figure 7.30.

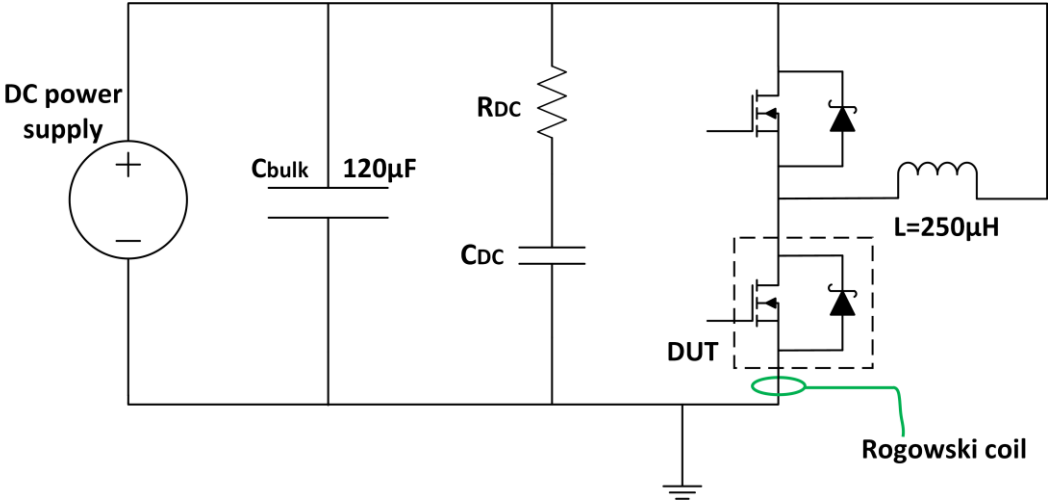


Figure 7.30: Test circuit including DC snubber

The DC snubber is connected across the DC+ and DC- power terminals of the SiC module. The addition of such a snubber circuit should improve the switching transients and the switching stresses on the DUT. The optimal values for R_{DC} and C_{DC} were found by analyzing their influence on the switching characteristics. It was found that the DC snubber giving the best switching transients was $R_{DC} = 3.33 \Omega$ and $C_{DC} = 1.8 nF$. Both components are chosen to be low-inductive types, and can be found in Appendix C. The resistance R_{DC} consists of three 10Ω resistors in parallel, which reduces the resulting stray inductance of the snubber resistor. Figure 7.30 shows the placement of the Rogowski coil, so that it measures the correct drain current of the DUT. The DUT turn-off characteristics at 30 A, 60 A, 90 A and 120 A drain currents with the optimal DC snubber are given in Figure 7.31, Figure 7.32, Figure 7.33 and Figure 7.34 respectively.

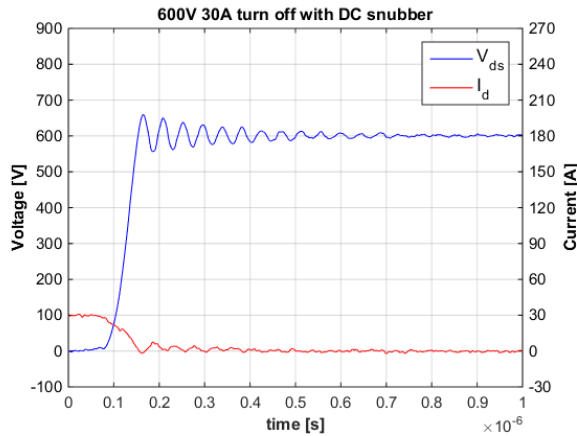


Figure 7.31: Experiment – Effect of DC snubber at 600 V 30 A turn off

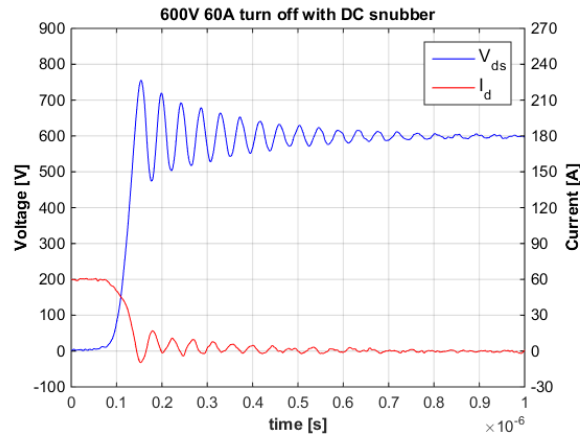


Figure 7.32: Experiment – Effect of DC snubber at 600 V 60 A turn off

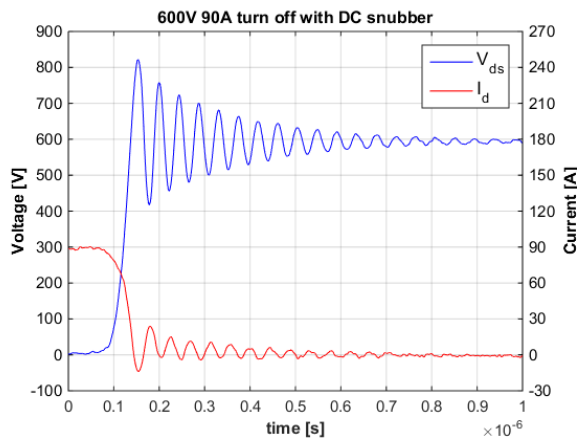


Figure 7.33: Experiment – Effect of DC snubber at 600 V 90 A turn off

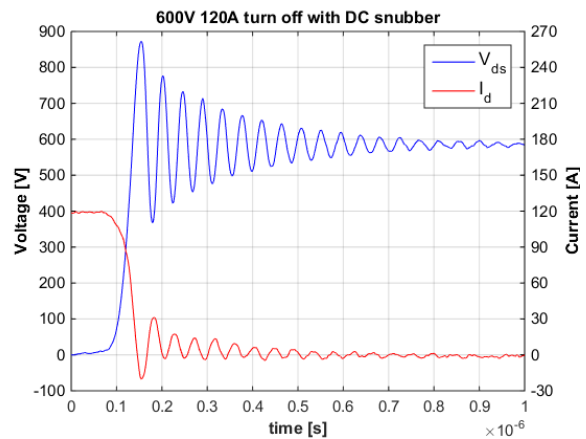


Figure 7.34: Experiment – Effect of DC snubber at 600 V 120 A turn off

The switching transient is improved, and the ringing duration is reduced significantly, compared to the results in Figure 7.20 – Figure 7.23. However, the voltage overshoot is still extensive. The optimal DC snubber values are very close to what was calculated in the theoretical part in Section 5.6.1.

The same improvement in ringing duration is found at DUT turn on. The DUT turn-on switching characteristics for the same currents as in Figure 7.31 – Figure 7.34 are presented in Appendix E.

It is found that the addition of a DC snubber does not influence the switching times considerably. This means that the switching losses are close to unaffected by the DC snubber. Thus, the implementation of a DC snubber improves the switching transients significantly without causing any disadvantages.

7.7.2 Turn-Off Snubber

In order to improve the switching characteristics even further, a turn-off snubber is added to the circuit. According to theory and simulation results, such a snubber would be able to reduce the turn-off voltage overshoot in addition to reducing the ringing duration even more. The turn-off snubber design was explained in Section 4.6, and tested through simulations in LTspice in Section 6.5.2. The resulting laboratory circuit after the addition of a turn-off snubber is presented in Figure 7.35. The Rogowski coil is placed as depicted in green, which makes it possible to measure the drain current of the DUT without measuring the current flowing through the snubbers.

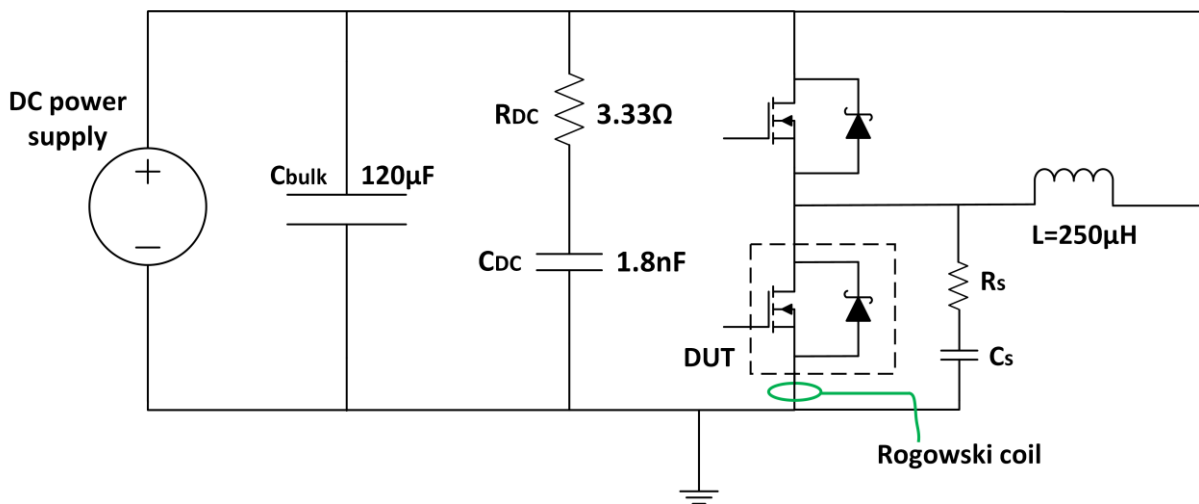


Figure 7.35: Test circuit including turn-off snubber

In order to obtain the optimal turn-off snubber values in the laboratory circuit, the influence of the snubber resistor R_s and the snubber capacitor C_s has to be found experimentally. The turn-off snubber is connected as shown in Figure 7.35, and the optimal turn-off snubber will be found through laboratory experiment. It is important to notice that the RC turn-off snubber does not include a snubber diode, as an RC snubber should be better at reducing the voltage overshoot than an RCD snubber (Section 4.7.1). The DC snubber from the previous section remains a part of the test circuit, as the DC snubber helped to improve the DUT switching characteristics.

7.7.2.1 Influence of Snubber Capacitor on Turn-Off Transient

The influence of the turn-off snubber capacitor is found through laboratory experiments. This is done by holding the turn-off snubber resistor constant. By varying the snubber capacitor, the influence of the capacitance on the switching characteristics can be investigated. Figure 7.36 presents the DUT voltage turn-off characteristics at 600 V 90 A with two different snubber capacitors and a constant snubber resistor.

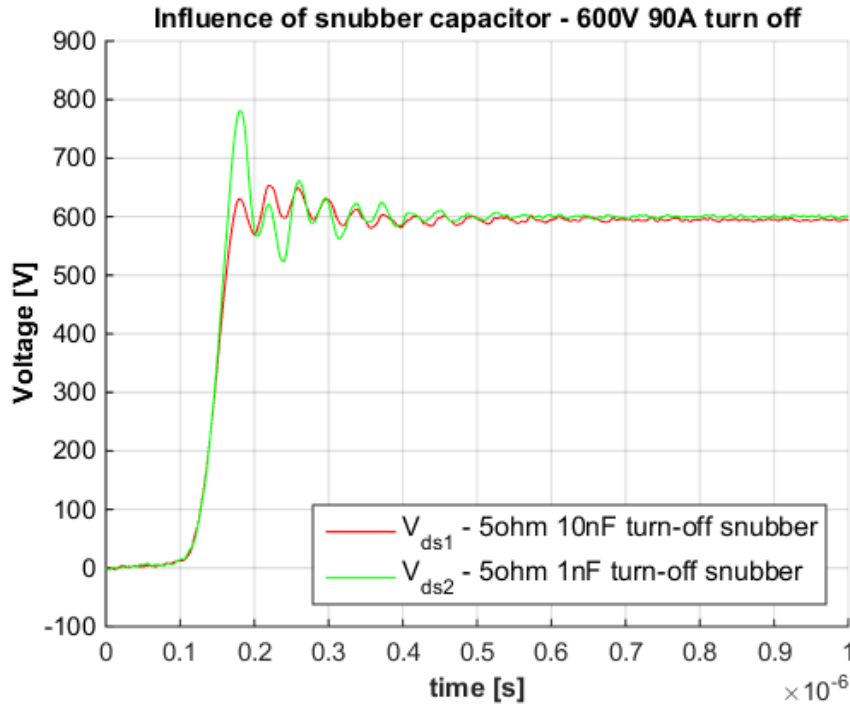


Figure 7.36: Experiment – Influence of snubber capacitor at 600 V 90 A turn off

It is clear from Figure 7.36 that an increased capacitance leads to slower switching. This again leads to higher damping and lower voltage overshoot at DUT turn off. The influence of the snubber capacitor on the total switching losses is presented in Table 7.5. The definition of the switching loss parameters was given in Section 6.5.2.1. It should be noted that Table 7.5 compare different snubber capacitors than Figure 7.36.

Table 7.5: Experiment – Influence of snubber capacitor on switching losses with $R_s = 5 \Omega$

| C_s [nF] | Turn on | | | Turn off | | |
|------------|---------------------|--------------------|-------------------|----------------------|---------------------|--------------------|
| | $E_{trans,on}$ [mJ] | $E_{snub,on}$ [mJ] | $E_{tot,on}$ [mJ] | $E_{trans,off}$ [mJ] | $E_{snub,off}$ [mJ] | $E_{tot,off}$ [mJ] |
| 1 | 4.21* | 0.07* | 4.28* | 0.58 | 0.11 | 0.69 |
| 3 | 4.55* | 0.40* | 4.95* | 0.56 | 0.25 | 0.81 |

*The turn-on losses are obtained with $R_{g,on} = 4.4 \Omega$

Even though the increased snubber capacitance gives a better turn-off transient with less voltage overshoot, increased capacitance also means higher total switching losses. In particular, the DUT turn-on switching losses increase. In addition, the switching losses in the snubber increase at both turn on and turn off due to more charge stored in the snubber capacitor. This can be seen from (4.8), which shows that the losses dissipated in the snubber resistor are proportional to the snubber capacitance.

7.7.2.2 Influence of Snubber Resistor on Turn-Off Transient

In the same manner, the influence of the snubber resistor can be investigated. This is done by holding the snubber capacitor constant. The influence of the snubber resistor on the DUT voltage turn-off waveform at 600 V 90 A is presented in Figure 7.37.

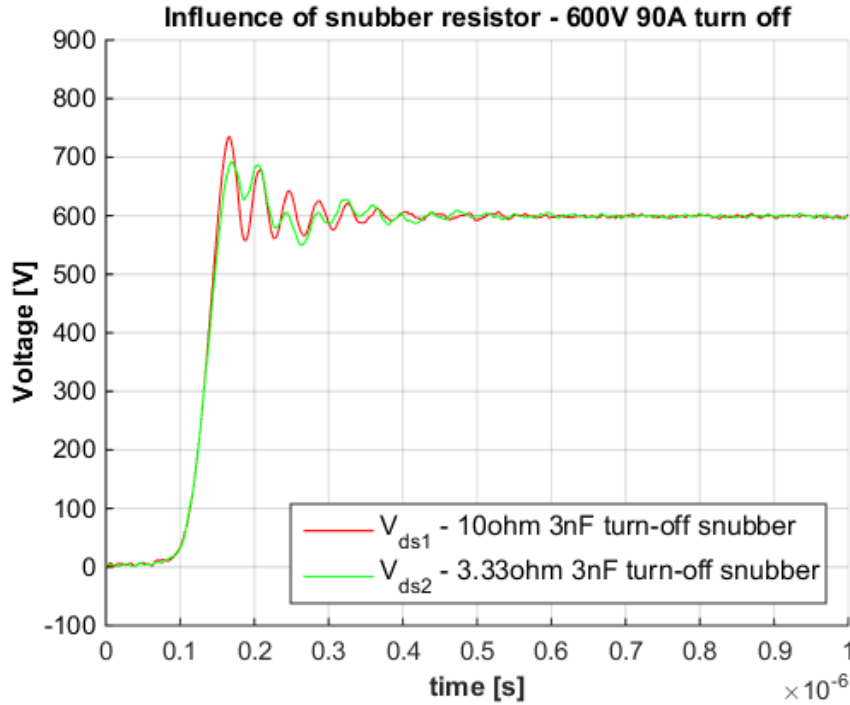


Figure 7.37: Experiment – Influence of snubber resistor at 600 V 90 A turn off

A smaller snubber resistance leads to higher damping and lower voltage overshoot during DUT turn off. This is consistent with what was presented in (4.12) for a parallel RLC circuit. However, the lower resistance introduces a low-frequency ringing. This is most probably because the 3.33 Ω resistance consists of three non-inductive 10 Ω resistors in parallel. Thus, the low-frequency ringing is caused by a resonance between the different components of the snubber. The influence of the snubber resistor on the total power losses is presented in Table 7.6. The definition of the switching loss parameters was given in Section 6.5.2.1.

Table 7.6: Experiment – Influence of snubber resistor on switching losses with $C_s = 3$ nF

| R_s [Ω] | Turn on | | | Turn off | | |
|--------------------|---------------------|--------------------|-------------------|----------------------|---------------------|--------------------|
| | $E_{trans,on}$ [mJ] | $E_{snub,on}$ [mJ] | $E_{tot,on}$ [mJ] | $E_{trans,off}$ [mJ] | $E_{snub,off}$ [mJ] | $E_{tot,off}$ [mJ] |
| 3.33 | 4.50* | 0.46* | 4.96* | 0.52 | 0.39 | 0.91 |
| 10 | 3.22* | 0.61* | 3.83* | 0.60 | 0.15 | 0.75 |

*The turn-on losses are obtained with $R_{g,on} = 4.4 \Omega$

The total turn-on losses $E_{tot,on}$ increase when the snubber resistance decreases. As the total turn-off losses $E_{tot,off}$ remain close to unchanged, lower snubber resistance leads to higher total losses. The increased power losses together with the low-frequency ringing are disadvantageous, even though the damping increases. Thus, it is chosen to use a turn-off snubber with $R_s = 10 \Omega$ and $C_s = 3 nF$ in the remaining of this report.

7.7.2.3 Turn-Off Switching Characteristics with $C_s = 3 nF$ and $R_s = 10 \Omega$

After analyzing the DUT switching characteristics with different snubber values, it was found that a turn-off snubber of $R_s = 10 \Omega$ and $C_s = 3 nF$ gives the most optimal switching transients. The passive components used in the turn-off snubber are chosen to be low-inductive types, as this helps to improve the effect of the snubber (Section 5.6). In addition, C_s consists of three 1 nF capacitors in parallel, which reduces the total stray inductance caused by the capacitors.

The following results are obtained using the optimal turn-off snubber. The DUT turn-off characteristics at 30 A, 60 A, 90 A and 120 A drain currents with turn-off snubber are given in Figure 7.38, Figure 7.39, Figure 7.40 and Figure 7.41 respectively.

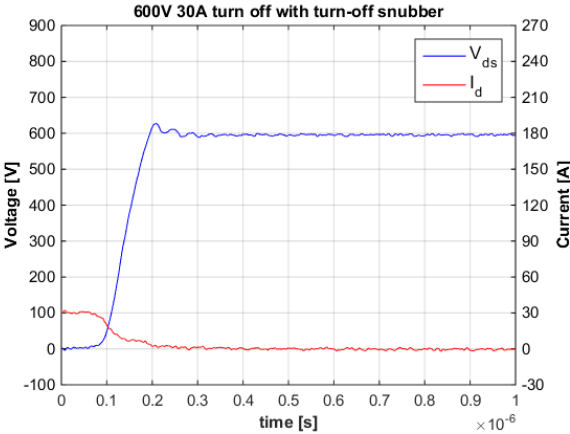


Figure 7.38: Experiment – Effect of turn-off snubber at 600 V 30 A turn off

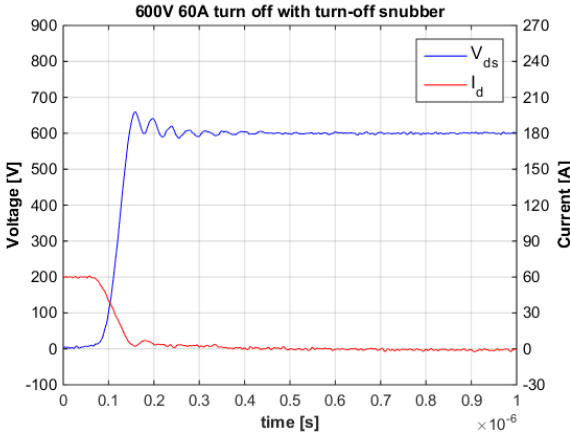


Figure 7.39: Experiment – Effect of turn-off snubber at 600 V 60 A turn off

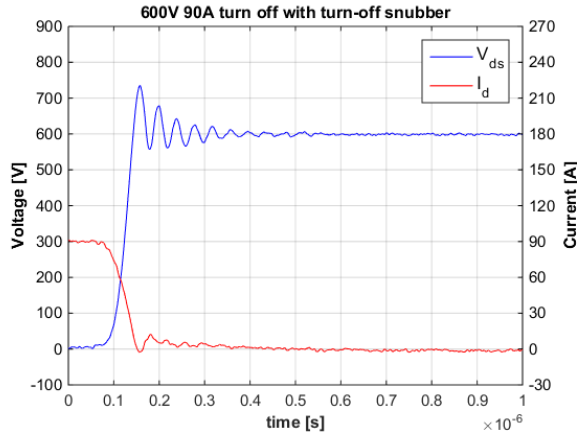


Figure 7.40: Experiment – Effect of turn-off snubber at 600 V 90 A turn off

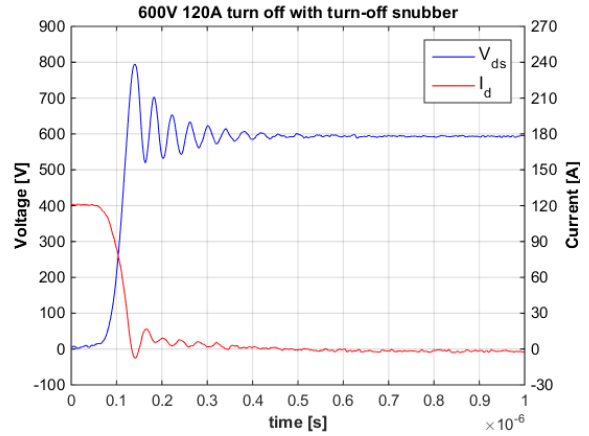


Figure 7.41: Experiment – Effect of turn-off snubber at 600 V 120 A turn off

When comparing these results with what was presented in Figure 7.20 – Figure 7.23, it is clear that the turn-off switching transient is improved significantly for all drain currents after the addition of snubbers. The turn-off switching times, voltage derivative and voltage overshoot are presented in Table 7.7.

Table 7.7: Experiment – Turn-off switching characteristics with snubbers

| I_d [A] | Turn off | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{rv} [ns] | t_f [ns] | dv/dt [V/ns] | V_{os} [V] |
| 30 | 77 | 106 | 6.2 | 28 |
| 60 | 46 | 63 | 10.4 | 97 |
| 90 | 39 | 52 | 12.2 | 136 |
| 120 | 36 | 48 | 13.3 | 196 |

When comparing Table 7.7 with Table 7.3, it is found that the switching times increase for low drain currents due to the addition of snubbers. The difference in switching time at high drain currents, however, is not significant. The voltage overshoot is reduced significantly. This is a huge advantage, as it reduces the switching stresses on the DUT.

7.7.2.4 Turn-On Switching Characteristics with $C_s = 3 \text{ nF}$ and $R_s = 10 \Omega$

The influence of the turn-off snubber on the turn-on transient will now be investigated. The DUT turn-off characteristics at 30 A, 60 A, 90 A and 120 A drain currents with turn-off snubber are given in Figure 7.42, Figure 7.43, Figure 7.44 and Figure 7.45 respectively.

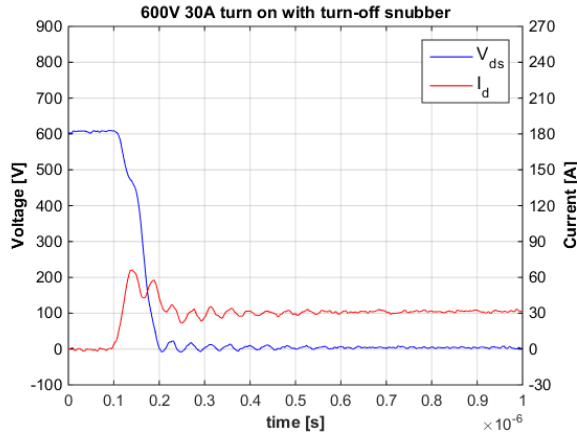


Figure 7.42: Experiment – Effect of turn-off snubber at 600 V 30 A turn on

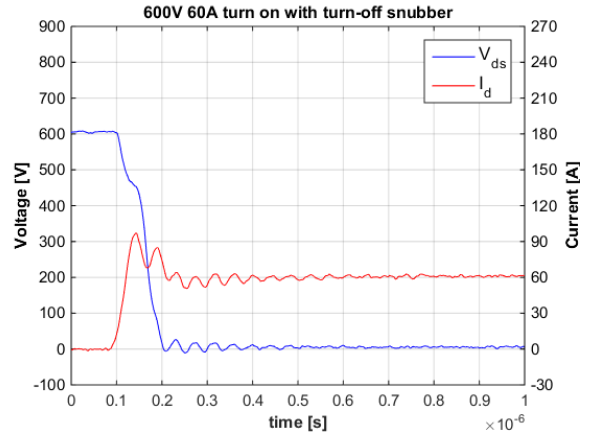


Figure 7.43: Experiment – Effect of turn-off snubber at 600 V 60 A turn on

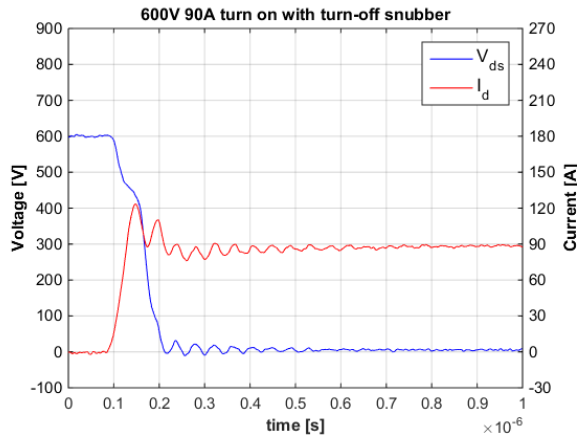


Figure 7.44: Experiment – Effect of turn-off snubber at 600 V 90 A turn on

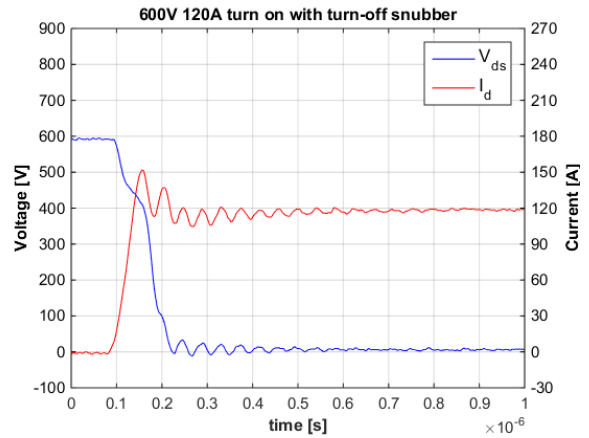


Figure 7.45: Experiment – Effect of turn-off snubber at 600 V 120 A turn on

Current rise time t_r , current derivative di/dt , voltage fall time t_{fv} and current overshoot I_{os} are found during DUT turn on, and are presented in Table 7.8.

Table 7.8: Experiment – Turn-on switching characteristics with snubbers

| I_d [A] | Turn on | | | |
|-----------|---------------|------------|----------------|--------------|
| | t_{fv} [ns] | t_r [ns] | di/dt [A/ns] | I_{os} [A] |
| 30 | 68 | 15 | 1.60 | 36 |
| 60 | 81 | 23 | 2.09 | 37 |
| 90 | 90 | 30 | 2.40 | 33 |
| 120 | 102 | 37 | 2.59 | 32 |

It is found that the turn-on switching transient still is very fast, even after the addition of the turn-off snubber. When comparing with the results in Table 7.4, the current rise time has in fact increased marginally. However, the turn-off snubber influences the turn-on transient in a negative manner by increasing the duration and the height of the current overshoot.

7.7.3 Switching Characteristics Improvement

In the same manner as in Section 6.5.3, a comparison of the switching characteristics before and after the addition of snubbers is done for the experimental part. Figure 7.46 presents the improvement in the DUT turn-off characteristics at 600 V 90 A after the addition of the optimal DC snubber.

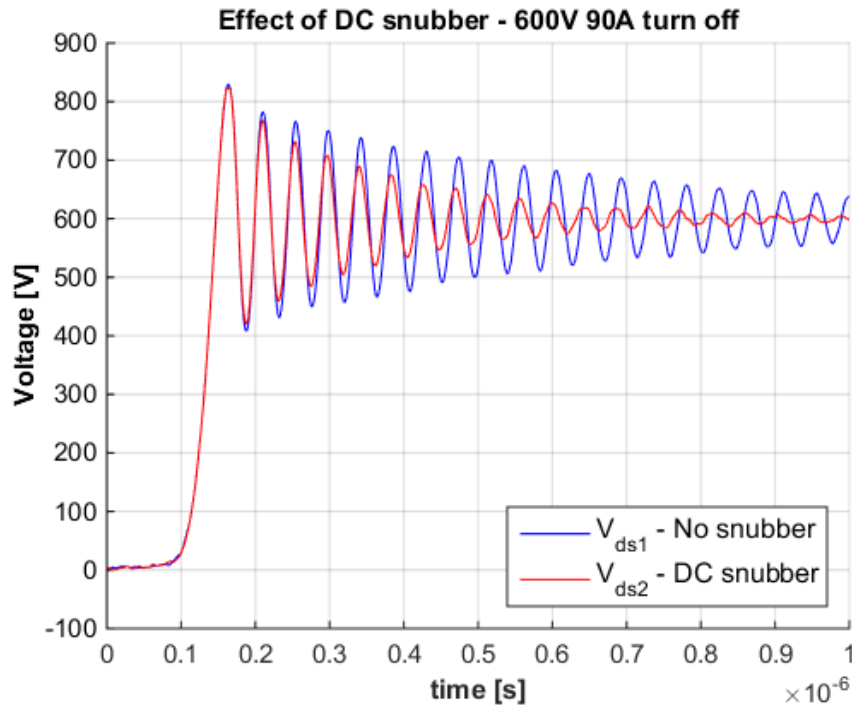


Figure 7.46: Experiment – Turn-off improvement after addition of DC snubber

It is clear that the DUT turn-off characteristics is improved significantly because of the DC snubber. The ringing duration at 600 V 90 A is reduced by approximately 60 %. This is done without influencing the switching time. The voltage overshoot, however, is only marginally reduced. As a big part of the parasitic inductance is located inside the module, such a DC snubber will not be able to reduce all voltage ringing and overshoot at turn off.

Figure 7.47 presents the DUT turn-off improvements at 600 V 90 A after the addition of the optimal turn-off snubber.

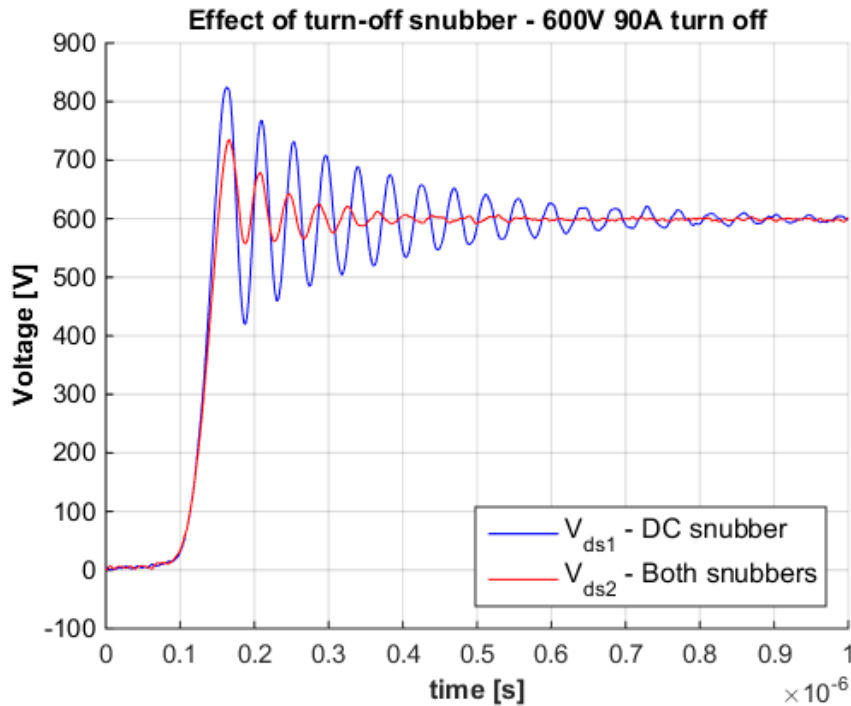


Figure 7.47: Experiment – Turn-off improvement after addition of turn-off snubber

The addition of the optimal turn-off snubber reduces the voltage overshoot by approximately 100 V, which is a reduction of 40 % at 600 V 90 A. In addition, the ringing duration is further reduced. The ringing duration is reduced by additional 65 %, resulting in a reduction of 85 % compared to without snubber. However, as can be seen from Figure 7.47, the switching time increases because of the turn-off snubber. This has an influence on switching losses.

The same kind of comparison is conducted at DUT turn on. The current turn-on transient at 600 V 90 A is presented without snubber and with the optimal DC snubber in Figure 7.48.

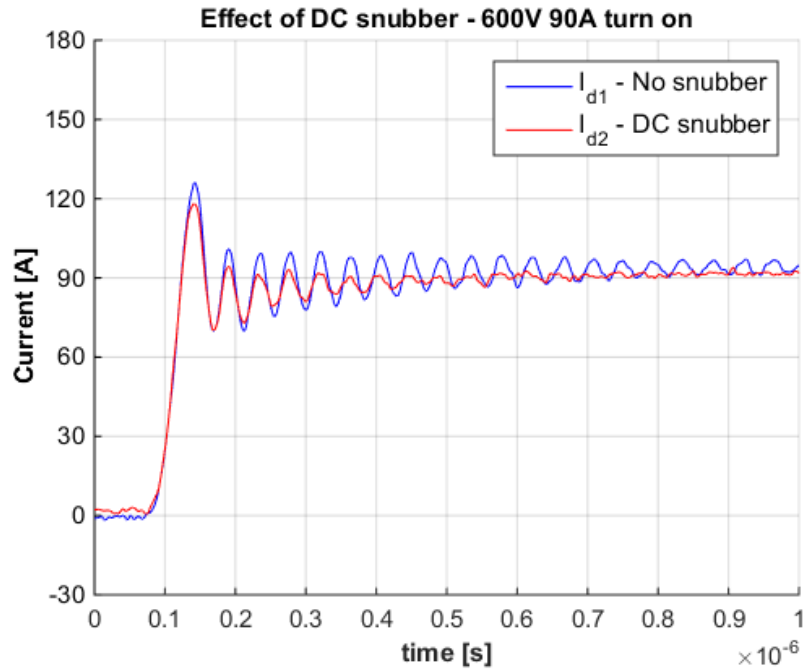


Figure 7.48: Experiment – Turn-on improvement after addition of DC snubber

The DC snubber helps to reduce the current ringing duration by approximately 43 % at DUT turn on. In addition, the current overshoot is reduced. This is achieved without influencing the switching time.

Figure 7.49 presents the turn-on current characteristics after the addition of the turn-off snubber, together with the turn-on transient with DC snubber.

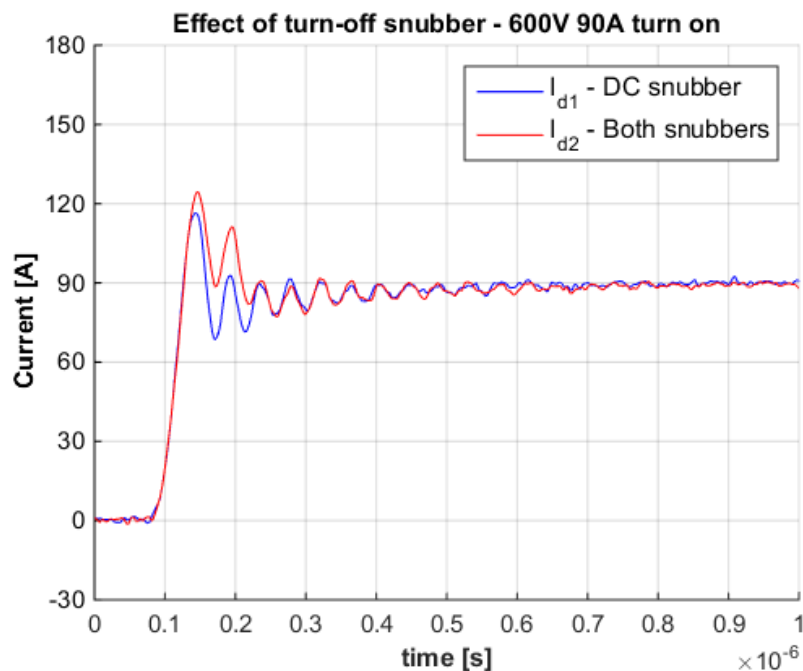


Figure 7.49: Experiment – Turn-on transient after addition of turn-off snubber

The turn-off snubber influences the turn-on transient in a negative way, in contrast to the DC snubber. It is clear that both the duration and the height of the current overshoot increase due to the addition of a turn-off snubber.

7.7.4 Switching Times with Snubbers

Figure 7.50 presents the switching times of the DUT after the addition of snubbers as a function of drain current. These results were obtained in Table 7.7 and Table 7.8.

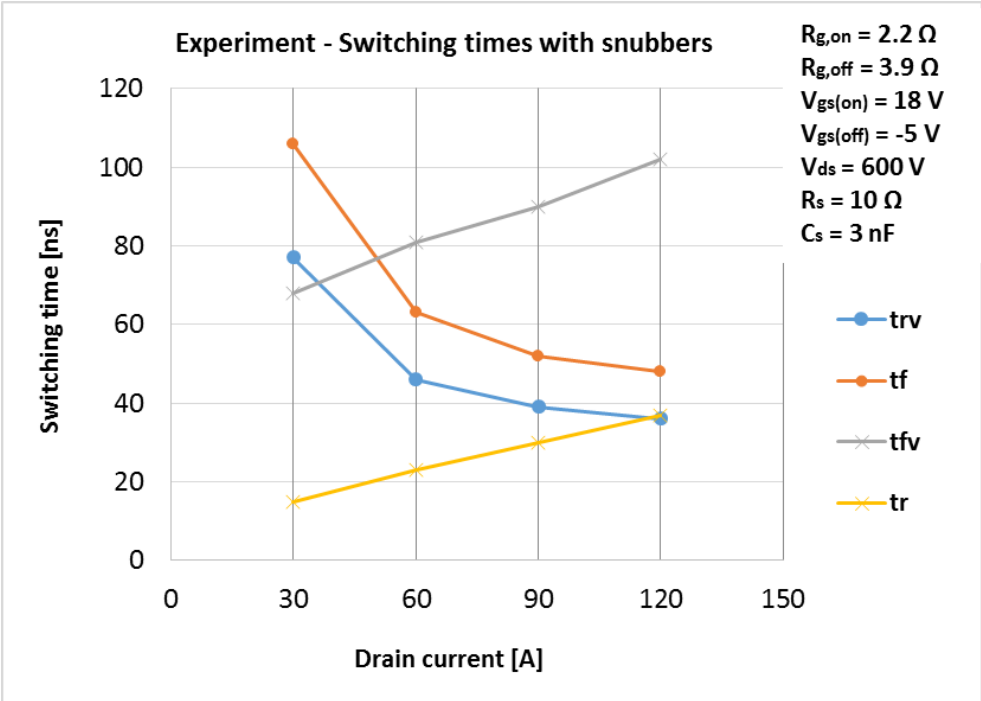


Figure 7.50: Experiment – Switching times as a function of drain current with snubbers

These results can be compared with the results without snubbers in Figure 7.28. It is found that all the switching times increase, except for the current rise time, which decreases marginally after the connection of snubbers. The biggest difference in switching time is found for small drain currents.

7.7.5 Switching Losses with Snubbers

The switching losses after the addition of snubbers are presented in Figure 7.51. The figure includes information on where in the circuit the losses are dissipated. The definition of the parameters in Figure 7.51 was given in Section 6.5.2.1.

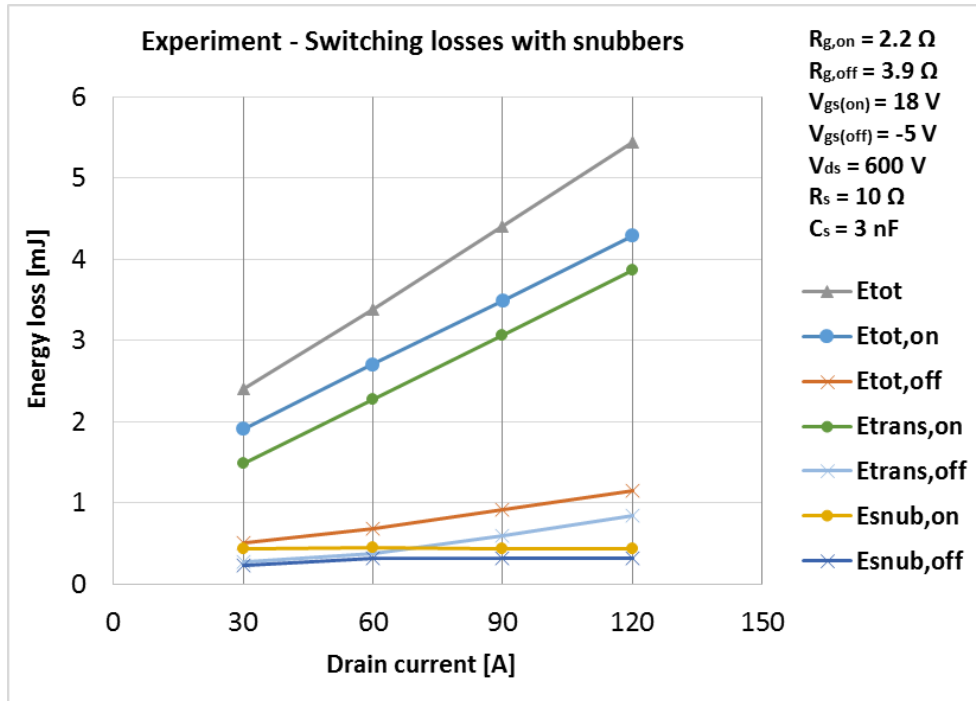


Figure 7.51: Experiment – Switching losses as a function of drain current with snubbers

The total turn-on and turn-off switching losses only increase marginally compared to what was presented in Figure 7.29. At a drain current of 120 A, the total turn-on switching losses $E_{tot,on}$ increase by 25 % and the total turn-off switching losses $E_{tot,off}$ increase by 18 %. This results in a 24 % increase in total switching losses E_{tot} , compared to Figure 7.29. The most significant switching losses are dissipated in the DUT at turn on, which are denoted as $E_{trans,on}$. As the losses in the snubber are very low compared to the turn-on switching losses in the DUT, the total switching losses do not increase significantly. The addition of a turn-off snubber actually leads to lower turn-off switching losses in the DUT, denoted as $E_{trans,off}$. This is a very handy property of the turn-off snubber, which was explained in Section 4.7.1. The snubber losses at turn on and turn off are close to independent of drain current. This is expected, as the losses dissipated in the turn-off snubber resistor only depend on the snubber capacitance and the voltage across it. This was shown in (4.8).

7.8 Voltage Dependence Test with Snubbers

In order to characterize the influence of the input DC voltage on the DUT switching losses and switching times, a voltage dependence test is conducted. This test is conducted at a constant drain current $I_d = 60$ A, with both snubbers connected. The switching losses as a function of drain-to-source voltage are presented in Figure 7.52. The definition of the parameters was given in Section 6.5.2.1.

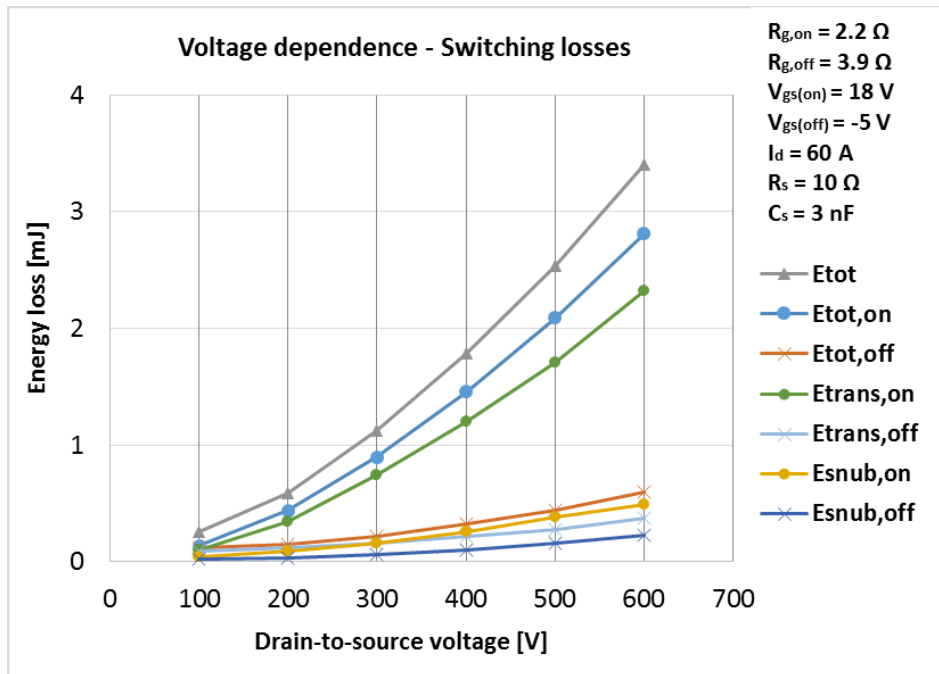


Figure 7.52: Voltage dependence – Switching losses

The turn-on and turn-off switching losses in the transistor increase with drain-to-source voltage. This should be expected, as the instantaneous power $v_{ds}(t) \cdot i_d(t)$ across the DUT increases. The switching losses in the snubber also increase with drain-to-source voltage. This can be explained using (4.8), which says that the losses dissipated in the turn-off snubber resistor are proportional to the square of the drain-to-source voltage.

The switching times as a function of drain-to-source voltage are given in Figure 7.53.

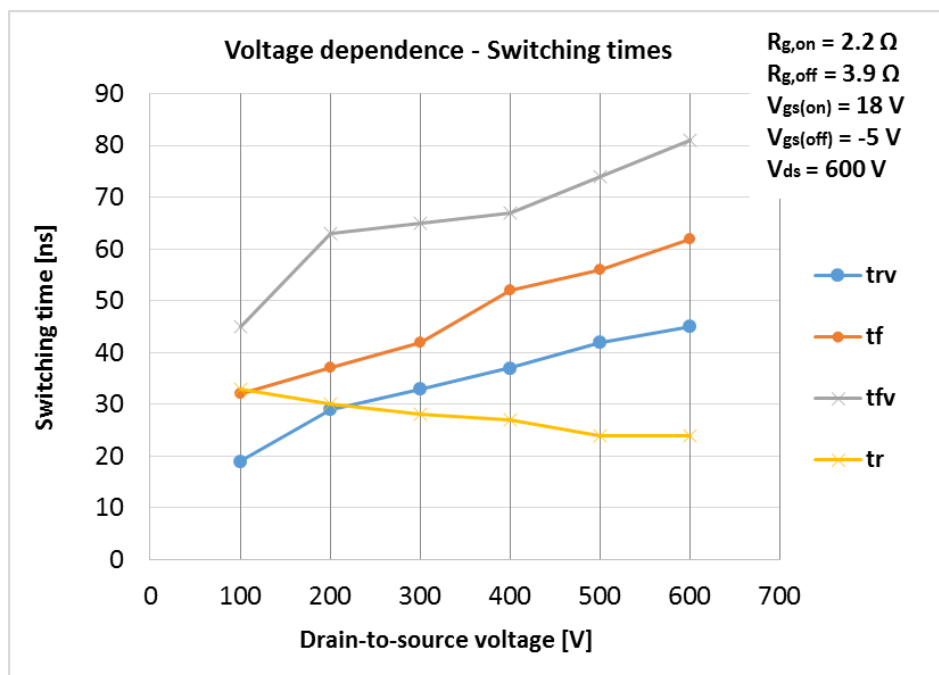


Figure 7.53: Voltage dependence – Switching times

All the switching times increase with the drain-to-source voltage, except for the current rise time t_r , which decreases.

7.9 Comparison of Experiment, Simulation and Datasheet

In this section, the switching characteristics and switching losses obtained through experiment and simulations are analyzed and compared. This is done in order to investigate how well the simulation circuit represents the laboratory circuit, and what improvements that could be made in the simulation circuit. The comparison also includes values from the SiC module datasheet.

7.9.1 Turn-Off Comparison without Snubber

The DUT turn-off voltage waveforms obtained in simulation and experiment at 600 V 90 A are plotted in the same figure in order to compare the transients. This is presented in Figure 7.54.

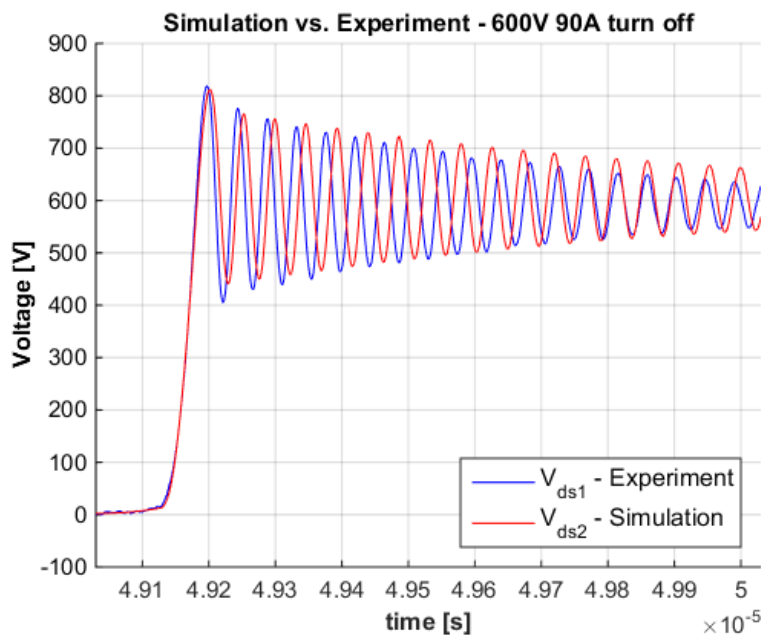


Figure 7.54: Without snubbers – Comparison of turn-off voltage waveforms at 600 V 90 A

The switching speed and voltage derivative seem very similar in simulation and experiment. The voltage overshoot is also very similar. The ringing frequency, however, is different in the two cases. In the simulation characteristics, the ringing frequency is $f_{r,sim} = 21.5 \text{ MHz}$. In the experiment characteristics, on the other hand, the ringing frequency is $f_{r,exp} = 22.7 \text{ MHz}$. The reason for this is that the stray inductance in the simulation circuit is a little too high. If the stray inductance L_{stray} in Figure 6.2 is changed from 55 nH to 47 nH, then the ringing frequency in simulation and experiment will be the same. This solution, however, reduces the voltage overshoot. This is shown in Figure 7.55.

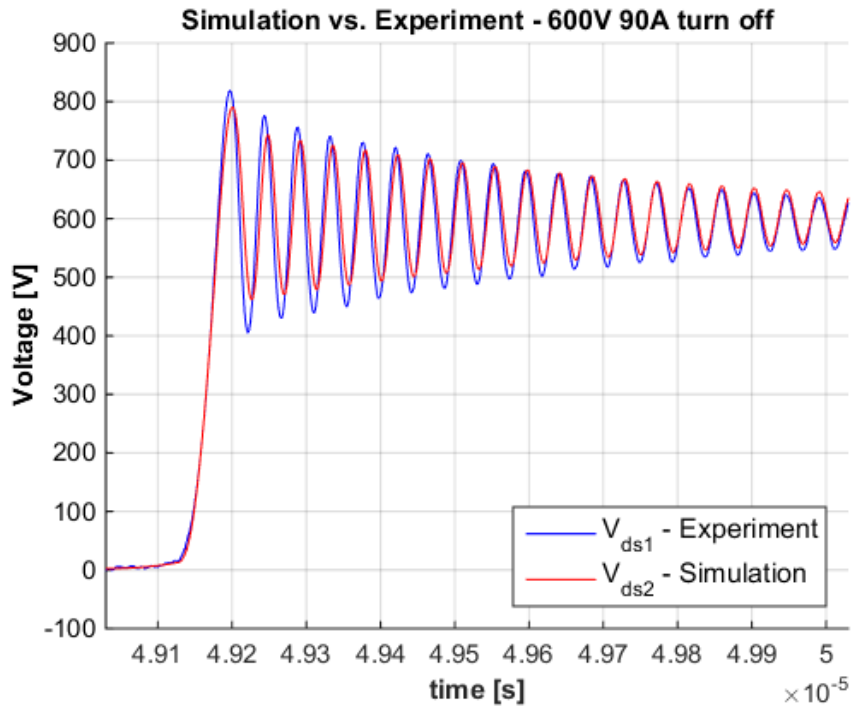


Figure 7.55: Without snubbers – Simulation circuit with reduced stray inductance

Even though this change in stray inductance influences the ringing frequency significantly, it does not influence the switching times and derivatives considerably. In Chapter 6, it was decided to use the stray inductance that gives the most similar voltage overshoot, which was 55 nH. For the remaining of this comparison, on the other hand, it is determined to use the stray inductance that gives the most similar ringing frequency in simulation and experiment, which is 47 nF.

7.9.2 Turn-Off Comparison with Snubbers

The same comparison can be conducted after including the optimal DC and turn-off snubbers. A comparison of the turn-off voltage waveforms with snubbers at 600 V 90 A are presented in Figure 7.56. It is clear from the Figure 7.56 that the turn-off voltage characteristics with snubbers are not perfectly represented by the simulation circuit. Whereas the voltage ringing in simulation is very quickly attenuated, the voltage ringing in experiment is more extensive. This might be due to simplifications in the simulation circuit that make it inaccurate compared to the laboratory circuit. Such simplifications are most likely located in the driver circuit, as well as in parasitic inductance, capacitance and resistance. The difference might also be due to influence of the measuring instruments used in the laboratory experiments. It is very difficult, however, to say exactly what makes the switching characteristics in simulation and experiment different.

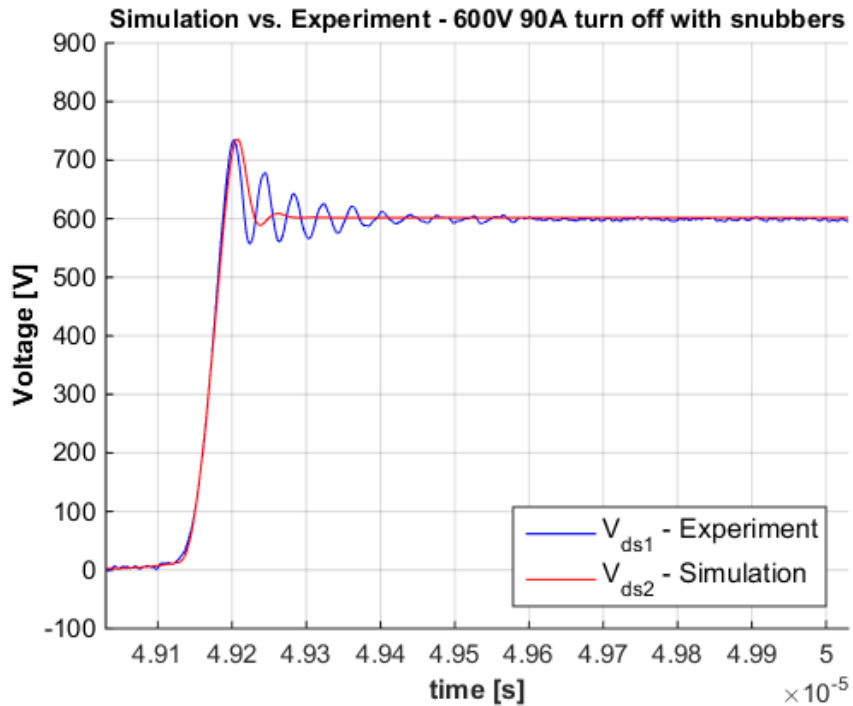


Figure 7.56: With snubbers – Comparison of turn-off voltage waveforms at 600 V 90 A

7.9.3 Turn-On Comparison without Snubber

In the same manner as in the previous section, a comparison of the turn-on switching characteristics in experiment and simulations is conducted. The turn-on current characteristics at 600 V 90 A are presented in Figure 7.57.

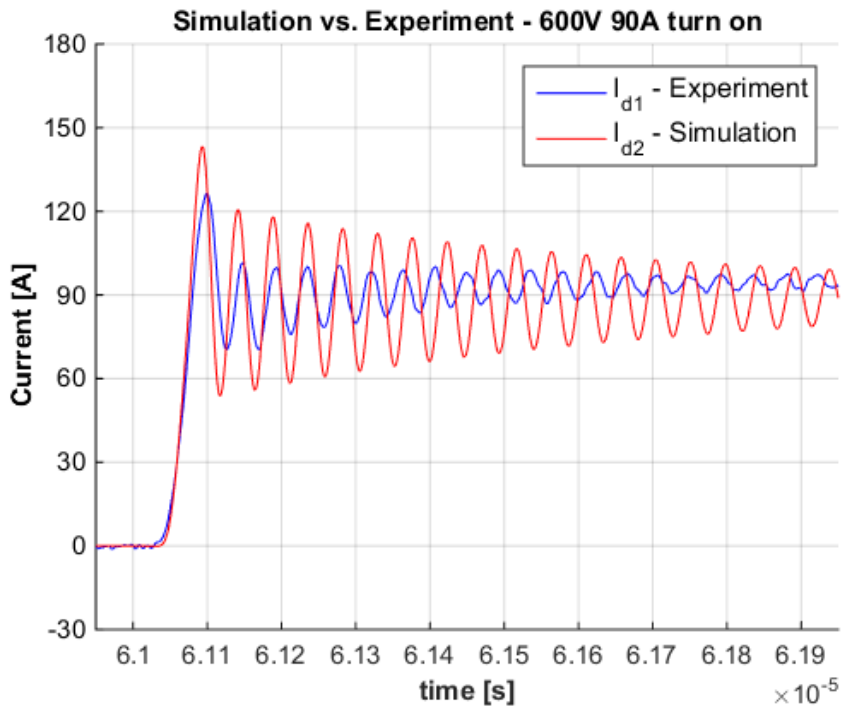


Figure 7.57: Without snubbers – Comparison of turn-on current waveforms at 600 V 90 A

It is clear that the current turn-on transient is not as well represented by the simulation circuit as the voltage turn-off transient. The current overshoot is higher, with a more long-lasting and high-amplitude ringing. This result suggests that the stray inductance in the simulation circuit is higher than what is actually the case in the laboratory circuit. However, as was seen in Figure 7.55, the turn-off voltage waveform was well represented by the same simulation circuit. The turn-on current characteristics can be modified by changing the turn-on gate resistance $R_{g,on}$ in Figure 6.2. By increasing the turn-on gate resistance to $R_{g,on} = 5 \Omega$, the result in Figure 7.58 is obtained.

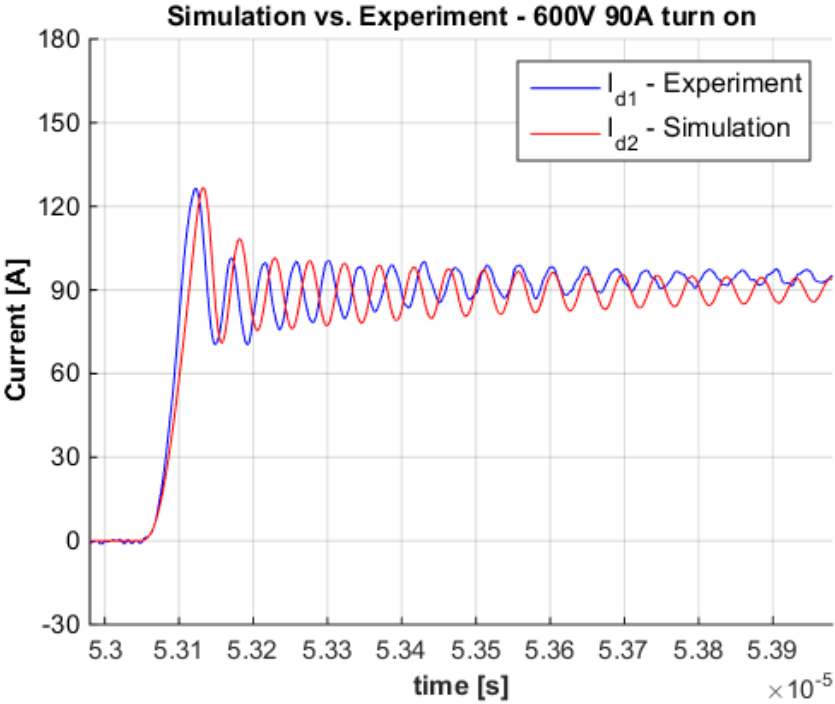


Figure 7.58: Without snubbers – Simulation circuit with reduced turn-on gate resistance

This modified simulation circuit represents the current turn-on transient in a better way. However, the turn-on switching time in simulation is now very different from the turn-on switching time in experiment. Thus, it was in this report determined to use the turn-on gate resistance that gave the most similar switching time, which is what was used in Figure 7.57. In the remaining of this comparison, on the other hand, it is determined to use the turn-on gate resistance that makes simulation and experiment as similar as possible. Thus, $R_{g,on} = 5 \Omega$ also in Figure 7.59.

7.9.4 Turn-On Comparison with Snubbers

The turn-on current waveforms at 600 V 90 A after the addition of snubbers are presented in Figure 7.59.

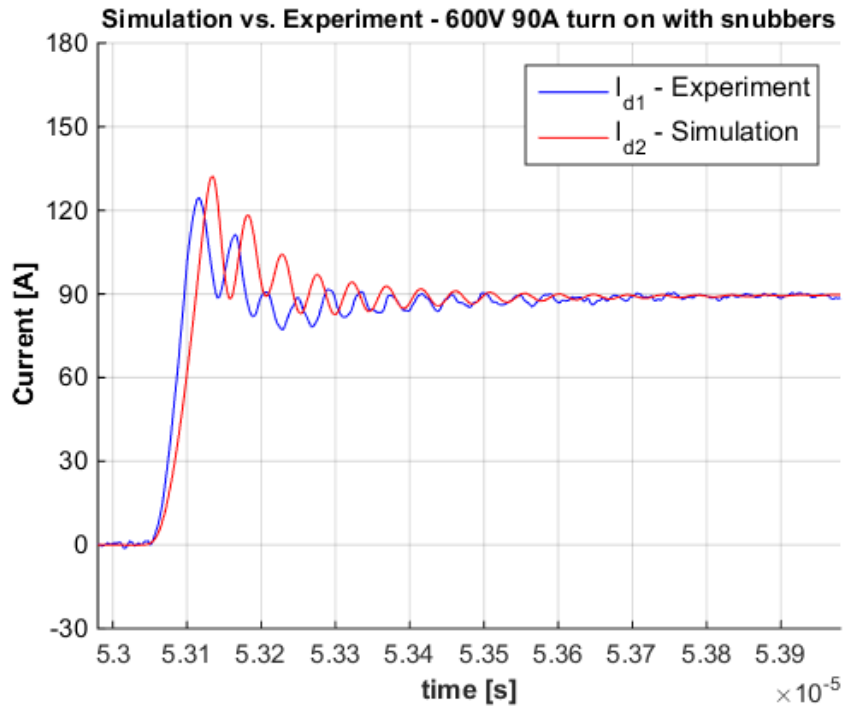


Figure 7.59: With snubbers – Comparison of turn-on current waveforms at 600 V 90 A

Even though the waveforms in simulation and experiment look very similar, there is a big difference in switching time due to the increase in turn-on gate resistance in the previous section.

It is clear from the comparisons that it is possible to make simulation results come very close to the real experimental results. However, there will always be aspects in the laboratory circuit that are very difficult to implement in a simulation circuit. In addition, the LTspice model of the SiC module might not be accurate. Thus, simulation results should only be used as guidance. Simulation is an excellent way of testing new ideas before implementing them at the laboratory.

7.9.5 Comparison of Switching Times

In this section, the switching times of the DUT obtained in simulation and experiment are plotted in the same figure and compared. In addition, the switching times presented in the SiC module datasheet are plotted together with simulation and experimental results [38]. Figure 7.60 presents the current switching times without snubbers as a function of drain current. The switching times denoted as “exp” are obtained through laboratory experiments, the switching times denoted as “sim” are found through simulations in LTspice and the switching times denoted as “dat” are presented in the SiC module datasheet.

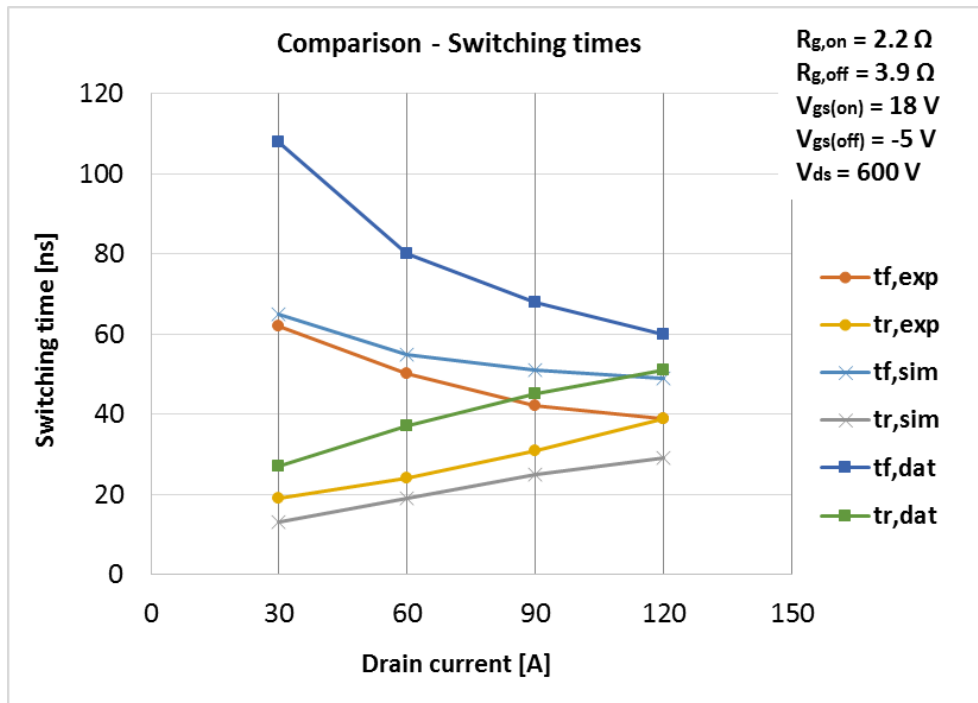


Figure 7.60: Without snubbers – Comparison of switching times in simulation, experiment and datasheet

The switching times presented in the SiC module datasheet are obtained with $R_{g,on} = R_{g,off} = 3.9 \Omega$. In addition, $V_{gs,off} = 0 V$. Thus, the conditions in the datasheet are different from what was used in simulation and experiment. A higher turn-on gate resistance leads to higher current rise time $t_{r,dat}$ in the datasheet than in experiment and simulation. By not applying a negative bias voltage at turn off, the current fall time obtained in the datasheet is higher than in experiment and simulation. However, the switching times in all three cases have similar development with increased drain current. The current rise time is higher in experiment than in simulation, while the current fall time is lower in the laboratory results.

The same kind of comparison is done for the current switching times after the addition of snubbers. This is presented in Figure 7.61. This figure shows the influence of the snubbers on the switching times in the experimental part. t_f and t_r are the current fall time and rise time without snubbers, while $t_{f,snub}$ and $t_{r,snub}$ are the current fall time and rise time after the addition of snubbers.

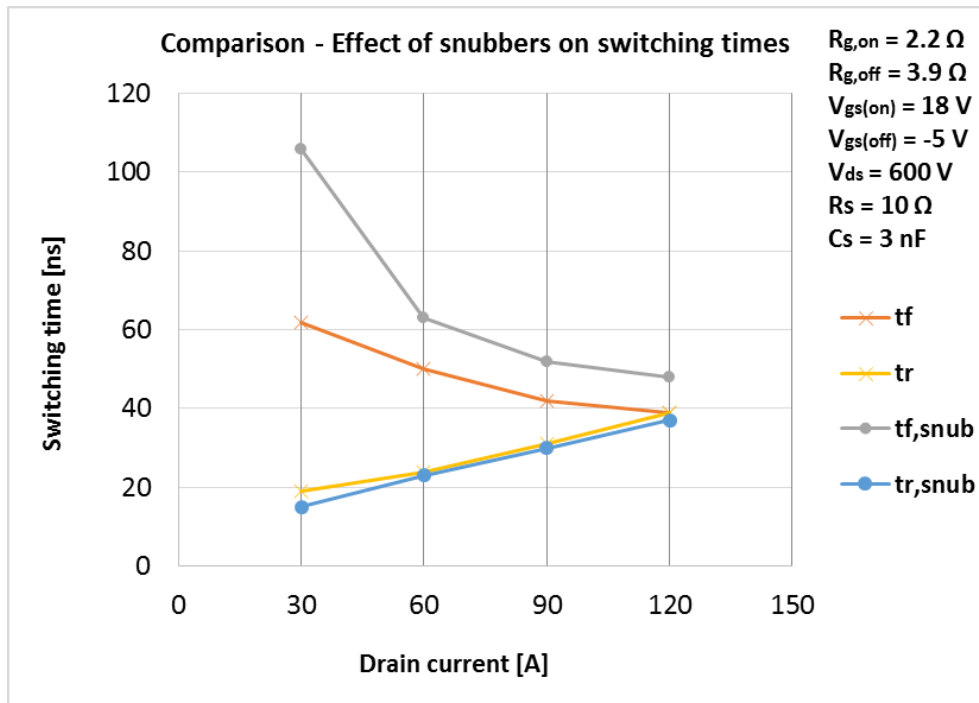


Figure 7.61: With snubbers – Comparison of switching times in simulation and experiment

It is clear that the turn-off snubber influences the turn-off transient more than it influences the turn-on transient. While the current rise time stays approximately the same, the current fall time is higher with snubber. This is expected, as the working principle of the turn-off snubber is to slow down the turn-off transient. However, at high drain currents the difference in current fall time is very small.

7.9.6 Comparison of Switching Losses

This section presents the switching losses obtained in simulation and experiment, and a comparison of the turn-on and turn-off switching losses. This is presented as a function of drain current in Figure 7.62. These are the switching losses before the connection of snubbers. The figure also includes the turn-on and turn-off switching losses presented in the SiC module datasheet. The switching losses denoted as “exp” are obtained through laboratory experiments, the switching losses denoted as “sim” are found through simulations in LTspice and the switching losses denoted as “dat” are presented in the SiC module datasheet.

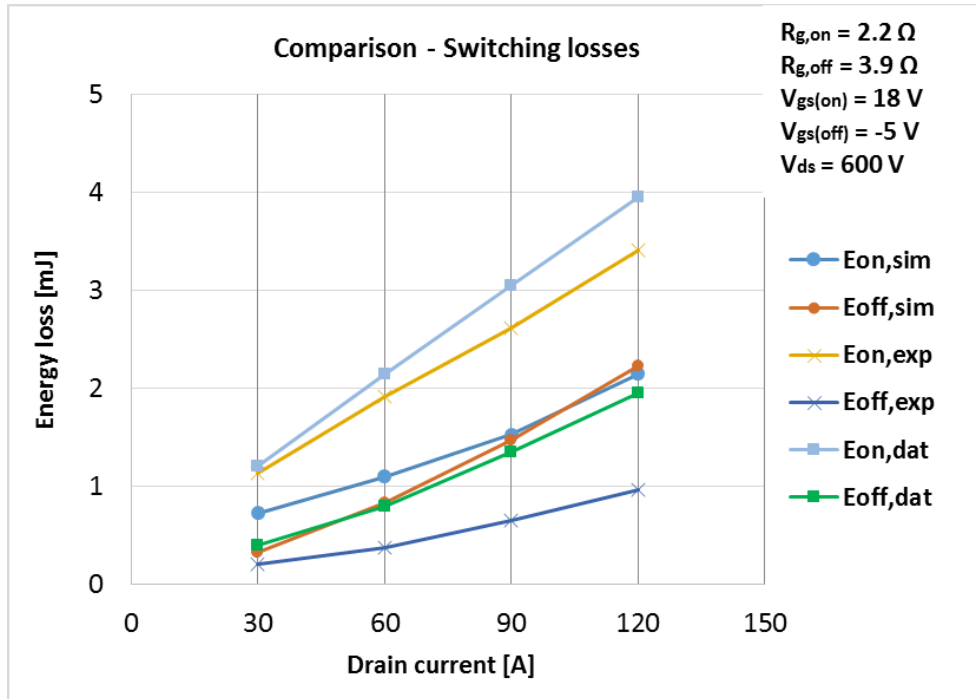


Figure 7.62: Without snubbers – Comparison of switching losses in simulation, experiment and datasheet

The switching losses obtained in simulation and experiment are very different, with higher E_{on} and lower E_{off} in the laboratory experiments. The total switching losses, however, are very similar with $E_{tot} = 4.4 \text{ mJ}$ at 120 A drain current. It is interesting to observe that the switching losses in datasheet and experiment have the same development with increased drain current. However, the switching losses in the datasheet are higher at both turn off and turn on due to higher turn-on gate resistance and no negative bias voltage at turn off.

A similar comparison is conducted in Figure 7.63, which presents the switching losses after the addition of snubbers. This figure, however, only compares the influence of the snubber on the total switching losses in the experimental part. In this figure, the following parameters are used:

- E_{on} and E_{off} represent the switching losses in the DUT without snubbers
- $E_{tot,on}$ and $E_{tot,off}$ represent the total switching losses in the turn-off snubber and the DUT, after the addition of snubbers.

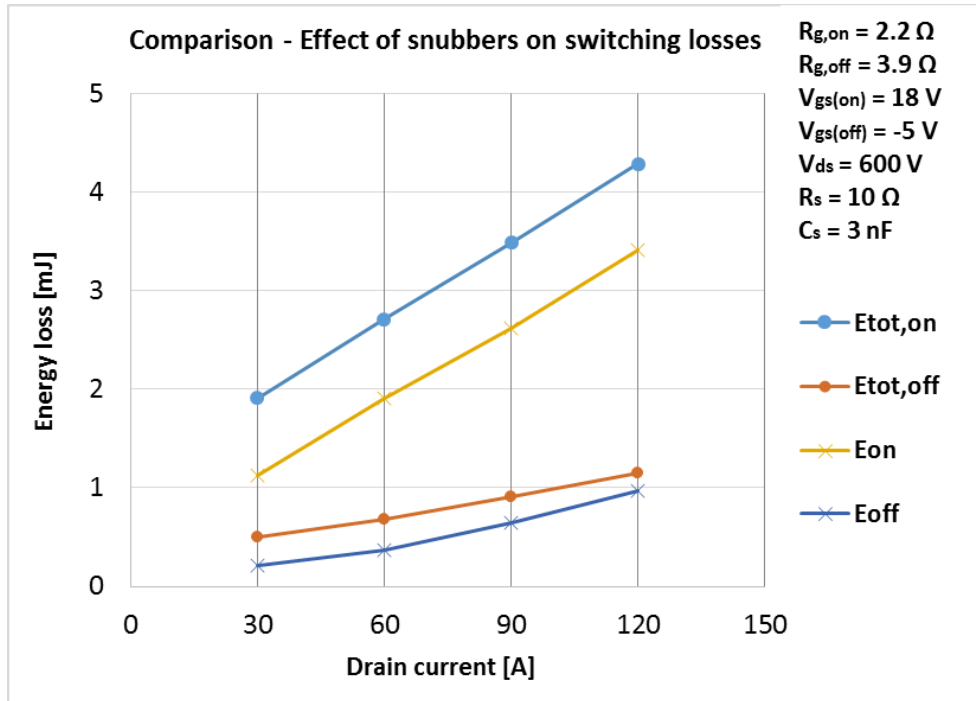


Figure 7.63: Influence of snubbers on switching losses in laboratory experiments

This shows us that the addition of snubber does not influence the total losses considerably, particularly at DUT turn off.

7.10 Total Switching Losses in a High-Frequency Switching DUT

In this thesis, the switching characteristics of the DUT have been obtained through experimental double-pulse tests. This has made it possible to investigate the switching transients, and to obtain the switching losses and the switching times. Such a double-pulse test, however, does not say much about what the power losses would be in a real high-frequency switching converter configuration. Nevertheless, the double-pulse test can be used to calculate the switching losses in such a converter configuration. In order to analyze the total switching power losses of the DUT at high switching frequencies, the following relation will be used:

$$P_{tot,sw} = f_{sw} \cdot (E_{trans,on} + E_{trans,off} + E_{snub,on} + E_{snub,off}) \quad (7.2)$$

This relation is an extension of what was deduced in (3.14), including the losses dissipated in the turn-off snubber during switching. By using the switching energy losses obtained in Figure 7.51, the total switching power losses $P_{tot,sw}$ can be calculated at a given switching frequency f_{sw} .

It is decided to investigate the total power losses in the DUT in a high-frequency switching converter configuration at different drain currents and a constant drain-to-source voltage of

600 V. Table 7.9 presents the switching power losses at a constant switching frequency of $f_{sw} = 50 \text{ kHz}$. It includes information on where the switching losses are dissipated.

Table 7.9: Total switching losses in the DUT at $f_{sw} = 50 \text{ kHz}$ and $V_{ds} = 600 \text{ V}$

| I_d [A] | $P_{trans,off}$ [W] | $P_{trans,on}$ [W] | $P_{snub,off}$ [W] | $P_{snub,on}$ [W] | P_{tot} [W] |
|-----------|---------------------|--------------------|--------------------|-------------------|---------------|
| 30 | 13.5 | 74 | 11.5 | 21.5 | 120.5 |
| 60 | 18.5 | 113.5 | 15.5 | 22 | 169.5 |
| 90 | 30 | 153 | 15.5 | 21.5 | 220 |
| 120 | 42 | 193 | 15.6 | 21.5 | 272.1 |

A similar analysis was conducted in the specialization project [16]. The total switching losses in Table 7.9 are lower than what was found in the specialization project for all drain currents higher than 30 A. The total losses in Table 7.9 are lower because the turn-off and turn-on gate resistances are half the size of what was used in the specialization project. In addition, the turn-off snubber influences the turn-off transient by reducing the turn-off losses in the DUT.

It is found in Table 7.9 that if the drain current is increased by a factor of 4 from 30 A to 120 A, the total switching losses P_{tot} increase with a factor of approximately 2.25. The total switching power losses in the transistor itself at the drain current rating of 120 A is 235 W. In the SiC module datasheet, it is stated that the maximum power dissipation in the module is 780 W [38]. Thus, the switching losses in Table 7.9 are well below the safety limit. It is also important to notice that the total switching losses in the turn-off snubber at the current rating of 120 A are approximately 37 W. This means that the snubber resistor should have a power rating of minimum 40 W in order for the snubber circuit to operate safely in converter mode.

These results can be compared with the total switching losses in a state-of-the-art IGBT half-bridge module. The SKM 400GB125D ultrafast half-bridge module from SEMIKRON is chosen for comparison [74]. The switching power losses at 120 A drain current and 600 V drain-to-source voltage are given in Table 7.10.

Table 7.10: Total switching losses in a state-of-the-art IGBT at $f_{sw} = 50 \text{ kHz}$ and $V_{ds} = 600 \text{ V}$

| I_d [A] | $P_{trans,off}$ [W] | $P_{trans,on}$ [W] | P_{tot} [W] |
|-----------|---------------------|--------------------|---------------|
| 120 | 400 | 650 | 1050 |

The total switching losses in a single IGBT transistor switching at $f_{sw} = 50 \text{ kHz}$ are about 4 times higher than what was found for the DUT, including snubbers. It is thus shown in both simulation and experiment that SiC modules should replace IGBT modules in high-frequency

applications. The possibility of switching at high frequencies makes it possible to reduce the size of all passive components, leading to a more compact design. In addition, the low switching losses in SiC MOSFETs compared to in Si IGBTs would lead to a much smaller heatsink and thereby a more compact converter.

8. Conclusion and Scope of Further Study

8.1 Conclusion

The master's thesis resulted in important conclusions related to double-pulse testing of SiC modules in simulation and laboratory experiment. The most important findings of the thesis are listed below:

- A theoretical efficiency comparison of three-phase inverters consisting of available state-of-the-art SiC MOSFET half-bridge modules and a state-of-the-art Si IGBT module has been conducted. The comparison considered conduction and switching losses in the transistors, while the gate driver and diode losses were neglected. At a DC voltage of 600 V, a load current of 100 A RMS and a switching frequency of 50 kHz, it was shown that all the SiC modules had an inverter efficiency of 98 % and higher. In comparison, the Si IGBT module had an inverter efficiency of about 93 %.
- The thesis has discussed the SiC MOSFET and all that needs to be considered when building a laboratory test circuit for such a device. This includes minimization of stray inductance, using adapted bus bar design and suitable DC-link capacitors. For security reasons, the importance of galvanic isolation in power supplies and measuring instruments was thoroughly discussed and underlined. The measuring instruments in a double-pulse test have to be carefully tested and found suitable for their purpose. As the switching transients have to be measured on a timescale of nanoseconds, it is important to measure the relative delay between different measuring instruments. If not, experimental switching loss calculations will be false.
- The load inductor in the double-pulse test was chosen to have an air core. It was found that the load inductor should not be too large, as the di/dt decreases with both inductance and DC resistance. Thus, a 250 μH air-core load inductor was chosen.
- LTspice simulation results from a double-pulse test of the BSM120D12P2C005 SiC half-bridge module from Rohm was presented. The realistic circuit design, involving stray inductance and series resistance, has been explained and justified. Results from double-pulse tests at 600 V drain-to-source voltage and 30 A, 60 A, 90 A and 120 A drain currents have been presented. An evaluation of the impact of gate resistance on switching times and switching losses was conducted, which showed that switching losses are close to proportional to the gate resistance. The influence of snubber circuits on switching characteristics was investigated, and it was found that the location of the

stray inductance has a big influence on whether snubbers help improve the switching characteristics, or not. The addition of a DC snubber and a turn-off snubber were found to have the desired influence on the DUT switching transients in simulation.

- The influence of the measuring instruments on the switching characteristics was analyzed through laboratory experiment. It was found that the stray inductance in the voltage probe could influence the switching transient. All measuring instrument should have a bandwidth that exceeds the high-frequency components of the switching transients for the results to be accurate.
- The influence of gate resistors on switching characteristics and switching losses was investigated through laboratory experiments. It was found that lower gate resistance gives faster switching, but higher switching stresses on the DUT. If the gate resistance is doubled, the switching power losses are almost doubled.
- A short-circuit protection was implemented in the gate driver. The performance of the SCP was tested at different conditions in order to get the desired behavior. It was experienced that an SCP for double-pulse testing has to be extremely fast, especially at high DC voltages. Thus, modifications to the theoretical SCP circuit had to be made. The final version of the SCP system showed successful results, with quick reaction and a safe and soft DUT turn off.
- The switching characteristics of the BSM120D12P2C005 SiC Power Module from Rohm Semiconductor were obtained through a standard double-pulse test. Extensive voltage overshoot and long-lasting ringing occurred at DUT turn off due to stray inductance inside the module and in other parts of the test circuit. Simulations in LTspice IV suggested two different snubber circuits to improve the turn-off characteristics. It is shown through laboratory experiments that the duration of the parasitic ringing is reduced by 60 % by implementing a DC snubber circuit. The DC snubber did not influence switching times or switching losses. However, the stray inductance inside the module still caused extensive voltage overshoot during DUT turn off. It was found that the addition of an RC turn-off snubber reduces the voltage overshoot by 40 % as well as reducing the duration of the parasitic ringing by additional 65 %, resulting in a total duration reduction of 85 % at 600 V drain-to-source voltage and 90 A drain current.
- At DUT turn on, it was found that the addition of a DC snubber reduces the ringing duration by 43 % without influencing the switching times or switching losses. The

turn-off snubber, on the other hand, influences the turn-on transient in a bad manner by introducing higher and wider current overshoot. The current overshoot was found to be close to independent of drain current. This was as expected, as the reverse-recovery current from the SiC SBD is close to independent of drain current.

- The switching losses in the circuit were found through both laboratory experiment and simulation, and it was found that the implementation of snubber circuits does not influence the total switching losses significantly. The total turn-off switching losses (including snubber losses) increase by a small margin of approximately 18 % after the addition of snubber circuits at 600 V 120 A. The turn-on switching losses are a little more influenced by the turn-off snubber, as the current overshoot increases. The total turn-on switching losses increase by approximately 25 % at 600 V 120 A. In total, the switching losses increase by approximately 24 % due to the implementation of two snubber circuits. However, the snubber circuits help to achieve acceptable switching characteristics, extremely fast switching and low overall switching losses.
- The total switching losses in the DUT and snubbers at 600 V 120 A were found to be 75 % lower than those of a state-of-the-art Si IGBT at a switching frequency of 50 kHz. Thus, it is possible to achieve good switching characteristics and much lower losses with a SiC MOSFET than with an Si IGBT. High-frequency switching with low losses using SiC MOSFETs and snubbers could be the solution to a more compact converter design.

8.2 Scope of Further Study

The work done in the master's thesis has led to promising results regarding the use of SiC half-bridge modules in power converters. Fast switching and low switching stresses were obtained after the addition of snubbers. Even though most of the goals for the master's thesis were reached successfully, there is still a lot of aspects that should be analyzed:

- The next step will be to continue the work from the master's thesis. As the SiC module is now working as desired at room temperature, it would be interesting to test the DUT in high-temperature operation through double-pulse tests. For the SiC module to be suitable for marine applications, it should be able to handle high temperatures very well.
- The main objective of Rolls-Royce Marine Trondheim is to design and build a full SiC three-phase inverter, by implementing three SiC modules. Such a converter design introduces new challenges that were not seen in the specialization project. A three-

phase inverter demands a much more complex control system, as six different MOSFETs have to be controlled simultaneously. Thus, a pulse-width modulation (PWM) system must be implemented. The risk of shoot through has to be avoided by considering blanking time and dead time.

- As a three-phase inverter contains six high-frequency switching SiC MOSFETs, it is important to dimension a suitable heatsink. In the double-pulse test, the heat removal is taken care of by reducing the double-pulse frequency. This will not be possible in a three-phase inverter.
- In the master's thesis, a theoretical efficiency comparison of an IGBT-based three-phase inverter and SiC MOSFET-based three-phase inverters was conducted. It would be interesting to conduct the same kind of comparison through laboratory experiments.
- The implementation of two RC snubber circuits proved to be successful in improving the switching characteristics of the DUT in the double-pulse test. However, the same kind of snubber circuit could be unsuccessful in a bridge configuration. If a turn-off snubber is connected across both transistors in a bridge leg, this could cause extensive current overshoot due to capacitive discharge during switching. Thus, the influence of turn-off snubbers used in a bridge configuration should be investigated through simulations in LTspice. An alternative could be to test and implement the Undeland snubber for bridge configurations [6].

9. References

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Appendix A – Electrical Clearance

When making a PCB or a bus bar, it is important to dimension the clearance distance between two leads/conductors with different potentials properly. As the voltage potential between to leads in a power electronic circuit might be large, the possibility of shoot through is present. Table A.1 gives the minimum spacing between to conductors.

Table A.1: Electrical clearance [67]

| Voltage Between Conductors (DC or AC Peaks) | Minimum Spacing | | | | | | |
|---|-------------------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | Bare Board | | | | Assembly | | |
| | B1 | B2 | B3 | B4 | A5 | A6 | A7 |
| 0-15 | 0.05 mm [0.00197 in] | 0.1 mm [0.0039 in] | 0.1 mm [0.0039 in] | 0.05 mm [0.00197 in] | 0.13 mm [0.00512 in] | 0.13 mm [0.00512 in] | 0.13 mm [0.00512 in] |
| 16-30 | 0.05 mm [0.00197 in] | 0.1 mm [0.0039 in] | 0.1 mm [0.0039 in] | 0.05 mm [0.00197 in] | 0.13 mm [0.00512 in] | 0.25 mm [0.00984 in] | 0.13 mm [0.00512 in] |
| 31-50 | 0.1 mm [0.0039 in] | 0.6 mm [0.024 in] | 0.6 mm [0.024 in] | 0.13 mm [0.00512 in] | 0.13 mm [0.00512 in] | 0.4 mm [0.016 in] | 0.13 mm [0.00512 in] |
| 51-100 | 0.1 mm [0.0039 in] | 0.6 mm [0.024 in] | 1.5 mm [0.0591 in] | 0.13 mm [0.00512 in] | 0.13 mm [0.00512 in] | 0.5 mm [0.020 in] | 0.13 mm [0.00512 in] |
| 101-150 | 0.2 mm [0.0079 in] | 0.6 mm [0.024 in] | 3.2 mm [0.126 in] | 0.4 mm [0.016 in] | 0.4 mm [0.016 in] | 0.8 mm [0.031 in] | 0.4 mm [0.016 in] |
| 151-170 | 0.2 mm [0.0079 in] | 1.25 mm [0.0492 in] | 3.2 mm [0.126 in] | 0.4 mm [0.016 in] | 0.4 mm [0.016 in] | 0.8 mm [0.031 in] | 0.4 mm [0.016 in] |
| 171-250 | 0.2 mm [0.0079 in] | 1.25 mm [0.0492 in] | 6.4 mm [0.252 in] | 0.4 mm [0.016 in] | 0.4 mm [0.016 in] | 0.8 mm [0.031 in] | 0.4 mm [0.016 in] |
| 251-300 | 0.2 mm [0.0079 in] | 1.25 mm [0.0492 in] | 12.5 mm [0.4921 in] | 0.4 mm [0.016 in] | 0.4 mm [0.016 in] | 0.8 mm [0.031 in] | 0.8 mm [0.031 in] |
| 301-500 | 0.25 mm [0.00984 in] | 2.5 mm [0.0984 in] | 12.5 mm [0.4921 in] | 0.8 mm [0.031 in] | 0.8 mm [0.031 in] | 1.5 mm [0.0591 in] | 0.8 mm [0.031 in] |
| > 500 See para. 6.3 for calc. | 0.0025 mm /volt | 0.005 mm /volt | 0.025 mm /volt | 0.00305 mm /volt | 0.00305 mm /volt | 0.00305 mm /volt | 0.00305 mm /volt |

B1 - Internal Conductors

B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]

B3 - External Conductors, uncoated, over 3050 m [10,007 feet]

B4 - External Conductors, with permanent polymer coating (any elevation)

A5 - External Conductors, with conformal coating over assembly (any elevation)

A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]

A7 - External Component lead termination, with conformal coating (any elevation)

In the master's thesis, Table A.1 was used during the making of the bus bar. The bus bar copper plates lie under the category "B2 – uncoated, external conductor at sea level". The minimum clearing distance d_{min} is given by:

$$d_{min} = 2,5mm + 0,005mm \cdot (V_{max} - 500V) \quad (\text{A.1})$$

As the maximum applied voltage in the laboratory experiment is 600 V, it was decided to dimension the clearance distance for $V_{max} = 1000V$ in order to take into consideration the overvoltages during switching. Thus, it was chosen to use a clearance distance of 5mm.

A detailed explanation of the bus bar design used in the laboratory experiment is shown in Figure A.1.

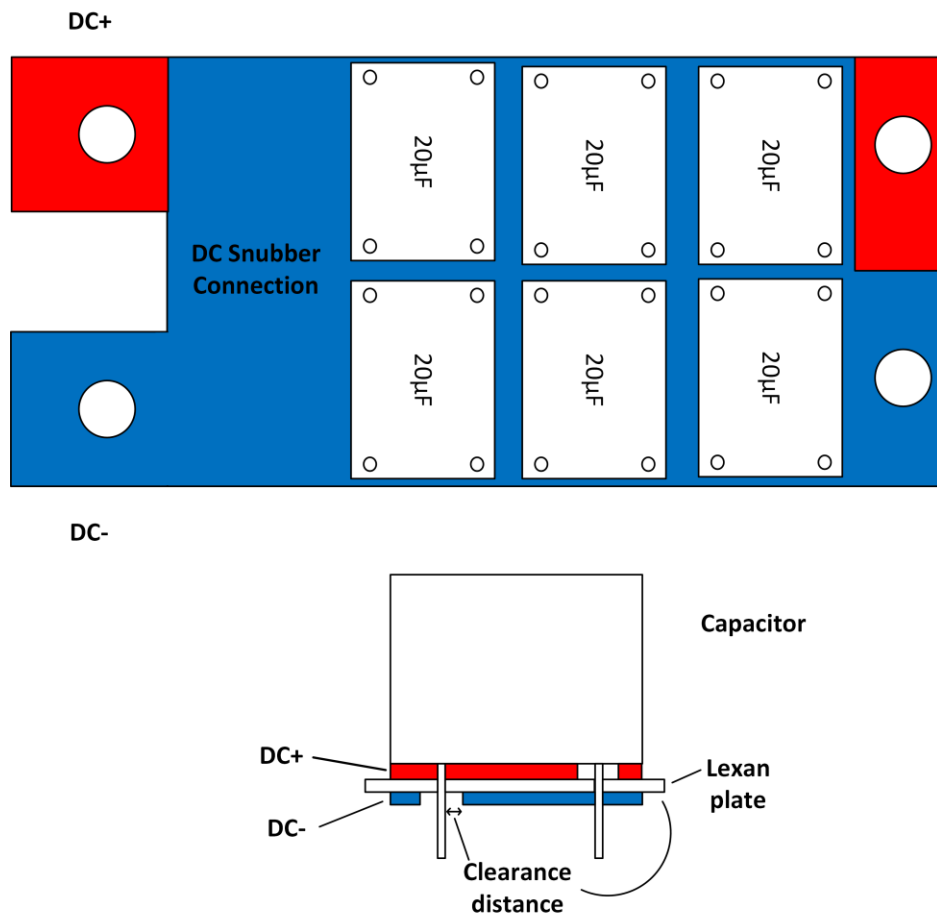


Figure A.1: Bus bar design including electrical clearance

The electrical clearance distance, which is specified in Figure A.1, is important to consider in proximity to capacitor pins and on the edges of the copper plates.

Appendix B – Circuit Diagrams in CadSoft Eagle

Figure B.1 and Figure B.2 present circuit diagrams in Cadsoft Eagle for the SCP and the DC/DC converters of the lower driver, explained in Section 5.1.3.

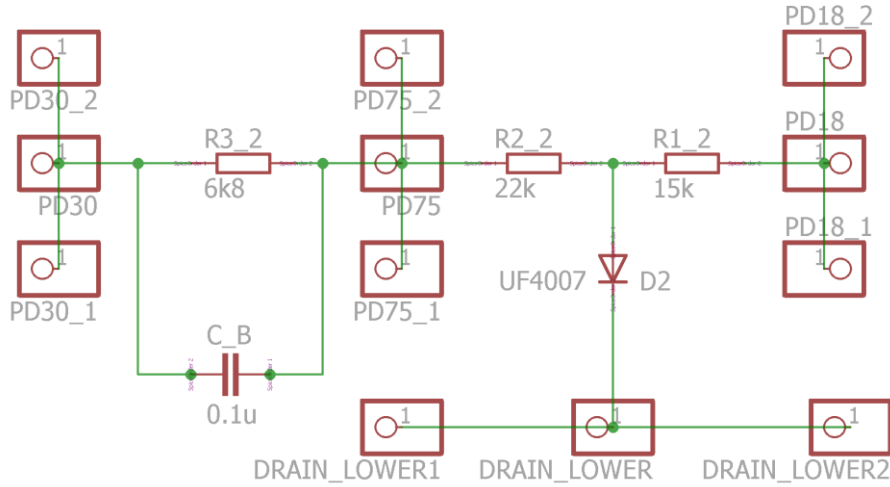


Figure B.1: CadSoft Eagle – SCP for lower driver

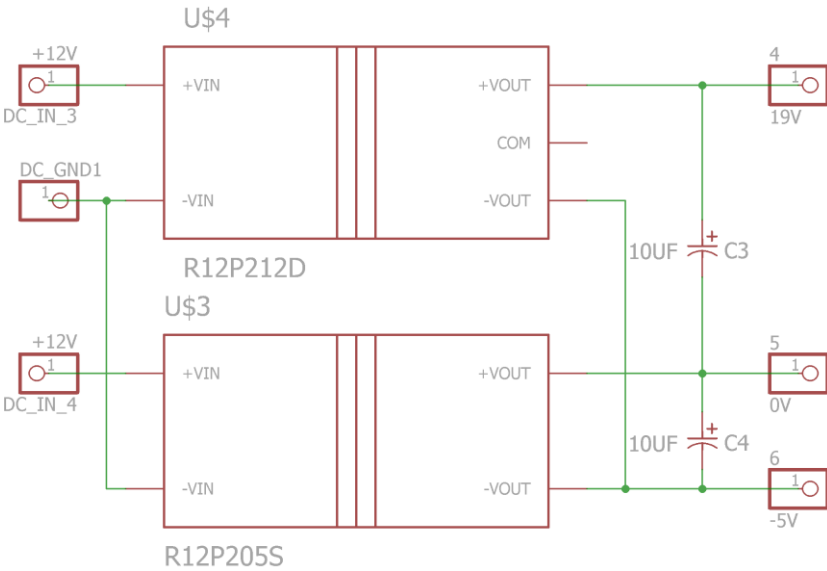


Figure B.2: CadSoft Eagle – SCP for lower driver

Appendix C – Bill of Materials (BOM)

Appendix C.1– BOM for the Gate Driver Circuit Board

Table C.1 presents the complete BOM for the gate driver circuit board and all required components. This includes the components needed in the PCB design for galvanic isolation and SCP for both the upper and the lower driver. This was presented in Figure 5.9.

Table C.1: BOM for the gate driver circuit

| Component | Description | Value | Rating | Qty | Manufacturer | Name | Order number |
|----------------------|---------------------------|----------------|--------------------|-----|--------------|----------------|------------------|
| R_1, R_{1_2} | SCP resistor | 15 k Ω | 30 V | 2 | - | - | - |
| R_2, R_{2_2} | SCP resistor | 22 k Ω | 30 V | 2 | - | - | - |
| R_3, R_{3_2} | SCP resistor | 6.8 k Ω | 30 V | 2 | - | - | - |
| C_{BL}, C_B | SCP capacitor | 0.1 μ F | 30 V | 2 | - | - | - |
| D_1, D_2 | SCP diode | - | 1000 V | 2 | Vishay | UF4007 | Farnell: 1836349 |
| U\$2, U\$3 | DC/DC converter | +5 V | 2 W | 2 | Recom | R12P205S | Farnell: 2440279 |
| U\$1, U\$4 | DC/DC converter | \pm 12 V | 2 W | 2 | Recom | R12P212D | Farnell: 2440280 |
| C_1, C_2, C_3, C_4 | Decoupling capacitor | 10 μ F | 50 V _{DC} | 4 | Jamicon | SSR100MIHE07VU | Elfa: 167-00-587 |
| | Zener diode | 13 V | 1.3 W | 4 | Vishay | BZX85C13 | Elfa: 300-30-862 |
| BW9499H | Gate driver circuit board | - | - | 1 | Rohm | BW9499H | - |

Appendix C.2 – BOM for the Bus Bar

Table C.2 presents the complete BOM for the PCB bus bar design described in Figure 5.11, including the DC snubber in Figure 7.30.

Table C.2: BOM for bus bar

| Component | Description | Value | Rating | Qty | Manufacturer | Name | Order number |
|--------------------------------|----------------------|-------------------|----------------------|-----|-----------------|-------------------------------|------------------|
| C_1 | DC snubber capacitor | 1.8 nF | 2000 V_{DC} | 1 | – | PS1n8J A3 | – |
| R_1 | DC snubber resistor | $10\ \Omega$ | 10 W | 1 | BI technologies | BPR10100J | Farnell: 9432442 |
| R_2 | DC snubber resistor | $10\ \Omega$ | 20 W | 2 | Vishay | RTO020F10R00FTE3 (RTO series) | Farnell: 2144976 |
| $C_2, C_3, C_4, C_5, C_6, C_7$ | Bulk capacitor | $20\ \mu\text{F}$ | 900 V_{DC} | 6 | Vishay | MKP1848 620 094P4 | Farnell: 1791635 |

Appendix C.3 – BOM for Turn-Off Snubber

Table C.3 presents the complete BOM for the turn-off snubber, which was presented in Figure 7.35.

Table C.3: BOM for turn-off snubber

| Component | Description | Value | Rating | Qty | Manufacturer | Name | Order number |
|-----------|----------------------------|---------------|----------------------|-----|-----------------|---------------------|------------------|
| R_5 | Turn-off snubber resistor | $10\ \Omega$ | 10 W | 1 | BI technologies | BPR10100J | Farnell: 9432442 |
| C_5 | Turn-off snubber capacitor | 1 nF | 2000 V_{DC} | 3 | WIMA | MKP01U011003C00KSSD | Elfa: 165-66-905 |

Appendix D – Additional LTspice Simulations

The additional simulations used in Chapter 6 are presented on the following pages.

Appendix D.1 – Turn-Off Switching Characteristics without Snubbers

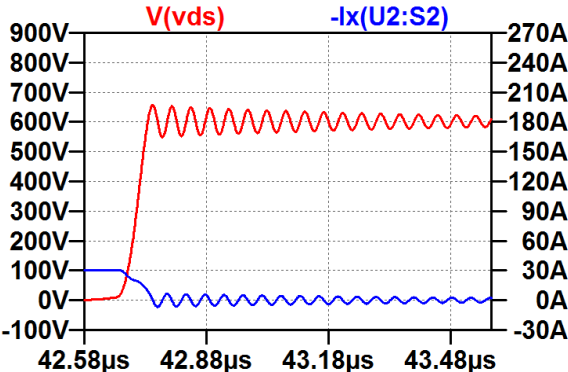


Figure D.1: Simulation – Turn-off characteristics at 600 V 30 A

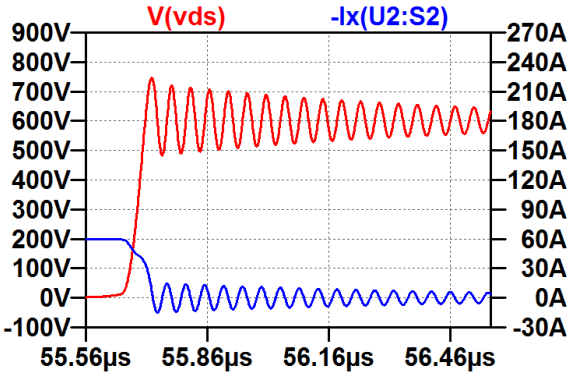


Figure D.2: Simulation – Turn-off characteristics at 600 V 60 A

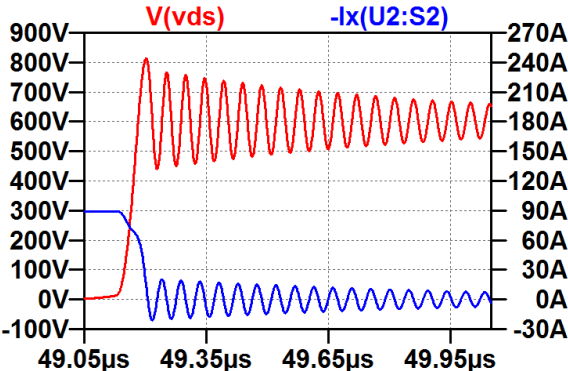


Figure D.3: Simulation – Turn-off characteristics at 600 V 90 A

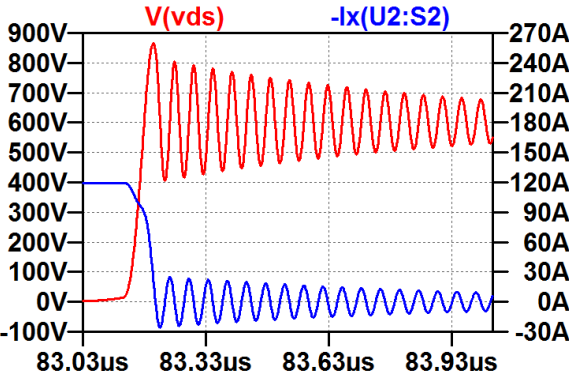


Figure D.4: Simulation – Turn-off characteristics at 600 V 120 A

Appendix D.2 – Turn-On Switching Characteristics without Snubbers

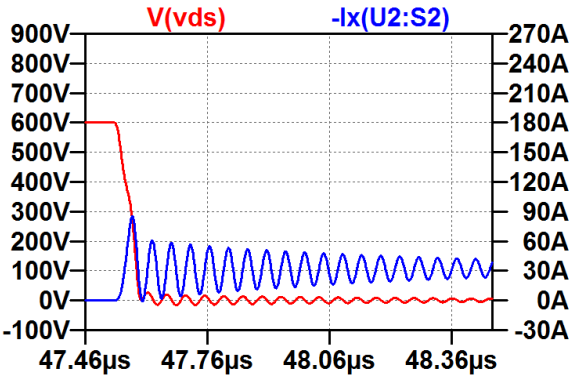


Figure D.5: Simulation – Turn-on characteristics at 600 V 30 A

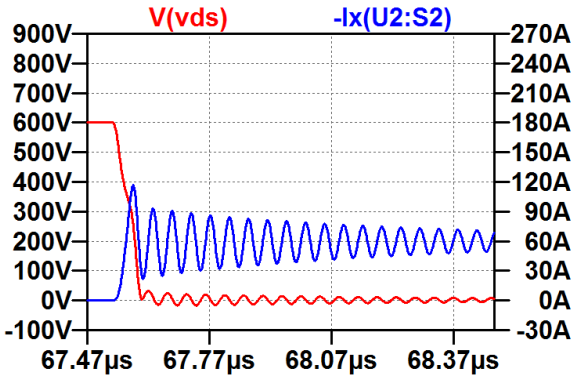


Figure D.6: Simulation – Turn-on characteristics at 600 V 60 A

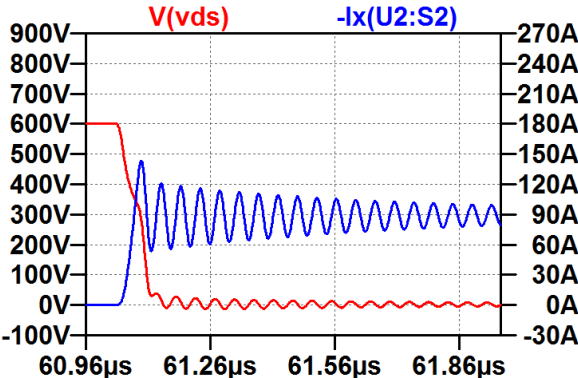


Figure D.7: Simulation – Turn-on characteristics at 600 V 90 A

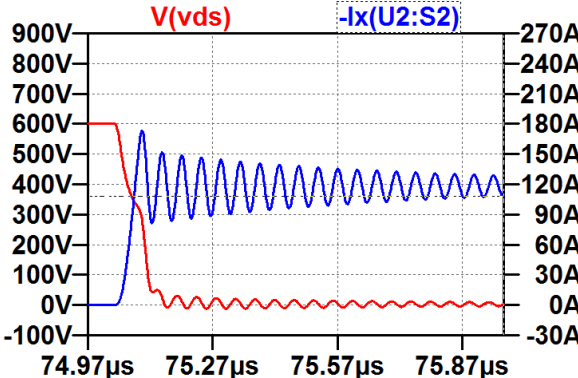


Figure D.8: Simulation – Turn-on characteristics at 600 V 120 A

Appendix D.3 – Turn-Off Switching Characteristics with DC Snubber

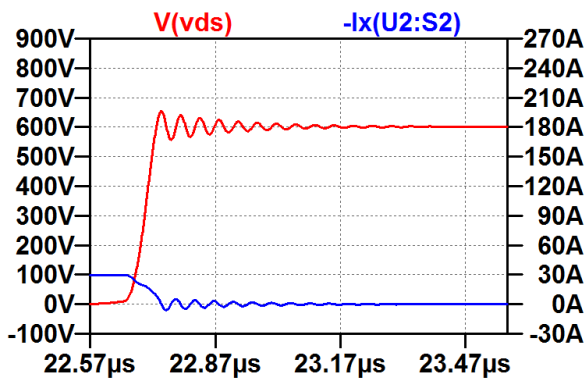


Figure D.9: Simulation – Effect of DC snubber at 600 V 30 A turn off

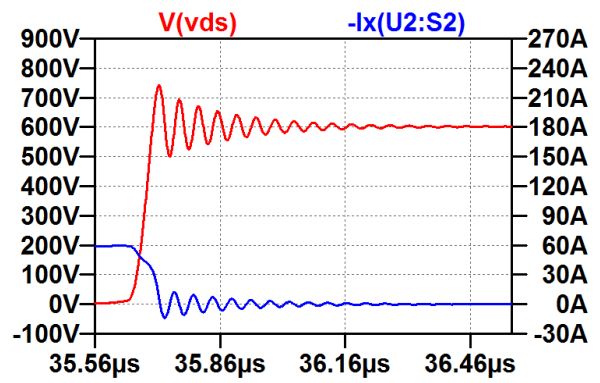


Figure D.10: Simulation – Effect of DC snubber at 600 V 60 A turn off

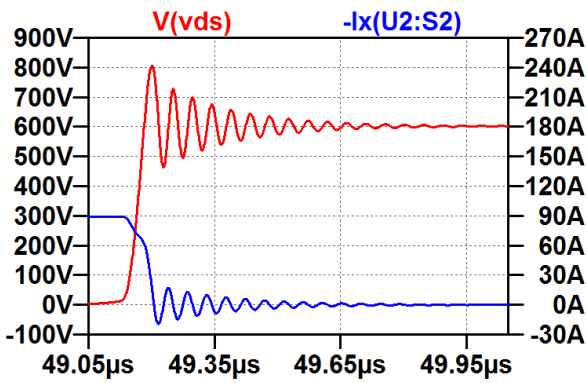


Figure D.11: Simulation – Effect of DC snubber at 600 V 90 A turn off

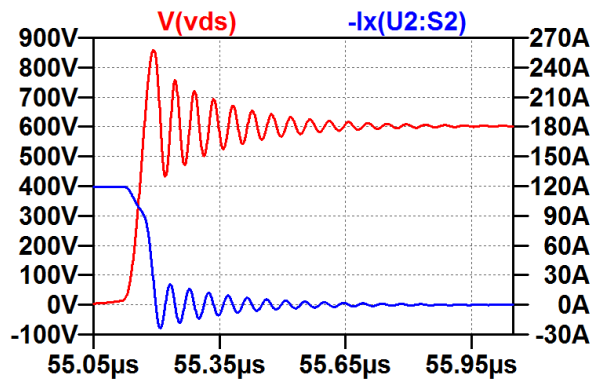


Figure D.12: Simulation – Effect of DC snubber at 600 V 120 A turn off

Appendix D.4 – Turn-On Switching Characteristics with DC Snubber

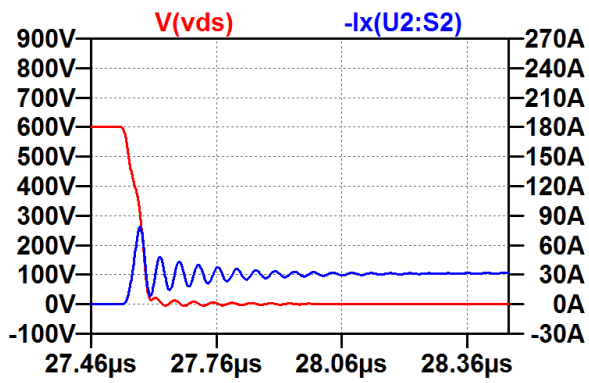


Figure D.13: Simulation – Effect of DC snubber at 600 V 30 A turn on

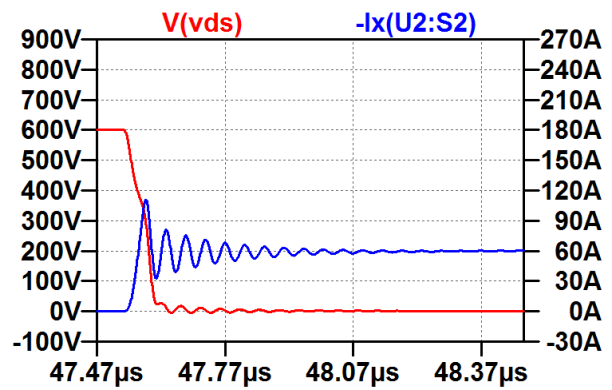


Figure D.14: Simulation – Effect of DC snubber at 600 V 60 A turn on

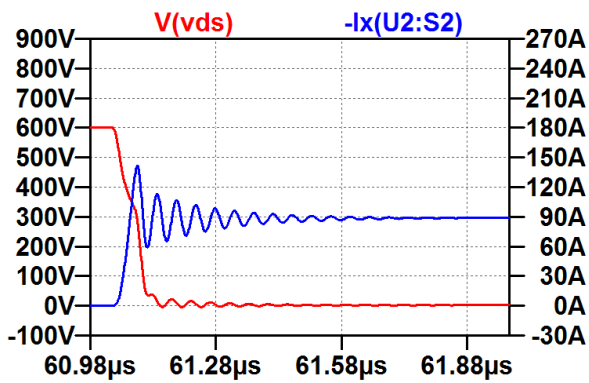


Figure D.15: Simulation – Effect of DC snubber at 600 V 90 A turn on

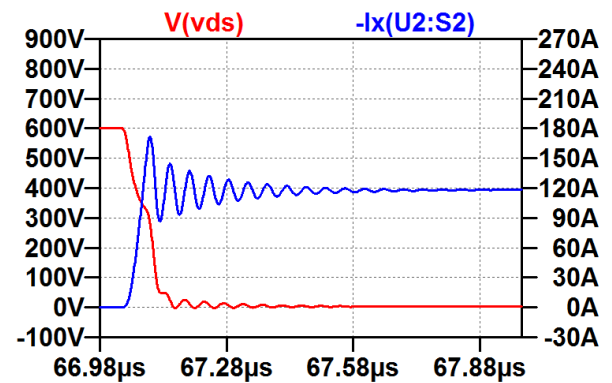


Figure D.16: Simulation – Effect of DC snubber at 600 V 120 A turn on

Appendix D.5 – Turn-Off Switching Characteristics with Turn-Off Snubber

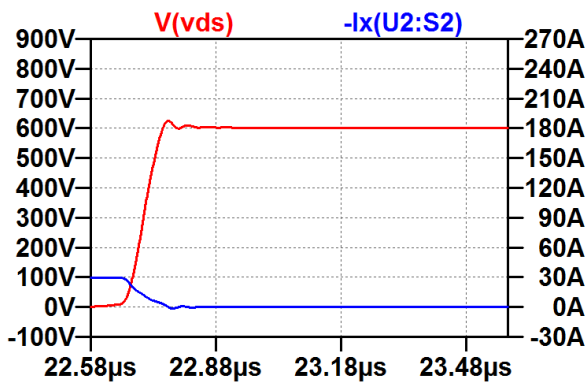


Figure D.17: Simulation – Effect of turn-off snubber at 600 V 30 A turn off

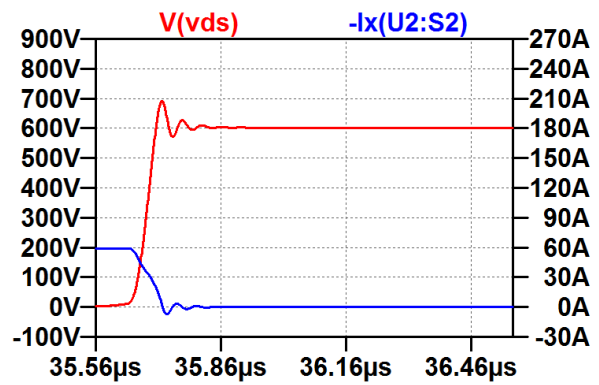


Figure D.18: Simulation – Effect of turn-off snubber at 600 V 60 A turn off

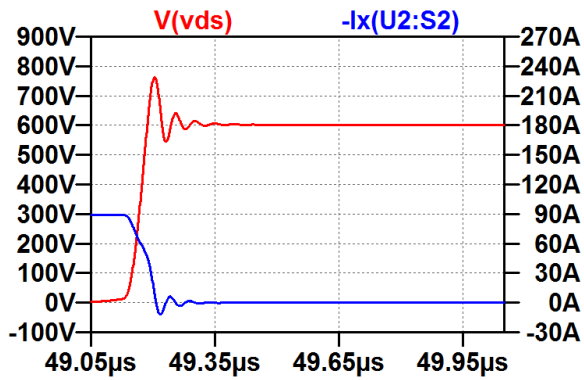


Figure D.19: Simulation – Effect of turn-off snubber at 600 V 90 A turn off

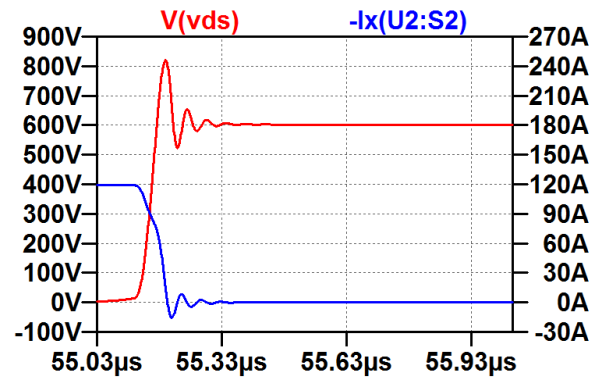


Figure D.20: Simulation – Effect of turn-off snubber at 600 V 120 A turn off

Appendix D.6 – Turn-On Switching Characteristics with Turn-Off Snubber

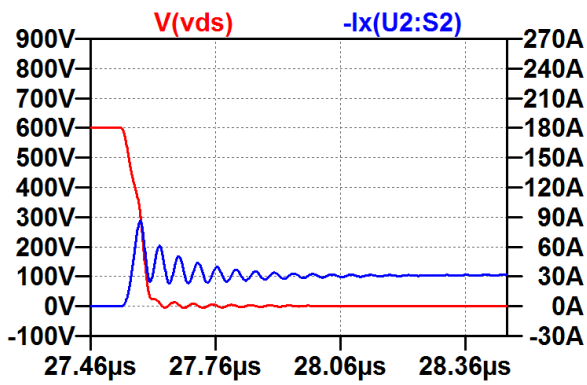


Figure D.21: Simulation – Effect of turn-off snubber at 600 V 30 A turn on

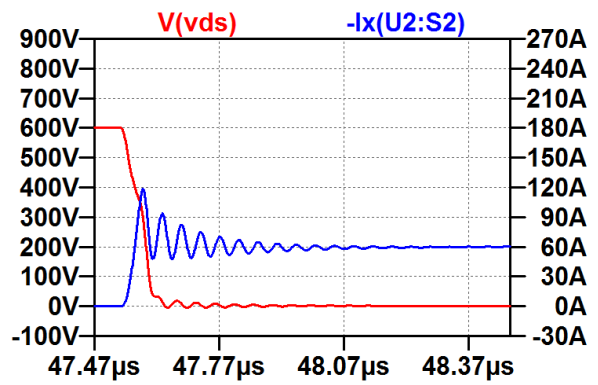


Figure D.22: Simulation – Effect of turn-off snubber at 600 V 60 A turn on

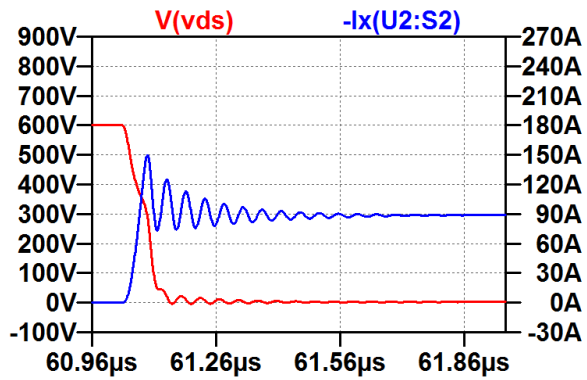


Figure D.23: Simulation – Effect of turn-off snubber at 600 V 90 A turn on

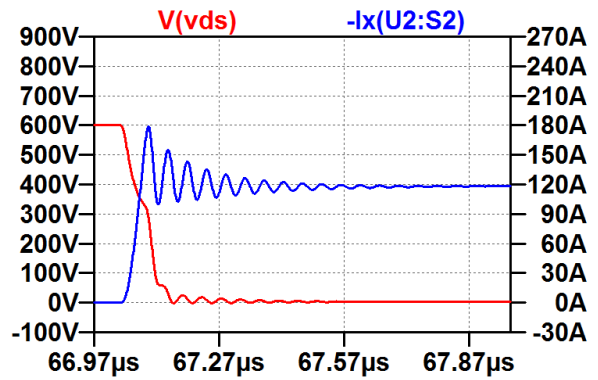


Figure D.24: Simulation – Effect of turn-off snubber at 600 V 120 A turn on

Appendix E – Additional Laboratory Results

An example of an experimental double-pulse test at 600 V drain-to-source voltage and 120 A drain current is presented in Figure E.1.

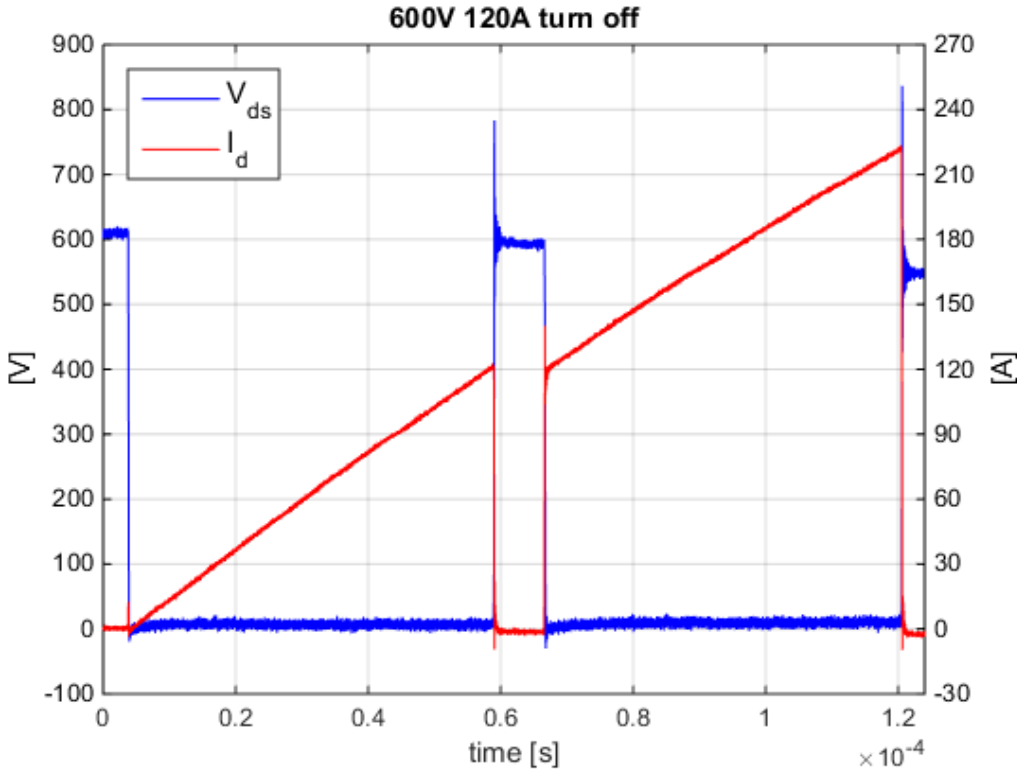


Figure E.1: Experiment – Double-pulse test at 600 V 120 A

The turn-on switching characteristics after the addition of DC snubber (Section 7.7.1) are presented for 600V drain-to-source voltage and 30 A, 60 A, 90 A and 120 A drain currents in the figures below.

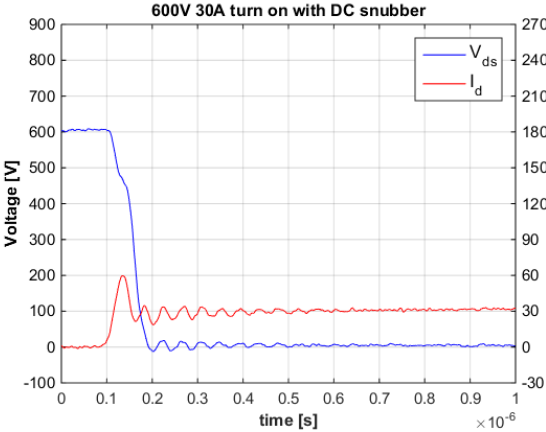


Figure E.2: Experiment – Effect of DC snubber at 600 V 30 A turn on

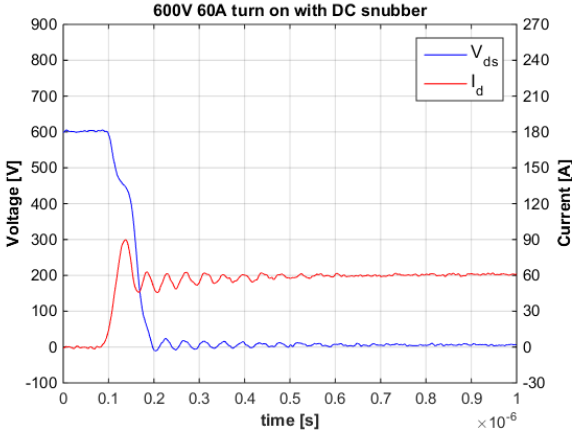


Figure E.3: Experiment – Effect of DC snubber at 600 V 60 A turn on

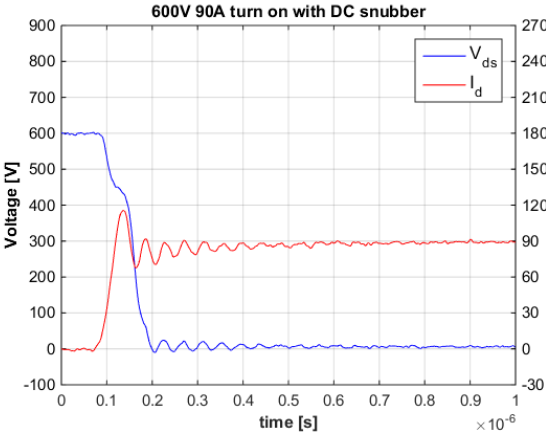


Figure E.4: Experiment – Effect of DC snubber at 600 V 90 A turn on

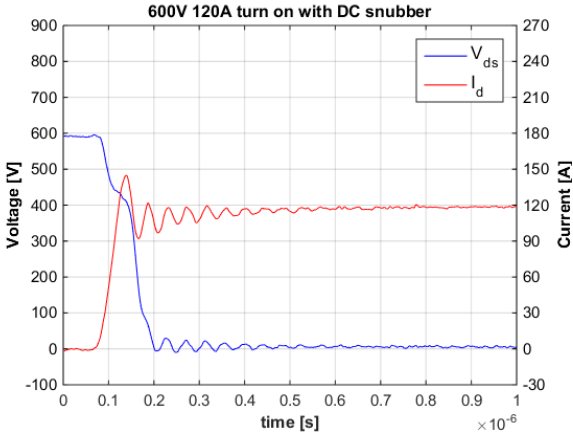


Figure E.5: Experiment – Effect of DC snubber at 600 V 120 A turn on

Appendix F – MATLAB Script

The MATLAB scripts below were used to filter the signals captured by the oscilloscope and to plot them with proper axes. The first script was used in Figure 7.2, which is a comparison of voltage probes with different bandwidths.

```
% -----  
t=linspace(0,1e-3,5e6);  
  
% Read .wfm files from oscilloscope  
% -----  
[uds1,t]=wfm2read('Turn_off_voltage_50MHz');  
% Drain-to-source voltage 50 MHz probe and time  
uds2=wfm2read('Turn_off_voltage_200MHz');  
% Drain-to-source voltage 200 MHz probe  
  
% Filtering of all signals  
% -----  
sr=length(t)/max(t);  
ff=100e6;  
wn=ff/(sr*0.5); % Cutoff frequency  
  
[B,A] = butter(2,wn); % Butterworth filter  
uds1f=filter(B,A,uds1);  
uds2f=filter(B,A,uds2);  
  
% Plot all signals as a function of time  
% -----  
tgen=t-(-0.95e-7);  
  
figure(2)  
hold on  
  
h1 = plot(tgen+2.5e-9,uds1f,'b');  
h2 = plot(tgen+2.5e-9,uds2f,'r');  
  
axis([0,10e-7,-100,900]);  
set(gca,'ytick',[-100:100:900],'ycolor','k')  
  
xlabel('time [s]')  
title('600V 90A turn off')  
ylabel('[V]')  
grid;  
  
M=[h1 h2];  
  
% Label all signals  
% -----  
A=legend(M,'V_d_s_1- 50MHz bandwidth','V_d_s_2 - 200MHz  
bandwidth','Location','SouthEast');  
set(A,'FontSize',12)
```

The second script was used in Figure 7.23, which is the DUT turn-off characteristics at 600 V 120 A.

```

% -----
t=linspace(0,1e-3,5e6);

% Read .wfm files from oscilloscope
% -----
[uds,t]=wfm2read('turn_off_600V_120A_voltage'); % Drain-to-source voltage
id_1=wfm2read('turn_off_600V_120A_current'); % Drain current

% Filtering of all signals
% -----
sr=length(t)/max(t);
ff=100e6;
wn=ff/(sr*0.5); % Cutoff frequency

[B,A] = butter(2,wn); % Butterworth filter
udsf=filter(B,A,uds);
idf_1=filter(B,A,id_1);

% Plot voltage and current as a function of time with two different axes
% -----
tgen=t-(-0.85e-7);
figure(2)

[AX,L1,L2]=plotyy(tgen,udsf,tgen,idf_1);
set(get(AX(1),'Ylabel'),'String','Voltage [V]','fontweight','bold',...
    'fontsize',12)
set(get(AX(2),'Ylabel'),'String','Current [A]','fontweight','bold',...
    'fontsize',12)
xlabel('time [s]','fontweight','bold','fontsize',12)
title('600V 120A turn off','fontweight','bold','fontsize',12)
grid;

axes(AX(1))
hold on
h1 = plot(tgen,udsf,'b');
axis([0,10e-7,-100,900]);
set(gca,'ytick',[-100:100:900],'ycolor','k','fontsize',11)
set(gca,'xtick',0:100e-9:10e-7);

axes(AX(2))
hold on
h2 = plot(tgen,idf_1,'r');
axis([0,10e-7,-30,270]);
set(gca,'ytick',[-30:30:270],'ycolor','k','fontsize',11)
set(gca,'xtick',0:100e-9:10e-7);

hold(AX(1),'on')
hold(AX(2),'on')
M=[h1 h2];

% Label all signals
% -----
ax = legend(M,'V_d_s','I_d','Location','NorthEast');
set(ax,'fontsize',13)

```

Appendix G – Pictures of the Laboratory Setup

Pictures of the laboratory setup are presented in the following figures.

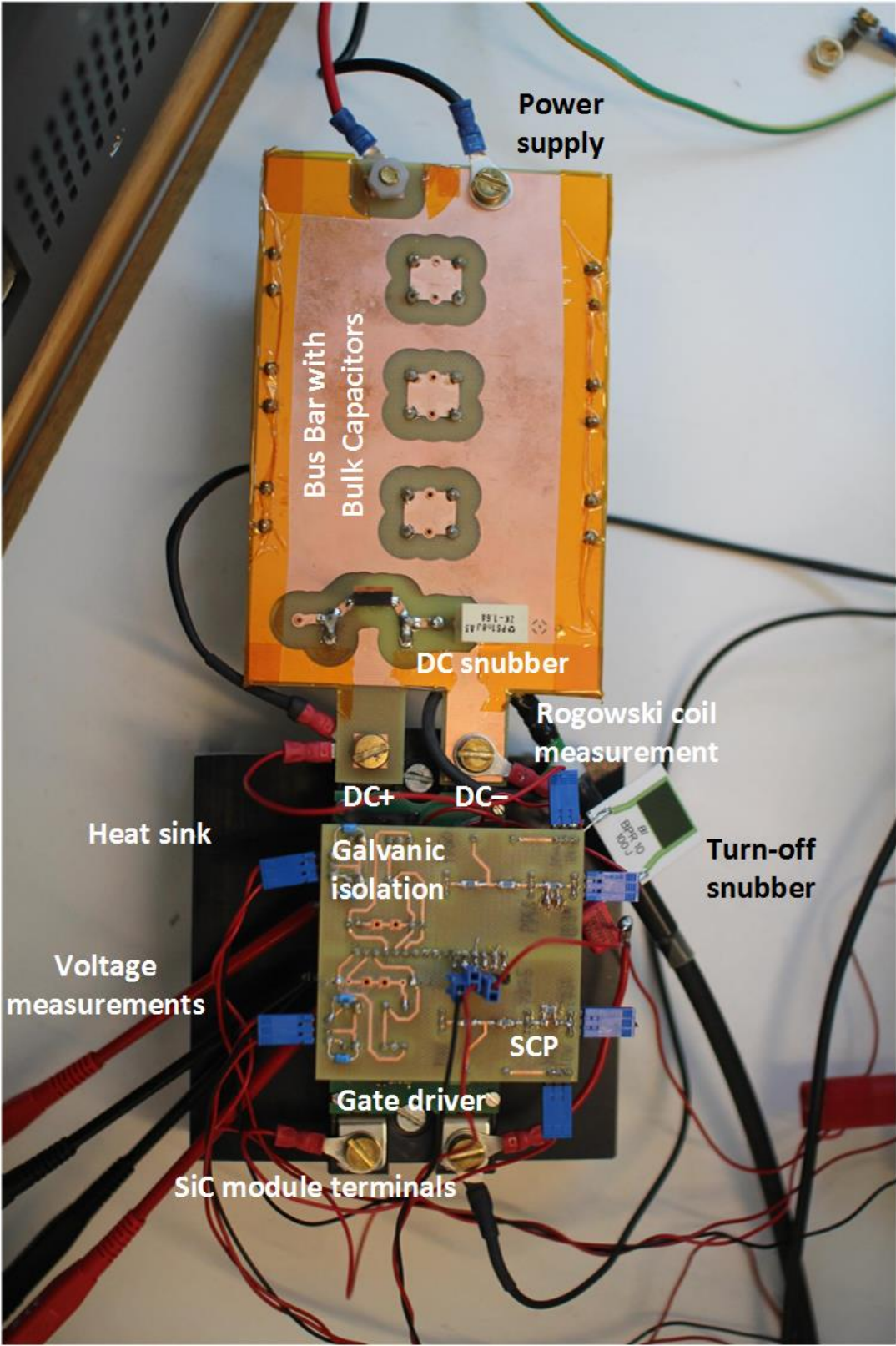


Figure G.1: Picture of the laboratory setup

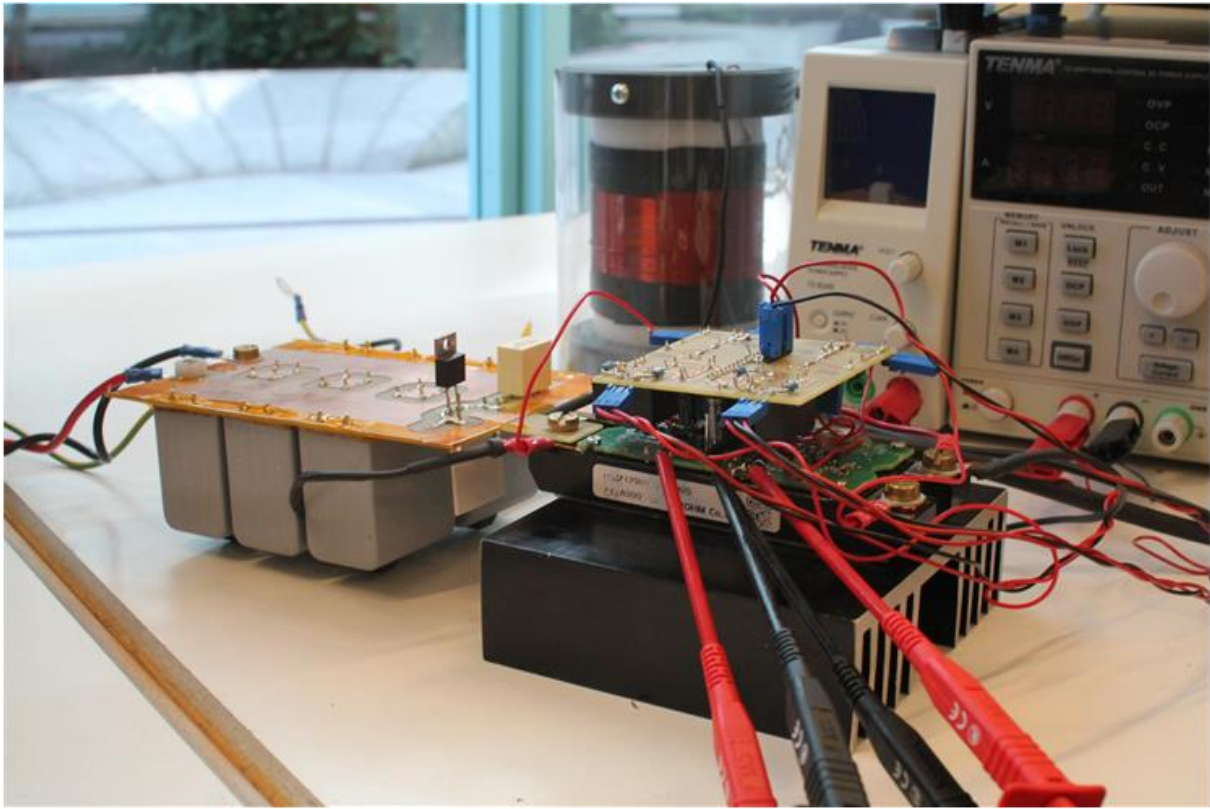
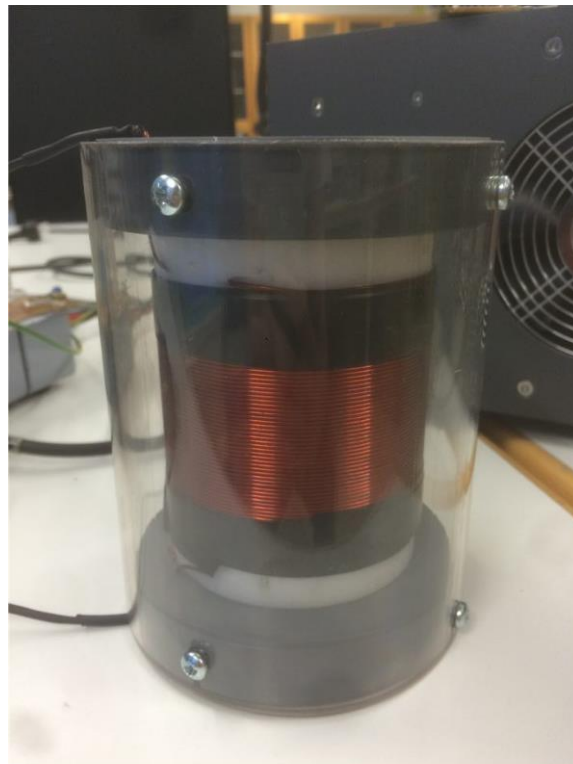


Figure G.2: Picture of the gate driver circuit board and voltage measurements



Load inductor $L=250\mu\text{H}$

Figure G.3: Picture of the load inductor

Appendix H – Scientific Paper

This appendix presents the scientific paper that was written for the PEDG 2016 conference in Vancouver, Canada. The paper was written in collaboration with my supervisors. It presents parts of the results obtained during the master's thesis, with focus on the implementation of snubber circuits to improve switching characteristics.

The paper was accepted by the PEDG conference on April 1 2016, and will be presented on June 28 2016 as a part of the conference program. The title of the scientific paper is “Experimental Evaluation of Switching Characteristics, Switching losses and Snubber Design for a Full SiC Half-Bridge Power Module”, and it is presented on the next eight pages.

Experimental Evaluation of Switching Characteristics, Switching losses and Snubber Design for a Full SiC Half-Bridge Power Module

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Abstract—This paper analyzes the switching performance of the full SiC half-bridge power module BSM120D12P2C005 from Rohm Semiconductor. It investigates if the combination of a DC snubber and a turn-off snubber helps to reduce sufficiently the electrical stresses on hard-switching power modules. Simulations in LTspice IV and laboratory experiments give the basis for the analysis. Standard double-pulse tests of the module are conducted at different drain currents. This makes it possible to analyze the switching characteristics and the total switching losses of the SiC module. Simulations in LTspice are used in order to investigate if the use of suitable snubber circuits improves the switching transients. The performance of these snubbers is tested and verified through laboratory experiments. It is shown in both simulations and laboratory experiments that a simple and well-known DC snubber circuit for half-bridge configurations attenuates ringing without reducing the voltage overshoot. In order to suppress this extensive voltage overshoot to an acceptable level during device turn off, a turn-off snubber must be added to the circuit. It is found that this solution does not increase the switching losses significantly.

Keywords—Silicon Carbide (SiC), Full SiC, Half-Bridge Module, MOSFET, Schottky Barrier Diode (SBD), Double-Pulse Test, LTspice IV, RC snubber, DC Snubber, Turn-Off Snubber, Switching Losses.

I. INTRODUCTION

The power quality in a distribution system with high penetration of distributed energy resources (DER) highly relies on power converter switching transients with low voltage and current overshoot, low EMI and little ringing. Suitable snubber circuits can help reduce such stresses and increase the output power quality during power converter switching [1] [2] [3] [4].

A great challenge in today's medium and low voltage power systems is the power converters and their considerable power losses during high-frequency switching. Power converters based on Si technology are reaching their theoretical limits and are not as efficient as desired and required [5]. SiC technology could help solve this challenge [6]. A performance evaluation from Cree Inc. states that the power losses in a DC/DC boost converter with SiC MOSFET had 99.3 % efficiency at 100 kHz, reducing the losses by 18 % from the best Si IGBT solution at 20 kHz [7].

As SiC MOSFETs have very fast switching transients compared to Si IGBTs, they introduce challenges related to voltage and current overshoot and parasitic ringing during hard-switching transients. Such overshoots can cause high electrical stresses on the power device, which at worst could be damaging. In order to reduce these stresses, snubber circuits can be designed and implemented [4].

In [8], a C-CR DC snubber is used to suppress voltage ringing in a full-SiC half-bridge configuration. This solution, however, might not always be sufficient in cases with half-bridge power modules, as significant amounts of stray inductance could be located inside the module package. An RC turn-off snubber could help reduce switching stresses on the power device to an acceptable level [9] [10]. This paper investigates if the combination of a DC snubber and a turn-off snubber helps to reduce sufficiently the electrical stresses on hard-switching power modules during switching.

II. LABORATORY SETUP

The device under test (DUT) in this laboratory experiment is the lower transistor of the BSM120D12P2C005 full SiC half-bridge Power Module from Rohm Semiconductor [11]. This is a half-bridge power module consisting of SiC MOSFET transistors with DMOS structure and SiC Schottky barrier diodes (SBD). It has a drain-to-source voltage rating of 1200 V and a drain current rating of 120 A. In order to drive this half-bridge module, the BW9499H “Gate driver circuit board for SiC Power Modules” from Rohm Semiconductor is used [12]. The driver circuit board includes two separate gate drivers, which means that it is able to drive both the upper and the lower transistor of the SiC module simultaneously. A picture of the laboratory setup is given in Fig. 1.

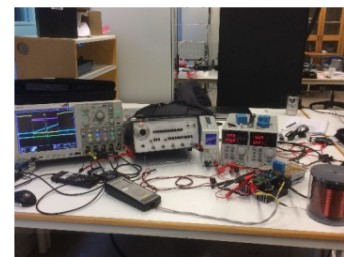


Fig. 1. Laboratory setup

III. CURRENT MEASUREMENT, SWITCHING CHARACTERISTICS AND SWITCHING LOSSES

A. Current Measurement

In order to investigate the switching characteristics and the switching losses, a double-pulse test of the DUT is conducted. A simplified figure depicting the double-pulse test circuit is presented in Fig. 2. By controlling the first pulse width of the double pulse, the current flowing through the DUT can be controlled. Thus, it is possible to analyze the turn-on and turn-off switching transients at the desired drain current. As the double pulses are supplied at a very low frequency, e.g. 1 Hz, this makes it possible to investigate the switching transients of the DUT without having to heat the device.

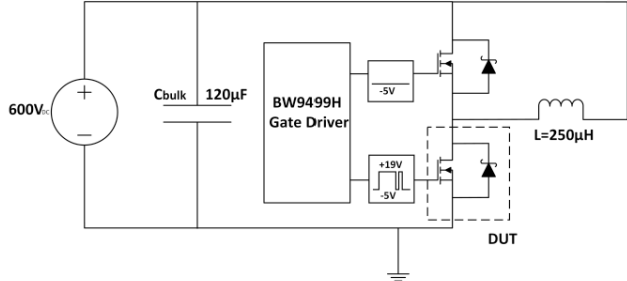


Fig. 2: Simplified double-pulse test circuit

The current measurement during fast transients highly relies on having the right measuring instrument. If high-frequency ringing occurs, the current measuring instrument should have higher bandwidth than this frequency in order to get the most accurate results. If not, this high-frequency ringing will be attenuated and the switching characteristics will be somewhat inaccurate. This is illustrated in Fig. 3, which is a DUT turn on at 600 V drain-to-source voltage and 90 A drain current. I_{d1} is measured with a CWT Mini 6B Rogowski coil, which has a bandwidth of 20 MHz. I_{d2} is measured with an SSDN series shunt from T&M Research Products, which has a bandwidth of 400 MHz.

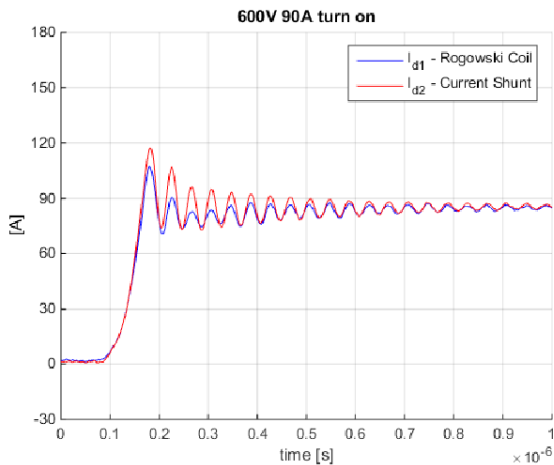


Fig. 3. Comparison of current measuring instruments at DUT turn on

The shunt measurement gives a little higher current overshoot during turn on as well as ringing with higher amplitude than with the Rogowski coil. Thus, the current measurement in the Rogowski coil is attenuated due to lower bandwidth. The high-frequency ringing has a frequency of approximately 24 MHz. The same phenomenon is depicted in Fig. 4, which is the DUT turn off at 600 V and 90 A.

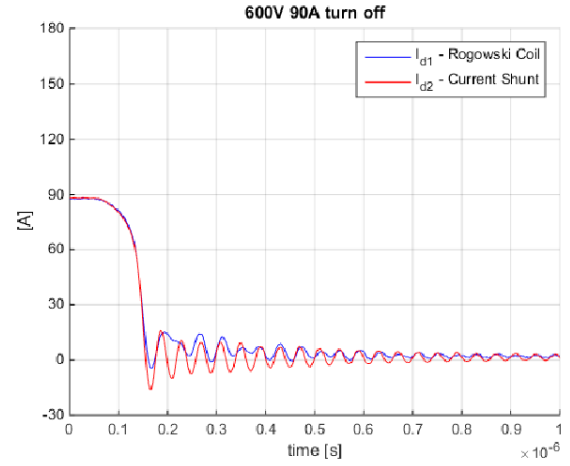


Fig. 4. Comparison of current measuring instruments at DUT turn off

Once more, the shunt measurement has higher oscillation amplitude. Even though the current shunt yields the most accurate drain current measurement, from this point onwards current will be measured with the Rogowski coil. This current measuring method is chosen because it is much more practical than using a current shunt. The drain-to-source voltage will be measured with a THDP0200 200 MHz differential high-voltage probe from Tektronix.

The measurements in Fig. 3 and Fig. 4 are done with an external turn-off gate resistor with higher resistance than the original value, i.e. $R_{g,off} = 7.8 \Omega$. This was done to slow down the turn off and thus reduce ringing and overshoot. In the following it is decided to go back to the original external turn-off gate resistor as this makes the turn-off switching as fast as possible. Thus, $R_{g,off} = 3.9 \Omega$. The turn-on gate resistor has a resistance of $R_{g,on} = 4.4 \Omega$.

B. Switching Characteristics

The switching characteristics of the DUT are investigated by measuring the voltage derivative dv/dt during turn off and the current derivative di/dt during turn on. This is presented in Table I for different drain currents I_a .

TABLE I. NO SNUBBER – DV/DT AND DI/DT AT TURN OFF AND TURN ON

| I_a | Turn off | Turn on |
|-------|----------------|----------------|
| | dv/dt [V/ns] | di/dt [A/ns] |
| 30A | 9.60 | 0.70 |
| 60A | 12.7 | 1.00 |
| 90A | 13.7 | 1.32 |
| 120A | 14.2 | 1.48 |

The values of di/dt and dv/dt are calculated from 10 % to 90 % of their nominal values of drain current and nominal drain-to-source voltage respectively.

Table II presents the current fall time t_{fi} , voltage rise time t_{rv} and voltage overshoot V_{os} at DUT turn off in addition to voltage fall time t_{fv} , current rise time t_{ri} and current overshoot I_{os} at DUT turn on for different drain currents. The current and voltage rise times during switching are measured from 10 % to 90 % of their nominal values. Similarly, the current and voltage fall times are measured from 90 % to 10 % of their nominal values [13].

TABLE II. NO SNUBBER – RISE TIMES, FALL TIMES AND OVERSHOOTS

| I_d | Turn off | | | Turn on | | |
|-------|----------|----------|----------|----------|----------|----------|
| | t_{rv} | t_{fi} | V_{os} | t_{fv} | t_{ri} | I_{os} |
| 30 A | 50 ns | 62 ns | 64 V | 71 ns | 34 ns | 25 A |
| 60 A | 37 ns | 50 ns | 160 V | 93 ns | 47 ns | 24 A |
| 90 A | 35 ns | 42 ns | 220 V | 107 ns | 55 ns | 22 A |
| 120 A | 34 ns | 39 ns | 292 V | 126 ns | 64 ns | 23 A |

A similar study as presented in Table II was conducted in [14], where the CCS050M12CM2 SiC six-pack module from Cree Inc. was double-pulse tested. It is found that all the switching transients in Table II are faster than in [14] for all drain currents. It is important to underline that these studies are based on different conditions, but the comparison still gives an idea of how fast the switching is.

C. Switching Losses

The turn-on and turn-off switching energy losses of the DUT can be calculated by integrating the power losses ($v_{ds} \cdot i_d$) of the lower switch during switching [15]. This is presented as a function of drain current in Fig. 5.

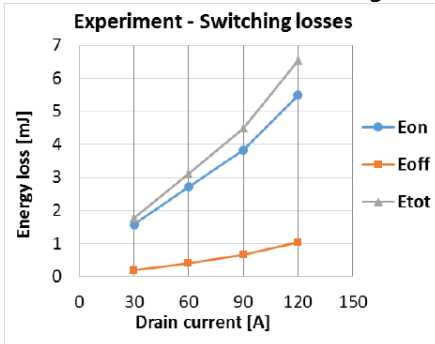


Fig. 5. Turn-on and turn-off switching losses

Comparing the switching losses in Fig. 5 to what is presented in [14] shows that the DUT has lower turn-off losses and slightly higher turn-on losses. The results in Fig. 5 are also similar to what is presented in the SiC module datasheet [11].

IV. SNUBBER DESIGN – THEORY, SIMULATION AND EXPERIMENT

A. Theoretical approach

The switching characteristics of the DUT show extensive voltage overshoot and long-lasting ringing due to parasitics inside the SiC power module and in other parts of the test circuit (Fig. 7). In order to reduce this parasitic oscillation, snubber circuits can be designed and implemented. There are different ways of implementing snubbers in power circuits,

depending on what kind of snubber that is needed. Two possible solutions are presented in Fig. 6.

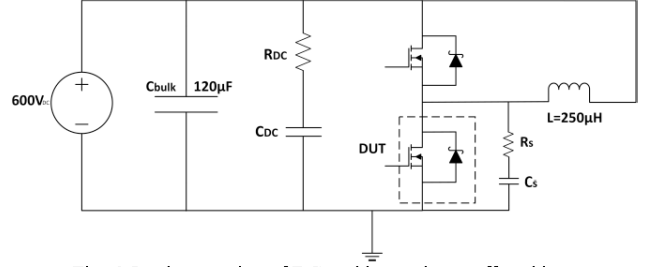


Fig. 6. Implementation of DC snubber and turn-off snubber

A DC snubber is connected in parallel with the half-bridge module, depicted by R_{DC} and C_{DC} . The snubber connected in parallel with the DUT, depicted by R_s and C_s , is called a turn-off snubber. These two snubbers have different properties and advantages that will be explained in the continuation. Both snubber configurations are RC snubbers.

In order to be able to design suitable snubbers, a double-pulse test without snubber is conducted at 600 V 90 A. This gives the DUT turn-off voltage characteristics in Fig. 7:

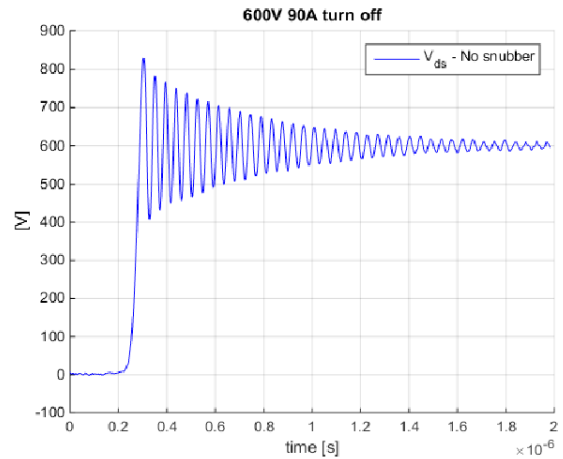


Fig. 7. DUT turn-off voltage characteristics at 600 V 90 A

Firstly, a DC snubber will be designed based on the turn-off characteristics. The extensive ringing in Fig. 7 has a frequency of $f_r = 21.3 \text{ MHz}$. This ringing is caused by a resonance between the parasitic capacitance C_p of the SiC power devices (SiC MOSFET and SiC SBD) and the stray inductance L_p in the test circuit. Thus, the following expression can be presented [8]:

$$f_r = \frac{1}{2\pi \cdot \sqrt{L_p \cdot C_p}} \leftrightarrow L_p = \frac{1}{(2\pi)^2 \cdot f_r^2 \cdot C_p} \quad (1)$$

From [11], $C_p = 1.45 \text{ nF}$. This gives a stray inductance of $L_p = 38.5 \text{ nH}$. This is the total stray inductance in the entire test circuit, where about half the inductance is placed inside the module itself. The damping coefficient ζ of such a parallel RLC resonant circuit can be expressed in the following manner, where R_{DC} is the resistance of the DC snubber resistor [9]:

$$\zeta = \frac{1}{2 \cdot R_{DC}} \cdot \sqrt{\frac{L_p}{C_p}} \leftrightarrow R_{DC} = \frac{1}{2 \cdot \zeta} \sqrt{\frac{L_p}{C_p}} \quad (2)$$

By choosing the damping coefficient in order to obtain critical damping of the ringing, i.e. $\zeta = 1$, the snubber resistor is calculated to be $R_{DC} = 2.6 \Omega$. For the DC snubber to be effective at the ringing frequency, the following equation must be true [9]:

$$f_r = \frac{1}{2\pi \cdot R_{DC} \cdot C_{DC}} \leftrightarrow C_{DC} = \frac{1}{2\pi \cdot R_{DC} \cdot f_r} \quad (3)$$

Thus, $C_{DC} = 2.9 \text{ nF}$. This DC snubber topology creates an alternative path for the inductive current during turn off, which reduces the turn-off surge voltage and the parasitic oscillation [16].

The turn-off snubber capacitor in Fig. 6 can be calculated by using the relation in (4) [4].

$$C_s = \frac{I_d \cdot t_{fi}}{2 \cdot V_{ds}} = \frac{90 \text{ A} \cdot 42 \text{ ns}}{2 \cdot 600 \text{ V}} = 3 \text{ nF} \quad (4)$$

I_d is the drain current, t_{fi} is the current fall time and V_{ds} is the drain-to-source voltage. From the 90A 600V characteristics, $t_{fi} = 42 \text{ ns}$. This gives $C_s = 3 \text{ nF}$.

The turn-off snubber resistor should be chosen so that the peak current through it is less than the reverse-recovery current of the freewheeling diode during turn on. The reverse-recovery current should be limited to $\frac{V_{ds}}{R_s} < I_{rr} = 0.2 \cdot I_0$ [4]. This gives at the drain current rating of 120A the following turn-off snubber resistor.

$$R_s = \frac{V_{ds}}{0.2 \cdot I_0} = \frac{600 \text{ V}}{0.2 \cdot 120 \text{ A}} = 25 \Omega \quad (5)$$

Turn-off snubbers are essentially used in order to limit switching energy losses during turn off by limiting the voltage rise across the transistor during the transient. Normally, turn-off snubbers are RCD circuits including a diode in parallel to the snubber resistor. Such a diode would help achieve a higher current flowing into the snubber capacitor (faster charging of C_s) during DUT turn off, as the current would flow through the diode instead of through the resistor [4]. Thus, an RCD snubber would reduce the power dissipation during DUT turn off compared to an RC snubber. However, by not including the diode, such a snubber circuit will be able to reduce significantly the turn-off voltage overshoot caused by parasitic inductance close to the switch as the voltage rise is restricted [9]. This is why the diode is not included in Fig. 6. A turn-off snubber affects the turn-on transient and switching losses in a negative manner, as the current overshoot increases due to discharge of the snubber capacitor through the snubber resistor during DUT turn on.

In a turn-off snubber, it is of great interest to keep the switching losses as small as possible in both the switch and the snubber. An increased capacitance C_s in the turn-off snubber would help reduce the voltage overshoot and reduce ringing. However, this would lead to higher losses as this slows down both the turn-on and the turn-off transients. In addition, the capacitor energy, which is dissipated in the snubber resistor, is given by [4]:

$$E_{R_s} = \frac{C_s \cdot V_{ds}^2}{2} \quad (6)$$

Thus, a higher capacitance C_s implies higher losses dissipated in the snubber resistor R_s .

B. Simulations in LTspice IV

In order to simulate the performance of the DUT, an LTspice model of the BSM120D12P2C005 is used. The model is provided by Rohm Semiconductor. The full LTspice IV simulation circuit is given in Fig. 8.

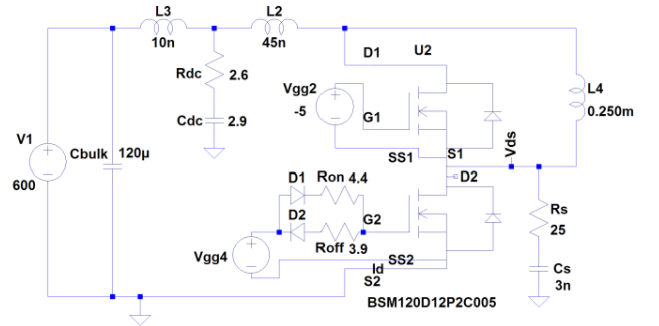


Fig. 8. LTspice IV double-pulse test circuit

The stray inductance in Fig. 8 is determined by comparing the experimental switching characteristics with the results found through simulations. However, this inductance should not be considered as the true stray inductance in the laboratory setup. The parasitic inductance is lumped and placed at two different locations. The reason for this is that the DC-link has very little inductance, which can be found as the 10 nH inductance in Fig. 8. However, the biggest part of the stray inductance is found close to, and inside, the module itself. This stray inductance is represented by the 45 nH inductance in Fig. 8. From Section IV.A, it is known that a DC snubber connected in parallel to the half-bridge module can reduce ringing in the switching characteristics, especially during turn off. However, such a snubber is only able to reduce the ringing caused by inductance between the power supply and itself.

By using the .step feature in LTspice IV, it is possible to simulate the switching characteristics of the DUT both with and without the DC snubber. Connecting a DC snubber, depicted by R_{dc} and C_{dc} in Fig. 8, gives the results in Fig. 9. It is important to underline that the turn-off snubber, depicted

by R_s and C_s in Fig. 8, is not yet connected. The blue waveform is the turn off at 600 V 90 A without snubber, while the red waveform is the turn off including the DC snubber with $R_{DC} = 2.6 \Omega$ and $C_{DC} = 2.9 \text{ nF}$.

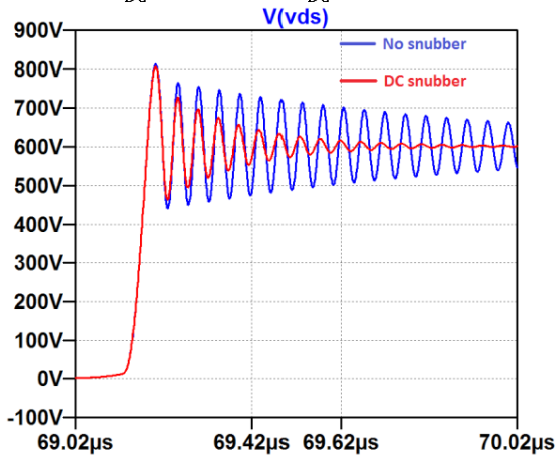


Fig. 9. Simulation – Effect of DC snubber

The DC snubber connected across the half-bridge module improves the turn-off transient by reducing the ringing during turn off. However, the extensive voltage overshoot and ringing caused by the inductance close to, and inside, the module is still significant. The addition of a turn-off snubber across the DUT could solve this problem. A turn-off snubber is depicted by R_s and C_s in Fig. 8. Fig. 10 presents the results of the implementation of a turn-off snubber in the simulation circuit. The blue waveform is the turn off at 600 V 90 A with only the DC snubber, while the red waveform presents the turn-off transient with both the DC snubber and a turn-off snubber with $R_s = 25 \Omega$ and $C_s = 3 \text{ nF}$.

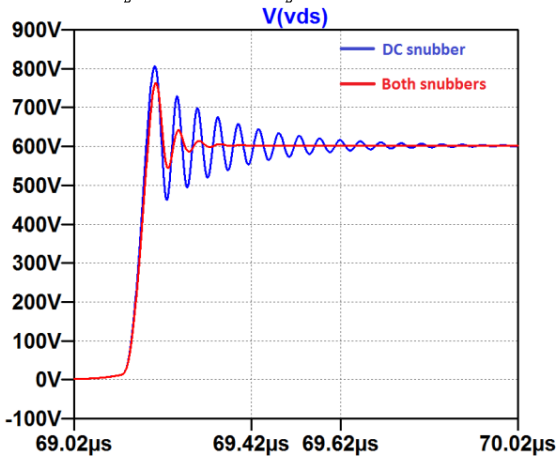


Fig. 10. Simulation – Effect of turn-off snubber

The turn-off snubber efficiently reduces the voltage overshoot and attenuates the long-lasting ringing. Thus, the addition of two snubber circuits greatly improves the switching characteristics during DUT turn off. These snubbers influence the switching performance and the switching rise times and fall times. It is thus interesting to analyze the switching losses with snubbers compared to without snubbers. The turn-off switching losses found

through simulations in LTspice IV are presented in Table III. The table includes information on where in the circuit the switching losses are dissipated.

TABLE III. SIMULATION - TURN-OFF SWITCHING LOSSES WITH AND WITHOUT SNUBBER

| | Turn-off switching losses | | | | |
|-------------|---------------------------|------------------------------|-----------------------|------------|------------|
| | With snubbers | | | | No snubber |
| Current [A] | Switch [mJ] | DC snubber [μJ] | Turn-off snubber [mJ] | Total [mJ] | Total [mJ] |
| 30 | 0.26 | 2.8 | 0.39 | 0.65 | 0.31 |
| 60 | 0.59 | 3.8 | 0.45 | 1.04 | 0.76 |
| 90 | 1.06 | 5.2 | 0.49 | 1.55 | 1.37 |
| 120 | 1.70 | 8.8 | 0.54 | 2.24 | 2.04 |

In Table III, it is shown that the addition of a DC snubber and a turn-off snubber increases the total turn-off switching losses. However, the switching performance is greatly improved. The results from simulations in LTspice IV should not be considered as realistic results, as the test circuit is simplified. There could be faulty parameters in the model of the SiC module as well as parasitics that are not added elsewhere in the circuit. However, simulation in LTspice IV is an important and valuable tool when investigating and determining the switching performance of a power device.

C. Laboratory Experiments

The DC snubber design and the turn-off snubber design found through theoretical calculations and simulations are tested through laboratory experiments. By varying the resistance and the capacitance of the DC snubber, it is found that the optimal values are $R_{DC} = 3.33 \Omega$ and $C_{DC} = 1.8 \text{ nF}$. It is found that such a DC snubber connected in parallel close to the SiC module reduces the duration of the voltage ringing during turn off. Thus, the laboratory experiments confirm the results found in simulation. This snubber is composed by one 1.8 nF capacitor and three parallel non-inductive 10 Ω resistors. These snubber values are close to what was calculated in the theoretical part, and what gave improvement in simulation. The turn-off voltage characteristics with the optimal DC snubber are presented together with the turn-off voltage characteristics without snubber in Fig. 11.

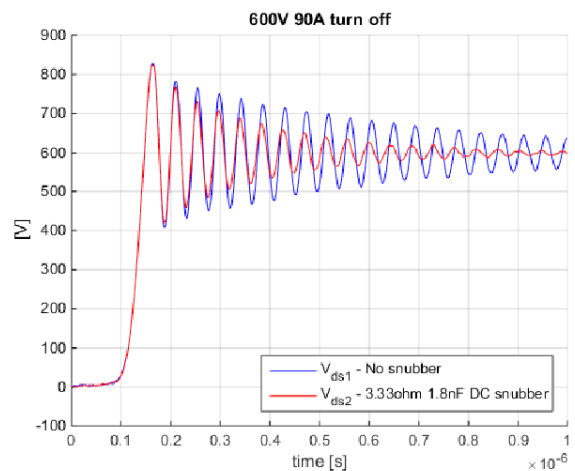


Fig. 11. Experiment – Effect of DC snubber

It is clear that the DC snubber in parallel with the SiC module improves the turn-off transient by attenuating the long-lasting ringing. The addition of the DC snubber reduces the duration of the ringing by approximately 60 %. Thus, this DC snubber will be included in the rest of the laboratory experiments. However, the voltage overshoot and ringing is still extensive, which is similar to what was found in simulation. This implies that there is a lot of inductance between the DC snubber and the DUT, both inside and outside the module. As shown through simulations in LTspice IV, this problem may be solved by connecting a turn-off snubber across the DUT. By varying the capacitance and the resistance of the turn-off snubber, it is possible to compare the performance of the different snubbers. It is important to underline that such a snubber has to be designed based on a compromise between switching losses and voltage overshoot/ringing.

Firstly, it was chosen to do tests with constant resistance in order to investigate the influence of capacitance in RC turn-off snubbers. Fig. 12 presents the turn-off characteristics at 600 V 90 A with two different turn-off snubbers. The resistance is the same in both snubbers, while the capacitance is different.

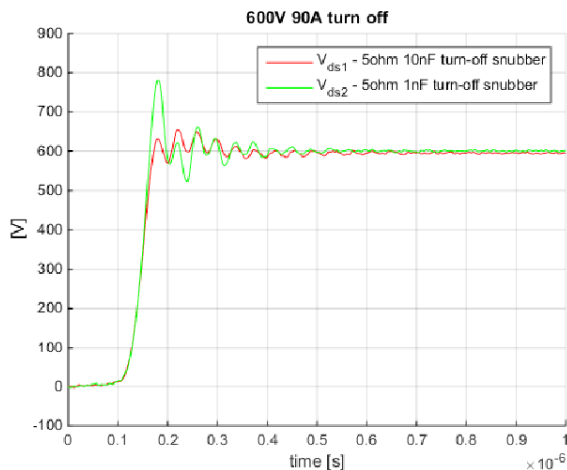


Fig. 12. Influence of snubber capacitor on turn-off transient

Fig. 12 shows that the 10 nF capacitor reduces the voltage overshoot by slowing down the voltage transient across the transistor. Even though this leads to higher damping and better turn-off switching response, the advantages are overshadowed by higher switching losses due to slower switching. By compromising between voltage overshoot and switching losses, it was decided that a capacitance of 3 nF yields the best turn-off transient. The 3 nF capacitance is achieved by paralleling three 1 nF capacitors. This helps to reduce the stray inductance in the snubber and thus the voltage overshoot.

Now, the snubber capacitor is held constant at 3 nF. The influence of the snubber resistor at 600 V 90 A is presented in Fig. 13.

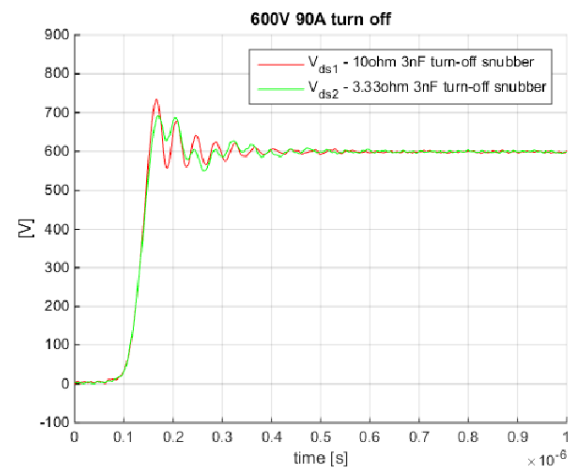


Fig. 13. Influence of snubber resistor on turn-off transient

It is shown that a reduction of the snubber resistance yields lower voltage overshoot. This corresponds to what was presented in (2), as the damping increases when the resistance decreases for a parallel RLC circuit. However, as can be seen in Fig. 13, this introduces a new low-frequency ringing component. The 3.33 Ω resistance is obtained by paralleling three non-inductive 10 Ω resistors. The low-frequency ringing could be caused a resonance effect between the different components of the snubber. In order to avoid the low-frequency ringing, it was decided to use a turn-off snubber with $R_s = 10 \Omega$ and $C_s = 3 nF$. The snubber resistance is chosen to be smaller than what was calculated as theoretically optimal, as this gives a better turn-off transient.

It is of interest to investigate if the addition of a turn-off snubber influences the turn-off losses considerably in the laboratory experiments. The turn-off switching losses for different drain currents are presented in Table IV, including information on where in the circuit they are dissipated. The turn-off snubber losses are found by integrating the resistive losses $R_s \cdot i_{snub}^2$ during DUT turn off, where i_{snub} is the current in the turn-off snubber.

TABLE IV. EXPERIMENT – TURN-OFF SWITCHING LOSSES WITH AND WITHOUT SNUBBER

| Current [A] | Turn-off switching losses | | | |
|-------------|---------------------------|-----------------------|------------|-----------------------|
| | Switch [mJ] | Turn-off snubber [mJ] | Total [mJ] | No snubber Total [mJ] |
| 30 | 0.29 | 0.17 | 0.45 | 0.19 |
| 60 | 0.365 | 0.19 | 0.56 | 0.40 |
| 90 | 0.60 | 0.16 | 0.76 | 0.66 |
| 120 | 0.895 | 0.15 | 1.13 | 1.05 |

The switching losses in the DC snubber are not included in Table IV, as these are negligible compared to the losses in the switch and the turn-off snubber. This was also the case in simulation. It is shown in Table IV that the total turn-off switching losses increase with increased drain current. However, due to much faster turn-off switching for higher drain currents, the snubber losses in Table IV do not increase.

V. INFLUENCE OF TURN-OFF SNUBBER ON TURN ON

It is shown that a DC snubber along with a turn-off snubber really improves the turn-off switching characteristics, without influencing the turn-off losses considerably. However, such a turn-off snubber will affect the switching performance during turn on. Fig. 14 presents the 600 V 90 A turn-on transient of the DUT with and without snubber.

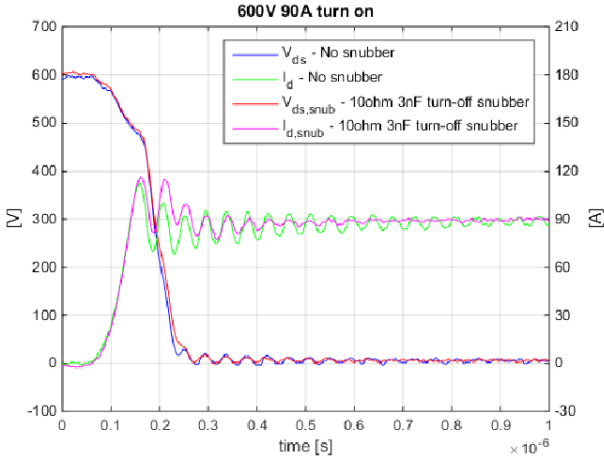


Fig. 14. Influence of turn-off snubber on DUT turn-on transient

It is clear that the turn-off snubber influences the turn on by introducing a higher and wider current overshoot. This leads to higher turn-on switching losses. In addition, the voltage fall time increases due to the capacitance in the turn-off snubber. On the other hand, the turn-off snubber reduces the ringing during turn on. The current in Fig. 14 is measured with the CWT Mini 6B Rogowski coil. As stated in Section III.A, this current measurement is not accurate due to the low bandwidth. Thus, the current overshoot is probably higher than what is shown in Fig. 14. However, it is accurate enough to give a good representation of the turn-on characteristics with and without turn-off snubber.

The turn-on switching losses will also change due to the addition of a turn-off snubber. Table V presents the turn-on switching losses with and without snubber, including information on where the losses are dissipated. The turn-off snubber losses are found by integrating the resistive losses $R_s \cdot i_{snub}^2$ during DUT turn on.

TABLE V. EXPERIMENT – TURN-ON SWITCHING LOSSES WITH AND WITHOUT SNUBBER

| Current [A] | Turn-on switching losses | | | | |
|-------------|--------------------------|------------|------|------------|------|
| | With snubbers | | | No snubber | |
| Switch [mJ] | Turn-off snubber [mJ] | Total [mJ] | | Total [mJ] | |
| 30 | 2.00 | 0.43 | 2.43 | | 1.57 |
| 60 | 3.06 | 0.50 | 3.56 | | 2.71 |
| 90 | 4.60 | 0.61 | 5.21 | | 3.83 |
| 120 | 6.05 | 0.75 | 6.80 | | 5.49 |

Table V shows that the turn-off snubber influences the turn-on transient by increasing the turn-on switching losses, and thus the total switching losses of the DUT.

The total DUT switching losses with snubbers as a function of drain current are presented in Fig. 15.

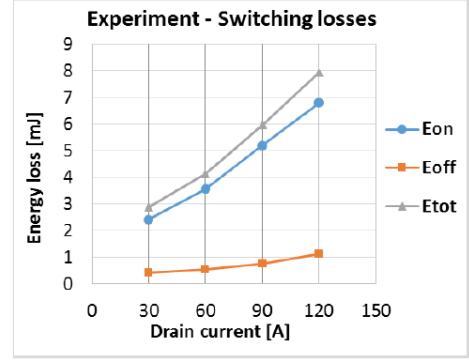


Fig. 15. Turn-on and turn-off switching losses with snubbers

E_{on} and E_{off} include the resistive losses in the snubber. When comparing the results in Fig. 15 with what was found in Fig. 5, it is clear that the switching losses increase due to the addition of snubbers. However, this is only marginally. The advantages of improved switching characteristics are much more significant than the disadvantages of increased switching losses. A somewhat similar study to what is conducted in this paper was conducted in [17], where double-pulse tests of the same DUT were carried out without considering snubbers. The results in Fig. 15 and Fig. 5 show significantly lower switching losses, both with and without snubber, due to a more suitable gate driver for SiC MOSFETs in this paper compared to what was used in [17].

VI. SWITCHING CHARACTERISTICS WITH SNUBBER CIRCUITS

The implementation of two snubber circuits influences the switching transients of the DUT. In order to investigate this influence, the voltage and current derivatives during turn off and turn on respectively are presented in Table VI.

TABLE VI. WITH SNUBBERS - DV/DT AND DI/DT AT TURN OFF AND TURN ON RESPECTIVELY

| I_d | Turn off | Turn on |
|-------|----------------|----------------|
| | dv/dt [V/ns] | di/dt [A/ns] |
| 30A | 6.2 | 0.68 |
| 60A | 10.4 | 1.07 |
| 90A | 12.2 | 1.24 |
| 120A | 13.3 | 1.54 |

Table VI shows that the two snubbers slows down the dv/dt during turn off while di/dt stays approximately the same compared to the results in Table I. The voltage and current rise times, fall times and overshoot are presented in Table VII.

TABLE VII. WITH SNUBBERS - RISE TIME, FALL TIME AND OVERSHOOT AT TURN OFF AND TURN ON

| I_d | Turn off | | | Turn on | | |
|-------|----------|----------|----------|----------|----------|----------|
| | t_{rv} | t_{fi} | V_{os} | t_{fv} | t_{ri} | I_{os} |
| 30 A | 77 ns | 106 ns | 28 V | 80 ns | 35 ns | 30 A |
| 60 A | 46 ns | 63 ns | 60 V | 97 ns | 44 ns | 28 A |
| 90 A | 39 ns | 52 ns | 136 V | 115 ns | 58 ns | 27 A |
| 120 A | 36 ns | 48 ns | 196 V | 131 ns | 62 ns | 27 A |

When comparing Table VII with the results in Table II, it is found that the turn-off snubber influences the turn off by increasing the switching time and reducing the voltage overshoot significantly. At DUT turn on, the switching time is close to unaffected. The current overshoot, however, increases marginally due to the turn-off snubber.

VII. CONCLUSION

The switching characteristics of the BSM120D12P2C005 SiC Power Module from Rohm Semiconductor are obtained through a standard double-pulse test. Extensive voltage overshoot and long-lasting ringing occur at DUT turn off due to stray inductance inside the module and in other parts of the test circuit. Simulations in LTspice IV suggest two different snubber circuits that improve the turn-off characteristics. It is shown through laboratory experiments that the duration of the parasitic ringing can be reduced by 60 % by implementing a DC snubber circuit. However, the stray inductance inside the module still causes extensive voltage overshoot during DUT turn off. It is found that the addition of an RC turn-off snubber reduces the voltage overshoot by 40 % as well as reducing the duration of the parasitic ringing by 65 % from the turn off with only DC snubber, resulting in a total duration reduction of 85 % at 600 V drain-to-source voltage and 90 A drain current.

The switching losses in the circuit are found through both laboratory experiment and simulation, and it is found that the implementation of snubber circuits does not influence the total switching losses significantly. The turn-off switching losses only increase by a small margin after the addition of the snubber circuits. The turn-on switching losses, on the other hand, are more influenced by the turn-off snubber as the current overshoot increases. The turn-on switching losses increase by approximately 24 % at the DUT current rating of 120 A. In total, the switching losses increase by approximately 20 % due to the implementation of two snubber circuits. However, the snubber circuits help to achieve satisfactory switching characteristics, extremely fast switching and low DUT switching losses.

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