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Design of RF/microwave integrated circuits in GaN MMIC technology (1 GHz - 12 GHz)

Construction of a GaN MMIC power amplifier
with active load modulation and dynamic bias

Jørn Frøysa

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Supervisor: Morten Olavsbråten, IET

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

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Abstract

Based on the concept developed by Morten Olavsbråten at the department of Electronics and Telecommunications at NTNU, an amplifier based on a modification of the Doherty amplifier is designed in Keysight Advanced Design System (ADS) with GaN MMIC models for all components except splitter and load. The goal of the amplifier is to remove the quarter-wave transmission lines to increase its bandwidth. Envelope tracking is used to ensure the same characteristic efficiency curve as the Doherty amplifier, and a linear voltage tracking scheme is found to produce the best combination of efficiency and gain. The parasitics of the transistor is included in the network designs to ensure increased control of the impedances observed by the transistors current source. The initial bandwidth goal is 800 MHz with center frequency at 2.4 GHz, but the final result yields a bandwidth of 1.2 GHz spanning from 1.6 GHz to 2.8 GHz. Drain efficiency lies above 40% efficiency for a power backoff of 13dB, for all frequencies.

Sammendrag

Basert på et konsept utviklet av Morten Olavsbråten ved Institutt for elektronikk og telekommunikasjon ved NTNU, blir en forsterker basert på Doherty topologien designet i Keysight Advanced Design System (ADS) med GaN MMIC modeller for alle komonenter, untatt splitter og last. Målet med forsterkeren er å eliminere kvart-bølge transmisjonslinjene for å øke forsterkerens båndbredde. Envelope tracking brukes for å oppnå samme karakteristiske effektivitetskurve som Doherty forsterkeren, og det blir konkludert med at lineær spennings-tracking gir den beste kombinasjonen av effektivitet og gain av de metodene som utforskes. Transistorens parasittiske komponenter er inkludert i designet av utgangsnettverket for å bedre kontrollen over hvilke impedanser transistorens interne strømkilde ser. Det opprinnelige båndbreddemålet er 800 MHz med en senterfrekvens på 2.4 GHz, men det endelige resultatet har en båndbredde på 1.2 GHz fra 1.6 GHz til 2.8 GHz. Drain-effektivitet ligger over 40% effektivitet fra en effekt back-off på 13 dB, for alle frekvenser.

Preface

This master thesis has been developed by Jørn Frøysa for the department of Electronics and Telecommunications at NTNU. Thanks to the guidance given by supervisor Morten Olavsbråten and countless hours spent working with fellow student Børge Myran, my physical and theoretical understanding of microwave and amplifier design has significantly increased. A big thank you goes to Morten Olavsbråten for his patience and passion for teaching.

A special thank you also goes to my father. Without his never ending patience when faced with stupid questions, I would never have gotten as far as I have.

Contents

1 Introduction

With increased focus on the environment and global warming, demand for energy efficient electronics is at an all time high. The demand for service, connectivity and high datarates at low prices is also very high as the wireless market and its services expands. These demands are not easy to simultaneously fulfill, as high efficiency and large bandwidth are somewhat contradictory. For certain modulation techniques such as higher order QAM efficiency can be a challenge as the modulated signal has a high peak to average ratio. The amplitude of these signals will, most of the time, be relatively low, but will for certain symbols increase to a much higher amplitude. The power amplifier used for a transmitter must be large enough to handle the highest peaks. This means its efficiency will be at its maximum for the peaks, while being much lower for the average amplitude levels.
The Doherty amplifier is one solution to this problem as its efficiency rises to a high level at a relatively low drive level, and then remains high all the way up to the peak values. A rather large drawback with the Doherty amplifier is its bandwidth, as it is typically limited to less than 10% of its center frequency. This is due to the quarter wave transmission lines used in the topology, and it limits the number of seperate carrier frequencies the amplifier can handle. This project will attempt to remedy this by removing the transmission lines altogether, while using envelope tracking to achieve the same characteristic efficiency curve as the Doherty amplifier. The modified amplifier is here called OLMET amplifier, Olavsbråten Load Modulated Envelope Tracking amplifier, and is named after Morten Olavsbråten at the Department of Electronics and Telecommunications at NTNU, who developed the concept. The only thing limiting the bandwidth once the quarter wave transformers are gone should be the components themselves. A wide bandwidth will allow a system to use the same amplifier for a wide range of carrier frequencies. This saves resources, greatly simplifies the overall system thus reducing the area needed for implementation.

The goals for the design are:

- Doherty-like efficiency curve.
- Center frequency at 2.4 GHz
- Bandwidth of at least 800 MHz.
- All components, with exception of load and input splitter, modeled with GaN MMIC models.
- Minimum of 10 Watts power delivered to load in band.
- Total die area of 2x2mm^2.
- Envelope tracking implemented mathematically.
- Active load modulation, similar to that of the Doherty amplifier.

Interconnects between components is not necessary, and there are no specific requirements to gain or efficiency, beyond those stated above. This is because the goal of this project is proof of concept of the OLMET amplifier, and not physical implementation.

This report will first present theory which is relevant for, and used in, the design of the amplifier, as well as understanding the operation of the Doherty amplifier upon which it is based. It then describes the design and implementation of the amplifier, before it goes on to present the results. The results are discussed in section 5, before a conclusion is reached. Parts of the theory was developed in cooperation with Børge Myran, so there will be similarities between this report and his.

2 Theory

2.1 S- and Z-parameters

There are several ways of analyzing a rather complicated network or device. One of these methods is defining the scattering parameters of the device. These parameters completely describe the behaviour of the system in question, by defining the ratio of voltage out of the device to the voltage into the device. The ratio of input and output currents can also be used, but voltage ratios are more common. Figure 1 shows the basic two-port system where the input voltages are defined as V_n^+ and the voltages going out of the device are V_n^-. The S-parameter matrix is shown in the device.

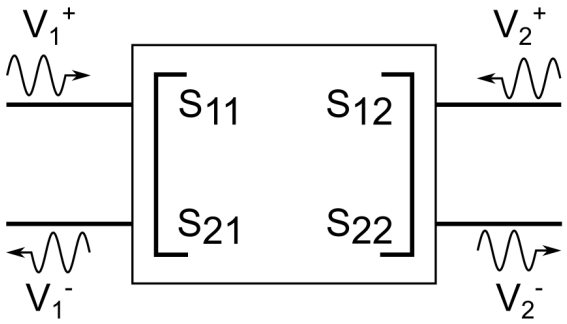


Figure 1: Two port S-parameters.

The S-parameters are formally defined as

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+=0 \text{for} k\neq j} \tag{2.1}$$

Which states that a given S-parameter is defined by the ratio of the output voltage at port i, to the input voltage at port j, when all other input voltages are set to zero (and terminated in 50Ω). The S-parameters can be divided into reflection coefficients and transmission coefficients, where S_{11} and S_{22} are the reflection coefficients of port 1 and 2 respectively, and S_{21} and S_{12} are the transmission coefficients from port 1 to port 2, and vice versa. If $S_{ij} < 1$, it means there is some reflection or transmission, but there is loss. If $S_{ij} = 1$ it means there is total reflection or transmission with no loss, and $S_{ij} > 1$ means the reflected or transmitted signal is amplified as it passes through the system. For a given system with N ports the scattering matrix can be defined as

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \cdot \\ \cdot \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \cdot & \cdot & S_{1N} \\ S_{21} & \cdot & \cdot & \cdot & \cdot & \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ S_{N1} & \cdot & \cdot & \cdot & \cdot & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \cdot \\ \cdot \\ V_N^+ \end{bmatrix} \tag{2.2}$$

The S-parameters are closely related to other parameters such as the admittance (Y) and the impedance (Z) parameters and once one is known, along with the voltages and currents, the others can be derived.

Z-paramters are defined as

$$Z_{ij} = \left. \frac{V_i^-}{I_j^+} \right|_{I_k^+ = 0 \text{for} k \neq j} \tag{2.3}$$

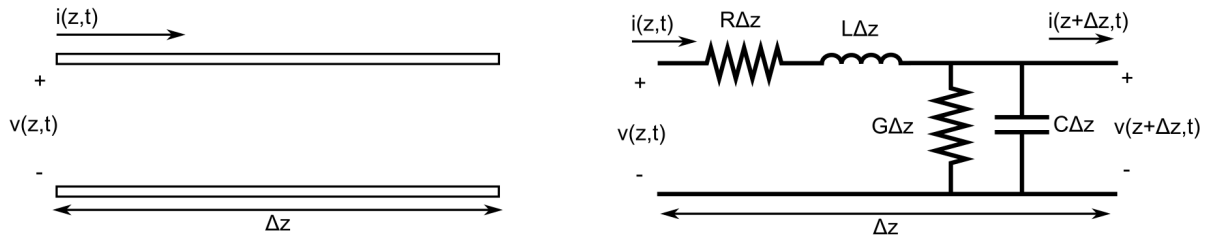
And gives the observed impedance between two ports, similiar to how S-parameters give reflection or transmission coefficients. However the Z-parameter sets the current at a given port to zero, which means its impedance at the port is ∞, in other words the port is open. While S-parameters assume a 50Ω load is attached to the port in question, to provide a match so that the voltage reflected from the load $V_k^+ = 0$.

As Y parameters haven't been utilized in this project, they will not be discussed further.

2.2 Transmission lines

Transmission line theory is a is an extensive field which affects all analog electronics design and analysis. At low frequencies it is not necessary to pay much attention to it as the physical size of the components, wires and traces are much smaller than the signal wavelength, so the voltage over, and current through, a trace can be considered constant for any given time. At high frequencies the wavelength of the signal becomes short enough to be comparable to the physical dimension of the traces, and the voltage over, and current through, a trace for a given snapshot of time is no longer constant. Combined with the fact that the effects of the parasitics of the line become much more significant for higher frequencies, even a simple line can have a huge effect on the observed impedance of a circuit.

A transmission line can be represented as a two-wire circuit, as shown in figure 2a, with a voltage and current as function of both time and location along the line. Δz shows this is a infinitesimally small section of the total line. A lumped component equivalent of the transmission line can be used to account for the losses and phase changes of the signal. The



(a) Voltage and current definitions (b) Lumped components equivalent

Figure 2: Basic transmission line definitions[1]

equivalent of a Δz section is shown in figure 2b. By applying Kirchhoff's current and voltage law, the telegrapher equations can be deduced. Their phasor representations are shown in equations 2.4.

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.4a}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.4b}$$

Further solving 2.4a for $I(z)$ and 2.4b for $V(z)$, and substituting one into the other gives

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.5a}$$

$$\frac{d^2I(z)}{dz^2} = -\gamma^2 I(z) = 0 \tag{2.5b}$$

Where

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.6}$$

is the complex propagation constant, and represents both the attenuation and phase change the propagating signal experiences. Equations 2.5 in turn can be solved to achieve the travelling wave solutions shown in equations 2.7a.

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.7a}$$

$$\begin{aligned} I(z) &= I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \\ &= \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{\gamma z} \end{aligned} \tag{2.7b}$$

Here the total voltage, or current, at any given point along the line is represented as the sum of two waves propagating in opposite directions. For voltage, the foward wave as V_0^+, and

the reflected wave as V_0^-, and similarly for the current. The lumped components of figure 2b can be represented by a single unit, the characteristic impedance, Z_0 which represents the resistance seen by a signal in either direction along an infinitely long transmission line. The characteristic impedance is important as it can be used as a transmission line property to transform the observed impedances of a system. Equations 2.8 shows the definition of the characteristic impedance.

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.8a}$$

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} \tag{2.8b}$$

When designing a transmission line the characteristic impedance can be changed by adjusting the lines width, which in turn also affects the maximum current that can run through it at any given time. Another important parameter to consider is the reflection coefficient, Γ, which is given by the ratio of the incident wave to the reflected wave. The reflection coefficient can be defined for both currents and voltages, though the latter is more commonly used. If first a load impedance is defined at a location $z = 0$, and it is connected to a source via a transmission line with characteristic impedance $= Z_0$ and length $l = -z$, then the load impedance is

$$Z_L = \frac{V(z=0)}{I(z=0)} = \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} Z_0 \tag{2.9}$$

By reorganizing this equation the voltage reflection coefficient can be achieved

$$\Gamma = \Gamma(z=0) = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.10}$$

The reflection coefficient is a function of position and equation 2.11 shows the coefficient when it is evaluated at the source, $l = -z$, given a lossless line, $\alpha = 0$,$\gamma = \beta$

$$\Gamma(l) = \frac{V_0^- e^{j\beta l}}{V_0^+ e^{j\beta l}} = \Gamma(0) e^{-2j\beta l} \tag{2.11}$$

This leads to the impedance also changing as a function of position, and by compbining equation 2.10 with 2.7a and 2.7b the impedance seen into the transmission line is found.

$$Z_{in} = \frac{V(-l)}{I(-l)} = Z_0 \frac{1 + \Gamma e^{-2j\beta l}}{1 - \Gamma e^{-2j\beta l}} \tag{2.12a}$$

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \tag{2.12b}$$

Equation 2.12b is an important one, as allows for evaluation of the input impedance at a given position along the line, and it states that the impedance of a transmission line is periodic by the tangiental function, and can therefore vary between $-j\infty < Z_{in} > +j\infty$. This allows the transmission line to replicate the effect of any lumped component at a specific frequency. This is the basis for the use of quarter-wave transmission lines, which is very important to the Doherty amplifier.

2.2.1 Quarter wave transmission line

A special case of transmission lines is the quarter-wave impedance transformer. The wavelength of a signal is defined as the physical distance between two points of equal phase along the transmission line, given as

$$\lambda = \frac{2\pi}{\beta} \tag{2.13}$$

Where β is the phase constant from equation 2.6. By careful choice of the line length, as a fraction of the wavelength, the impedance seen into the transmission line can be manipulated. By chosing the length to be equal to $\lambda/4$ equation 2.12b gives

$$Z_0^2 = Z_{in} Z_L \tag{2.14}$$

Which is the impedance equation for the quarter wave transmission line. This shows that if the characteristic impedance of the line is fixed and the load impedance increases, the impedance observed at the input of the line must decrease and vice versa. It also shows that transformation between a load impedance, and a desired input impedance can be achieved by choice of the characteristic impedance.

2.3 Parasitics

2.3.1 Components

Parasitics in components due to length of conductors (resistor and inductor) or proximity of parallell conductors, or conductors and ground plane (capacitors).

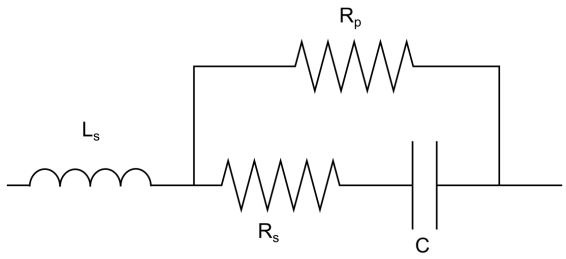
Due to the physical shape of electronic components, or the proximity to ground planes or electrical conductors, they can display inductive or capacitive behaviour even though the component itself is not designed for it.[2] This is due to coupling of electrical fields between the

conducting parts of the circuit, making the component act more as a capacitor or inductor at high frequencies. These unwanted "components" are called parasitics, and great care must be taken when doing a high frequency design as they can drastically alter the behaviour of a circuit.

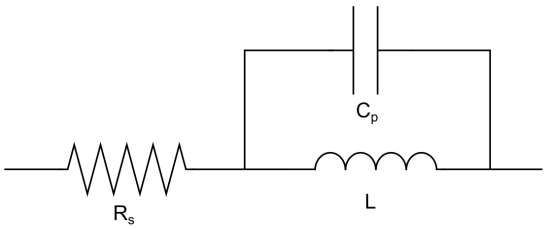
Capacitor: L_s is due to wires connecting the capacitor, R_s is due to resistance in the wires, R_p is due to imperfect dielectric, letting some current through, and C is the designed capacitance.

Inductor: R_s is due to resistance in the wires, C_p is due to stray fields and capacitance between turns in the inductor coil as well as solder plates in lumped surface mounted components, and L is the designed inductance.

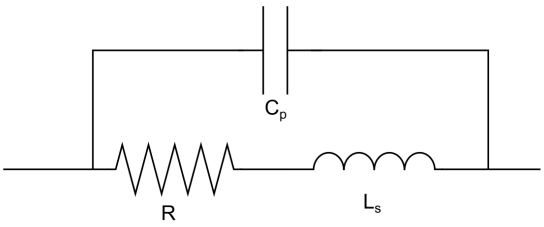
Resistor: C_p is due to capacitance between solder terminals of resistor, L_s is due to inductance of the wire, and R is the designed resistance.



(a) Parasitic model of capacitor.



(b) Parasitic model of inductor.



(c) Parasitic model of resistor.

Figure 3: Component parasitic models

In addition each component can have capacitances to ground on each side of the component to represent the capacitance between the conductors in the component and the ground plane beneath (if present). As the frequency of the signal increases the effect of the parasitics grows, and at some point the nature of the component can change. Capacitors starts acting like inductors, and vice versa. This is due to the parasitics becoming larger than the inherent

component value. The frequency where the components behaviour changes is called the componenents resonance frequency, and great care must be taken when designing RF systems to ensure the resonance frequency does not interfere with the desired behaviour of the system. The models can differ a little depending on whether they are integrated circuit or lumped component equivalents. Figures 3 are typical discrete, surface mount component models. MMIC models will be explored more in 2.10

2.3.2 Transistor

Like the components above the transistor is also subject to parasitic componenets due to its physical architecture. Figure 4 shows the generic model for transistor parasitics [3]. C_{gs} is the capacitance between the gate and source terminal of the FET due to them being physically isolated. However some leakage is present at higher frequencies, and R_i represents the minimum input resistance that can be observed when the impedance from C_{gs} alone becomes negligible. C_{gd} is the reason S_{12} of a real transistor isn't zero as it provides a path between the gate and drain terminal, thus the more correct model of a transistor is bilateral instead of unilateral which is often used as a simplification in transistor theory. This causes the input to see impedance changes due to network changes on the output and vice versa. The current source is the internal and ideal current source which represents the transistors functionality as current amplifier. When using load line theory in amplifier design as discussed in section 2.4.5 it is the impedance seen by this ideal current source that decides the slope of the load line. C_{ds} and R_{ds} represents the capacitance between drain and source, and the resistance seen through the charge carrying channel of the transistor.

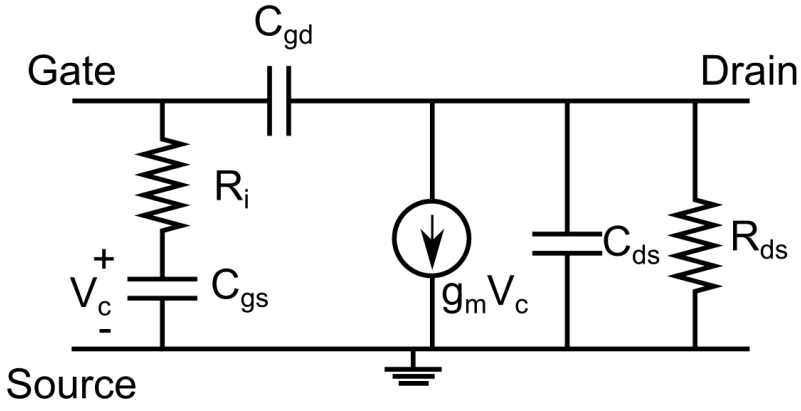


Figure 4: Parasitic model of Field effect transistor.

2.4 Power amplifiers

The goal when designing a power amplifier is to create a device which delivers a significant amount of electrical power in a controlled and predictable manner to a specific load. Amplifier types and topologies are numerous, and only those relevant to the project will be discussed.

An amplifier produces an amplified version of its input signal by converting DC power to AC power by use of the transistor, a non-linear device which conducts differing amounts of current based on an input current (BJT), or voltage (FET). The circuit surrounding the transistor provides stability and ensures the transistor "sees" the impedances which are optimal for its operation. Figure 5 is a simplified example of the constituent parts of a general amplifier design. In a proper design the different parts of figure 5 is combined together to simplify the design as much as possible, and they can therefore be indistinguishable from one another, e.g. stabilization and matching networks become the same network.

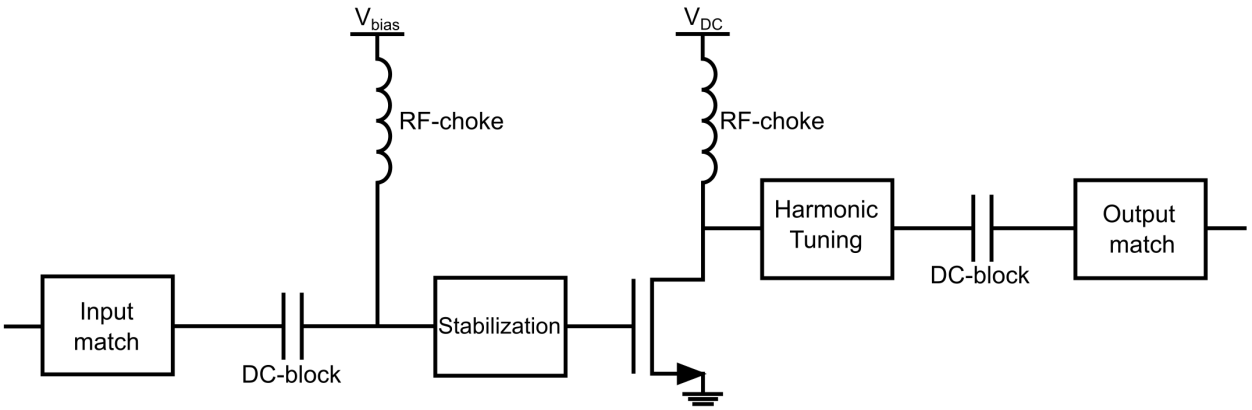


Figure 5: General power amplifier

2.4.1 Classes

The most basic amplifier classes are class A, B, AB and C, and all of them can be of the topolgy seen in figure 5. At first glance the most prominent design difference is the transistor bias voltage, where the class A amplifier has the highest voltage and class C has the lowest. This change in bias affects numerous properties such as how much of an input signal the amplifier conducts, the amplifiers efficiency, linearity, stability and gain.

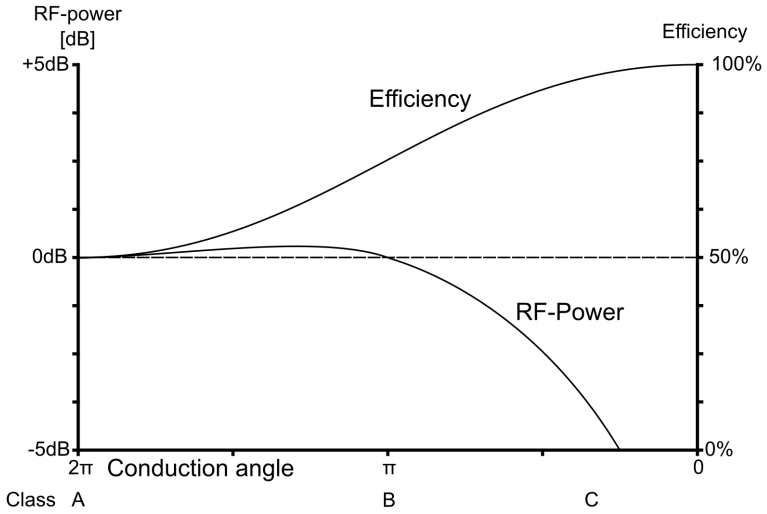


Figure 6: comparison of amplifier classes. Power relative to class A.

Figure 6 is a comparison between the amplifier classes, and shows the massive impact class choice has on the performance of the amplifier. Perhaps most notably is the efficiency shown on the right hand side of the graph, as it goes from 50% for a class A amplifier to 100% for a deep class C. The power on the left hand is relative to the expected output power of a class A amplifier, and shows the output power capacity increases slightly for a class AB amplifier before it dips sharply. These numbers are for ideal amplifiers and for real amplifiers the numbers would be lower. Conduction angle is a measure of how much of a signal is conducted by the transistor. The rest of the signal is lost due to the cut-off region of the transistor.
An amplifiers conduction angle isn't necessarily constant, and the angle shown in figure 6 assumes large signal operation, i.e. the output signal is close to its maximum. If a very small signal is applied to a class AB amplifier the signal will not be large enough for the transistor to reach its cut off region, therefore the amplifier conducts the entire signal which is consistent with class A operation. As conduction angle affects efficiency, the efficiency of a class AB amplifier will be similar to that of a class A amplifier, if the output signal is small enough. Amplifier efficiency is explored in more detail in section 2.4.4 When designing for different classes it is necessary to consider the harmonic currents and voltages through, and over, the transistor. Class-B amplifiers only conducts current during the positive half-period of the signal. This means the current through the transistor is the sum of the fundamental frequency, and its even-harmonics. Therefore in a class-B amplifier some attention should be paid to ensure the even harmonics, or at least second harmonics, sees a very small impedance towards the output of the amplifier.

2.4.2 Stability

Amplifier stability is dependent on signal frequency and load impedance. An unstable amplifier will uncontrollably produce large amounts of power at a certain frequencies which, more often than not, will be different from the center frequency. This will reduce the amount of power that can be generated at the desired frequency as well as potentially damage the amplifier or load circuitry. We differentiate between two states of stability, conditional and unconditional. A conditionally stable amplifier is only stable for certain frequencies and load impedances, and must be designed with great care and only be used in specific applications where stability is ensured. An unconditionally stable amplifier is stable for all frequencies and load impedances.

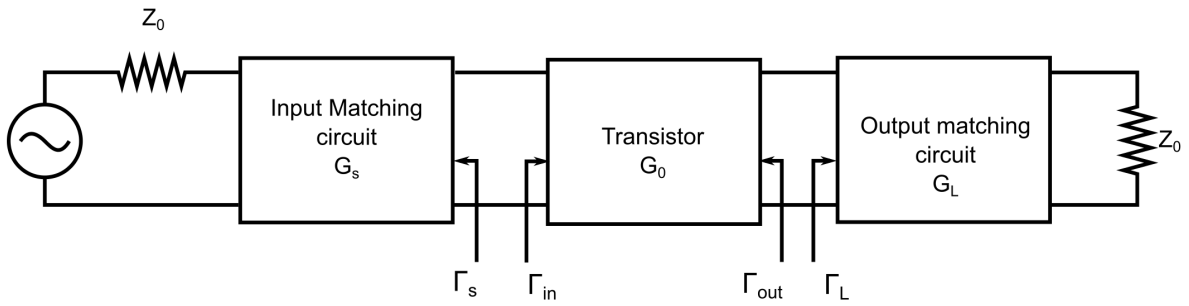


Figure 7: General transistor power amplifier[1]

Figure 7 shows a basic amplifier setup. Γ_{in}, Γ_{out}, Γ_S, and Γ_L are the reflection coefficients of the input and output of the transistor, and for the input and output matching circuit, seen from the transistor, respectively. The reflection coefficients gives the relationship between an input signal voltage and its reflection, and is used as a measure of impedance mismatch between circuits. A reflection coefficient greater than unity implies an amplification of the signal, therefore for unconditional stability the magnitude of the reflection coefficients for the transistor must be less than 1. This is expressed as

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.15a}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.15b}$$

Where S_{ij} represents the scattering parameters for the transistor. As equations 2.15a and 2.15b are dependent on Γ_L and Γ_S stability can be ensured by proper design of the input and output matching circuit. As long as the device is bilateral, equations 2.15a and 2.15b

represents a range of values for Γ_L and Γ_S which ensures stability. By setting the equations to 1 and manipulating them algebraically equations describing stability circles can be obtained, which shows the boundaries between stable and unstable regions.

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \tag{2.16a}$$

$$R_L = \left| \frac{S_{12}S21}{|S_{22}|^2 - |\Delta|^2} \right| \tag{2.16b}$$

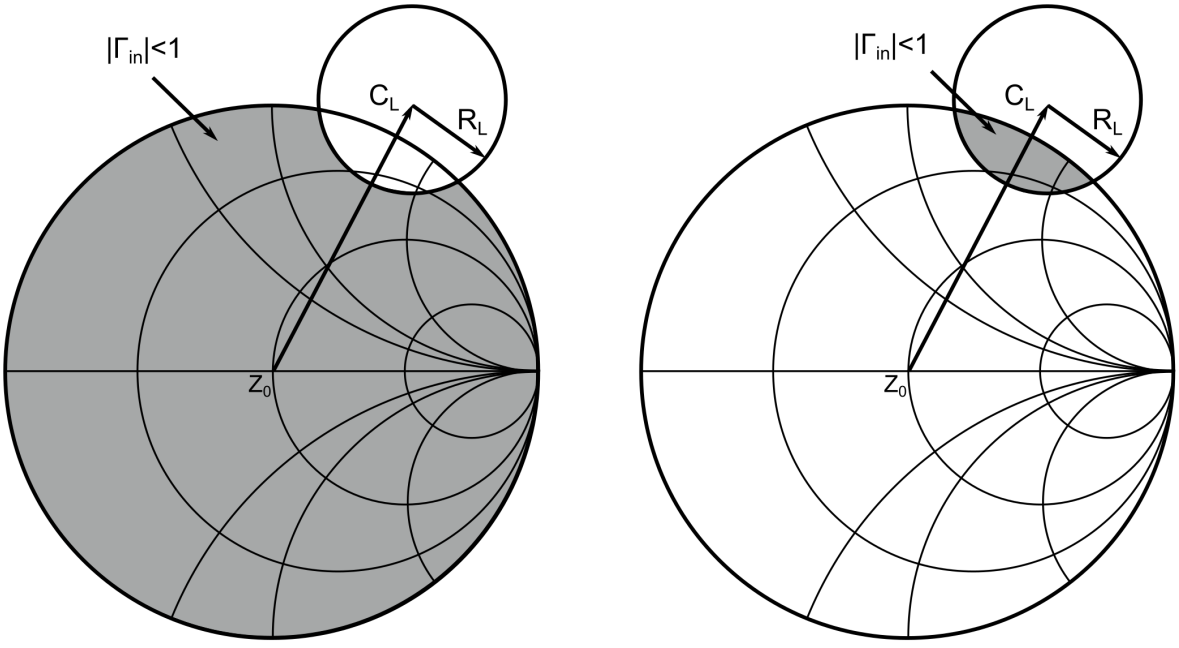
$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \tag{2.17a}$$

$$R_S = \left| \frac{S_{12}S21}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2.17b}$$

Where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.18}$$

Equations 2.16a and 2.17a gives the location of the center of the load and source stability circles, and equations 2.16b and 2.17b gives the radius of the circles. These can then be represented graphically in the smith-chart.



(a) Conditional stability when $|S_{11}| < 1$ (b) Conditional stability when $|S_{11}| > 1$

Figure 8: Conditional stability circles

Figure 8 shows the output stability circle for a active device. On one side of the stability circle $|\Gamma_{7in}| < 1$, and on the other $|\Gamma_{in}| > 1$. To determine which is which consider the following. If the load impedance is equal to Z_0, then $|\Gamma_L| = 0$. Then equation 2.15a gives $|\Gamma_{in}| = |S_{11}|$. If $|S_{11}| < 1$ the amplifier is stable, hence the impedance in the center of the smith chart lies in the stable region. If $|S_{11}| > 1$ the center of the smith chart lies in the unstable region, and the region inside both the smith chart and the stability circle represents the stable region. These two cases are shown in figure 8a and 8b respectively.
For a device to be unconditionally stable, the stability circles must either be wholly outside the smith chart, or completely engulf the smith chart.

A simpler test for unconditional stability is the K-Δ test, or simply K-factor or stability factor, where the device is unconditionally stable if

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.19}$$

and

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.20}$$

The K-factor only shows whether a device is unconditionally stable or not, and gives no indication of how stable a device is. A measurement of stability which does possess this quality are the μ-factors shown in figures 2.21b and 2.21a.

$$\mu_{prime} = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*\Delta| + |S_{21}S_{12}|} \tag{2.21a}$$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{21}S_{12}|} \tag{2.21b}$$

μ-prime gives the distance from the center of the smith chart to the nearest unstable part of the source stability circle, and μ gives the same for the load. If $\mu > 1$ and $\mu_{prime} > 1$ then both stability circles are either located outside the smith chart, or are engulfing the smith chart, and stability is ensured.

2.4.3 Gain/Match

An amplifier can be designed for different purposes. Characteristics of the amplifier is largely decided by the transistor, and the impedances it observes. Manipulating these impedances

will change the current-voltage ratio, affecting power, noise figures, efficiency and gain.

The gain of an amplifier is the ratio between its output, and input. An amplifier designed for voltage gain will generate a large voltage swing compared to that of the input, but a very small current swing and vice versa. An amplifier designed for power gain outputs large swings in both voltage and current. From here on power gain will be discussed.

Commonly three measurements of power gain is used. [3]

Power Gain: $G = {}^{P_L}/_{P_{in}}$ A measurement of power that is independent on Z_s

Available Gain: $G_A = {}^{P_{avn}}/_{P_{avs}}$ A measurement of power that is dependent on Z_s bit not Z_L

Transducer power gain: $G_T = {}^{P_L}/_{P_{avs}}$ A measurement that is dependent on both Z_s and Z_L

The difference between these gain definitions is how they define the impedance match between the device and the source and load networks. If both networks are conjugately matched to the device, the three definitions above will produce the same result. The transducer gain is the most useful of them as it accounts for impedance mismatch, and will therefore be used in the upcoming examples.

$$G_T = G_s G_0 G_L \tag{2.22}$$

where G_s, G_0 and G_L are shown in figure 7 and is defined as

$$G_S = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{in}\Gamma_S|^2} \tag{2.23a}$$

$$G_0 = |S_{21}|^2 \tag{2.23b}$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.23c}$$

By ensuring a conjugate match between the device and the load and source matching networks the gain is maximized.

$$\Gamma_{in} = \Gamma_S^* \tag{2.24a}$$

$$\Gamma_{out} = \Gamma_L^* \tag{2.24b}$$

Since a transistor is a bilateral device Γ_{in} is affected by Γ_{out} and vice versa, and the two must be matched simultaneously. We have

$$\Gamma_S^* = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.25a}$$

$$\Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.25b}$$

and

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{2.26a}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{2.26b}$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta^2| \tag{2.27a}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta^2| \tag{2.27b}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{2.27c}$$

$$C_2 = S_{22} - \Delta S_{11}^* \tag{2.27d}$$

Where the Δ is defined in equation 2.18. Equations 2.26 can only be solved when the term under the square root is positive, which coincides with a stable device ($K > 1$). Once a conjugate match has been achieved the maximum achievable gain is defined as

$$G_{Tmax} = \frac{|S_{21}|}{S_{12}}(K - \sqrt{K^2 - 1}) \tag{2.28}$$

By matching differently the amplifier can also be designed with a minimized noise figure. This is commonly done with low noise amplifiers for wireless receivers, and will not be discussed further here. As with stability circles, gain and noise circles can also be plotted in the smith chart, and be used to create a matching network which attempts to fulfill both gain and noise requirements.

2.4.4 Efficiency

Efficiency is a measurement of the DC to AC energy conversion capabilities of the amplifier. The more power that is lost, usually to heat dissipation, the less efficient the amplifier is. Designing amplifiers with a high efficiency rating allows longer battery time for portable devices, reduced requirements for heat handling, and generally a more environmental friendly product.

The main culprit of efficiency loss in an amplifier is the transistor itself, as it can have a large voltage across it while conducting a large current. This is very much the case in class-A operation as the transistor is constantly conducting current.

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.29}$$

Equation 2.29[3] shows the widely used drain efficiency. It is a simple comparison between power delivered to the load and the DC power delivered to the amplifier. This does not necessarily give a good indication of the actual efficiency as power delivered to the amplifier input can contribute to an increase in output power. For amplifiers with low gain equation 2.29 will give a falsely high result. A measurement which includes input power is power added efficiency, PAE given as

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\frac{P_{out}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\eta \tag{2.30}$$

Here the input power is subtracted from the power delivered to the load, so only output power generated by the amplifier is compared to the delivered DC power. For amplifiers with high gain the output power will be much larger compared to the input power so that

$$P_{out} - P_{in} \approx P_{out} \tag{2.31}$$

Which reduces equation 2.30 to equation 2.29.

Even though PAE gives a better indication for amplifiers with moderatly low gain, it does suffer from a falsely low efficiency number if the gain is very low. If the input power exceeds that of the output power in a very low gain amplifier power added efficiency will become negative, which physically makes no sense. A third option, which does not suffer from this, is Total efficiency. It is defined as

$$\eta_{Total} = \frac{P_{out}}{P_{DC} + P_{in}} \tag{2.32}$$

This gives the efficiency as the ratio of the power out to all power delivered to the amplifier, which makes very much sense physically. This report however, will focus mostly on drain efficiency and PAE. The former because it shows the potential of the concept without worrying about mismatches and low gain, and the latter because it is the most commonly used in radio design.

High efficiency can be achieved by selection of the amplifier bias (amplifier class), and by tuning the harmonics present on the amplifier output. Different amplifier classes has different

conduction angle as shown in figure 6. For inverting amplifiers current and voltage are 180° out of phase. For a class-B amplifier this means the current is zero when the voltage is at its peak, this increases efficiency compared to a class-A amplifier which conducts current at all times. A class-C amplifier spends even more time with its current at zero, further decreasing the overlap between current and voltage which further increases its efficiency.
The harder an amplifier is driven, the higher the efficiency becomes as the voltage drops the more the current increases.[4, p.285] In saturation a minimum overlap between voltage and current is achieved, thus achieving the highest efficiency the amplifier is capable of. When maximum efficiency for an amplifier is discussed it is assumed the amplifier is driven into saturation. Manipulating the harmonics present on the amplifiers output can also increase efficiency as it allows for shaping of the current through, and voltage across, the transistor. For the class-B amplifier the current through the transistor is a half-rectified sine wave, this implies a short for 2. harmonics must be ensured on the output. To further increase efficiency voltage can be shaped by presenting the odd harmonics with a open circuit at the output. This shapes the voltage over the transistor into a square wave, further reducing the overlap between current and voltage which increases efficiency. This is known as a class-F amplifier and is discussed more in section 2.4.7
In this project the main amplifier is biased in very deep AB behaviour. Its efficiency will be close to that of a class-B amplifier which is, as shown in figure 6, somewhere around $70-80\%$. Since the conduction angle of a class-B is $\frac{\pi}{2}$, an avarage of the half period of a sine is first found.

$$A_{av} = \frac{1}{\pi}\int_0^{\pi} A_p \cdot sin(x)\mathrm{d}x \tag{2.33}$$

Where A_{av} is avarage amplitude and A_p is peak amplitude. This then becomes

$$A_{av} = \frac{A_p}{\pi}[-cos(x)]_0^{\pi} = \frac{2A_p}{\pi} \tag{2.34}$$

$\frac{2}{\pi}$ can be multiplied with the peak value of any half-period sine to find its avarage value. The DC power delivered to the amplifier, seen from the power supply, is then

$$P_{DC} = V_{DC} \cdot I_D \cdot \frac{2}{\pi} \tag{2.35}$$

where V_{DC} is the power supply voltage and I_D is the peak of the current delivered to the amplifier from the power supply. The current is shaped as a half-rectified sine, and thus the only contributer to power is the half-period where $I_D \neq 0$ The power out is defined as

$$P_{out} = \frac{V_{DC}I_D}{2} \tag{2.36}$$

Which is simply the power calculated from the RMS values of the voltage and current sine waves the load sees at the fundamental frequency. The theoretical maximum efficiency can now be found as

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{V_{DC}I_D}{2V_{DC}I_D \cdot \frac{2}{\pi}} \cdot 100\% = \frac{\pi}{4} \cdot 100\% = 78.53\% \tag{2.37}$$

This efficiency applies to an ideal amplifier where all networks are lossless, and the amplifier is driven into saturation. The Auxiliary amplifier used for this project is a Class-C amplifier, whose conduction angle depends wholly on the bias point of the amplifier. The efficiency calculation would be similar to that of a class-B, but where the integral in equation 2.33 has different limits to represent its conduction angle.

2.4.5 Load line

A handy tool when designing an amplifier is the amplifiers load line, which is a plot of the current and voltage seen by the internal, and ideal, current source of the transistor, shown in figure 4. The load line is often plotted along with the DC-characteristics of the transistor as they complement each other. An example of the load line for a class B amplifier can be seen in figure 9.

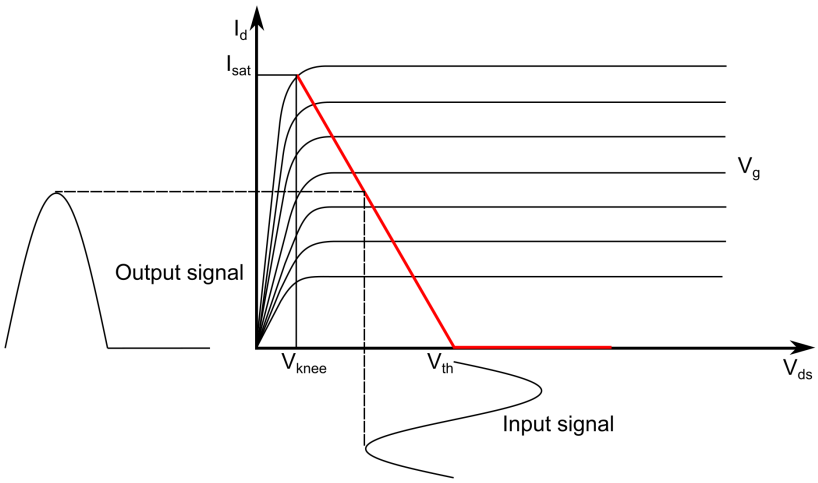


Figure 9: Ideal load line of a class B amplifier with input and output signals.

To achieve maximum output power the load line should ideally be angled as in figure 9, where the maximum current swing reaches the point where the angle of the tangent line of the knee is 45°. This will ensure the combination of the largest current and voltage swing. This should not be confused with matching for maximum power transfer, as that refers to impedance matching

between the amplifier and the load to minimize Γ_L. The relationship between current and voltage is affected by the load impedance seen by the amplifier, and therefore affects the load lines slope.

The load which gives the specified loadline can calculated as shown in equation 2.38.

$$R_{opt} = \frac{\Delta V}{\Delta I} = \frac{V_{th} - V_{knee}}{Isat} \tag{2.38}$$

Where V_{th} is the drain-source voltage for which the current becomes zero. Ideally the current source of the transistor should see a completely real impedance, i.e. reactance equal to zero, as is depicted in figure 9, but in reality the reactance will be non-zero due to parasitics. Charging and discharging of these parasitics causes memory effects, which manifests itself as looping in the load line. Also, the current at the threshold voltage in the figure above goes sharply to zero, which would demand a summation of all even harmonics, which is practically impossible.

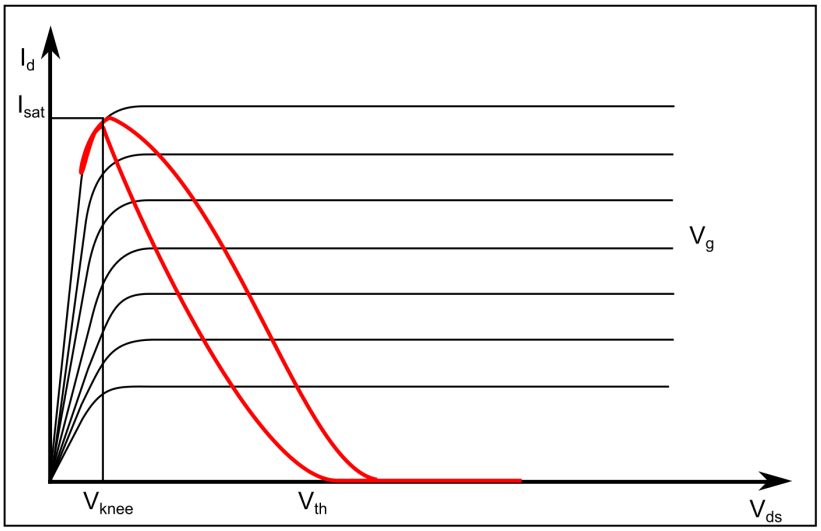


Figure 10: Example of real effects in loadline of a class B amplifier.

Figure 10 is an example of a more realistic loadline. As mentioned above the current at V_{th} is not as sharp as in the ideal case due to even harmonics not being properly shorted. The dip in current seen at the knee is due to the emergence of odd harmonics, and most prominently the third harmonic, which reduces the the peak of the current. The drain-source voltage is allowed to swing from just below V_{knee} to $2 \cdot V_{DC}$ at saturation. The voltage is allowed to swing like this due to the DC-feed inductor shown connected to the amplifiers drain terminal in figure 5.

2.4.6 Distortion

The transistor is a non-linear device and this has consequences for the output signal. The transistor characteristic can be divided into three sections, Cut-off, linear region, and saturation. Cut-off is when the gate-source voltage (V_{GS} is lower than the transistor threshold, meaning it will not conduct current. In saturation V_{GS} is too large, and the transistor is conducting as much current as it is capable of. Between these two extremes is the linear region, where the output signal is approximately a linear function of the input signal. Amplifiers operating purely in this region, such as class-A, should in theory amplify a given signal without changing it. In reality the linear region isn't ideally linear, and the non-linear regions of the transistor behaviour physically affects the current and voltage waveform, which gives rise to additional signal components with harmonic frequencies. Figure 11 shows the frequency components present when a two-tone signal is presented to a non-linear device.

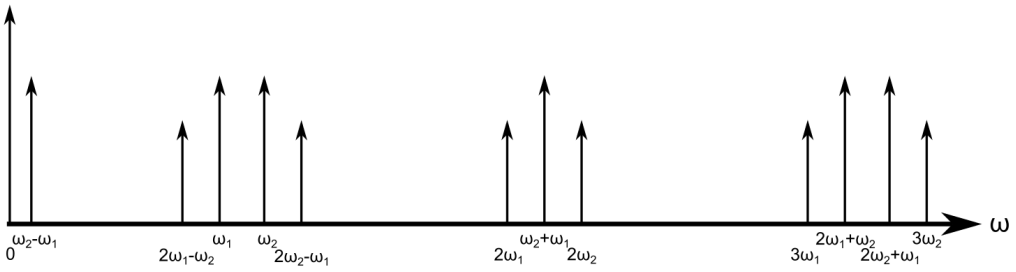


Figure 11: Intermodulation distortion[3]

In addition to second and third harmonics of ω_1 and ω_2, subtraction and addition of the different components takes place, these are called intermodulation products. They give rise to even more frequency components, some of which lie so close to the fundamental frequencies they can not be filtered out. In figure 11 these signals are marked $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. Another potential troublemaker is marked $\omega_2 - \omega_1$, as it lies very close to DC, and can therefore potentially affect the power supply. Since operation in the linear region has very low harmonic components class-A amplifier excels at linearity, while classes AB, B and C must have harmonic filtering at the output to ensure low distortion delivered to load.

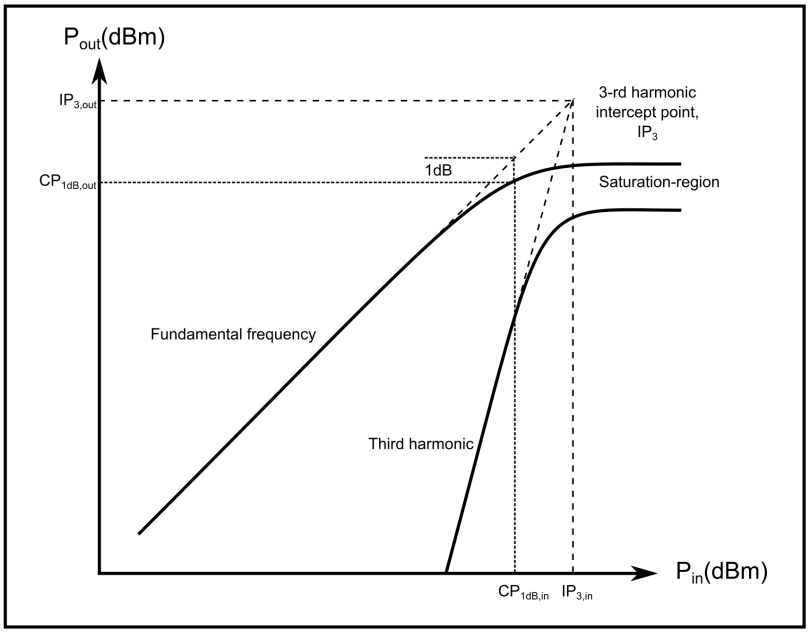


Figure 12: 1dB compression point, and third harmonic intercept point

2.4.7 Class-F Amplifier

Beyond the traditional class-A, class-AB, class-B and class-C amplifier classes, which are only defined by their Bias point, several modified classes or sub-classes exists. One of these are the class-F amplifier, which is a modified class-B amplifier which uses the over-harmonics to achieve higher efficiency. The basic concept is that by adding odd-harmonics on the voltage and even-harmonics on the current, the peak amplitude is reduces and the transistor voltage V_{DS} can be driven harder, allowing more of the DC power to be converted to RF power at high input drive levels. The theory explained here are taken from [4][p.143].

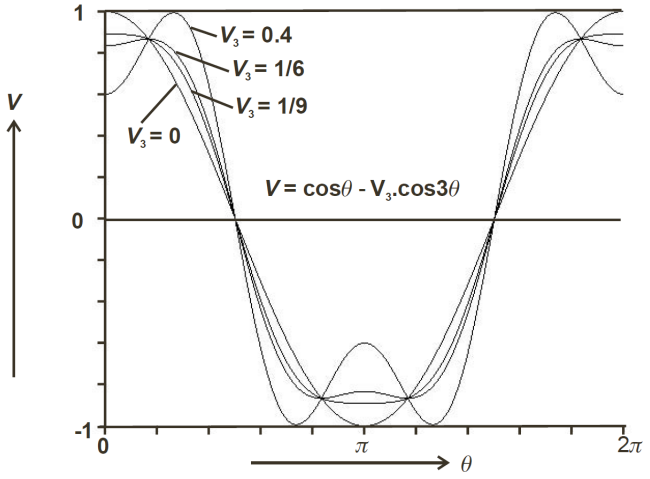


Figure 13: Third harmonic squaring effect, [4][p.143]

Figure 13 shows the waveform of $V = \cos(\theta) - V_3 \cos(3\theta)$ for various values of V_3. A generic input signal with fundamental and third harmonic can be given as

$$v(\theta) = V_1 \cos(\theta) - V_3 \cos(\theta) \tag{2.39}$$

Then, any value of $V_3/V_1 < 1/9$ yields a single amplitude peak, given as $V_{pk} = (V_1 - V_3)$, while values of $V_3/V_1 > 1/9$ yields a double peak. Both of which are shown in figure 13. The value of the double peak decreases up to the global maximum point of $V_3/V_1 = 1/6$, to which V_{pk} reaches its global minimum point of

$$V_{pk} = \frac{\sqrt{3}}{2} V_1 \tag{2.40}$$

For V_3 values higher than $V_1/6$, the amplitude of the waveform increases. Thus by only adding 3rd harmonics, a maximum possible amplitude decrease given by equation 2.40 can be achieved. By deducting equation 2.39, it can be seen that for V_3 values of $0 \geq V_3 \geq V_1/2.5$, the corresponding waveform amplitude are decreased by a factor κ, making $V_{pk} = \kappa V_1$. This makes the maximum possible amplitude increase from $V_{max} = V_1$ to $V_{max} = V_1/\kappa$. The increased value of V_{max} allows more of the DC power to be converted to RF power, yielding a maximum theoretically drain efficiency of $\eta = 90.7\%$. Dependency of η and its corresponding potential increased P_{out} to the 3rd harmonic amplitude V_3 are given in figure 14, where the amplitude is normalized as $v_3 = V_3/V_1$.

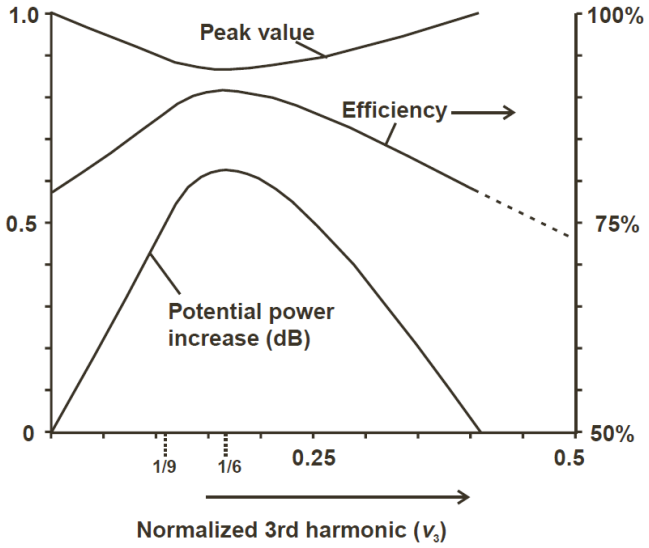


Figure 14: Reduction in amplitude, with corresponding efficiency and increased $P_{out,dB}$, [4][p.145]

v_1	v_3	v_5	v_7	$P(dB)$	$\eta[\%]$
1	-	-	-	0	78.5
1.155	0.1925	-	-	0.625	90.7
1.207	0.2807	0.073	-	0.82	94.8
1.231	0.3265	0.123	0.0359	0.90	96.7

Table 1: Class-F optimal results

2.4.7.1 Maximal flat waveforms Adding the odd over-harmonics naturally alters the waveform of both the voltage and current across the transistor. As explained above, values of $V_3 < V_1/9$ yields single peaks while $V_3 > V_1/9$ yields double peaks. Thus the case $V_3 = V_1/9$ is the maximal flat waveform possible only using 3rd harmonics, yielding $\kappa = 9/8$ and $\eta = 88.4\%$. The voltage and current waveform of this values are given in figure 15, and these waveforms are interesting as they may occur unintentionally, as will be seen in section 4

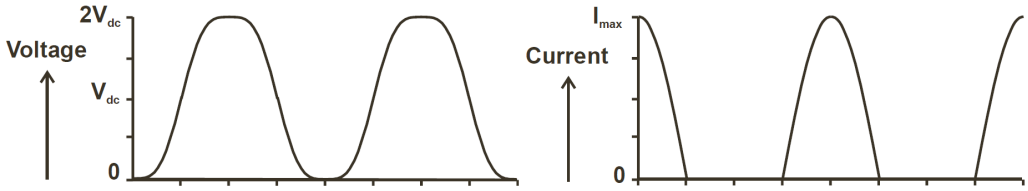


Figure 15: Voltage and current waveform for $V_3 = V_1/9$, [4][p.145]

2.4.7.2 Higher order odd-harmonics Theoretically its possible to add any number of odd over-harmonics to achieve a perfect square voltage signal, which would increase the maximum possible peak amplitude to $V_{max} = (4V_1)/\pi$, giving $\kappa = \pi/4(\approx 1dB)$. The mathematically deduction of the signal using higher order odd harmonics are similar to the above, but for sake of simplicity, the most important results are given in table 1, where the normalized odd harmonic amplitudes are given together with the potential increased power in dB and the corresponding efficiency. The table only gives up to 4 odd over-harmonics, but adding a infinite number would yield $\eta = 100\%$.

2.5 Load pull

Load pull is a term which originates from oscillator design, where the oscillators change of frequency as function of load impedance is measured. [4, p.359] For amplifiers load pull measurements has traditionally been used to determine matching requirements for amplifiers.

Another use is a technique known as active load pull, which involves changing the perceived impedance of a load by applying current through it from a second current source.

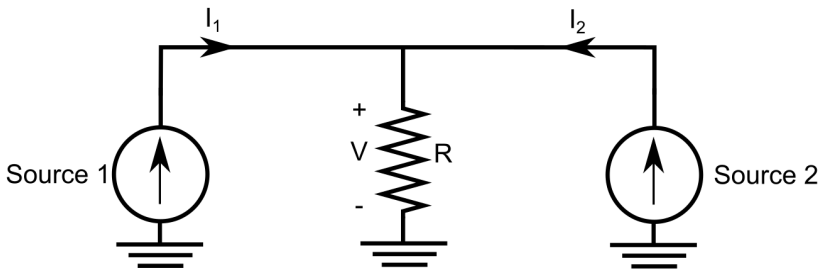


Figure 16: Loadpull circuit

Figure 16 shows a basic circuit for active load pull. The impedance seen from source 1 can be expressed as

$$R_{L1} = \frac{V}{I_1} = \frac{R \cdot (I_1 + I_2)}{I_1} = R(1 + \frac{I_2}{I_1}) \tag{2.41}$$

and similarly for source 2

$$R_{L2} = \frac{V}{I_2} = \frac{R \cdot (I_1 + I_2)}{I_2} = R(1 + \frac{I_1}{I_2}) \tag{2.42}$$

For source 1, when $I_2 = 0$ equation 2.41 reduces to the actual load resistance. But when $I_2 \neq 0$ the fraction in the right hand term becomes greater than zero, and the perceived resistance increases. When $I_2 = I_1$ the load resistance seen by source 1 is twice that of the actual resistance. If we apply the same analysis for source 2 we find the resistance begins at infinity, due to a zero in the denominator in the right hand term, and and reduces to twice that of the load resistance. so we have

$$R \leq R_{L1} \leq 2R \tag{2.43a}$$

$$\infty \leq R_{L2} \leq 2R \tag{2.43b}$$

in figure 17 the change in impedance seen by a source is illustrated. When the second source is zero, current-voltage ratio follows the plain line. Once the second source starts conducting, and the resistance increases the current is reduced, causing a decrease in the load line slope as the dashed lines illustrate.

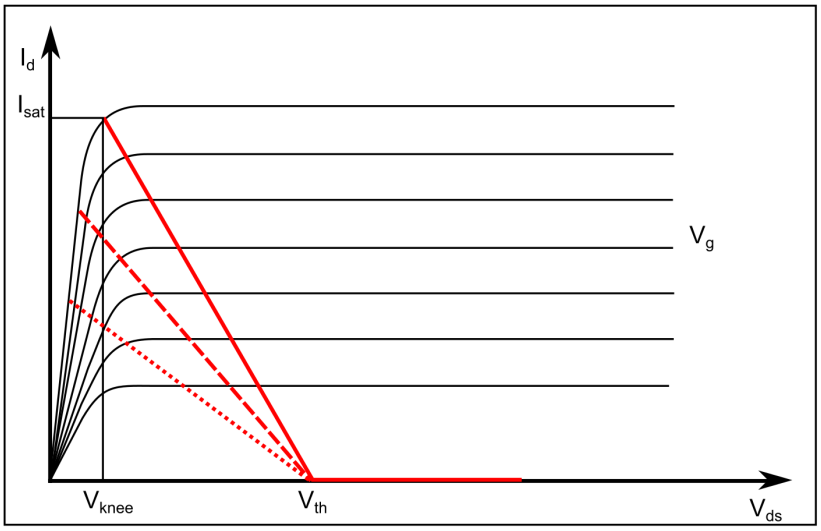


Figure 17: Loadpull effect on ideal loadline

2.6 The Doherty amplifier

As the Doherty amplifier is the basis of the modified amplifier it will be described in detail in this chapter, first discussing general operation before moving on to efficiency calculations.

2.6.1 Theory of operation

An amplifier topology which uses the active load pull technique is the Doherty amplifier. First developed by William Humphrey Doherty in 1936 while working with bell laboratories [5][6], the Doherty amplifier was designed in an attempt to increase efficiency without decreasing the signal quality. The amplifier works especially well for signals with a high peak to avarage ratio [4], meaning the signal normally has a relativly low amplitude, but can greatly increase for certain symbols. The power amplifier handeling the signal must be large enough to handle the peak amplitudes, and this causes low efficiency at the lower amplitudes, where the signal spends most of its time due to a higher number of symbols being represented there.

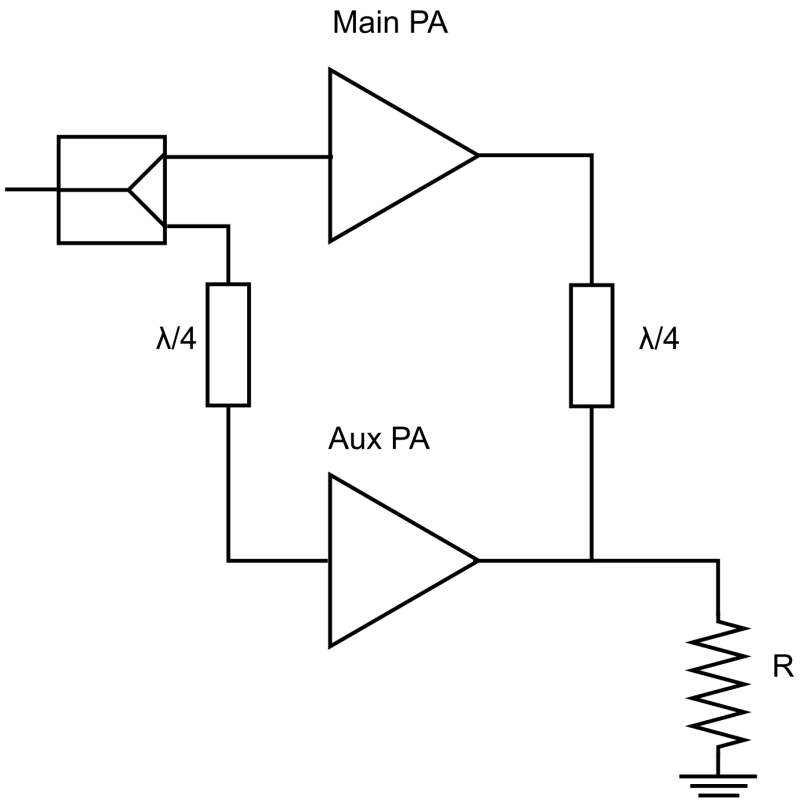


Figure 18: The Doherty amplifier topology

The topology consists of two amplifiers in parallel, separated by a splitter, and a $\lambda/4$ transmission line on the input, and only a $\lambda/4$ transmission line on the output. Figure 18 shows the two amplifiers. The system works similarly to basic load pull as described in section 2.5, the difference being the transmission line seperating the amplifiers output. When the main amplifier operates below saturation, it behaves as a current source, as seen in figure 19, and the voltage across the load is determined by the current flowing through it.

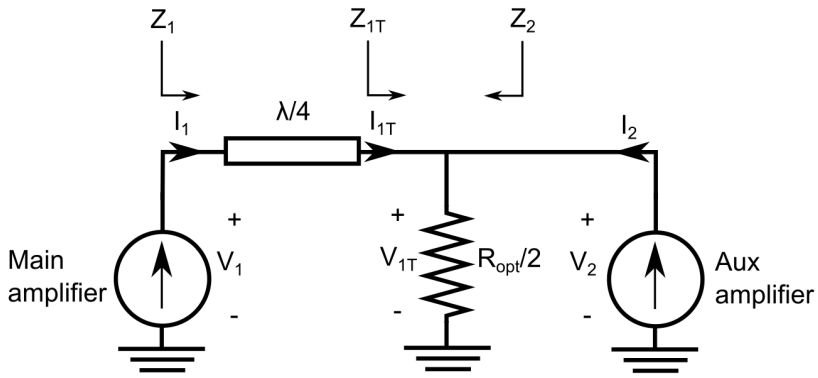


Figure 19: Principle of doherty operation

When the input signal is small the Aux amplifier is turned off, and only the Main amplifier will be conducting current. After the input signal reaches a certain power level the Aux amplifier will begin to conduct current, increasing the total current through the resistance R. The final power delivered to the load will be a combination of both devices, and each of them typically delivers half the power, as illustrated in figure 20. The input drive level for which the Aux amplifier turns on is then 6dB below the maximum delivered power. Since only the Main amplifier conducts when the drive signal is below the 6dB backoff point, it is natural to divide the amplifier operation into two, namely below and above the backoff point. The amplifier currents for operation above the backoff point can then be defined as

$$I_1 = \frac{I_{max}}{4}(1+\xi) \tag{2.44a}$$

$$I_2 = \frac{I_{max}}{2}\xi \tag{2.44b}$$

Where I_{max} is the maximum current delivered by the doherty amplifier, and ξ is the normalized input power for the upper 3/4th input power, such that $0 < \xi < 1$ for $P_{max}/4 \leq P_{in} \leq P_{max}$. Then we apply this to the load pull techniques as seen in equations 2.41 and 2.42, but modified for the circuit seen in figure 19, to obtain the observed impedances.

$$Z_{1T} = \frac{R_{opt}}{2}(1+\frac{I_2}{I_{1T}}) \tag{2.45a}$$

$$Z_2 = \frac{R_{opt}}{2}(1+\frac{I_{1T}}{I_2}) \tag{2.45b}$$

$$R_{opt} = V_{dc}\frac{2}{I_{max}} \tag{2.45c}$$

$$Z_1 = \frac{Z_T^2}{Z_{1T}} = \frac{2Z_T^2}{R_{opt}(1+\frac{I_2 Z_T}{U_1})} \tag{2.45d}$$

Equation 2.45a and 2.45b now contains I_{1T} which is current I_1 transformed through the quarter-wave transmission line, and R_{opt} which is the optimum loadline impedance for power described in equation 2.38. By chosing $Z_T = R_{opt}$ the equations show that unlike the observed impedance from section 2.5 the amplifiers see the following impedance changes

$$2R_{opt} \leq Z_1 \leq R_{opt} \tag{2.46a}$$

$$\infty \leq Z_2 \leq R_{opt} \tag{2.46b}$$

The load line of the main amplifier now rises, instead of falling, and behaves opposite of what is shown in figure 17, allowing the current from the amplifier to increase after it originally reached saturation. The voltage can be found by substituting equations 2.45d and 2.44a into $V_1 = I_1 Z_1$

$$V_1 = (\frac{Z_T}{R_{opt}})(\frac{I_{max}}{2})[Z_T + \xi(Z_T - R_{opt})] \tag{2.47}$$

and having $Z_T = R_{opt}$ leads to

$$V_1 = R_{opt}(\frac{I_{max}}{2}) \tag{2.48}$$

Which shows the voltage is no longer dependent on the input power, and will ideally be constant after the 6dB-backoff point as shown in figure 21b

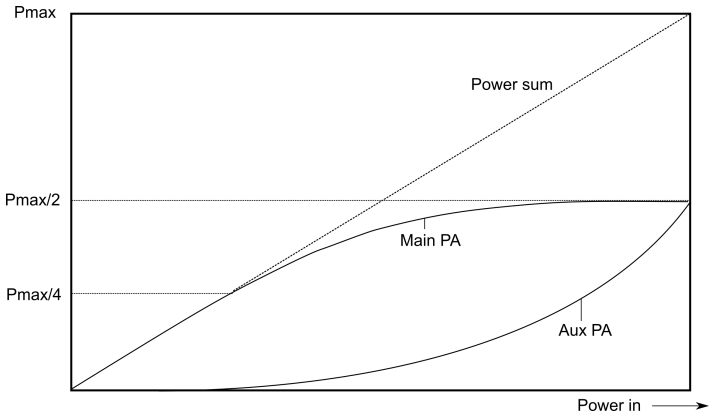
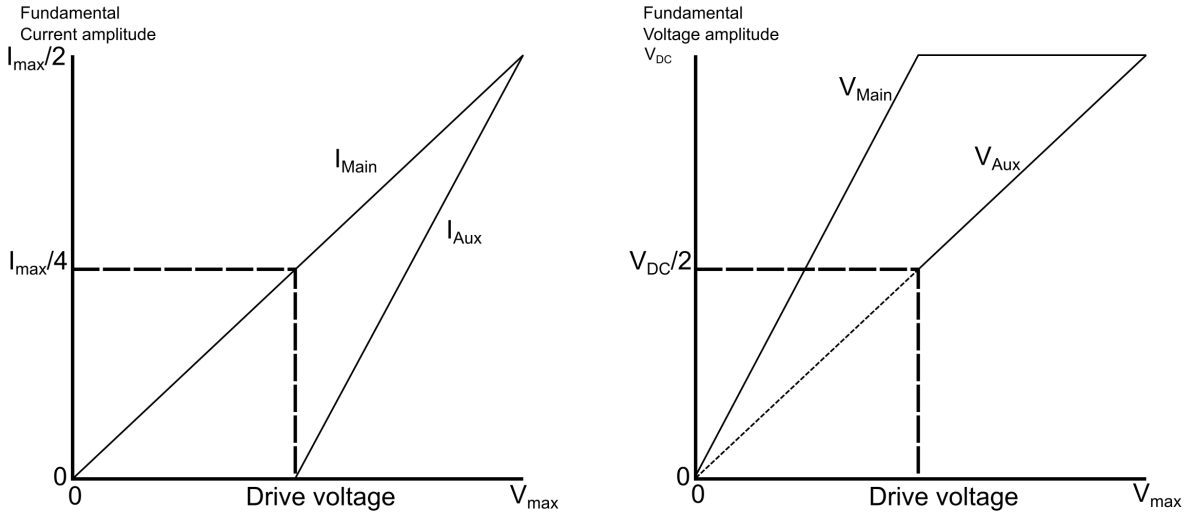


Figure 20: Power output from amplifiers in Doherty



(a) Fundamental currents

(b) transistor voltages at fundamental

Figure 21: Current and voltage characteristics of the Doherty amplifier[4]

The voltage across the load resistor observed by both amplifiers is V_{1T}, as the transmission line in figure 19 is considered lossless. This fact combined with equation 2.14, gives the following expressions for voltages and currents across the transmission line

$$V_{1T} \cdot I_{1T} = V_1 \cdot I_1 \tag{2.49a}$$

$$(\frac{V_{1T}}{I_{1T}}) \cdot (\frac{V_1}{I_1}) = Z_T^2 \tag{2.49b}$$

There is a phase difference of 90° between I_1 and I_{1T}, but it is omitted here. Again by setting $Z_T = R_{opt}$, this reduces to

$$V_{1T} = I_1 \cdot R_{opt} \tag{2.50}$$

Which is the final composite RF voltage across the load. When the main amplifier reaches saturation, it changes behaviour from a voltage controlled current source to a voltage source. This prevents the voltage over the load from increasing, and sets the current through it. Since voltage sources have a very low output impedance, any excess current supplied by the auxiliary source will ground itself in the voltage source. The quarter wave transformer changes the observed impedance of the main amplifier from low to high, thus changing its behaviour back to that of a current source.

2.6.2 Efficiency

Based on the definitions above the Doherty efficiency characteristics can be developed, which is an important part considering the topology was designed to give enhanced efficiency compared to traditional amplifier designs. As before the operation of the doherty is divided in two, below and above the 6dB back-off point. When below the back-off point only the main amplifier is conducting and is designed to reach its maximum efficiency at $P_{in} = P_{in,max}/4$, once above the back-off point the main amplifier will stay close to saturation as P_{in} increases and the current from the aux amplifier modifies the main amplifiers load-line. This means the main amplifier remains close to maximum efficiency, which ideally is 78.5% assuming a class B amplifier. The auxiliary amplifier will not reach its peak efficiency until P_{in} is at its maximum, but due to the low power contribution at lower signal levels the overall efficiency loss is rather low. [4] Below the back-off point the efficiency of the main amplifier can be expressed as

$$\eta_{comp} = \frac{2v_{in}}{V_{max}}(\frac{\pi}{4}), 0 \leq v_{in} \leq \frac{V_{max}}{2} \tag{2.51}$$

Above the 6dB back-off the calculations become more complex. In accordance with figure 19 and equation 2.50 the composite output power can be expressed as

$$P_{comp} = I_1^2 \cdot R_{opt} \tag{2.52}$$

Then by combining equations 2.44a, 2.45c and 2.52 along with $(1+\xi) = 2v_{in}/V_{max}$ it becomes

$$P_{comp} = \left(\frac{I_{max}}{2}\right) \cdot \left(\frac{v_{in}}{V_{max}}\right)^2 \cdot V_{dc} \tag{2.53}$$

Note that in the source litterature [4], from which all the formulas are taken, equation 2.53 has an error as it lacks the square exponential. If both the main and the auxiliary amplifier are of ideal class-B, and the auxiliary turns itself on at the 6dB back-off point, the DC power consumption for the individual power amplifier, and the resulting total DC power consumption can be expressed as

$$P_{DCM} = \left(\frac{v_{in}}{V_{max}}\right)\left(\frac{I_{max}}{\pi}\right) \cdot V_{dc} \tag{2.54a}$$

$$P_{DCA} = 2 \cdot \left(\frac{v_{in}}{V_{max}} - 0.5\right)\left(\frac{I_{max}}{\pi}\right) \cdot V_{dc} \tag{2.54b}$$

$$P_{DC} = \left(\frac{I_{max}}{\pi}\right) \cdot \left(3\left(\frac{v_{in}}{V_{max}} - 1\right)V_{dc}\right. \tag{2.54c}$$

By combining equation 2.53 and 2.54c

$$\eta = \frac{P_{COMP}}{P_{DC}} = \frac{\pi}{2} \cdot \frac{\left(\frac{v_{in}}{V_{max}}\right)^2}{3 \cdot \left(\frac{v_{in}}{V_{max}}\right) - 1} \tag{2.55}$$

Equation 2.55 shows us $\eta = \pi/4 = 78.5\%$ for both $v_{in} = V_{max}/2$ and $v_{in} = V_{max}$, this shows us the ideal Doherty amplifier first reaches maximum for its amplifier class at half of the maximum input drive, and again for the maximum drive. Between these two points the efficiency remains high, dropping a little due to the low efficiency of the auxiliary amplifier just after it has begun conducting. Figure 22 shows the efficiency compared to that of a class-B amplifier. If the auxiliary amplifier class is C instead of B, the efficiency will rise even higher towards V_{max}, as the class-C amplifier is generally more efficient than a class-B.

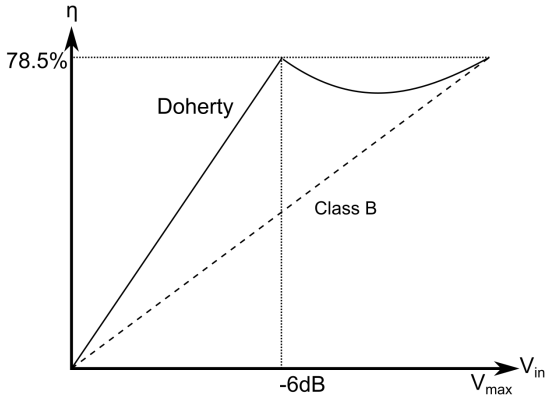


Figure 22: Efficiency of ideal doherty amplifier

2.6.3 Practical implementation of the Doherty amplifier

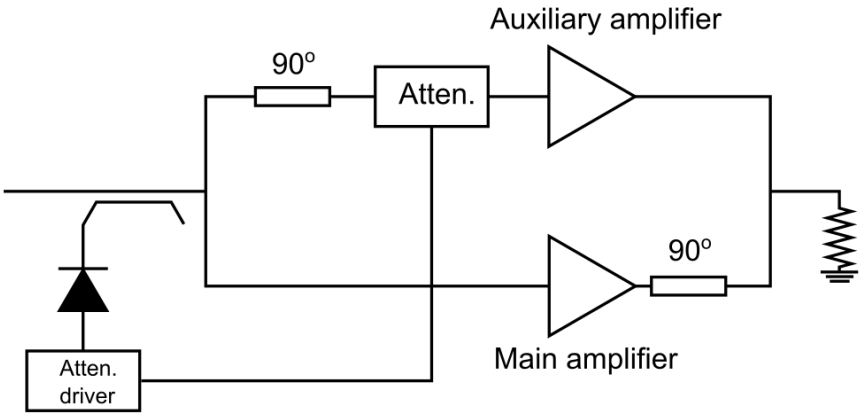
In the above section it was assumed both main and auxiliary amplifiers were class-B amplifiers, where the auxiliary magically started conducting as the main amplifier reached half its maximum output power. As the auxiliary amplifier can't just turn itself on, this subsection will look at a couple of techniques to achieve the desired behaviour. Controlling when the auxiliary begins to conduct in relation to the main amplifier is very important as it, through load modulation, affects the load impedance observed by the main amplifier. This affects efficiency, linearity in delivered output power, and the range of input drive levels within the high efficiency area of operation. There are two commonly used topologies which will briefly be discussed, the use of an attenuator in front of a class-B auxiliary, and biasing the auxiliary as a class-C amplifier.

2.6.4 Doherty realized with attenuator

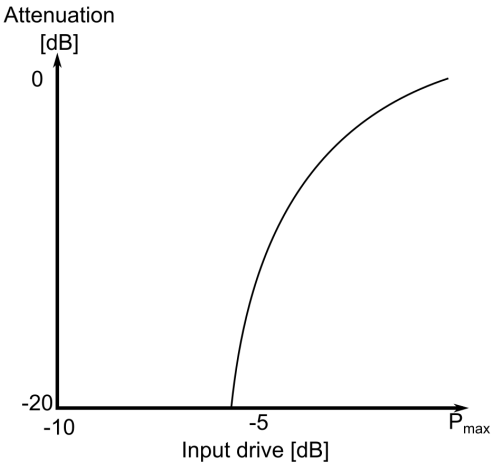
In order to realize the Doherty with two class-B amplifiers the auxiliary input signal can be attenuated in such a way that it doesn't conduct until the input signal reaches a certain drive level. This can be realized as shown in figure 23a which shows an ideal attenuator controlled by the input signal. The attenuation should follow the characteristics shown in figure 23b, completely reducing the signal until the input drive reaches the 6dB-backoff point. The attenuator would have to take care of the necessary cut-off and gain adjustment functions to achieve the Doherty characteristics shown in figure 21a. The attenuation characteristics of fire 23b can be expressed as

$$A_{aux}(dB) = 20 \cdot \log\left[2\Big(1 - \frac{V_{max}}{2v_{in}}\Big)\right], \frac{1}{2} \leq \frac{v_{in}}{V_{max}} \leq 1 \tag{2.56}$$

This method requires additional circuitry due to the input signal dependency of the attenuator and adds an extra level of complexity. It is therefore not pursued further in this project.



(a) Doherty with auxiliary attenuator



(b) Attenuation characteristics

Figure 23: Attenuation characteristics

2.6.5 Doherty realized with class-C auxiliary amplifier

A simpler, and more common, approach is the use of a class-C auxiliary amplifier. The auxiliary amplifier is biased so it does not conduct current until the 6dB-backoff point is reached. Once it starts conducting it will conduct linearly increasing current until the input drive reaches its maximum, at which point the class-C should reach saturation, optimizing its efficiency. This method does not require additional circuitry compared to the class-B amplifier and the efficiency at V_{max} will be higher than shown in figure 22, due to class-C naturally having higher efficiency. Because of the inherent benefits of using a class-C amplifier, this approach was chosen for this project.

2.7 Envelope Tracking

Envelope tracking is a method used to increase the efficiency of amplifiers by keeping the amplifier close to saturation at all times. This is commonly used for classes A, AB and B, and not high efficiency, non-linear amplifiers. [7] This is done by manipulating the amplifiers supply voltage, drain-voltage for FET, so it follows the envelope of the input signal. Figure 24 shows a amplitude-modulated signal, and its envelope, with some headroom, marked in red. By providing the amplifier with enough headroom to prevent significant clipping it can approach its maximum efficiency, and hold it for a large range of input drive voltages without distorting the output signal.

Figure 25 shows a general envelope tracking circuit, where part of the input signal is split off by a coupler, its envelope is detected using a diode detector. It is then sent to a power conditioner which functions as power supply for the output amplifier.

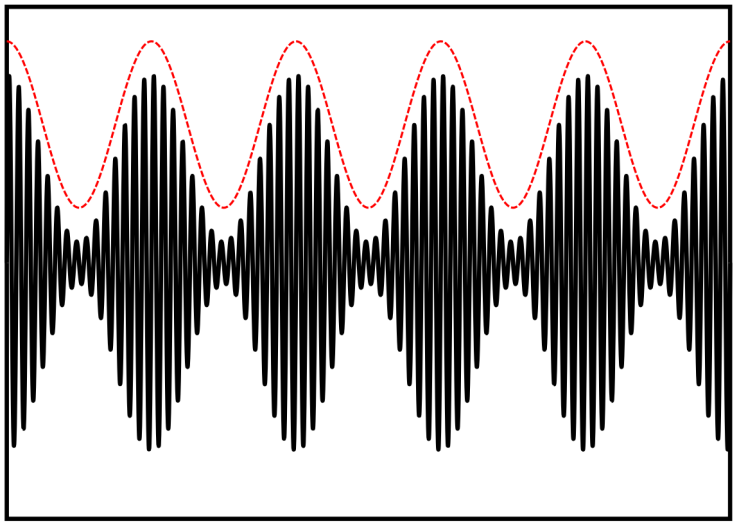


Figure 24: Example of envelope tracking a AM signal.

The tracking does not have to closely follow the signal, somewhat close can be good enough for a significant increase [4]. But the more closely the tracker follows the signal the better the efficiency becomes. The circuit for envelope tracking is in no way connected to matching circuitry, meaning the amplifier can be designed as it would without ET and the tracking just comes in addition. The most basic envelope tracking methods involves simply switching between discrete voltage levels. More advanced can follow the envelope more fluidly, but it quickly becomes advanced. Also sharp changes in the voltage requires a system capable of generating signals over a large bandwidth, which greatly increases the trackers complexity. Usually compromises are made, and the sharpest notches and largest transients are avoided.

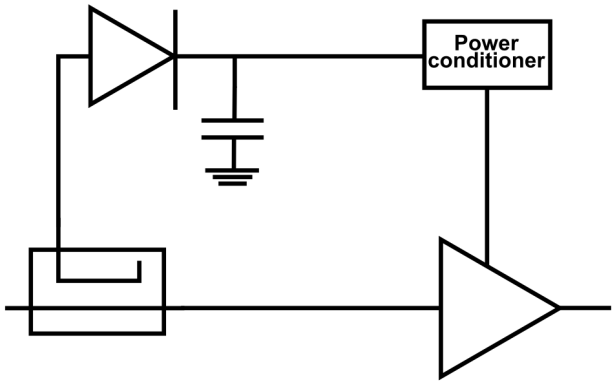


Figure 25: Circuitry for envelope tracking.

2.8 OLMET, the modified amplifier

As mentioned before the goal of this project is to modify the Doherty amplifier, and obtain an amplifier with larger bandwidth but the same characteristic efficiency curve. The quarter wave transmission lines of the Doherty is its greatest limitation in terms of bandwidth, as a quarter wave line, and hence also the Doherty amplifier, is typically said to have a bandwidth of less than 10% of its center frequency. By removing the transmission line the amplifiers bandwidth is now mostly limited by its input and output networks, but it destroys the very reason the Doherty amplifier works in the first place, the impedance transformation. With the transmission line gone the amplifier will behave as described in section 2.5, which means the current of the main amplifier will be limited as the auxiliary amplifier conducts more current, due to the increase in load impedance as seen in equations 2.43. Eventually when the main amplifier enters saturation, it will change behaviour from current source to voltage source, which then dictates the voltage over the load. To resolve this issue the main amplifier must be kept from saturation, and its loadline must reach R_{opt} when P_{in} is at its maximum, even though the loadline now is falling instead of rising. The solution used in this project, is envelope tracking.

By tracking the drain voltage of the main amplifier it can be kept close, but not quite in, saturation. And by increasing the drain voltage proportional to the fall of the load line a doherty-like behaviour, as seen from the load, can be achieved. Figure 26 shows the general behaviour of the loadline of the main amplifier. As the amplifier will be kept close to saturation, its efficiency can be expected to behave as is described in section 2.7, and as the amplifier still ends up with the optimal load line for power amplification, the overall efficiency curve for the entire device should be similar to that of the Doherty amplifier.

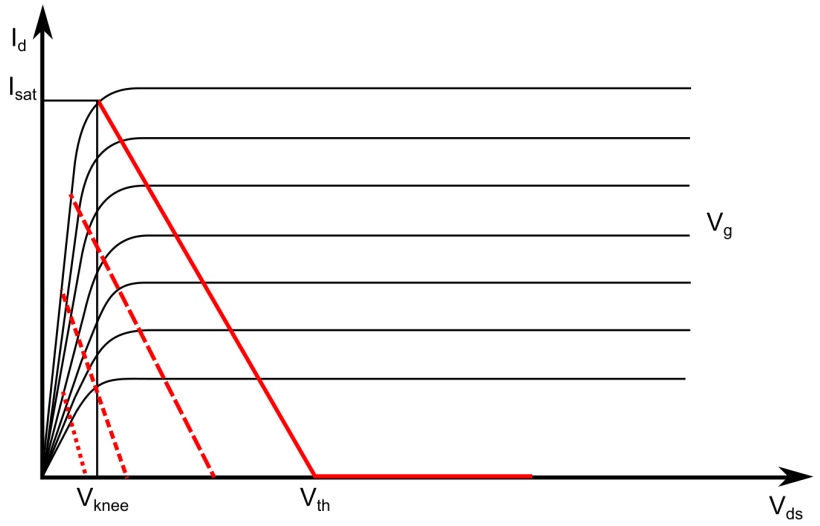


Figure 26: Load line of the modified amplifier.

2.9 Gallium Nitride (GaN)

2.9.1 Basic semiconductor theory

Gallium Nitride is a semiconducting material which is a compound of the chemical elements Gallium (Ga) and Nitrogen (N). A semiconductor is in essence a material that conducts electricity under some conditions, and not for others. This allows for active components, such as transistors and diodes. In its fundamental properties, a semiconducting material has 4 electrons in its outer electron shell, out of a total of 8 (true for the second shell and true only in basic chemistry, disregarding any quantum theory). Thus the material itself is electrically neutral. By doping the material with either electrons or holes (lack of electron) makes the material either negatively or positively charged. This slight electron inbalance makes it possible for the semiconductor to change between behaving as a insulator and as a conductor, depending on outer conditions. In the periodic table, Gallium has 3 valence electrons and Nitrogen has 5 valence electron, giving their compound 4 valence electrons before doping.

2.9.2 The GaN Advantage

The best way to explain the properties of GaN is to compare some of its basic properties to other materials, mostly semiconductors, which is done in table 2. The table are taken from a presentation slide found at [8]. The value of E_g gives the energy gap, alas band-gap, and is the range where no electrons can exist. GaN has the highest E_g-value among semiconductors in the table, which means GaN are able to support higher internal electric fields. High E_g also means it has a higher breakdown voltage compared to other semiconductors, which means

Material	$E_g(eV)$	ϵ_r	$K(W/^\circ K - cm)$	$E_c(V/m)$
Vacuum	-	1	-	-
Si	1.12	11.9	1.5	3×10^5
GaAs	1.43	12.5	0.54	4×10^5
InP	1.34	12.4	0.67	4.5×10^5
3C-SiC	2.3	9.7	4	1.8×10^6
4H-SiC	3.2	10.0	4	3.5×10^6
6H-SiC	2.86	10.0	4	3.8×10^6
GaN	3.4	9.5	1.3	2×10^6
Diamond	5.6	5.5	20-30	5×10^6

Table 2: Comparison of semiconductors

GaN are able to support more W/m^2. Next, its relatively low dielectric constant, ϵ_r means lower capacitive loading, and are as a result able to support higher RF currents. Also, a lower ϵ_r value means a higher propagation speed through the device. Furthermore, it has relatively good thermal conductance, K, which means dissipated thermal power can be extracted from the device more easily. Lastly, the value of E_c gives the carrier mobility, which is also seen to be high. A higher E_c-value means electrons can move faster through the material, which allows for a higher operating frequency without adding significant parasites. To sum up, GaN performs well over a range of variables, making it a preferred material in MMIC, where all the above mentioned parameters are important for overall performance. As GaN is not a ferromagnetic material, its relative permeability, $\mu_r = 1$.

2.9.3 HEMT

High electron mobility transistors, or heterostructure Fet[9], are field effect transistors which uses the junction between two materials with differing band gap levels as conduction channel, rather than using regions of doped versions of the intrinsic material. The combination of Gallium arsenide (GaAs) and Aluminium gallium arsenide (AlGaAs) is quite common, but Gallium nitride and Aluminium gallium nitride is growing in popularity due to their ability to handle higher power. An illustration of a GaN/AlGaN HEMT is shown in figure 27. The 2DEG abbreviation stands for 2-dimensional electron gas, which forms due to free electrons wandering from the AlGaN layer, down to the GaN layer due to the lower energy band level of GaN. This gas, or plasma, is free to move in any direction but vertical, and helps improve the gain of the transistor at high frequencies. Figure 28 shows the energy bands for the first two layers in an section under the gate.

The conduction band, E_c, and the valence band, E_v, represents the two energy states the electrons can have. The area between them are energy states the electrons cannot have. The

fermi-level, denoted E_f is the highest energy level containing an electron. Semiconductor technology is based on having the fermi-level between these two bands. As the valence band is entirely below the fermi-level, the electrons there are unable to move. Similarily there is no current due to the conduction band either as the fermi level lies entirely beneath it. In HEMT transistors there is a portion of the conduction band which dips below the fermi level, which means there will be free electrons present even when no voltage is applied. This dip is caused by the increased number of electrones in that part of the cross section. The electrons moving from the AlGaN layer "sees" a high net negative charge, and their energy is therefore increased, leading to the heightened tip just before the dip. The dip itself is formed by the electrones in the GaN section observing an abundance in positive charge carriers from the donors in the AlGaN material, which reduces the electrons energy.

As energy is delivered to the materials from an increasing input signal E_f rises, causing more and more electrons to enter the conduction band. The transistor will quickly begin conducting current as the electrones in the 2DEG is already free.

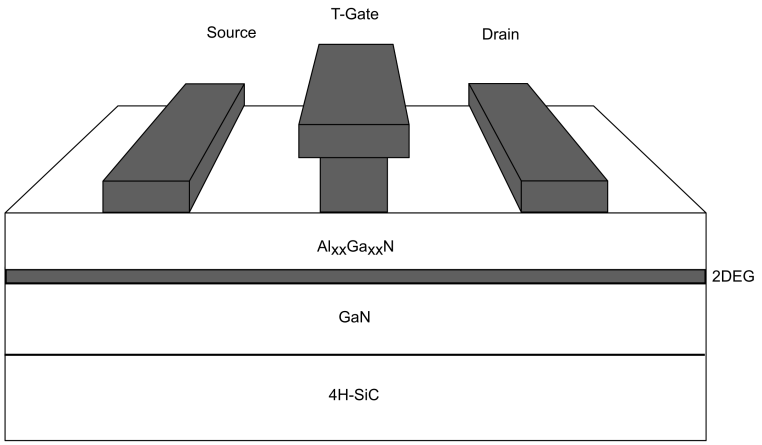


Figure 27: Cross section of a general GaN HEMT transistor

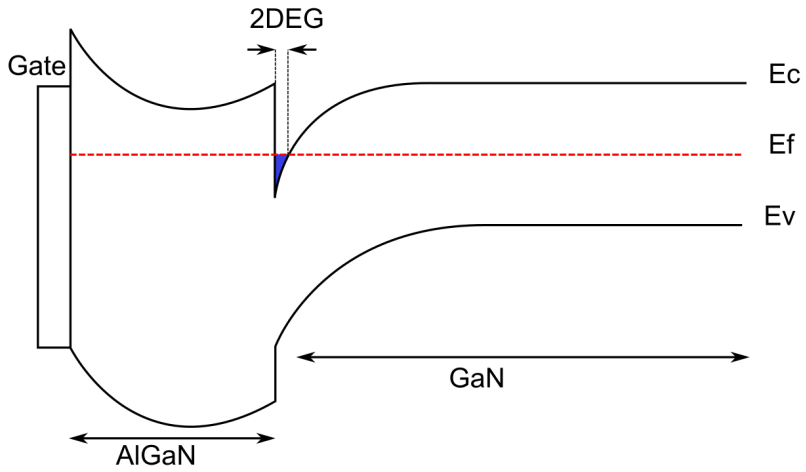


Figure 28: Energy bands of GaN HEMT amplifier

2.10 MMIC

A Monolithic Microwave Integrated Circuit (MMIC) is as the name suggests a type of integrated circuit. The word monolithic means "single stone", and any MMIC is based on a single semiconductor material. When all passive and active components, as well as the interconnect between them are based on the same semiconductor material, any transition in the circuit becomes smooth, causing little boundary effects of the transversing EM-wave. This avoids fringe-field effect and minimize unwanted wave reflection and diffractions. The word "Microwave" indicates operation in the frequency range, typically $300MHz \leq f \leq 300GHz$. As mentioned in subsection 2.2, the characteristic impedance of a transmission line (equation 2.8) is given by its material parameters, and to achieve Z_0 in the range around 50Ω for microwave frequencies, the MMIC circuits has to be small, which is generally an advantage. Typical MMIC area dimensions ranges from $1mm^2$ to $10mm^2$, though smaller and bigger chip sizes are both theoretically and practically possible [10]. For practical MMIC design, a designer needs to choose a *foundry*, which in essence is a library of components which has a number of material properties in common, and can therefore be thought of as "one technology". A foundry is inherently connected to its producer.

2.10.1 The MMIC advantage

The main advantages of using MMIC over other techniques ([10], p.6), is that it combines several important design factors. MMIC Transistors are generally high-performance, meaning they can be expected to reliably deliver high powers at high frequencies, compared to for example analog CMOS, which generally cannot reliably deliver the same high powers [10].

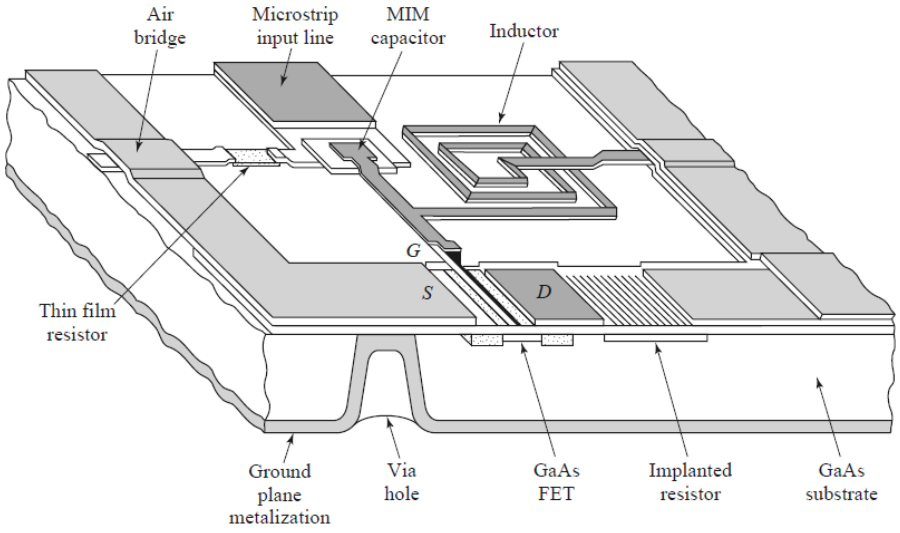


Figure 29: General MMIC layout, [1][p.550]

Another advantage is the MMIC's ability to handle mechanical impacts, making it suitable for military devices. The dimensions of MMIC are generally an order of magnitude smaller than both the *Hybrid MIC (HMIC)*, and discrete components. This allows MMIC to be used mobile electronic applications, and also decreases material cost if a large scale production is wanted. This can be a strong advantage if costly semiconducting or conducting materials are used. This also means that MMIC weigh less than HMIC or discrete, which can be an advantage in both commercial electronics as well as in space applications, where each gram of equipment may cost a multitude of dollars. Combining the above factors make MMIC an attractive technology for both commercial, military and space applications. One main drawback of MMIC is the cost of producing a wafer for a single circuit, making the "per-unit" price for small quanta large compared to other technologies.

2.10.2 Fundamental MMIC architecture

Figure 29 shows a general MMIC layout including both active and passive components. In the figure, GaAs technology is used for illustration, though the same principles apply for GaN. In the fundamental MMIc achitecture, components lie on top of a substrate, with conductive metal interconnects between them. The substrate consists of the semiconducting technology used, which allows propagation of the electric fields. Under the substrate, a conductive metal ground plane gives the circuit a reference to ground. Any component that is connected to ground in the circuit achieves this with a VIA hole connected through the substrate.

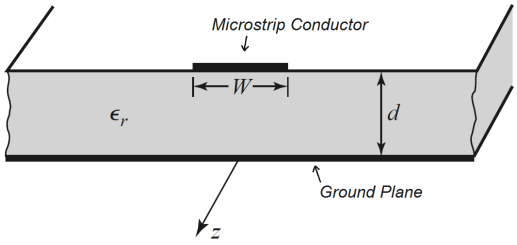


Figure 30: General Microstrip Transmission Line, [1][p.147]

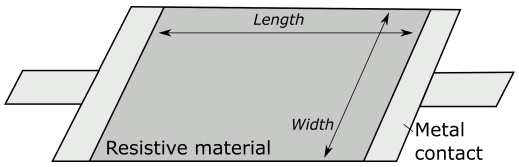


Figure 31: General MMIC resistor construction

2.10.3 MMIC Transmission Lines

Transmission lines in MMIC are usually implemented as *Microstrip* Transmission Lines, with the general layout shown in figure 30. The architecture consists of a microstrip conductor on top of a substrate, and the ground plane underneath the substrate. With reference to figure 29, the interconnects between the components are done with a microstrip transmission line. For the CREE foundry, the transmission line conductors can be implemented in two ways. Either by using just one conductor material, *Metal1*, or by reinforcing Metal1 with another conductor material, *Metal2*. For the MMIC designer, two important parameters of the conductor is its minimum width parameter and its maximum current per-unit-width parameter. These are not given here due to the confidential nature of the CREE foundry, but can be found in [11].

2.10.4 MMIC Resistors

In general, there are two ways of realizing MMIC resistors, which is either done by using the active semiconductor layer under the MMIC surface, or by laying a thin film of resistive metal on top of the surface. For both methods, the resistivity of the component is defined by the length-to-width relation, denoted, $R_{\square}$. Thus the general formula for a MMIC resistor is given in equation 2.57, with $R_{\square}$ varying between technologies. Theoretically from equation 2.57, a $20x20$um resistor has the same ohmic resistance as a $200x200$um resistor, though any size changes would yield a phase change, making the impedance of the resistor complex. Also, most technologies has a minimum width, W_{min} value, giving restrictions to how physical small the resistor can be.

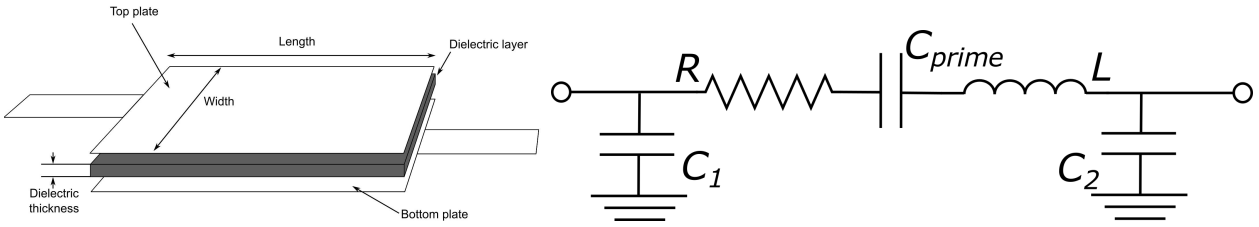
The CREE MMIC Foundry offers three different resistor type, with different resistivity. These

are *Thin Film Resistor*, *Bulk GaN Resistor 1 (BGR1)* and *Bulk GaN Resistor 2 (BGR2)* respectively. [11] gives the minimum, typical and maximum value of $R_\square$ for the three and their W_{min} values. From [11] it's readily seen that BGR2 has the larger square resistivity, but also a larger uncertainty range, making it useful for large resistors where precision is not important. For smaller resistors where precision is more important, the thin film should be used.

$$R_{eq} = \frac{L}{W} \cdot R_\square \tag{2.57}$$

2.10.5 MMIC Capacitors

As with resistors, there are generally two methods of realizing MMIC capacitors, which are *Interdigital Metal Strips* capacitor and *metal-insulator-metal (MIM)* capacitor. The interdigital capacitor uses in essence a number of fingers, spaced a certain *Finger Spacing* distance apart from each other, which in turn gives the capacitance of the component, depending of number of fingers and finger spacing. As the interdigital capacitor is not part of the Cree foundry, it's not explored in further detail here. The MIM capacitor construction is given in figure 32a, with the corresponding equivalent circuit in figure 32b.



(a) MIM construction, [10][p.45] (b) MIM equivalent, [10][p.77]

Figure 32: Construction and equivalent of the MIM MMIC Capacitor

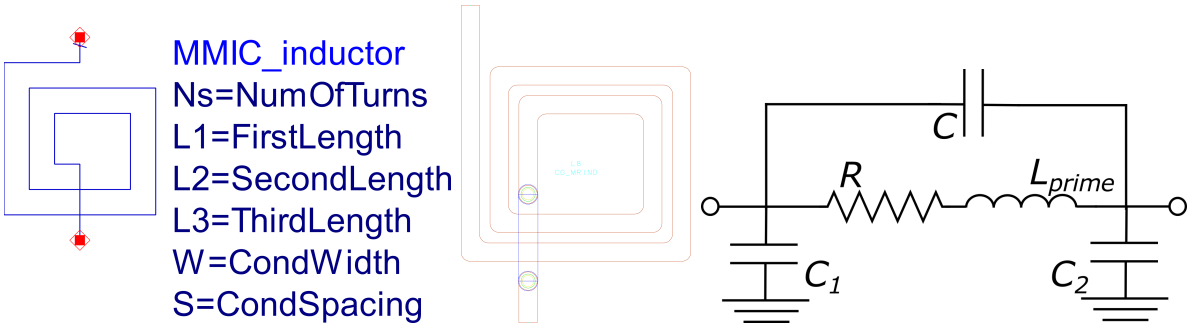
In figure 32b, C_{prime} is the primary capacitance and should be much larger than the parasites C_1 and C_2. R and L gives the resistive loss and inductive parasite of the MIM. Examining figure 32a, the EM-wave has two main paths of propagation, which is either through the dielectric, or between the plate edges outside the dielectric. This in turn means that a MIM capacitor has two main sources of capacitance, which is the parallel plate capacitance C_A, and edge parasitic capacitance, C_p. C_A is dependent of plate area and has unit $[F/\mu m^2]$, while C_p has unit $[F/\mu m]$. A general formula for MMIC MIM capacitor is given as

$$C_{eq} = L * W * C_A + 2(L + W)C_p \tag{2.58}$$

For many practical applications, C_p can be assumed close to zero, reducing equation 2.57 to $C_{eq} = L * W * C_A$. In the Cree foundry, no value of C_p is given, and the value of C_A is given in [11].

2.10.6 MMIC Inductors

Generally, a components ability to store current gives its inductance, and as described above, this may also occur as unwanted parasites in any conducting material. For a transmission line, the narrower the conductor width in relation to substrate height, the better its inductance. But for a high power PA, this means that the current density becomes high, and may in extreme cases overheat the MMIC, burning up the substrate. It is therefore generally hard designing inductors in MMIC, and they generally use more space than resistors and capacitors. For increased powers and currents, the resulting size of the inductor increases proportionally, making it a challenge for a PA designer. A common design method to realize MMIC inductors, and also the inductor found in the Cree foundry is the *Spiral Track* inductor, which basically is transmission lines spiraling inwards, with a bridge from the innermost conductor to the output. Figure 33a shows a schematics of the Cree inductor with some basic parameters, figure 33b shows the equivalent inductor layout and figure 33c gives the lumped component equivalent.



(a) Schematics (b) Layout (c) Equivalent, [10][p.80]

Figure 33: Illustration of inductors in MMIC

NumOfTurns in figure 33a gives the number of straight segments in the inductor, illustrated here with Ns = 9. As the name implies, $L1$, $L2$ and $L3$ are the first, second and third segment of the inductor, illustrated here with $L1 > L2 > L3$. W gives the conductor width and S the spacing between the conductors, illustrated here with $W > S$. Perhaps the most important conclusion of the above is that MMIC inductors contains a much larger number of variables compared to capacitors and resistors, and no single equation of width and length yield the inductance. Designing inductors also requires a trade-off between increasing inductivity, satisfying $[mA/\mu m]$ demands while keeping the area low. Therefore, as a designer rule of thumb, the use of inductors should be kept to a minimum, and if capacitor can replace an inductor, a designer should do so.

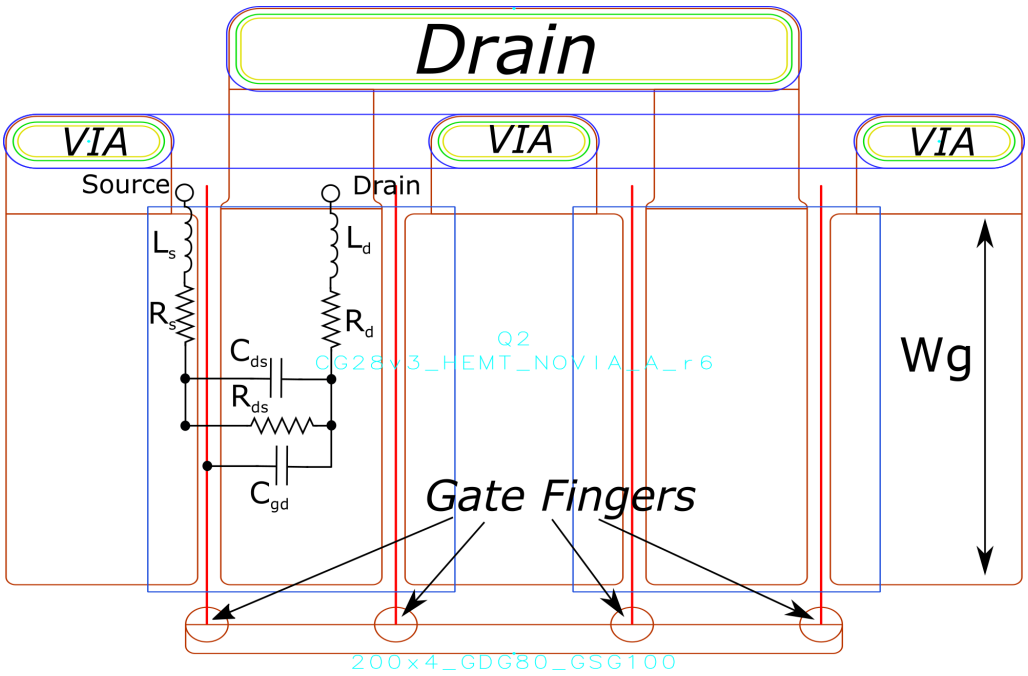


Figure 34: General HEMT layout with parasites illustration

2.10.7 MMIC HEMT Transistor

The general behaviour of a HEMT transistor is described in subsection 2.9.3. In the CREE foundry, a number of HEMT transistors exists for the designer to choose from. The details of the CREE foundry transistors are not explained in detail here, but in subsection 2.3.2 the choice of transistor for this project is given with an explanation of some HEMT parameters. In essence the HEMT MMIC has two main parameters to define its size, and corresponding $I_{D,max}$. These are the number of gate fingers, Ngf, and Wg, the length of each gate finger. These are illustrated in figure 34 with Ngf = 4. Figure 34 also gives an illustration of the parasites given schematically in figure 4. The Gate parasites are omitted for readability.

2.10.8 The Olavsbråten Parasite model

As shown in figure 4 and 34, a general HEMT MMIC transistor have a variety of parasitic effects occurring when applying voltages and currents to the transistor. These can be modeled with lumped components and a general parasitic model for a FET transistor is shown in figure 4. When designing both input and output networks of an amplifier, as described in subsection 2.4, the parasites can be useful as circuit elements if they correctly portray the equivalent effect of an lumped component. To find the equivalent lumped component values of the parasites, a model was created by Morten Olavsbråten which gives the values of the components. This is shown in figure 35, with the circuit symbol given in figure 36.

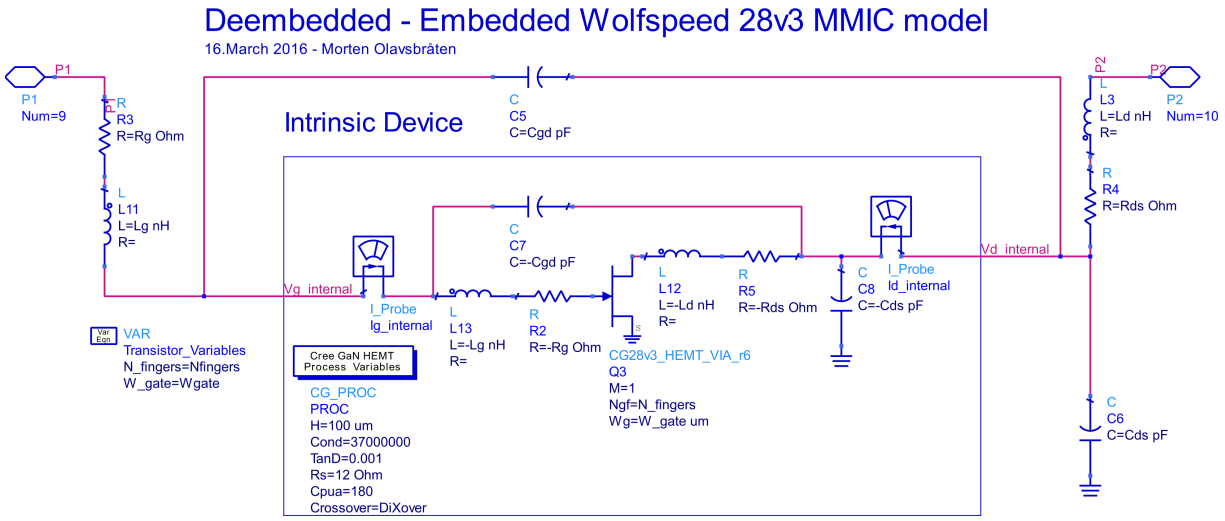


Figure 35: The Olavsbråten Parasite Model circuit

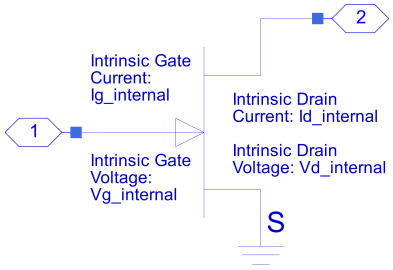


Figure 36: The Olavsbråten Parasite Model symbol

The idea behind the model is that the parasites are dependent on transistor geometry, and for the most part, independent of frequency. As an MMIC HEMT transistors geometry are mainly dependent on the number of fingers, $N_{fingers}$, and the width of each finger, W_g, equations could be developed for $L_g, R_g, C_{gd}, C_{ds}, R_d$ and L_d, all dependent only on geometry. These equations are not written here due to their confidential nature, but can be found in [11]. The method in finding these values exploits the CADs possibility to use negative component values. Adding a negative resistor or inductor in series, or a negative capacitor in shunt effectively eliminates the the parasites of figure 4. Thus by consecutively adding negative components, a designer should be left with only the ideal voltage controlled current source in figure 4. The Olavsbråten model of figure 35 omits some parasites for simplicity, and can not be seen as a complete model. Specifically, the CG28v3_HEMT_VIA_r6 transistor model creates a VIA-hole directly to ground, not allowing any manipulation of the Source node.

2.11 Wolfspeed

Wolfspeed is an american company, and the creator of the MMIC technology used in this project. It is sub-division of Cree, Inc. and went under their name in the past. They were

later established with their own name, Wolfspeed. They focus on wide bandgap GaN and SiC products for power amplifiers and RF.

2.12 Wilkinson Splitter

The input signal must be divided between the two amplifiers in such a way the class-C amplifier starts conducting at the right time, and that both amplifiers deliver the same amount of power at $P_{in,max}$. Ideally the impedance the amplifiers see towards the source should not be affected by the other amplifier as this would change the impedance when the auxiliary amplifier begins conducting, which would affect the match between source and amplifiers input. The Wilkinson power divider is a power splitter where all ports are matched, and the two output ports are isolated, which makes it a good choice for this design. As will be made clear in section 3 the splitter used in this project was ideal, and therefore the splitter is not pursued any further here.

3 Practical

3.1 Overview

The basis for the amplifier design was the ideal Doherty amplifier design which was made the fall of 2015.[12] The design was made completely with ideal components, exception being the transistor itself, for 100MHz to decrease the impact from parasitics. The only requirements was a doherty-like efficiency curve, and an output power of at least 10 Watts on the fundamental frequency. The amplifier designed in this project has a center frequency of 2.4 GHz, and a bandwidth of 800 MHz, ranging from 2.0 GHz to 2.8 GHz. All components are non-ideal MMIC models, exceptions being the load and the splitter on the input, and is able to handle the currents and voltages present in the circuit.

When first designing the amplifier ideal components were used, and were only replaced with the MMIC models towards the end when all component values were set. First a designbench supplied in Keysight ADS was used for small signal and S-parameter analysis. Ideal DC-blocks and DC-feeds were used to ensure restriction of DC and AC signals. Unconditional stability was ensured for every frequency by use of the μ-factors and the stability circles produced by ADS. Then a rudimentary match for gain was made for the input.

Morten Olavsbråten supplied an expanded model of the transistor. This gave a much better representation of the loadline observed by the ideal, internal current source, see figure 4. The optimal load line for output power for the AB-amplifier had been derived from the DC-characteristics simulations in the foregoing project [12]. An output network was then created to ensure the optimal load line was achieved at peak output power, and that second harmonics saw a low output impedance to ensure class-B operation. The internal parasitics of both transistors were included as part of the network. After the output network was in place, and the large signal analysis gave satisfying results the ideal components were switched out with MMIC-models, ensuring that all of them could handle the currents and voltages present. Finally the envelope tracking was implemented mathematically. It is important to note that the connections between the components in the final design are ideal, as is the splitter on the input and the load. The latter is due to the fact that the actual load will not be an MMIC component, but most likely an antenna. While the former two were not realized with MMIC models as the focus of this project is the conceptual realization of the amplifier, not the physical one.

3.2 Design software

All circuit design and simulation was done in Keysight (formerly Agilent) advanced design system, which is a powerful design tool for RF, microwave and high speed applications. Small signal, large signal and transient analysis can be performed. The software has a powerful optimization tool which allows the designer to define parameters the software is allowed to change, and goals for the optimization. The software will then perform an iterative optimization procedure, changing the predefined parameters in an attempt to best fulfil the goals. Once an improvement is achieved, it keeps the current parameter values and uses that as basis for the next iteration.
This optimization tool was used during the design of the output network described in section 3.6

3.3 Transistor

There are several different transistors to choose from from Wolfspeed. For this project the G28V3 with integrated vias was chosen for its power handling and compact layout. With a maximum drain voltage of 28 V it can easily be used to generate the desired output power levels, while keeping the transistor relatively small. The expanded version of the transistor model supplied by Morten Olavsbråten allowed for the parasitics to be included as part of the network designs, allowing much greater control of what the internal current source of the transistor sees. The parallel parasitic from Drain to Gate of the transistor, shown in figure 35, was remodeled to two capacitors on either side, according to Miller's theorem, for proper implementation into the output network. The final model used for simulations can be seen in figure 37 with capacitors C7 and C8 being the miller equivalents to capacitor C5.

The specifics of the model and the values of the parasitics can be seen in appendix [11].

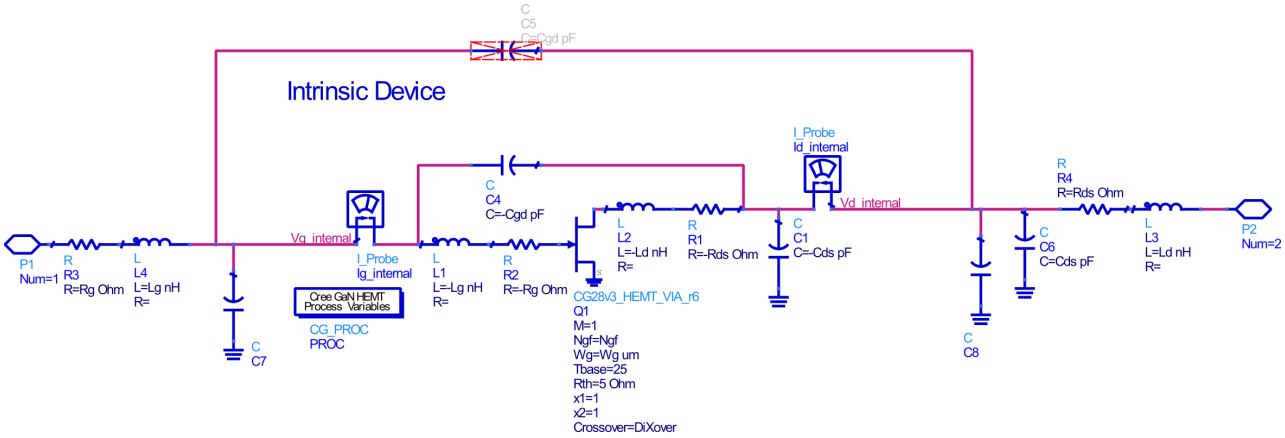


Figure 37: Transistor model with parasitics from general high frequenc transistor model.

3.4 Amplifiers

3.4.1 Main amplifier

For main amplifier a deep class-AB was chosen, rather than a class-B. When looking at the DC-characteristics of the transistor some drain current lines can be seen to appear and rise above 0 a little way above the $V_{ds} = 28V$ bias point. To ensure predictable behaviour the transistor was instead biased in deep-AB at $-3V$ so that the input drive level is too large to produce any currents on the negative swing. The transistor was dimensioned to handle a little over 5 Watts to ensure a little headroom. The transistor for the Main amplifier has 4 gate fingers and a gate width of $350\mu m$ [12]

3.4.2 Auxiliary amplifier

As mentioned in 2.6.5, a class-C amplifier was chosen for the Auxiliary amplifier to simplify the turn on/turn off operation at different drive levels. The bias level of the Aux amplifier was originally set to -5.6V, and as explained in section 3.9 later adjusted to -4V. The transistor was dimensioned to have a gate length 2.5 times larger than the Main amplifier transistor in accordance with the theory of Cripps. [4]. The transistor for the Aux amplifier has 6 gate fingers, and a gate width of $550\mu m$.[12]

3.5 Input network

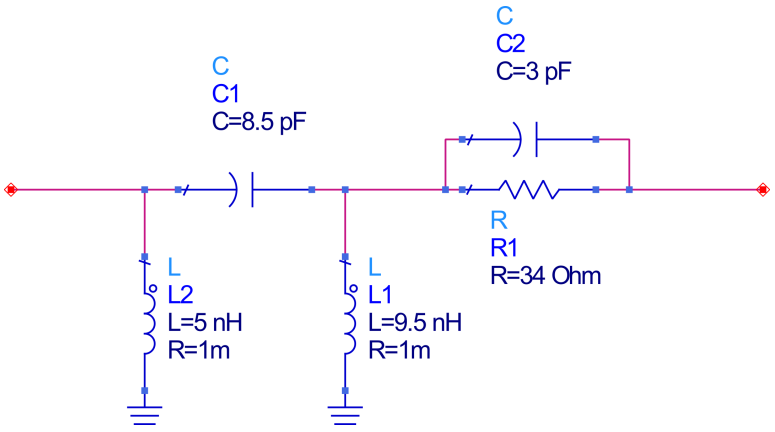
The input network was not a priority in the design of this amplifier, as the main point of interest was what was happening at the output of the amplifier. The input network was designed for maximum small signal gain. The bandwidth of the nework was made larger than the intended bandwidth of the amplifier to avoid it becoming a limiting factor at any point during the design process. Once stability had been ensured the designbench from ADS was used to find the simultaneous match for maximum gain, and that impedance was used to match the input of the amplifier. The input matching network was not changed after this, except when changing the ideal components for MMIC-models. Some adjustment had to be made to ensure all the components could handle the current of the circuit. Small signal analysis were made after the adjustments and the results were at the time deemed acceptable. The input network was made before the expanded transistor model was supplied from Morten Olavsbråten, and the output network was finalized. It was not revisited to include the transistormodel, or to compensate for the changes made to the output network, see section 5.1

3.5.1 Main amplifier

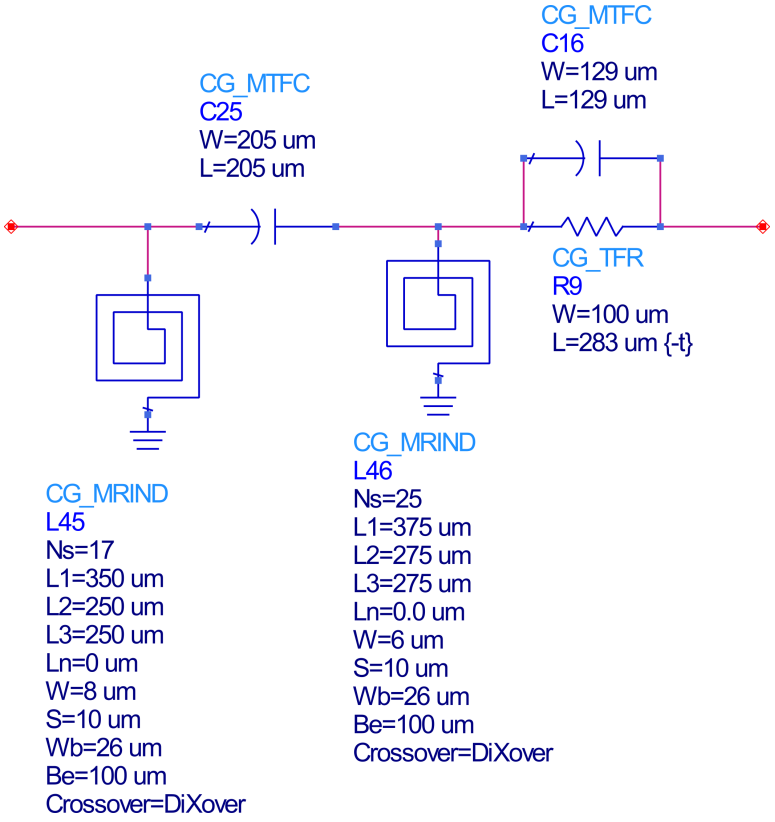
The design of the input network began with stabilization of the amplifier for small-signal analysis. Originally the stabilization network consisted of components C2 and R1 seen in figure 38a, and a feedback network from the transistor drain to gate. The feedback network was later removed as it was no longer needed to ensure stability, once the input network had been expanded to include matching networks.

3.5.2 Aux amplifier

As the Aux amplifier is a class-C amplifier proper small signal analysis cannot be performed, as the amplifier is in cut-off for very small signals. For stabilization and matching the amplifier was therefore biased like the Main amplifier, and similar network topology was used. Originally the stabilization network for the Aux amplifier included a feedback network from drain to gate, as the Main amplifier had. But this too was removed as it was no longer needed to ensure stability, once the network had been expanded. In figure 39a R24 and R25 were placed in parallel as the currents through the resistor were too large according to the maximum ratings stated in appendix [11]. While there is no guarantee that the stabilization and matching networks has the exact same performance once the amplifier is biased below cut-off, and is only driven to conduction by large signals, it is considered satisfactory for this project.

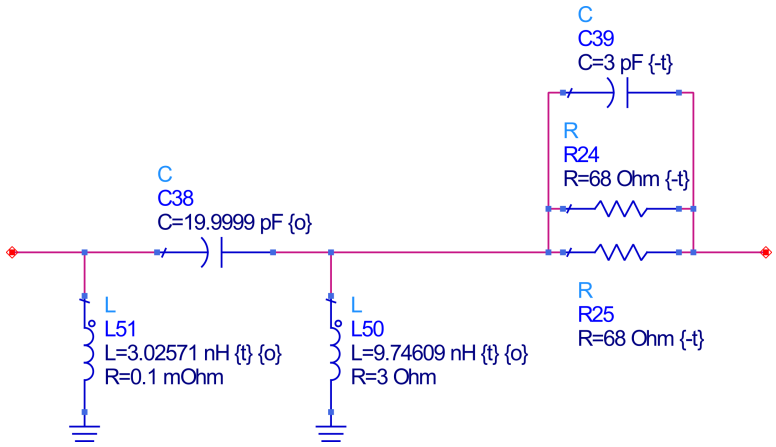


(a) Ideal components

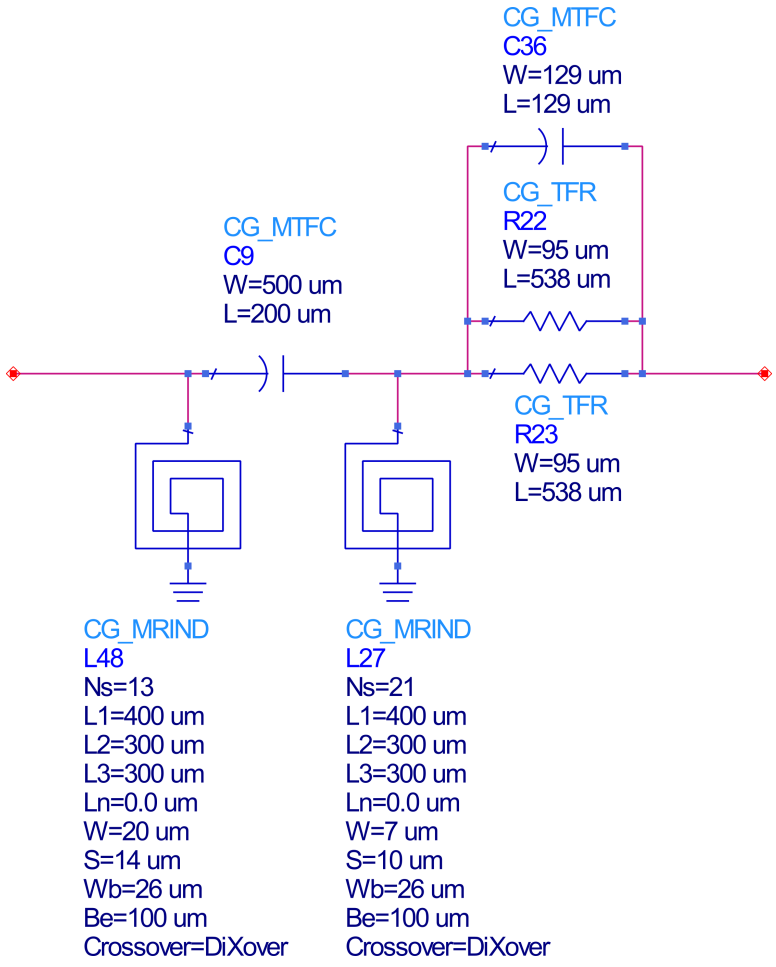


(b) MMIC components

Figure 38: Main amplifier input netowrk.



(a) Ideal components



(b) MMIC components

Figure 39: Aux amplifier input netowrk.

3.6 Output network

For the output network a "black box" approach was used. An ideal version of the network in figure 16 was set up for small signal analysis in ADS as reference, with a 25Ω load. The idea was to create a new network that would have the exact same behaviour as the ideal circuit at the fundamental frequency.

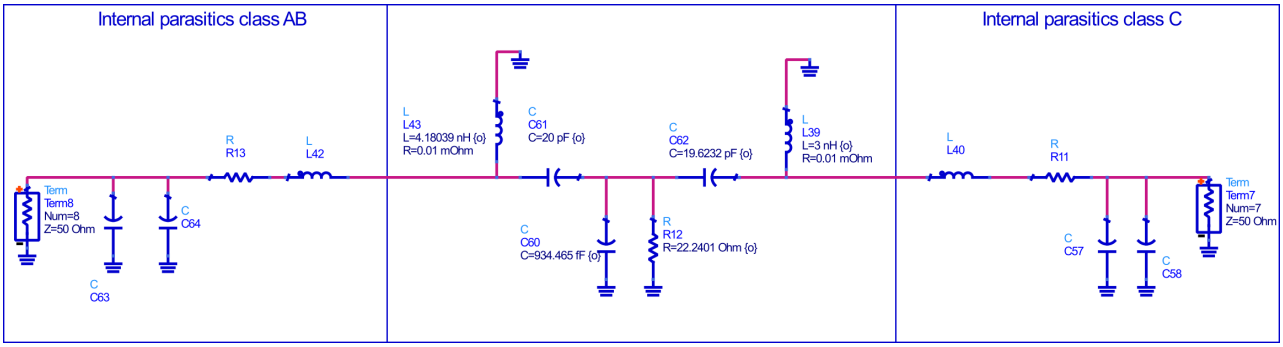


Figure 40: Output network with ideal components

The resulting network would have to have the internal parasitics of the transistors present as constant components, that the optimizer of ADS was not allowed to change. Then components were added as needed to give the optimizer freedom to alter the observed impedances. In addition to the transistor parastics, the DC-feed inductors, and the DC-blocking capacitors were also a requirement. The optimizer was then allowed to adjust the component values, whithin certain limits determined by the maximum ratings of the components, to achieve the desired impedances. The goals compared the Z-parameteres of the ideal network and the output network, and tried to minimize the difference between them, as well as ensure a low impedance for second harmonics.

The goals were set as

$$|Z_{11,output} - Z_{11,ideal}| = 0 \tag{3.1a}$$

$$|Z_{22,output} - Z_{22,ideal}| = 0 \tag{3.1b}$$

$$|Z_{11,output}|_{2ndharmonic} \leq 5 \tag{3.1c}$$

$$|Z_{22,output}|_{2ndharmonic} \leq 5 \tag{3.1d}$$

Where $Z_{11,output}$ and $Z_{22,output}$ are the impedances seen by the internal current sources of the Main and Aux amplifier respectively. $Z_{11,ideal}$ and $Z_{22,ideal}$ represents the same for the ideal circuit.

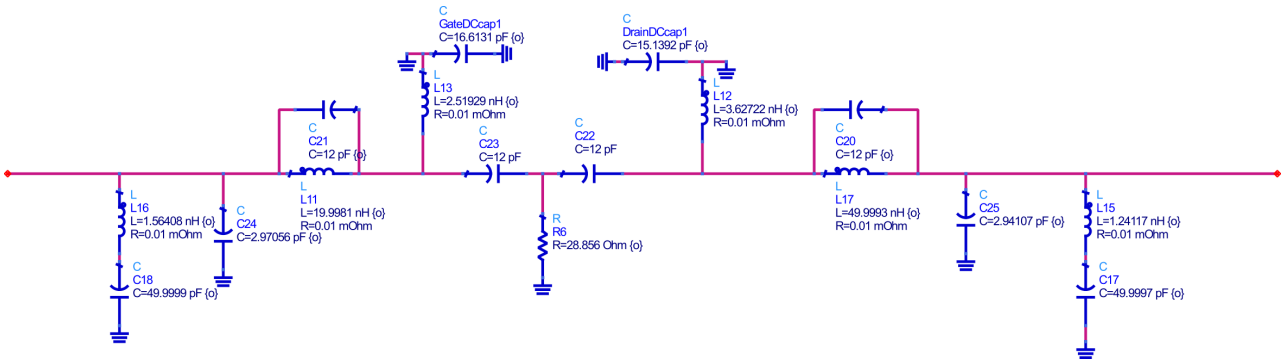


Figure 41: The first iteration of the output network

The first iteration of the output network is shown in figure 41. Now the component values were evaluated. If the optimizer does not want a component in the circuit it tends to either reduce the component value (for series inductors, resistors, and shunt capacitors) or increase them (series capacitors, shunt inductors and resistors) as far as it can. Based on this several components were removed from the design, with very little impact on the actual result.

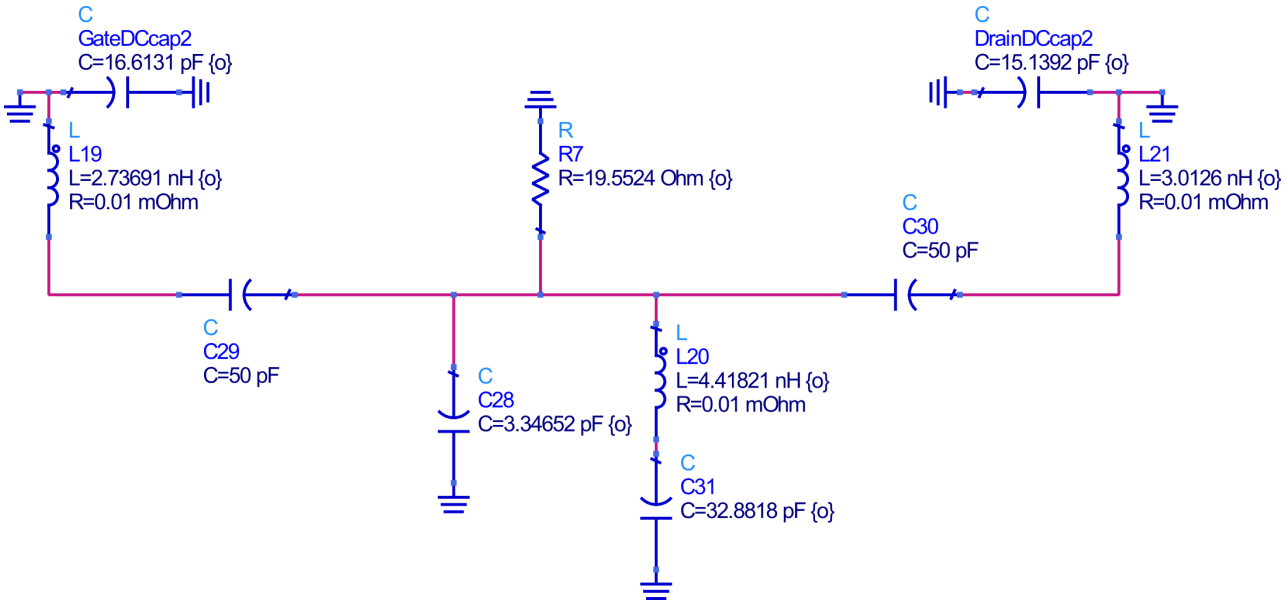
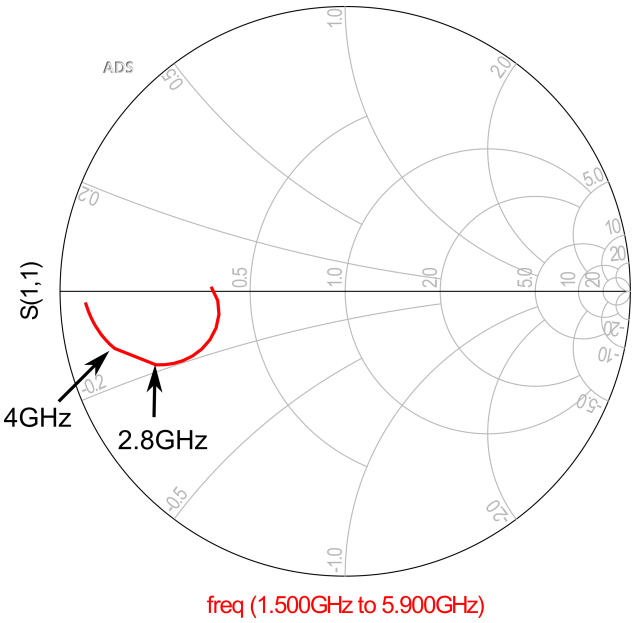
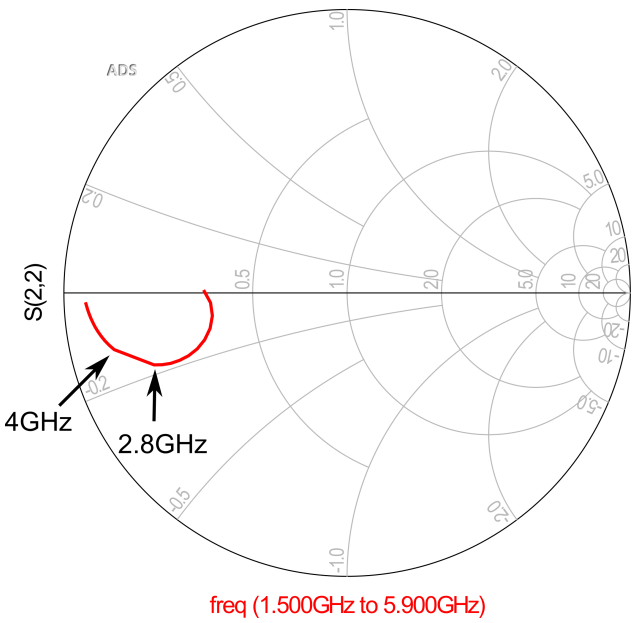


Figure 42: The second iteration of the output network

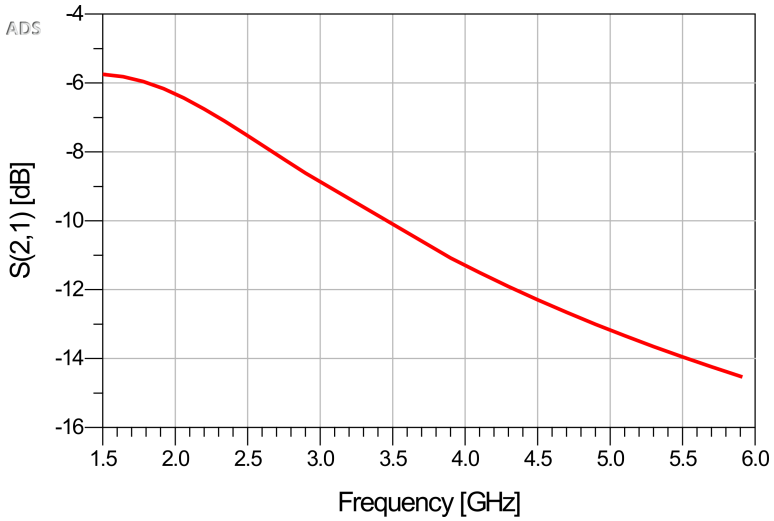
After more simulation, the end result is shown in the mid-section of figure 40



(a) Output network seen from main amplifier



(b) Output network seen from aux amplifier



(c) Transmission Coefficient from main to aux

Figure 43: Output network simulation results

Once large signal analysis showed expected results the currents and voltages in the circuit were noted, and the ideal components were switched out with MMIC models.

3.7 Real component models

Once the large signal analysis were satisfactory the ideal components could be switched out with their MMIC model counterpart. First the currents through the resistors and the inductors, and the voltage of any shunt capacitor were noted. The voltage over the capacitors were checked

against the maximum ratings of Wolfspeeds foundry manual, see appendix [11] to make sure they weren't exceeded. For resistors and inductors, the width of the lines were set first to make sure the component could handle the current. The dimensions of the capacitors and resistors were found with equations2.58 and 2.57 for the desired component value. The MMIC component was then simulated and special care was taken to ensure the resonance frequency of the component was above the second harmonic of the highest frequency in the band, i.e. 5.6 GHz. If this was not the case the component dimensions was adjusted to increase the resonance frequency while maintaining the same component value. The most challenging component in the design process was the inductor, as it was more trial and error. After the width of the wire was set to handle the current, the inductors many parameters was adjusted to achieve the best possible result. If the inductance dropped too low, the fundamental and harmonic currents through the inductor would increase to a point where the wire width was too small. If the inductance was increased too much, the resonance of the inductor would enter the second harmonic band.

Figure 44 shows the circuit for measuring a capacitor in ADS. A small signal analysis is done with the option of deriving the Z-parameters checked. By plotting the real and imaginary part of Z_{11} the resistance and reactance can be found as shown in figures 45a and 45b. By using the imaginary part of Z_{11} the capacitance of the capacitor can be expressed as a function of frequency

$$C_{cap} = \frac{1}{imag(Z_{11}) \cdot 2 \cdot \pi \cdot f} \tag{3.2}$$

The equation is plotted in figure 45c, and here the resonance of the capacitor is very easily observed. Just before marker 18 in figure 45c the capacitance of the capacitor seems to be rising very quickly, and then turn negative. This can be explained by looking at figure 45b where, for the same frequency, the reactance can be seen crossing the zero line. As the reactance goes from negative to positive, the capacitor begins behaving more and more like an inductor instead of a capacitor.

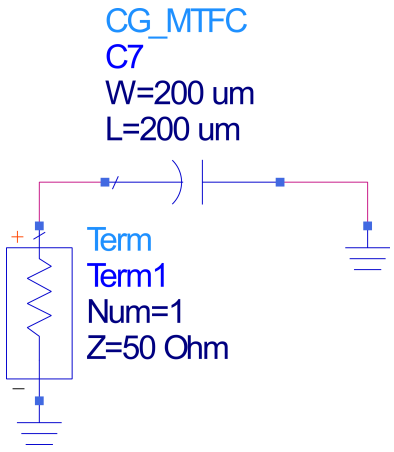
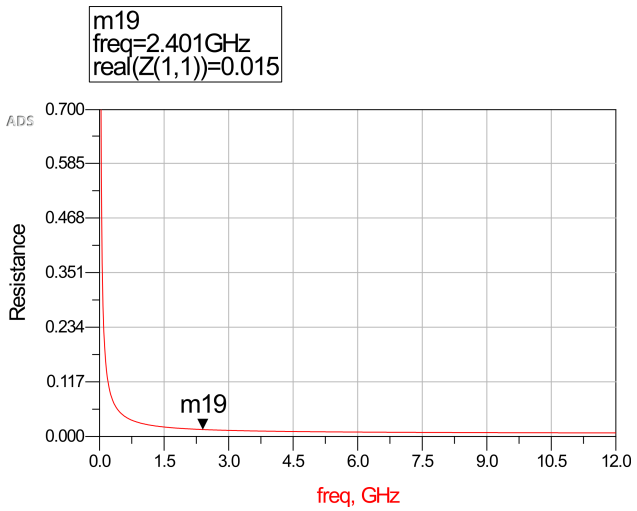
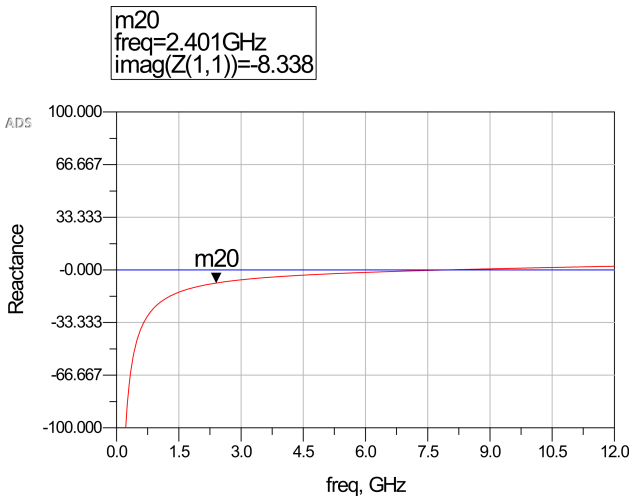


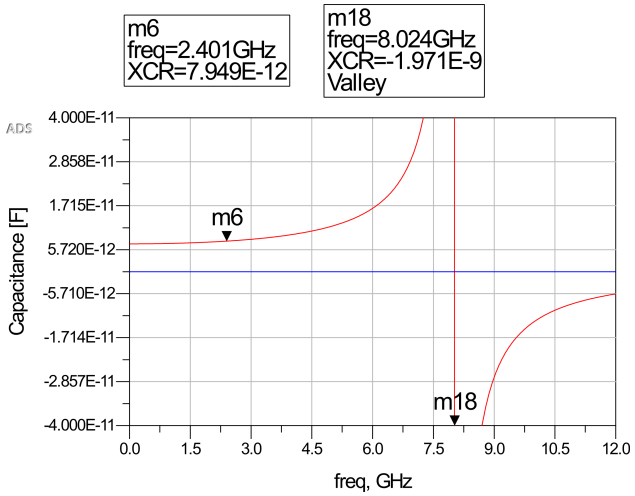
Figure 44: Measurement of MMIC capacitor.



(a) Resistance of MMIC capacitor



(b) Reactance of MMIC capacitor



(c) Capacitance of MMIC capacitor

Figure 45: MMIC capacitor measurements.

A similar equation to 3.2 is used for the inductor.

$$L_{ind} = \frac{imag(Z_{11}}{2 \cdot \pi \cdot f} \tag{3.3}$$

And it has a similar behaviour as shown in figures 45.

3.8 Envelope tracking

The last thing to be implemented was the envelope tracking. Three envelope tracking schemes were explored. The input signal was manually stepped through all its values, and for each input value the drain voltage was adjusted to maximize the power added efficiency of the system. The values were plotted in excel and a trendline, represented by a 6th order polynomial, was

derived. This polynomial was then adapted to ADS' syntax, and added as an if-statement in the variable controlling the main amplifiers drain voltage.The if-statement was used to ensure the drain voltage never rise above 28 V, even if the input signal was increased. A slightly different approach was also attempted, where the drain voltage values were chosen so the load line of the amplifier were very close to saturation at all times, except for the lowest input signal values. Finally a linear tracking scheme was devised, which simply generates the supply voltage as a linear function of input voltage. The three mathematical equations used is shown in equations 3.4, 3.5 and 3.6

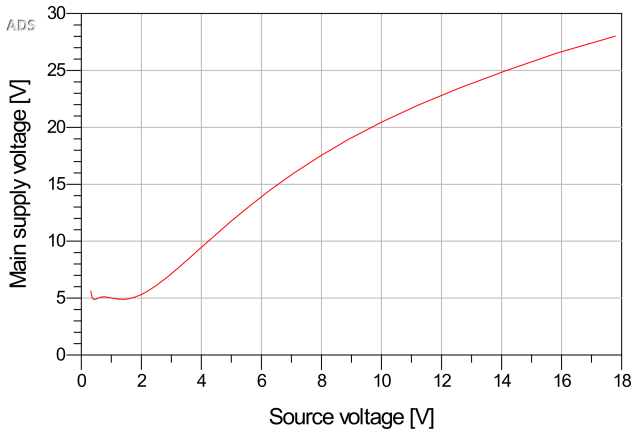
Equations3.4, 3.5 and 3.6 are the polynomial used for tracking based on PAE, saturation and linear tracking respectively.

$$\begin{aligned} &0.000000307209 \cdot PRF^6 - 0.000034607672 \cdot PRF^5 + 0.001422319618 * PRF^4 - \\ &0.025235755164 \cdot PRF^3 + 0.200678329638 \cdot PRF^2 - 0.648411727234 \cdot PRF + \\ &5.593005810020 \end{aligned} \tag{3.4}$$

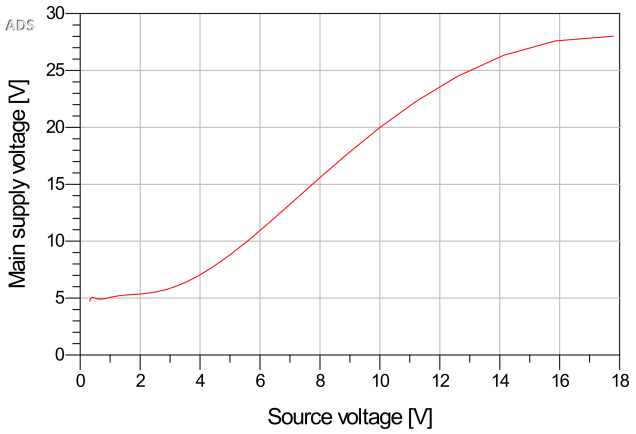
$$\begin{aligned} &- 0.000000535188 \cdot PRF^6 + 0.000047230092 \cdot PRF^5 - 0.001487736768 \cdot PRF^4 + \\ &0.021426272448 \cdot PRF^3 - 0.140826294490 \cdot PRF^2 + 0.366732488212 \cdot PRF + \\ &4.738271787413 \end{aligned} \tag{3.5}$$

$$1.293385048 * (sqrt(dbmtow(PRF) * 100)) + 5 \tag{3.6}$$

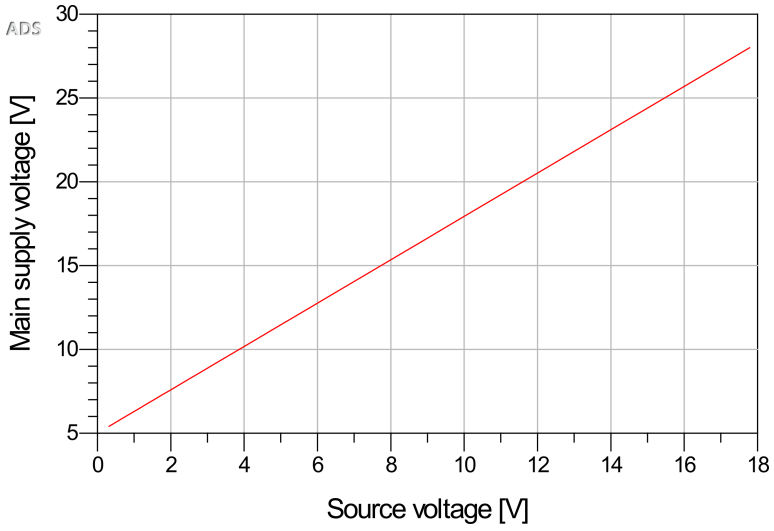
Where PRF is input power in dBm, and $\sqrt{dbmtow(PRF) \cdot 100}$ is the input drive voltage level. it is important to have a high number of digits for the polynomials especially for the higher order terms to minimize deviation from the desired voltages.



(a) Tracking based on PAE



(b) Tracking based on load line clipping



(c) Linear tracking

Figure 46: Tracking curves

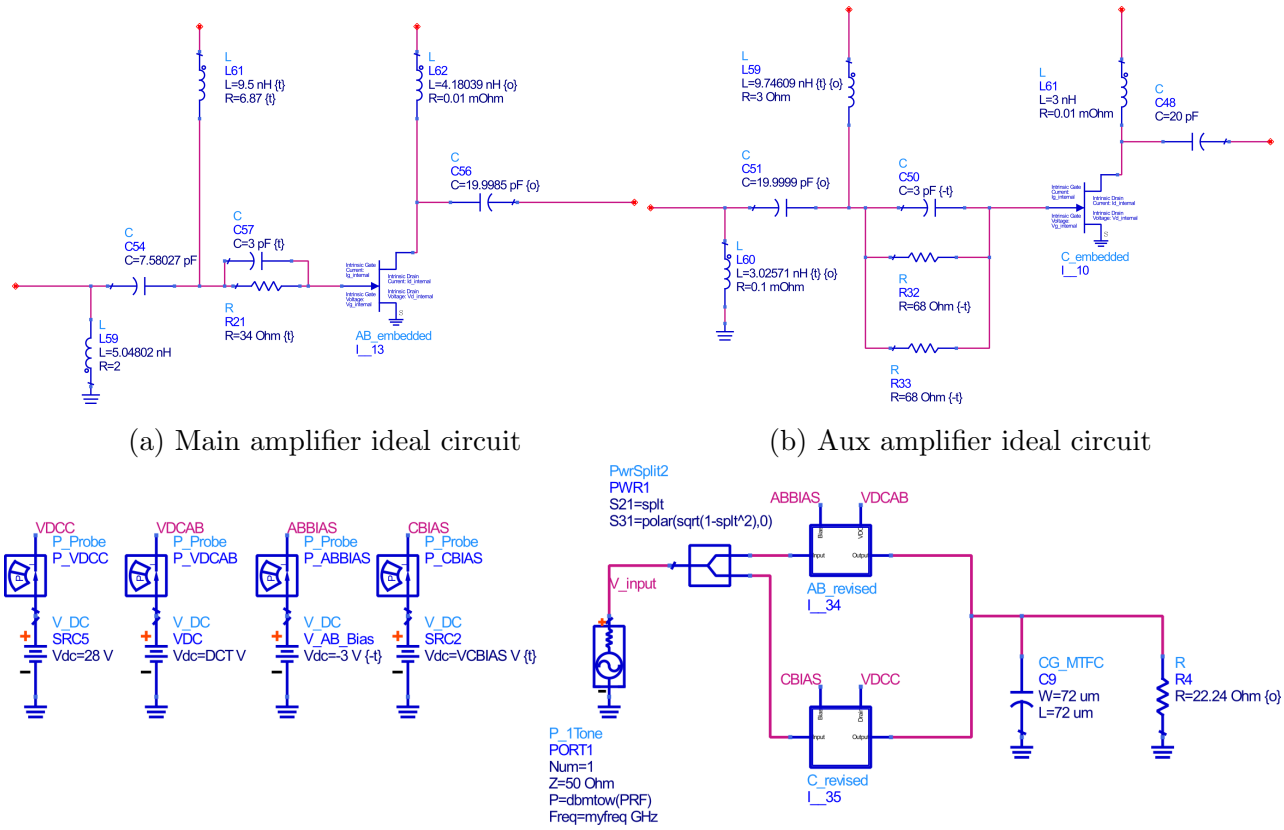
Figures 46 shows the drain voltages as functions of input voltage for the different tracking schemes. Beyond this mathematical approach to envelope tracking, there was no attempt at realizing an actual envelope tracker as that would be a project in and of itself.

3.9 Complete amplifier

Cripps [4] describes an amplifier where the Aux amplifier turns on at -6dB input drive level. In this no strict requirements were set. Once the amplifier topology was in place, the Aux amplifier bias point and the ratio of the splitter was adjusted to optimize the results. The bias voltage for the Aux amp was finally set to $-4V$ and the splitter was set to a power split so that 77.44% of the power goes to the Main amplifier, and the remaining 22.56% is delivered to the aux amplifier, with $S_{21} = 0.88$ and $S_{31} = \sqrt{1 - S_{21}^2} = 0.475$.

The finished amplifier design is shown in figure 47, and the Main and Aux amplifiers with MMIC models are shown in 48.

Areal?

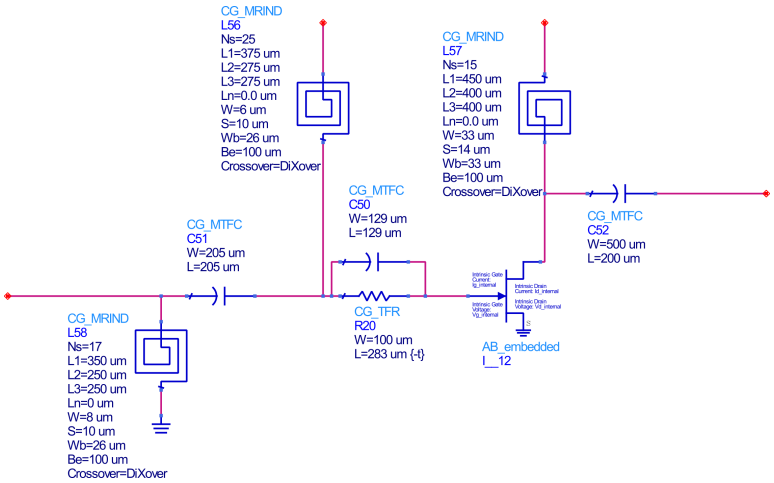


(a) Main amplifier ideal circuit

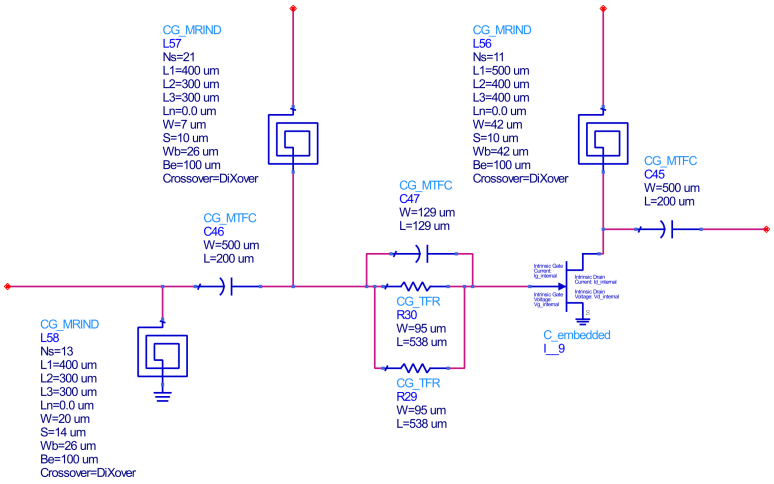
(b) Aux amplifier ideal circuit

(c) Whole amplifier

Figure 47: Amplifier circuits



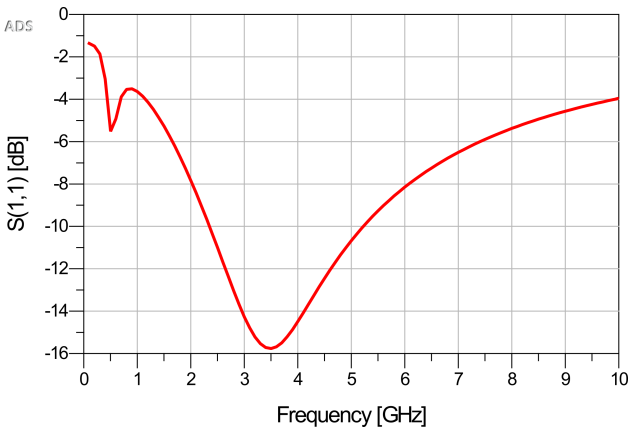
(a) Main amplifier circuit



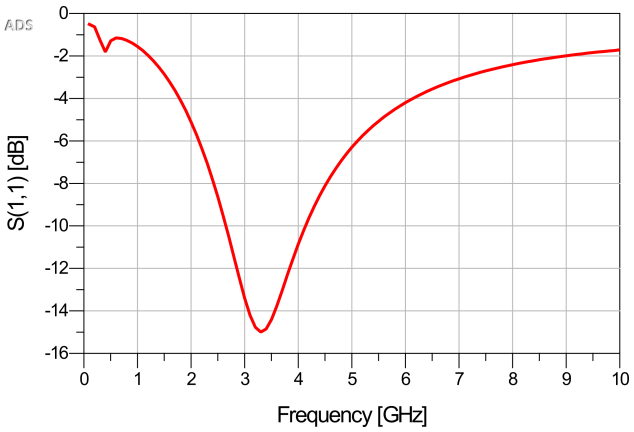
(b) Aux amplifier circuit

Figure 48: Amplifier circuits

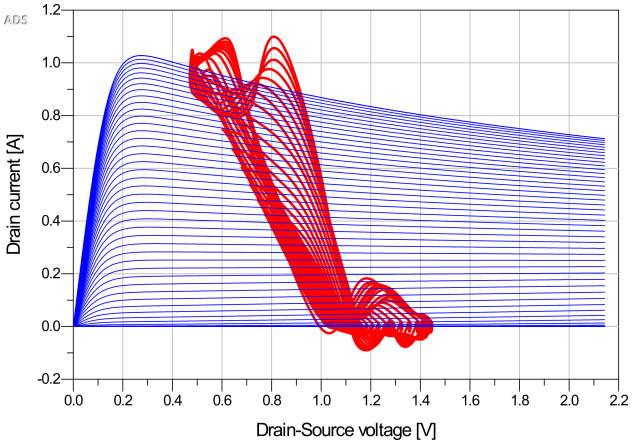
4 Results



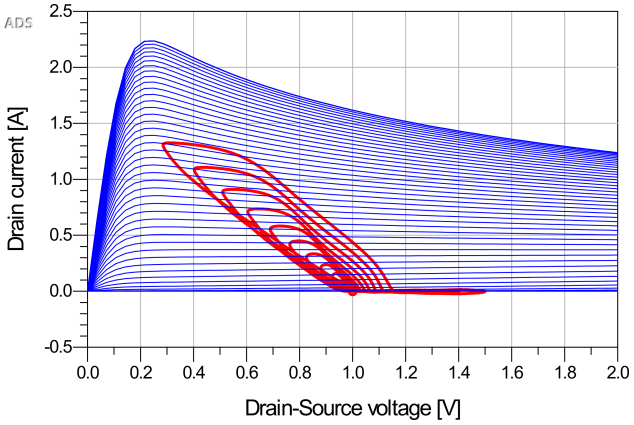
(a) Main amplifier input network S_{11}.



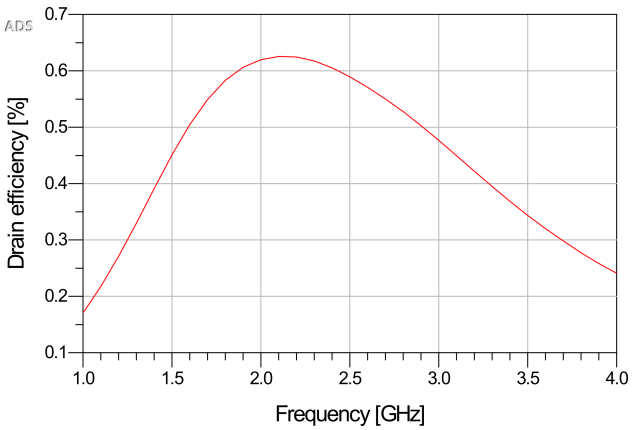
(b) Aux amplifier input network S_{11}.



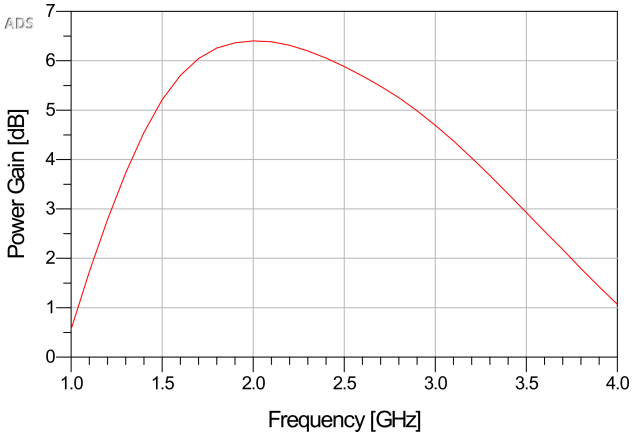
(c) Main amplifier load line.



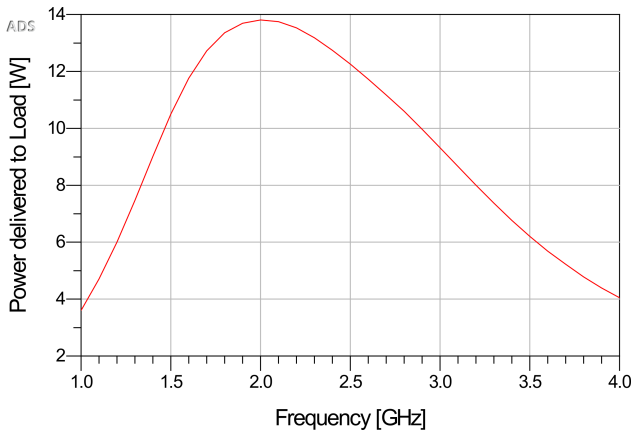
(d) Aux amplifier load line.



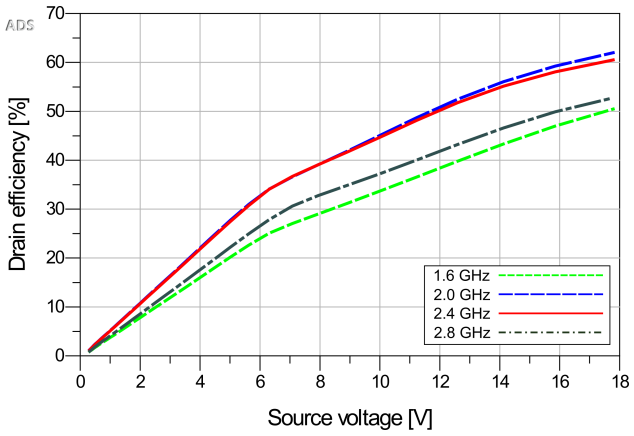
(e) Drain efficiency at maximum input drive level.



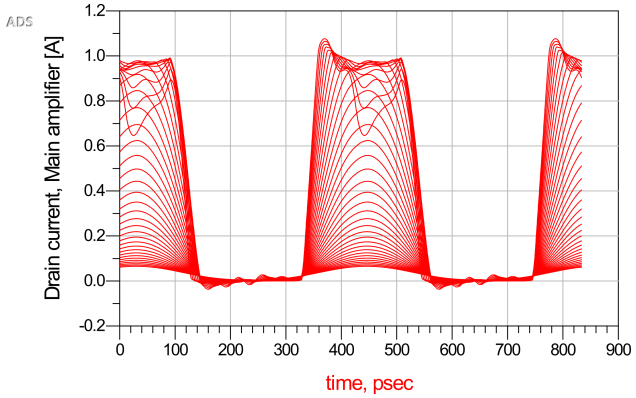
(f) Power gain at maximum input drive level.



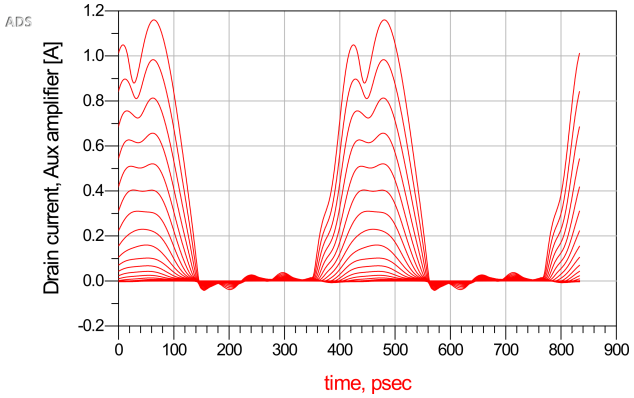
(g) Power at load at maximum input drive level.



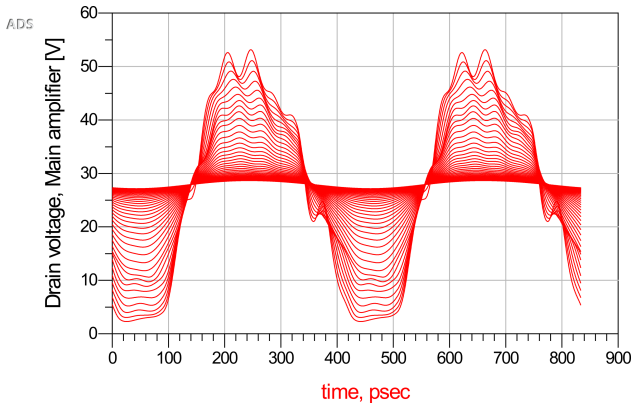
(h) Drain efficiency, no tracking



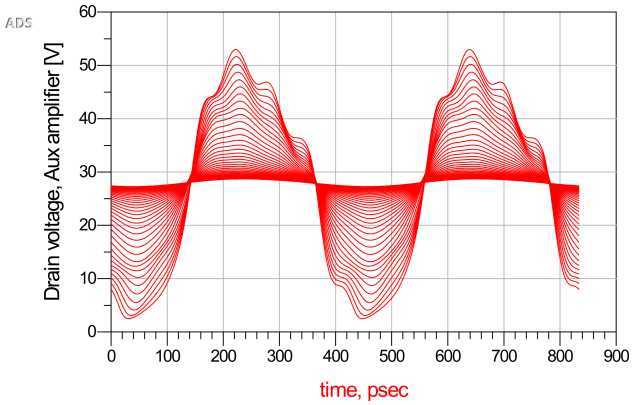
(i) Main amplifier drain current, No tracking.



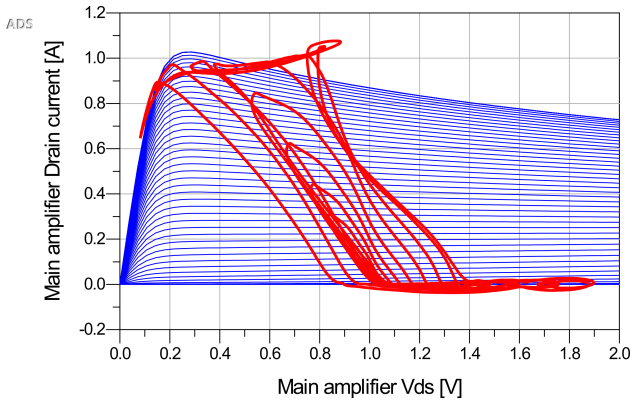
(j) Aux amplifier drain current.



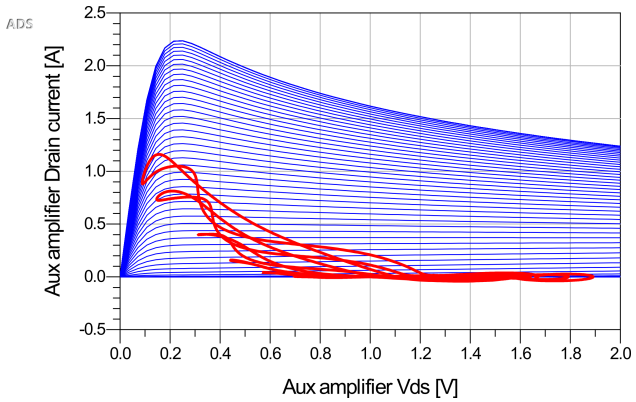
(k) Drain-source voltage for Main amplifier, no tracking.



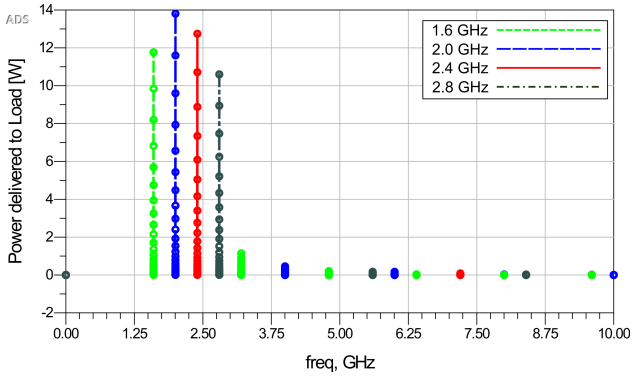
(l) Drain-Source voltage for Aux amplifier.



(m) Load line of Main amplifier, no tracking.



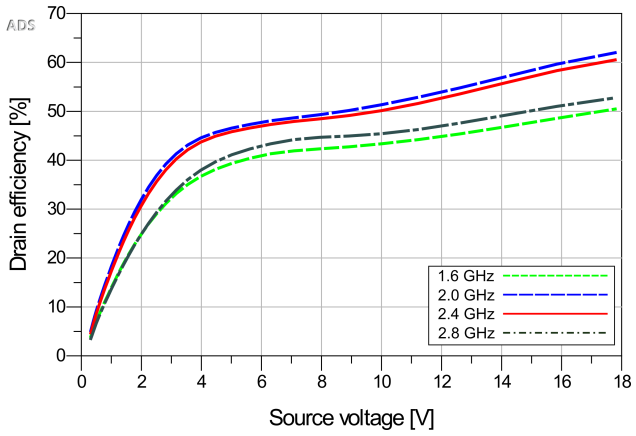
(n) Load line of Aux amplifier, no tracking.



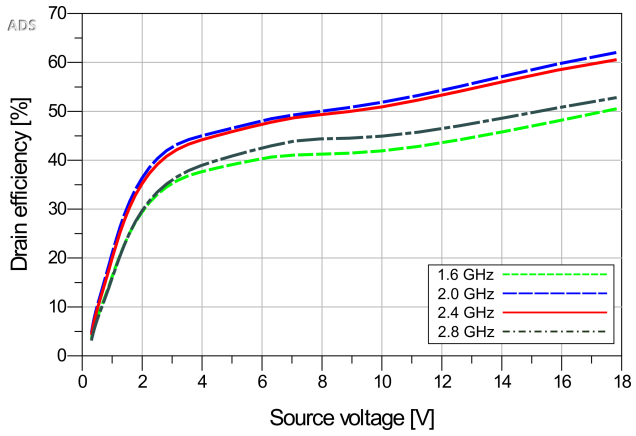
(o) Power delivered to load

Figure 49: Simulation results with no tracking.

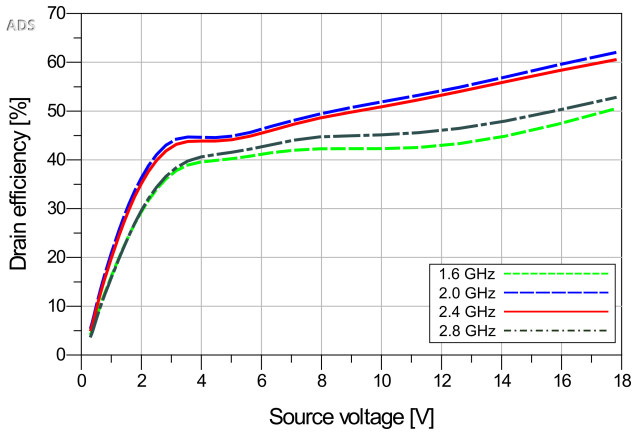
Figure 49 shows the simulation results for the amplifier before envelope tracking is implemented. Drain voltage of the main amplifier is set to 28 V. Loadlines shown in figures 49c and 49d are from the large signal analysis of the main and auxiliary amplifier, so there is no load modulation in effect. Figures 49m and 49n on the other hand is from the complete amplifier, and the effect on the loadlines can be observed. The X-axis of all the load line curves is normalized to supply voltage.
The results will be further discussed in section 5.1.



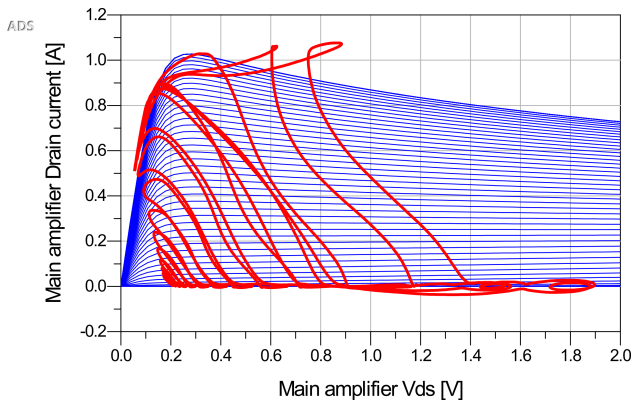
(a) Drain efficiency with linear tracking.



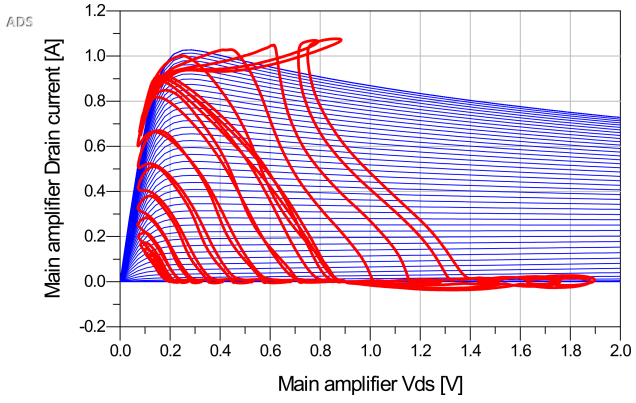
(b) Drain efficiency with tracking for PAE.



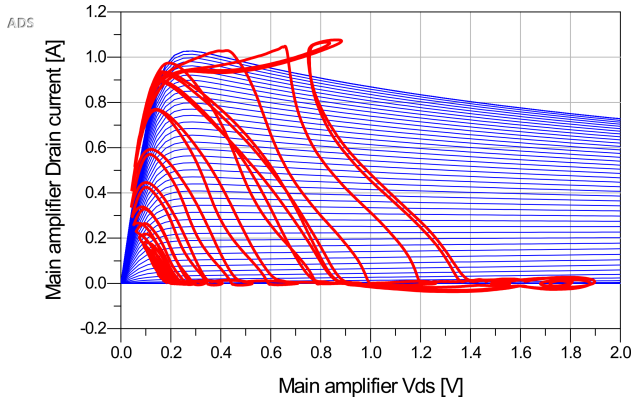
(c) Drain efficiency with tracking for saturation.



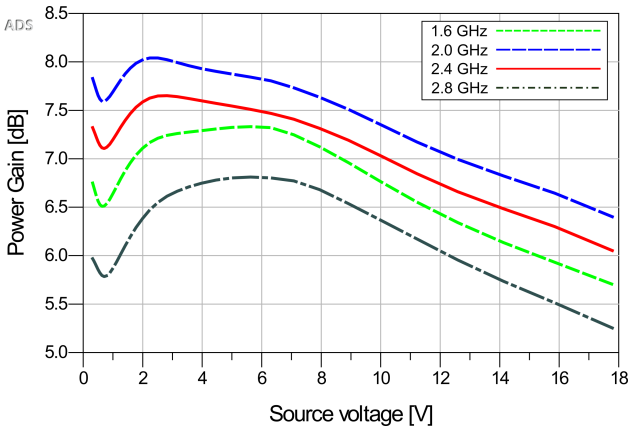
(d) Main amplifier loadline with linear tracking.



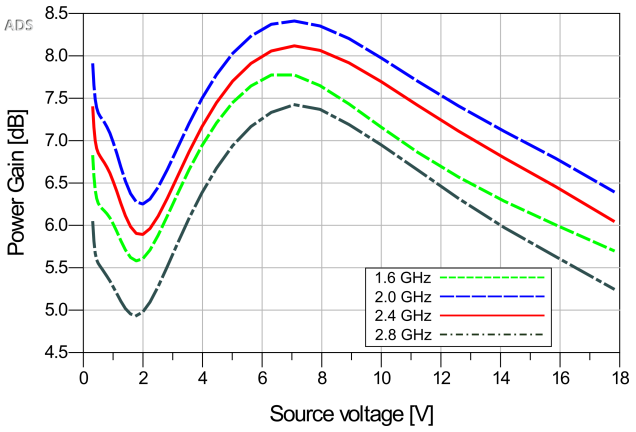
(e) Main amplifier loadline, tracking for PAE.



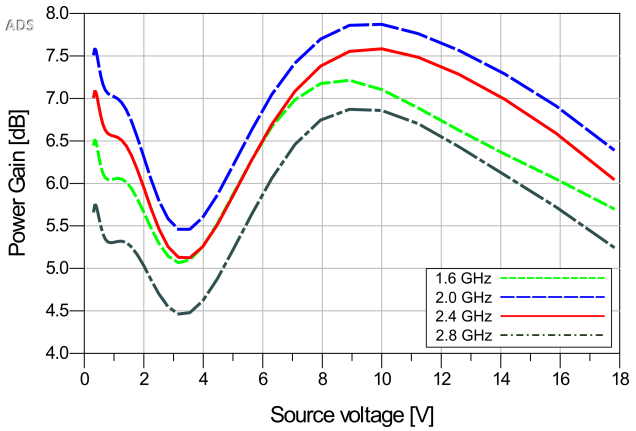
(f) Main amplifier loadline, tracking for saturation.



(g) Power gain, linear tracking.



(h) Power gain, tracking for PAE.



(i) Power gain, tracking for saturation.

Figure 50: Simulation results with three tracking methods.

Figure 50 shows simulation results after envelope tracking is implemented. Three tracking methods is used, as mentioned in section 3.8, linear tracking, tracking for optimized PAE and tracking for saturated load line. As in the previous figure, the X-axis of the load line figures is normalized to supply voltage. The results will be further discussed in section 5.1.

5 Discussion

5.1 Simulation results

The goal of this project was to design an amplifier with "real" MMIC components for a 800MHz band around 2.4GHz, 10 Watts output power and a doherty-like efficiency curve, on a 2mm^2 die area. Figures 50a, 50b and 50c show the efficiency curve criteria has been met, as all three envelope tracking methods gives the characteristic doherty efficiency curve. Figure 49g shows that at maximum input drive level 10 Watts or more is delivered to the load for the entire band, which fullfills the power criteria. In fact the amplifier is capable of delivering 10 Watts to a wider band than it was initially designed for, and 1.6 GHz was added to all the result plots where frequency is a factor, as the amplifier performs similarily at 1.6 GHz as 2.8 GHz. As such the actual center frequency can be defined as 2.2 GHz, with a bandwidth of 1.2 GHz, or 54.5% of center frequency, but for formalitys sake the center frequency will be kept at 2.4 GHz. This only shows the initial choice of bandwidth was too conservative.
As explained in section 3 all component models are of the MMIC models delivered by Wolfspeed, with the exception of the load and splitter. Interconnects however are ideal but as long as close attention is paid to their effect to phase, their impact on the performance of the system should be small. The only criteria which was not met was for the 2mm^2 die area. The technology from Wolfspeed is recently aquired by NTNU, and the area requirement was set from experience with previous technologies. During the design of the circuit it became apparent the components would simply be too large to fullfill the requirement, and it was therefore set aside. The complete amplifier without interconnects, vias and capacitor connectors is roughly 2.2x3.2mm^2. It is very likely that a more experienced MMIC designer would be able to further reduce the die area, bringing it closer the original requirement. It should be noted that the area requirement was not an essential part of the project as the true goal, as previously mentioned, is a proof of concept for the amplifier.
Figures 50g, 50h and 50i shows the power gain of the amplifier for the three envelope tracking methods explored. The gain lie between 4.5 and 8 dB, depending on which tracking method is used, which is somewhat low for a power amplifier. Part of the gain can be explained by looking at 49a and 49b. They show the S_{11} parameter for the input networks for the main and the aux amplifier respectively. The minima of the curves should be at the center frequency, they are however located well above the band. At center frequency the graphs show S_{11} to approximately be -11 dB for the main amplifier and -7.5 dB for the auxiliary amplifier. When this is taken into consideration along with the power lost at low drive levels due to the splitting of the signal, and loss from the components themselves, the full picture is starting to take form. As stated in section 3, the input network was initially designed for the simultaneous maximum gain impedances given by the design bench of ADS, and it is clear now that the impact of the

input network was severely underestimated. Some loss of gain at low drive levels can also be attributed to the envelope tracking, as it reduces the drain-source voltage, which is the main source of delivered power when the currents are small.

As described in section 3.8 three methods of tracking was explored. Linear, tracking for maximum PAE and tracking where the loadline is kept close to saturation at all times. Both PAE and saturation methods use a 6th order polynomial to control the drain voltage. This implies a tracker with a very wide bandwidth, which means it will be very complicated to make. It is therefore much easier, and more common, to make a linear voltage tracker. It is clear from figures 50a, 50b and 50c that the efficiency for the linear tracking method yields very similar results to the other two, being about 5 percentage points lower at low drive levels, while being almost identical at higher drive levels. These results point in the direction that making a more complicated tracker most likely isn't worth the cost and effort, and a linear tracker is a more reasonable choice.
The size of the class-C amplifier was chosen according to cripps' rule of thumb, which states the transistor should be 2.5 times larger than the transistor in the main amplifier. Figure 49d shows the load line of the class C amplifier, and it is clear that the transistor is very overdimensioned compared to what is needed. Reducing the transistor would further reduce the area of the amplifier die, and improve the efficiency of the class C amplifier at peak.
The gain seen in figure 50g varies with approximately 1.5dB during the drive level sweep. This affects the linearity of the amplifier, and figure 49o shows there are some harmonics delivered to the load. If better linearity is desired a technique such as predistortion might be a good solution.

5.2 Output network

As described in section 3.6 the output network was designed to include the internal parasitics of the transistors as part of the network. This gives much better control of what the internal current source sees, and allows for better compensation for unwanted parasitics. The final network was small and simple, but a more complicated network can be used to improve the results. Figures 43a and 43b show the impedances seen from the internal current source of the main amplifier, and aux amplifier respectively. Ideally the rightmost part of the lines, which is 2.8GHz and below, should lie around 25Ω, or 0.5 in the smith chart. The leftmost part of the line, which is 4GHz and above, should lie as close to physical short as possible, as this would function as a harmonic short and ensure proper class-B operation. Instead the impedances seen in band by the Main amplifier ranges from $18 + j052\Omega$ to$8.7 - j9.1\Omega$, and $16.5 + j0.24\Omega$ to $8.13 - j8.77\Omega$ for the auxiliary amplifier. A more complicated network might be able to achieve a better seperation between the two bands.

5.3 Optimal load error

The main amplifier was designed so that when at its peak, its load line would reach the knee of the IV-curves in accordance with the theories of Cripps for maximum power generation. The load which give this load line is called R_{opt}. The transistor size was thought to be chosen in the project before this one so that its R_{opt} was 50Ω. And it was therefore not given much more thought in this project. It was near the end of the project that it was discovered that the actual R_{opt} was closer to 25Ω, the reason this was not discovered sooner was that the results observed matched what was expected. The error in R_{opt} was probably due to a misunderstanding, and the load line was calculated for a class-A amplifier. The reason the results were as expected is due to the output network mismatch. The actual impedance observed by the Main amplifier is, as mentioned above, ranging from 8 to 18Ω. This means when the amplifier is operating at peak, the impedance seen by the internal current source is ranging from 16 to 36Ω, which is relatively close to the amplifiers actual R_{opt}.

6 Conclusion

The goal of this report was to present an overview of the theory deemed relevant for the project. This should give the reader the necessary information to understand the concept of operation, and evaluate the performance of the OLMET amplifier. A description of the steps taken to design the amplifier has been given, before the results were presented and evaluated. As described in section 5 all goals, but the area goal, were fulfilled, and the achieved bandwidth exceeded the original goal by approximately 400 MHz. The amplifier has a drain efficiency above 40% for a 12V input drive level span, from approximately 4-5 V to 18V, depending on frequency. This corresponds to a 13 dB power back off. The gain is somewhat low, but should be remedied by ensuring a better input and output match, or using two cascaded amplifiers if even more gain is needed. All components are designed to handle the currents found in the large signal analysis, and the amplifier is as such fairly close to being realizable. The amplifier shows a lot of potential and even better performance is expected in future designs as mistakes are avoided, and the methods in use become better adapted to the topology.

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[11] *Appendix I: Specific values and equations.*

[12] Jørn Frøysa. "Design av RF/mikrobølge integrerte kretser i GaN MMIC teknologi, Doherty design". Pre-Master Project. Norwegian University of Science and Technology, 2015.

List of Figures