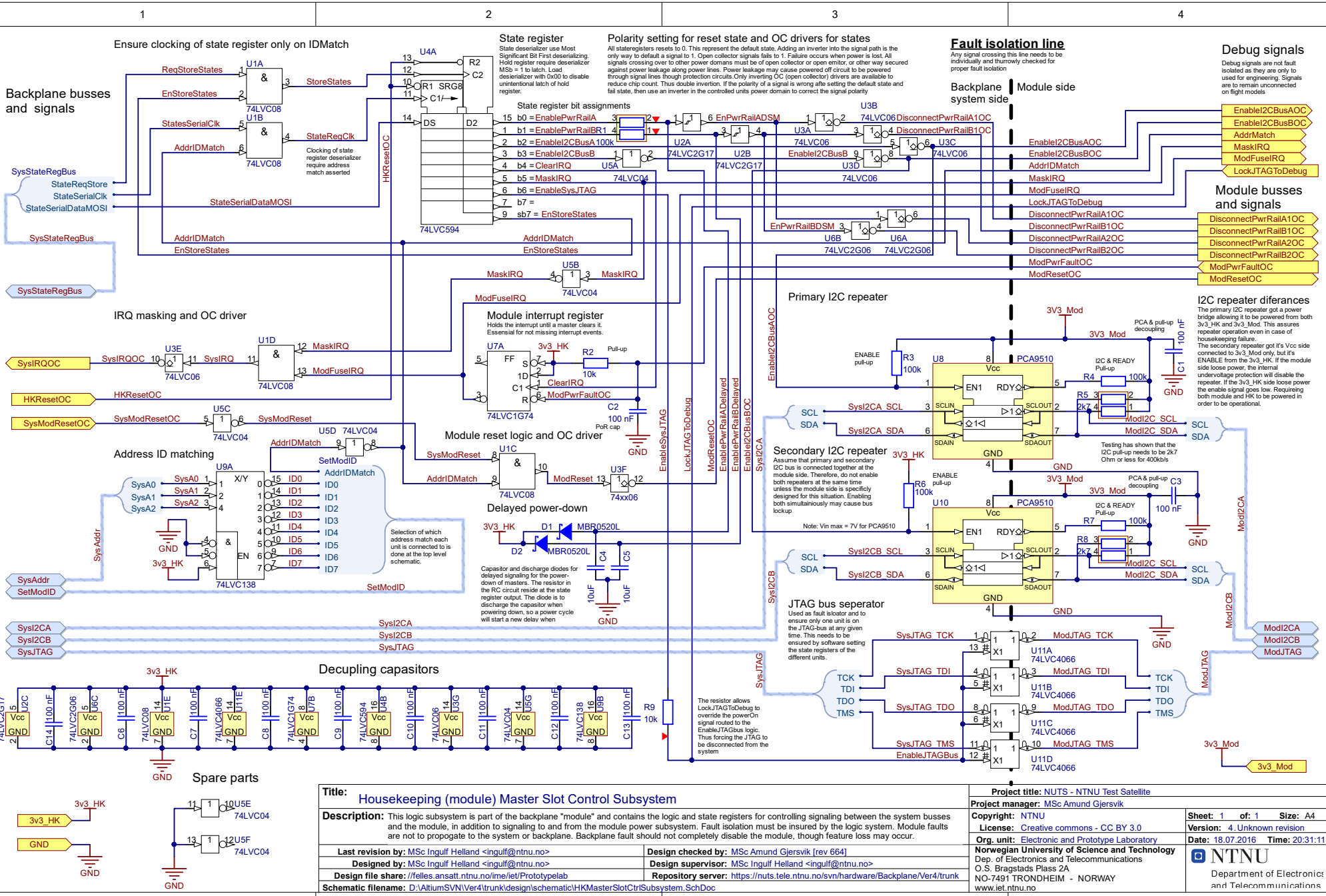
Ensure clocking of state register only on IDMatch
Backplane busses and signals
State register
State register bit assignments
Polarity setting for reset state and OC drivers for states
Fault isolation line
Backplane system side
Module side
Debug signals
Module busses and signals
IRQ masking and OC driver
Module interrupt register
Module reset logic and OC driver
Address ID matching
Delayed power-down
Primary I2C repeater
I2C repeater diferances
Secondary I2C repeater
JTAG bus seperator
Decupling capasitors
Spare parts
Title: Housekeeping (module) Master Slot Control Subsystem
Description: This logic subsystem is part of the backplane "module" and contains the logic and state registers for controlling signaling between the system busses and the module, in addition to signaling to and from the module power subsystem. Fault isolation must be insured by the logic system. Module faults are not to propogate to the system or backplane. Backplane fault should not completely disable the module, though feature loss may occur.
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Project manager: MSc Amund Gjersvik
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Org. unit: Electronic and Prototype Laboratory
Sheet: 1 of: 1 Size: A4
Version: 4.Unknown revision
Date: 18.07.2016 Time: 20:31:11
Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab
Design checked by: MSc Amund Gjersvik [rev 664]
Design supervisor: MSc Ingulf Helland <ingulf@ntnu.no>
Repository server: https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\HKMasterSlotCtrlSubsystem.SchDoc
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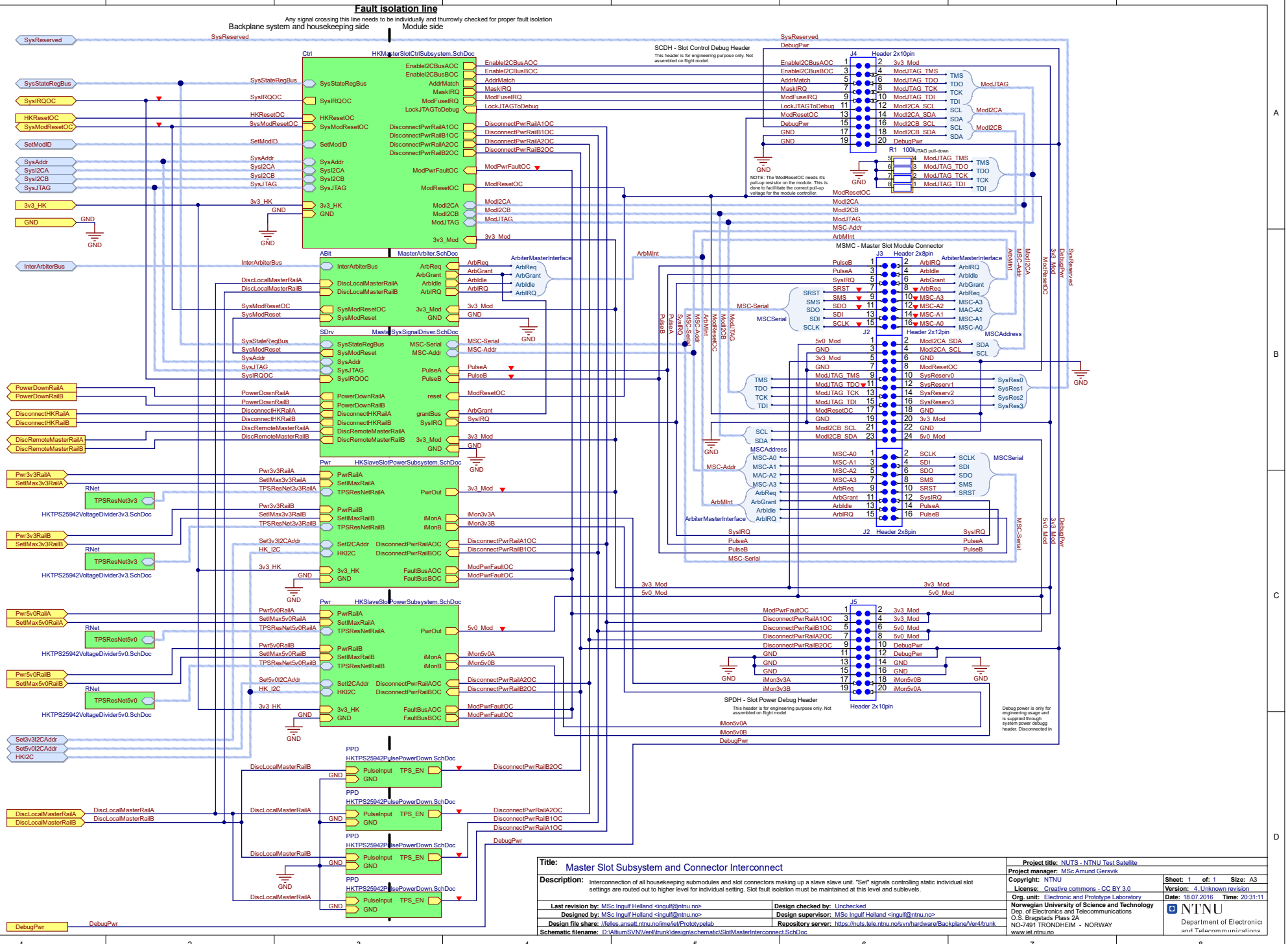
Fault isolation line
Any signal crossing this line needs to be individually and thurrowly checked for proper fault isolation
Backplane system and housekeeping side
Module side
HKMasterSlotCtrlSubsystem.SchDoc
MasterArbiter.SchDoc
MasterSysSignalDriver.SchDoc
HKSlaveSlotPowerSubsystem.SchDoc
HKSlaveSlotPowerSubsystem.SchDoc
HKTPS25942VoltageDivider3v3.SchDoc
HKTPS25942VoltageDivider3v3.SchDoc
HKTPS25942VoltageDivider5v0.SchDoc
HKTPS25942VoltageDivider5v0.SchDoc
HKTPS25942PulsePowerDown.SchDoc
HKTPS25942PulsePowerDown.SchDoc
HKTPS25942PulsePowerDown.SchDoc
HKTPS25942PulsePowerDown.SchDoc
SCDH - Slot Control Debug Header
This header is for engineering purpose only. Not assembled on flight model.
SPDH - Slot Power Debug Header
This header is for engineering purpose only. Not assembled on flight model.
MSMC - Master Slot Module Connector
Header 2x10pin
Header 2x12pin
Header 2x8pin
ModJTAG
ModI2CA
ModI2CB
MSCAddress
MSCSerial
R1 100k JTAG pull-down
NOTE: The !ModResetOC needs it's pull-up resistor on the module. This is done to facilitiate the correct pull-up voltage for the module controller.
Debug power is only for engineering usage and is supplied through system power debugg header. Disconnected in
Title: Master Slot Subsystem and Connector Interconnect
Description: Interconnection of all housekeeping submodules and slot connectors making up a slave slave unit. "Set" signals controlling static individual slot settings are routed out to higher level for individual setting. Slot fault isolation must be maintained at this level and sublevels.
Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\SlotMasterInterconnect.SchDoc
Design checked by: Unchecked
Design supervisor: MSc Ingulf Helland <ingulf@ntnu.no>
Repository server: https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Project title: NUTS - NTNU Test Satellite
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Org. unit: Electronic and Prototype Laboratory
Sheet: 1 of: 1 Size: A3
Version: 4 .Unknown revision
Date: 18.07.2016 Time: 20:31:11
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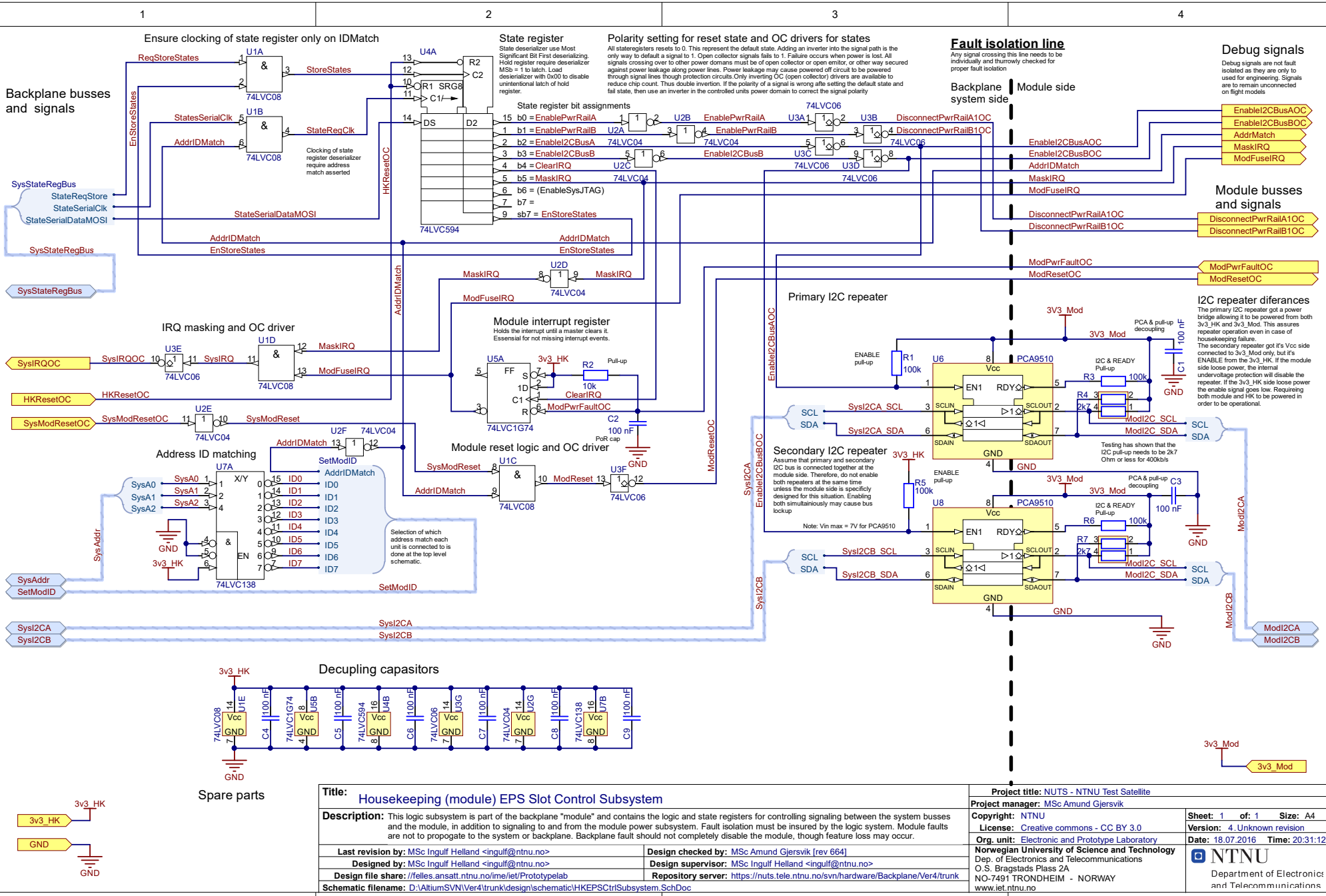
Ensure clocking of state register only on IDMatch
Backplane busses and signals
State register
State register bit assignments
Polarity setting for reset state and OC drivers for states
Fault isolation line
Backplane system side
Module side
Debug signals
Module busses and signals
IRQ masking and OC driver
Module interrupt register
Primary I2C repeater
I2C repeater diferances
Address ID matching
Module reset logic and OC driver
Secondary I2C repeater
Decupling capasitors
Spare parts
Title: Housekeeping (module) EPS Slot Control Subsystem
Description: This logic subsystem is part of the backplane "module" and contains the logic and state registers for controlling signaling between the system busses and the module, in addition to signaling to and from the module power subsystem. Fault isolation must be insured by the logic system. Module faults are not to propogate to the system or backplane. Backplane fault should not completely disable the module, though feature loss may occur.
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Sheet: 1 of: 1 Size: A4
Version: 4.Unknown revision
Date: 18.07.2016 Time: 20:31:12
Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab
Design checked by: MSc Amund Gjersvik [rev 664]
Design supervisor: MSc Ingulf Helland <ingulf@ntnu.no>
Repository server: https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\HKEPSCtrlSubsystem.SchDoc
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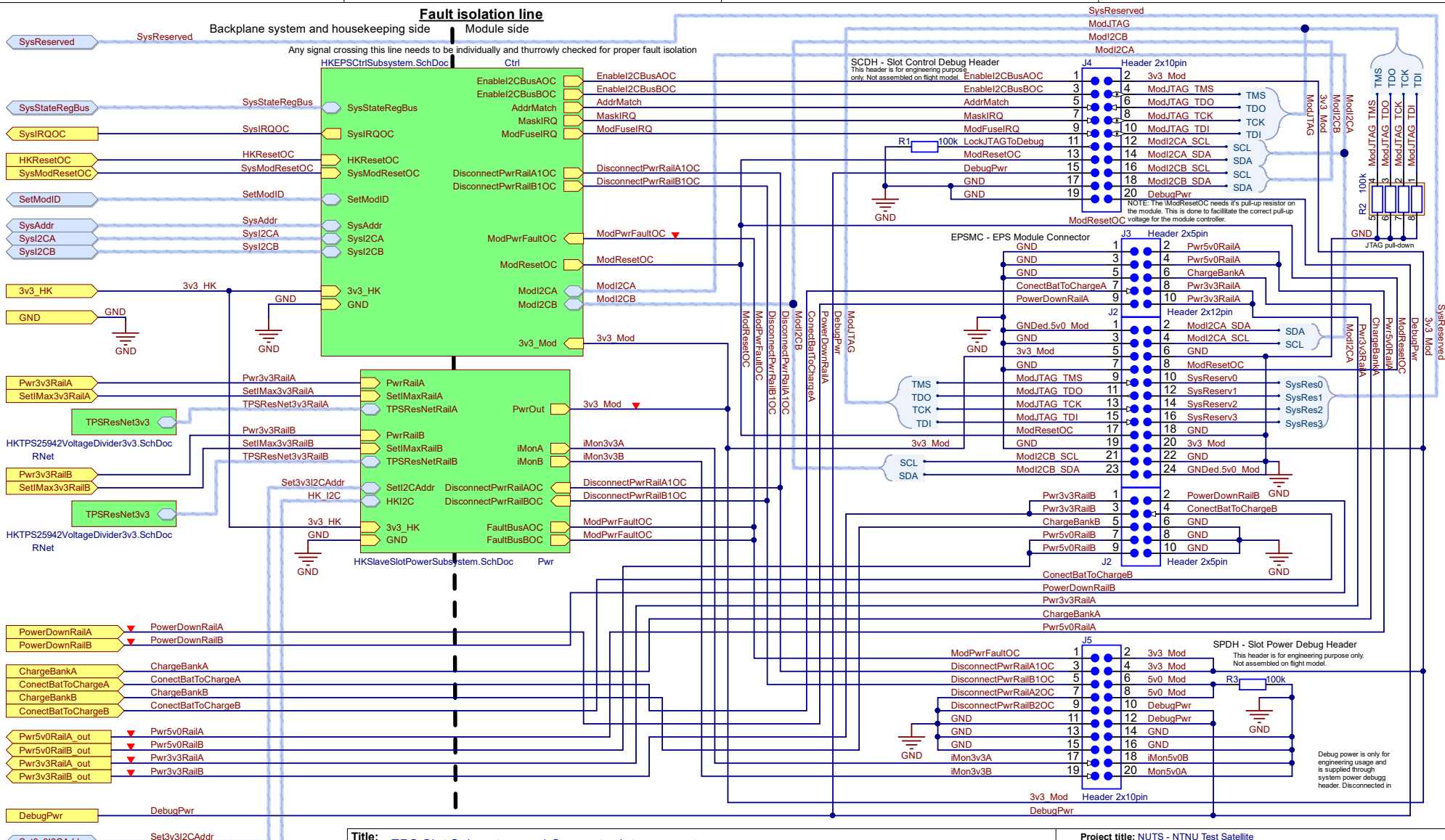

Title: EPS Slot Subsystem and Connector Interconnect

Description: Interconnection of all housekeeping submodules and slot connectors making up the EPS slot. "Set" signals controlling static individual slot settings are routed out to higher level for individual setting. Slot fault isolation must be maintained at this level and sublevels.

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Designed by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design supervisor:** MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab	**Repository server:** https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\SlotEPSInterconnect.SchDoc	

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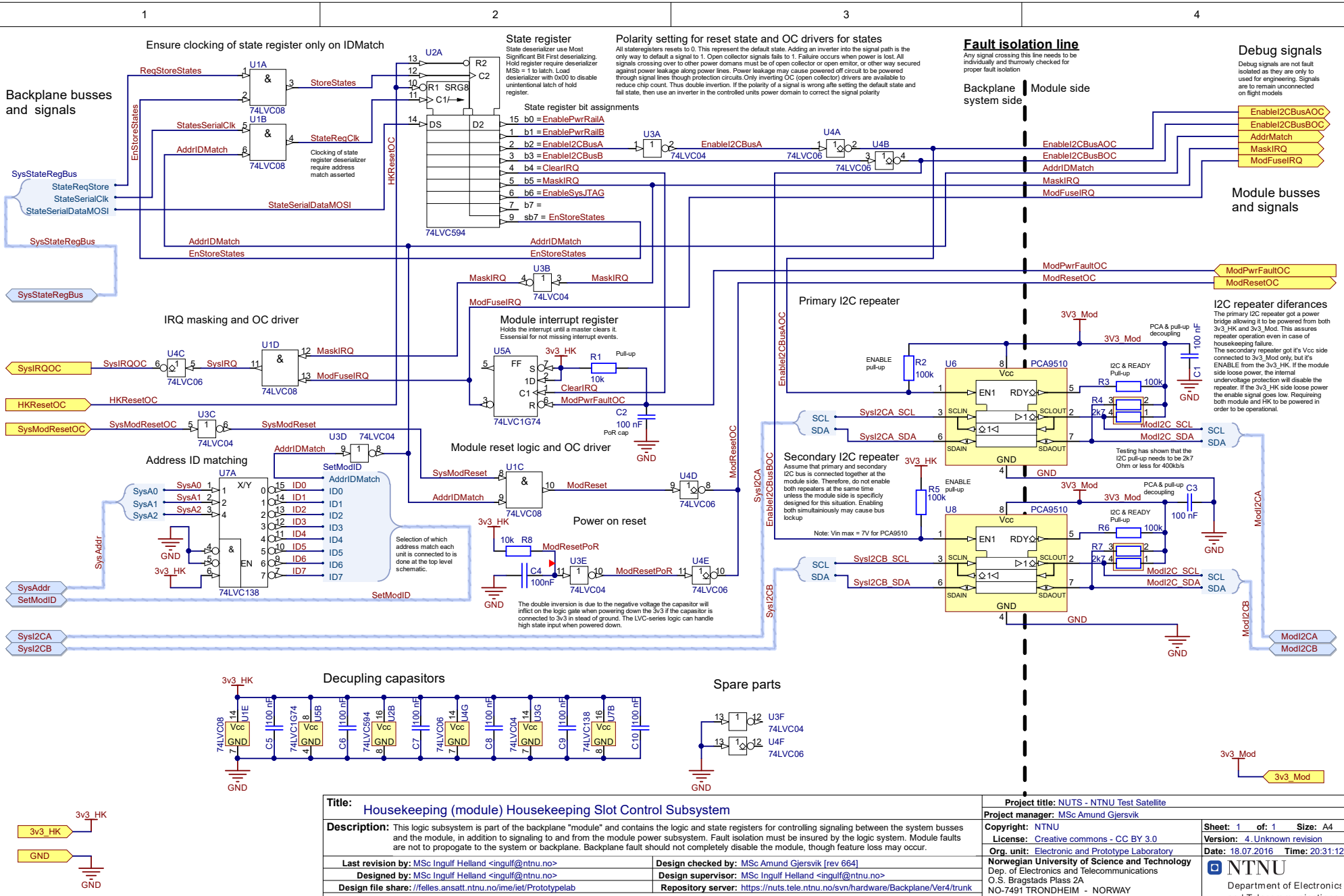
Ensure clocking of state register only on IDMatch
Backplane busses and signals
State register
State register bit assignments
Polarity setting for reset state and OC drivers for states
Fault isolation line
Backplane system side
Module side
Debug signals
Module busses and signals
IRQ masking and OC driver
Module interrupt register
Module reset logic and OC driver
Address ID matching
Power on reset
Primary I2C repeater
Secondary I2C repeater
I2C repeater diferances
Decupling capasitors
Spare parts
Title: Housekeeping (module) Housekeeping Slot Control Subsystem
Description: This logic subsystem is part of the backplane "module" and contains the logic and state registers for controlling signaling between the system busses and the module, in addition to signaling to and from the module power subsystem. Fault isolation must be insured by the logic system. Module faults are not to propogate to the system or backplane. Backplane fault should not completely disable the module, though feature loss may occur.
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Date: 18.07.2016 Time: 20:31:12
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Design checked by: MSc Amund Gjersvik [rev 664]
Design supervisor: MSc Ingulf Helland <ingulf@ntnu.no>
Repository server: https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\HKHousekeepingSlotCtrlSubsystem.SchDoc
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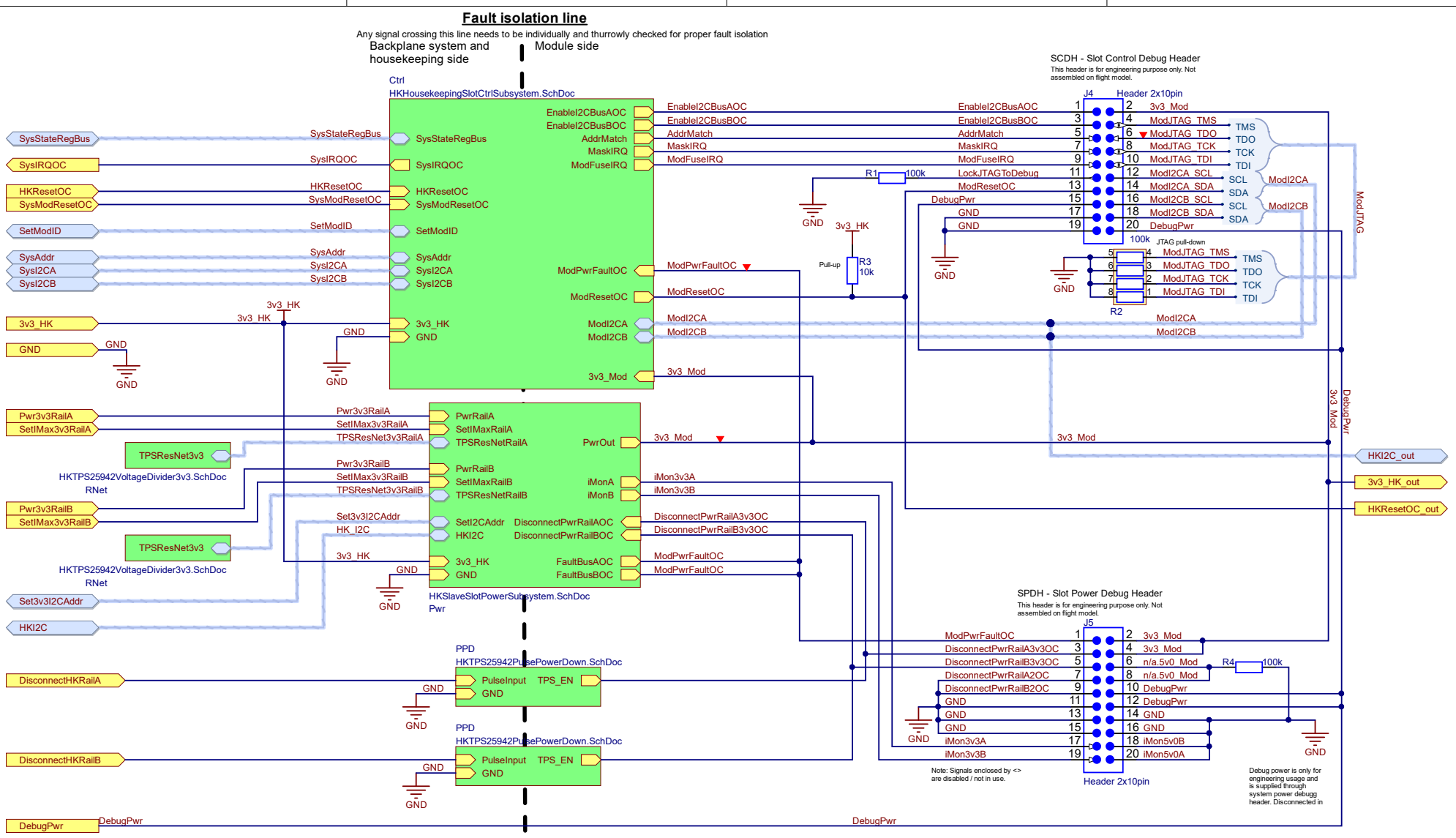

Title: Housekeeping Subsystem and Interconnect

Description: Interconnection of all subsustems making up the housekeeping "slot controller". Signals are routed from the housekeeping slot controller to the housekeeping subsystems on each individual unit through the HK_ signals. "Set" signals controlling static individual slot settings are routed out to higher level for individual setting. Slot fault isolation must be maintained at this level and sublevels.

Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design checked by:** Unchecked
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design supervisor:** MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab	**Repository server:** https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\SlotHousekeepingInterconnect.SchDoc	

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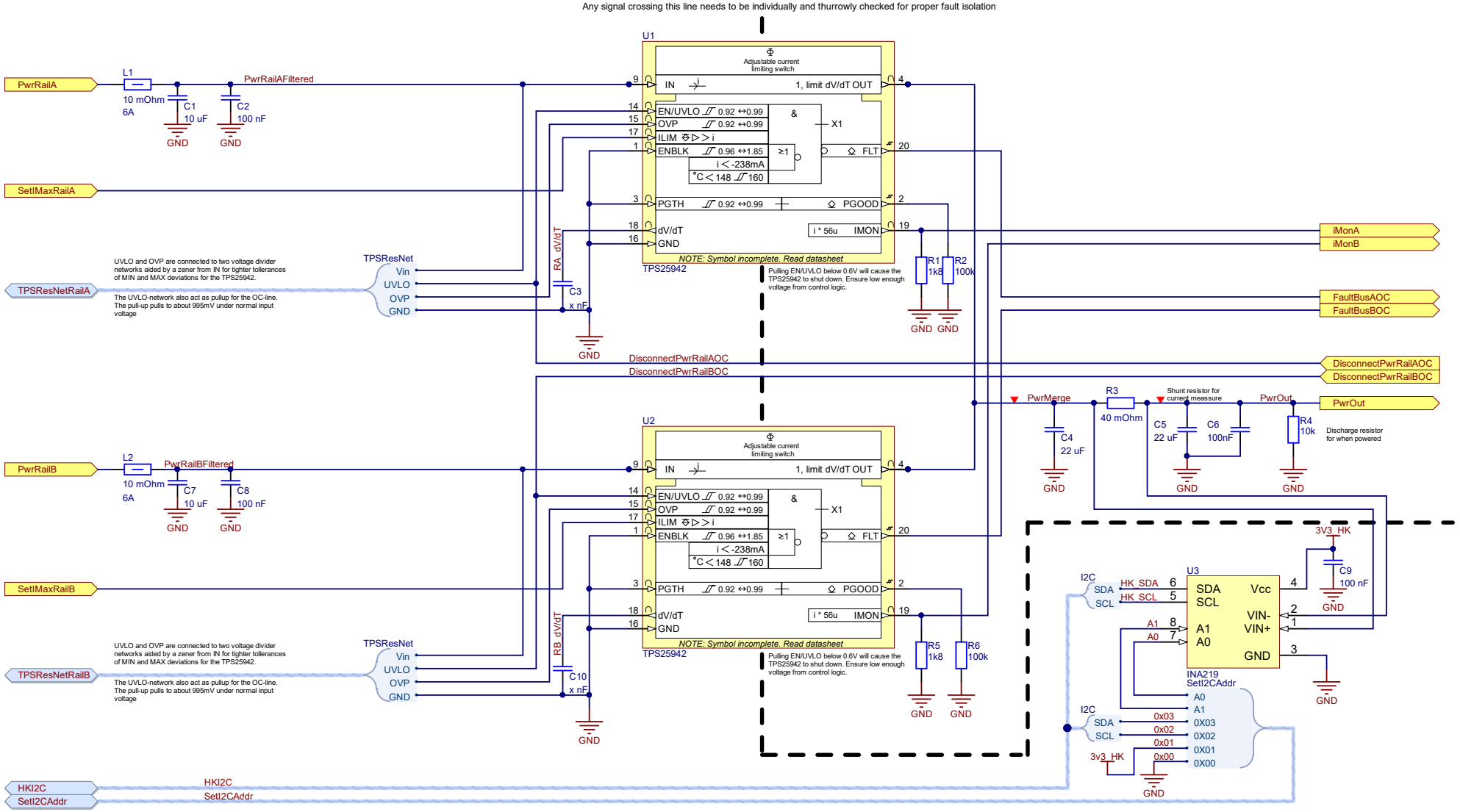
Fault isolation line

Any signal crossing this line needs to be individually and thurrowly checked for proper fault isolation



Title:	House Keeping (module) Slave Slot Controller Power Subsystem
Description:	
Last revision by:	MSc Ingulf Helland <ingulf@ntnu.no>
Designed by:	MSc Ingulf Helland <ingulf@ntnu.no>
Design file share:	//felles.ansatt.ntnu.no/ime/iet/Prototypelab
Schematic filename:	D:\AltiumSVN\Ver4\trunk\design\schematic\HKSlaveSlotPowerSubsystem.SchDoc
Design checked by:	Unchecked
Design supervisor:	MSc Ingulf Helland <ingulf@ntnu.no>
Repository server:	https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk

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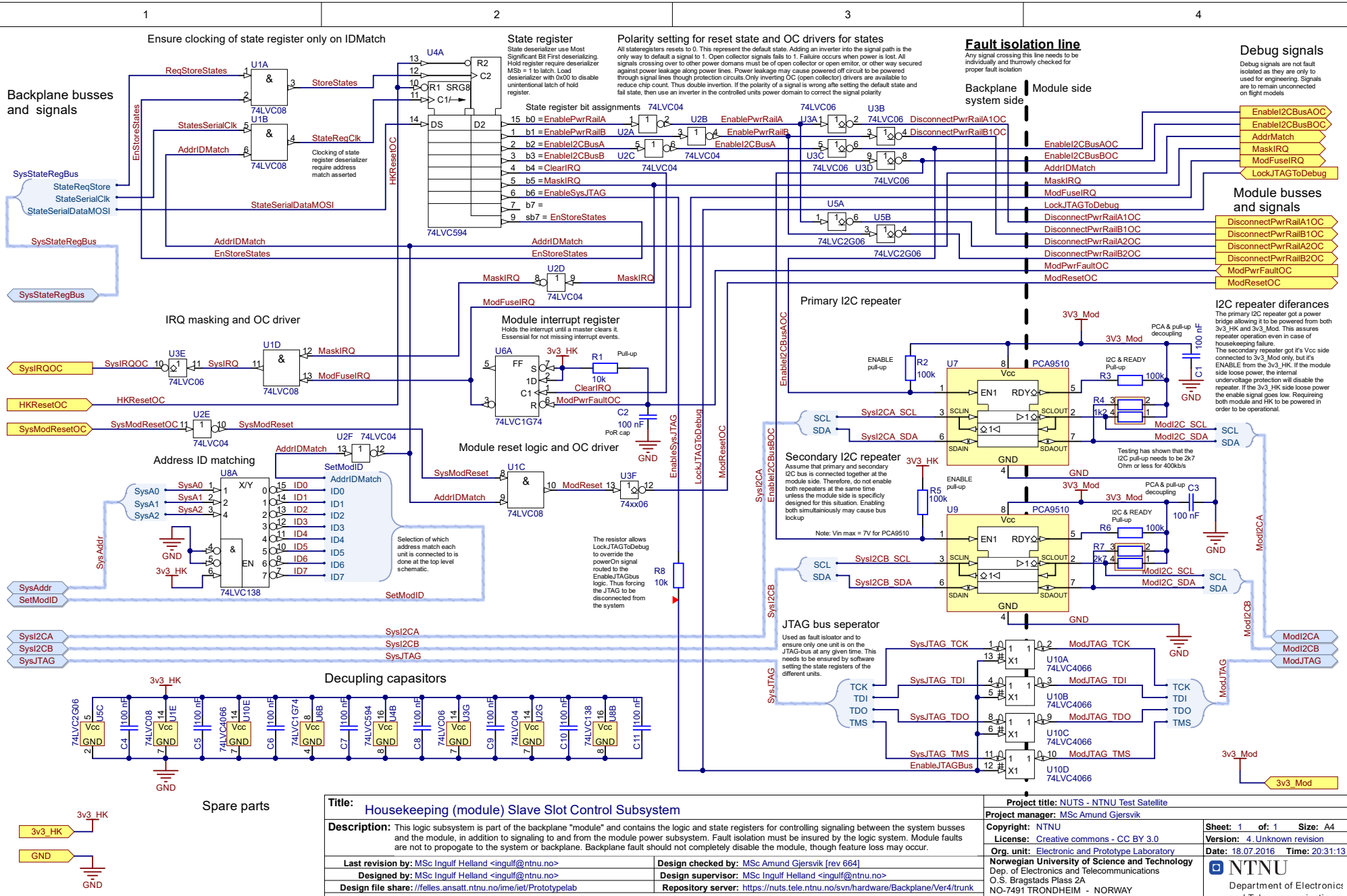
Backplane busses and signals
Ensure clocking of state register only on IDMatch
State register
State register bit assignments
Polarity setting for reset state and OC drivers for states
Fault isolation line
Backplane system side
Module side
Debug signals
Module busses and signals
IRQ masking and OC driver
Module interrupt register
Module reset logic and OC driver
Address ID matching
Primary I2C repeater
I2C repeater diferances
Secondary I2C repeater
JTAG bus seperator
Decupling capasitors
Spare parts
Title: Housekeeping (module) Slave Slot Control Subsystem
Description: This logic subsystem is part of the backplane "module" and contains the logic and state registers for controlling signaling between the system busses and the module, in addition to signaling to and from the module power subsystem. Fault isolation must be insured by the logic system. Module faults are not to propogate to the system or backplane. Backplane fault should not completely disable the module, though feature loss may occur.
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Date: 18.07.2016 Time: 20:31:13
Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab
Design checked by: MSc Amund Gjersvik [rev 664]
Design supervisor: MSc Ingulf Helland <ingulf@ntnu.no>
Repository server: https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\HKSlaveSlotCtrlSubsystem.SchDoc
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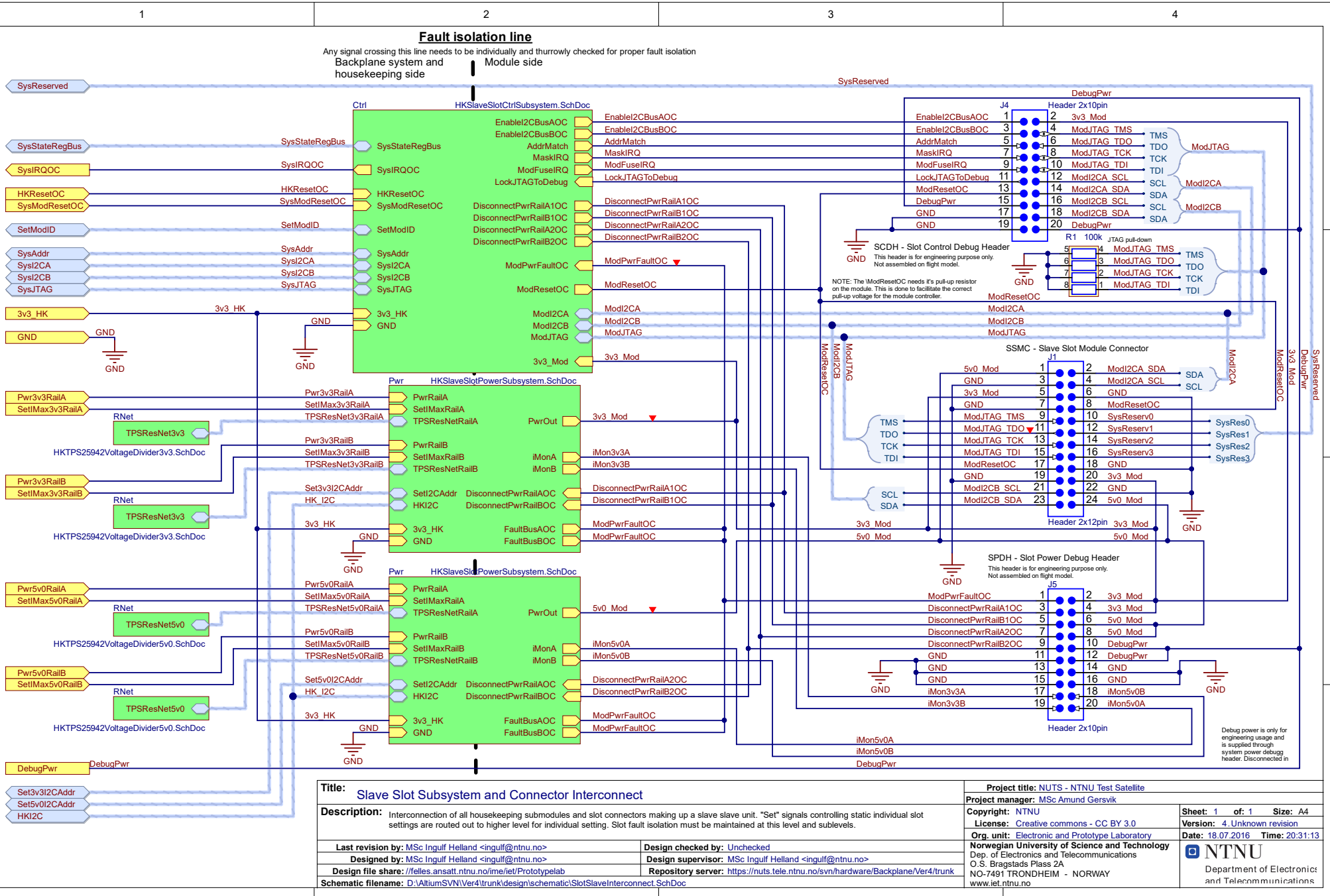

Title: Slave Slot Subsystem and Connector Interconnect

Description: Interconnection of all housekeeping submodules and slot connectors making up a slave slave unit. "Set" signals controlling static individual slot settings are routed out to higher level for individual setting. Slot fault isolation must be maintained at this level and sublevels.

Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design checked by:** Unchecked
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design supervisor:** MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab	**Repository server:** https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\SlotSlaveInterconnect.SchDoc	

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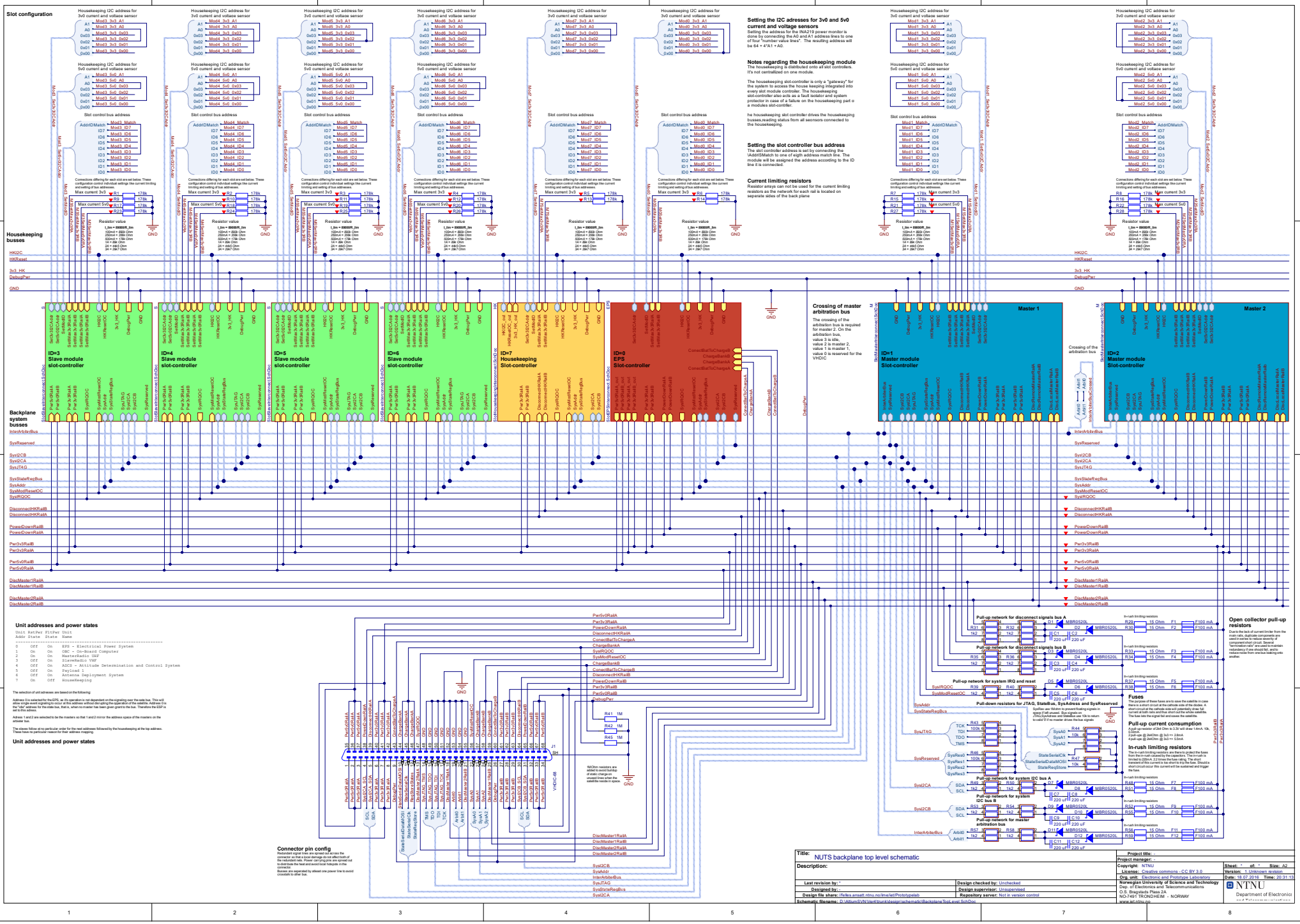
Slot configuration
Housekeeping busses
Backplane system busses
ID=3 Slave module slot-controller
ID=4 Slave module slot-controller
ID=5 Slave module slot-controller
ID=6 Slave module slot-controller
ID=7 Housekeeping Slot-Controller
ID=0 EPS Slot-Controller
ID=1 Master module Slot-Controller
ID=2 Master module Slot-Controller
Master 1
Master 2
Setting the I2C adresses for 3v0 and 5v0 current and voltage sensors
Notes regarding the housekeeping module
Setting the slot controller bus address
Current limiting resistors
Crossing of master arbitration bus
Unit addresses and power states
Unit addresses and power states
Connector pin config
Pull-up network for disconnect signals bus A
Pull-up network for disconnect signals bus B
Pull-up network for system IRQ and reset
Pull-down resistors for JTAG, StateBus, SysAdress and SysReserved
Pull-up network for system I2C bus A
Pull-up network for system I2C bus B
Pull-up network for master arbitration bus
Open collector pull-up resistors
Fuses
Pull-up current consumption
In-rush limiting resistors
Title: NUTS backplane top level schematic
Description:
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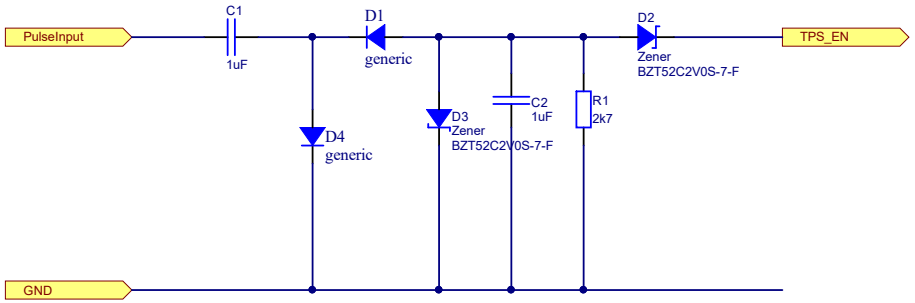

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Description:		**Project manager:** -	
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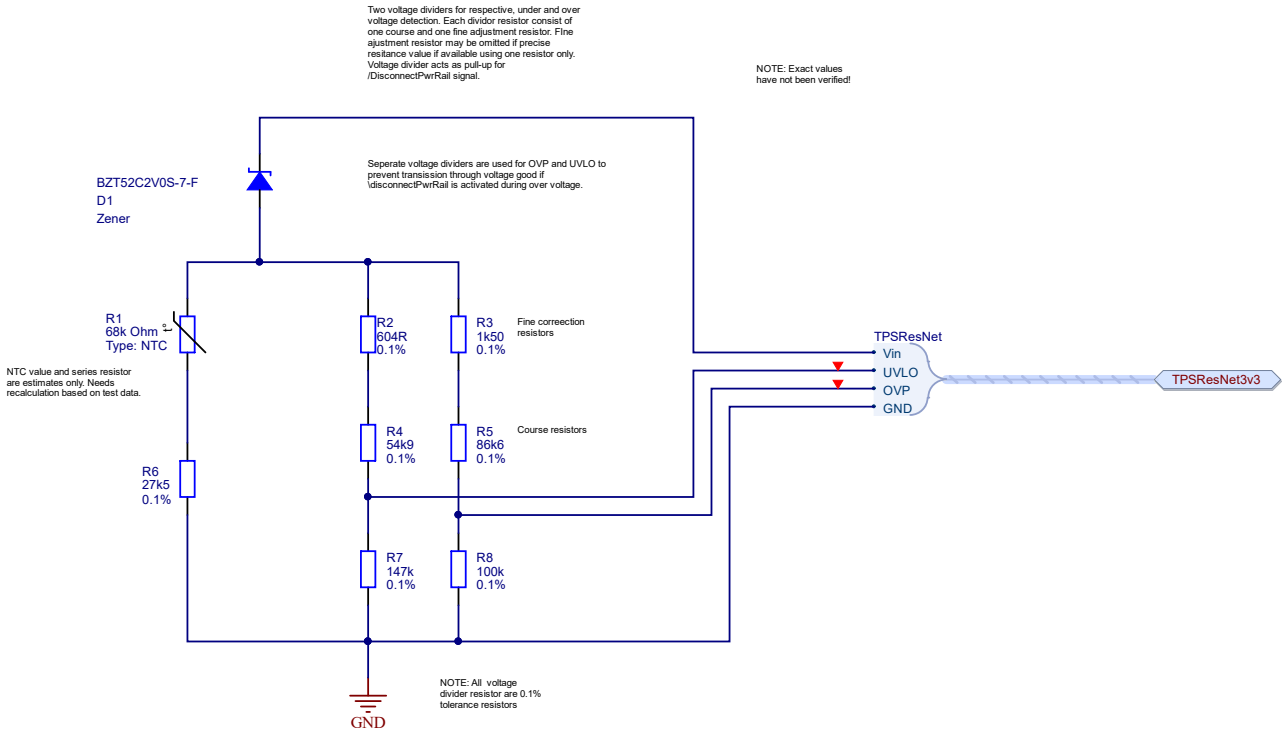
		License: Creative commons - CC BY 3.0	**Version:** 1.Unknown revision
		Org. unit: Electronic and Prototype Laboratory	**Date:** 18.07.2016 **Time:** 20:31:14
Last revision by: -	**Design checked by:** Unchecked	**Norwegian University of Science and Technology** Dep. of Electronics and Telecommunications O.S. Bragstads Plass 2A NO-7491 TRONDHEIM - NORWAY www.iet.ntnu.no	NTNU Department of Electronics and Telecommunications
Designed by: -	**Design supervisor:** Unsupervised		
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab	**Repository server:** Not in version control		
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\HKTPS25942PulsePowerDown.SchDoc			



Title:	TPS25942-voltage divider for 3v3
Description:	
Last revision by:	MSc Ingulf Helland <ingulf@ntnu.no>
Designed by:	MSc Ingulf Helland <ingulf@ntnu.no>
Design file share:	//felles.ansatt.ntnu.no/ime/iet/Prototypelab
Schematic filename:	D:\AltiumSVN\Ver4\trunk\design\schematic\HKTPS25942VoltageDivider3v3.SchDoc
Design checked by:	Unchecked
Design supervisor:	MSc Ingulf Helland <ingulf@ntnu.no>
Repository server:	https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk

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Version:	4.Unknown revision
Date:	18.07.2016 **Time:** 20:31:14

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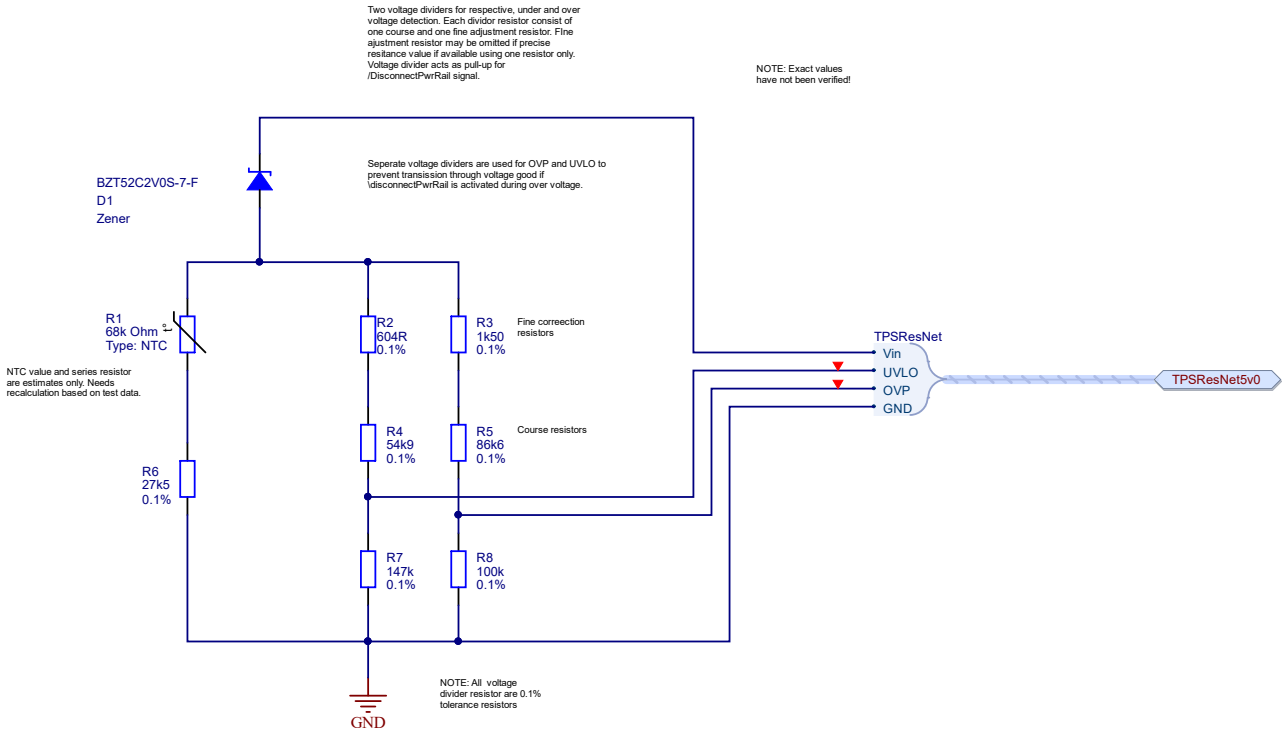

Title:	TPS25942-voltage divider for 3v3
Description:	
Last revision by:	MSc Ingulf Helland <ingulf@ntnu.no>
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Schematic filename:	D:\AltiumSVN\Ver4\trunk\design\schematic\HKTPS25942VoltageDivider5v0.SchDoc
Design checked by:	Unchecked
Design supervisor:	MSc Ingulf Helland <ingulf@ntnu.no>
Repository server:	https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk

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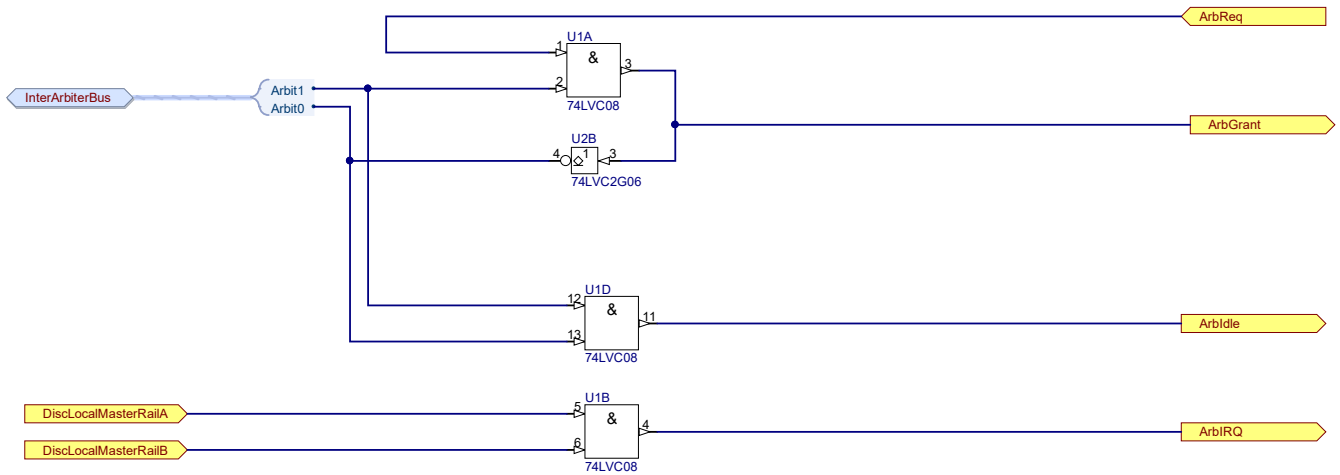
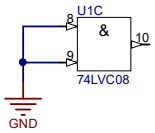
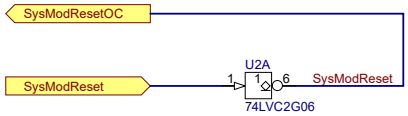
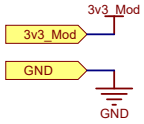


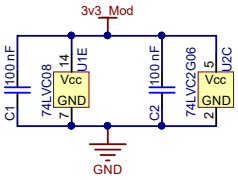
Spare parts



74LCV2G06 reside in this subsheet in order for the \SysModResetOC to share IC with the InterArb OC driver.







Title: MasterArbiter

Description:

Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design checked by:** Unchecked
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>	**Design supervisor:** MSc Ingulf Helland <ingulf@ntnu.no>
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab	**Repository server:** https://nuts.tele.ntnu.no/svn/hardware/Backplane/Ver4/trunk
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\MasterArbiter.SchDoc	

Project title: NUTS - NTNU Test Satellite
Project manager: MSc Amund Gersvik
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Sheet: * **of:** * **Size:** A4
Version: 1.Unknown revision
Date: 18.07.2016 **Time:** 20:31:14

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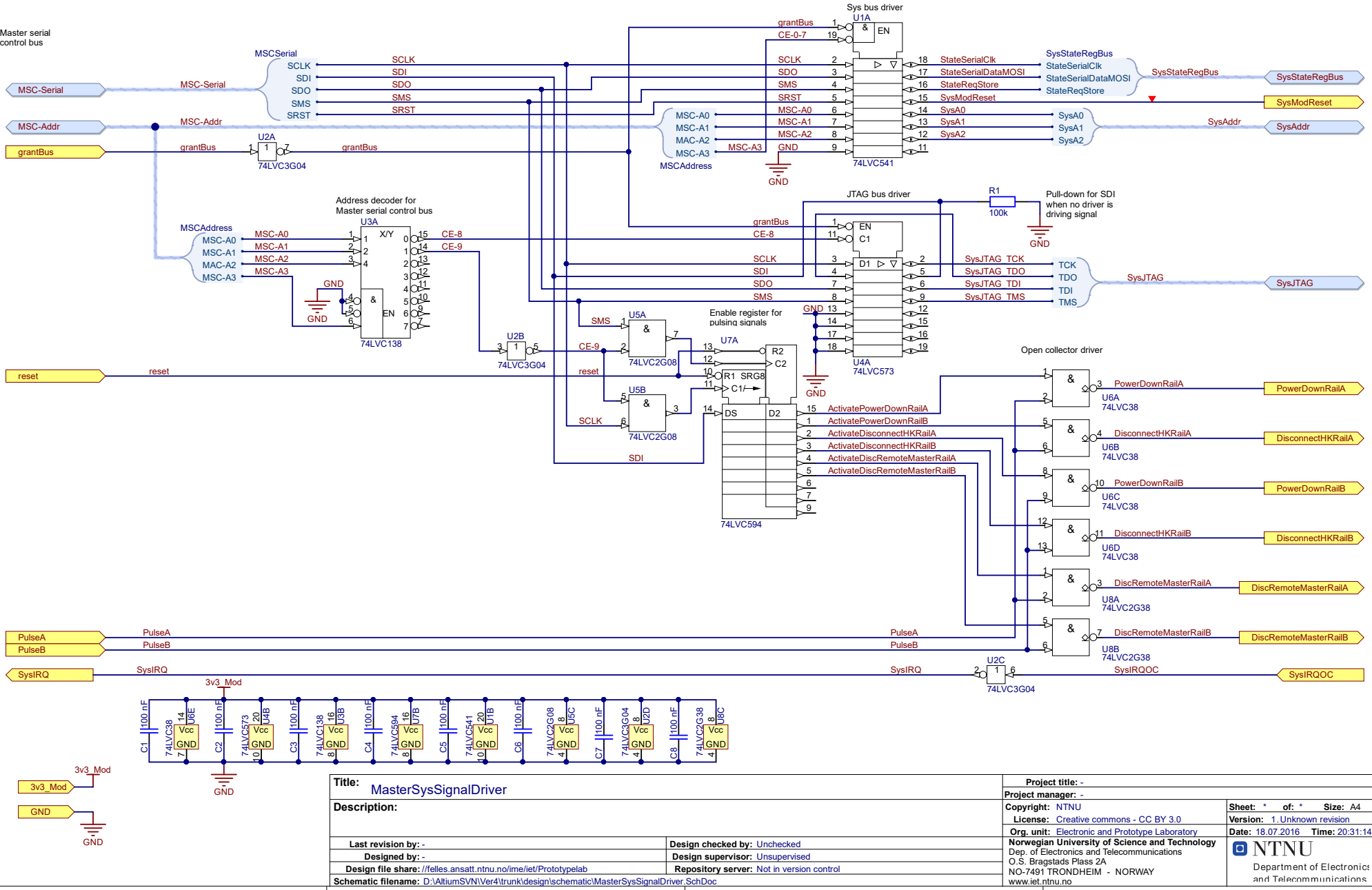
Master serial control bus
MSC-Serial
MSC-Addr
grantBus
MSCSerial
SCLK
SDI
SDO
SMS
SRST
MSCAddress
MSC-A0
MSC-A1
MAC-A2
MSC-A3
U2A
74LVC3G04
Address decoder for Master serial control bus
U3A
74LVC138
CE-8
CE-9
GND
Sys bus driver
U1A
CE-0-7
StateSerialClk
StateSerialDataMOSI
StateReqStore
SysModReset
SysA0
SysA1
SysA2
SysStateRegBus
SysAddr
74LVC541
JTAG bus driver
R1
100k
Pull-down for SDI when no driver is driving signal
SysJTAG_TCK
SysJTAG_TDO
SysJTAG_TDI
SysJTAG_TMS
TCK
TDO
TDI
TMS
SysJTAG
U4A
74LVC573
Enable register for pulsing signals
U5A
U5B
74LVC2G08
U7A
R1 SRG8
C1/
R2
C2
D1
D2
DS
74LVC594
U2B
reset
Open collector driver
ActivatePowerDownRailA
ActivatePowerDownRailB
ActivateDisconnectHKRailA
ActivateDisconnectHKRailB
ActivateDiscRemoteMasterRailA
ActivateDiscRemoteMasterRailB
PowerDownRailA
PowerDownRailB
DisconnectHKRailA
DisconnectHKRailB
DiscRemoteMasterRailA
DiscRemoteMasterRailB
U6A
U6B
U6C
U6D
U8A
U8B
74LVC38
74LVC2G38
PulseA
PulseB
SysIRQ
U2C
SysIRQOC
3v3_Mod
100 nF
C1
C2
C3
C4
C5
C6
C7
C8
U6E
U4B
U3B
U7B
U1B
U5C
U2D
U6C
Vcc
GND
Title: MasterSysSignalDriver
Description:
Project title: -
Project manager: -
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Org. unit: Electronic and Prototype Laboratory
Sheet: * of: * Size: A4
Version: 1.Unknown revision
Date: 18.07.2016 Time: 20:31:14
Last revision by: -
Designed by: -
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Design supervisor: Unsupervised
Design file share: //felles.ansatt.ntnu.no/ime/iet/Prototypelab
Repository server: Not in version control
Schematic filename: D:\AltiumSVN\Ver4\trunk\design\schematic\MasterSysSignalDriver.SchDoc
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