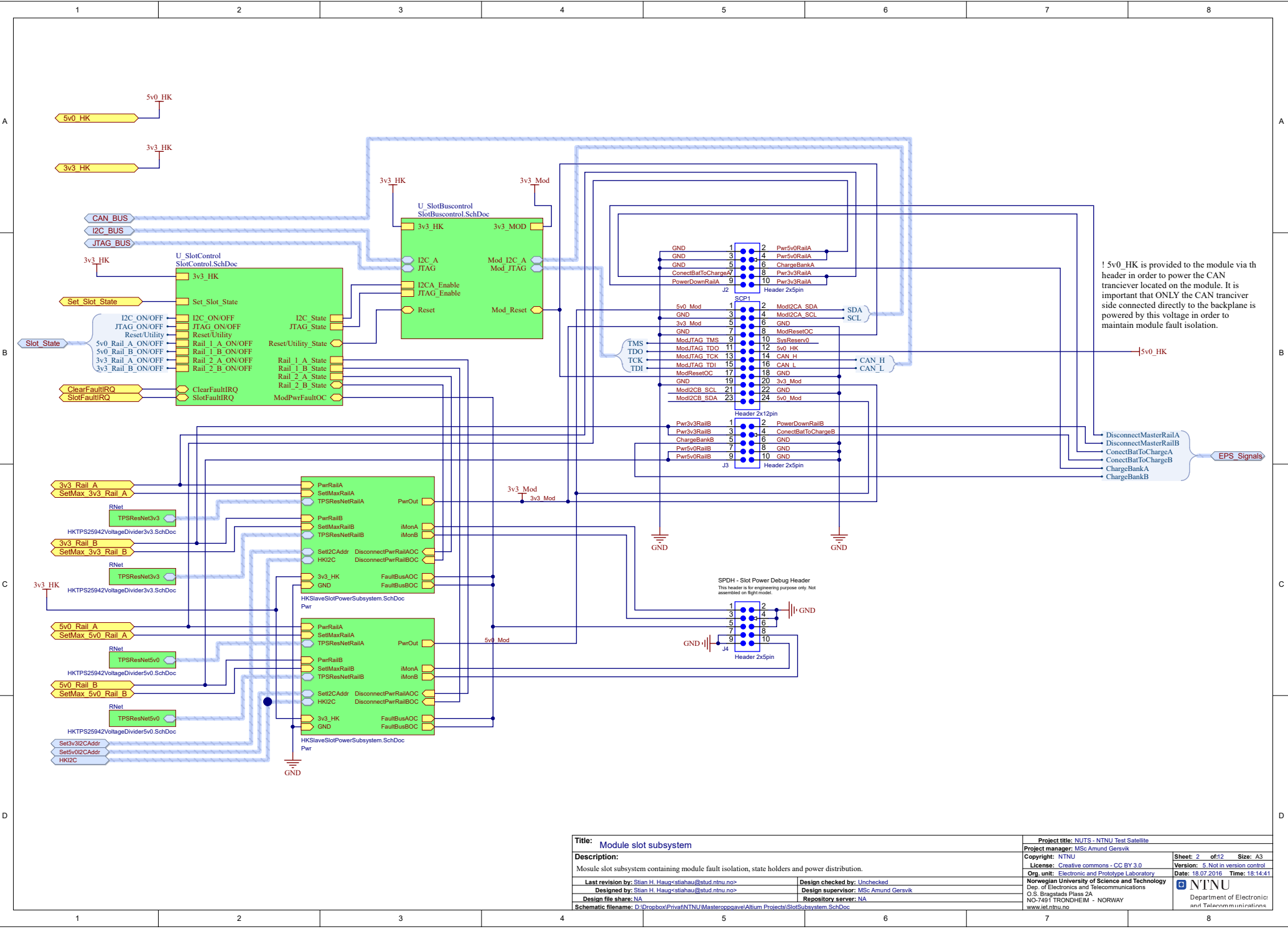
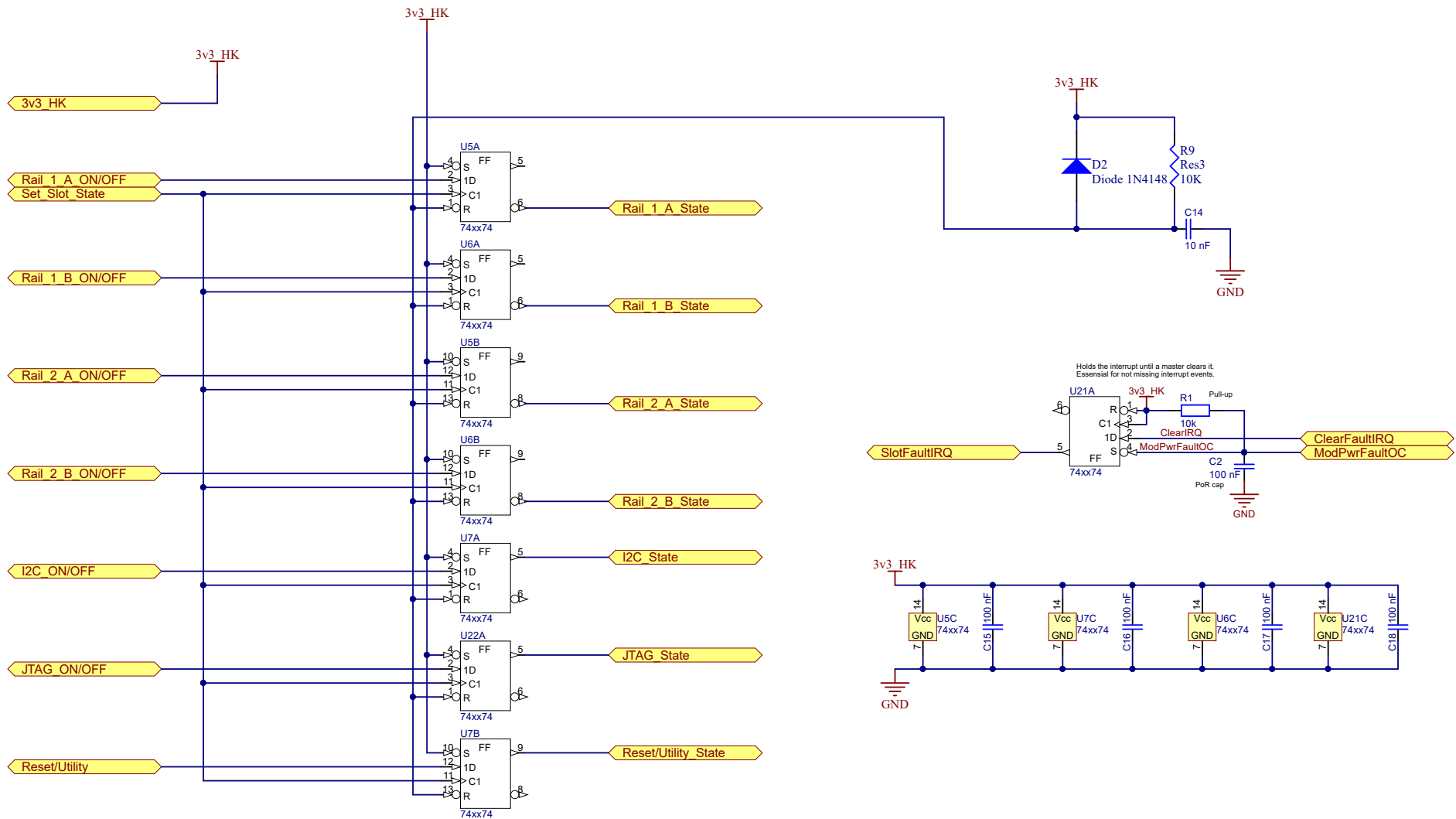


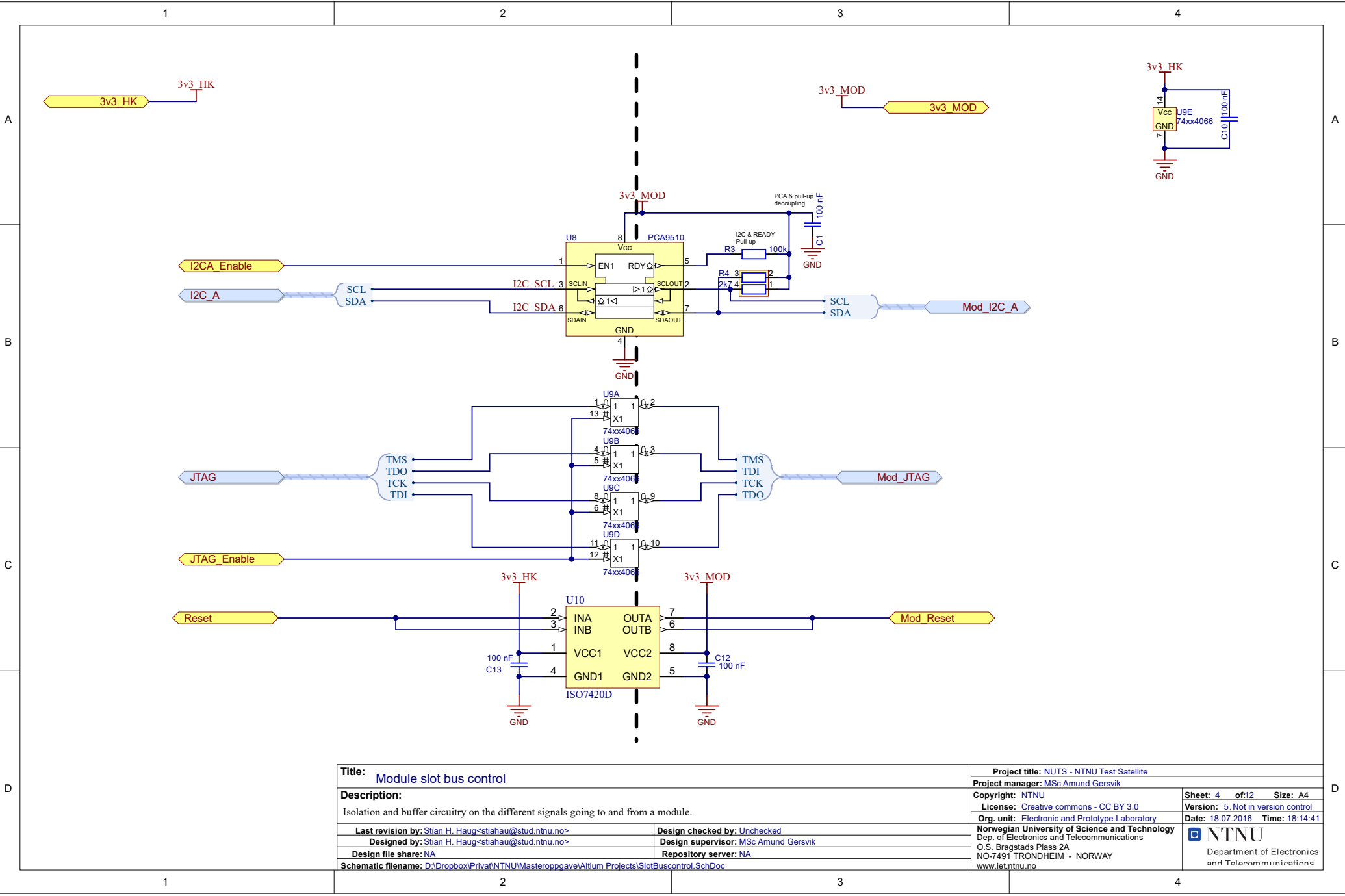
Title:		Project title:	
Description:		Copyright: NTNU	
Last revision by: Eirik H. Hagen		License: Creative Commons - CC BY 3.0	
Designed by: Eirik H. Hagen		Design checked by: Unik	
Drawn by: Eirik H. Hagen		Design supervisor: Mikael Amund Gensvik	
Schedule: Eirik H. Hagen		Repository server: Mikael Amund Gensvik	
		Sheet: 1 of 2	
		Version: 1.0.0	
		Date: 18.07.2018	
		Time: 18.14.41	
		NTNU	
		Department of Electronics and Telecommunications	



Title: Module slot subsystem				Project title: NUTS - NTNU Test Satellite			
Description: Module slot subsystem containing module fault isolation, state holders and power distribution.				Project manager: MSc Amund Gersvik			
Last revision by: Sitan H. Haugstahau@stud.ntnu.no>				Copyright: NTNU			
Designed by: Sitan H. Haugstahau@stud.ntnu.no>				License: Creative commons - CC BY 3.0			
Design file share: NA				Org. unit: Electronic and Prototype Laboratory			
Schematic filename: D:\Dropbox\Privat\NTNU\Masteroppgave\Allium Projects\SlotSubsystem.SchDoc				Design supervisor: MSc Amund Gersvik			
				Repository server: NA			
				Norwegian University of Science and Technology Dep. of Electronics and Telecommunications O.S. Bragestads Plass 2A NO-7491 TRONDHEIM - NORWAY www.iet.ntnu.no			
				NTNU Department of Electronics and Telecommunications			
				Sheet: 2 of 12 Size: A3			
				Version: 5. Not in version control Date: 18.07.2016 Time: 18:14:41			



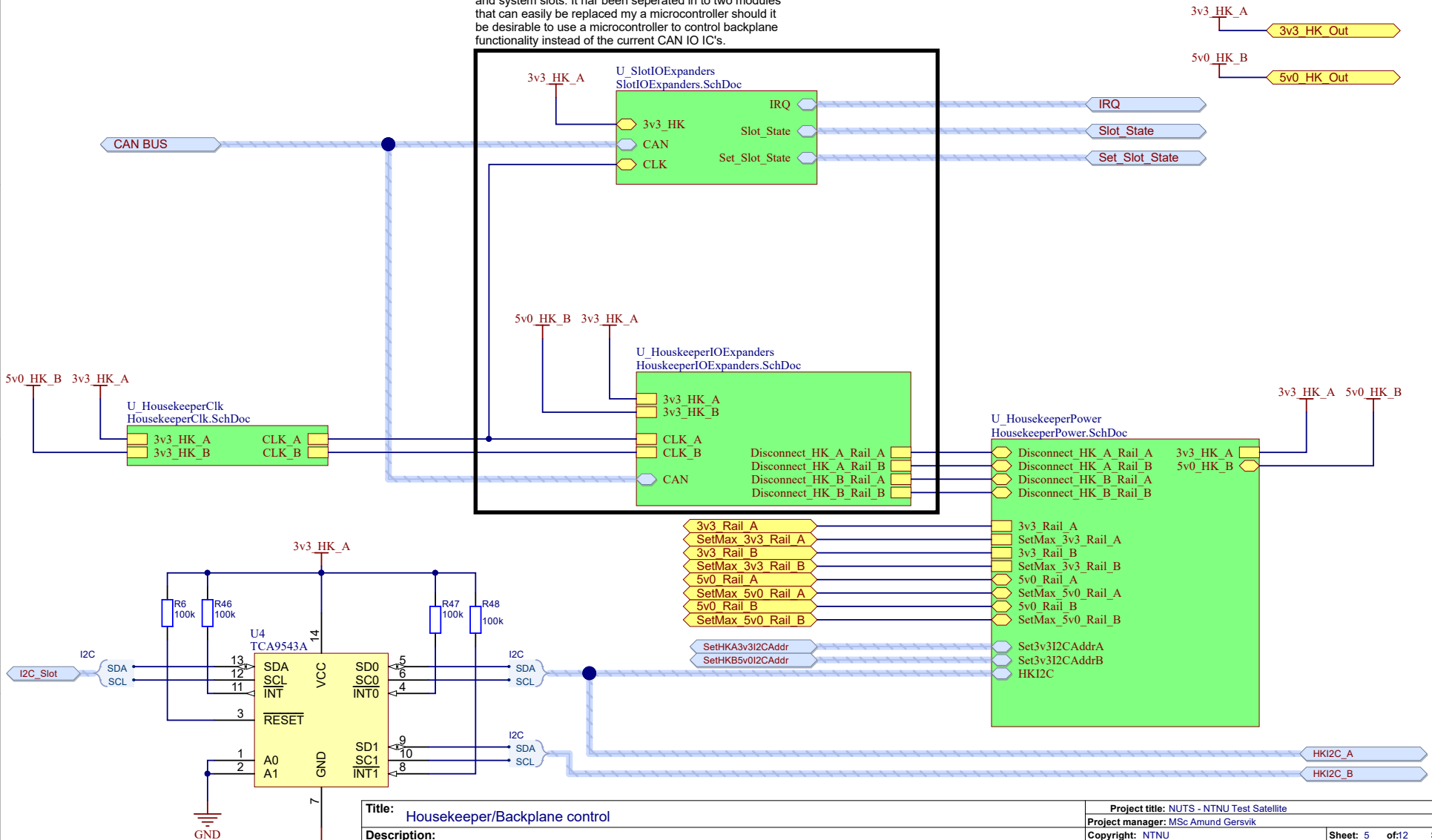
Title: Slot state holder and IRQ circuitry		Project title: NUTS - NTNU Test Satellite	
Description:		Project manager: MSc Amund Gersvik	
Last revision by: Stian H. Haug <stiahau@stud.ntnu.no>		Copyright: NTNU	Sheet: 3 of 12 Size: A4
Designed by: Stian H. Haug <stiahau@stud.ntnu.no>		License: Creative commons - CC BY 3.0	Version: 5. Not in version control
Design file share: //felles.ansatt.ntnu.no/time/iet/Prototypelab		Org. unit: Electronic and Prototype Laboratory	Date: 18.07.2016 Time: 18:14:41
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Design checked by: Unchecked		Department of Electronics and Telecommunications	
Design supervisor: MSc Amund Gersvik			
Repository server: NA			



Title: Module slot bus control		Project title: NUTS - NTNU Test Satellite	
Description: Isolation and buffer circuitry on the different signals going to and from a module.		Project manager: MSc Amund Gersvik	
Last revision by: Stian H. Haug<stiahau@stud.ntnu.no>		Copyright: NTNU	Sheet: 4 of 12 Size: A4
Designed by: Stian H. Haug<stiahau@stud.ntnu.no>		License: Creative commons - CC BY 3.0	Version: 5. Not in version control
Design file share: NA		Org. unit: Electronic and Prototype Laboratory	Date: 18.07.2016 Time: 18:14:41
Schematic filename: D:\Dropbox\Private\NTNU\Masteroppgave\Altium Projects\SlotBuscontrol_SchDoc		Norwegian University of Science and Technology Dep. of Electronics and Telecommunications O.S. Bragstads Plass 2A NO-7491 TRONDHEIM - NORWAY www.iet.ntnu.no	
Design checked by: Unchecked		Repository server: NA	
Design supervisor: MSc Amund Gersvik		NTNU Department of Electronics and Telecommunications	

Backplane housekeeping control logic

The marked area contains the control logic for backplane and system slots. It has been separated in to two modules that can easily be replaced by a microcontroller should it be desirable to use a microcontroller to control backplane functionality instead of the current CAN IO IC's.



Title: Housekeeper/Backplane control

Description:

Housekeeper control logic, powersupply and I2C bus multiplexer.

Last revision by: Stian H. Haug<stiahau@stud.ntnu.no>

Designed by: Stian H. Haug<stiahau@stud.ntnu.no>

Design file share: NA

Schematic filename: D:\Dropbox\Private\NTNU\Masteroppgave\Altium Projects\Housekeeper.SchDoc

Design checked by: Unchecked

Design supervisor: MSc Amund Gersvik

Repository server: NA

Project title: NUTS - NTNU Test Satellite

Project manager: MSc Amund Gersvik

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Dep. of Electronics and Telecommunications

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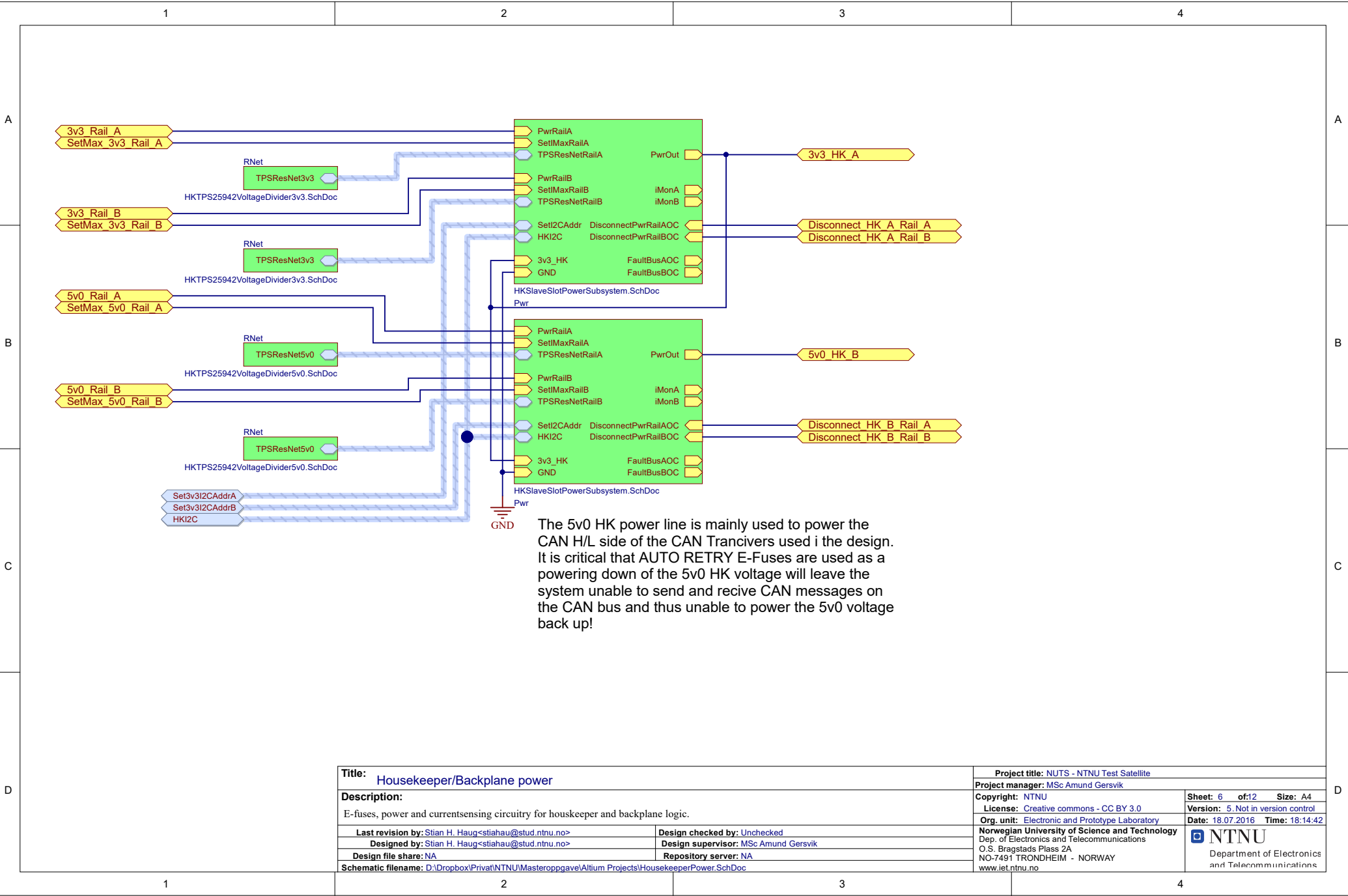
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Version: 5. Not in version control

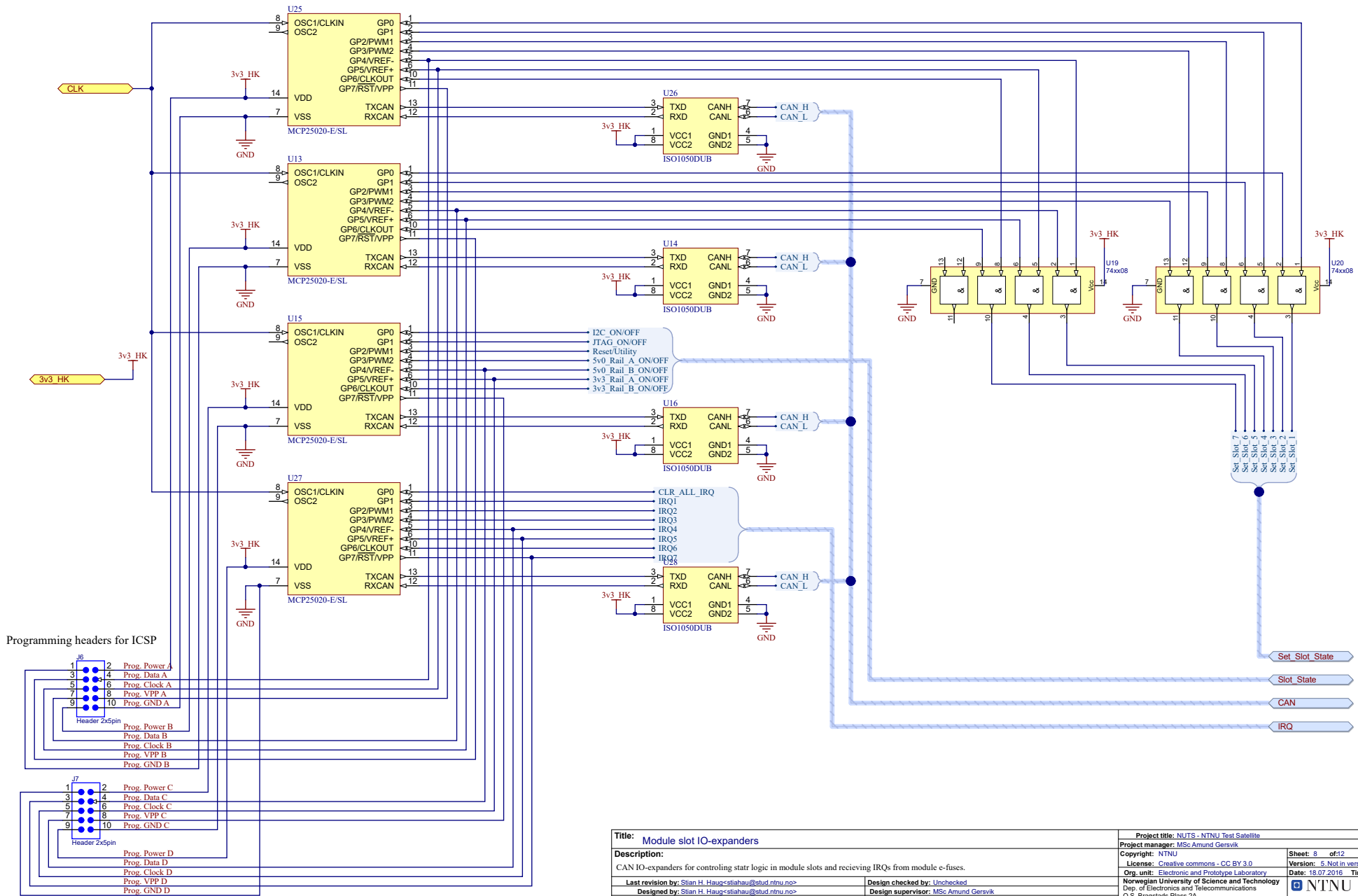
Date: 18.07.2016 Time: 18:14:41

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Title: Housekeeper/Backplane power		Project title: NUTS - NTNU Test Satellite	
Description: E-fuses, power and currentsensing circuitry for houskeeper and backplane logic.		Project manager: MSc Amund Gersvik	
Last revision by: Stian H. Haug<stiahau@stud.ntnu.no>		Copyright: NTNU	Sheet: 6 of 12 Size: A4
Designed by: Stian H. Haug<stiahau@stud.ntnu.no>		License: Creative commons - CC BY 3.0	Version: 5. Not in version control
Design file share: NA		Org. unit: Electronic and Prototype Laboratory	Date: 18.07.2016 Time: 18:14:42
Schematic filename: D:\Dropbox\Private\NTNU\Masteroppgave\Altium Projects\HousekeeperPower.SchDoc		Norwegian University of Science and Technology Dep. of Electronics and Telecommunications O.S. Bragstads Plass 2A NO-7491 TRONDHEIM - NORWAY www.i.et.ntnu.no	
Design checked by: Unchecked		Repository server: NA	
Design supervisor: MSc Amund Gersvik		 NTNU Department of Electronics and Telecommunications	



Title: Module slot IO-expanders		Project title: NUTS - NTNU Test Satellite	
Description:		Project manager: MSc Amund Gersvik	
CAN IO-expanders for controlling start logic in module slots and receiving IRQs from module e-fuses.		Copyright: NTNU	
Last revision by: Sitan H. Haug-stalahau@stud.ntnu.no		License: Creative commons - CC BY 3.0	
Designed by: Sitan H. Haug-stalahau@stud.ntnu.no		Org. unit: Electronic and Prototype Laboratory	
Design file share: NA		Norwegian University of Science and Technology	
Schematic filename: D:\Dropbox\Private\NTNU\Masteroppgave\Allium Projects\SlotIOExpanders_SchDoc		Dep. of Electronics and Telecommunications	
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		Department of Electronics and Telecommunications	
		Sheet: 8 of 12 Size: A3	
		Version: 5. Not in version control	
		Date: 18.07.2016 Time: 18:14:42	

1

2

3

4

A

B

C

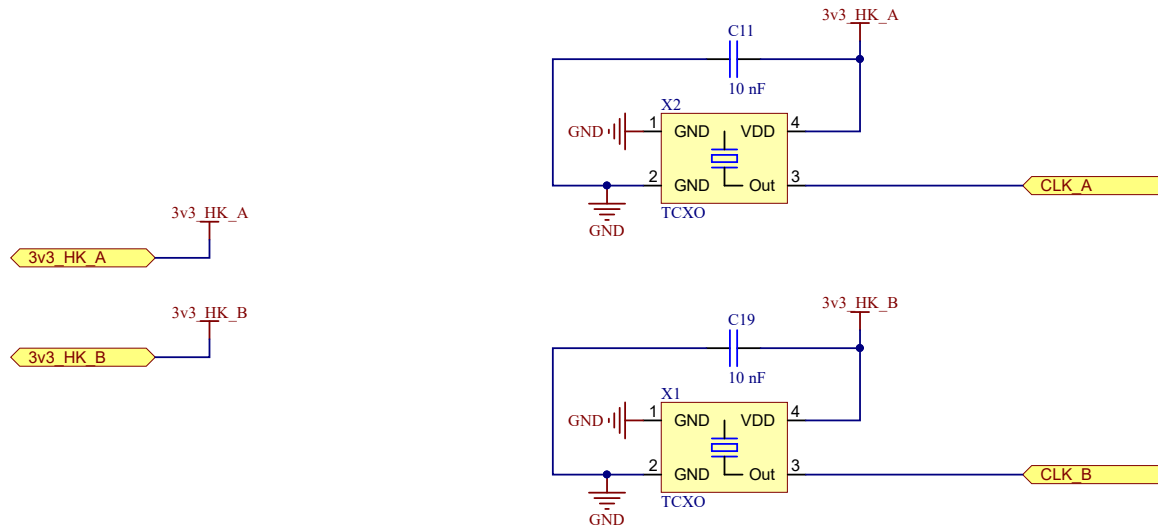
D


A

B

C

D



Title: Housekeeper clock sources		Project title: NUTS - NTNU Test Satellite	
Description: Clock sources providing clock to housekeeper logic.		Project manager: MSc Amund Gersvik	
Last revision by: Stian H. Haug<stiahau@stud.ntnu.no>		Copyright: NTNU	Sheet: 9 of 12 Size: A4
Designed by: Stian H. Haug<stiahau@stud.ntnu.no>		License: Creative commons - CC BY 3.0	Version: 5. Not in version control
Design file share: NA		Org. unit: Electronic and Prototype Laboratory	Date: 18.07.2016 Time: 18:14:42
Repository server: NA		Norwegian University of Science and Technology Dep. of Electronics and Telecommunications O.S. Bragstads Plass 2A NO-7491 TRONDHEIM - NORWAY www.i.et.ntnu.no	
Schematic filename: D:\Dropbox\Privat\NTNU\Masteroppgave\Altium Projects\Housekeeper\Clk_SchDoc		 Department of Electronics and Telecommunications	

1

2

3

4

1

2

3

4

Fault isolation line

Any signal crossing this line needs to be individually and thoroughly checked for proper fault isolation

A

A

B

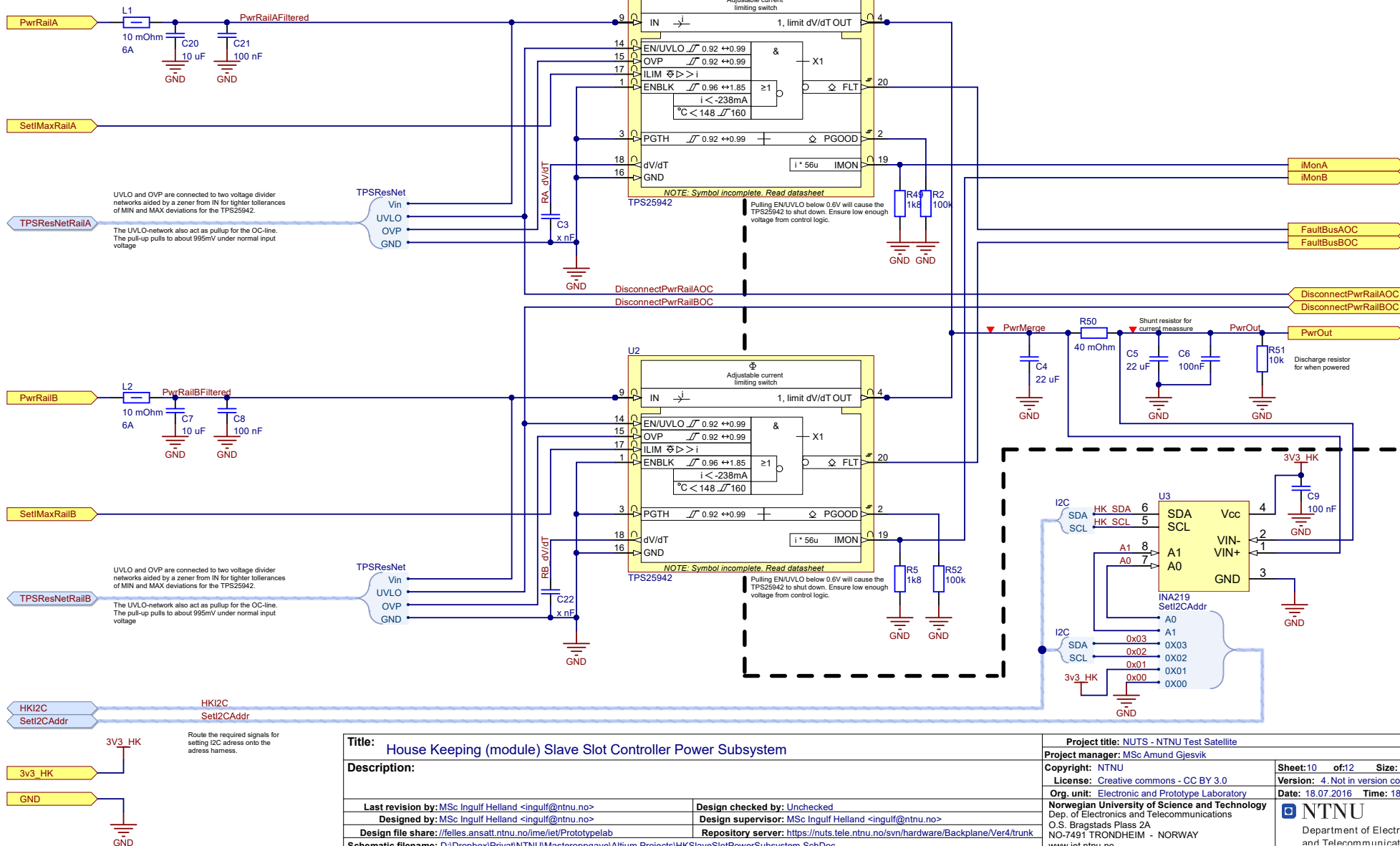
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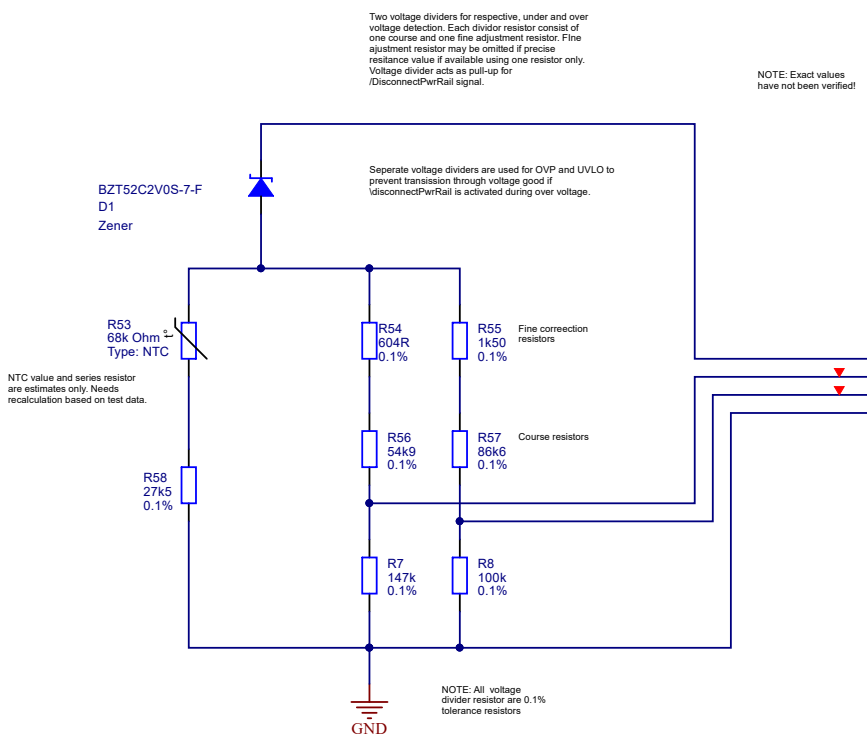
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D

D



Title: TPS25942-voltage divider for 3v3		Project title: NUTS - NTNU Test Satellite	
Description:		Project manager: MSc Amund Gersvik	
Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>		Copyright: NTNU	Sheet: 11 of: 12 Size: A4
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>		License: Creative commons - CC BY 3.0	Version: 4. Not in version control
Design file share: //felles.ansatt.ntnu.no/time/iet/Prototypelab		Org. unit: Electronic and Prototype Laboratory	Date: 18.07.2016 Time: 18:14:42
Schematic filename: D:\Dropbox\Privat\NTNU\Masteroppgave\Altium Projects\HKTPS25942VoltageDivider3v3.SchDoc		Norwegian University of Science and Technology Dep. of Electronics and Telecommunications O.S. Bragstads Plass 2A NO-7491 TRONDHEIM - NORWAY www.iet.ntnu.no	
		 NTNU Department of Electronics and Telecommunications	



Title: TPS25942-voltage divider for 3v3		Project title: NUTS - NTNU Test Satellite	
Description:		Project manager: MSc Amund Gersvik	
Last revision by: MSc Ingulf Helland <ingulf@ntnu.no>		Copyright: NTNU	Sheet: 12 of: 12 Size: A4
Designed by: MSc Ingulf Helland <ingulf@ntnu.no>		License: Creative commons - CC BY 3.0	Version: 4. Not in version control
Design file share: //felles.ansatt.ntnu.no/time/iet/Prototypelab		Org. unit: Electronic and Prototype Laboratory	Date: 18.07.2016 Time: 18:14:42
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