NTNU – Trondheim
Norwegian University of
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Fabricating Si[111] Nanostructures on Graphene by Aluminum-Induced Crystallization for High Yield Vertical III-V Semiconductor Nanowire Growth

Ida Marie Høiaas

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Supervisor: Helge Weman, IET
Co-supervisor: Dong-Chul Kim, CrayoNano

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Abstract

III-V semiconductor nanowire-graphene photovoltaics is an emerging technology that has the potential of highly efficient, flexible and ultra-thin solar cells. This thesis has explored aluminum-induced crystallization(AIC) of amorphous silicon on graphene and graphite surfaces, with the aim of increasing the nucleation yield of nanowires. It is demonstrated that thin films of aluminum and amorphous silicon, separated by an oxide membrane, produces [111]-oriented crystalline silicon after annealing at 470-500°C, well below the crystallization temperature of silicon, for glass, kish graphite and graphene substrates. The crystal orientation and elemental composition of the samples are characterized by X-ray diffraction(XRD), electron backscatter diffraction(EBSD) and energy-dispersive X-ray spectroscopy(EDX). The crystallized silicon forms semi-continuous films on glass and graphene, while it forms dendrite structures on kish graphite substrates. Silicon crystallization is achieved with both sputtering and electron beam evaporation of aluminum, and it is suggested that the aluminum microstructure is the determining factor for whether silicon crystallization occurs or not. The developed process for AIC of amorphous silicon is combined with the one-shot exposure electron beam lithography(EBL) technique to pattern silicon nanodot arrays on few-layer graphene substrates, showing high yields and controllable dot diameter sizes of 80-160 nm. The processes developed in this thesis would have a high potential for the high-density nucleation of vertically aligned, self-catalyzed gallium arsenide(GaAs) nanowires on graphene, enabling the fabrication of an ultra-thin solar cell with GaAs nanowires as the photoactive component and graphene as the bottom electrode.

II

Sammendrag

III-V halvledernanotråder på grafén er en ny teknologi som skaper et potensiale for fleksible og ultratynne solceller med høy virkningsgrad. Denne masteroppgaven har tatt for seg aluminium-indusert krystallisering(AIC) av amorft silisium på grafitt- og grafénoverflater, med mål å øke nukleeringstettheten av nanotråder. Ved bruk av tynnfilmer av aluminum og silisium separert av et oksidmembran, demonstreres krystallisering av [111]-orientert silisium ved 470-500°C, som er langt under krystalliseringstemperaturen til silisium. EDX, røntgen- og elektrondiffraksjon er brukt som karakteriseringsmetoder for AIC på glass-, grafén- og grafittsubstrater. Det krystalliserte silisiumet dannes i form av semikontinuerlige filmer på glass og grafén, men danner dendritter på grafittsubstrater. Krystallisering av silisum demonstreres med sputret og fordampet aluminium, og mikrostrukturen til aluminium foreslås som den avgjørende faktoren for om silisiumkrystallisering oppnås eller ikke. Prosessen som er utviklet kombineres med elektronstrålelitografi(EBL) til å deponere en matrise med silisiumsirkler på multilagsgrafén. Diameteren til silisumsirklene er kontrollerbar i området 80-160 nm. Prosessen som er utviklet muliggjør høyere tetthet av vertikale GaAs nanotråder på grafén, slik at ultratynne solceller med GaAs nanotråder som den fotoaktive komponenten og grafén som bunnelektrode kan fabrikeres.

IV

Preface and acknowledgements

The present work is a Master thesis in the Master of Science program in Nanotechnology with specialization in Nanoelectronics at the Norwegian University of Science and Technology(NTNU/NUTS). The thesis has been part of the work done by the nanowire group at the Department of Electronics and Telecommunications at NTNU, which is led by Professor Helge Weman and Professor Bjørn-Ove Fimland. The group is making efforts towards the development of nanowire devices, and this project was part of the group's goal to develop photovoltaics based on nanowires grown on graphene substrates. The work was carried out at the NTNU NanoLab, the IET XRD-lab and the IMT SEM-lab from January 20th 2014 to June 16th 2014.

First of all, I would like to thank my supervisor Prof. Helge Weman for giving me the opportunity to work on such an exiting project, and for valuable feedback throughout the semester.

I would also like to thank the staff and users of the NTNU NanoLab, whom have been of great help during my lab work and offered constructive discussions on research methods and procedures. I would especially like to thank Renato Bugge, for teaching me how to perform EDX measurements. Thank you Ingrid Hallsteinsen for patient help with the XRD start-up process, and being available at any hour of the day. I want to thank Min Zha, Jarle Hjelen and Yingda Yu for performing the EBSD measurements on thin films with me, something which was new to all of us.

Last, but not least, I would like to thank my co-supervisor Dr. Dong-Chul Kim, who more than anyone has taught me proficient and precise laboratory work habits. He had the main responsibility for learning me the skills necessary to undertake this project, and has also welcomed any questions I might have had, as well as providing constructive discussion of the results.

The graphene substrates grown on copper foil by chemical vapor deposition were provided by Keunsoo Kims group at Sejong University, Seoul, South-Korea, which also performed the Raman spectroscopy measurements.

Ida Marie Høiaas
NTNU, Trondheim
June 16, 2014

List of abbreviations

AFM	Atomic Force Microscope
AIC	Aluminum-Induced Crystallization
ALILE	Aluminum-Induced Layer Exchange
a-Si	Amorphous Silicon
BZ	Brillouin Zone
CVD	Chemical Vapor Deposition
EBL	Electron Beam Lithography
EBSD	Electron Backscatter Diffraction
EDX	Energy-Dispersive X-ray spectroscopy
ER	Electron Resist
e-beam	Electron Beam
FCC	Face-Centered Cubic
FWHM	Full Width at Half Maximum
GIXRD	Grazing Incidence X-ray Diffraction
IPA	Isopropanol
ITO	Indium Tin Oxide
KG	Kish Graphite
MBE	Molecular Beam Epitaxy
MIC	Metal-Induced Crystallization
MOCVD	Metal-Organic Chemical Vapor Deposition
NW	Nanowire
PLD	Pulsed Laser Deposition
PMMA	Poly Methyl Methacrylate
RHEED	Reflection High-Energy Electron Diffraction
RT	Room Temperature
RTP	Rapid Thermal Processing
sccm	standard cubic centimeters per minute
SEM	Scanning Electron Microscope
TCE	Transparent Conductive Electrode
TEC	Thermal Expansion Coefficient
TEM	Transmission Electron Microscope

UHV	Ultra-High Vacuum
WF	Write Field
XRD	X-ray Diffraction

Contents

Chapter 1

Introduction

Solar cells, also called photovoltaics, are an essential part of the transition from conventional to green energy sources that the world is experiencing today. Within the field of photovoltaics, the silicon solar cell is the most mature technology, and it constitutes most of the commercial market. However, several emerging technologies have the potential to surpass silicon solar cells in efficiency and lower the costs. These technologies hold the promise of ultra-thin and flexible solar cells, with excellent photoconversion properties, and are often based on novel materials and structures at the nanoscale. Two examples are organic solar cells that utilize fullerenes for carrier transport and quantum dot cells with tunable energy band gaps.

One emerging technology is the nanowire array solar cell. The semiconductor wires have an absorption cross-section larger than their spatial extent, reducing the solar absorber material to a tenth of the equivalent bulk material[1]. The maximum efficiency achieved today with a nanowire array solar cell is 13.8%[2], and the maximum theoretical efficiency is 32 %[3][4][5]. A drawback with these structures is that they are normally grown on a thick semiconductor substrate. The growth of nanowire array solar cells on two-dimensional materials like graphene reduces the volume of the solar cell substantially and is a step towards ultra-thin and flexible devices. The most efficient nanowire-graphene solar cell to date has an efficiency of 2.51 %[6].

Graphene is the substrate of choice because of its excellent electronic, optical and mechanical properties. It is stable as a monolayer at ambient conditions, has a high electron mobility and a high transmittance, which means it can be used both as a bottom and top electrode[7]. Efforts have been made to fabricate

graphene at a large scale, and this has led to graphene being commercially available today[8]. Due to its lack of dangling bonds, it is difficult to grow thin films or bulk materials on graphene. However, if the structures are laterally confined, several materials can be epitaxially grown on graphene by quasi-van der Waals bonding[9]. The major challenges of growing vertical nanowires on graphene are low densities of nanowires[9][10], lack of vertical alignment[11][12][13] and parasitic semiconductor growth[14][15].

GaAs nanowire array solar cells on Si(111) substrates have been successfully fabricated in the NTNU NanoLab by S. Sandell[16]. This thesis has looked at the possibility of using [111]-oriented silicon nanostructures as nucleation sites for the growth of self-catalyzed vertical GaAs nanowires on graphene, to improve the yield of nanowires. The growth of nanowires on very thin films of Si[111] on amorphous SiO_2 substrates has been successfully achieved by Cohin et al.[17], suggesting that this method can be used with any substrate.

An additional advantage of using Si[111] nanostructures as nucleation sites for nanowires is that the growth conditions established for the growth of nanowires on silicon substrates can be used with the modified graphene substrates. One technique has been investigated in detail for this purpose; aluminum-induced crystallization(AIC) of silicon, while there has been done preliminary tests on the evaporation of silicon in a chemical vapor deposition(CVD) chamber. This is the first work done on silicon nanostructures in the nanowire research group at NTNU, and the thesis has therefore focused on establishing if the mentioned techniques are viable options to increase the nanowire yield on graphene. The main thesis questions are:

- Is it possible to fabricate Si[111] on graphene and/or graphitic surfaces?
- Can we precisely control the thickness, position and shape of the these structures, to accommodate to the NW array solar cell fabrication process?

Due to the molecular beam epitaxy(MBE) system at NTNU being rebuilt, no nanowires were grown during the spring of 2014. This thesis has therefore focused on optimizing a process for depositing Si[111] on graphene surfaces, and the study of the effect on nanowire yield must be done at a later point in time.

The thesis is divided in six chapters, and starts with a literature review in chapter two. The experimental methods and materials used in the laboratory work are described in chapter three, before the results and discussion sections in chapters four and five. Both chapter four and five are divided in two parts, the AIC process and patterning of silicon dot arrays. The preliminary experiments on the evaporation of silicon have been included in the appendix.

Chapter 2

Theory

In this chapter, literature reviews of the relevant fields are presented. First, the background and motivation for this thesis are elucidated through the description of nanowire photovoltaics. Thereafter, the properties of graphene are discussed as well as the prospect of nanowire growth on graphene. Then the principles of the metal-induced crystallization process are explained. Lastly, the electron-beam lithography process and the employed characterization methods are briefly discussed.

2.1 Nanowire solar cells

The basis for converting the energy of photons to electrical energy with any semiconducting material is the p-n junction. The junction is formed by the interface between regions of the same material with different dopants, namely electrons and holes. This is called n- and p-type doping, respectively, and is a form of controlled introduction of impurities. At the interface between the two regions, charge carriers diffuse and a depletion region is formed. The diffusion of charge carriers create ionized dopant atoms, and an electric field gradient that can separate photogenerated electron-hole pairs.

The properties of this junction can also be explained by looking at the energy diagrams of the respective regions. Introducing an excess of electrons to a semiconductor material will increase the Fermi energy level to right below the conduction band, while introducing an excess of holes will lower the Fermi energy level to right above the valence band. This is shown schematically in figure 2.1.

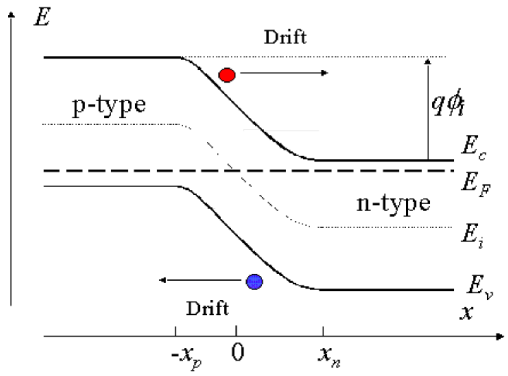

Figure 2.1: Energy diagram of a pn-junction in equilibrium, with electrons as red dots and holes as blue dots. The depletion region extends from $-x_p$ to x_n, and the conduction band(E_c), valence band(E_v) and fermi energies(E_F) are indicated. The built-in potential ϕ_i is equal to the work function difference between the n-type and p-type semiconductors. Illustration adapted from [18].

At the p-n junction, the Fermi levels will equalize in equilibrium, and the result is band bending of the conduction and valence bands. Due to this bending of the energy bands, holes and electrons generated by light are separated at the junction as it is energetically favorable for them to drift in opposite directions, giving rise to the photovoltaic effect.

2.1.1 The efficiency limits of single-junction solar cells

A theoretical limit for the efficiency of solar cells made of a single p-n junction was predicted by William Shockley and Hans J. Queisser in 1961[19]. They found that the maximum efficiency for a solar cell is 30% for a device with a band gap of 1.1 eV(silicon), when there is no radiative combination and the solar cell is under AM1.5 illumination. AM1.5 means that the air mass coefficient used for the solar spectrum is 1.5 times the atmosphere thickness, and this value is used for standard measurements. For a material with an optimal band gap of 1.4 eV the maximum efficiency would be 33%[20]. To find this limit, they stated some requirements for the device:

1. There are no losses, meaning that all recombination is radiative and the quantum efficiency QE = 1.

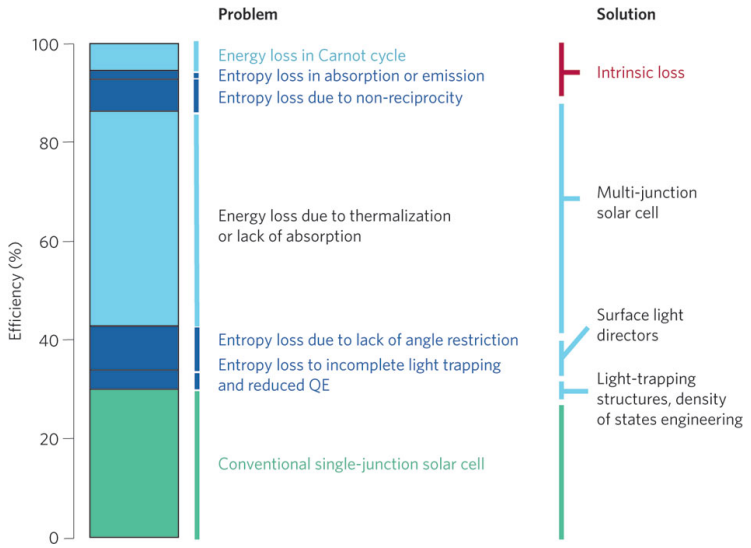

Figure 2.2: Efficiencies and losses for a solar cell. Dark blue indicates entropy-related losses while light blue indicates energy-related losses. Solutions to reducing the losses are listed to the right. Illustration from [20].

2. All photons with an energy above the semiconductor band gap are absorbed.

3. Each absorbed photon is converted to an electron-hole pair with a voltage equal to the bandgap.

The third requirement necessitates that an absorbed photon with an energy above the band gap energy E_g thermalizes via collisions until its energy is equal to E_g. Before thermalization it is what is called a hot carrier, meaning that the electron has a higher temperature than the crystal lattice around it. If the electron can be extracted before it thermalizes, the excess energy can be conserved, resulting in a higher open-circuit voltage, V_{OC}, for the solar cell. An advantage with nanowire solar cells is that these hot carriers can be extracted if the nanowire radius is smaller than the hot carrier diffusion length[21].

In a real solar cell, there are other loss mechanisms that also must be considered. Figure 2.2 shows various efficiency limits of solar cells and the associated losses, which can be studied by an expression for V_{OC}[20]:

$$qV_{OC} = E_g(1 - \frac{T}{T_{sun}}) - kT[\ln(\frac{\Omega_{emit}}{\Omega_{sun}}) + \ln(\frac{4n^2}{I}) - \ln QE] \tag{2.1}$$

The first term represents fundamental thermodynamic losses based on Carnot's theorem where E_g is the bandgap energy, T is the solar cell temperature and T_{sun} is the temperature on the surface of the sun. This term reduces V_{OC} with minimum 5%[20]. The three terms in the square brackets account for entropy related terms. The first reflects entropy increase as a result of the solid angle Ω_{emit} of spontaneous emission deviating from the solid angle of solar radiation Ω_{sun}. The corresponding loss for V_{OC} can be as large as 315 mV, and it is evident that photonic structures designed to have limited angles of radiative emission will reduce this loss. The second term in the square brackets, $\ln(4n^2/I)$, represents losses due to incomplete light trapping inside the solar cell. n is the refractive index of the solar absorber, and I is the light concentration factor. For a planar cell with no light trapping, this loss corresponds to a reduction of V_{OC} of 100 mV[20]. The last term is related to the electronic material properties, and describes the loss in V_{OC} due to non-radiative recombination caused by defects and impurities. QE is the quantum efficiency of the cell and is defined by

$$QE = \frac{R_{rad}}{R_{rad} + R_{nrad}} \tag{2.2}$$

where R_{rad} and R_{nrad} are the radiative and non-radiative recombination rates. The less-than ideal QE typically leads to a reduction of V_{OC} of about 60 mV[20].

There are three types of recombination; radiative recombination, Auger recombination and Shockley-Read-Hall recombination. Radiative recombination is the emittance of a photon as a result of an electron in the conduction band recombining with a hole in the valence band, and is most significant in direct band gap materials. Auger recombination is a form of non-radiative recombination which involves two electrons in the conduction band and one hole in the valence band. When one electron and one hole recombines, the released energy is transferred to a second electron in the conduction band. The released energy is normally lost due to the thermalization of the excited electron. As Auger recombination requires the interaction of several excited carriers, it is most prominent in highly doped materials. The second form of non-radiative recombination is Shockley-Read-Hall recombination. It is a recombination route enabled by the presence of impurities, which can function as energy traps and recombination centers in the band gap. The first two recombination types are intrinsic to the material, while the third is a result of material quality.

The three entropy related loss terms in equation 2.1 can all be reduced by material and structural improvements, and this is part of the reason why nanowire solar cells show great potential in improving existing photovoltaic technology. The second entropy term, $\ln(4n^2/I)$, is limited by $I \leq 4n^2$ in classical ray optics. This limit has been exceeded by recent advances in nanostructuring of solar cell surfaces[22][23] and demonstrates the potential of breaking the Shockley-Queisser efficiency limit. Krogstrup et al. showed that a single GaAs nanowire had a solar conversion efficiency of 40%[1], due to its absorption cross-section being larger than its physical dimensions.

In semiconductor nanowires, both Auger and Shockley-Read-Hall recombination can be reduced by reducing the distance to the pn-junction. However, nanowires have an increased surface to bulk ratio. A larger surface area increases the number of trapping states at the surface of the nanowire, leading to surface recombination[24].

2.1.2 Nanowire solar cell design

Optical nanostructures can change the reflection, scattering and absorption of a material. Radial junction nanowires combine a long absorption length with a short carrier diffusion length, making it an interesting design for optimizing photo-conversion efficiency. The doping of nanowires can be controlled during synthesis[25], and this is further explained in section 2.1.3.

There are two main types of p-n junctions in semiconductor nanowires; radial and axial junction. For the radial junction, a junction is formed along the length of the nanowire radially, and this design is often referred to as core-shell nanowires as shown in the cross-section in figure 2.3b). The axial junction has a junction orthogonal to the length of the wire, reducing the junction area compared with the radial nanowires. This is shown schematically in figure 2.3a). Nanowires with a radial p-n junction are generally more efficient than their axial junction counterpart, as the axial junction nanowires have higher probabilities for surface recombination[26].

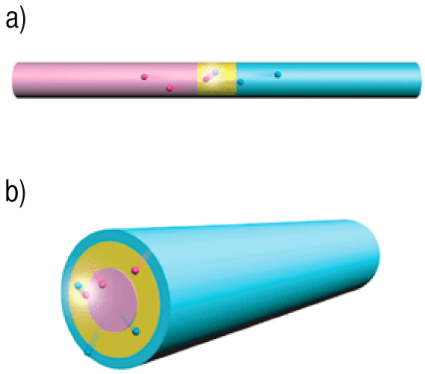

Figure 2.3: The two most common p-i-n junctions in nanowire solar cells: a) Axial junction and b) radial junction. An intrinsic layer, which is yellow, is inserted between the p- and n-doped regions which are pink and blue. Illustration from [25].

Arrays of nanowires have both excellent antireflective and light-trapping properties[27][28]. Ordered arrays have been found to have higher absorptions than randomly oriented arrays, as the latter has a stronger tendency to scatter light out of the top of the structure[29]. Nanowires have an absorption cross-section that is larger than their diameter[1], so a reduced area coverage does not decrease the efficiency of the solar cell.

2.1.3 Gallium arsenide nanowire growth by molecular beam epitaxy

The vapor-liquid-solid(VLS) technique by MBE is the growth method used to grow nanowires at NTNU. It offers precise control of stochiometry and deposition rate of materials, but is not scalable. What separates MBE from other vapor-phase epitaxy techniques is that it occurs by molecular flow, in contrast to viscous flow, something which can only be achieved under ultra-high vacuum(UHV). Viscous flow means that molecules collide and interact before arriving at the substrate, but with molecular flow there are no chemical reactions between molecules during deposition[30, p 74].

MBE is a thermally controlled evaporation process, where target elements are heated in crucibles known as Knudsen cells to create molecular beams. The

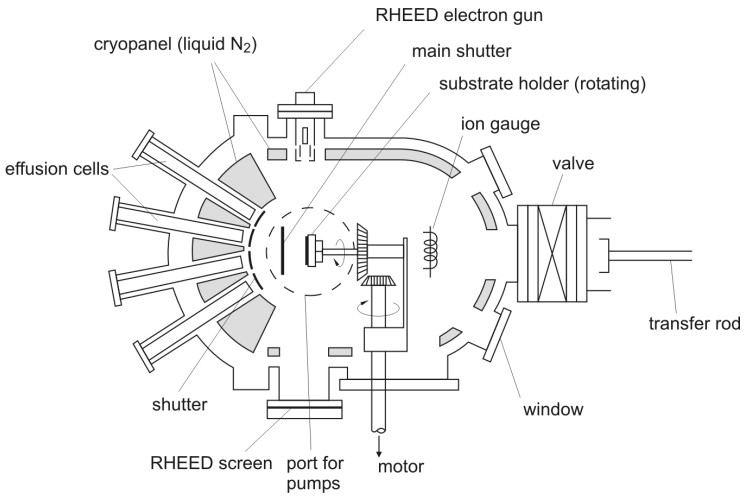

Figure 2.4: A schematic view of a typical MBE setup. A loading valve is used to introduce the sample without losing vacuum. The different materials are deposited by molecular beams formed from heating the effusion cells. The sample is mounted on a rotating stage with a temperature controller. Shutters enable atomic layer control over the growth process, and a RHEED gun and detector are used to control the composition of the deposited film. An ion gauge monitors the ultra-high vacuum, while liquid nitrogen cryopanels are used to reduce the vapor pressure of water and other contaminants. Illustration from [31].

molecular beams are then directed onto a heated substrate. The growth rate in an MBE chamber is slow, about one atomic layer per second[30, p 74], and this enables the formation of very abrupt interfaces, as the deposition composition can be altered across one atomic layer. The development of the deposited film can be monitored by a reflection high-energy electron diffraction(RHEED) gun and a detector. Electrons are incident on the film surface at a glancing angle, and the diffraction pattern at the detector is a result of the crystalline composition of the sample surface. It is also common to use a mass spectrometer to monitor the flux of the various materials, which again determines the evaporation temperature[30, p 75]. An example of a MBE setup is shown in figure 2.4.

The absorption of a specific material on the sample surface is governed by kinetics, and is therefore material dependent. For vertical GaAs nanowires, growth can be initialized either by a metal precursor or by self-catalyzation. The difference is whether a metal or gallium droplet is used to initiate the growth of the wires. For the process using self-catalyzed growth of radial junction nanowires on silicon substrates, which is the method applied at NTNU, the growth occurs as follows[32]:

1. Gallium is first introduced in the chamber at 630°C, a temperature used for all steps. Self-assembly occurs at the substrate and liquid gallium droplets are formed, during the course of about 1 minute and with a Ga deposition rate of 0.5-1 ML/s.

2. When the liquid gallium droplets have formed, arsenic, in the form of As_2 or As_4 is introduced in the chamber at a flux of about $5 * 10^{-6}$ Torr. A p-dopant is also introduced, and the three species; Ga, As_x, and the p-dopant solidify underneath the gallium droplet. The length of this process step decides the length and diameter of the p-doped region of the nanowires, as both are linear with time.

3. A n-dopant is introduced, to form a n-region GaAs shell over the p-region. The length of this process step decides the length and diameter of the n-doped region of the nanowires, as both are linear with time.

4. A passivation layer made up of AlGaAs is grown to suppress the surface states, by introducing aluminum.

5. At this point, there is still a gallium droplet at the top of the wire. This droplet is solidified by only supplying arsenic at a flux of $9 * 10^{-6}$ Torr for ten minutes.

6. An additional layer of AlGaAs of a thickness of about ∼25 nm is grown.

7. Finally, a 5 nm thick GaAs cap layer is grown which prevents the oxidation of AlGaAs.

The resulting nanowires have diameters on the order of a few hundred nanometers and lengths of a few microns. The final shape and density of nanowires are highly dependent on process parameters like temperature, material flux and deposition time. The parameters mentioned in this section are parameters optimized for the growth of GaAs nanowires on a Si(111) substrate, and will vary with other substrates or different nanowire compositions.

2.2 Graphene

Graphene is a one atom thick layer of carbon atoms in a honeycomb, or hexagonal, lattice. It is one of few two-dimensional(2D) materials known to exist, and can be used as a building block for three-dimensional(3D) graphitic materials, as shown in figure 2.5. The discovery of graphene earned the nobel prize in 2010[33], when Andre Geim and Kostya Novoselov verified it's existence through the physical exfoliation method.

The electronic properties of graphene change towards 3D behavior with an increasing number of layers, and it has been shown[35] that at about ten layers it exhibits close to the electronic properties of graphite. Therefore, structures of more than ten(10) layers of graphene are considered as thin films of graphite, while graphene is divided into single-, double- and few- (three to ten) layer graphene, all of which exhibit different crystal structures and electronic properties. Nearly completely transparent and highly flexible, graphene can be used both as a top- or bottom-contact in solar cells. Epitaxial growth by chemical vapor deposition is the most promising technique to ensure large area, single-layer graphene. It has been shown that graphene can be grown in this fashion on metal catalysts such as Ni[36] and Cu[37] substrates, and subsequently transferred to arbitrary substrates[38].

2.2.1 Electronic properties

The electronic landscape of graphene enables charge carriers to travel several thousands interatomic distances without scattering. For single-layer graphene, charge carrier mobilities have been found to exceed 15 000 $cm^2V^{-1}s^{-1}$ under ambient conditions[39][40].

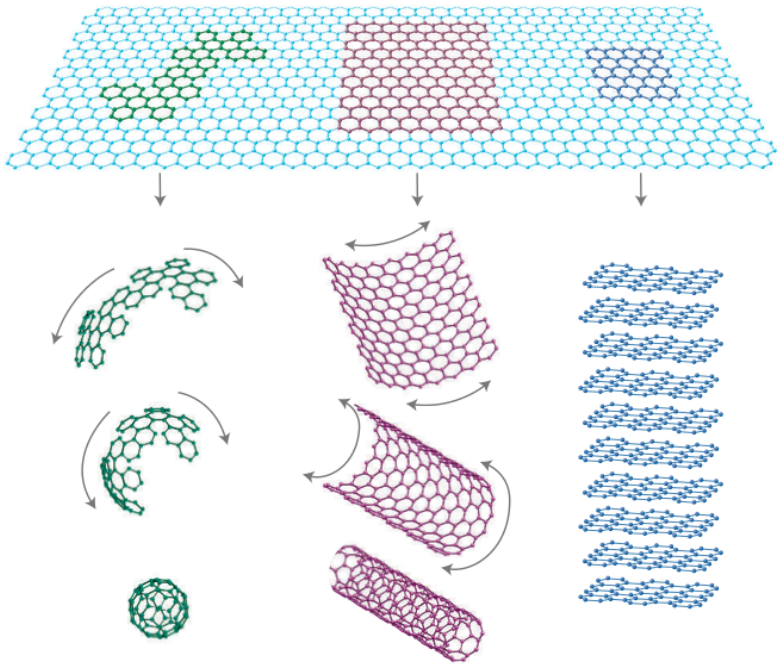

Figure 2.5: The two-dimensional graphene layer can be used as building blocks for other-dimensional structures. Here, graphene is wrapped up to a zero-dimensional buckyball, a one-dimensional carbon nanotube and three-dimensional graphite. Illustration adapted from [34].

The C-C binding in graphene consists of the hybridization of one s orbital and two p orbitals, and is thus named sp^2 hybridization, with a bond length of 1.42 Å. The s and two p orbitals of adjacent carbon atoms overlap, and form a strong σ bond which accounts for the structural stability of graphene. The remaining p-orbital however, which is perpendicular to the planar structure formed by the σ bonds, does not directly overlap with adjacent orbitals and can form a covalent π band. This band is half filled as there is one electron in each p orbital. The electronic properties of graphene are determined by the delocalized electrons in the π band[41].

The electric field effect describes how the conductance of a material is altered by the application of an external field. This effect is used in several semiconductor devices, like the field-effect transistors(FETs), and the Schottky diode. The electric field effect is not observable in metals, as the electric field is screened at distances below 1 nanometer[42]. The effect was observed in few-layer graphene[42] in 2004, and is one of the main reasons for graphene's potential in electronic applications.

To explain the electric field effect in graphene, it is necessary to look at the electronic band structure of graphene. The crystal structure of graphene is defined by the translational vectors

$$\vec{a_1} = a_0(\frac{3}{2}, \frac{\sqrt{3}}{2}), \vec{a_2} = a_0(\frac{3}{2}, -\frac{\sqrt{3}}{2}) \tag{2.3}$$

where a_0 is the nearest neighbor distance of 0.142 nm. The corresponding reciprocal lattice is spanned by the vectors

$$\vec{b_1} = \frac{2\pi}{a_0}(\frac{1}{3}, \frac{1}{\sqrt{3}}), \vec{b_2} = \frac{2\pi}{a_0}(\frac{1}{3}, -\frac{1}{\sqrt{3}}) \tag{2.4}$$

as shown figure 2.6. Also shown in the figure is the Brillouin zone(BZ), which is the unit cell of the reciprocal lattice and represents inequivalent points in reciprocal space. Using high symmetry points in the BZ, one can map the electronic band structure as seen in figure 2.7. The valence and conduction bands overlap at the corners of the Brillouin zone, the K points.

The linear dispersion at the K points is the reason why graphene is often referred to as a zero-gap semiconductor, where low-E quasiparticles called massless Dirac fermions are used to describe the electrons' interaction with the periodic potential of the honeycomb lattice[34].

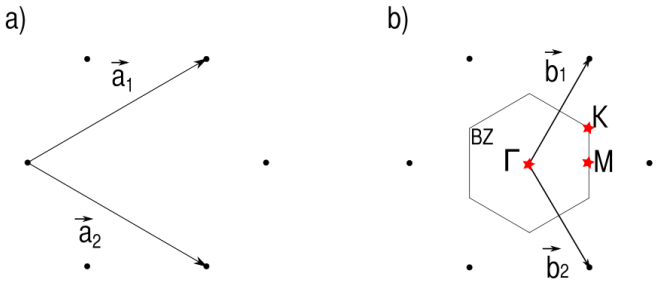

Figure 2.6: The a) lattice vectors and b) reciprocal lattice vectors of graphene. High symmetry points are indicated as stars.

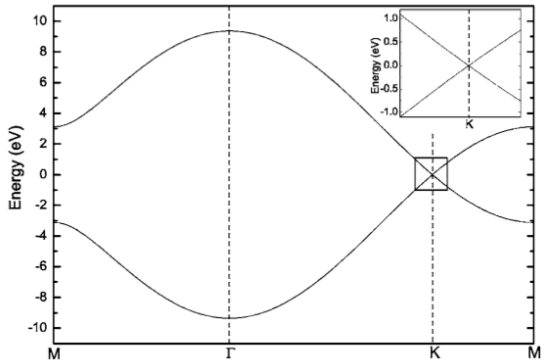

Figure 2.7: The band diagram of graphene. Illustration from [35].

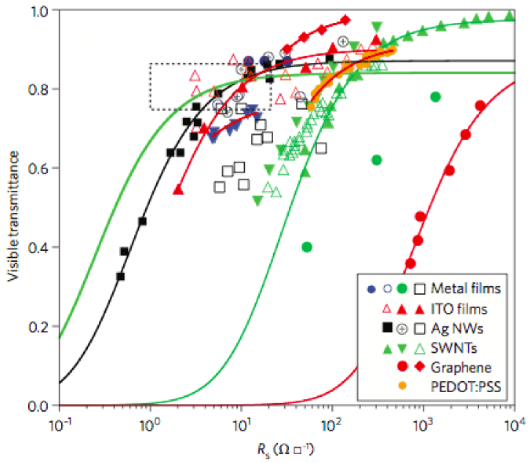

Figure 2.8: Comparison of the transmittance as a function of sheet resistance for different materials used as TCEs, measured at $\lambda = 550$ nm. The dotted rectangle marks the target region for TCE application. Illustration from [7].

2.2.2 Optical and mechanical properties

The low carrier concentration of graphene, $\sim 10^{12}/cm^2$ corresponding to $\sim 10^{20}/cm^3$ in a three-dimensional structure[43], is what causes the high transmittance of light. A high plasma edge wavelength, λ_p, is also key to good transmitting properties as this wavelength is the upper limit of the spectral range. For graphene, $\lambda_p > 1\ \mu m$, which is higher than for example oxide transparent conductive materials with $\lambda_p \sim 1\ \mu m$[7]. The transmittance of graphene has been demonstrated to be as high as 97.5%[44]. The sheet resistance of undoped graphene is higher than other transparent electrodes at $\sim 6\ k\Omega\square^{-1}$[7], but due to natural doping by defects the sheet resistance is normally in the tens of $\Omega\square^{-1}$ range, and thus comparable to state of the art transparent electrodes like ITO[7]. A comparison between different transparent conductive electrodes(TCEs) is shown in figure 2.8, plotting the transmittance at $\lambda = 550$ nm as a function of sheet resistance. ITO, graphene and Ag grids are the materials that best fit the target application(the dashed rectangle).

The breaking strength of graphene has been measured to $42Nm^{-1}$[45], which is comparable to that of diamond, and the Young's modulus to 1.0 terapascals[45],

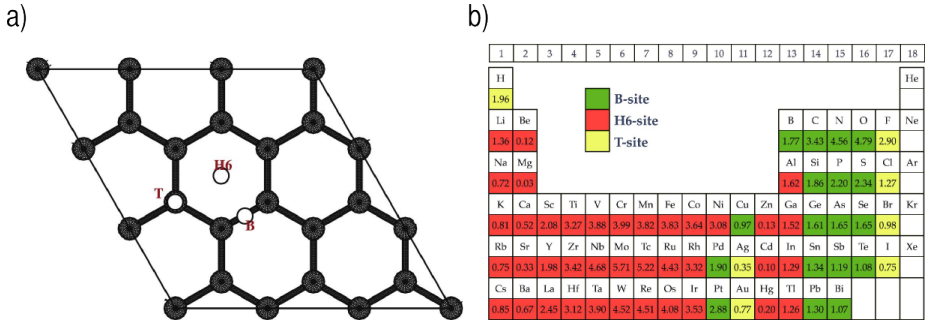

Figure 2.9: Absorption sites and binding energies for adatoms on graphene. a) The three different binding sites T, B and H6. b) The bond energy at the most stable binding site upon the adsorption of an adatom on graphene[47].

which is equal to that of bulk graphite[46]. The high breaking strength is due to the C-C bond.

2.2.3 Epitaxial growth of III-IV nanowires on graphene

Most materials have a low adhesion on graphene due to graphene's lack of dangling bonds. The bondings of materials on graphene are not fully understood, but there is ongoing research to determine the mechanisms of these bondings. Nakada and Ishii described three possible adsorption sites for adatoms on graphene; the B, T and H6-sites as shown in figure 2.9a)[47]. They also calculated the binding and migration energies of all elements, and the binding energy is shown in figure 2.9b). The calculated energies give an indication of what crystal structures might arise from the adsorption of different elements on graphene. Nakada and Ishii also predicted that adsorption at less stable sites might disturb the structure of graphene.

Weman et al. looked at the epitaxial growth of semiconductor nanowires on graphene and graphitic surfaces[9]. A higher lattice mismatch can be accommodated with nanowire growth compared to bulk growth, so by using this type of nanostructuring they could grow materials on graphene that can not be grown epitaxially in bulk form. A quasi-van der Waals binding mechanism was suggested, which is a form of 3D-2D heteroepitaxy. The growth of GaAs nanowires on graphene was demonstrated, and the nanowires were found to grow in the [111]-direction. However, low yields or parasitic crystal formation occured at

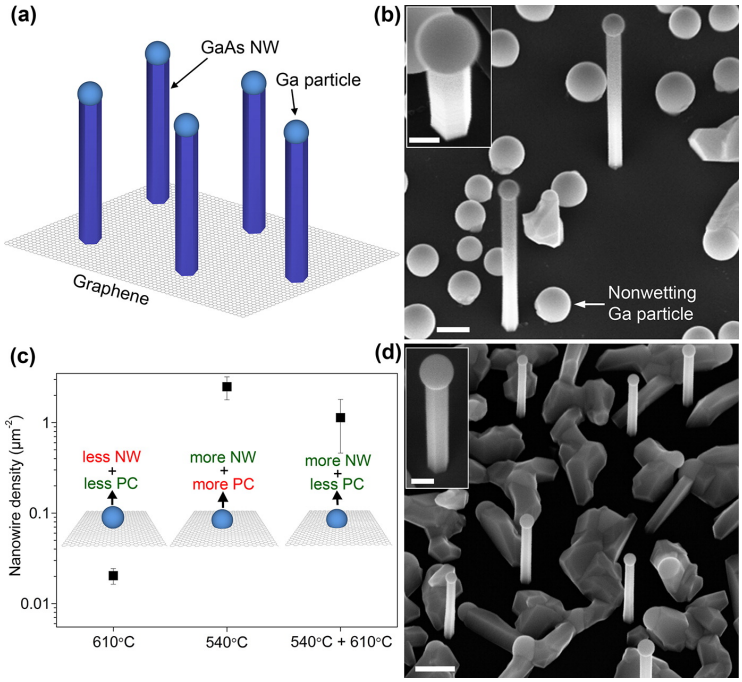

Figure 2.10: GaAs nanowires grown on graphene. a) is a schematic of the components, b) and d) are SEM images of nanowires grown on high and low+high temperatures, respectively. c) explains the dependency of formation of nanowires and parasitic crystals(PC) on growth conditions. The scale bars are 200 nm in the large images and 100 nm in the insets. Images from [9].

high and low MBE growth temperatures, as shown in figure 2.10. What enabled the growth of NWs on graphene was the implementation of a two-temperature growth sequence by MBE, were the nanowires were nucleated at 540°C, and subsequently grown at 610°C.

The efficiency record for nanowire-graphene photovoltaics is held by Mohseni et. al., at 2.51%[6]. They have grown InGaAs nanowires on four-layer CVD graphene by a seed-free metal-organic chemical vapor deposition(MOCVD) process. Their results show that the nanowires are vertically aligned, but with varying densities and there is two-dimensional growth in the form on InAs islands. They call the growth mechanism van der Waals epitaxial self-assembly

of nanowires.

2.3 Si[111] by metal induced crystallization

Metal-induced crystallization (MIC) is a technique where amorphous silicon (a-Si) is crystallized at a low temperature[48][49]. A metal-semiconductor contact allows for a migration path for the amorphous silicon through the metal, where it rearranges as a polycrystalline film. The annealing temperature required for crystallization of the amorphous silicon has been found to be significantly lower than for non-metal-induced crystallization at 850-1000°C[50]. The main principles are shown in figure 2.11a).

2.3.1 Mechanism

There are two different mechanisms that can crystallize the silicon. Some metals form eutectics with Si and follow the layer exchange mechanism. Other metals react with the amorphous silicon and form silicides[51, p 461].

The layer exchange mechanism of MIC has been studied with in-situ transmission electron microscopy(TEM), showing that the metal phase provides nucleation sites for the crystalline Si and acts as a transport medium for the Si layer[52]. Diffraction and spectroscopy investigations have revealed that the Si crystallizes either in the [001]- or [111]-direction with respect to the substrate surface[17][53][54], making this technique interesting for the epitaxial growth of semiconducting nanowires.

The reaction starts in the metal layer, followed by the splitting and migration of metal grains through the amorphous silicon[52]. As the metal grains migrate, the semiconductor atoms diffuse through the metal[55], and the resulting supersaturation of Si in Al is relieved through the nucleation and growth of crystalline Si[56][57]. The migration of the metal phase is achieved by the diffusion of semiconductor atoms as well as the diffusion of metal atoms within the metal grains. It has been suggested that this diffusion mechanism provides the fastest reaction path for the system to reduce its excess free energy at temperatures lower than the eutectic temperature[52][51, p 461]. The energy released locally during crystallization results in a temperature field gradient, which is the reason for the fractal formation of silicon[51, p 463]. Polycrystalline films with monocrystalline individual grains can be achieved by MIC[17].

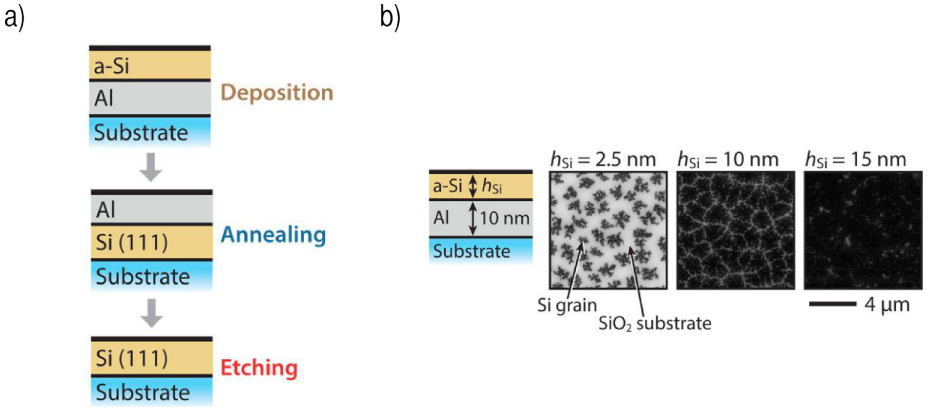

Figure 2.11: The sequence of metal-induced crystallization is shown in a), while SEM images of the polycrystalline Si layer are shown in b), with the Al/a-Si ratio indicated. Illustrations from [17].

2.3.2 Aluminum-induced crystallization

It has been shown that a-Si can crystallize in contact with several metals, like Au, Al, Ag and Ni[52]. Aluminum provides the lowest induced-crystallization temperature, which varies between different reports but has been found to be as low as 150°C[58], compared with an eutectic temperature of 577°C[52]. Thin films of Al and Si have been grown on glass substrates, showing crystalline Si grown from a-Si films as thin as 2.5 nm[17]. The crystalline Si films grown by AIC are believed to be p-type due to doping by Al during the crystallization process[59]. The crystallization process takes between 30 and 45 min at 500°C when the silicon is deposited directly on top of the aluminum, and the time needed for complete crystallization increases as the temperature is lowered[58]. During the crystallization the layers also switch positions, leading to some calling this process aluminum-induced layer exchange(ALILE).

A semipermeable membrane can be formed by oxidizing the aluminum[60] or depositing SiO_2[61] before the deposition of silicon. The thicker the membrane, the slower the subsequent crystallization of Si. Doherty and Davis have shown that aluminum oxide formed on crystalline aluminum tends to form in alignment with the metal at temperatures above approximately 500°C[60]. Jeurgens et al. argues that the oxide layer forms into crystalline γ-Al_2O_3 in alignment with the metal crystal orientation at temperatures above 300°C[62].

Cohin et al. have investigated how thin the Al and a-Si can be and still produce crystalline Si. Using a 10 nm Al film, they deposited Si films of varying thickness, as shown in figure 2.11b). When the a-Si layer is very thin, < 5 nm, the crystalline Si is present in the form of islands. As the initial a-Si layer thickness increases, the islands grow and eventually form a continuous film at a a-Si thickness of about 15 nm.

There is disagreement regarding which parameters governs the orientation of the crystallized Si after AIC. Most groups monitoring the silicon orientation after AIC use the same deposition conditions but anneal at several temperatures and durations. The two parameters that are most commonly referred to as crucial for the crystalline silicon orientation are Al/Si layer thickness and the formation of an oxide layer between these. The different process parameters are:

1. Deposition method for Al and Si. Electron beam deposition and sputtering are the two most common methods.
2. Rate, temperature and pressure during deposition.
3. Al and Si thickness.
4. The presence of an oxide layer between the metal and semiconductor layers, and the thickness of this layer.
5. Annealing temperature and duration.

The influence of Al deposition method on Si crystal orientation

Most groups reporting Si[111] thin films use Al sputter deposition[61][63][64], but some groups also report [001]-orientation[57]. One group using e-beam evaporation of Al report (111)-orientation[65], but most report a preferential [001]-orientation[66][67]. The major difference between sputtered and evaporated Al is the orientation of the Al, which is oriented in the (111) direction when sputtered but more randomly oriented after evaporation[68].

The influence of Al and Si thickness on crystal orientation

Kurosawa et al. suggest that a thinner Al film leads to Si[111] as shown in the electron backscatter diffraction(EBSD) maps in figure 2.12a)[1]. This is also confirmed by Numata et al.[64], who found an increase in the [111]/[100]-orientation

[1]For an explanation of pole figures, see section 2.5.3.

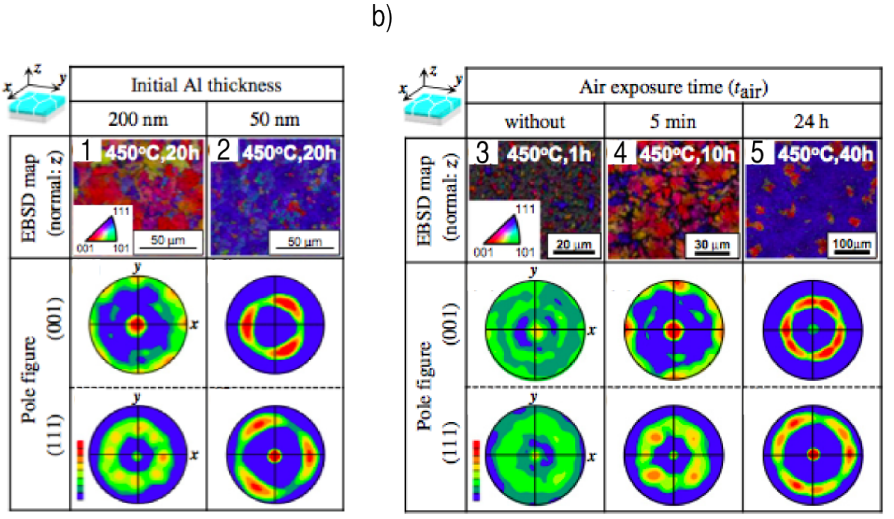

Figure 2.12: EBSD maps (1-5) and pole figures showing the Si crystal orientation after AIC of Al/Al_2O_3/a-Si samples. The crystal orientation dependency on Al thickness is shown in a), while the crystal orientation dependency on air exposure time is shown in b). Samples 1 and 2 were exposed to air for 5 minutes and annealed at 450°C for less than 10 hours, while samples 3-5 had an initial Al thickness of 100 nm and were annealed at 450°C until crystallization. Adapted from [54].

ratio with decreasing Al and Si thicknesses from 400 to 50 nm. They found that the change in preferred orientation happened around 100 nm thickness. The samples prepared by Numata et al. were annealed at 425°C for 10 hours and a thin SiO_2 layer formed a membrane between Al and Si.

The influence of oxide layer formation on crystal orientation

An oxide layer can form between the aluminum and amorphous silicon layers by either exposure to air after Al deposition or inserting a silicon dioxide layer. The annealing time required to crystallize silicon increases drastically with the duration of air exposure for Al, suggesting that the Al_2O_3 layer thickens with increasing time[54]. A thicker oxide leads to Si[111] according to Kurosawa et. al., as shown in figure 2.12b), where all samples were annealed at 450°C until

complete layer exchange. Kurosawa et al. also report that longer air-exposure time leads to larger Si grains.

Okada et al. have investigated the resulting silicon crystal orientation when depositing a silicon dioxide layer between the Al and Si before annealing. They conclude that the resulting Si orientation strongly depends on the SiO_2 thickness, and that the amount of [111]-oriented Si increases with thicker layers up to a certain thickness[61].

Crystalline silicon grain size

Lower annealing times can lead to larger Si grains, up to tens of microns, as the nucleation rate is slowed compared with the velocity of grain growth[69][51]. Sugimoto et al. report grain sizes of 0.2-3 μm, which is one order of magnitude smaller than most other groups, as a result of their native oxide free AIC process[65].

2.4 Electron beam lithography

Electron beam lithography (EBL) shares several principles with light microscopy, but has replaced many of the key elements to obtain a higher resolution. A high voltage source and a filament are used in stead of a light source, and magnetic fields replace the lenses. Vacuum is a requirement, to ensure that the electrons do not collide with anything before hitting the sample. A typical setup for EBL is shown in figure 2.13. An EBL system is comprised of three main parts; a scanning electron microscope(SEM), a stage and a computer control system. The stage can be controlled with high precision in the x-y-z directions because of a laser-interferometric positioning system with a resolution of 5 nm and a combination of servo-motors and piezo-electric actuators[70]. A computer system is connected to both the SEM and stage, and it enables detailed control of the beam shape and position. The computer system is also used to load a pattern and set exposure parameters.

Intrinsic EBL resolutions of only a few nanometers have been demonstrated[71], but normally the post-treatment and the pattern transfer stages limit the final resolution of a pattern made with EBL. The limitations presented by treating the resist after exposure results in a lowest possible resolution of $\sim$10 nm[72, 153].

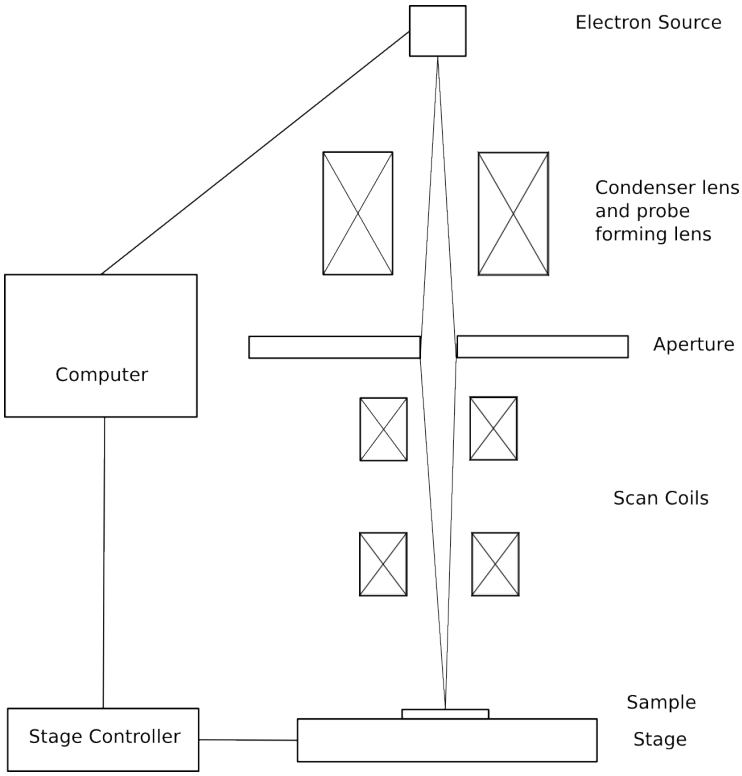

Figure 2.13: Diagram of a typical EBL set-up.

The operating principles of EBL

The electron source of an EBL setup is either a thermionic or field-emission emitter. The latter can produce the smallest incident beam size(down to 1 nm)[72]. The voltage used to accelerate electrons from the electron source to the specimen determines the kinetic energy of the incident electrons, and thereby their penetration depth. Condenser lenses shape the beam, and the objective lens (which is the lens closes to the specimen) determines the final spatial resolution. The quality of the objective lens governs the amount of aberrations, or distortions, to the patterning.

Two sets of deflecting coils can deflect the beam to scan the sample. The incident beam scans the specimen in two perpendicular directions: the x- and y-directions. The beam is blanked in the areas the pattern is not to be exposed. This process is called raster scanning. The beam is moved over the specimen in the x-direction first, by a step size s, performing a line scan. After reaching its endpoint in the x-direction, it returns to its origin and the time consumed during the return is called the flyback time. An offset equal to the step size is introduced in the y-direction to scan the next line. If the beam is moved continually in the x- and y-directions during exposure it is called vector scanning. After scanning, a rectangular portion of the specimen has been exposed, called a frame. The frame size is also referred to as the write field(WF) size, and can be adjusted. A larger WF generally means less precision as the magnification is diminished. To expose an area larger than one WF the specimen must be moved, and the next frame must be exposed adjacent to the last one. This procedure is called stitching, and can result in offsets between neighboring frames, referred to as stitching errors.

The wavelength of the incident electrons is the ultimate limitation on resolution for any electron-based microscope. The wavelength has an inverse dependency on the accelerating voltage, and the voltage is therefore usually held high, see equation 2.6. The wavelength of electrons is given by the de Broglie relation in equation 2.5[73, p 172-173]

$$\lambda_e = \frac{h}{p} = \frac{h}{\sqrt{2m_e E_{kin}}} \tag{2.5}$$

Here, h is Planck's constant with a value of $6.63 * 10^{-34}\ m^2 kg/s$, p is the momentum, m_e is the electron mass of $9.11 * 10^{-31}$ kg and E_{kin} is the kinetic energy of the electrons. Simplifying equation 2.5 by inserting number values and the electric potential V for E_{kin} gives equation 2.6.

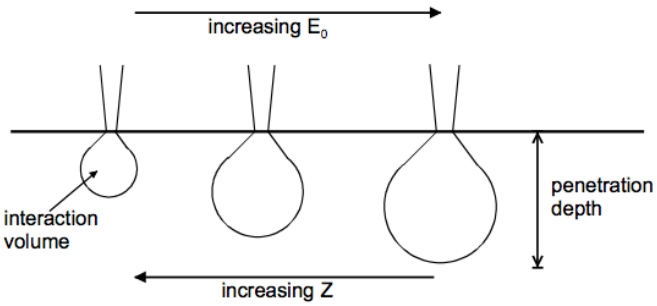

Figure 2.14: Interaction volume dependency on electron energy and the atomic number of the sample[72].

$$\lambda_e = \sqrt{\frac{150}{V}} \tag{2.6}$$

The answer is given in units of angstrom, while V is given in Volts. This leads to wavelengths of 0.02-0.4 Å. If the accelerating voltage is 20 kV, then λ_e is 0.087 Å.

The penetration depth of the electrons increases linearly with the energy and increases inversely with the density of the solid, as shown in figure 2.14. The volume affected by the scattering electrons is called the interaction volume, and is a quantity found by averaging a large number of electrons. To find the interaction volume of a given solid, Monte Carlo simulations are typically used. As is evident from figure 2.14, the electron resist(ER) layer must be thin to prevent too much lateral scattering and loss of resolution.

Exposure

To find exposure parameters that produce the correct pattern in the ER, several parameters must be adjusted. The electron beam current, the electron beam's dwell time and the step size all influence the exposure dose, D, as is shown in the case of area exposure in equation 2.7[70]. The dwell time is the duration of exposure for each 'stop', or step, of the beam.

$$D = \frac{It}{s^2} \tag{2.7}$$

Here, I is the current in Ampere, t is the dwell time in seconds and s is the step size in meters. The dose is a number in the range 0-200 given as $\mu As/cm^2$. Usually, the dose, current and step sizes are chosen and then the EBL system chooses the appropriate dwell time.

Exposure modes

Different exposure modes can be used during EBL operation, and the choice affects the pattern exposure and exposure time. There are two modes that can be used to expose circular features; area exposure and circular exposure. By altering the parameters of the area exposure mode a third mode can also be used; one-shot exposure. The most important difference between these modes is the time consumed when exposing larger areas of resist. One-shot exposure is significantly faster than circle exposure, which in turn is significantly faster than area exposure. Time consumption was investigated by Susanne Sandell in the spring of 2012, and the following times were found when exposing a 100 μm x 100 μm pattern made up of a circle array[74]:

- Area exposure: 49 min 7 s
- Circle exposure: 2 min 40 s
- One-shot exposure with 5 ms dwell time: 51 s

Area exposure

The beam is scanned across the sample in the x- and y- directions. A circular feature is divided into trapezoids, and the beam is blanked when moving between these trapezoids. Area exposure thus leads to rough edges for circular features. This is shown in figure 2.15a).

Circular exposure

This mode can only be used for completely filled and circular features. The beam exposes the sample by writing rings that decrease in size. By reducing the need for moving the stage without doing exposure, this is faster then area exposure when exposing circular patterns, and the outer edge is sharper than with area exposure. See figure 2.15b).

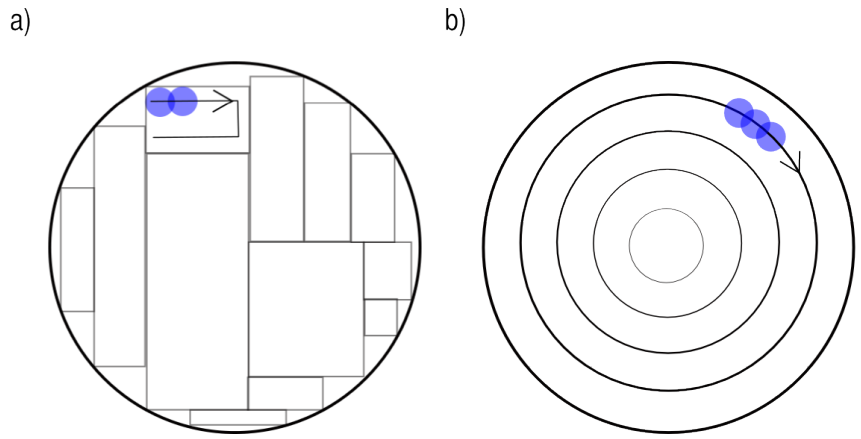

Figure 2.15: The two main exposure modes in EBL, where a) is area mode and b) is circular mode for a ∼100 nm dot.

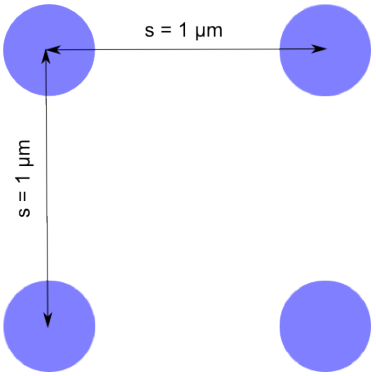

Figure 2.16: The one-shot exposure mode, exemplified by exposure done with a pitch distance of 1 μm and circles with a ∼100 nm diameter.

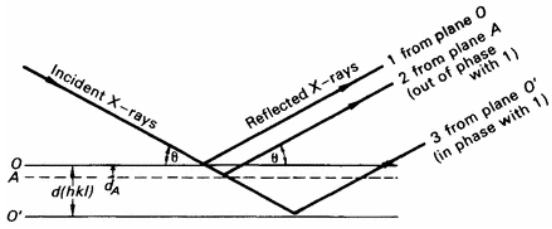

Figure 2.17: Bragg reflection from (hkl) planes. Planes O and O' are in the same family of planes and A is not.[75]

One-shot exposure

This mode utilizes the fact that both the beam and the pattern share the same shape; a circle. It is a variation of area exposure, but the step size is increased to the μm range, and is thereby determining the pitch size, as seen in figure 2.16. The beam dwells at each step for an extended amount of time, which creates a circle due to the electron scattering. The circle diameter now only depends on the dwell time, current and voltage of the beam. Dwell time is typically in the range of ms, and the resulting circles are between fifty to a few hundred nm in diameter.

2.5 Characterization techniques

2.5.1 X-ray diffraction

X-ray diffraction(XRD) can be utilized both to study the material composition and the crystal structure of a sample because the wavelength of x-rays, 0.7 to 2 Å, is similar to the spacing between atoms in a crystal. X-ray diffraction is a combined scattering and interference effect[75, p 134], and complex calculations are required to understand the complete process. However, much information can be revealed by the Bragg treatment.

Bragg treated crystal planes as atomic mirrors, supported by the fact that if a crystal is rotated by an angle α, the diffracted ray is rotated by 2α. He furthermore described x-rays as having equal angles of incidence and reflectance. Some part of the incoming x-ray beam would be reflected by the first plane of atoms in the crystal, while the rest would continue to repeat the process at the next plane of atoms[30, p 193]. This process is shown in figure 2.17, and a

relationship between the interplanar spacing d, the x-ray wavelength λ and the Bragg angle θ can be found by a geometrical treatment of this figure:

$$n\lambda = 2d\sin\theta \tag{2.8}$$

The equation is called Bragg's law, and states that only the waves with a path length difference of $n\lambda$ will be reflected. The reason is that the waves reflected at each plane of atoms will interfere, and only waves interfering constructively will contribute to the total reflection. Total constructive interference means the superposition of waves with the same amplitude and phase, which means a path length difference of $n\lambda$. The integer number n is often included in the term $d(hkl)$ and so the Bragg equation becomes

$$\lambda = 2d(hkl)\sin\theta(hkl) \tag{2.9}$$

The spacing $d(hkl)$ can be related to the lattice constant a through the equation[30, p 194]:

$$d(hkl) = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{2.10}$$

Bragg reflection is used to calculate the lattice spacing and crystal orientation of a material by varying the incident angle θ and reflected angle 2θ.

There are two main techniques that are used in x-ray photography; single-crystal and powder photographs[75, p 139]. Powder photographs can be used to identify substances, but provide limited information on crystal structure.

Single crystal x-ray photographs

Two methods can be used within single-crystal x-ray photographs: The Laue method and the oscillation/rotating-crystal method. The main difference between the two methods is that the Laue method varies the wavelength of the incident x-rays to produce a diffraction spectrum, while the oscillation method varies the angle θ by rotating the crystal to produce a diffraction spectrum.

Measurement set-up

Different measurements can be done by XRD. The two main groups are in-plane measurements and out-of-plane measurements. With in-plane measurements, the observed planes are perpendicular to the sample surface, and the diffraction angle is denoted as $2\theta_\chi/\phi$[76, p 190]. In out-of plane measurements the

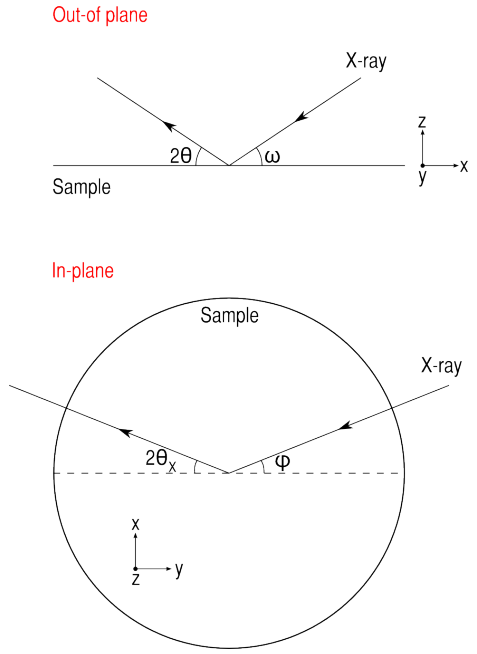

Figure 2.18: In-plane measurements are done with the observed planes perpendicular to the sample surface, while out-of plane measurements are done with the observed planes parallel to the sample surface.

observed planes are parallel to the sample surface and the diffraction angle is denoted $2\theta/\omega$. The difference between these two measurements is shown in figure 2.18. The most common type of in-plane measurements is Grazing Incidence XRD(GIXRD), and the most common out-of-plane measurements are rocking curve and $2\theta/\omega$. With a rocking curve measurement, only the incident angle(ω) is altered, while in a $2\theta/\omega$ measurement both the incident angle ω and the detector angle 2θ are moved, keeping the relationship between the two angles fixed to $\omega = \theta = \frac{1}{2}2\theta$ or $\omega = \frac{1}{2}2\theta + offset$.

2.5.2 Electron-dispersive X-ray spectroscopy

Energy-dispersive x-ray(EDX) spectroscopy is an analysis method that can be used in combination with a scanning electron microscope(SEM). The probing of a sample with an electron beam not only scatters the electrons, but gives rise to other excitation phenomena as well. Upon the excitation of an electron from the inner shell of an atom, a hole is left behind which is filled by an electron from another shell. The electron then emits excess energy in the form of x-rays or Auger electrons. These emissions are characteristic for the atom emitting them and can thus be used to analyze the atomic composition of a sample[30, p 373]. Since the x-ray energy depends on the atomic number of the target atoms, it is limited to elements of atomic number greater than about ten.

The escape depth of x-rays can be several micrometers below the sample surface, and depends on the sample material and the energy of the incoming electron beam. This is related to the interaction volume of the incoming electrons with the sample and thus limits the resolution of EDX in the xyz-directions.

2.5.3 Electron Backscatter Diffraction

Electron backscatter diffraction(EBSD), also called backscatter Kikuchi diffraction(BKD), is a characterization method that probes the microstructure of material surfaces, and can be used with conventional scanning electron microscopes. The technique can reveal information on the microstructure, crystal orientation, phase identification, grain boundaries and deformation of the sample material. The main principle is the automated detection of electron diffraction patterns from scanning an electron beam over a tilted sample.

The primary electrons, in contrast to low-energy secondary electrons, of the electron beam are scattered by the lattice planes in the target material. The scattered primary electrons are then termed backscattered electrons. This process is very similar and arises from the same geometric considerations as

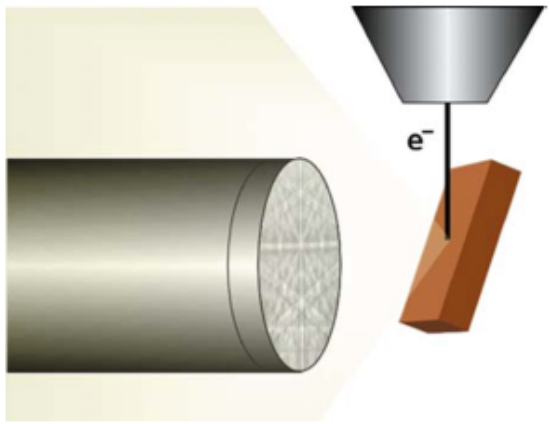

Figure 2.19: A typical EBSD setup, showing the incoming electron beam on a tilted sample and the phosphor screen detector[77].

discussed under x-ray diffraction in section 2.5.1. The path difference between electrons diffracted at two adjacent lattice planes must equal a integer number of wavelengths for in-phase reflection, as seen from Bragg's law in equation 2.8. The diffracted pattern can be compared with a calculated crystal coordinate system, and the crystallographic orientation can be determined from this comparison.

The experimental setup when performing EBSD is based on scanning an electron beam over a tilted sample, as shown in figure 2.19. The angle between the incident beam and the sample surface is usually around 20°[77], and this is also the reason why the surface must be as flat as possible. If the surface is rough, shadow effects will limit the spatial resolution.

The spatial resolution of EBSD is limited by two factors; the minimum diffraction volume and the ability of the system software to deconvolute overlapping patterns. The beam should be as small as possible, consistent with the current being large enough for detecting a signal. For standard equipment, this means a probe diameter of 2 nm when operated at 20 kV with a field emission source[77]. The electrons used to form a EBSD image have lost little or no energy upon scattering, and the diffraction volume of the sample would be 22 nm[77] with the mentioned conditions. This results in a resolution of less than $0.02\mu m$. Precision can also be lost when the beam crosses a grain boundary. The images from the two different orientations will overlap at the boundary,

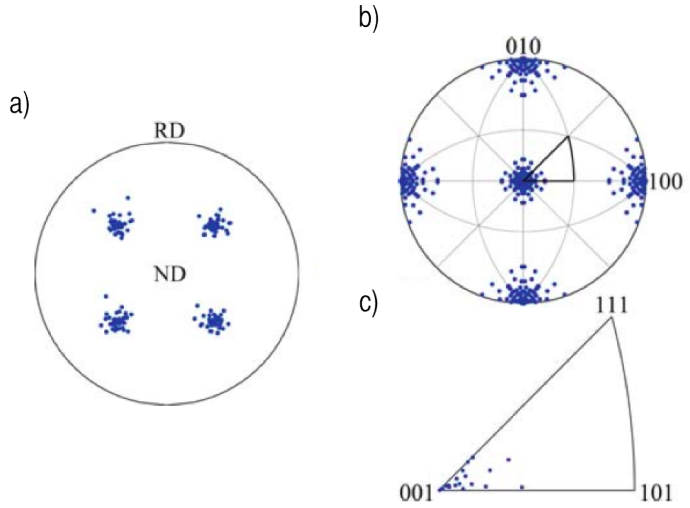

Figure 2.20: a) A {111} pole figure for a cube texture, with the b) normal-direction inverse pole figure and the standard stereographic triangle outlined and magnified in c). 'ND' corresponds to the normal direction and 'RD' corresponds to the roll direction. Illustration adapted from [78].

and it is the computer software's ability to separate the two images that decides wether or not an indexing error occurs.

Measurement types

Normally, the complete microstructure is mapped, coloring each grain in the material in different colors to represent their crystal orientation[78]. Sometimes, it is more interesting to represent the texture of the material without concern for the spatial characteristics. Two coordinate systems are applied to determine the crystallographic orientations. One specimen coordinate system that describes the specimen in real space, and one crystal coordinate system which contains all the different directions in the crystal. An orientation matrix is used to relate the two, and various orientation descriptors can be gathered from this orientation matrix. The most common of these are Euler angles, orientation distribution functions, 'ideal orientation' notation, pole figures, inverse pole figures and the Rodrigues vector.

Pole figures are used to map the distribution of several measurements, and is a statistical data representation. It is a stereographic projection of a certain crystallographic axis, as exemplified in figure 2.20.

Chapter 3

Methods and materials

An explanation of the various materials and processes is given here, while numbers and detailed step-by-step descriptions can be found in appendix B. Substrate preparations, the AIC process and the EBL patterning process are described in said order, before the specific instruments used with the experiments are presented.

3.1 Substrate preparation

This section describes the preparation of the different substrates used during the AIC and Si evaporation processes. Glass substrates were used for investigating annealing parameters, graphite and graphene substrates were used to investigate the AIC process on the respective surfaces, and GaAs substrates were used to perform EDX on Al/Si structures without background noise signals from the substrate.

3.1.1 Glass substrates

Microscopy cover slips were used as glass substrates, and were annealed at 500°C for 1-2 hours under ambient nitrogen gas to remove possible contamination before being used in the AIC process. Cover slips and not slide glasses were used because substrates had to be very thin($< \sim$1.5 mm) to do XRD measurements.

3.1.2 Kish graphite substrates

Kish graphite is a byproduct that is produced when iron melts. It is formed on the free surface of molten iron during cooling and grows in a foliated dendritic manner[79]. It has a near ideal crystal structure, as XRD investigations have shown that it is near identical to natural graphite[80]. To achieve single-layer graphene, kish graphite can be micro-mechanically cleaved by exfoliation with tape.

P-doped silicon wafers with a 300 nm thermal oxide layer or (111)-oriented gallium arsenide wafers were the basis for these substrates. The advantage of using the Si/SiO_2 substrates is that interference makes the single- and few-layer graphene visible in an optical microscope. The wafers were cleaned with acetone, isopropanol and dried with N_2. They were subsequently oxygen plasma etched to improve adhesion properties and few-layer graphene was transferred onto the substrates by the exfoliation of kish graphite(KG) with tape. The substrates were thereby annealed under a flow of forming gas to remove any tape remnants. This annealing step was performed at 350°C for two hours with a 75 sccm flow of H_2/Ar.

3.1.3 Graphene on copper substrates

Single-layer graphene produced by mechanical exfoliation is size-limited to samples of $< 10\ \mu m$[42]. Synthesis by CVD can be done at a larger scale, and has therefore been the main focus for large-scale production of graphene the past few years. In the CVD process for copper substrates, methane gas is mixed with hydrogen gas and introduced to the copper substrate at temperatures of about ∼1000°C and low pressures(0.5-50 Torr)[37][81]. The methane gas decomposes at the copper surface, and the carbon nucleates and grows in a randomly orientated matter. This leads to the formation of grains in the resulting graphene layer. The chemical reaction is described in equation 3.1.

$$CH_4 \rightarrow C + 2\,H_2 \tag{3.1}$$

The graphene grown on copper also contains wrinkles, and this is contributed to the large differences in thermal expansion coefficients(TEC) of graphene and copper. $\alpha_{graphene} = -6 * 10^{-6} K^{-1}$ at 27°C[82] and $\alpha_{Cu} = 16.5 * 10^{-6} K^{-1}$ at 27°C[83], where the negative sign of graphene's TEC indicates that the lattice of graphene shrinks when the temperature is increased. The large difference in thermal expansion coefficients suggests that Cu shrinks significantly more than graphene upon cooling, which induces mechanical stress that is released through

the formation of wrinkles in the graphene. Ridges, swells and cracks are also common defects with this growth method[84]. The resulting graphene layers can be contaminated by copper if the copper etch is incomplete.

The deposition of graphene on copper foil has advanced the most, but deposition on Ni[85], Pt[86], Ru[87] and Ge[88] has also been done. In addition to induced defects in graphene that have already been mentioned, the CVD on metal substrates method necessitates a transfer step that degrades graphene quality. Some new methods have recently been developed that reduce grain formation[89] and circumvent the transfer step[90][91][88].

A group led by Keunsoo Kim at Sejong University in Seoul, South-Korea has developed a CVD process for depositing high-quality graphene on copper. These substrates were therefore used as delivered from South-Korea, and no further cleaning steps were necessary. The substrates consisted of thin copper foil covered with single-layer graphene on both sides.

3.2 Process routes

3.2.1 Metal-Induced Crystallization

Different substrates, as described in section 3.1, were used during the investigation of metal-induced crystallization. Aluminum and amorphous silicon thin films were deposited on these substrates by electron beam evaporation or sputtering, either by a Pfeiffer Classic 500 e-beam evaporator or an AJA international sputter and evaporator. All depositions were done at high vacuum($< 5 * 10^{-6}$ Torr) and with a rotating sample holder. After depositing aluminum, the samples were exposed to oxygen for a time interval between 20 minutes and 24 hours to allow an oxide layer to form, see table 3.1. Amorphous silicon was deposited by e-beam evaporation at 1 Å/s. Table 3.1 lists these steps. An annealing step was then performed to induce crystallization and rearrange the stacking of the aluminum and silicon layers. The annealing was done in a gold furnace, at 470 or 500°C under ambient N_2 gas flow at varying time intervals. Copper substrates had to be processed to remove the copper before annealing, see the appendix C.1. The aluminum was removed by etching in 25 % hydrochloric(HCl) acid for $\sim$ 45 min. After etching, the samples were rinsed in water for $\sim$ 5 minutes and dried with N_2 gas.

Table 3.1: Parameters used for the deposition of Al and Si thin films.

Step	Material	Thickness [nm]	Rate [Å/s]
1	Al	10-50	1-1.7
3	Si	2.5 - 50	1

3.2.2 Silicon patterning of few-layer graphene by electron beam lithography

The patterning of nanostructures with EBL is done by patterning an electron-sensitive resist with a focused high-energy electron beam. The ER used in this work was a double layer of 200k and 950k PMMA giving a total thickness of ∼150 nm. These are positive resists, meaning that the areas exposed to the electron beam dissolve during development. The k number refers to the atomic weight of the polymers in the resist, and the lower the number the more easily the bonds in the resist weaken upon exposure. Before exposing the sample, a reference mark was made and suitable pattern positions, which contained kish graphite flakes, were located. A square region of 100 μm x 100 μm was scanned by the electron beam, setting the step size to 1 μm and using one-shot exposure as described in section 2.4. The exposure dose was chosen by adjusting the exposure time, and the exposure was done at 30 kV with a 40 μA current. The sample was developed in a mixture of isopropanol and water, before an oxygen plasma etching step was performed to remove remnants of PMMA from the exposed areas of few-layer graphene. The AIC process was then performed as described in section 3.2.1, the only difference being that lift-off was performed after the deposition of silicon to remove the PMMA and non-patterned aluminum and silicon. The sample was subsequently annealed and etched. The detailed steps of the process are found in appendix C.2.

3.3 Instruments

3.3.1 Sputtering

An AJA international sputter and evaporator was used to deposit thin films by sputtering. It can operate at 50-400 W, and uses a DC field to ionize Ar atoms supplied at 67 sccm under a pressure of 1-10 mTorr. The Ar atoms bombard the material target to eject atoms from the surface. These ejected atoms hit the

substrate to deposit a thin film. Substrates can rotate and be heated during deposition.

3.3.2 Electron beam evaporation

E-beam evaporation was carried out with two instruments; a Pfeiffer Classic 500 e-beam evaporator and the AJA international sputter and evaporator.

Pfeiffer Classic 500 e-beam evaporator

The electron gun operates at 8 kV under a pressure of $\sim 10^{-7}$ Torr. A MDC-360 Deposition controller is used to control the fim deposition, and the deposition rate can be varied from 1 to 200 Å/s, depending on the target material. Substrates can be rotated during deposition to achieve uniform film thickness.

AJA international sputter and evaporator

An e-gun operating under a voltage of 8.9 kV heats the target material to achieve evaporation. The pressure in the specimen chamber is on the order of 10^{-8} to 10^{-7} Torr. Deposition rates are 1 to 10 Å/s and the film thickness can be between 1 nm and 2 microns. Substrates can rotate and be heated during deposition.

3.3.3 Electron Beam Lithography

The EBL setup at NTNU NanoLab is a Hitachi Field emitter 4300 SEM with a Raith Elphy+ stage system. The electron source is a ZrO/W Schottky Emission tip, polished to a sharp needle point and heated to 1700 K upon emission. The accelerating voltage is between 0.5-30kV, and an electromagnetic lens reduction system focuses the beam. The SEM has a maximum resolution of 1.5 nm at 30kV with a working distance of 5 nm. The electron gun operates under a vacuum of $\sim 10^{-7}$ Pa by ion pumps, and the specimen chamber can reach a vacuum of $7 * 10^{-4}$ Pa with oil rotary pumps[92]. The laser interferometer stage enables stitching between write fields with less than 20 nm shift. Masks are written in either Elphy plus software or Clewin. With the resist and processes at NTNU NanoLab, 30-40 nm structures should be feasible.

3.4 Characterization

X-ray diffraction

A D8 HRXRD system is installed at NTNU. It is mainly used to study thin films, and has an unfiltered intensity of 170 000 000 cps(counts per second) and registers both $K\alpha 1$ and $K\alpha 2$. The width and length of the x-ray on the sample is decided by the insertion of slits. If no slit is inserted, the width is about 12 mm and the height is governed by equation 3.2[93]

$$L = \frac{h}{\sin(\omega)} \tag{3.2}$$

Here, L is the length of the beam on the sample, h is the height of the beam determined by the slit and ω is the incident angle.

The X-ray source is a copper filament, resulting in x-rays with a wavelength of 1.5406Å, and the generator is normally set to 40 kV and 40 mA.

Before collecting a $2\theta/\omega$ scan, the x-ray source was pre-warmed for at least 30 minutes. The sample was aligned by doing z- and rocking curve-scans on the sample surface three times, and the aligned angle ω was adjusted according to this procedure. A step size of 0.001° and a step counter of 7 s was used for all long(2θ between 20° and 70°) scans.

Energy-dispersive X-ray spectroscopy

The EDX system at the NTNU NanoLab consists of a Hitachi S-5500 S(T)EM and Bruker XFlash EDX Detector. The acceleration voltage can be 0.5-30 kV and the highest resolution possible is 0.4 nm. It is an in-lens cold field emission electron microscope, something which limits the sample size to about 0.5x1 cm.

Electron backscatter diffraction

The EM-lab at NTNU Department of Materials Science and Engineering has two SEMs that are configured to do EBSD mapping; a Zeiss Ultra 55 FE-SEM and a Hitachi SU6600 FEG SEM. They can be used with voltages of 2-30 kV and 1-30 kV, and the resolutions are 0.8 and 1.2 nm, respectively. Both microscopes were used during this project.

Chapter 4

Results

4.1 Low yield of vertical nanowires grown on graphene surfaces

The experimental work has focused on methods that can improve the yield of GaAs nanowires grown on graphene by introducing Si[111] as nucleation sites on graphene substrates. Epitaxial growth of GaAs nanowires on few-layer graphene had earlier been achieved, but with low yields and significant two-dimensional growth both on the few-layer graphene and oxide substrate, this is shown in figure 4.1. The GaAs nanowire yield achieved for a hole-patterned oxide mask on a silicon substrate has been close to 80%[32], meaning that there is a GaAs nanowire growing in eight out of ten patterned holes. In comparison, the yield achieved for nanowires grown on an open region of few-layer graphene with the two-temperature MBE process has been $\sim$0.6 NW/μm^2. For a hole-patterned oxide mask on few-layer graphene, only one or two out of a hundred holes were occupied by nanowires.

Using silicon on graphene to increase the nucleation density of GaAs nanowires was proposed as a possible solution to increase the nanowire yield. As described in the theory section 2.2.3, decreasing the two-dimensional growth can be achieved by employing the same high-temperature scheme as is used for nanowires on silicon substrates. However, this leads to a lower density of nanowires. The ideal situation would be where growth of GaAs nanowires takes place at a high temperature, without the elevated temperature causing a decrease in the yield.

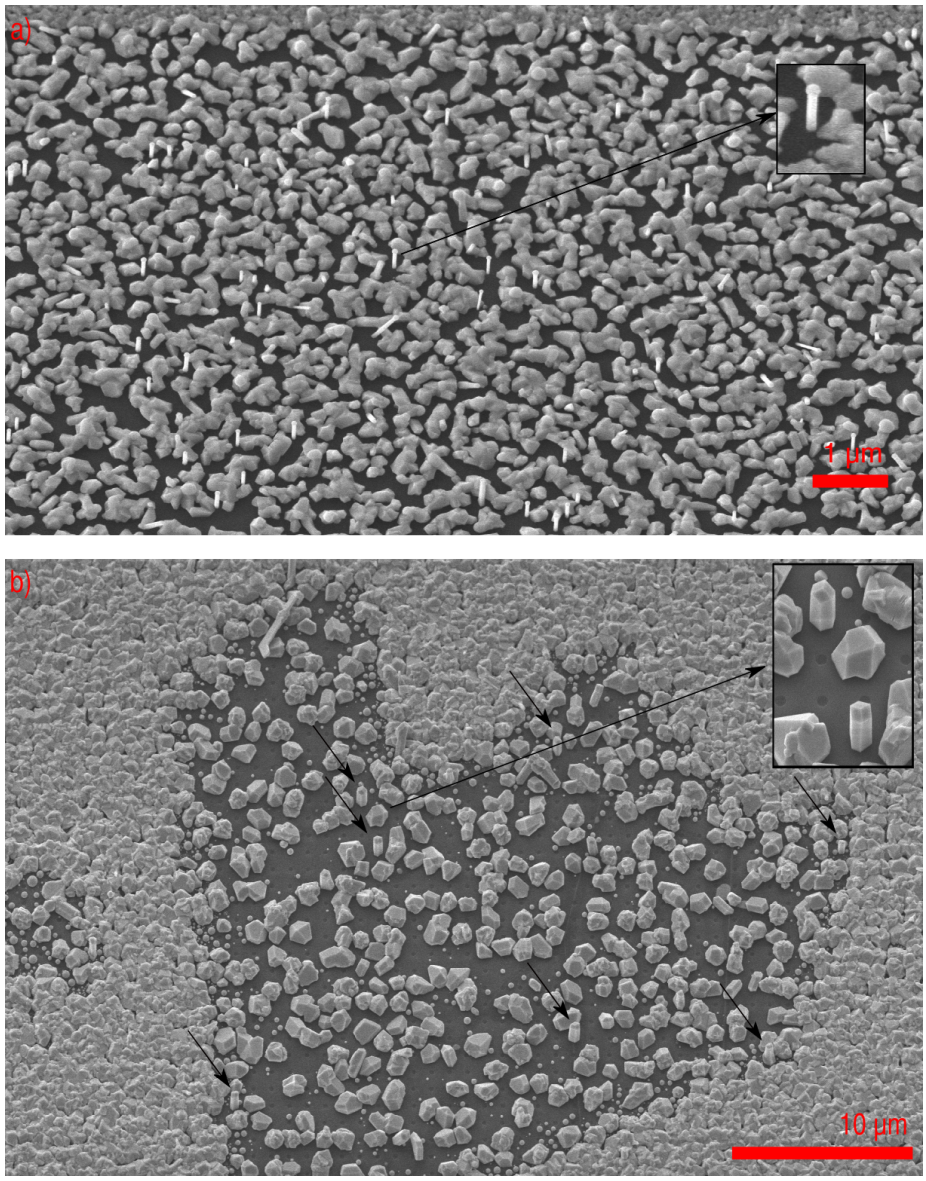

Figure 4.1: SEM images of GaAs nanowires grown on few-layer graphene during my project work in the fall of 2013. In a), a sheet of few-layer graphene is exposed. Several vertical nanowire cores can be seen, indicating epitaxial growth, but a significant amount of two-dimensional growth is also present. b) shows core-shell nanowires grown on few-layer graphene with a patterned oxide mask. Two dimensional growth occurs to some extent on the few-layer graphene, but even more so on the surrounding substrate as a result of the low temperature employed during nanowire nucleation. The arrows point to nanowires.

A first attempt to increase the yield of nanowires was to deposit a thin film of amorphous silicon on few-layer graphene, and the result of growing nanowires on this sample is shown in figure A.1 in the appendix. The results were ambiguous as it was unclear if the amorphous silicon had actually deposited on the few-layer graphene or only on the SiO_2 substrate. The nanowires had a larger yield on the amorphous silicon, but were not vertically aligned, which is important in the fabrication of a photovoltaic device. This is the reason why the silicon should be [111]-oriented; any other orientation will not lead to vertical nanowires. As described in theory section 2.1.2, the geometry of the nanowire solar cell influences its efficiency.

Two methods of depositing [111]-oriented silicon on a graphene surface were tested; aluminum-induced crystallization(AIC) and silicon island formation by chemical vapor deposition. The main focus was directed towards AIC, and the principles and process are described in the theory section 2.3 and methods section 3.2, while the evaporation of silicon principles and process are described in the appendix sections E.1 and E.2.

4.2 Aluminum-induced crystallization

The high temperature required for crystallization of amorphous silicon severely reduces the substrates that can be used. Metal-induced crytallization(MIC) is a method that reduces the crystallization temperature of silicon by contacting a semiconducting material with a metal and thus allowing for a diffusion pathway to crystallization, which lowers the free energy of the amorphous phase at elevated temperatures. For our purposes, the material chosen to be the metal contact should be compatible with later processing in the MBE chamber and be available in the laboratory facilities at NTNU. The choice therefore fell upon aluminum, as Al does not contaminate the MBE chamber and can be deposited both by sputtering and evaporation techniques in the NTNU nanolab.

In order to tailor silicon structures deposited by aluminum-induced crystallization(AIC), several properties must be controlled. These properties are the crystal orientation, morphology and spatial arrangement of the silicon structures. Four different substrates were used for investigating the various aspects of AIC and the silicon structures formed by it; glass, kish graphite on both Si/SiO_2 and GaAs wafers, and graphene substrates.

Two main techniques were used to characterize the crystal orientation of aluminum and silicon during the AIC process; x-ray diffraction(XRD) and electron backscatter diffraction(EBSD). The first is useful for gaining information

Table 4.1: Calculated 2θ values for materials studied in this thesis. $\lambda = 1.5406$ Å.

	2θ values				
Crystal orientation	Al	Cu	Graphite	Si	GaAs
111	38.47	43.32		28.44	27.30
002	44.72	50.45	26.60	32.96	31.63
022	65.10	74.13		47.30	45.34
113	78.23	89.94		56.12	53.73
222	82.44	95.15			56.33
004	99.09	116.93	54.67	69.13	66.05
133	112.03	136.50		76.38	72.87
024	116.58	144.71			75.09
224	137.47			88.03	83.75

on the orientation of all layers of the sample, but is a bulk technique. The second spatially maps the orientation of grains, but is limited to characterizing the sample surface. The morphology of the samples was imaged with an optical and electron microscope. Selected samples were characterized with electron dispersive x-ray spectroscopy(EDX) to spatially map element composition and to calculate element concentrations.

To analyze the data collected by XRD, the Bragg angles of the relevant materials were calculated, using Bragg's law from equation 2.9 and equation 2.10, which relates the lattice plane spacing d with the lattice constant a. These values are found in table 4.1.

4.2.1 Glass substrates

The AIC process was first tested with glass substrates, as this allows for comparison with literature, and gives and indication on what parameters to employ with more complex substrates. A thickness of 50 nm was chosen for the aluminum layer and a thickness of 30 nm was chosen for the silicon layer, as it has been reported that a ratio of less than one for Si/Al content is beneficial to attain a smooth surface[69]. Ultimately, the films should be thinner when used as a nucleation layer for nanowire growth, but initial investigations were done on thicker films to ease XRD characterization.

Three different types of aluminum were tested on glass substrates; e-beam evaporated aluminum with either a Pfeiffer or AJA system and sputtered aluminum. The process steps after depositing aluminum were identical. All samples were annealed at 500°C, but two different annealing times were tested; five and fifteen hours. The results of testing different annealing times are shown in figures 4.2 and 4.3. The optical images shown in the same figures reveal the morphology of the films and can be used to assess how complete the layer exchange has been.

For the sample with Pfeiffer e-beam aluminum in figure 4.2, isolated grains of Si[111] have formed after fifteen hours. The as-deposited aluminum has no preferential crystal orientation, but weak (002)- and (222)-peaks can be seen after annealing. A weak Si(111)-peak is also present after annealing.

The sample with sputtered aluminum in figure 4.3 has [111]-oriented aluminum and silicon, where the aluminum is [111]-oriented as-deposited. No silicon grains can be observed in the optical microscopy images after five and fifteen hours annealing. It does not look like the layer exchange has been complete, as the sample is still green except for the edges which have a silver color.

Based on the results from varying the annealing time, 15 hours annealing was chosen for later samples. E-beam aluminum deposition by a different system was tested, the AJA international sputter and evaporator. The results of the AIC process for this second type of e-beam aluminum are shown in figures 4.4 and 4.5. The Al(111)-peak was measured before annealing(figure 4.23), and the peak intensity is very low. The annealing process led to a complete layer exchange, which could be observed by the eye because of the color change before and after annealing, from green to silver. The XRD scans in figure 4.4c) show a strict [111]-orientation for the silicon, while a small Al(111)-peak can be seen before etching but not after, which together with the optical images indicate that most of the aluminum has been removed by the etching step.

The EBSD map in figure 4.5 shows the orientation of the grains in the silicon film from figure 4.4b). The insulating glass substrate is exposed between adjacent silicon grains, leading to multi-oriented areas due to charging. The EBSD map also shows a dominant [111]-orientation, with the presence of a few small [001]-grains. The grain size can be estimated by the EBSD software, and this was done for the sample in figure 4.4. It was found that the grains were between 20 and 100 μm big, and consisted of subgrains with an average diameter of 11.19 ± 3.31 μm.

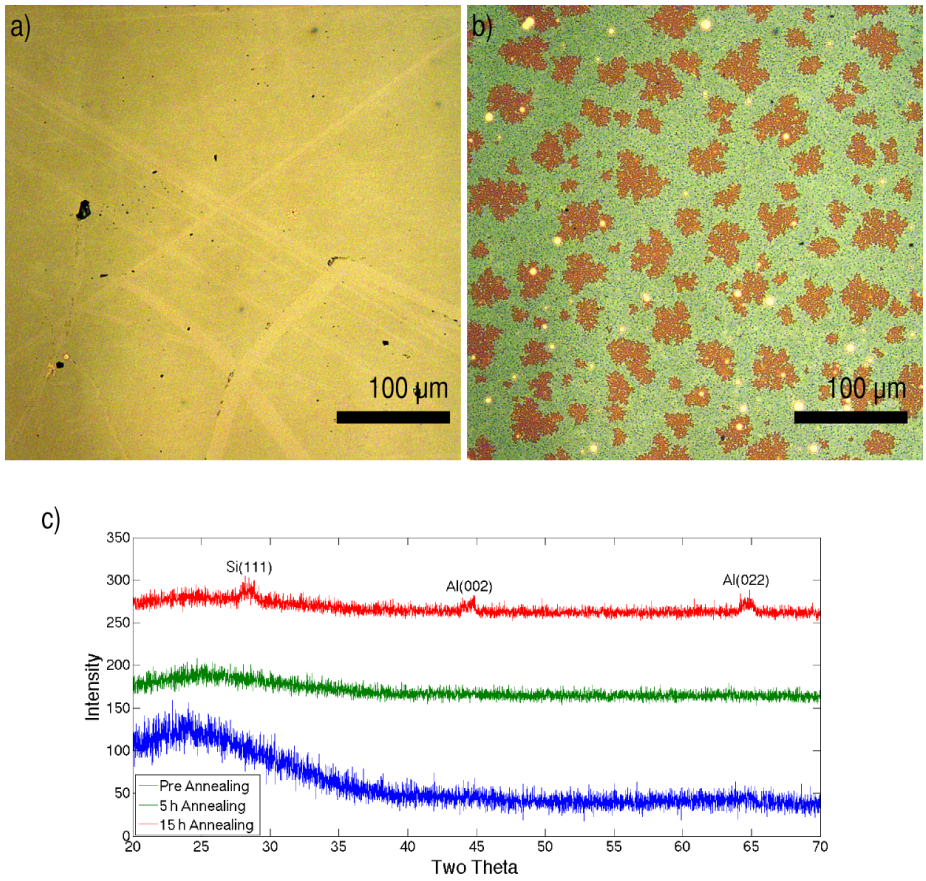

Figure 4.2: Optical images and XRD analysis of a glass substrate with e-beam aluminum from the Pfeiffer Classic 500 e-beam evaporator. The sample was exposed to air for 24 hours after the deposition of 50 nm Al, and 30 nm Si was subsequently deposited. a) Shows an area in the middle of the sample after 5 hours annealing, while b) shows an area in the middle of the sample after 15 hours annealing. The sample was characterized by XRD before and after annealing at 500°C, as shown in c).

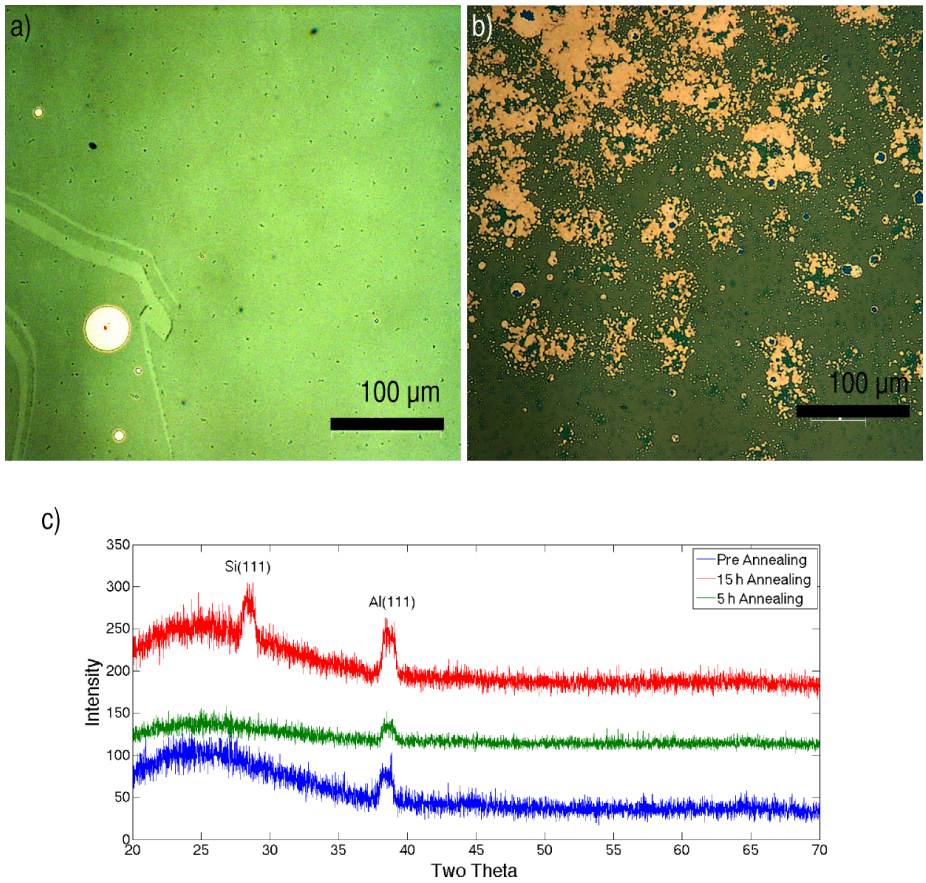

Figure 4.3: Optical images and XRD analysis of a glass substrate with sputtered aluminum. The sample was exposed to air for 24 hours after the deposition of 50 nm Al, and 30 nm Si was subsequently deposited. a) Shows an area at the edge of the sample after 5 hours annealing, while b) shows an area at the edge of the sample after 15 hours annealing. The sample was characterized by XRD before and after annealing at 500°C, as shown in c).

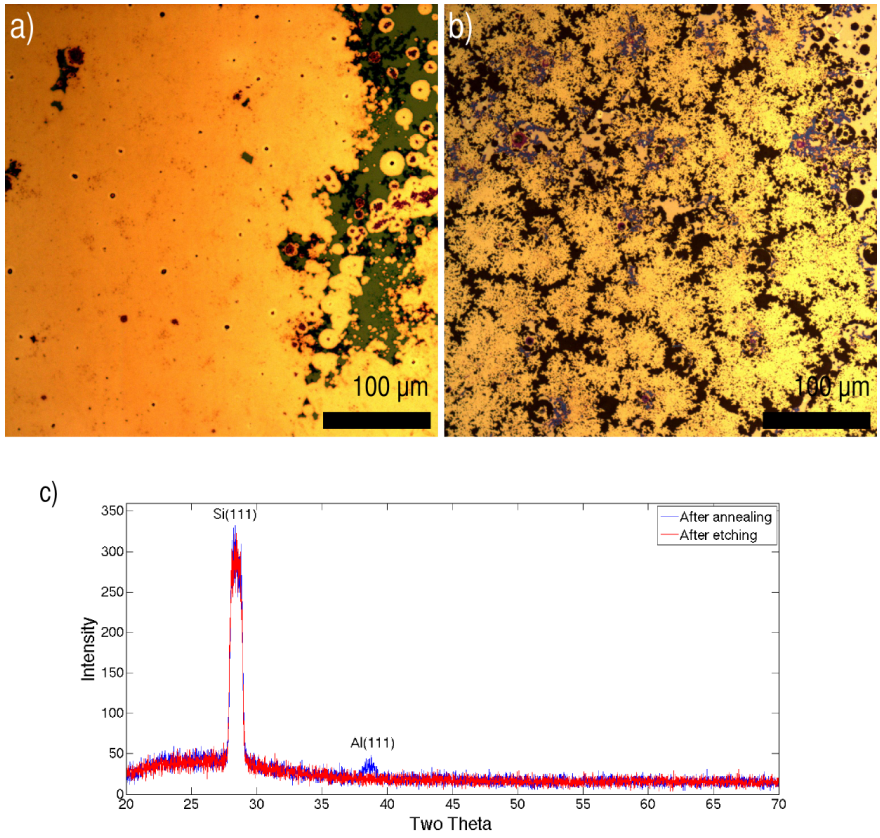

Figure 4.4: Optical images and XRD scans of a glass sample covered with 50 nm AJA e-beam evaporated aluminum and 30 nm silicon. a) depicts the sample after 15 h annealing at 500°C under ambient N_2 gas, b) depicts the sample after etching in 25% HCl, and c) shows the XRD scans after each of the two steps.

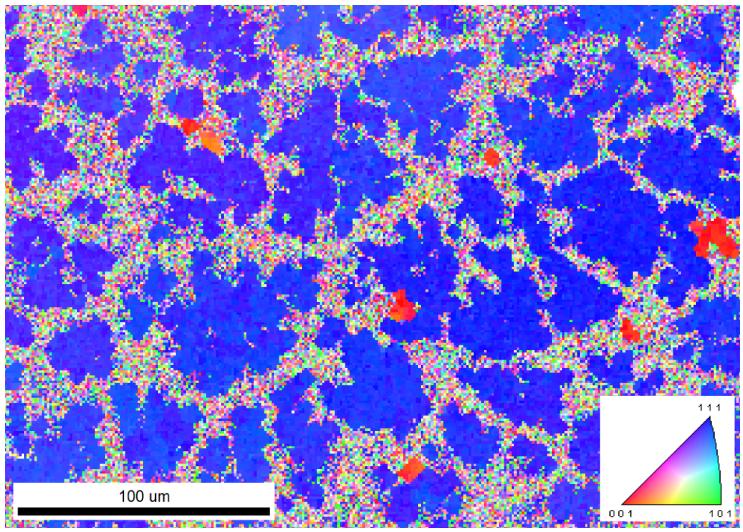

Figure 4.5: EBSD inverse pole figure map of the glass sample in figure 4.4b), which shows a dominant [111]-orientation of the Si grains, with a few interspersed [001]-grains. The insulating glass substrate is exposed between adjacent silicon grains, leading to multi-oriented areas due to charging.

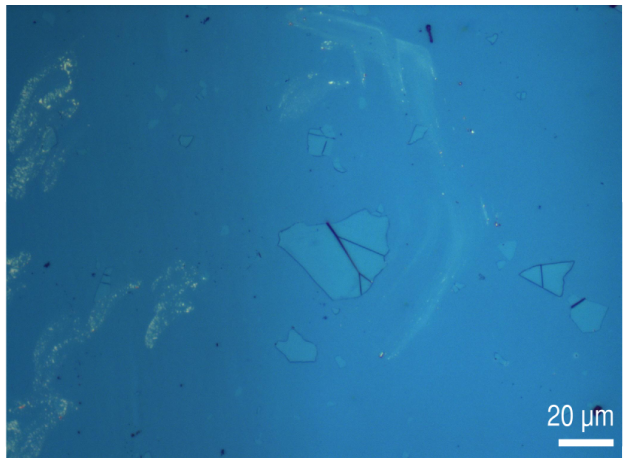

Figure 4.6: An example of a kish graphite sample after the deposition of a thin Al and Si film. The films are uniform and transparent, and kish graphite flakes are clearly visible.

4.2.2 Kish graphite substrates

The substrates were prepared as described in section 3.1.2, using a Si/SiO_2 wafer, and the presence of few- and many-layer graphene was verified by an optical microscopy inspection before depositing thin films on the substrates. Figure 4.6 shows a kish graphite sample after the deposition of 50 nm Al and 30 nm Si, but before any annealing. The films are uniform and transparent, and pieces of graphite can clearly be seen.

Both Pfeiffer and AJA e-beam aluminum were deposited on kish graphite samples. Pfeiffer aluminum was deposited on several samples, but none showed any sign of a Si(111)-peak after annealing, as exemplified by the XRD scan of sample #a-Si07 in figure 4.7. For the samples with Pfeiffer aluminum, the annealing time was varied between 1 to 24 hours and two annealing temperatures were tested; 400°C and 500°C. The oxidation pressure and time was varied between the samples, from almost no exposure($6 * 10^{-3}$ mbar for 20 min) to exposure in an ambient atmosphere for 20 hours. The presence of the Si(004)-peak is due to the silicon substrate, which is Si(001) with a layer of 300 nm SiO_2 on top.

The deposition of AJA e-beam aluminum on kish graphite samples led to

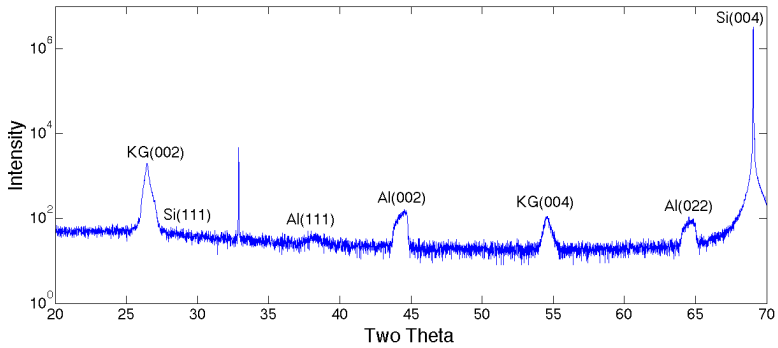

Figure 4.7: A XRD scan of sample #a-Si07 after annealing. 10 nm Pfeiffer e-beam Al was deposited before the sample was exposed to air for 20 hours. 15 nm amorphous silicon was then deposited and the sample was annealed for 24 hours at 500°C. The spike at ∼33° is from the silicon substrate.

Si[111] after annealing as shown in figure 4.8. The XRD scans shown in figure 4.8c) show little change, except for the Al(111)-peak, which has almost disappeared after etching. It can be seen from the optical images that the white areas from figure 4.8a) have been etched away in figure 4.8b). What is also worth to note, is that the dark blue dendrites and white areas in figure 4.8a) only exist in areas where kish graphite is present. EDX was used to study the composition of the sample after etching, and the results are shown in figure 4.9.

The optical images in figure 4.8a) and d) show that several phases exist after annealing and etching the kish graphite sample. EDX was performed to check if the different phases could be distinguished by their elemental composition. The composition of Al, C, Si and O was mapped as shown in figure 4.9c) and e) - g). The dark blue areas in the optical images of figure 4.9a) and d) are areas where the SiO_2 substrate is exposed, as evidenced by the high intensity of oxygen in these areas. As the substrate also contains silicon, it is not possible to map the silicon content, as seen in figure 4.9g). The aluminum map in figure 4.9c) is more informative. The Al is not uniform, and it seems that the dendritic structures seen in the optical images are more Al-rich than other areas.

Annealing times from 20 to 60 hours were tested, to see if extended annealing could influence the dendrite growth seen in the optical images in figure 4.8, and lead to a more uniform film. The results from sample #a-Si10 are shown in figure

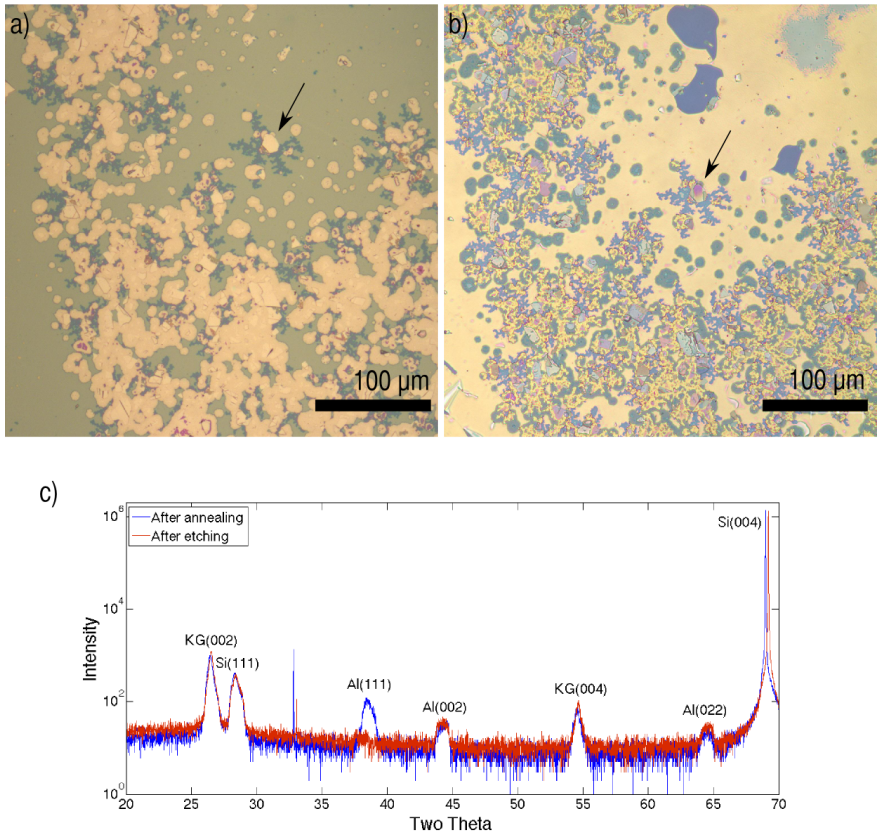

Figure 4.8: 50 nm Al and 30 nm Si was deposited on a kish graphite sample at room temperature by e-beam deposition with 1Å/s deposition rate, interspersed with a 24 hour period of oxidation. The sample was annealed for 15 hours at 500°C with flowing N_2. The optical images are of the same area on the sample, where a) shows the sample after annealing and b) depicts the sample after etching in 25% HCl. The XRD scans from the two process steps are shown in c). The arrows point to the same dendrite. The white areas in a) have been removed by the etchant, revealing yellow and blue dendrite areas in b).

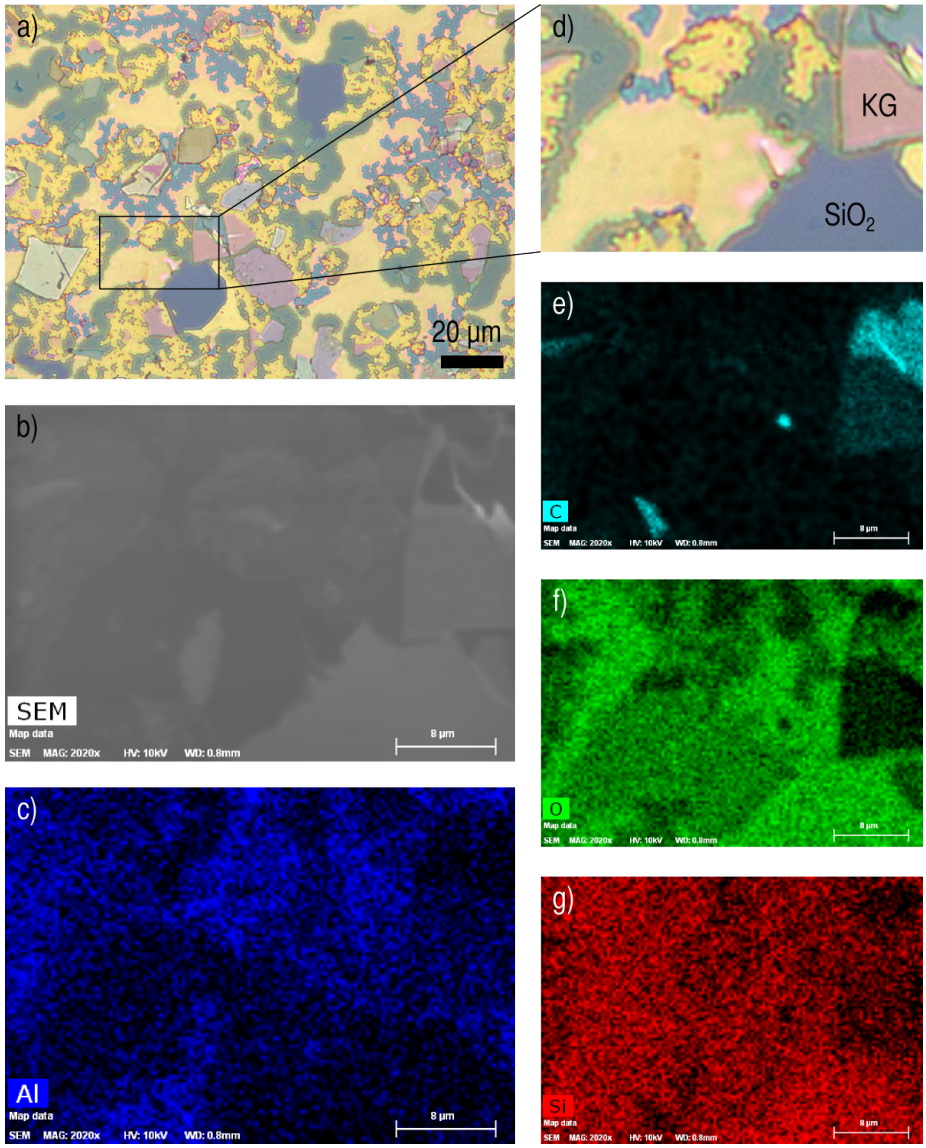

Figure 4.9: EDX measurements of a kish graphite on Si/SiO_2 sample at 5 kV. Optical images of a selected area of the sample in figure 4.8b) are shown in a) and d). b) is a SEM image of the same area, while c) and e)-g) are EDX elemental mapping images. c) depicts aluminum, e) carbon, f) oxygen and g) silicon. All scale bars are 8 μm and KG = kish graphite.

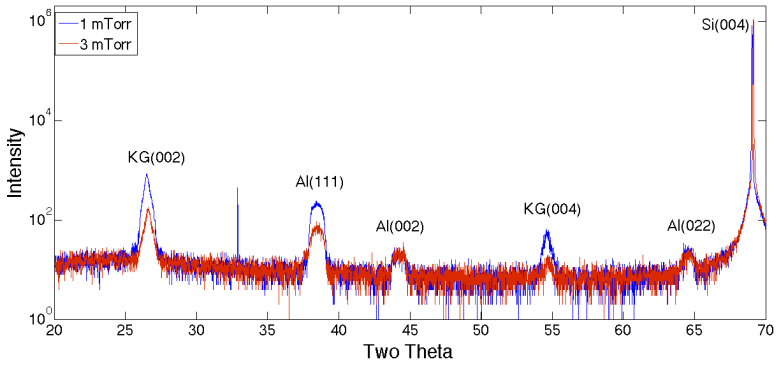

Figure 4.10: XRD scans of samples #a-Si12 and #a-Si13 after the deposition of a 50 nm thick sputtered Al film with a rate of 1 Å/s. The films were deposited under 3 mTorr and 1 mTorr Ar pressure, respectively.

D.1 in the appendix D, and no change can be seen from 20 hours annealing to 60 hours. The annealing time was therefore kept at 15 hours.

Sputtered aluminum was also used in the AIC process on kish graphite substrates. Both different deposition pressures and rates were used to study the resulting orientations of Al and Si. Aluminum was sputtered under two different Ar pressures, 1 mTorr and 3mTorr. Reducing the pressure is equivalent to reducing molecule interactions from target material to substrate. XRD scans of the resulting thin films, before annealing, are shown in figure 4.10. The absolute strength of the signal from the film deposited under 1 mTorr is stronger, but this is inherent to the measurements and is not indicative of any film differences. However, the relative strength of the Al(111)-peak to the other Al-peaks is larger for the 1 mTorr sample.

The two samples showed further differences after annealing, as seen in figure 4.11. The blue color of the silicon is dominant for the sample #a-Si12, while a magenta hue has replaced most of the blue color from silicon for sample #a-Si13. Only sample #a-Si13, with an aluminum film deposited at 1 mTorr Ar pressure, had Si[111] after annealing, as seen in figure 4.12, indicating that the sputter deposition pressure is of great importance for the diffusion mechanism in the AIC process. The XRD scan of #a-Si13 after etching is found in figure D.2 in the appendix, and shows similar results as other kish graphite samples. The Al(111)-peak is the only peak altered by the etching process.

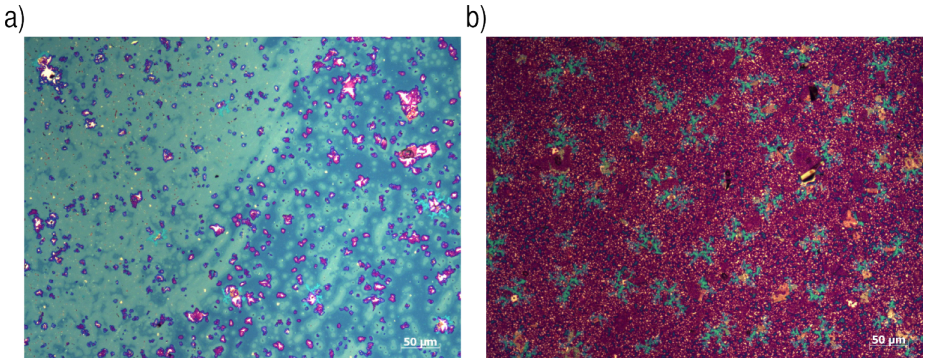

Figure 4.11: Optical images of samples a) #a-Si12 and b) #a-Si13 after annealing. The films were deposited under 3 mTorr and 1 mTorr Ar pressure, respectively.

Table 4.2: Observed Al sputter deposition rates with varying DC-field strength and pressure.

Pressure	DC power	Rate
1 mTorr	250 W	1 Å/s
	400 W	1.7 Å/s
3 mTorr	300 W	1 Å/s

Al films were also sputtered at two different rates. The rate is a result of the DC-field strength, and table 4.2 shows the deposition rates found during these experiments. Aluminum was deposited at a rate of 1.7 Å/s under 1 mTorr Ar pressure for sample #a-Si14. The sample had similar characteristics as sample #a-Si13 after annealing and etching, indicating that the deposition rate is not critical for the AIC process.

Kish graphite on GaAs substrates

Kish graphite was deposited on a GaAs(111) wafer for the EDX measurements on the Al and Si thin films after etching, to remove the dominating signal from a Si substrate. 50 nm aluminum was sputtered at a rate of 1 Å/s under an Ar

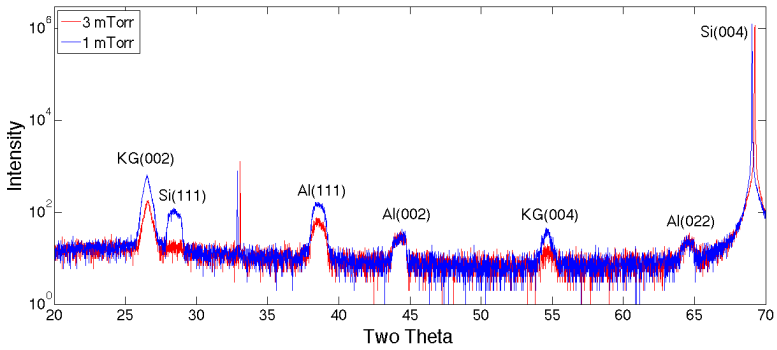

Figure 4.12: XRD scans of samples #a-Si12 and #a-Si13 after annealing. The films were deposited under 3 mTorr and 1 mTorr Ar pressure, respectively.

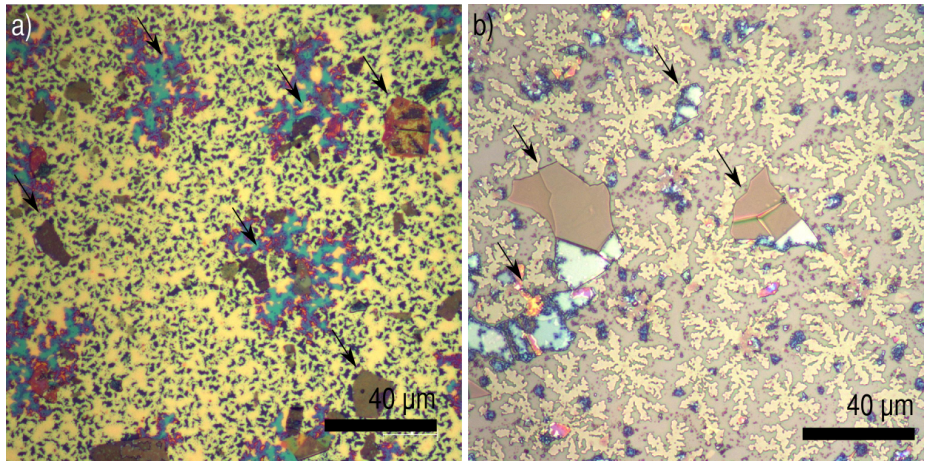

Figure 4.13: Dendrites formed after annealing on a a) KG/SiO_2 and b) KG/GaAs substrate. Arrows point to kish graphite flakes.

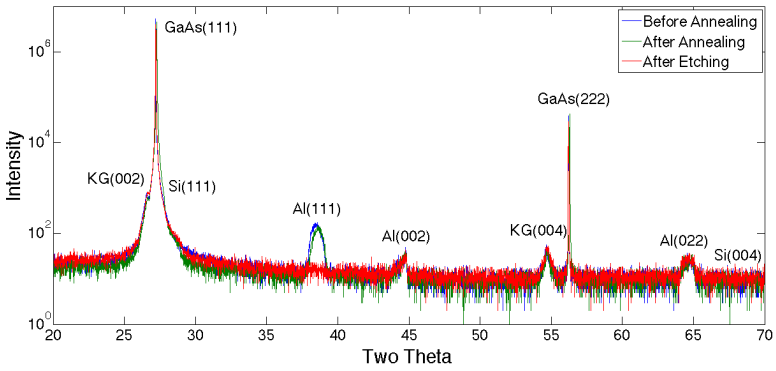

Figure 4.14: XRD scans during the AIC process of sample #a-Si16, with kish graphite on a GaAs substrate. The GaAs(111)- and Si(111)-peaks overlap.

pressure of 1 mTorr, before 20 hours of oxidation and e-beam evaporation of 30 nm silicon for sample #a-Si16. The sample was annealed at 470°C instead of 500°C with flowing N_2 gas to guarantee that no arsenic evaporated during heating. An XRD scan taken prior to annealing revealed the presence of [111]-, [001]- and [011]-oriented aluminum, with the Al(111)-peak being about one order of magnitude stronger than the other two. The XRD scans of sample #a-Si16 can be found in figure 4.14, and show that the GaAs(111)- and Si(111)-peak overlap.

The sample was very similar to identically processed samples with Si/SiO_2 substrates after annealing, but had more homogenous dendrites as shown in figure 4.13. The dendrites also grew on the substrate surface and not only around the kish graphite flakes. The elemental composition of these dendrites was mapped by EDX, and the results are summarized in figure 4.15. The EDX results show that silicon is present as dendrites both on the graphite and on the substrate in 4.15b), and that there is a much higher concentration of Si than Al in the spectrum in figure 4.15e). Figure 4.15d) further shows that there is a higher concentration of Al in the dendrites than on the substrate, and that there is less Al on the graphite surface than on the substrate.

The atomic % of each element can be calculated by the Bruker Esprit software which is used to do the EDX scans. The background signal is removed and the peaks are deconvoluted before the weight and atomic percentages are measured. For sample #a-Si16 in figure 4.15 the atomic percentage of Al/Si was

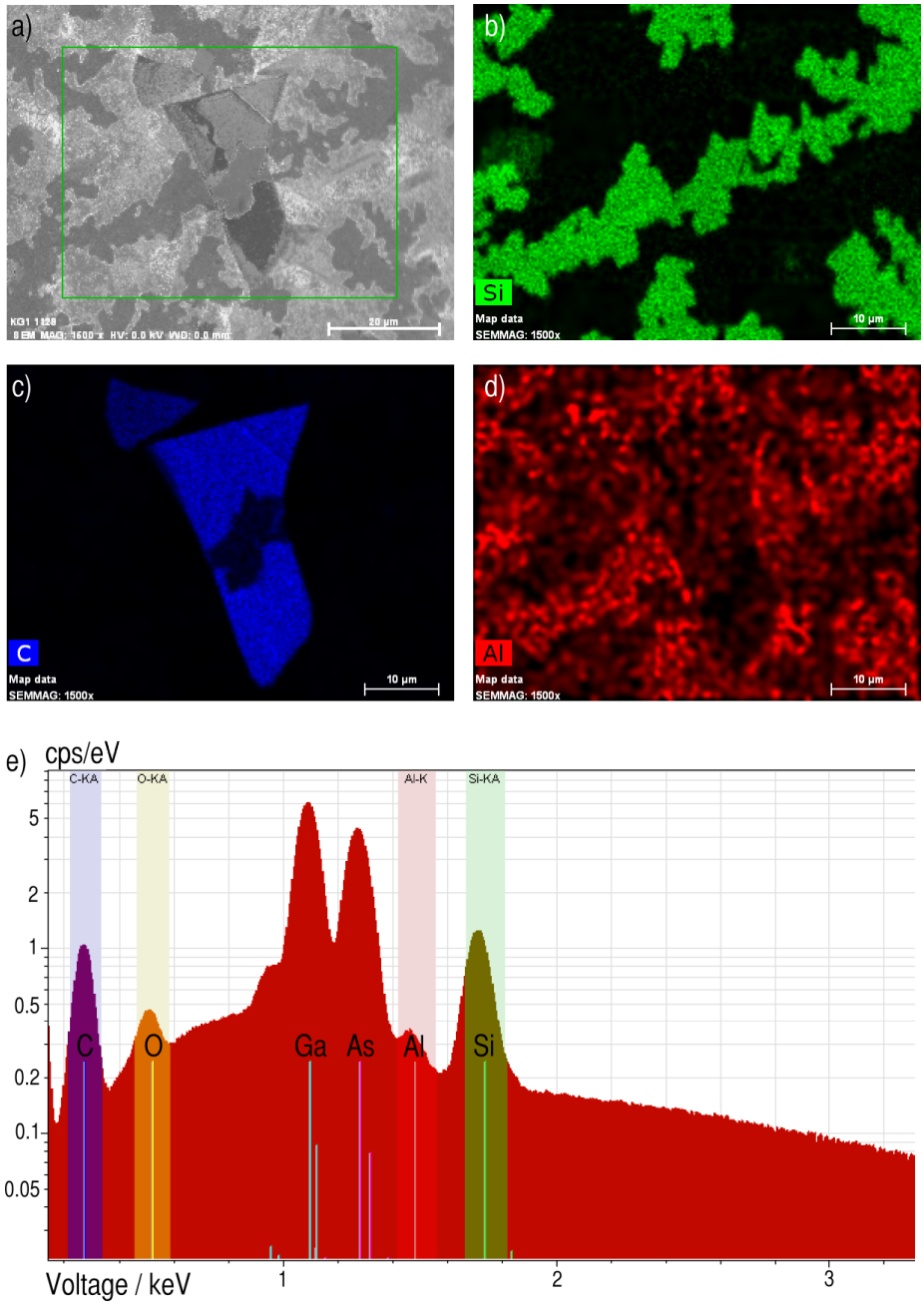

Figure 4.15: EDX mapping of sample #a-Si16 at 5 kV. a) shows the area examined, while mapping is done for b) silicon, c) carbon and d) aluminum. e) shows the spectrum of the sample. All scale bars are 10 μm except for a) which is 20μm.

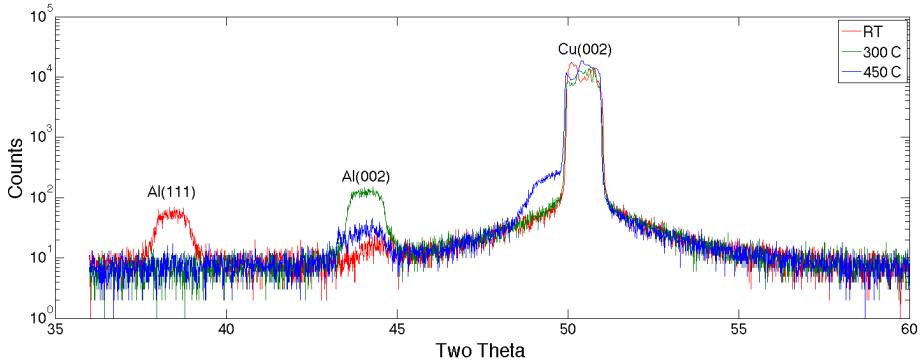

Figure 4.16: XRD analysis of graphene on copper substrates with AJA e-beam aluminum. 50 nm Al was deposited at all samples at 1Å/s, but at different substrate temperatures.

found to be $4.42 \pm 0.15\%$. The raw data that are the basis for this calculation can be found in figure D.3 in appendix D.

4.2.3 Graphene substrates

This section describes results required from single-layer graphene samples. The samples consist of graphene on copper or glass substrates.

The dependency of aluminum orientation on deposition temperature was investigated with AJA e-beam deposition on graphene substrates. The results are shown in figure 4.16. There are major differences between the aluminum orientation at the various temperatures. At room temperature, a (111)-peak is dominating and there is a weak (002)-peak. The (111)-peak is completely missing at higher temperatures. At 300°C, the Al(002)-peak is dominating, but this peak is a lot weaker at 450°C. Further more, the substrate peak changes nature from 300°C to 450°C, indicating that the crystal structure of copper is affected at higher temperatures. The shoulder of the Cu(002)-peak is most likely from copper alloying with the aluminum. SEM images of these samples revealed dendrite formation in the aluminum as the temperature was increased, shown in figures 4.17b) and c). Figure 4.17a) shows the aluminum surface after e-beam deposition at 20°C, and a periodic pattern of spheres can be seen, which are enlarged in the inset.

The first graphene samples omitted transferring the graphene from the orig-

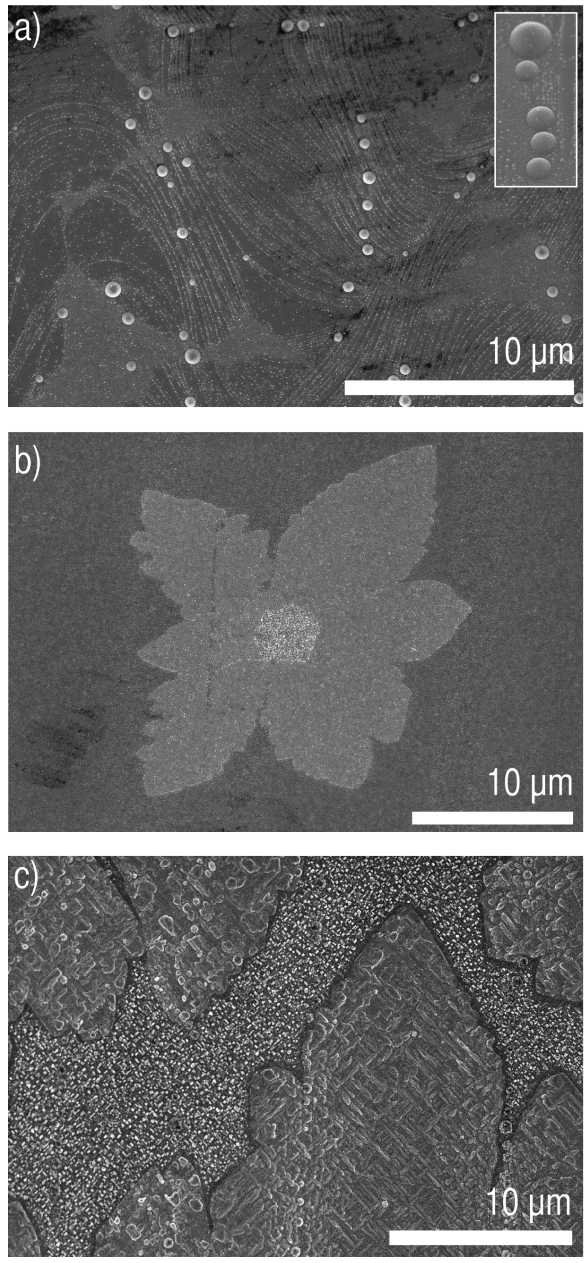

Figure 4.17: SEM images of graphene on copper substrates with AJA e-beam aluminum. 50 nm Al was deposited on all samples at 1 Å/s, with a temperature of a) 20°C, b) 300°C and c) 450°C. The inset in a) shows a zoomed in image of the dots seen in the main image.

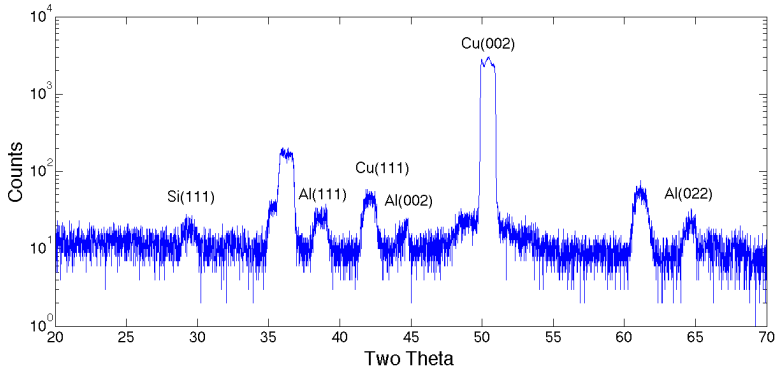

Figure 4.18: XRD analysis of graphene on a copper substrate with 15 nm AJA e-beam aluminum and 10 nm amorphous Si. The sample was annealed at 500°C for 15 h. Two peaks, at 36.4° and 61.1°, do not belong to the diffraction patterns of Al, Cu nor Si.

inal copper substrate to a glass substrate before annealing. The whole AIC process was thus performed while the graphene was still attached to copper. Figure 4.18 shows the XRD spectrum of a sample with 15 nm Al and 10 nm Si deposited on a graphene-copper substrate after annealing. Si[111] is present, but the peak does not have a high intensity. Two peaks, at ∼36° and ∼61° do not belong to the diffraction patterns of neither Si, Al or Cu, indicating alloying of two or more of the constituents. The optical and SEM images in figure 4.19 further confirm that extensive copper migration has occurred.

To avoid the problem with copper migration and crystallization, samples were transferred to a glass substrate after thin film deposition but before annealing, following the procedure described in appendix C.1. A picture taken of one such sample is shown in figure 4.20. The transfer process can damage the graphene sheet and the thin films, leading to holes, tears or rough surfaces.

Both e-beam and sputtered aluminum was deposited on graphene substrates, but no sputtered samples yielded XRD measurements with high enough intensities to do an analysis. This is most likely due to the transfer process introducing a non-planar surface. Figure 4.21b) shows the XRD analysis after annealing for a sample with 50 nm AJA e-beam aluminum and 30 nm silicon. The Al(111)-peak was measured by XRD before annealing and was found to be of moderate intensity, as shown in figure 4.23. The XRD signal is weak after the anneal-

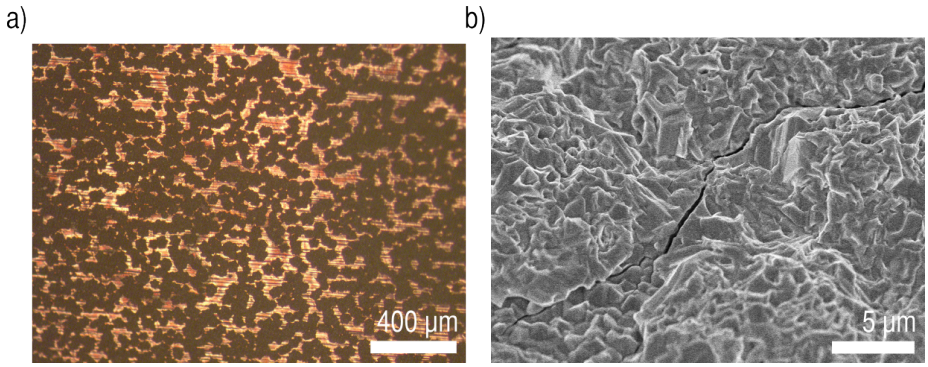

Figure 4.19: a) shows an optical image of a graphene-copper-graphene sample with 15 nm Al and 15 nm Si after annealing. b) shows a SEM image of a similar sample with 15 nm Al and 10 nm Si after annealing.

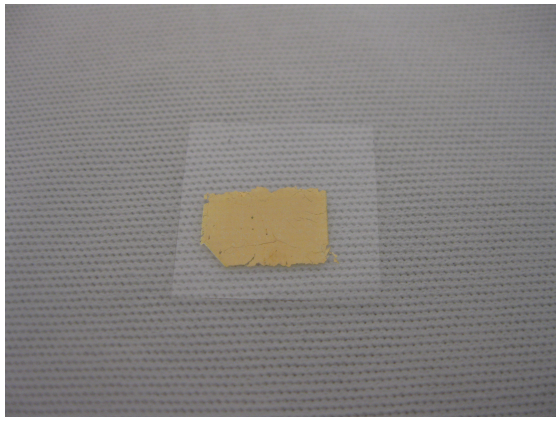

Figure 4.20: A picture taken of sample #a-Si08 after the graphene transfer process. 50 nm Al and 50 nm Si was deposited with AJA e-beam deposition while the graphene was still attached to the copper substrate. PMMA was spin-coated on, the copper was etched away and the graphene-Al-Si-PMMA sheet was transferred to a glass substrate before the PMMA was dissolved in acetone.

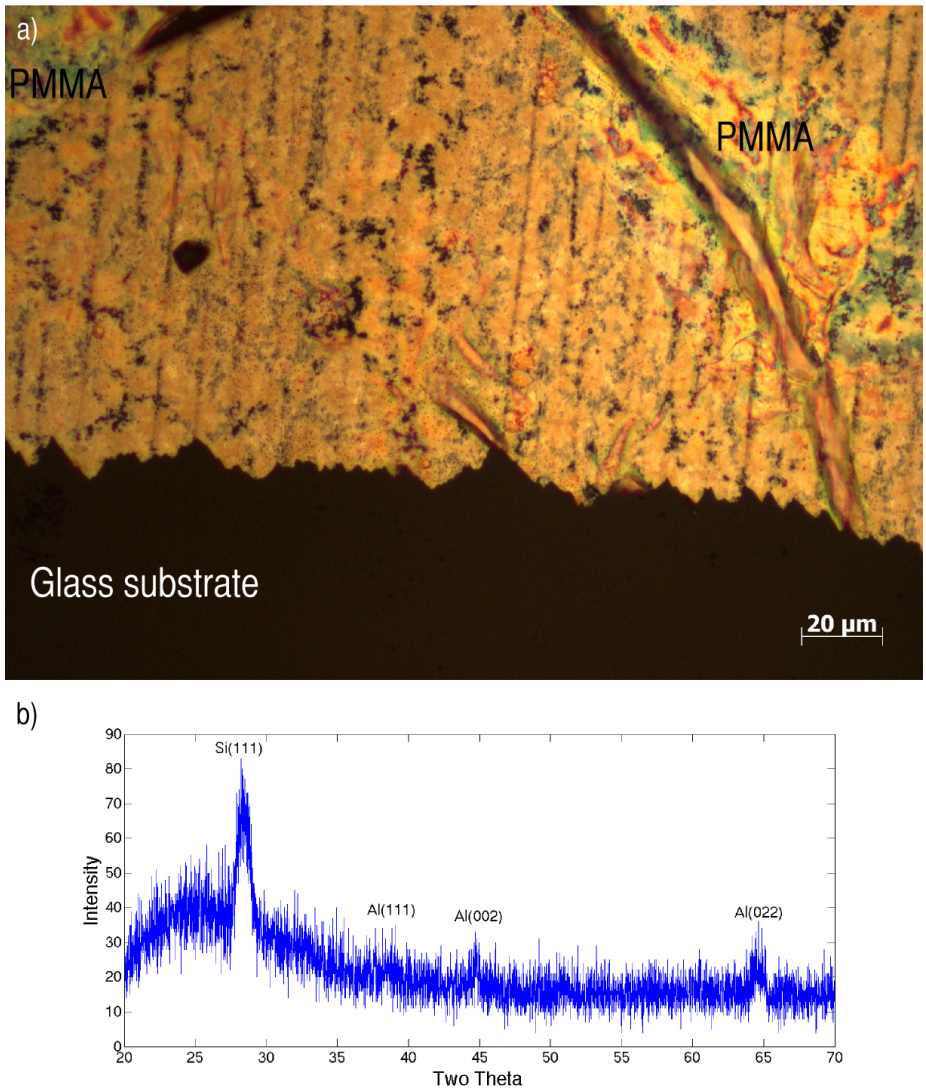

Figure 4.21: a) Optical image of a transferred graphene sample with 50 nm e-beam aluminum and 30 nm silicon after annealing and etching, where grains can be seen in the regions that are not covered with PMMA. b) XRD scan of the graphene sample after annealing for 15 hours at 500°C.

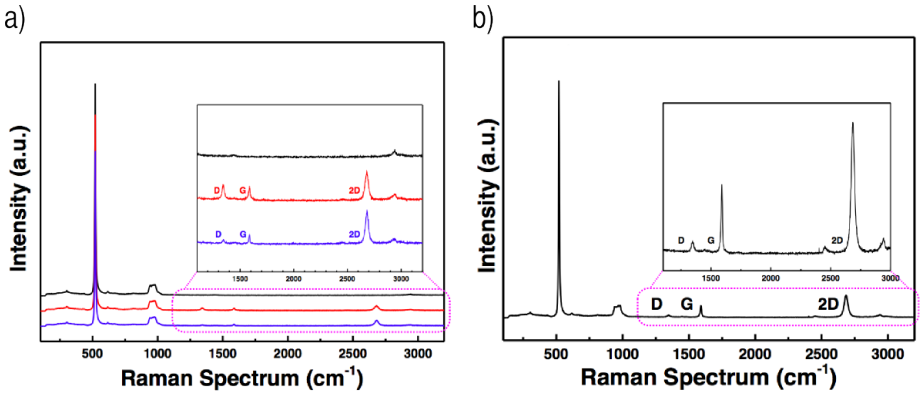

Figure 4.22: Raman spectroscopy of a) three locations on a reference sample of graphene fastened on Si/SiO_2 with PMMA, and b) graphene after sputtering aluminum on it and fastening it with PMMA on a Si/SiO_2 substrate. The peak at $\sim$500 cm^{-1} originates from the silicon substrate, while the small peak at $\sim$3000 cm^{-1} is from the PMMA.

ing step, and this could be attributed to the transfer process from a copper to glass substrate, which introduces wrinkles and roughnesses in the graphene-Al-Si sheet. Some remnants of PMMA was also present after the transfer step, and this contributed to an incomplete etch. The sample was partly removed during the etching process, by rinsing it with water, which meant that XRD measurements were not possible as the sample was not big enough. An optical image of the remnants of the sample after etching is shown in figure 4.21a), and shows that grains have formed during the annealing step.

To check if sputtering would damage the graphene, Raman spectroscopy was used to check graphene samples with and without sputtered Al. A thin layer of Al, with a thickness of $\sim$1.5 nm, was sputtered on the graphene and a transfer process was performed. This process is described in section C.3. The samples were then sent to Sejong University in South-Korea, along with a reference sample, and the results are shown in figure 4.22. Both graphs show a D, G and 2D peak for the areas with graphene. The relative intensities do not differ much, meaning that the relative sizes G/2D and D/2D are similar.

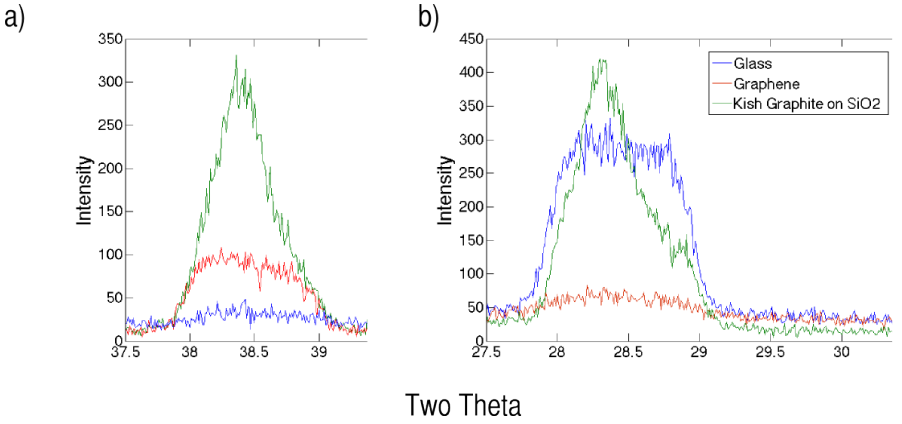

Figure 4.23: 50 nm Al was deposited on different substrates at room temperature by e-beam deposition with 1Å/s deposition rate, and the Al(111)-peak is shown in a). b) shows the Si(111) peak after annealing.

4.2.4 Comparison of the different substrates

The three different substrates were loaded into the AJA e-beam deposition chamber at the same time, and 50 nm Al was deposited with a deposition rate of 1 Å/s on all samples simultaneously. The Al(111)-XRD peak at 38.47° was investigated for the three samples and the result is shown in figure 4.23a). The peak intensities may vary from measurement to measurement, but significant differences can still be seen between the samples. An almost complete absence of the Al(111)-peak is seen for the glass substrate, while the peak is stronger for the kish graphite and graphene samples. What is interesting to note is that all of the samples represented in figure 4.23a) produced Si[111] after annealing, shown in 4.23b). The Si(111)-peak has a lower intensity for graphene than the other substrates, most likely to due to the transfer step performed before annealing.

The position of the various XRD peaks for the thin films of aluminum and silicon were measured by finding the mean 2θ-value at FWHM, and the results are summarized in table 4.3. An uncertainty of $\pm 0.1°$ is inherent to the measurements, but the results show a clear trend where the (002)- and (222)-peaks are shifted to a lower 2θ angle than the reference value, with the maximum shift being $-0.52°$ and $-0.6°$ respectively. The Si(111)-peak deviates with a maximum of $\pm 0.07°$ and the Al(111)-peak is within $+0.23°$ of the reference

Table 4.3: Measured XRD peak positions for Al- and Si- thin films deposited at RT.

		Measured peak position			
Substrate	Aluminum type	Si(111)	Al(111)	Al(002)	Al(022)
Glass	Pfeiffer e-beam	∼28.4	-	∼44.5	∼64.5
	AJA e-beam	28.4	38.6	-	-
	Sputter	28.43	38.66	-	-
KG on Si	Pfeiffer e-beam	-	-	44.25	64.5
	AJA e-beam	28.4	38.5	44.2	64.5
	Sputter	28.44	38.55	44.2	64.56
KG on GaAs	Sputter	28.37	38.62	44.59	64.62
Graphene	AJA e-beam	28.5	38.7	44.5	64.6
	Sputter	-	38.5	-	-
Reference values		28.44	38.47	44.72	65.10

value. The peaks did not change position before and after annealing for the same sample.

A summary of the parameters tested on the various substrates is shown in tables B.1 and B.2 in appendix, together with a qualitative analysis of the XRD results in table B.3.

4.3 Si[111] dot array patterning with electron beam lithography

A pattern of silicon dots was prepared by a combination of EBL patterning and the AIC process established in section 4.2. The dot size of the pattern is governed by the voltage, current and exposure time of the electron beam when using one-shot exposure which is described in section 2.4. Figure 4.24 shows the resulting dot size when varying the mentioned parameters, found during previous work[94]. The patterning was done on a kish graphite on GaAs substrate, to enable EDX characterization of the Al/Si dots without signal disturbance from the substrate. The process is described in detail in section 3.2.2.

Initial tests revealed that the electron resist(ER) thickness was crucial for

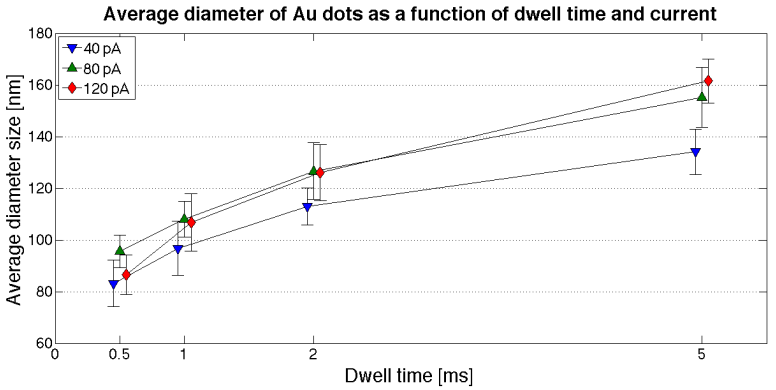

Figure 4.24: The diameter of Au dots after lift-off, when patterned by EBL at 30 kV.

the patterning process. A thin 950k PMMA A2 ER of about 60 nm thickness led to dots comprised of 15 nm Al and 10 nm Si patterned on graphite being removed during lift-off, while the dots on the GaAS substrate remained. This is due to aluminum's lower adhesion to graphite. The aluminum was deposited by sputtering, which has a conformal sputtering profile. Using a resist with an undercut can improve the lift-off in such cases. Two layers of resist were therefore used; first a layer of 200k PMMA A3 of 110 nm thickness, with a layer of 60 nm 950k PMMA A2 on top. By use of this two-step ER coating, patterns of dots with diameters of ∼80-120 nm were made with high yields both on kish graphite and substrate.

The dots with 15 nm Al and 10 nm Si had low EDX signal intensity, so sample #a-Si17 was patterned with 20 nm Al and 20 nm Si to improve on the signal intensity. When used to nucleate nanowires, the silicon layer should be thinner, but for EDX measurements a certain thickness is required to get a high enough signal intensity. SEM images and EDX measurements after annealing and after etching are shown for sample #a-Si17 in figures 4.25-4.28. After annealing, the sample had a characteristic bright circle at the edges of each dot as seen in figure 4.25a)-b). The dots were ∼115 nm, ∼130 nm and ∼150 nm in diameter after 1, 2 and 5 ms exposure. The area with the largest dots had a bigger yield than the area with the smallest dots, differing from almost ∼100% for the largest dots to ∼70% for the smallest dots. Figure 4.26 shows EDX measurements of sample #a-Si17 after annealing. The Al and Si composition

along a line is mapped for three dots and one dot in 4.26a)-b). The graphs show that there is approximately the same amount of Al and Si in the dots, but that the Al has concentrated at the edges of the dot, explaining why each dot has a bright ring. The spectrum taken from the centre of one dot, shown in figure 4.26c), shows an Al/Si concentration of 26.5%. The quantitative results can be found in figure D.4 in the appendix.

The same measurements were done after etching the sample in 25% HCl to remove the aluminum, and these results are found in figures 4.27 and 4.28. The GaAs substrate appeared damaged after etching, and contamination could be found on the surface of the kish graphite. The dots were ∼90 nm, ∼110 nm and ∼125 nm in diameter after 1, 2 and 5 ms exposure, so they had all diminished in size compared with the diameters measured before etching. Figure 4.28 shows EDX measurements of sample #a-Si17 after etching. The Al around the edges of the dots has mostly vanished, but the Al content in the middle of the dot is not so different from that before etching, as seen in figure 4.28b)-c). The Al/Si concentration in the middle of one dot is calculated to 27.95%. The quantitative results can be found in appendix D figure D.5.

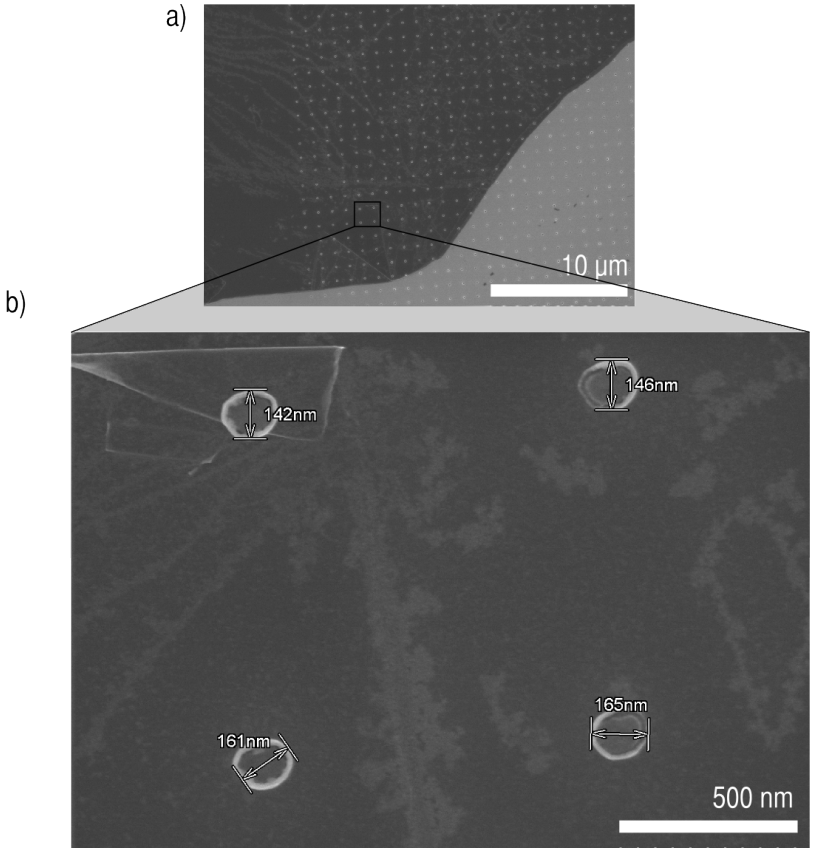

Figure 4.25: SEM images of a) the yield and b) dot sizes of sample #a-Si17, after annealing, for an area where each dot is the result of 5 ms exposure time.

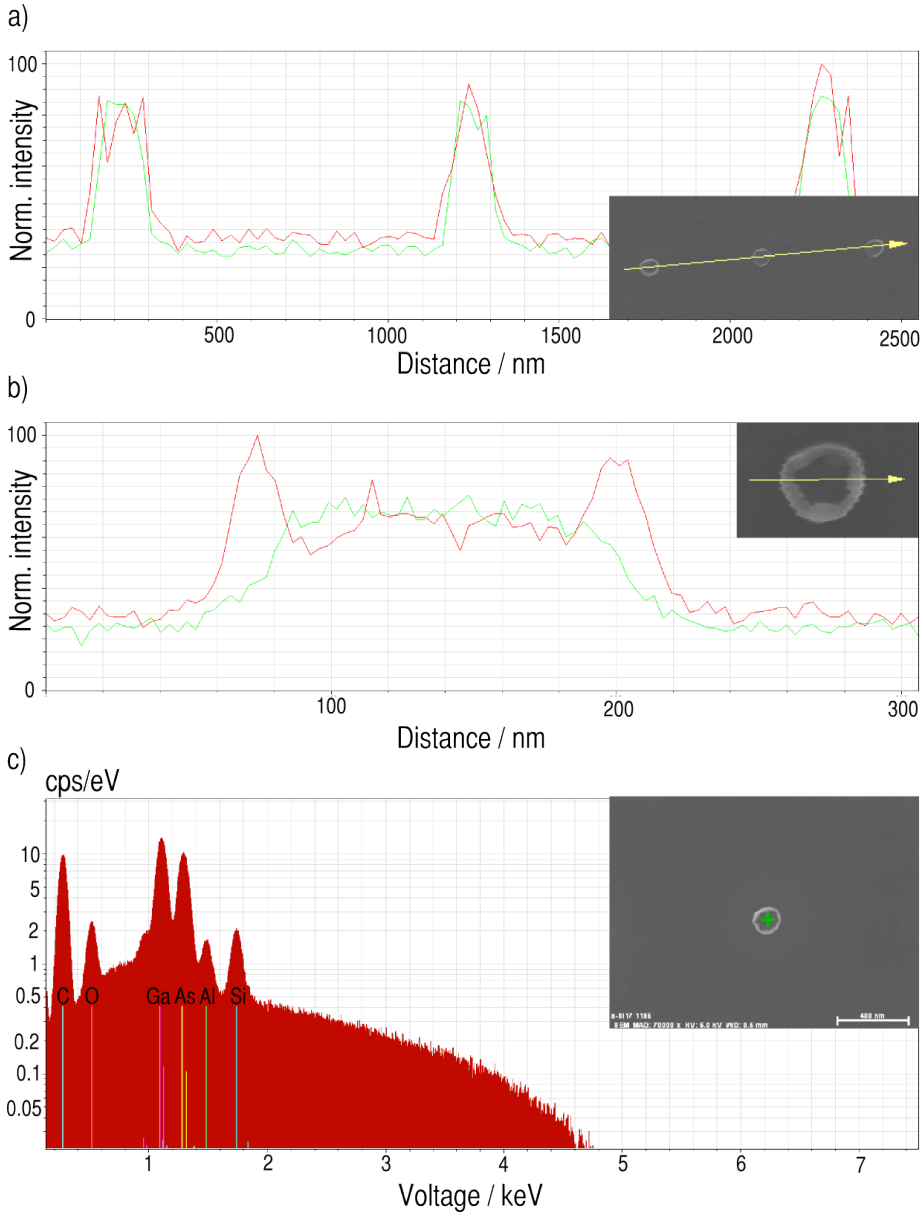

Figure 4.26: EDX measurements on sample #a-Si17 after etching. The Al/Si composition of a) three dots and b) one dot is measured and c) the spectrum of one dot is shown. In a) and b), aluminum is represented by the red line and silicon is represented by the green line.

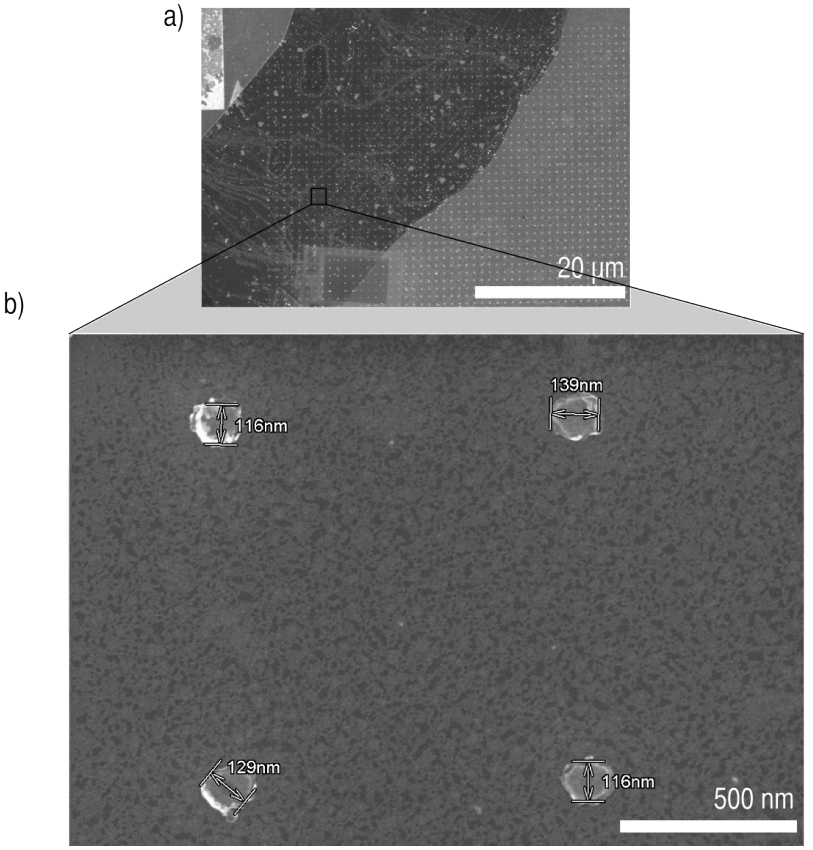

Figure 4.27: SEM images of a) the yield and b) dot sizes of sample #a-Si17 after etching. The area shown contains dots which are the result of 5 ms exposure time.

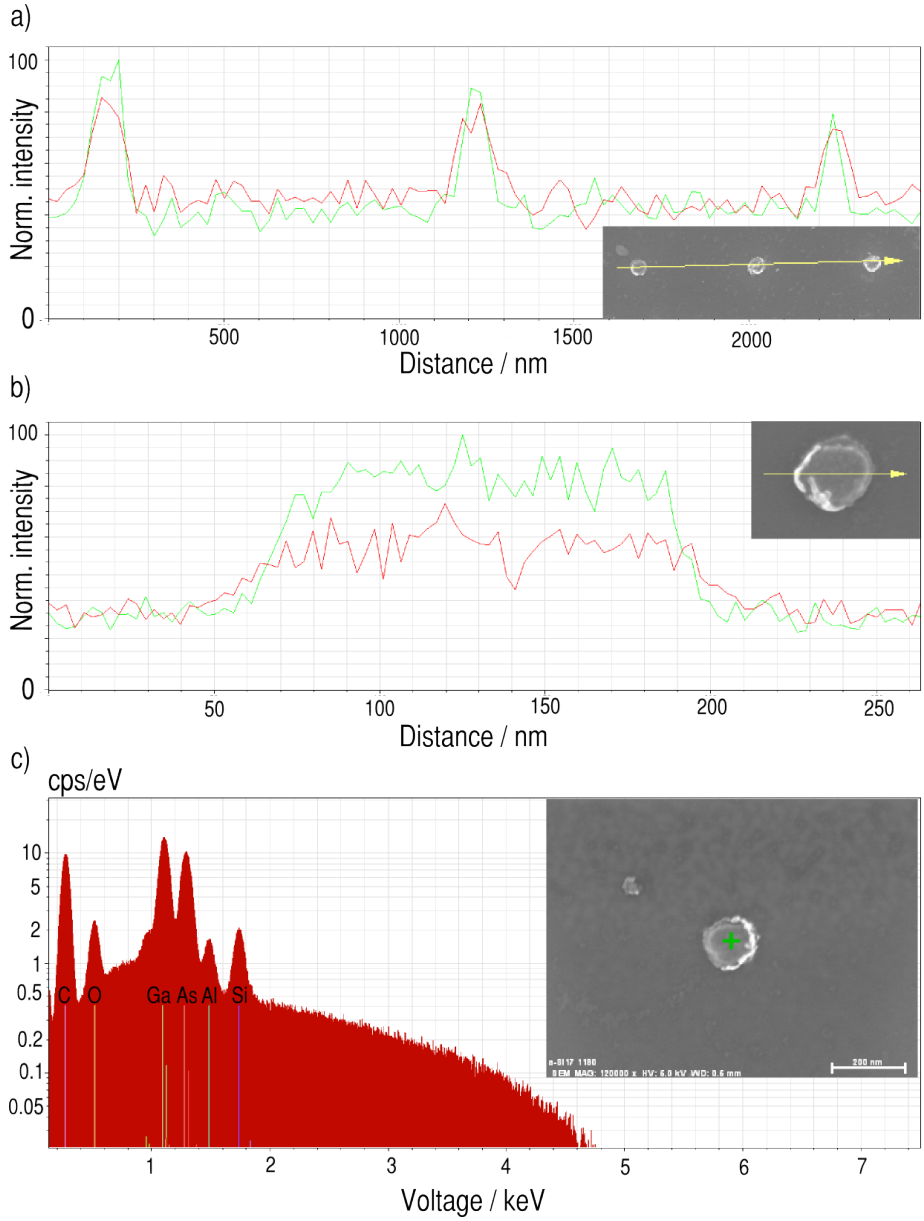

Figure 4.28: EDX measurements on sample #a-Si17, after etching, of the Al/Si composition of a) three dots and b) one dot is measured and c) the spectrum of one dot. In a) and b), aluminum is represented by the red line and silicon is represented by the green line.

Chapter 5

Discussion

The two main goals of this thesis was to explore if Si[111] could be deposited on graphene surfaces and to pattern ordered arrays of Si[111] nanodots on graphene by EBL. The starting point was to review examples of existing metal-induced crystallization processes for glass substrates, referenced in the theory chapter 2.3, and extract the conditions that were most likely to result in Si[111. The extracted parameters were then optimized on glass substrates, before doing experiments with kish graphite and graphene samples. This chapter discusses the process development and how varying the experimental parameters affected the outcome, before the outlook of using the developed process in photovoltaics is described and discussed. The findings are compared to relevant results from other groups when possible, but literature is not always available as the field of semiconductor-graphene hybrid structures is novel.

The thesis work is related to previous work in the nanowire group, especially by Mazid Munshi[9][32] and Susanne Sandell[16] in 2012-2013. M. Munshi demonstrated the growth of GaAs nanowires on graphene, while S. Sandell looked at the possibility of patterning graphene by using oxide hard masks. The work of S. Sandell was further continued in the fall of 2013, were size-controlled patterning of oxide hard masks on graphene was demonstrated[94]. It was during this project work that D.C. Kim had the idea of using Si[111] as nucleation sites for GaAs nanowires. It was evident that the low yield of nanowires on graphene was the limiting factor in realizing graphene-nanowire photovoltaics, and this thesis addresses said limitation.

5.1 Aluminum-induced crystallization

Aluminum and silicon thin films were used in an AIC process that produced Si[111] films on glass, kish graphite and graphene substrates. Several deposition methods and parameters were tested to gain an understanding of the process and optimizing it.

5.1.1 Effect of Al deposition parameters

All of the films studied in these thesis were very thin(< 100 nm), which according to literature favors a [111]-orientation of the crystallized silicon[64][65], as does oxidation of the aluminum layer[54][61]. Most groups use glass or other amorphous substrates when investigating the AIC process. As no studies are published on AIC of Si on graphene substrates, it was not clear upon starting what the influence of using graphene and kish graphite substrates would be on the AIC process.

There were large differences between aluminum films deposited by sputtering and e-beam evaporation, and also between aluminum films deposited with the two different e-beam systems available in the NTNU NanoLab. The aluminum deposited by AJA e-beam had no Bragg-peaks when deposited on glass, [111]-orientation on graphene, and all peaks were present when deposited on kish graphite. The sputtered aluminum showed a preferential [111]-orientation on glass and graphene substrates, but showed several orientations when deposited on kish graphite. The [111]-orientation of sputtered aluminum is in agreement with literature, as the sputter yield of face-centered cubic(FCC) materials like Al varies with crystal orientation as $S_{(111)} > S_{(001)} > S_{(001)}$[95].

There are two main differences between the two e-beam evaporation systems. The first is that the vacuum is higher for the AJA e-beam than for the Pfeiffer e-beam. The second difference is an experienced increase in radiation heat during the e-beam deposition for the Pfeiffer system. This might be why all deposition methods except Pfeiffer e-beam aluminum on kish graphite samples led to crystallized Si[111].

The effect of deposition rate

The deposition rate was kept at 1Å/s for most depositions to allow for the comparison of other parameters. The deposition rate is a result of the applied power to the electron beam or sputter field. During e-beam Al deposition on samples #a-Si08-#a-Si10, the deposition rate oscillated rapidly between 0.5 and

2 Å/s, but this did not lead to any apparent differences in the resulting silicon film. Sputtering was performed at two different rates, 1 Å/s and 1.7 Å/s, and no differences could be discerned in the result.

The effect of sputter deposition pressure

Varying the aluminum sputter deposition pressure had a large effect on the morphology and crystal orientation of the aluminum and silicon films, as seen in figures 4.10-4.12. The microstructure of sputtered thin films is related to the mobility of the sputter target adatoms during growth, which increases with increased temperature and pressure[96, p 402]. Figure 5.1 shows the relationship between argon pressure, substrate temperature and metal film morphology for metal films deposited by magnetron sputtering. In zone 1, where the substrate temperature is low and the Ar pressure is elevated, tapered crystals form and there is a rough surface. By increasing the substrate temperature or decreasing the Ar pressure a dense fibrous structure accompanied with a smooth surface is achieved in the transfer T zone. At higher temperatures, in zones 2 and 3, columnar grains form[97].

Figure 5.1 shows that the microstructure of aluminum gets finer with decreasing pressure. The melting temperature of aluminum, T_m, is 993 K[98], and if deposition is at room temperature, $T = 293K$, then $T/T_m = 0.3$, which is in the T zone for low Ar pressures. This could be part of the reason why the aluminum films deposited under different pressures had different structures after annealing. Altering the aluminum microstructure will affect the diffusion mechanism between aluminum and silicon, and might explain why an aluminum film deposited under 3 mTorr Ar pressure did not result in any [111]-oriented silicon, while an aluminum film deposited under 1 mTorr Ar pressure did.

The effect of substrate temperature on e-beam evaporated Al

Increasing the substrate temperature during aluminum deposition with e-beam evaporation led to the formation of 'leaf'-like aluminum dendrites as seen in figure 4.17, accompanied with a shift from [111]-orientation to [001]-orientation. Dendrites are normally associated with the preferential growth in a certain crystallographic direction upon solidification of a liquid. Lee et al. state that both theoretical predictions and experimental findings agree on a [001]-orientation for dendrites formed in aluminum[99], something which may explain the change in crystal orientation upon deposition at elevated temperatures.

The temperatures of the substrates were 20°C, 300°C and 450°C, which are

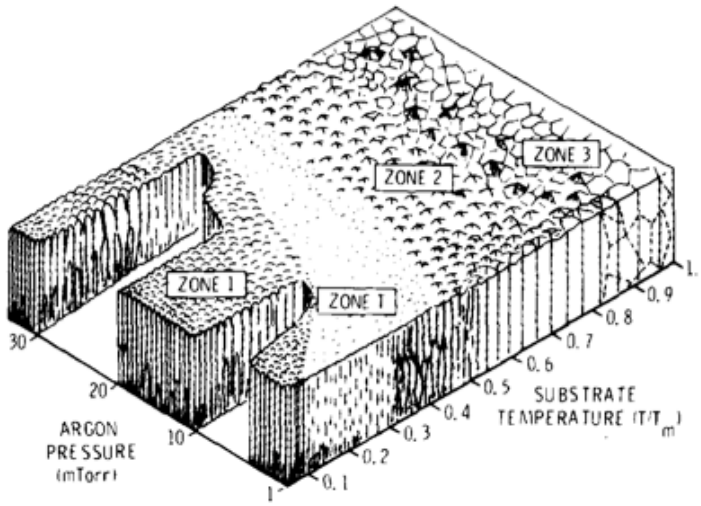

Figure 5.1: The influence of argon pressure and substrate temperature on the microstructure of a metal film deposited by magnetron sputtering. T(K) is the substrate temperature and $T_m(K)$ is the melting point of the metal film. The figure is divided in zones 1-3, with a transition zone T between zones 1 and 2. Illustration from [97].

all far lower than the melting point of aluminum at 660°C[98]. Furthermore, the XRD 2θ (002)-peak of the aluminum film deposited at 300°C was shifted to the left as seen in figure 4.16, resulting in a peak centered at 44.1° in contrast to the calculated (002)-peak of 44.72°. A 2θ (002)-peak centered at 44.1° corresponds to a lattice parameter of $a = 4.1037$ Å which is larger than the equilibrium lattice parameter of aluminum of 4.0495 Å. This could indicate a strained structure. Subsequent depositions were done at room temperature, as the Al(111)-peak intensity was highest for this substrate temperature.

Raman spectroscopy of graphene after aluminum sputter deposition

Figure 4.22 shows Raman spectroscopy of graphene after aluminum sputter deposition, and a reference sample for comparison. When analyzing the Raman spectrum of graphene, there are three relevant peaks:

- The 2D peak, which is located at $\sim$2700 cm^{-1}. The width and lineshape of this peak contains information on the number of graphene layers. For monolayer graphene, a symmetric 2D peak and a FWHM of $\sim 25cm^{-1}$ is characteristic[100].
- The G peak, which is located at $\sim$1582 cm^{-1}. The linewidth varies with the doping level of graphene[101].
- The D peak, which is located at $\sim$1350 cm^{-1}. This peak is related to defects, and the intensity is a measure of short-range disorder[102].

Further more, the ratio G/2D is dependent on charge carrier concentration and polarization[101]. All three peaks are present in both the reference sample and the sample with a thin layer(1.5 nm) of sputtered Al. The presence of the D-peak in the reference sample is not as expected, as this sample should contain pristine graphene and thus not have a D-peak. It is noted that the D-peak can be generated from the transfer process itself. Based on the results found here, it seems that the sputtering does not damage the graphene much as the D/G peak ratios are approximately the same for the sputtered sample and the reference sample.

5.1.2 Effect of substrate

The films deposited on glass and graphene substrates were mostly uniform both before and after annealing. The films deposited on kish graphite samples always

had dendrite-like growth occurring in regions with kish graphite flakes. This could have several explanations, such as a difference between growth conditions on the substrate and kish graphite, or that the rough surface caused by kish graphite flakes leads to dendritic growth. As kish graphite was deposited both on Si/SiO_2 and GaAs substrates, the film formation on these two substrates can be compared. Dendrites formed on both samples, but there seemed to be fewer phases present with the GaAs substrate, as well as dendrites forming both around the kish graphite flakes and on the substrate. This is shown in figure 4.13. As dendrites formed both on the KG/SiO_2 substrate, which has surfaces with crystal planes hexagonal(0001)/amorphous, and the KG/GaAs substrate were the surfaces have hexagonal(0001)/(111) crystal planes, it could be that the presence of kish graphite edges and thus dangling bonds initiates dendrite formation. The GaAs(111) substrate can also have edges intrinsically, and this might explain why dendrites form on the GaAs substrate and not the SiO_2 substrate.

EDX measurements on a KG/GaAs sample revealed that the dendrites seen in the optical microscope consisted mostly of silicon, as seen in figure 4.15. There was a higher concentration of Al in the dendrites than in other areas, and there was a lower concentration of Al in the dendrites on kish graphite than on the GaAs substrate. Combined with the XRD scan, which showed Al(002)- and Al(022)-peaks but not the Al(111)-peak after etching, this indicates that the dendrites are an alloy of silicon and aluminum, with an Al-content calculated to $4.42 \pm 0.15\%$.

Epitaxial matching of graphene and aluminum

Nakada et. al. theoretically suggest that aluminum has a low binding energy of 1.6 eV with graphene and adsorbs preferentially at H6-sites[47], as shown in figure 2.9 in the theory section. Materials with a good lattice match can form epitaxial structures, and it is therefore interesting to investigate if any of the aluminum crystal orientations have a good lattice match with graphene and can form an epitaxial thin film. The atomic plane structures of the (001), (011) and (111) planes of aluminum, which has a face-centered cubic(FCC) crystal structure, are depicted in figure 5.2a).

The lattice mismatch can be calculated by the following formula:

$$\Delta a = \frac{a_s - a_f}{a_s} \tag{5.1}$$

where a_s is the substrate lattice parameter, in this case graphene(a = 2.46

Å), and a_f is the thin film lattice parameter, in this case aluminum(a = 4.0495 Å).

Only the (111)-plane has the same geometry as the hexagonal graphene lattice, enabling an epitaxial match. If the aluminum atoms arrange at a mixture of H6- and T-sites, a lattice match as low as 0.7% is possible. This is shown in figure 5.2b). The distance between neighboring atoms in the (111)-plane of Al is $a/\sqrt{2} = 2.8634$ Å, while the distance between the points marked with stars in figure 5.2b) is 2.84 Å. The (002)-plane of aluminum means that each Al atom is separated by a distance of 2.85Å. This leads to a lattice mismatch of 0.7% in the x-direction and 16.3% in the y-direction if the atoms arrange as shown in figure 5.3a). For the (022)-plane, the mismatch is 0.7% in the x-direction but 17.7% in the y-direction as shown in figure 5.3b). Based on these calculations, Al[111] has the best match for an epitaxial deposition on graphene, which was actually observed in the deposition of Al at room temperature(figure 4.16). However, this involves aluminum occupying both H6- and T-sites, and according to Nakada et al.[47] it is not a very stable configuration, as aluminum has a low binding energy of 1.6 eV at H6-sites and a lower binding energy at T-sites. Also, the observation of the Al(002)-peak on graphene with high temperature e-beam deposition could be related to not only the crystal lattice matching, but the [001]-oriented dendrite formation at elevated temperatures[99] as discussed before.

Hillocks, or copper lumps, were observed before and after aluminum was deposited on graphene, and are shown in figure 5.4b). Images taken with a SEM revealed hillocks in the shape of spheres and hemispheres which had a diameter of around 500 nm. Hillocks form due to the strain on the copper from the graphene overlayer[103]. Because of their large size compared with the 50 nm aluminum thin film, they remain on the substrate throughout the process, and together with the copper steps they might affect the lattice matching of Al with graphene. The hillocks were big enough to be observed in an optical microscope, and arranged in periodic patterns according to the steps of the copper substrate. Nucleation of graphene at copper steps is shown in figure 5.4a), and copper steps can be observed in the optical image in figure 5.4b). The hillocks were still present after etching the aluminum, and this could contaminate the final silicon film.

5.1.3 Effect of Al orientation

It is not clear how the orientation of aluminum affects the orientation of the post-annealing silicon film, or even if this is the most important parameter.

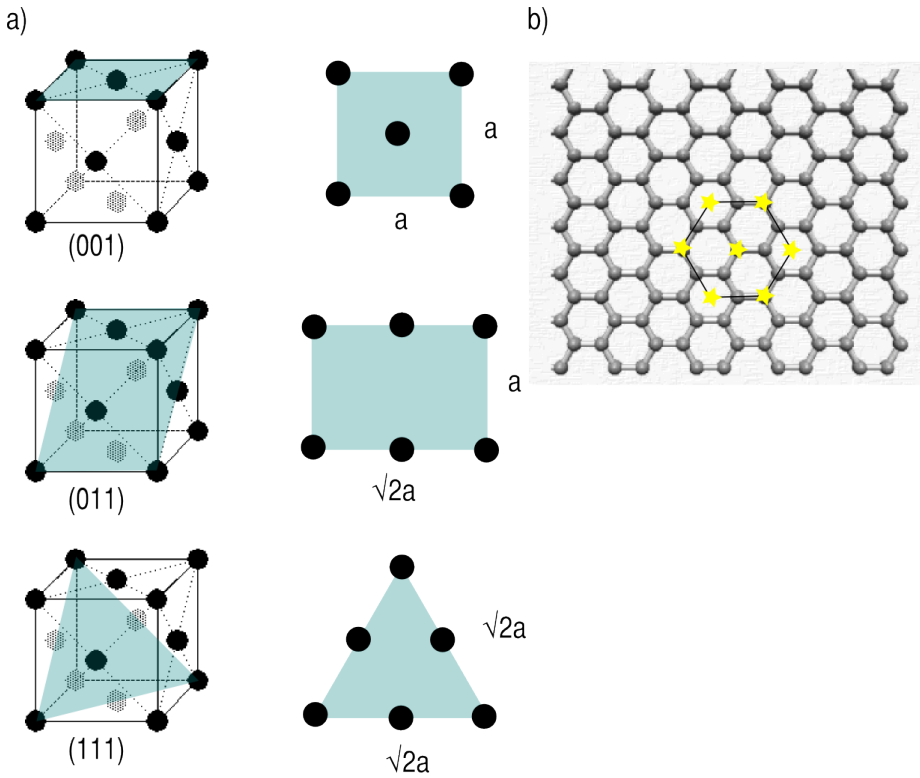

Figure 5.2: a) Crystal lattice and lattice planes in a fcc structure, where a is the lattice constant. b) shows a possible epitaxial configuration for the Al(111)-plane on graphene.

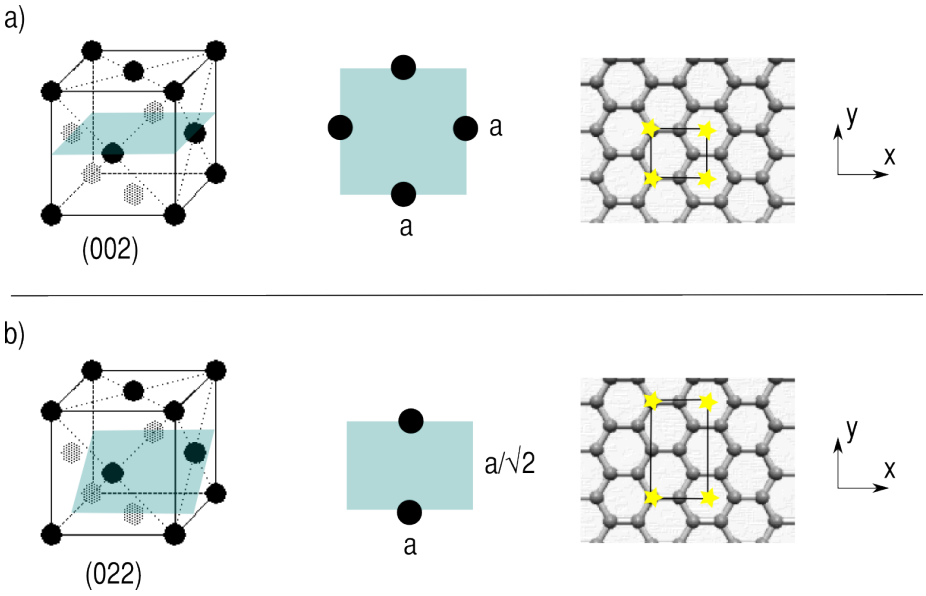

Figure 5.3: Crystal lattices and the a) (002)-plane and b) (022)-plane for a fcc structure, where a is the lattice constant. Possible epitaxial configurations for planes on graphene are also shown.

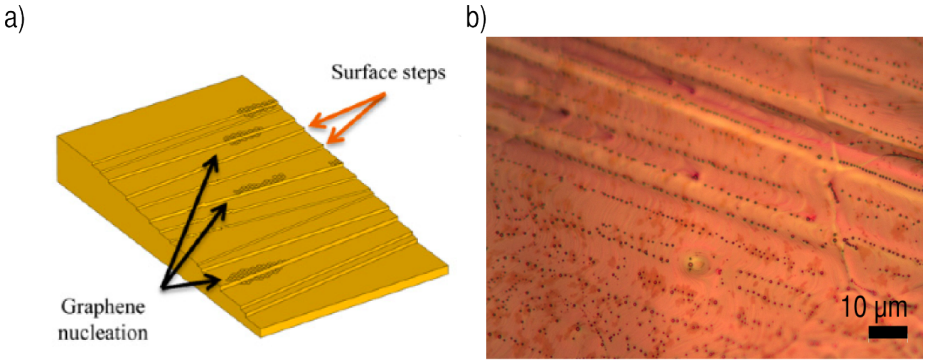

Figure 5.4: a) Schematic of graphene nucleating at copper steps. b) Copper steps and hillocks observed in the optical microscope after CVD growth of graphene. Adapted from [104].

The annealing and etching of AJA e-beam aluminum and silicon on glass led to a Si[111] thin film almost free of aluminum, although no aluminum XRD-peaks were detected in the pre-annealing scan. A weak Al(111)-peak could be detected after annealing. The deposition of e-beam aluminum deposited with a Pfeiffer system had very weak or non-existing Si(111)- and Al(111)-peaks after annealing, both on glass and kish graphite samples, but the (002)- and (222)-peaks of aluminum could be detected. The only conclusion one can draw from these results is that Al[111] is not an absolute requirement for a Si[111] phase, it could be that the absence of Al[001] and Al[011] is more important.

An indication that [111]-oriented aluminum plays a larger role in the AIC process than other orientations is that it is the only orientation changing noticeably upon etching of the aluminum. This is seen by the XRD scans in figure 4.8c). The Al(111)-peak has almost disappeared after the etching of aluminum, while the other aluminum peaks are as strong as before etching. This can be perceived as the Al[111] phase being the only aluminum transported to the surface of the sample during the layer exchange process. Another possible explanation would be a difference in etch rates for the various crystal planes. The surface atomic density of the crystal planes for aluminum increases as (011)<(001)<(111). It has been shown that the corrosion rates for a 3M solution of HCl, which is equivalent with a weight percentage of 10.4%, scale inversely with the density of the crystal planes[105]. Thus, the (111)-plane should have the lowest etch rate. The etching time applied here is fairly long, 45 minutes, so planes with a slow etch rate would be affected by the long immersion in the etchant in the case of plane-specific etching. This indicates that the [002]- and [022]-oriented aluminum has not exchanged position with the Si, or is present as an Al/Si alloy.

The EDX measurements support this notion. The Al-content after etching is spatially mapped in figures 4.9c) and 4.15e) for two samples with SiO_2 and GaAs substrates. Both images show a tendency of a higher aluminum concentration in the dendrites. Further more, figure 4.15e) shows the overlapping of high intensity regions of Al and Si. XRD measurements of the same samples verify that the Al[111] has been removed by the etching process and only Al[001] and Al[011] remains. It is therefore suggested that dendrite formation occurs in areas with Al[001] and Al[011].

Peak shifts of Al(002)- and Al(022)-XRD peaks

Peak shifts can have several origins, as for example very small crystallites or strain. A peak shift to a lower 2θ value means a larger lattice plane spacing

d, and vice versa. For thin films, a shift to a lower angle is also an indication of tensile stress, while a shift to a higher angle is an indication of compressive stress. The peak shift will be more pronounced for peaks at a higher angle, as evidenced by the relationship established by differentiating Bragg's Law:

$$\frac{\Delta d}{d} = -\Delta\theta \cot\theta \tag{5.2}$$

The measured 2θ values for the Bragg peaks of Si, Al and KG are shown in table 4.3. For the peak shifts observed here, the deviation is most evident for the Al(002)-peak of kish graphite on Si/SiO_2 substrates and the Al(022)-peak on all substrates. The first is shifted with $\Delta\theta_1 = -0.5°$ and the second is shifted with $\Delta\theta_2 = -0.5{\sim}0.6°$, which corresponds to a shift in lattice plane spacing $\Delta d_1 = 0.0215$ Å and $\Delta d_2 = 0.0029{\sim}0.0035$ Å. This corresponds to a deviation from the lattice parameter $a = 4.0495$ Å of 1.06% and 0.2∼0.24%, respectively. From these calculations, it is apparent that the Al[001] grains in films deposited on kish graphite samples experience the most tensile stress.

Tensile stress can occur as a result of a mismatch between the lattice constants of the deposited thin film and the substrate, or a difference in the thermal coefficients of the substrate and film. To accurately determine the amount of stress in the thin film, a residual stress XRD analysis should be applied.

5.1.4 The morphology of the silicon film after aluminum etching

The AIC process was done to completion for the glass substrate shown in figure 4.4 and the graphene substrate in figure 4.21, bot resulting in a semi-continuous silicon film after etching the aluminum. Silicon grains between 20 and 100 μm had formed, consisting of subgrains with an average size of 11 μm, something which is similar to what other groups performing AIC on glass substrates have achieved[54][69]. The silicon grains grew in a fractal manner in agreement with literature[51][17].

5.1.5 EBSD characterization

EBSD measurements were performed on several samples, but valid results were only achieved for a thin Si film on a glass substrate. The main limitation was acquiring strong enough Kikuchi lines from the thin films of Al and Si. Lines could be discerned for Si, but not Al, even after plasma etching the Al surface to decrease roughness. As the films were 30 nm thick for Si and 50 nm thick for

Al, it might be advantageous to use thicker films to ensure that the material to be examined is thicker than the interaction volume of the electron beam with the sample.

EBSD measurements require very flat surfaces, and it is suspected that the rough surface morphology introduced by the kish graphite flakes effectively hindered imaging with EBSD. However, it should be possible to image Si thin films on graphene, based on the results acquired with Si on glass.

5.2 Si[111] dot array patterning with electron beam lithography

The results obtained from the AIC process on kish graphite and graphene in sections 4.2.2 and 4.2.3 showed that the final silicon film grew either in a dendritic manner or as a semi-continuous film. If a sample with a thin film of Si[111] or Si[111] dendrites was put in the MBE chamber to grow GaAs nanowires, it would result in a random arrangement of nanowires with varying densities. A continuous silicon film covering the graphene electrode could also lead to significant leakage from the final photovoltaic device. Growing ordered arrays of nanowires is an advantage both for the processing and solar conversion efficiency of the photovoltaic, and this can be achieved by patterning kish graphite or graphene with a Al/Si dot array, where each dot will function as a nucleation site for a GaAs nanowire. In an actual device, an oxide hard mask should be deposited on top of the graphene, which isolates the individual nanowires and the graphene electrode. The patterning and AIC process could then be performed after the deposition of the hard mask. The proposed scheme is illustrated in figure 5.5. To prove this concept, an Al/Si dot array was deposited directly onto a piece of kish graphite.

5.2.1 Dot array dimensions and pattern yield

The dots were designed to have a diameter of 95, 110 and 130 nm, by using the previously optimized EBL parameters for one-shot exposure in figure 4.24. The resulting dot diameters after etching were ∼90 nm, ∼110 nm and ∼125 nm for 1 ms, 2 ms and 5 ms exposure to the 30 kV/40pA electron beam, which confirms the high reproducibility of the developed EBL process. However, before etching the dots were significantly larger, ∼115 nm, ∼130 nm and ∼150 nm, due to the presence of an aluminum ring. The increased dot size is due to the combination of a two-layer resist and sputtering. As the bottom layer of resist

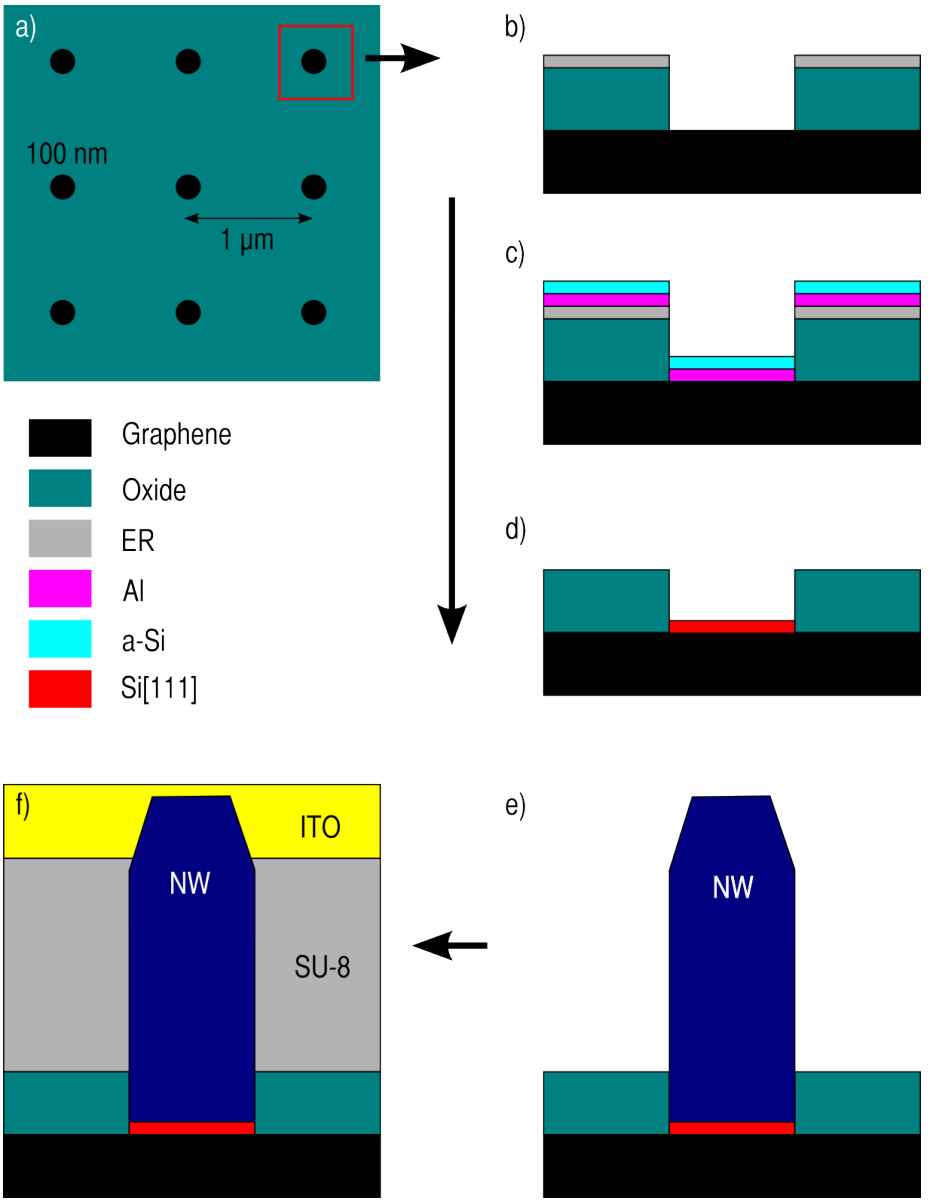

Figure 5.5: The AIC process can be incorporated in the process route of a nanowire solar cell. First, (a) a graphene substrate with an oxide hard mask is patterned by EBL, and the crossection is shown in (b). Al and Si are deposited (c). After lift-off, annealing and etching of Al, Si[111] is formed (d). High-yield, vertical nanowires are grown in the holes, on top of a thin layer of Si [111] (e). An insulating layer of SU-8 and a top contact (e.g. ITO) are deposited (f).

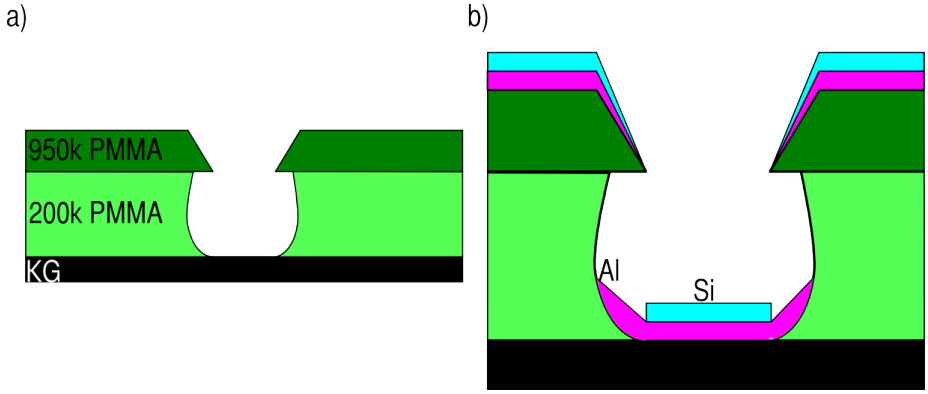

Figure 5.6: The deposition profile with two layers of electron resist is shown in a), and the corresponding deposition profiles of sputtered Al and e-beam Si are shown in b).

has a lower molecular weight, it will dissolve more readily upon exposure to the electron beam than the top layer of higher molecular weight. This leads to an etching profile as visualized in figure 5.6a). Sputtering is a conformal deposition method, meaning that it covers the side walls of the electron resist as well as the patterned area. The expected result of sputtering aluminum before depositing e-beam silicon in a concave hole pattern is shown in figure 5.6b), and would explain the aluminum ring seen in the experiments.

The area patterned with large dots(125 nm), had a higher yield than the area patterned with small dots(90 nm). This could be due to the edge profile proposed in figure 5.6. For smaller features, there will be more ER covering the side walls relative to the amount covering the substrate than for larger features, increasing the chance of feature removal upon lift-off. A possible solution to this problem is to use e-beam aluminum, which has a more anisotropic deposition profile without any deposition on the ER side walls.

One-shot exposure

A technique developed by us, termed 'one-shot exposure', was used to pattern the kish graphite sample. In stead of raster scanning every dot with the electron beam, the beam is programmed to settle for several milliseconds, resulting in a circular feature due to the scattering of the beam. The resulting pattern does

not differ from one exposed by conventional methods, the important parameter in this context is time. During the fall of 2013, we showed that a large area of 1 x 1 mm could be patterned with dots 1 μm apart, in less than one hour by using one-shote exposure. Using the fastest conventional exposure, the same process would take 5-6 hours.

5.2.2 Etching of aluminum

The SEM images in figure 4.27 show that substantial contamination has occurred during the etching process of aluminum with 25% HCl with KG/GaAs substrates. EDX measurements indicated that the contamination particles were not made up of silicon, aluminum nor carbon but had a high concentration of oxygen, suggesting that they have formed by degradation of the GaAs substrate. HCl is known to etch oxide formed on GaAs but not the substrate itself[106]. As the substrate also appeared damaged, it is likely that the GaAs oxide has been etched by HCl acid, introducing stray particles that contaminate the kish graphite surface. Contamination after etching was not observed with other substrates, like Si/SiO_2 and glass. Using one of these substrates with the AIC process would therefore be beneficial.

The EDX measurements done on individual dots showed little or no change in Al/Si ratio before and after etching with HCl to remove aluminum. Layer exchange is a consequence of the crystallization of silicon, and these results indicate that layer exchange has not occurred or that the Al and Si form an alloy which has not been affected by the HCl treatment. If layer exchange has not occurred, we would expect the bottom layer of Al to be etched and thus removing the top layer of silicon. As this was not the case, alternative explanations must be sought.

Samples #a-Si16 and #a-Si17 were identically processed, except for the patterning step applied to sample #a-Si17. The EDX measurements done on sample #a-Si16 are shown in figure 4.15, and the Al/Si ratio is very low after etching, at about 4.4%. The corresponding value for #a-Si17 is 28%. It must be stressed that even though EDX measurements were done for several dots for each sample, only one dot was used to extract the ratio data. The deviation between dots is therefore not known, but a side note is that dots within the same sample appeared similar during EDX measurements. The trends of higher Al-content in the dots of sample #a-Si16 compared with the dendrites in sample #a-Si17 were consistent for several dots. It might be that the small feature size in sample #a-Si17 has affected the energetics of the AIC process. As mentioned previously, the aluminum forms a concave ring around the silicon upon dot

patterning with a two layer electron resist. This specific geometry might also influence the result of the AIC process.

Melting point depression is a phenomenon where the melting point of a material is lowered with the reduction of material size. Nanoscale materials can melt at temperatures hundred of degrees lower than their bulk counterparts[107]. For Al, the melting temperature is lowered with 4 K for spheres 46 nm in diameter and 13 K for spheres 11 nm in diameters[108]. The Al nanostructures used in the patterning are roughly 20 nm high and 100 nm wide. It seems unlikely that the Al should melt, but one cannot exclude the possibility that eutectics are formed more easily on the nanoscale, accounting for the higher Al-content in Si found in the nanostructures compared with the thin films. Further investigations are necessary to try and understand the silicon crystallization for the dot array pattern.

5.2.3 Implications for the electronic properties of the graphene substrate

To the extent of our knowledge, there is no literature discussing the potential modulation of graphene's electronic properties by the presence of Al-doped silicon dots. However, similar systems have been fabricated and documented. Lee et al. showed that pure silicon islands 1-3 nm in height and 20-50 nm wide evaporated onto graphene by CVD actually increased the hole mobility with a factor of two, from $\sim 360 cm^2 V^{-1} s^{-1}$ to $\sim 780 cm^2 V^{-1} s^{-1}$. The maximum current increased with a factor of three as well, when comparing graphene covered with silicon islands with pristine graphene. They explain their findings with the silicon islands recovering defects in the graphene, like Stone-Wales defects, vacancies of carbon atoms and line defects at grain boundaries[109]. The same arguments are used for parasitic InAs islands formed with InGaAs nanowire arrays. It is claimed that the parasitic growth is actually beneficial, and the conductivity of graphene had a two-fold increase after island deposition. A proposed explanation is that the islands form alternative charge carrier pathways at graphene scattering centers[6].

Tai et al. have investigated the effect of a dense array of 35 nm high and 60 nm wide c-Si/Ni dots on the electronic properties of graphene. They used pulsed laser deposition(PLD) for the deposition of Ni and Si, and found that the incorporation of ions in the graphene crystal lattice during deposition increased the D-peak in the graphene Raman spectrum, which is a sign of increased defects, and blue-shifted the G- and 2D-peaks, which is a sign of strain. They found that the maximum current decreased by a factor of 5 and that the hole mobility

was decreased from $62cm^2V^{-1}s^{-1}$ to $43cm^2V^{-1}s^{-1}$. They attribute the losses to the incorporation of defects in graphene from the pulsed laser deposition process[110].

As Al-doped silicon will have holes as majority charge carriers, it is expected that the presence of these structures will increase the hole mobility in graphene, as observed by Lee et al[109]. The results of Tai et al.[110] on Si/Ni-dots on graphene indicate that to achieve an improvement of the electronic properties of graphene, and not a degradation, the deposition methods used for the metal and silicon layer should be as non-invasive as possible. Electron-beam evaporation is thus a good candidate for the deposition of Al. It is also valuable to know if sputtering introduces defects to the graphene layer, and the Raman results from Sejong University in figure 4.22 suggest that the sputtering of Al does not damage the graphene too much.

Chapter 6

Conclusions

The formation of Si[111] on glass, kish graphite and graphene substrates below the Si crystallization temperature has been demonstrated. A process involving AIC on these three substrates has been developed, which to the extent of our knowledge is the first time AIC has been demonstrated on graphene. This can be an important step towards the realization of photovoltaics comprised of self-catalyzed GaAs nanowires on graphene substrates. The following list summarizes the most important findings of the present work:

- An annealing time of 15 hours, at 470-500°C, is sufficient to achieve silicon crystallization with AIC.
- Both e-beam evaporated and sputtered aluminum can result in a Si[111] structure if the deposition parameters are optimized.
- AIC of silicon on glass substrates resulted in 20-100 μm silicon grains, consisting of subgrains with an average size of 11.16 μm.
- Thin film deposition of aluminum on exfoliated kish graphite substrates leads to multi-orientation of the Al film, independent of deposition method and parameters.
- Al[111] is the only crystal orientation removed by HCl etching, indicating that this orientation would be the only one active in a layer exchange process.
- The Al-content in the Si[111] film after the etching of aluminum was found to be 4.4% for a sample with kish graphite on a GaAs substrate.

- Patterning of aluminum and silicon with the previously developed EBL one-shot exposure technique on a few-layer graphene surface was demonstrated, resulting in a high yield dot array with a controllable diameter size of 80-160 nm. The dots were found to have an Al/Si ratio of 28% after etching the aluminum.
- A process-route for the incorporation of AIC in the development of GaAs nanowire-graphene solar cells has been suggested.

Further work

Two main studies should be done following the work of this thesis:

- A study of the effect of Si[111] nanodots on nanowire yield, and optimizing the MBE process with these dots.
- Characterization of how the deposited silicon structures affect the electronic properties of graphene and kish graphite.

The first point should be addressed by preparing multiple samples of kish graphite/graphene substrates covered with a hole-patterned oxide hard mask with silicon dots in the holes. The effect on nanowire yield of varying the silicon thickness and hole diameter should be studied. In addition, the MBE process must also be tuned by varying the deposition temperature to try and achieve a higher density of nanowires and less parasitic growth.

The second point is more straightforward. Samples of kish graphite/graphene substrates with and without silicon dots should undergo four-probe measurements to determine the effect of the silicon structures on the sheet resistance and mobility of graphene. This could be done by for example van der Pauw probing measurements. Raman spectroscopy can be used with the graphene substrates to identify a possible increase in graphene defects and doping introduced by the AIC process.

In addition, it would be interesting to study the crystal structure of very thin/small silicon features on graphene, something which could be done by TEM. It might even be possible to look at the interface between the two materials, to see how the silicon atoms arrange themselves on the graphene.

Si island evaporation

CVD grown graphene should be used to test this technique, to eliminate the possibility of forming carbon structures from tape residues, as was seen with the kish graphite samples. However, it might be that the CVD chamber in the NTNU NanoLab does not provide high enough pressures for a successful deposition of Si islands, and that the evaporation step must be carried out elsewhere. It is also possible to try high T e-beam evaporation of Si with the AJA international system.

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Appendices

Appendix A

Preliminary results

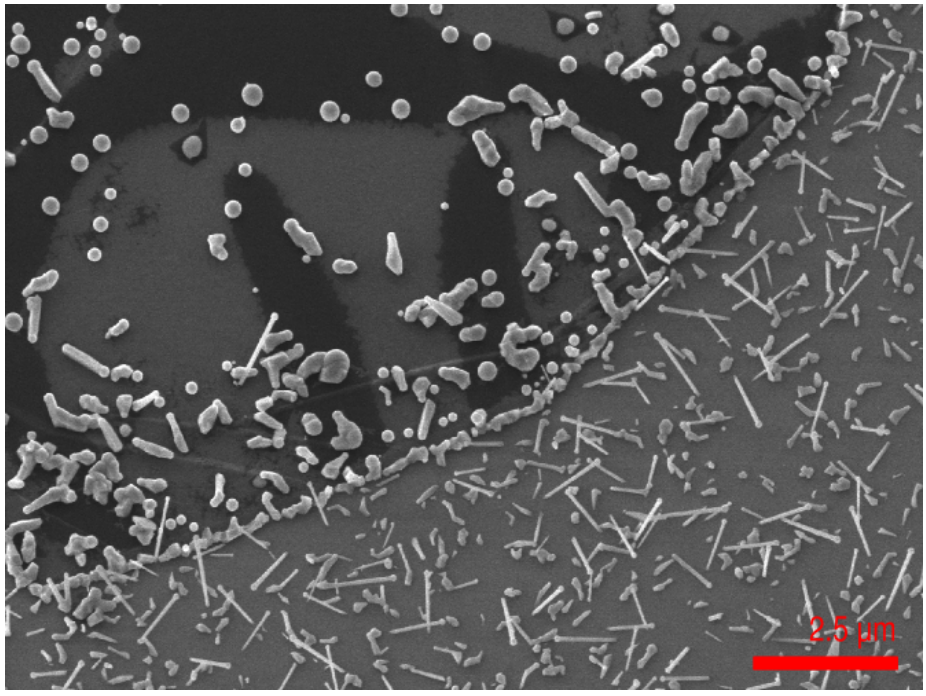


Figure A.1: SEM image of GaAs nanowires grown on graphene during my project work in the fall of 2013. A thin layer of amorphous silicon was deposited on a KG/SiO_2 substrate at high T, and randomly oriented NWs are mostly observed on the Si/SiO_2 substrate part. Also the surface of the kish graphite suggests no significant deposition of Si there.

Appendix B

Sample summary

Table B.1: Selected glass and kish graphite samples with deposition parameters for e-beam and sputtering processes. d = thickness.

Sample	Substrate	d_{Al}	Deposition details	d_{Si}	Annealing
#G-1	Glass	50	Sputter, AJA 1 Å/s, 3 mTorr 24 hr ambient O_2	30	500°C, 15 hr
#G-2	Glass	50	E-beam, pfeiffer 1 Å/s 24 hr ambient O_2	30	500°C, 15 hr
#G-3	Glass	50	E-beam, AJA 1 Å/s 24 hr ambient O_2	30	500°C, 15 hr
#a-Si04	KG	10	E-beam, Pfeiffer 1 Å/s 20 min $\sim 10^{-3}$ mbar O_2	15.5	500°C, 15 hr
#a-Si07	KG	10	E-beam, Pfeiffer 1 Å/s 20 hr ambient O_2	15	500°C, 24 hr
#KG-Al	KG	50	E-beam, AJA 1 Å/s 20 hr ambient O_2	30	500°C, 15 hr
#a-Si10	KG	50	E-beam, AJA 0.5-2 Å/s 20 hr ambient O_2	30	500°C, 40 hr
#a-Si12	KG	50	Sputter, AJA 1 Å/s, 1 mTorr 20 hr ambient O_2	30	500°C, 15 hr

Table B.2: Selected graphene and kish graphite samples with deposition parameters for e-beam and sputtering processes. d = thickness.

Sample	Substrate	d_{Al}	Deposition details	d_{Si}	Annealing
#g-Cu1	Graphene	15	E-beam, AJA 1 Å/s 20 hr ambient O_2	15	500°C, 15 hr Cu migration
#g-Cu2	Graphene	50	E-beam, AJA 1 Å/s 20 hr ambient O_2	30	500°C, 15 hr
#a-Si08	Graphene	50	E-beam, AJA 0.5-2 Å/s 20 hr ambient O_2	-	500°C, 20 hr
#a-Si15	Graphene	50	Sputter, AJA 1.7 Å/s, 1 mTorr 20 hr ambient O_2	30	500°C, 15 hr
#a-Si16	GaAs	15	Sputter 1 Å/s 20 hr ambient O_2	50	470°C, 15 hr
#a-Si17	GaAs	15	Sputter 1 Å/s 20 hr ambient O_2	50	470°C, 15 hr

Table B.3: Selected samples with qualitative XRD results.

Sample	XRD analysis	Etching results
#G-1	Pre annealing: Al(111) Post annealing: Al(111) and Si(111)	Not performed
#G-2	Pre annealing: No peaks Post annealing: Al(002), Al(022) and Si(111)	Not performed
#G-3	Pre annealing: - Post annealing: Al(111) and Si(111)	Only Si(111)
#a-Si04	Pre annealing: - Post annealing: Al(111), Al(002) and Al(022)	Not performed
#a-Si07	Pre annealing: - Post annealing: Al(111), Al(002) and Al(022)	Not performed
#KG-Al	Pre annealing: - Post annealing: Al(111), Al(002), Al(022) and Si(111) Post etching: Al(002), Al(022) and Si(111)	Incomplete etch
#a-Si10	Pre annealing: - Post annealing: Al(111), Al(002), Al(022) and Si(111)	Not performed
#a-Si12	Pre annealing: Al(111), Al(002) and Al(022) Post annealing: a-Si12-14	Not performed
#g-Cu1	Pre annealing: Al(111) Post annealing: Al(111), Al(002), Al(022) and Si(111)	Incomplete etch
#g-Cu2	Pre annealing: Al(111) Post annealing: Al(022) and Si(111)	Incomplete etch
#a-Si08	Pre annealing: - Post annealing: Al(002)	Not performed
#a-Si15	Pre annealing: Al(111) Post annealing: -	-
#a-Si16	Pre annealing: Al(111), Al(002) and Al(022) Post annealing: Al(111), Al(002) and Al(022) Post etching: Al(002) and Al(022)	Incomplete etch

Appendix C

Detailed process routes

C.1 Graphene transfer process for graphene-copper substrates

1. Attach sample to glass cover slide with capton tape, with the silicon surface exposed.
2. Cover sample with a few drops of A3.51 950K PMMA, use a chuck to spin coat it at 4000 rpm for 2 minutes. This leads to a PMMA thickness of ∼200 nm. Bake the sample for 2 min at 70°C to harden the resist.
3. Remove glass cover slide and capton tape.
4. Plasma etch the sample with oxygen plasma to remove the bottom layer of graphene. Use a power of 90 watts, a gas pressure of 4 mbar and etch for 2.5 minutes.
5. Etch the sample in ammonium persulfate(APS). 3 g APS with 100 mL deionized water gives an etchant of concentration 0.15M. Stir with a magnetron bar for 2 hours in a fume hood.
6. Transfer the sample to two consecutive water baths and keep it immersed during transfer.
7. Scoop out the floating sample with a glass cover slide and let it dry. Dry at room temperature for one hour and bake on a 80°C hotplate for 30 min.

8. Remove the PMMA by lift-off with acetone for more than 10 hours.
9. Let dry at RT, as any rinsing/blow-drying might damage the sample.

C.2 Patterning by electron beam lithography

1. Spin-coat sample with A3.5 200k PMMA, at 4000 rpm for 2 minutes which gives a thickness of ∼110 nm, and hard bake for 2 minutes at 180°C.
2. Spin-coat sample with A2 950k PMMA, at 4000 rpm for 2 minutes which gives a thickness of ∼60 nm, and hard bake for 10 minutes at 180°C.
3. Identification of suitable pattern positions by using a reference scribble and an optical microscope.
4. EBL exposure at 30 kV and 40μA.
5. Pattern development in 9:1 IPA:H_2O for 15 s. Rinse in water and dry with N_2. Inspection by optical microscope.
6. Oxygen plasma ashing for 12 seconds at 50 Watts and 0.33 mbar O_2 pressure.
7. Deposition of 20 nm aluminum by sputtering at 1Å/s and 1 mTorr Ar pressure.
8. Oxidation by leaving in an ambient atmosphere for 20 hours.
9. Deposition 20 nm silicon by e-beam evaporation at 1Å/s.
10. Lift-off in acetone for 10 minutes at RT to remove ER.
11. Annealing for 15 hours at 470°C.
12. Etching of top aluminum layer in 25% HCl for 45 minutes.

C.3 Sample preparation for Raman spectroscopy

A very thin film of Al was sputtered on top of a graphene-copper-graphene substrate. To be able to investigate the quality of the graphene after Al sputtering, the following process steps were performed:

1. A substrate of Si and 300 nm SiO_2 was cleaned with acetone and IPA.
2. A drop of PMMA was placed on the Si/SiO_2 substrate, and the graphene-copper-graphene-Al sample was placed on the Si/SiO_2 substrate with the Al-side down. Gentle pressure was applied to make the sample stick.
3. The sample was baked for 10 minutes on a 150°C hotplate, to harden the PMMA and improve adhesion.
4. The top layer of graphene was removed by oxygen plasma ashing for 2.5 minutes at 90 watts and 4 mbar O_2 pressure.
5. The sample was immersed in APS for ∼12 hours to etch away the copper.
6. The sample was packed and shipped to Sejong University for Raman spectroscopy.

Appendix D

AIC process optimization results

D.1 Test of effect of extended annealing for kish graphite samples

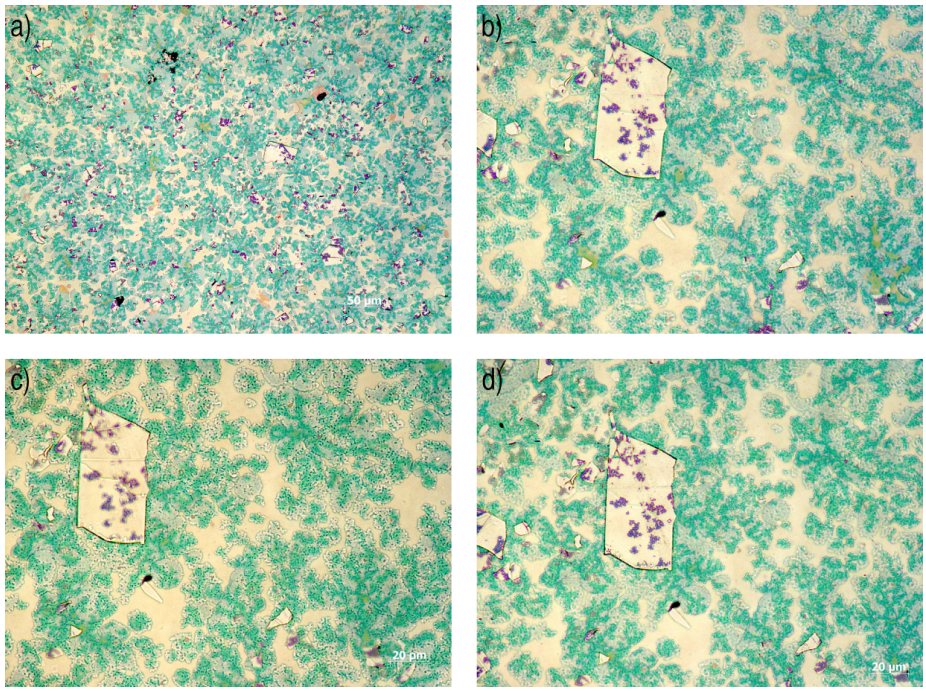


Figure D.1: Sample #a-Si10 was annealed in steps of 10 and 20 hours. The images were taken after a) 20 hours, b) 30 hours, c) 40 hours and d) 60 hours.

D.2 X-ray diffraction results

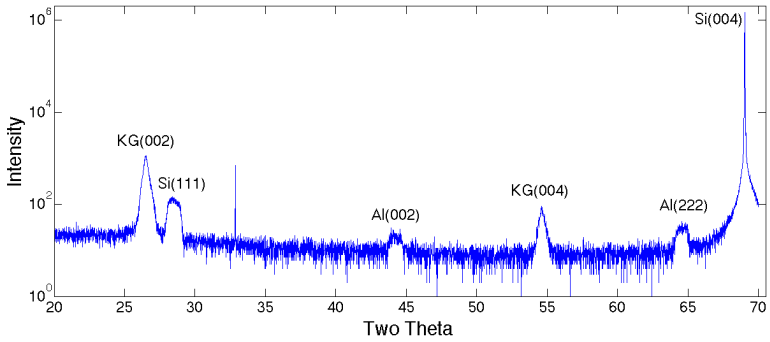
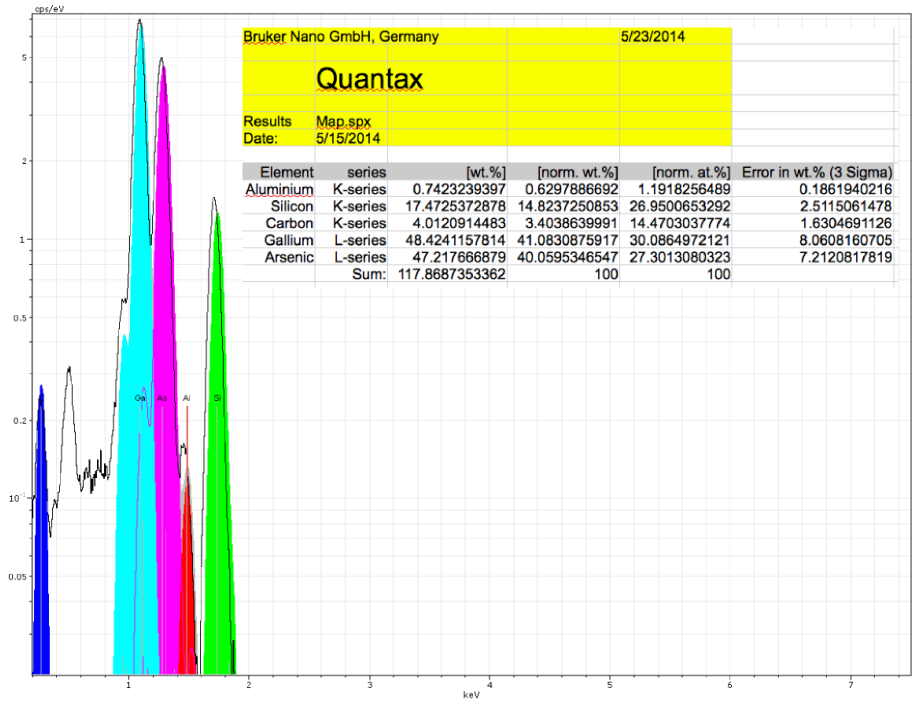


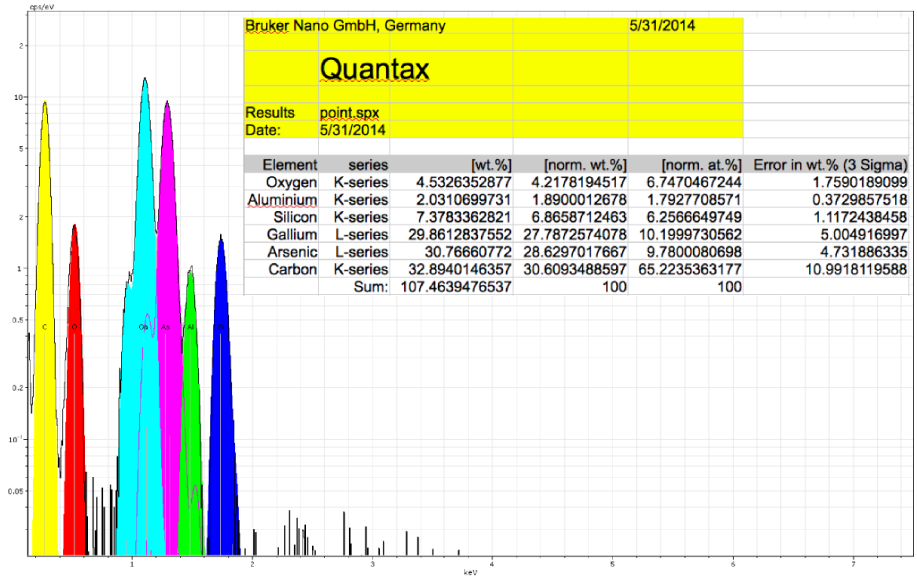
Figure D.2: XRD scan after etching of sample #a-Si13, with kish graphite on a Si/SiO_2 substrate.

D.3 Energy-dispersive X-ray diffraction results



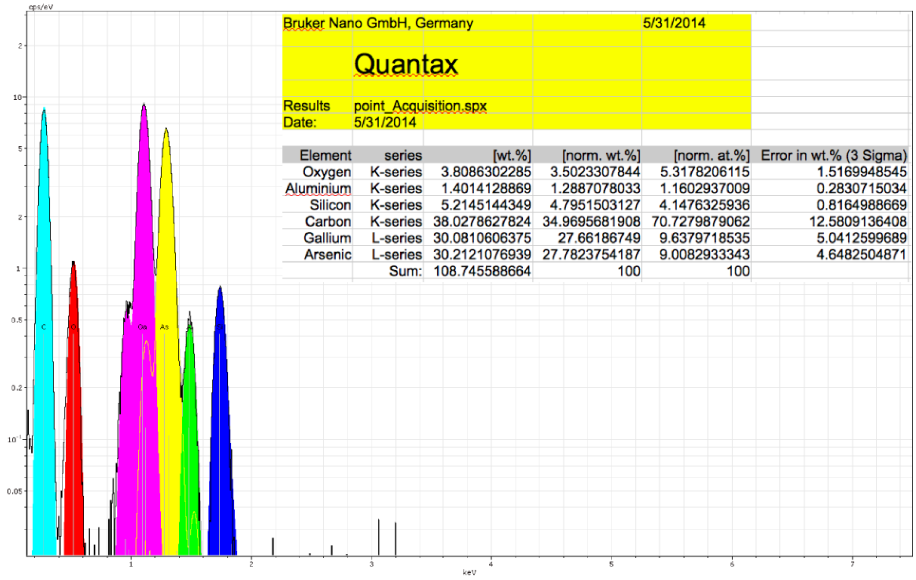
Element	series	[wt.%]	[norm. wt.%]	[norm. at.%]	Error in wt.% (3 Sigma)
Aluminium	K-series	0.7423239397	0.6297886692	1.1918256489	0.1861940216
Silicon	K-series	17.4725372878	14.8237250853	26.9500653292	2.5115061478
Carbon	K-series	4.0120914483	3.4038639991	14.4703037774	1.6304691126
Gallium	L-series	48.4241157814	41.0830875917	30.0864972121	8.0608160705
Arsenic	L-series	47.217666879	40.0595346547	27.3013080323	7.2120817819
	Sum:	117.8687353362	100	100	

Figure D.3: EDX scan of #a-Si16 after etching, with kish graphite on a GaAs substrate. The peaks have been deconvoluted by the Bruker Esprit software, and the measured values for weight and atomic percentages are shown in the insert.



Element	series	[wt.%]	[norm. wt.%]	[norm. at.%]	Error in wt.% (3 Sigma)
Oxygen	K-series	4.5326352877	4.2178194517	6.7470467244	1.7590189099
Aluminium	K-series	2.0310699731	1.8900012678	1.7927708571	0.3729857518
Silicon	K-series	7.3783362821	6.8658712463	6.2566649749	1.1172438458
Gallium	L-series	29.8612837552	27.7872574078	10.1999730562	5.004916997
Arsenic	L-series	30.76660772	28.6297017667	9.7800080698	4.731886335
Carbon	K-series	32.8940146357	30.6093488597	65.2235363177	10.9918119588
	Sum:	107.4639476537	100	100	

Figure D.4: EDX scan of #a-Si17 after annealing, with kish graphite on a GaAs substrate. The peaks have been deconvoluted by the Bruker Esprit software, and the measured values for weight and atomic percentages are shown in the insert.



Element	series	[wt.%]	[norm. wt.%]	[norm. at.%]	Error in wt.% (3 Sigma)
Oxygen	K-series	3.8086302285	3.5023307844	5.3178206115	1.5169948545
Aluminium	K-series	1.4014128869	1.2887078033	1.1602937009	0.2830715034
Silicon	K-series	5.2145144349	4.7951503127	4.1476325936	0.8164988669
Carbon	K-series	38.0278627824	34.9695681908	70.7279879062	12.5809136408
Gallium	L-series	30.0810606375	27.66186749	9.6379718535	5.0412599689
Arsenic	L-series	30.2121076939	27.7823754187	9.0082933343	4.6482504871
	Sum:	108.745588664	100	100	

Figure D.5: EDX scan of #a-Si17 after etching, with kish graphite on a GaAs substrate. The peaks have been deconvoluted by the Bruker Esprit software, and the measured values for weight and atomic percentages are shown in the insert.

Appendix E

Preliminary results of silicon evaporation

E.1 Theory

It has been shown that silicon islands growing in the [111]-direction can be deposited on graphene through chemical vapor deposition(CVD)[109]. By evaporating amorphous Si, the gaseous Si atoms can physisorb onto the graphene via van der Waals interactions. The Si islands that form can be very thin, $<$ 5 nm, and their lateral size is determined by the temperature and duration of deposition[109]. Lee et al. found that the honeycomb lattice structure of the graphene was preserved, while the electrical properties changed with the deposition of Si. The bandgap was found to increase with increasing Si coverage, as did the maximum current level and the transconductance[109].

The evaporation of silicon or silicon monoxide powders can also lead to the formation of silicon nanowires, and these processes are typically carried out at temperatures of 1100-1300°C for 30 minutes to several hours[111][112].

E.2 Experimental methods

Kish graphite samples were prepared as described in section 3.1.2. The samples were annealed in a CVD chamber at 1000°C for a varying amount of time under 45 sccm of Ar and 5 sccm H_2 gas flow at 10 Torr pressure. A 0.5 cm tall

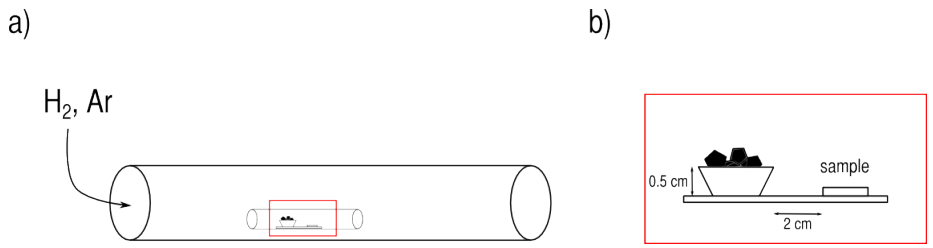


Figure E.1: a) shows the experimental setup for evaporating Si onto kish graphite by CVD, while b) shows the details of the sample mounting.

alumina crucible containing lumps of silicon was placed ∼2 cm upstream from the sample, as shown in figure E.1. The silicon lumps were immersed in 5% hydrofluoric(HF) acid for 1 minute to remove native oxide prior to the heating step. The details of the heating process are described in section E.2.1.

E.2.1 CVD heating process for silicon island deposition

1. Vent chamber and insert sample.
2. Pump chamber to vacuum.
3. Turn on H_2/Ar gas.
4. Raise temperature of chamber to 1000°C, this takes approximately one hour.
5. Set pressure and let the sample be annealed for the chosen amount of time.
6. Turn off H_2, increase Ar flow to 100 sccm, go to vacuum and turn off heater.
7. Wait 30 minutes before turning off Ar flow and pump.
8. Vent chamber to ∼1 Torr.
9. When the chamber reaches a temperature of 200°C, the sample can be removed.

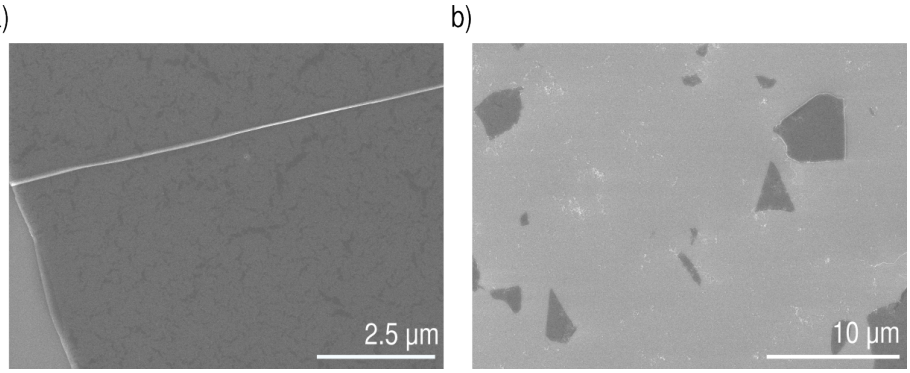


Figure E.2: SEM images of sample #is-Si01, which was annealed for 30 minutes in the CVD chamber. a) shows the surface of kish graphite, while b) shows a larger area of the sample.

E.3 Results

Sample #is-Si01 was annealed for 30 min in the CVD chamber. SEM images of the sample are shown in figure E.2, and it can be seen that some form of particles are present on the SiO_2 substrate surface. The particles are not found on the graphite pieces, but these have some dark areas of unknown origin.

Sample #is-Si02 was annealed for one hour under the same conditions as sample #is-Si01. A yellowish ring of deposited material could be seen in the inner tube of the CVD chamber after deposition, indicating some form of evaporation had taken place. SEM images were also taken of this sample, and these are shown in figure E.3. It was attempted to do EDX, but data could not be collected without destroying the sample in the process. The SEM images in figure E.3 show some 'spaghetti'-like structures both on top of and surrounding the kish graphite flakes. A test was done with a reference sample, annealing it without the presence of silicon for one hour. The reference sample also showed presence of these 'spaghetti'-structures, and it was therefore assumed that they had formed from carbon remnants deposited during the exfoliation process of the graphite.

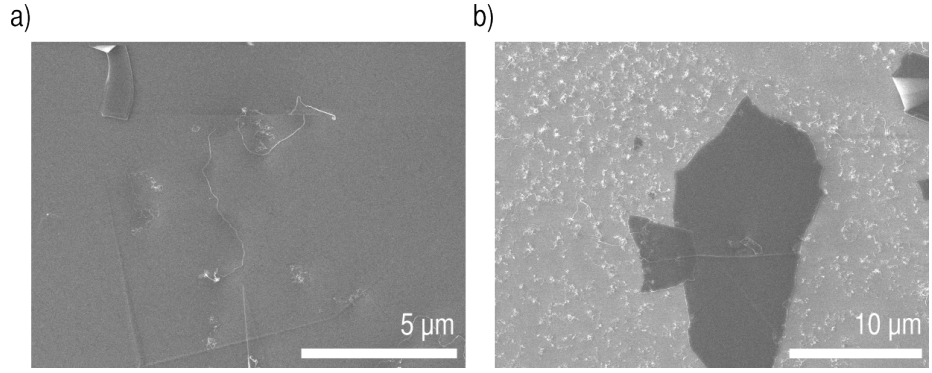


Figure E.3: SEM images of sample #is-Si02, which was annealed for 60 minutes in the CVD chamber. a) shows the surface of kish graphite, while b) shows a larger area of the sample.

E.4 Discussion

It can not be concluded upon wether or not silicon island structures have been successfully deposited on graphene. The characterization methods available at the time of this thesis were not sufficient to make a final conclusion.

The SEM images in figures E.2 and E.3 indicate that some wire-like structures start forming at a deposition time between 30 and 60 minutes when evaporating Si in the CVD chamber. The structures form both at the substrate and graphite surface, and were found to be up to about 5 μm long. Closer inspection revealed that the wires grew preferentially on corners and edges of the graphite flakes, as shown in figure E.4.

In order to investigate if the wires were made from silicon or carbon, a reference sample was placed in the CVD chamber for 60 minutes at 1000°C without any presence of silicon. After annealing, the reference sample looked identical to the samples heated in the presence of silicon, indicating that the wires are made of carbon. However, this does not exclude the possibility that silicon has been deposited on the graphite.

AFM imaging did not yield any results, due to the carbon wires protruding from the samples. EDX was attempted, but the procedure destroyed the sample before any useful results could be collected. The kish graphite flakes were deposited on Si/SiO_2 substrates, making EDX investigations difficult as the substrate would subdue any signal from thin silicon islands. To mitigate the prob-

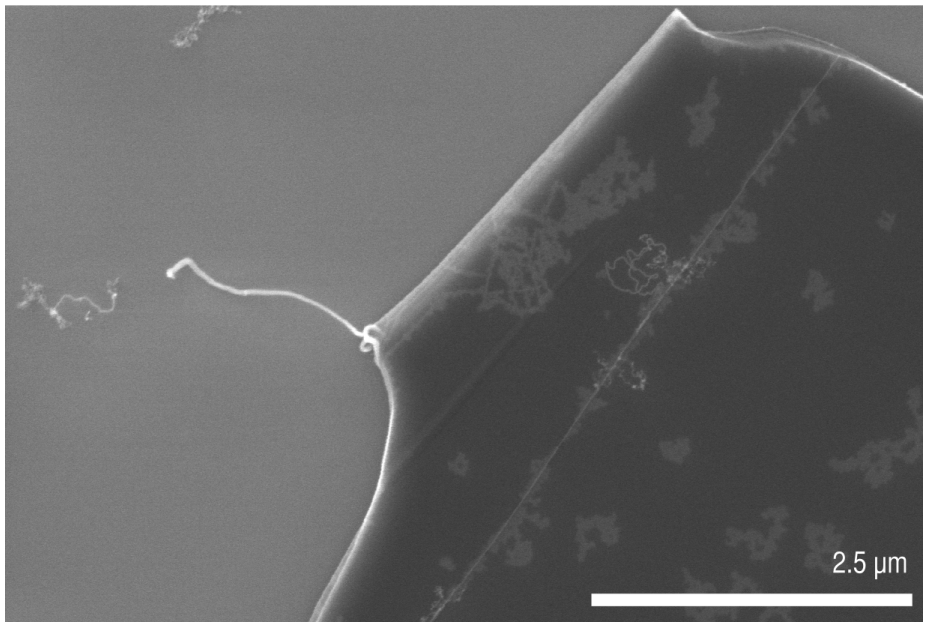


Figure E.4: A piece of kish graphite with a wire growing from one corner on sample #is-Si04

lem with carbon contamination, any future experiments should be performed on single-layer graphene samples prepared by CVD evaporation on copper foil.

Experiments performed by others suggests that higher pressures than what can be achieved with the NTNU NanoLab CVD chamber should be employed. Groups reporting the successful growth of silicon islands and wires use pressures of 50-400 Torr[109][113][112], while the maximum pressure possible at NTNU NanoLab is 10 Torr.