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Design and Operation Principles of DC Circuit Breakers

Development of a Solid State DC Breaker for the NTNU/SINTEF Smart Grid and Renewable Energy Laboratory

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Submission date: January 2016
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Problem Description

The goal of the work is to gain a deep understanding of the design principles and operation of a DC circuit breaker through analytical calculations, simulation activities and lab-scaled experimental validation. In particular, the investigation will be focused on the design of a lab-scaled solid state DC circuit breaker in the range of 700 V 100 A for the DC grid in the NTNU/SINTEF Smart Grid and Renewable Energy Lab. The work is targeted at development of simplified simulation models in EMTP/PSCAD, experimental laboratory activities and the development on basic design guidelines for DC circuit breakers.

Acknowledgments

This thesis is a contribution to the Protection and Fault Handling in Offshore HVDC Grids project (ProOfGrids), financed by the Norwegian Research Council's RENERGI programme and industry partners (EDF, National Grid, Siemens, Statkraft, Statnett, Statoil and NVE). The work was carried out in a collaboration between NTNU and SINTEF. In this regard, I would like to thank the main supervisor and professor Elisabetta Tedeschi, research scientist and co-supervisors from SINTEF Kjell Ljøkelsøy ans Salvatore D'Arco for their support. I would also like to thank to the service lab and the workshop at the Department of Power Engineering NTNU for their help with organizing the laboratory work. Finally, I would like to thank my fellow students and Sigurd Jakobsen for their help and support.

E.Ø.N.

Abstract

Exciting high voltage direct current (HVDC) transmission systems are mainly point-to-point connections. A multi-terminal HVDC grid consisting of three or more inter connected converter stations is suggested in order to increase the reliability, redundancy and flexibility in long distant bulk power transmission. Similar to AC (alternating current) grids, a protection system of HVDC-grids must be able to clear faults without affecting the remaining healthy parts of the grid. Thus, there is a need for HVDC circuit breakers, in which development is challenging:

- The circuit breaker must interrupt the current typically within 5 ms.
- The circuit breaker itself must provide the zero current crossing, as no natural zero crossing is exciting in DC grids.
- The circuit breaker must dissipate the magnetic energy provided by the line inductance
- The circuit breaker must withstand residual overvoltages after current interruption

This master thesis describes the development of a solid state dc circuit breaker for the DC grid in the NTNU/SINTEF Smart Grid and Renewable Energy Systems Laboratory. The DC breaker main components are Insulated bipolar gate transistors (IGBT) and metal oxide varistors (MOV). Under normal operation the IGBTs are placed in series with the DC line. The current commutates the current into a parallel MOV if current interruption is demanded. The MOV provides subsequently a counter voltage and forces the current to zero.

A test model was assembled initially and corresponding simplified PSCAD simulation model was developed in order to gain a deeply understanding of the operation of a DC breaker and facilitate the selection of components and the design of the DC breaker for the SINTEF/NTNU laboratory.

The selection of components for the DC breaker was based on the results from the experimental activities. In addition, corresponding ratings were obtained in an adjusted PSCAD model, which included an electro thermal equivalent circuit for temperature calculations.

A developed theoretical background including the components used in the DC breaker and general techniques of DC current interruption supported the work. Design guidelines for HVDC breaker based on the experiences from the work were also developed.

Sammendrag

Per i dag er flesteparten av likestrøms-kraftoverføringer (HVDC) punkt-til-punktforbindelser. Det er foreslått å knytte sammen flere fremtidige og nåværende forbindelser sammen til HVDC-nett, bestående av 3 eller flere omformerstasjoner. I HVDC-nett forventes å øke fleksibiliteten og påliteligheten sammenlignet med eksisterende lang distanse HVDC transmisjon. Vernsystemet i HVDC-nett vil måtte tilfredsstille tilsvarende krav som for konvensjonelle HVAC-nett, og må etter seleksjonskriteriet være i stand til raskt å klarere feil, f.eks. kortslutninger, slik at driften av det resterende nettet forblir upåvirket. Følgelig vil det være et behov for HVDC-effektbrytere hvis utvikling har flere utfordringer:

- Likestrøm (DC) har ingen naturlig null-gjennomgang og må genereres av bryteren selv.
- Feil i DC-nett utvikler seg svært raskt og kan påføre stor skade på resten av systemet som f.eks. på omformerstasjoene. Bryteren må derfor være i stand til å bryte strømmen og klarerere feilen innen typisk 5ms.
- Bryteren må kunne absorbere den gjenværende magnetiske energien i den utkoblede linjen på grunn av induktans.
- Bryteren må ha en holdespenning høyere enn de transiente overspenninger som på grunn av induktans oppstår ved brytning strøm.

I denne masteroppgaven følges prosessen av konstruksjonen av en DC effektbryter til bruk i NTNUs og SINTEFs laboratorium for smartgrid og fornybar energi. Krafttransistorer, i form av IGBTer og metalloksidavledere som utfører strømbrytningen, utgjør hovedkomponentene. Transistorene leder strømmen under normal drift, og vil under strømbrytning kommutere strømmen inn i parallelle metalloksidavlederne. Avlederen sørger for at strømmen faller til null ved å generere motspenning, og absorberer den resterende magnetiske energien. En DC-kontaktor benyttes for å opprette et fysisk isolerende skille etter at feilstrømmen er klarert. Som bakgrunnsmateriale presenter oppgaven en teoridel som tar for seg strømbrytning i DC-nett, de aktuelle komponentene og verktøy for termiske beregninger i form av en elektrotermisk kretsekvivalent.

En forsøksmodell ble satt sammen i forkant av konstruksjonen av DC bryteren til bruk på NTNU/SINTEF-laboratoriet. Forsøkene som ble utført utført ga et grunnlag for en dypere forståelse av virkemåten til en DC-bryter og for å kunne velge ut egnede komponenter.

Dette arbeidet ble støttet av simuleringer av en forenklet modell utført i PSCAD. Komponenter til DC bryteren ble valgt ut basert på erfaringene fra forsøksmodellen og simuleringer. Nye tilpassede simuleringer ble utført for å kunne gi indikasjon på forventet virkemåte og for å bestemme DC-bryterens merkedata.

Basert på erfaringer fra hele prosessen foreslås enkle retningslinjer for oppbygningen av DC-brytere i HVDC-sammenheng. Tilsvarende DC brytere som ble konstruert til NTNU/SINTEF laboratoriet vurderes til å medføre for store effekttap på grunn av ledespenningsfallet over transistorene. Det ble foreslått en utvidelse til en hybrid løsning bestående av ultra hurtige mekaniske brytere i tillegg.

Acronyms

NTNU Norwegian University of Science and Technology

HVDC High voltage alternating current

AC Alternating current

DC Direct current

MOV Metal oxide varistor

PSCAD Power system computer aided design

EMTP Electromagnetic transient programming

VSC Voltage source converter

LCC Line commutated converter

MMC Modular muilti-level converter

IGBT Insulated bipolar gate transistor

GTO Gate turn-off thyristor

LCS Load commutation switch

UFD Ultra fast disconnecter

emf Electromotive force

TIV Transient interruption voltage

MOSFET Metal oxide semiconductor field effect transistor

ZnO Zinc oxide

SiC Silicon carbide

OHL Overhead line

CLR Current limiting reactor

BIGT Bi-mode insulated gate transistor

BS Bypass switch

CS Charging switch

IS Isolator switch

FPGA Field programmable gate array

Symbols

Latin Alphabet

C_{DC} DC capacitor voltage

C_{MOV} MOV capacitance

C_{snub} Snubber capacitance

C_v Heat capacity

C_θ Thermal capacitance in elctro thermal circuits

$C_{\theta i}$ Thermal capacitance in elctro thermal circuits of layer i

g_m Forward transconductance

I Current

I_C Collector current

I_{Crm} Repetitive peak current

I_{Cmax} Rated collector current

I_{line} Line current

I_{max} Maximum current interruption capability

I_{switch} Contactor current

I_{trip} Detection trip level of the protetion system

I_0 Peak line current

K_{MOV} Ceramic material constant

L_{LCR} Current limiting reactor inductance

L_{line} Line inductance

L_{load} Load inductance

L_σ Stray Inductance

P_{cond} Heat conduction loss

P_{MOVmax} MOV maximum average power

P_{MOV} MOV power

P_{tot} Maximum power dissipation of an IGBT

P_{loss} Power loss

R_D Discharge resistance

R_{load} Load resistance

R_{ON} On-state resistance

R_θ Thermal resistance

$R_{\theta ja}$ Thermal resistance from junction to ambient

Q Energy as heat

t Time

T Temperature

T_a Ambient temperature

t_{aux} Time interval from V_{coil} is set to 0 to V_{aux} is open circuited

T_j Semiconductor junction temperature

t_{break} Break time, time form peak current to zero current

$T_{ciritical}$ MOV critical temperature

T_{case} Case temperature

T_{jmax} Maximum junction temperature

T_{MOV} MOV temperature

t_{pulse} Pulse time

t_{step} Simulation step time

$T_{response}$ Response time of the protection system

t_{zero} Time interval from V_{coil} is set to 0 to I_{switch} = 0 V

V_{aux} Contactor auxiliary contacts voltage

V_{DC} DC source voltage

V_{CB} Circuit breaker voltage

V_c MOV Clamping voltage

V_{CE} Collector-emitter voltage

V_{CEsat} Collector emitter saturation voltage

V_{CEmax} Rated collector-emitter voltage

V_{CBmax} Maxium DC breaker voltage

V_{coil} Contactor coil voltage

V_{DC} Voltage source voltage

V_{fb} Forward voltage base drop

V_{fc} Forward voltage drop due to current conduction

V_{GE} Gate-emitter voltage

$V_{I.C}$ Insulation coordination level

V_{MOV} MOV voltage or rated operating voltage

V_{margin} Voltage margin

V_{line} Line voltage

V_{switch} Contactor voltage

$V_{snubMOV}$ Snubber MOV voltage

W_{Csnub} Snubber capacitor energy

V_v Rated varistor voltage

V_w Withstand voltage

W_{Csnub} Snubber capacitor energy

W_{line} Energy stored in the DC line

W_{source} Energy provided by the voltage source

$W_{switchingloss}$ Total switching loss

W_{MOV} MOV energy dissipation

W_{MOVmax} MOV maximum energy dissipation

Z_θ Thermal transient impedance

Greek Alphabet

Φ Magnetic flux

α Non linearity exponent

λ Thermal conductivity

τ Time constant

$\tau_{\theta i}$ Thermal time constant of layer i

Contents

Chapter 1

Introduction

1.1 Background

Renewable energy resources such as wind, solar and hydro power have gained considerable interest in recent years. Massive exploitation of these resources typically requires long distant bulk power transmission from remote areas, where high voltage direct current (HVDC) is the only feasible option [1]. Present HVDC systems are mainly point to point connections, but development of multi-terminal meshed HVDC grids is suggested and may contribute to increase the power system flexibility, reliability and redundancy and also reduce the number of converter stations [2]. However one of the obstacles of realizing such grids is the need for a protection system to minimise the effects of faults [3]. In excising HVDC point to point connections faults are cleared from the AC (Alternating Current) side of the converter stations. A protection system of a HVDC grid must also comply with the selectivity criterion as in present AC grids which provides the demand for HVDC circuit breakers [4].
There are several challenges related to the development of HVDC Circuit breakers [5, 2, 6]:

- The rise of the fault current in DC (Direct Current) grids is very high compared to AC grids because the low line impedance of DC lines. Accordingly, the DC breaker must interrupt the current typically within 5 ms.

- In AC grids the arc in the circuit breaker under current interruption is extinguished by the zero current crossing which is provided naturally by the system. In DC grids the zero current crossing must be provided by the circuit breaker itself.

- Unlike AC girds, the magnetic energy of DC grids is stored in the system inductance. The DC circuit breaker must dissipate this energy.

- The DC breaker must withstand the residual overvoltages after the current interruption.

There are promising HVDC breaker topologies suggested from ABB and ALSTOM. They differ from AC circuit breakers as they are based on semiconductor technology, metal oxide varistors (MOV) and ultra-fast switches [5, 7]. A simplified version of these topologies is the solid state DC circuit breaker. A lab scaled type for research applications will be developed for the DC grid in the NTNU/SINTEF Smart Grid and Renewable Energy Lab.

1.2 Objectives

The main objectives of this thesis are:

- Develop a theoretical background for the design of DC circuit breaker.
- Assemble a lab-scaled solid state DC circuit breaker test model.
- Design a lab-scaled solid state DC circuit breaker for the DC grid in NTNU/SINTEF Smart Grid and Renewable Energy Lab.
- Develop simulation models in EMTP/PSCAD of the lab-scaled DC circuit breaker test model and of the lab-scaled solid state breaker for the DC grid in NTNU/SINTEF Smart Grid and Renewable Energy Lab
- Develop guidelines for the design of a high voltage DC circuit breaker on the basis on the experimental work, simulations and design process.

1.3 Limitations and Simplifications

The following limitations of scope and simplifications are considered in this work:

- A DC grid is represented by an inductance and a resistor. Travelling waves and distributed parameters are not considered in the emulation of DC grids.
- The AC/DC converters stations are represented as DC voltage sources or capacitor banks. Harmonics, ripple and control system of the DC grid representation are omitted.
- The work is carried out practically with simplified analytic calculations. Advanced analytic calculations for DC systems are omitted.
- Semiconductor physics are briefly considered.
- The control of the solid state breaker is manual, the focus is on the operation of the electrical aspects DC breaker and not the protective relays.
- Thermal modelling is carried out in one dimension.
- The protection system of the converters are not considered. The emphasis is on the protection from line faults.

1.4 Methodology/Approach

Initially a theoretical background will be established with emphasis on the requirements of DC circuit breakers in a DC grid, the separate components and the challenges related to them.

To facilitate the selection of the components for the lab-scaled solid state DC circuit breaker for the NTNU/SINTEF Smart Grid and Renewable Energy Lab, a test model will be assembled

and tested experientially. The experimental work with the test model is supported by preliminary simulations in EMPT/PSCAD. The simulations will thereafter be adjusted according to the experimental results from the test model to obtain a realistic, but simplified DC breaker simulation model.

The results from experimental work and the simulations will be analysed in order to determine the components of the solid state DC circuit breaker for the NTNU/SINTEF Smart Grid and Renewable Energy Lab and development of basic guidelines for DC circuit breaker design for high voltage applications. MATLAB will be used for processing results from EMPT/PSCAD and experimental work.

1.5 Contributions

The result of the work contributes with a detailed analysis and insight of the operation of solid state DC circuit breakers. A final lab-scaled prototype DC-breaker is developed, that is useful for further research on HVDC multi-terminal grids at the NTNU/SINTEF Smart Grid and Renewable Energy Laboratory.

1.6 Structure of the Report

Chapter 2: Background information of DC grids and DC breaker topologies.

Chapters 3, 4 and 5: Theoretical background in terms of the components, system aspects and current interruption in DC grids.

Chapter 6: Brief description of the NTNU/SINTEF Smart Grid and Renewable Energy Lab and the implementation the DC breaker test model for experimental activities.

Chapter 7: Considerations and development of PSCAD simulation models.

Chapter 8: The results from experimental work with the test model and results from PSCAD simulations.

Chapter 9: Selection of the components for the DC breaker intended for use in the NTNU/SINTEF Smart Grid and Renewable Energy Lab. Determination of the expected rating.

Chapter 10: Implementation of he DC breaker with description of configuration and a function test.

Chapter 11: Guidelines for DC breakers for high voltage applications based on experiences with the development of the DC breaker.

Chapter 12: Discussion, conclusion and suggestions for further work.

Chapter 2

DC Grids

This chapter introduces the concept of DC grids briefly. The key aspects of faults and DC circuit breaker is described in order to provide some background information. High voltage power system applications are emphasised, as the DC grid in NTNU/SINTEF Smart Grid and Renewable Energy Lab is intended to emulate a HVDC transmission system.

2.1 Defintion of DC Grids

Applications of DC grids have a wide area and may vary from medium voltage power system on ships, low voltage solar powered micro grids in remote areas [8] to a high voltage "supergrid" connecting Europe, Middle-East and northern Africa [6].
A multi-terminal HVDC grid system is defined by CIGRE as a HVDC transmission system connected to more than 2 converter stations [9]. An example of a simple DC grid is shown in figure 2.1, which depicts an offshore wind farm power plant connected with 3 converter stations onshore. In the introduction the motivation for such grids were mentioned briefly, and the HVDC circuit breaker is regarded as one of the key components for the development [2].

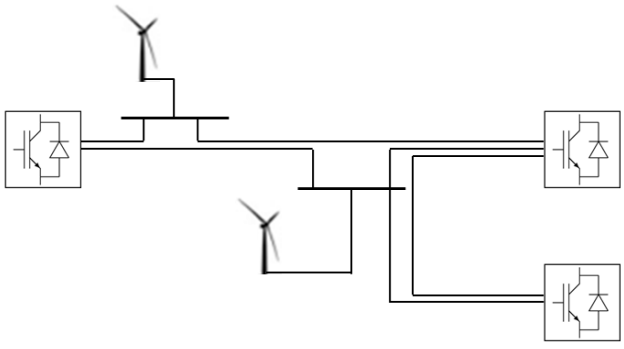


Figure 2.1: Example of a DC grid connected to an offshore wind power plant [4]

2.2 Voltage Source Converters

Two types of converter technologies are used in HVDC transmission: Line commutated converters (LCC) and voltage source converters (VSC). VSC technology is suggested for DC grids applications [4]. There are several advantages such as: Better control of power flow, black start capability and provision of lower harmonic emission [2]. VSC converter stations are characterised by: AC side filters, AC phase reactors, 3-phase converter bridge with a power transistors (IGBT), a DC side capacitor bank [1]. A general overview of a VSC converter station in an HVDC system is shown in figure 2.2. The 3-phase bridge may be of a modular multi-level converter

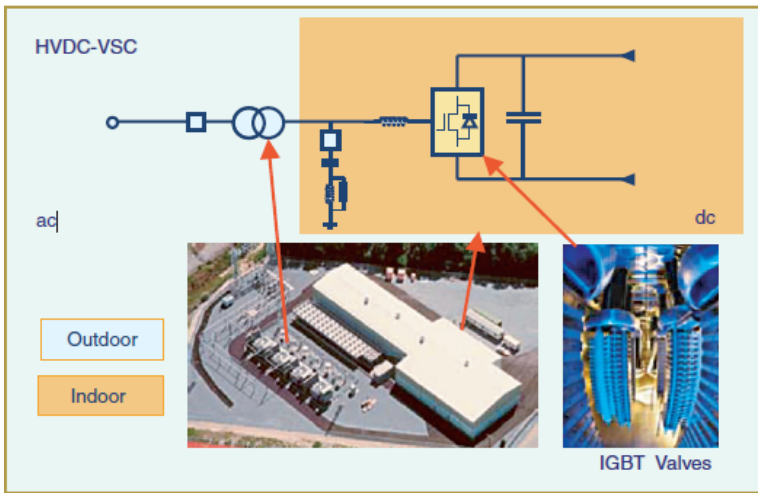


Figure 2.2: An overview of a HVDC VSC converter station [10]

(MMC) topology in future DC grids [11]. The type of converter technology will affect the fault behaviour of the system, and the protection system must therefore be designed accordingly as discussed in the following section [1].

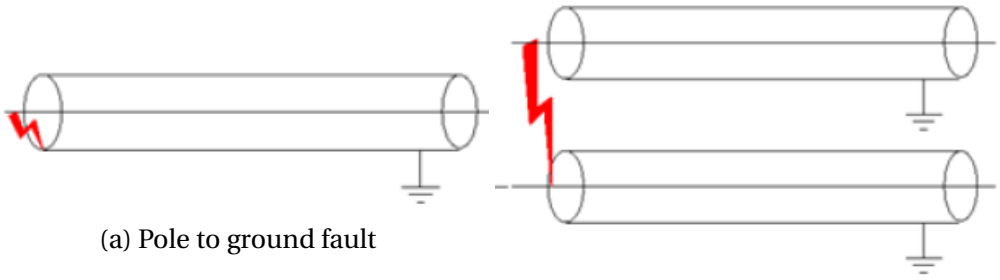
2.3 Faults in DC Grids

Assuming a two pole configuration in a DC grid, two main types of faults are possible: Pole-to-ground fault and pole-to-pole fault seen in figure 2.3. The pole-to-ground fault is assumed to be the most likely to occur, while the pole-to-pole fault is the most severe [12]. The expected behaviour the fault types mentioned are dived into 3 phases [13]:

1. Capacitor dischrarge phase The DC side capacitor will discharge immediately when the fault has occurred.

2. Frewheeling diode phase After the capacitor has discharged, the converter voltage falls to zero, and currents will be conducted through the diodes of the converter station as the transistors are most likely blocked. The converter operates as an uncontrolled rectifier.

3. AC side feeding phase The fault will eventually be fed from the AC grid.



(a) Pole to ground fault

(b) Pole to pole fault

Figure 2.3: Types of faults in a DC grid [4]

A detailed study of the Transient fault current in VSC HVDC grids is found in [14]. In the mentioned reference, travelling wave phenomena are also simulated in PSCAD/EMTP. The current through a DC circuit breaker under a pole-to-ground fault, obtained from the simulations, is shown in figure 2.4. The contributors to the fault current are depicted, in the figure: Area A)

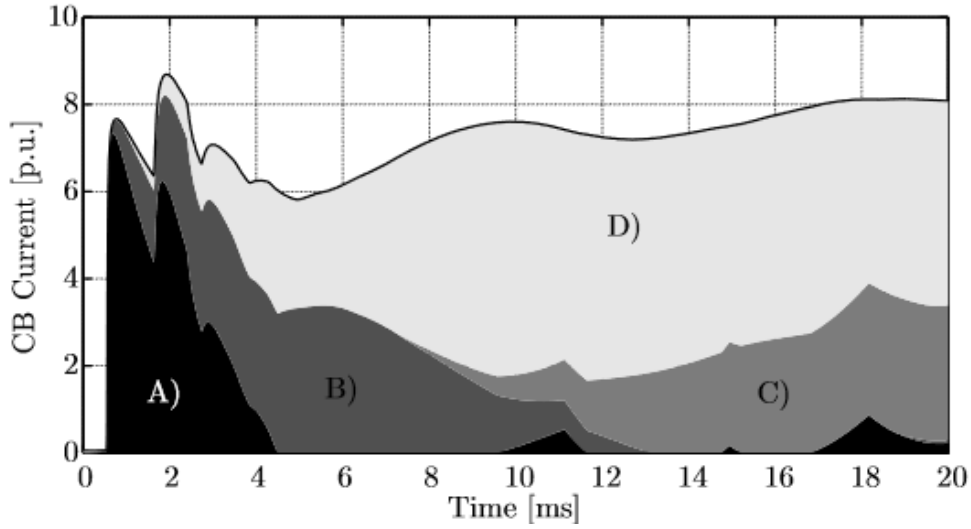


Figure 2.4: Fault current through a DC circuit breaker with a pole to ground fault 100 km away simulated in PSCAD [14]

represents the current contribution from the DC capacitor, B) from the adjacent cable feeder and both C) and D) from different converter stations in the model simulated. The intention presenting figure 2.4 is to show the contributions to the fault current and a steep rise up to 7-8 pu within the first 2 ms.

2.4 DC Grid Protection System

The function for a protection system is to protect of the system itself and its user against damage while provide a reliable supply [1]. A power system protection scheme, regardless of AC or DC,

should provide the properties or criteria listed in [4]. The criteria in particular concerning DC breakers are:

Selectivity States the demand for DC circuit breakers in general, the protection system must be able to isolate faulted parts of the system only.

Speed States the demand for the DC circuit breaker to operate before the fault current damages the power system system and its users.

Reliabilty States the requirement for the DC circuit breakers in the system to be able to conduct its required function under different modes and scenarios that may occur in DC grid.

The speed criterion provides some challenges due to fast rising fault currents seen in last section and in the introduction. The fault currents in DC grid may rapidly damage the free-wheeling diodes of the converter stations and thus the DC breaker should operate before the event of diode damage is likely to occur. As stated in the introduction, the protection system must clear the fault within a few ms.

2.5 DC Circuit Breaker Topologies

The DC circuit breaker topologies may be divided into three main types [1]:

1. Resonance DC breakers
2. Solid state DC breakers
3. Hybrid DC breakers

2.5.1 Resonance DC Circuit Breakers

Attempts to develop resonance HVDC circuit breakers were made as early in the 1980s' [1]. An outline of the topology is shown in figure 2.5. The topology consist of mechanical switches and interrupts the current when a zero crossing is generated with the help of a capacitive-inductive current path (commutation current path) in parallel with the main mechanical switch. The topology also includes an absorbing branch consisting of MOVs. The technology has been proven too slow for fault current interruption in DC grid based on VSC technology [2]. The resonance topology may still provide useful applications such as load switching as it has a low resistive on-state loss compared to newer topologies mentioned in this section [15]. The tree main branches of the resonance DC breaker topology are:

1. The nominal current path
2. The current commutation path
3. The energy absorption/dissipation path

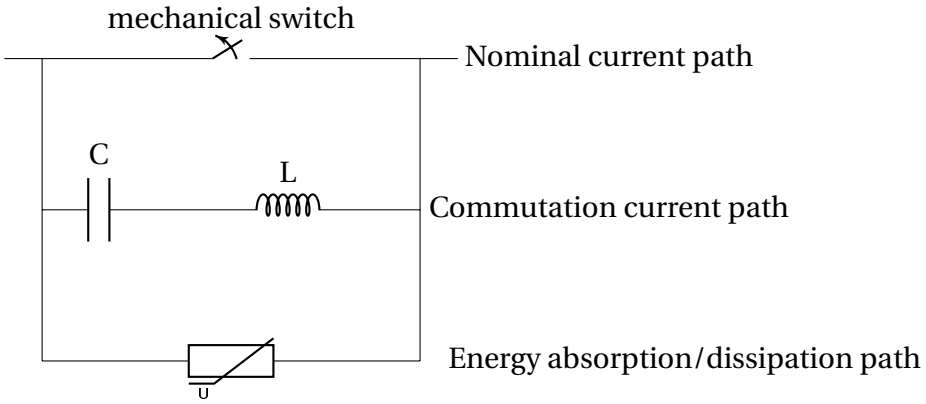


Figure 2.5: Resonance DC circuit breaker topology [1]

Under normal operation the current is flowing through the nominal current path. If the breaker receives an interruption command, the mechanical switch will open and arc will occur and current will start to commutate into the commutation path. At this stage, the current oscillations are generated. The voltage drop of the arc contributes to generate current oscillations due to the commutation path which will provide the zero current crossing and eventually extinguish the arc. Thereafter, the current will flow into absorption path in order to dissipate the residual magnetic energy in the system.

2.5.2 Solid State DC Circuit Breakers

The solid state topology consists of semiconductor devices such as the insulated gate bipolar transistor (IGBT) or gate turn-off thyristor (GTO) and parallel MOVs [15]. Under normal operation the current flows through the devices. To interrupt the current, the devices are switched off and current is commutated into the parallel MOV which here function both as the commutation path and the energy absorbing path. Similar to the resonance topology, the MOV will dissipate the energy stored in the system. Figure 2.6 depicts an example of a solid state topology with the use of IGBT and diodes for bi-directional applications. In figure 2.6 a solid state DC

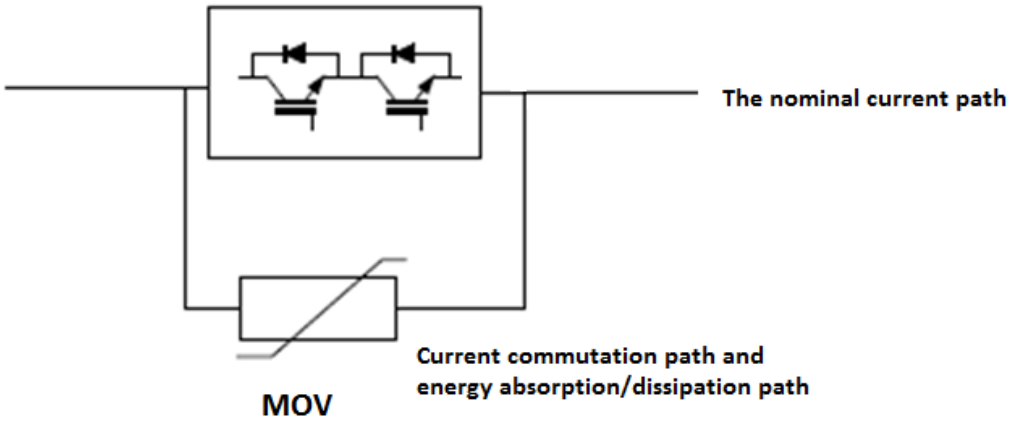


Figure 2.6: Solid state DC circuit breaker topology [13]

breaker for one directional current interruption is shown. Bi-directional current interruption is achieved by placing a similar IGBT with an anti-parallel diode in anti-series. More breaker cells may be placed in series to increase the rated voltage level. The solid state state circuit breaker has proven to break current with the required speed for fault current interruption. But as the semiconductors are conducting current under normal operating conditions, the losses due to the voltage drop over the breaker will be high especially in high voltage applications [15, 13]. The DC breaker intended in the DC gird in the NTNU/SINTEF lab is a lab-scaled solid state DC circuit breaker. Unless other topologies stated in further chapters, a solid state DC breaker is refereed to as DC breaker.

2.5.3 Hybrid DC Circuit Breakers

Hybrid topologies consists of both mechanical switches and semiconductor devises. There are existing different topologies suggested which are surveyed in [16]. ABB and ALSTOM have developed HVDC circuit breaker prototypes which are presented as promising technologies in recent research literature [5, 7]. Figure 2.7 depicts the main outline of the circuit breaker. The breaker may be seen as an extension of an IGBT based solid state topology, since the breaker essentially has an additional branch with a mechanical low-ohmic ultra fast disconnecter (UFD) and a load commutation switch (LCS). The LCS is also a solid state DC breaker, but has only sufficient breaker cells in order to commutate the current into the main breaker. The Hybrid

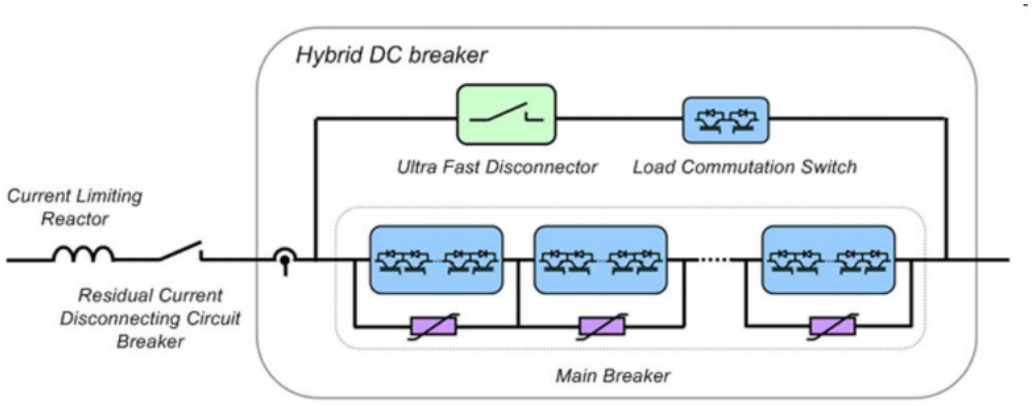


Figure 2.7: ABB hybrid HVDC circuit breaker topology [5]

topology overcomes the issue with conduction losses of the solid state topology by letting nominal current under normal operation flow through a nominal current path consisting of the LCS, and a UFD indicated in figure 2.7. When the circuit breaker receives an interruption command, the LCS switches off and commutates the current into the main breaker similar to the solid state breaker. After the commutation, the UFD opens and creates a physical isolation, protecting the LCS from the voltage drop when the main breaker interrupts current. The UFD is a key component to keep the losses under normal operation as low as possible and obtaining the fast current interruption needed. The UFD is an electromagnetic actuator, using magnetic forces in order to obtain the fast switching speed required. The operation and structure of a UFD is described in detail in [17]. ABB claims that their HVDC circuit breaker is able to clear faults within in 5

ms [18]. In figure 2.7 a current limiting reactor (CLR) is shown which is an auxiliary series inductance with the line. The function of a CLR is to limit a high slope of the fault current. A switch in parallel with the hybrid dc breaker is also indicated which provides physical isolation after the fault current has been cleared.

Chapter 3

Theoretical Background - General Electric Concepts

The following three chapters(chapter 3-5), outline the theoretical background for the design and operation of a DC breaker. This includes phenomena that cause issues related to fault current interruption as well as physical components used for DC breaker applications.

3.1 Magnetic Phenomena

Before defining the transient interruption voltage (TIV), the definition of inductance and Faraday's law is described to illustrate the connection with basic electromagnetic laws.

3.1.1 Inductance

Inductance is a physical quantity defined in [19] as the ratio of total flux linkages $N\Phi$ to the current which they link I :

$$L = \frac{N\Phi}{I} \tag{3.1}$$

When a circuit segment with inductive properties experiences a change in the current, the linking flux will also change and provide time varying flux linkage. According to Faraday's law this will induce a counter electromotive force (emf):

$$emf = -\frac{dN\Phi}{dt} \tag{3.2}$$

Equation 3.3, which combines 3.2 and 3.1, is applicable for circuit calculations:

$$V_{line} = L_{line}\frac{dI_{line}}{dt} \tag{3.3}$$

The equation states that interruption of DC currents will induce negative voltages in the lines connected to the DC-breaker due to time-varying magnetic field related to decreasing currents.

3.1.2 Transient Interruption Voltage

The simplified DC grid model shown in figure 3.1 is used to illustrate the transient interruption voltage (TIV) phenomenon. Assuming a fault occurs and the load R_{load} is short circuited: The ideal DC breaker quickly interrupts the fault current resulting in high and negative current slope dI_{line}/dt. This induces an overvoltage in the line L_{line}, according to equation 3.3. The overvoltage is referred to as the transient interruption voltage, analogous to transient recovery voltage in AC circuit breakers [7]. The relation in equation 3.3 is also important in terms of fault clearance time since it states that the TIV and fault-clearance time are inverse quantities.

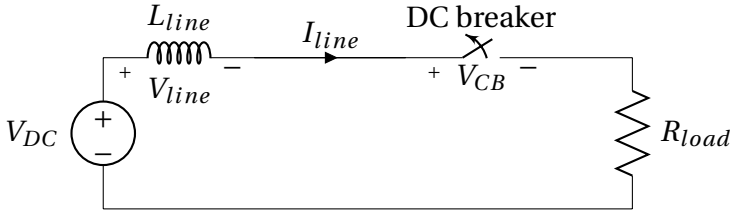


Figure 3.1: DC grid model with an ideal circuit breaker

3.2 Counter Voltage

The counter voltage principle describes an approach for forcing the DC current to zero. Unlike AC grids, there is no zero-current crossing provided naturally by the system. With regard to the figure 3.1, the slope of the current in the presence of short circuited load may be expressed as:

$$\frac{dI_{line}}{dt} = \frac{V_{DC} - V_{CB}}{L_{line}} \tag{3.4}$$

$$V_{CB} > V_{DC} \Rightarrow \frac{dI_{line}}{dt} < 0 \tag{3.5}$$

The equations 3.4 and 3.5 states that slope of the fault current will depend on the the DC breaker voltage. In order to force the current to zero, the DC-breaker must provide a counter voltage higher than the system voltage to ensure a negative voltage over the line inductance L_{line}. A suggested solution for a DC breaker is to provide the counter voltage with metal oxide varistors (MOV) [2].

3.3 Magnetic Energy

The stored magnetic energy in the inductive line segment W_{line} during a fault can be expressed as:

$$W_{line} = \frac{1}{2} L_{line} I_0^2 \tag{3.6}$$

Where I_0 is peak current of I_{line}. During the fault interruption, when the current decreases, the voltage source continues to deliver energy into to system [20]. This energy can be expressed as:

$$W_{source} = \int_0^{t1} V_{DC} I_{line}\, dt \tag{3.7}$$

If a constant DC source voltage is assumed, equation 3.7 can be rewritten as:

$$W_{source} = \frac{L_{line} V_{DC} I_0^2}{2(V_{CB} - V_{DC})} \tag{3.8}$$

The total energy the DC breaker must dissipate is then be expressed as:

$$W_{tot} = \frac{1}{2} L_{line} I_0^2 (1 + \frac{V_{DC}}{(V_{CB} - V_{DC})}) \tag{3.9}$$

3.4 Successful Interruption

For successful current interruption, a DC breaker must both be capable to dissipate the magnetic energy stored in the system and withstand the TIV by providing a counter voltage. In AC circuit breaker technology the magnetic energy is absorbed by the system itself due to the nature of AC grids. The transient recovery voltage, analogous to TIV in AC grids, may cause reignition of the arc between the circuit breaker separating contacts, but is eventually handled by the distance between the contacts and by an insulating dielectric medium such as SF6 in the arcing chamber [21, 7]. The suggested solutions for DC breakers will be discussed in the following sections and involves as mentioned the use of MOVs.

Chapter 4

Theoretical Background - Basic Components

4.1 The Insulated Gate Bipolar Transistor

Transistors are semiconductor devices capable of controlling the current through their terminals by applying current or voltage signals. A transistor that conducts currents is referred to as being in on-state mode. While a transistor that blocks currents referred to as being in off-state mode. Transistors may therefore be used to commutate or interrupt DC fault currents. The Insulated Gate Bipolar Transistor (IGBT) is considered a good option for the choice of semiconductor both for a solid state and a hybrid topology DC breaker [22].

The IGBT has been widely used since the early 1990s' in various applications such as voltage source converters (VSC). The IGBT was designed for high switching speeds and low on-state losses, and is based on an existing metal oxide semiconductor field effect transistor (MOSFET) structure [23].

This section briefly describes the structure of the component followed by the operation principles with a practical approach necessary for the DC-breaker design. IGBT semiconductor physics can be studied in literature such as [24, 25].

4.1.1 Insulated Gate Bipolar Transistor Structure

The IGBT has three terminals or connection points: Emitter, collector and gate. This is equivalent to the source, drain and gate of a MOSFET. The circuit symbol is shown in 4.1. Figure 4.2 depicts the cross section of the component with its n- and p-layers and junctions.

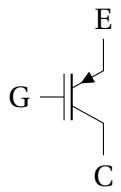


Figure 4.1: IGBT circuit symbol showing the G-gate, C-collector and E-emitter terminals

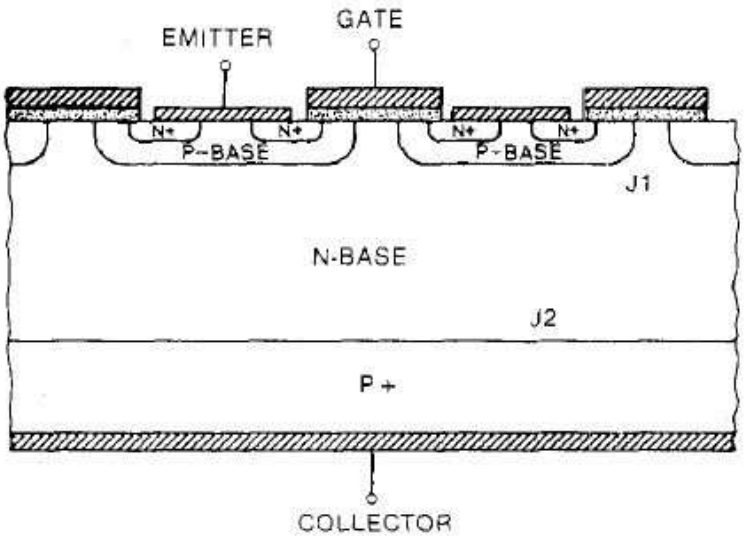


Figure 4.2: Cross section of an IGBT, with the junctions J1 and J2 and the n and p-layers indicated [26]

The semiconducting materials inside the component consist of a lattice structure of silicone (Si) doped with impurities. The impurities in the n-layer provides an extra electron co-valance band in the lattice. While the p-layer is doped with a material such that there are lacking electron covalent bands, and hence generating electron holes in the lattice. These p- and n-layers are also referred to as *donors* and *acceptors*, respectively. An excessive electron in the n-layer may be captured in an empty co-valance band, or in the p-layer captured in a hole. This process is referred to as *recombination*. The essential is that a junction of an n-layer and a p-layer interface is able to conduct or block current, depending on the voltage bias applied. These junctions are referred to p-n junctions. The working principle is that a positively biased p-n junction provides a current conducting channel through the p- and n-layers and the junction. While a negatively applied bias provides insignificantly small reverse current [23]. A synthesis of these junctions then provides the features of component as in this case the IGBT, which has two pn-junctions, J1 and J2, shown in figure 4.2.

4.1.2 IGBT Operation

The gate of the IGBT is first assumed to be open circuited, which in this case means there is no electrical connection to the gate terminal. If a positive voltage bias is applied to the collector with respect to the emitter, J2 will become negative biased and hence block current. Similarly if the IGBT is negatively biased, J1 will become negatively biased and current conduction will be blocked. Hence the IGBT will not conduct current without applying voltage to the gate.
An applied gate-voltage will invert the upper p-layer allowing electrons to flow from the upper n-plus-layer to the n-minus layer indicated in figure 4.2. This inversion allows positive current conduction from the collector terminal to the emitter terminal. This state of the IGBT is referred to as the on-state mode. Opposite currents remain blocked due to the negatively biased J2. Typical on-stae gate-emitter voltage is V_{GE} = 15 V of a V_{CEmax} = 1000 V rated IGBT. The switching

from on-state to the off-state (positive biased, no current conduction) is made by short circuiting the gate to the emitter, which will remove the invention of the p-layer [26]. This turn-off transition is characterised by two time intervals: t_{fi1} and t_{fi2}. During t_{fi1} the current quickly falls to a level I_{tail}. From here, the current decays exponentially t_{fi2} due to free residual electrons which will decay by recombination [25]. The current during a transition from turn-on to turn-off is illustrated in figure 4.3.

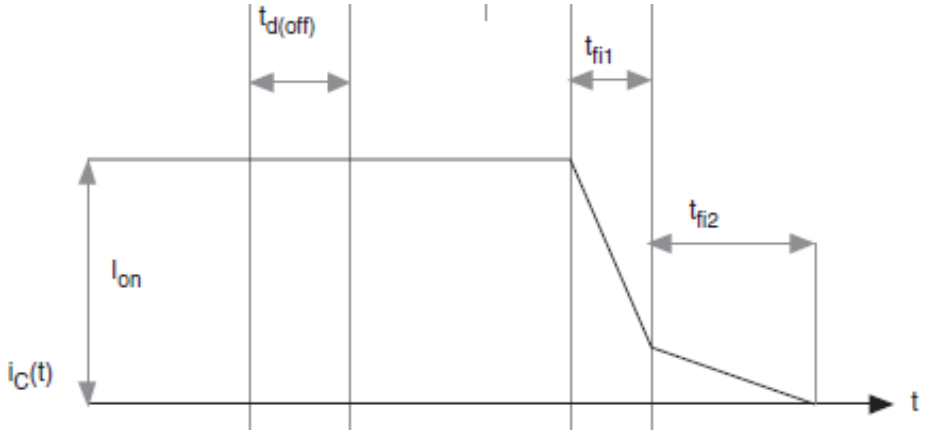


Figure 4.3: IGBT turn off with the two time intervals t_{fi1} and t_{fi2} indicated [27]

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Anti-Parallel Diode

As mentioned, the IGBT only allows one-directional current conduction. To enable bi-directional current conduction, an anti-parallel diode is attached, illustrated in figure 4.4.

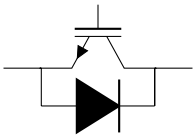


Figure 4.4: IGBT with an anti-parallel diode

IGBT Voltage-Current Characteristic

Figure 4.5 illustrates the typical collector emitter voltage, V_{CE}, and the collector current I_C of an IGBT. It should be noticed that the forward voltage drop is another term used for V_{CE} and more generally for all types of semiconductor devices. The figure also shows the dependence of V_{GE}. Operation in the active region indicates an on-state mode where V_{CE} is determined by circumstances in the outside electrical circuit of the IGBT [28]. The forward-blocking characteristics indicate the off-state, in which an insignificant so-called cut-off current I_{CES} will flow. High forward bias voltages lead to avalanche breakdown and potential component destruction. The breakdown value is indicated as $V_{(BR)CES}$.

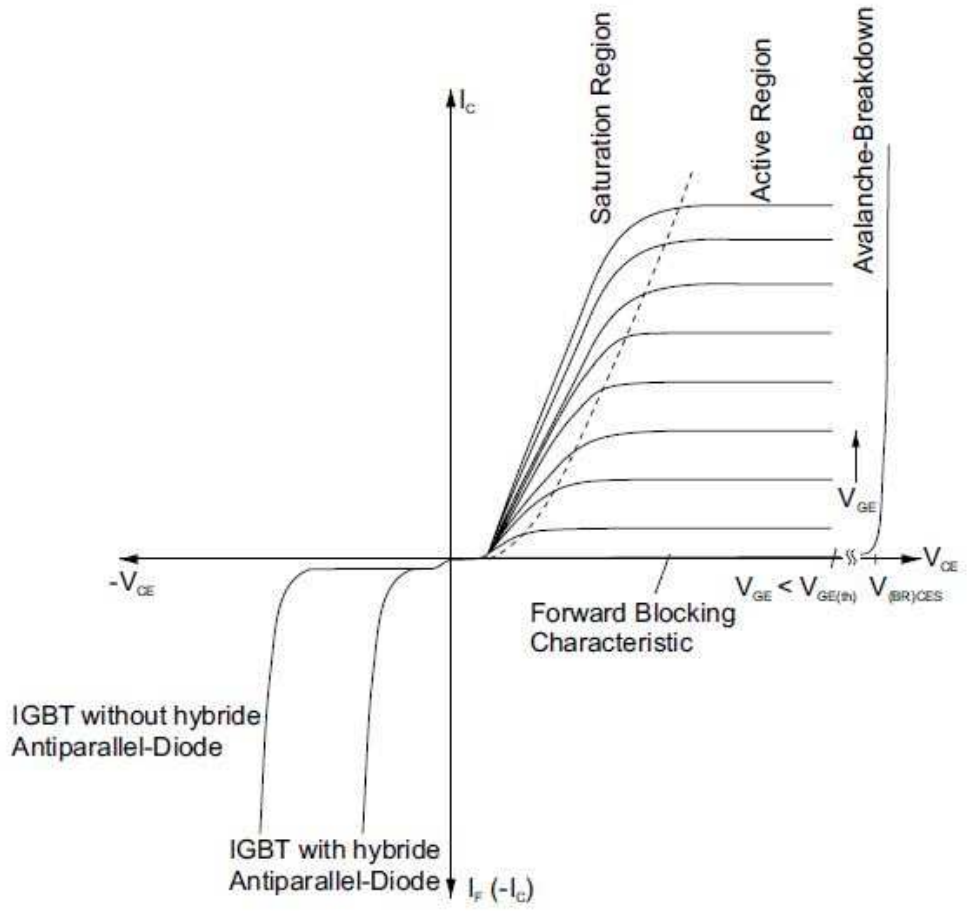


Figure 4.5: Current and voltage characteristic of an IGBT. $V_{(BR)CES}$ is the collector emitter breakdown voltage [28]

The on-state I_C - V_{CE} characteristic is normally temperature dependent. Typical junction operation temperature for an IGBT is from $25-125°C$. The thermal aspects of the component operation will be discussed in section 5.2.

4.1.3 IGBT Power Loss

A practical approach for the IGBT losses is derived in the following sections. This should suitable for hand calculations and simplified simulations according to he initial objectives and calculate the temperature rise due to loss dissipated as heat.

ON-State Conduction Loss

As seen in figure 4.5, the current conducting IGBT provides an on-state voltage drop V_{CE} and will thus generate power loss dissipated into heat. The voltage drop may be divided into a base forward voltage drop $V_{fb} = V_{CE}(I_C = 0)$ and a forward voltage drop due to current conduction $V_f c = V_{CE}(I_C) - V_{CE}(I_C = 0)$. $V_f b$ is normally given in data sheets provided by the manufacturer.

Accordingly, the power loss may be described as:

$$P_{loss} = (V_{fc} + V_{fb}) I_C \tag{4.1}$$

The on-state power loss may be described by resistive electrical properties. Transconductance g_m is defined in [24] as the change the collector current, I_C, with respect to the collector-emitter voltage V_{CE}:

$$g_m = \frac{\partial I_C}{\partial V_{CE}} \tag{4.2}$$

Partial differentials are employed in equation 4.2, since the variables have other dependencies e.g. temperature. A linear relation between the V_{CE} and I_C may also be assumed, provided that V_{GE} is kept constant, the IGBT not operating in the active region and with a constant component temperature. This may described by a constant transconductance g_m. The on-state power loss P_{loss} can thus be expressed as:

$$P_{loss} = (V_{fb} + \frac{I_C}{g_m}) I_C \tag{4.3}$$

$1/g_m$ is in some literature and simulation applications such as PSCAD referred to as the ON-state resistance R_{ON}. The switching operations of the IGBT provide additional power loss. During a turn-OFF interval the voltage rises and current will decrease simultaneously and generate power loss as:

$$W_{swichingloss} = \int_{t1}^{t2} V_{CE} I_C dt \tag{4.4}$$

Where $t1$ is the time when switching interval starts, and $t2$ is the time when the switching interval ends. Typical values are including switching times are specified in the manufacture data sheet.

4.1.4 IGBT ratings

In this section some of the parameters rated provided in data sheet for the IGBT is presented, as these values are assumed essential for DC breaker design and simulation studies. The parameters and physics regarding IGBT temperature is discussed in section 5.2.

Rated collector emitter voltage V_{CEmax} Maximum permissible voltage over collector-emitter terminals at module case temperature $T_c = 25$ °C.

Maximum power dissipation P_{tot}

Rated collector current I_{Cmax} Maximum permissible continuous DC current based on the total power dissipation.

Repetetive peak current I_{Crm} Maximum current magnitude exceeding I_{Cmax} for a specified amount of time.

4.2 Metal Oxide Varistor

The Metal Oxide Varistor (MOV) is a non-linear resistor consisting of zinc oxide elements (ZnO) that is normally used for protection applications from low voltage circuits to high voltage power apparatus in which the MOV protects from lightning surges and other overvoltages. In a DC breaker, the MOV may be an essential component for protecting the IGBT from overvoltages such as the TIV, providing the counter-voltage and dissipating the magnetic energy stored in the line inductance. In terms of over-voltages a snubber circuit may also provide protection discussed in section 5.1.1.

4.2.1 MOV Structure

The MOV is consist of ceramic microstructures of ZnO grains coated by an intergranular boundary containing other oxides. A typical ZnO grain diameter size indicated by d in figure 4.6 is typically $10-100$ μm while the intergranular boundary thickness t is typically $0.01-0.1$ μm. For low electric field strength, the MOV elements is highly resistive. However, when exposed to high electric fields it becomes highly conductive. The physical dimensions og the MOV determines the ratings. The capability of voltage is reflected in the length, and the capability to handle currents in the cross sectional area. Thus the absorbing energy capacity is determined by the volume. The MOV is normally capsuled with an insulating barrier [29, 30, 31].

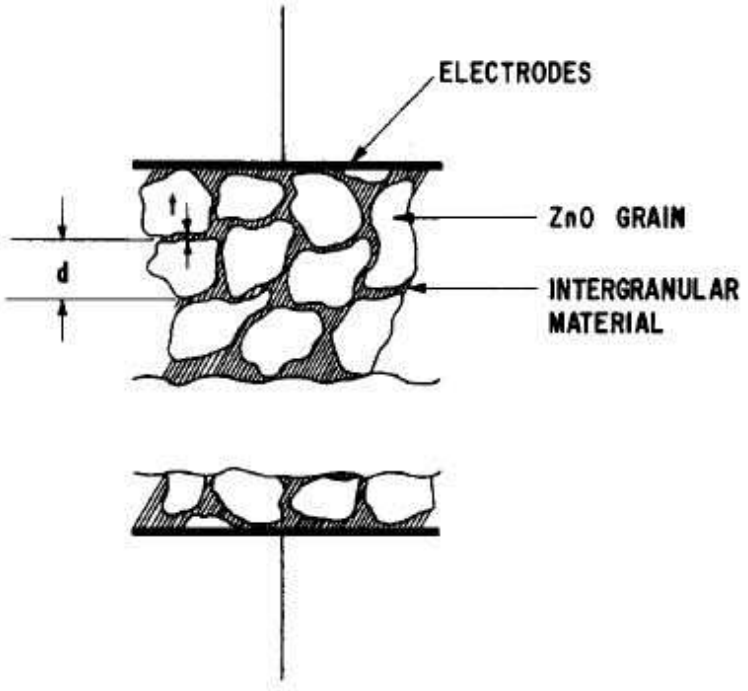


Figure 4.6: Idealized structure of an MOV where d is the diameter of the ZnO grains and t is the thickness of the intergranular region [29]

4.2.2 MOV Voltage-Current Characteristic

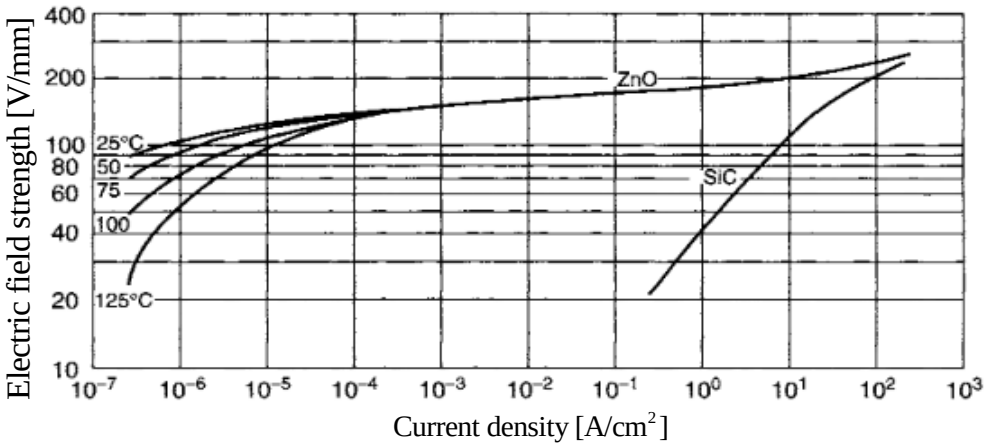


Figure 4.7: Typical voltage-current characteristic of a ZnO MOV with the temperature dependency in the leakage current region, and the older silicon carbide (SiC) surge arrester characteristic also indicated [32].

The combination of the highly conductive ZnO grains an the more resistive intergranular boundary provides a voltage-current characteristic beneficial for overvoltage protection as depicted in figure 4.7. The voltage-current characteristic is divided into three regions [31]:

1. *The leakage current region*
2. *The protective region*
3. *The linear region*

The interfaces of the regions may be gradual. The leakage current region in figure 4.7 may in this case be assumed to be in the range of $10^{-7}-10^{-5}$ A/cm^2 and provides very small currents, related to the high resistivity of the inter granular boundary. In the normal operating region, which in this case can be assumed to $10^{-5}-10^{2}$ A/cm^2, a clear non-linear characteristic is observed. A high rise in the current will provide only a marginal increase in voltage. This effect is associated with the electron tunnelling phenomenon. In the linear region with higher current density from 10^2 A/cm^2 and upwards, the characteristic tends more to linear resistive properties. The leakage current region also has an unfavourable negative temperature coefficient, meaning that an increased MOV-temperature provides higher leakage currents at a given voltage [30]. The VI-characteristics of a given type of an MOV may vary due to minor manufacture fluctuations. A 10 % tolerance band in the voltage at given current should be expected according to [31].

4.2.3 MOV Equivalent Circuit and Equations

The VI characteristic may be expressed as:

$$I_{MOV} = K_{MOV} V_{MOV}^{\alpha} \tag{4.5}$$

Where K_{MOV} is the ceramic material constant and α is the non-linearity exponent dependent on the operating region of the MOV. In the linear region $\alpha = 1$, and in the non-linear region α is determined by the VI-characteristic of the component, and can be found by logarithmic calculations. If a constant MOV-voltage is assumed, the energy dissipated by the MOV during fault clearance may be expressed by as:

$$W_{MOV} = V_{MOV}^{\alpha+1} K_{MOV}\, t_{break} \tag{4.6}$$

Where t_{break} is the break time of the DC breaker, the time interval between the DC breaker trips (peak line current) and the line current I_{line} is zero. If other resistive elements in the DC breaker and in the DC system are neglected, the DC breaker should be able to dissipate energy equal to magnetic energy stored in the DC line and fed by the source during the fault clearance similar to equation 3.9.
Figure 4.8 depicts an simple equivalent circuit of the MOV [31]. More detailed models can be found in [33]. Besides the non-linear property, the MOV also has dielectric properties reflected in C_{MOV} and a certain stray inductance L_{MOV} due to the geometry of the current path. A variable resistor R_{MOV} corresponds to the non-linear resistive property.

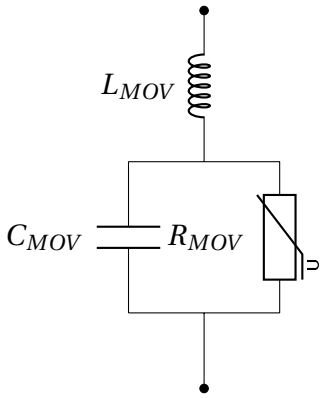


Figure 4.8: MOV equivalent ciruit

4.2.4 MOV Thermal Considerations and De-rating

The energy absorbed by the MOV will be dissipated as heat. If the electrical power losses are bigger than heat dissipation, thermal instability may occur. Thermal instability involves deterioration of the protection capabilities and eventually permanent component failure du to damage of the ZnO materials [30, 34]. Figure 4.9 illustrates this effect. For operating temperatures typically higher than 85 °C, the MOV operating conditions in terms of voltage, surge current, and energy absorption will de-rate [31]. This temperature is also referred to the critical temperature.

The handling of energy absorption is divided into two categories: *Single impulse handling capability* and *thermal energy handling capability*. The former relates to the sudden extreme increase in temperature experienced by an MOV under current surges e.g. fault current and lightning impulses. This sudden temperature rise may lead to damages such as cracks in the ZnO material. The latter thermal energy handling capability, is related to thermal instability which is more associated e.g. continuous electrical stresses and ageing [35].

The performance of the MOV will de-rate under other circumstances such as repetitive surges and the number of surges handled by the MOV in a long term perspective. The impact of de-rating due to temperature and current surges are normally provided in data sheets from the manufacturer.

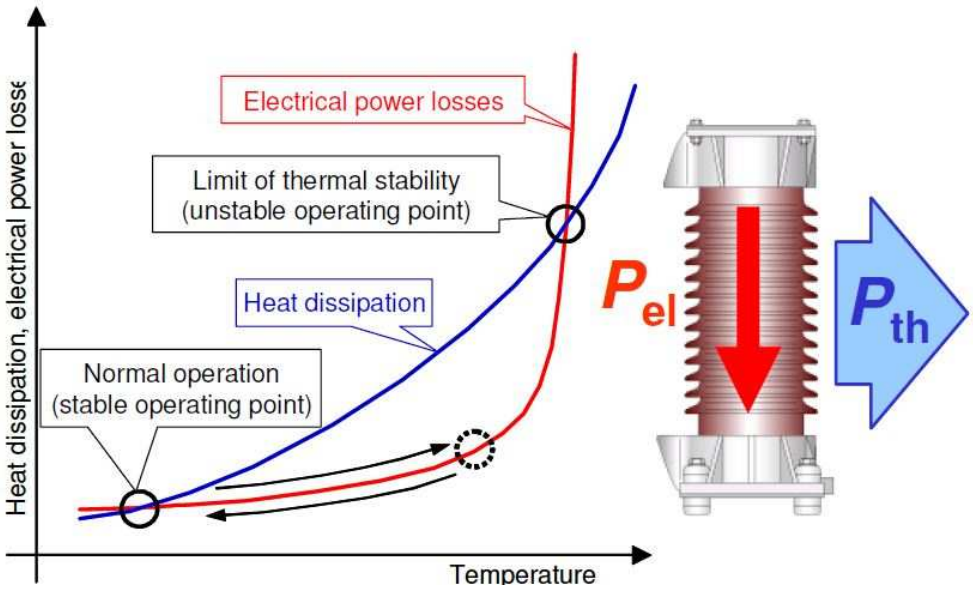


Figure 4.9: Illustration of thermal stability of an MOV[34]

4.2.5 MOV Ratings

The MOV has the following ratings that should be considered for the DC-breaker design. The ratings listed are collected from [30, 31]

Operating voltage V_{MOV} The voltage level (AC or DC) of the MOV that should only be exceeded by transients - hence the maximum permissible voltage under normal operation.

Varistor voltage V_V The voltage level of the MOV with $1mA$ applied .

Maximum energy dissipation $W_{MOV\,max}$ The maxium amount of energy dissipated over a period of 2 ms.

Maximum avarage power $P_{MOV\,max}$ The maxium power dissipation if the MOV has sufficient time to cool between the surges.

Protection level/Clamping voltage V_c The voltage level of the MOV with currents higher than $1mA$ applied.

Critical temperature $T_{critical}$ For temperature exceeding this level de-ratings of the MOV applies.

Chapter 5

Theroretical Background - System Aspects

5.1 Stray inductance and Snubber Circuits

5.1.1 Stray Indcutance

Stray inductance L_σ is the unwanted inductive contribution in the commutations circuit to transient overvoltages occurring during a semiconductor turn-off. For a DC breaker, this means the IGBT turn-off. According to [36], the stray inductance is expressed as:

$$L_\sigma = -\Delta V_{CE} \frac{dt}{dI_C} \tag{5.1}$$

Where ΔV_{CE} is the additional voltage rise over the collector emitter terminals, and dt/dI_C, in this case, the inverse of the slope of the falling collector current when the semiconductor switches off. An example of an idealised turn-off with stray inductance is shown in figure 5.1.
It should be distinguished between the transient overvoltage contribution from L_{line} referred to as TIV and the contribution from L_σ referred to as ΔV_{CE}. L_σ as mentioned unwanted inductance in the commutation circuit and is provided e.g. by the arrangement of the connected wires and geometry of the electrical connections to the components.

5.1.2 Snubber Circuit

A snubber circuit is a parallel branch attached to the semiconductor with the intention of reducing stresses on the component during turn-on and turn-off. During turn-off, transient overvoltages may induced over the component due to stray inducances. For a DC breaker, a parallel capacitor may protect the IGBT from transient overvoltages exceeding V_{CEmax} and thus avoid component failure [37]. The snubber may be realized with a capacitor only, or as a RCD snubber consisting of a diode and a resistor in addition to the capacitor. The snubber should be placed as close possible the protected component as seen in figure 5.2. This will both reduce the stray inductance in the snubber circuit itself and protect the device from the transient over voltage contributions from stray inductances. The energy stored in the snubber capacitor for after a switching operation can be expressed as:

$$W_{Csnub} = \frac{1}{2} C_{snub} V_{CE}^2 \tag{5.2}$$

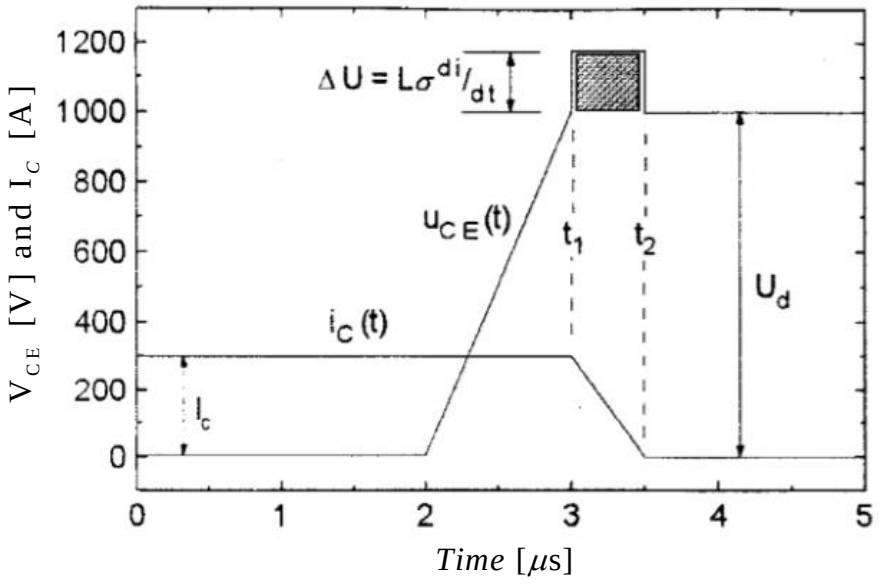


Figure 5.1: Idealised IGBT turn-off transient due to stray inductance[36]

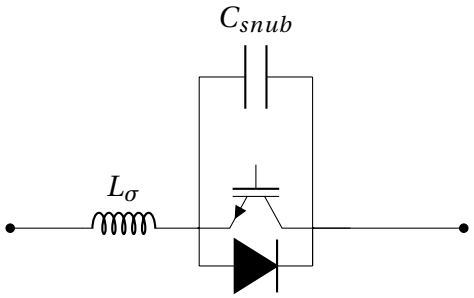


Figure 5.2: IGBT with free-wheeling diode, capacitor snubber circuit C_{snub} and stray inductance L_σ

For a solid state DC breaker using an additional small disk MOV replacing the capacitor snubber in figure 5.2 is also suggested [38]. This MOV may protect the IGBT from transient overvoltages, but without being the major contribution to dissipate the energy in system seen in equation 3.9.

5.2 Thermal Design Considerations

The performance power of semiconductors depends on the temperature of the device. When the component junction temperature T_j, referred the intrinsic temperature, surpasses a certain level, the characteristics of the device are lost and may lead to failure. In the component data sheets the manufacturer specifies the maximum junction temperature T_{jmax}. By practical means, the power loss will increase with the junction temperature, as a self amplifying pro-

cess as temperature will increase even further. Higher junction-temperature may also reduce reliability of the component [25]. Thermal considerations normally includes to determine an adequate heat sink and cooling medium to conduct the heat away from the component in order to maintain the junction temperature below T_{jmax}. In the following sections simplified circuit models is described intended to emulate the dynamics and steady-state characteristics of heat transfer and temperature in semiconductors devices. For simplification only one dimensional heat transfer is considered.

5.2.1 Thermal Resistance

The energy flow or conducted heat P_{cond} per unit time through a section of material may be expressed as:

$$P_{cond} = \frac{\lambda A \Delta T}{d} \tag{5.3}$$

Where λ $[W/m \cdot C°]$ is the thermal conductivity , ΔT $[°C]$ is the temperature difference across the material , d is the length $[m]$ and A $[m^2]$ the cross-section area.
From equation 5.3 the thermal resistance R_θ $[W/C°]$ can be defined as:

$$R_\theta = \frac{\Delta T}{P_{cond}} = \frac{d}{\lambda A} \tag{5.4}$$

R_θ for a given semiconductor is normally provided in data sheets, with typically different values for the layers of the device which in sum may determine the steady-state thermal impedance from the junction to the case surface of the component.

5.2.2 Thermal Capacitance

To obtain an emulation of the dynamic behaviour a thermal capacitance C_θ analogous to electrical capacitance is considered. Thermal transients must be considered when switching, and having rapid changes in currents. This may generate additional heat to the steady state on-state losses. DC grid faults may also provide fast a changing current and additional power loss. The dynamics is related to the thermal heat capacity C_v, which is defined by the change of heat dQ with respect to the temperature change dT. For a square shaped box of an arbitrary material the heat capacity C_v is defined as:

$$C_v = \frac{dQ}{dT} Ad \tag{5.5}$$

5.2.3 Thermal Equivalent Electrical Circiut

The time response is simplified into one dimensional heat conduction which includes exponential behaviour with thermal time constants [25]. The exponential behaviour may be modelled as an electrical RC network intended to emulate both the steady state and the dynamic temperature response. The power dissipated in the semiconductor $P(t)$ is reflected as the current in the network and the temperature as the voltage. An example of a network is shown in figure 5.3 referred to as the Cauer electro thermal model. The voltage $T_1(t)$-T_a represents the temperature difference between layer 1 and the ambient temperature. Layer 1 typically represents the junction in a semiconductor-device. The Cauer model represents a physical approach to transient

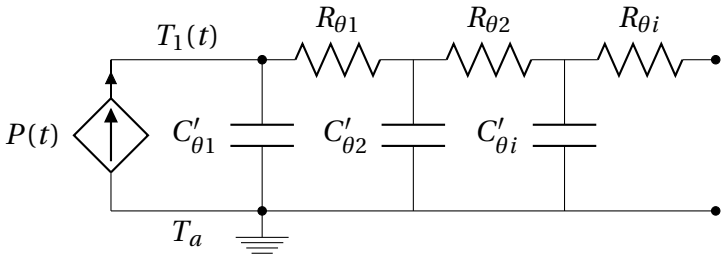


Figure 5.3: Cauer electro thermal model

thermal equivalent impedance, but provides complex calculations to obtain the time constants for each layer [39, 40]. A mathematically simpler model, The Foster model, may be used for thermal calculation instead. This model represents each layer with a time constant and emulates the a time dependent transient thermal-impedance $Z_{\theta jc}(t)$. Figure 5.4 depicts an example of the Foster model. The thermal transient may be fitted into an exponential curve obtained in [39], expressed as:

$$Z_{\theta jc}(t) = \sum_{i=1}^{n} R_{\theta i}(1 - e^{\frac{-t}{\tau_{\theta i}}}) \tag{5.6}$$

Where $\tau_{\theta i}$ is thermal time constant for the respective layers. The Foster model does however not represents the physical layers along the heat conduction path. The circuit parameters in the Foster model are normally given in data sheet as $\tau_{\theta i}$ and $R_{\theta i}$. $C_{\theta i}$ is calculated by:

$$\tau_{\theta i} = R_{\theta i} C_{\theta i} \tag{5.7}$$

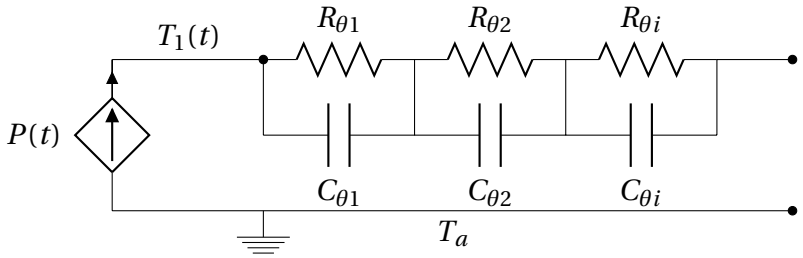


Figure 5.4: Foster electro thermal model

5.3 Heat sinks, Thermal Grease and Cooling Medium

The purpose of using a heat sink is to provide a low thermal resistance heat conduction path between the cooling medium or ambient air and the semiconductor. I.e. is to conduct heat away from the device and maintaining an acceptable component temperature. As seen the in equation 5.3, the heat power loss is conducted to the surroundings by keeping the distance of heat conduction d small and the cross sectional area of the material A big as possible. The heat sink should therefore maximise its surface area, but provide a small path for the heat conduction. Efficient heat-conduction is dependent on the movement of the ambient air or the

cooling medium. Standstill air may result in increasing surrounding temperature, and thus increasing component temperature as $R_{\theta heatsink}$ is expected to be higher. Auxiliary fans attached to the heat sink may contribute to mitigate this effect. Heat sinks have time constants $\tau_{heatsink} = 4 - 15\ min$ typically [25].

A thin layer of thermal grease should be applied between the heatsink surface and semiconductor device in order to avoid having air between the case and heat sink surface. This layer should be as thin as possible such that the total thermal resistance $R_{\theta ja}$ between the junction and the ambient, is not significantly increased. The mounting torque of the device should also be considered, since it may contribute to minimise the amount air between the surfaces.

The maximum thermal resistance of the heat conduction path $R_{\theta ja}$ with the heat sink resistance included can be found by the equation:

$$R_{\theta ja} = \frac{T_{jmax} - T_a}{P_{loss}} \tag{5.8}$$

Where T_{jmax} is the maximum allowable junction temperature, T_a temperature of the ambient, and the P_{loss} the average loss of the semiconductor device.

Chapter 6

Considerations and Description of Laboratory Work

This chapters introduces the NTNU/SINTEF Smart Grid and Renewable Energy Lab including a DC grid, for which the final DC breaker should be designed for. A DC breaker test model used in the design process and a test of a contactor switch is described as well.

6.1 NTNU/SINTEF Smart Grid and Renewable Energy Lab

The NTNU/SINTEF Smart Grid and Renewable Energy Lab is a power system infrastructure built for research related to smart grids and renewable energy generation. The laboratory will further be referred to as the NTNU/SINTEF lab. The NTNU/SINTEF lab consist of different parts including an induction generator, a distribution grid and a DC grid consisting of four interconnected 60 kVA voltage source converters (VSC) intended to emulate a HVDC transmission system. The following section describes the details needed for the DC breaker design. A more detailed description of the laboratory is found in [41, 42].

6.1.1 The 60 kVA Converter

Figure 6.1 shows the configuration of the three main parts. The three main parts of the converter are:

Converter module: IGBT brigdes and DC-link capacitor

Harmonics filter: LCL-type filter

Switchgear: Contactor, charging and discharge circuit.

The converter and the DC grid model has the following rated values:

Rated DC-voltage: 0-750 V

Rated current: 0-100 A

DC-link capacitor bank: $12 \cdot 4700\ \mu\text{F} = 56.4$ mF

IGBT modules: 400 A 1200 V IGBT module, 2 per phase

The DC-link capacitors must be charged by an external circuit before the converter can operate. The IGBT driver circuits are also equipped with overcurrent protection with an adjustable tip-range of $0-800$ A. A technical detailed description of the VSC is given in [43].

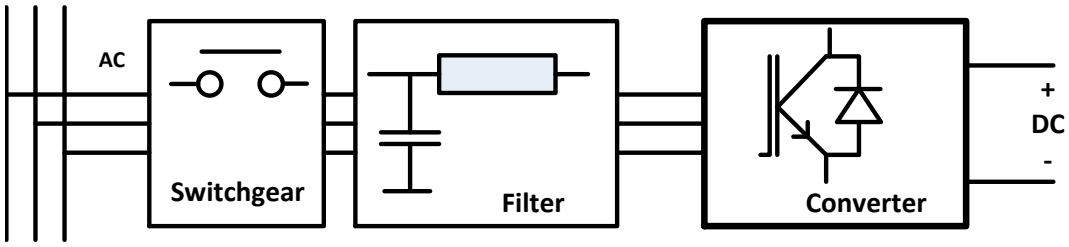


Figure 6.1: Main parts of the 60 kVA VSC for the DC grid in the NTNU/SINTEF lab [43]

6.2 Solid State DC Circuit Breaker Test Model

6.2.1 Purpose

The aim of the experimental work with the test model is to gain insight to the operation of a solid state DC breaker and facilitate the selection of components for the solid-state DC circuit breaker design. This is done by assembling a test model and generating short circuits by discharging a DC-capacitor bank. As previously mentioned, in DC grids the main contribution to the fault current within the first ms of a fault, is the discharge of the DC capacitor [14]. The test model aims to emulate this effect similarly, to what is experted of short circuit behaviour in the DC grid with the 60 kVA lab converter. Constrains and stresses on the components should be assessed, while the results related to the theoretical background, and the correlations and limitations of the simulations done in PSCAD are investigated. Short circuits are generated as pulses by controlling the off- and on-state of the IGBT through a controllable pulse generator and a driver circuit. The basic electrical circuit of the test model is shown in figure 6.2, and the different parts are explained in the following sections.

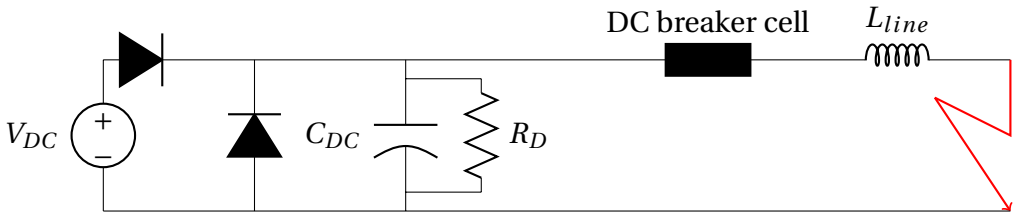


Figure 6.2: Circuit diagram of the test model with one DC breaker cell, DC capacitor bank C_{DC} and discharge resistors R_D. The arrow indicates a short circuit

6.2.2 Voltage Source and DC Capacitor

The capacitor bank C_{DC} consists of eight similar DC electrolytic capacitors of 4700 μF each and are arranged in parallel; in total C_{DC} = 37.6 mF. The capacitor bank is shown in figure 6.3. It is charged with a adjustable DC source $V_{DC} = 0 - 300$ V with a current limitation of 1 A. The use of the DC source is beneficial since it can be connected to the 230 V supply. Blocking diodes are connected in series with the positive pole of the voltage source V_{DC} and in parallel with the capacitor C_{DC}. This is to protect the capacitor bank and the voltage source from high inrush currents during short circuits. For safety reasons, 8 high ohmic discharge resistors of R_D =47 kΩ each, are connected in parallel with the 8 capacitors. The resistors dissipate the stored energy and ensure 0 V capacitor terminal voltage when not in use.

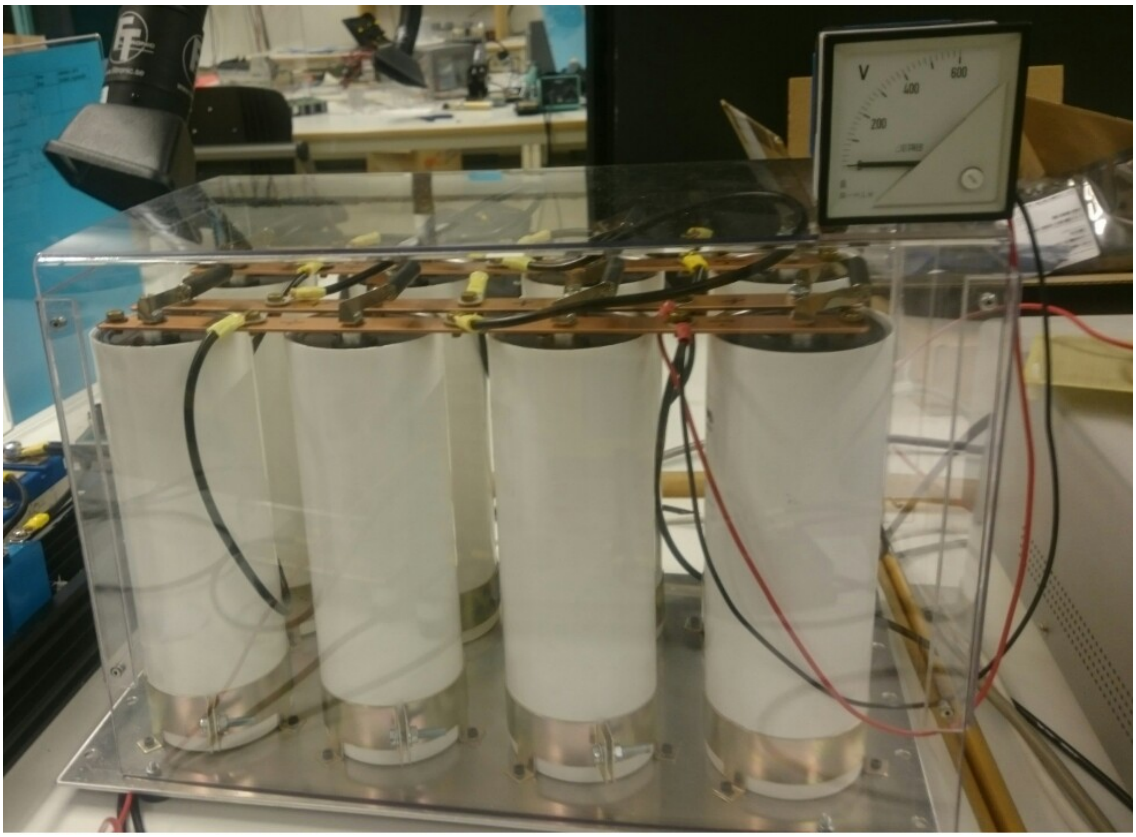


Figure 6.3: Test model capacitor bank C_{DC}

6.2.3 Solid State DC Circuit Breaker

Configuration

Figure 6.4 depicts the configuration of the DC breaker, and figure 6.5 shows the set up. The IGBTs used are SIEMENS Single switch IGBT Power Modules with free-wheeling diodes. The ratings are listed in table 6.1. The data-sheet is attached in appendix A. For the basic configuration in figure 6.4, an MOV is connected in parallel with a set of the SIEMENS IGBT modules in anti-series according to the solid state DC breaker topology. The MOV types used in the experiments

are EPCOS high-energy varistors and are listed in table 6.2. The MOV indicated in figure 6.4 is named Energy MOV, as it is mainly used for energy dissipation in the experiments related to the test model. Transient overvoltage suppression due to stray inductances is provided by solutions which will be explained in chapter 8. The IGBTs in anti-series are named $A-$ and $A+$, since the control system originally is design for a 3-phase converter.

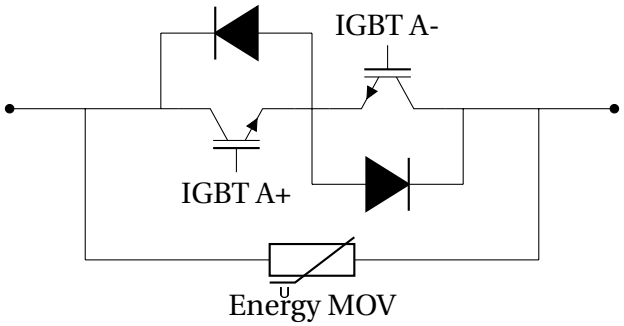


Figure 6.4: Basic configuration circuit diagram of the DC breaker in the test model

Figure 6.5: Basic configuration of the DC breaker in the test model

Table 6.1: Ratings for SIEMENS SM 300 GA 120 DN2 Single switch IGBT module

SIEMENS Single Swith IGBT	
V_{CEmax}	1200 V
I_{Cmax}	430 A (DC)

Table 6.2: MOV types in the test model and their operating DC voltage

MOV type	**Operating DC voltage** V_{MOV} [V]
B32K130	170
B32K275	350
B32K385	505
B32K420	560

Gate Driver and Control System

A gate driver circuit controls the gate voltage of the IGBT and thus the switching between on- or off-state. In on-state, the gate driver ensures a gate-emitter voltage $V_{CE} = 12 - 15V$, depending on the gate driver power supply. The gate driver used in the test model is SINTEF Gate Driver SMD2 [44]. Galvanic isolation is realised using optocouplers in the gate driver circuit avoiding electrical contact between the power circuit, the control system equipment and ground potential. The gate driver has implemented a local short-circuit protection that switches the IGBT from on- to off-state at a certain detection level of V_{CE}. This is measured to $V_{CE} = 4.2V$ with a potentiometer. In the original description of the driver the detection level is $V_{CE} = 8\ V$. During a short circuit, the current may rise so high that the IGBT operates in the active region. Compared to normal operation, higher V_{CE} is provided and the local protection may trip. This mechanism should be avoided under experiments, since a DC breaker in a DC grid should interrupt short circuit current detected by an external protection in order to comply with the selectivity criterion. The local short circuit protection should however not be removed as it provides back-up protection in case of external protection failure.

The signals to the drivers are provided by a driver interface card [45]. This is the signal interface between the rest of the control system and the gate driver. The driver interface is originally intended for VSC control applications and contains logic circuits that ensure that the controlled switches will not be in a risk of failure or short-circuit. I.e. circuit logic to prevent the IGBTs on the same bridge leg in a VSC are in on-state simultaneously. This feature is unfavourable for a DC breaker in the test model as at least two IGBTs are placed in anti-series and switched on simultaneously. The gate interface is therefore adjusted and this function removed. The input control signals are provided by a circuit board *Vekselretter Testkort* [46] connected to a signal/pulse generator. An outline of the control system set-up described in this section is illustrated in figure 6.6

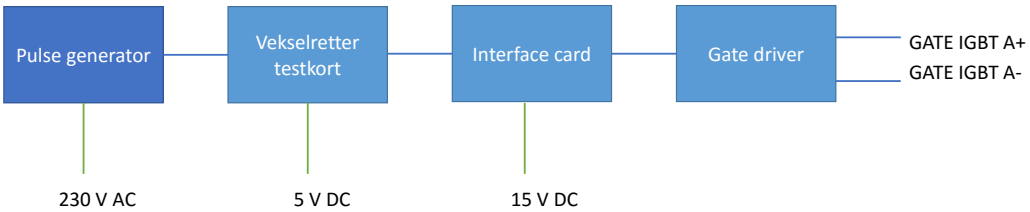


Figure 6.6: Ouline of the gate driver and control system in the test model

6.2.4 Inductive Element

The inductance L_{line}, indicated in figure 6.2, represents an inductive property in a DC line or a cable. The inductance should be varied as faults may occur on different locations a DC-grid. Low inductances may represents short circuits near the converter stations, and the higher value, the further fault distance from the converter station. Linear inductors are used, such that the inductance is not affected by the magnitude of the current. The inductances used are listed in table 6.3

Table 6.3: Inductors used in the lab test model

Inductor	**Inductance** [μH]
L_1	44.5
L_2	119.5
L_3	1091.6

6.2.5 Measurement Technique

In order to capture the voltage and current waveforms a TEKTRONIX TDS 2014 oscilloscope is used. The current is measured via a current clamp meter, LEM sensors and a Rogowski coil. The voltage is measured with differential probes and provides galvanic isolation to avoid ground potential contact. A temperature transducer is also used for measuring the surface temperature of the components and connected to an Agilent LXI data acquisition unit.

6.2.6 Limitations

The test model described will have some limitations. Relevant correlations for the DC breaker design for the NTNU/SINTEF lab as well as a full scale DC grid may not be tested. The test model has no load and only short circuits are generated, meaning that the on-state losses under normal operation (non-fault state) cannot be investigated. Thus heating of the semiconductors and the MOVs under the mentioned circumstances cannot be investigated directly. There is also no protection system, and the durations of the short circuits are manually controlled by the *Vekselretter Testkort* and the signal generator. A contactor switch is not included in the set-up of the test model. And therefore the interaction between this component and remaining cannot be tested directly.

6.3 Contactor Switch Test

Physical isolation is needed after the DC breaker has forced the current to zero in a DC grid. This is to provide a separation of the faulted parts from the healthy parts in the power system. For the DC breaker in the NTNU/SINTEF lab, a contactor switch in series with the DC breaker is suggested for this application. Therefore some testing of this device will be undertaken.

The contactor should be able to isolate and break eventual residual current that may occur after the DC breaker has forced the short circuit current to zero. The contactor will be in

the series with L_{line} and will thus interrupt residual inductive current. As seen in the theoretical background section 3.1 this may be problematic as the inductance will try to maintain a constant flux and induce high voltages if the current is interrupted. An experimental test is undertaken in order to investigate the behaviour of the contactor switch under the mentioned circumstances. The purpose of this test is to provide predictions of the operation of a contactor switch for isolator applications in relation with a solid state DC breaker. The set up of the test is shown in 6.7 A contactor switch for DC applictations of type KILOVAC EV200 [47] is tested with

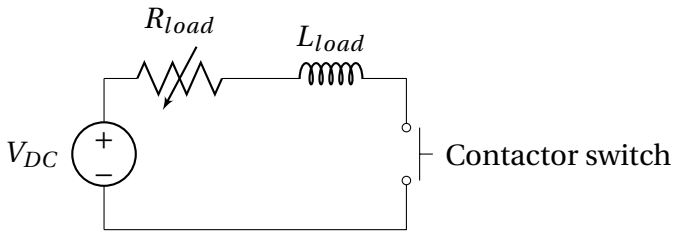


Figure 6.7: Contactor switch test circuit

an inductive load L_{load} = 117 mH, an adjustable resistor R_{load} controls the current and a voltage source V_{DC} = 300 V. The test circuit seen in figure 6.7. The switches is controlled by a DC supply V_{coil}, providing voltage to a coil energising an electromagnet inside the contactor switch housing. When the supply is switched on, i.e V_{coil} = 24 V, current conducts freely through the main contacts. When the supply is switched off, i.e. V_{coil} = 0 V, the switch is isolating as the electromagnet is demagnetised. The contactor switch also has auxiliary contacts which are open when the contactor is open. The voltage of the auxiliary contacts is referred to as V_{aux}. These contacts may be used to provide signals to the control system. The detailed electromagnetic and mechanical operation the structure of a DC contactor switch can be studied in [48].

Chapter 7

PSCAD DC Breaker Model

This chapter describes the development of a simulation model of the DC breaker in Power System Computer Aided Design (PSCAD). Preliminary simulations are performed prior to the experiments of the test model described in 6.2 in order to predict the results in the experimental work. The results from these simulations should also be compared to the experimental results from the test model and adjuste d accordingly to obtain a more realistic, but simplified simulation model. This process should also indicate the limitations of the simulation model.

7.1 Software Description

PSCAD is a graphical interface for Electromagnetic Transient Programming (EMTP). EMTP is a numerical solution method that involves electrical networks modelled as differential equations. The time response is solved using the trapezoidal method. The results provide accurate transient time responses as the solution time-step t_{step} is adjustable [14]. Details regarding EMTP can be studied in [49].
For modelling and simulating a DC breaker, a small time-step solution by trapezoidal calculations will be favourable in order to simulate fast switching operations of IGBTs and the nonlinear properties of the MOV.

7.2 DC Breaker

The DC breaker PSCAD simulation model has the same basic components as the the test model shown in figure 6.4. The simulation model is shown in figure 7.1. The parameters for the IGBT and the diode are obtained from the data-sheet from the manufacturers. The respective on-state voltage drops are obtained by the equivalent on-resistance or transconductance by interpolation of the VI characteristic similar to the approach discussed in section 4.1.2. The true VI-characteristic of the IGBT and the diode are not exactly linear, such that the interpolation is done in the expected area of operation in the VI-characteristic. $T_a = 25\ °C$ is assumed initially. The MOV VI-characteristic is also obtained from the manufacturer. Initially, 10 data-points from the characteristic are implemented.

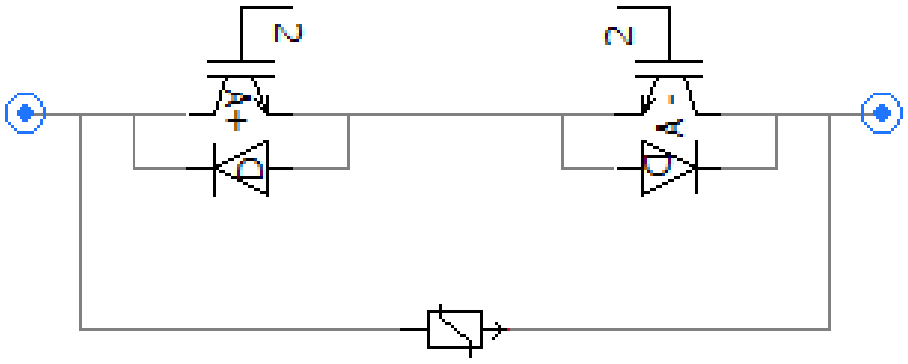


Figure 7.1: Basic DC breaker model in PSCAD

7.3 DC Grid

7.3.1 DC Line

The DC line model is modelled with an inductor and a resistor in series. There are existing more complicated frequency dependent models for overhead lines (OHL) and cables in PSCAD suitable for full scale system simulations as described in [49]. For both the test model and as a starting point for the DC grid in the NTNU/SINTEF lab a simple configuration shown in figure 7.2 is used. In the preliminary simulations the resistor is set to zero since there is only an inductor in the test model, as seen in figure 6.2. The internal resistance in the inductor and the wires are assumed to be insignificant in the preliminary simulations.

Figure 7.2: DC line model in PSCAD

7.3.2 Voltage Source, Capacitor and Load

For simulations of the test model the voltage source and the DC capacitor bank is implemented as shown in figure 7.3. The Ideal breakers, indicated as BRK1 and BRK2, control the charging and discharging of the capacitor bank. No load is implemented since only short circuits are generated as seen in figure 6.2. The discharging resistor R_D is omitted in the simulation model due its to high time-constant value compared to the duration of the short circuit. As a simplification,the NTNU/SINTEF lab DC grid converter is implemented as a single voltage source. Implementation of a real VSC model would require more complicated models including a converter control system. Similar simplification has been done in [14, 50]. The load in the NTNU/SINTEF lab DC

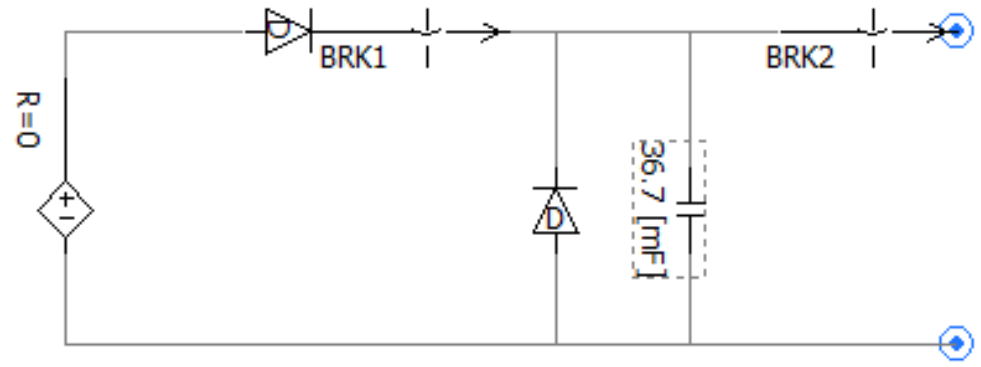


Figure 7.3: Test model capacitor and voltage source in PSCAD

grid PSCAD model is implemented as a controllable voltage source and set to zero when a short circuit is simulated.

7.4 Overcurrent Protection

A protection system is assumed for the NTNU/SINTEF lab DC grid. The selected approach in PSCAD is to implement a simple overcurrent protection. This is done by simple logics, in this case a J-K latch, witch is trigged by a signal comparator when the line current exceeding a specified magnitude. The protection system response time $t_{response}$ is emulated via a time delay function.The PSCAD overcurrent protection implemented is shown in figure 7.4. The interpolation capability in PSCAD is used, and therefore the J-K latch needs two signals for each input.

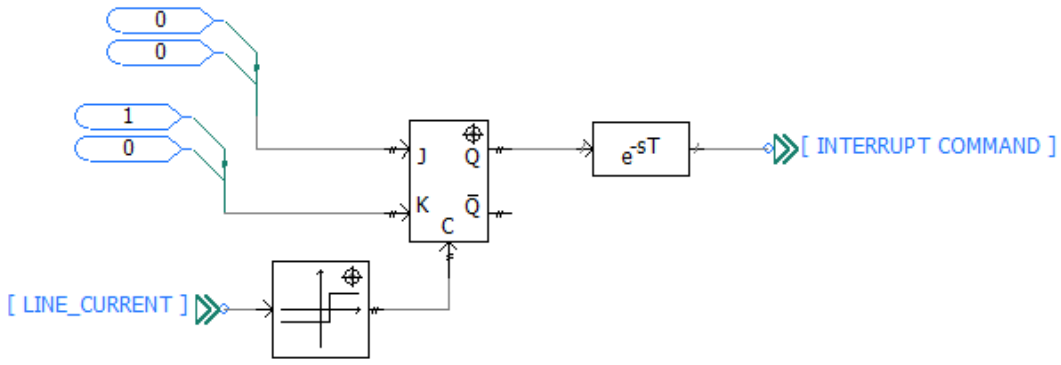


Figure 7.4: Protection system model in PSCAD with line current comparator, the J-K latch, and the time delay function

7.5 Electro Thermal Circuit

For obtaining the expected temperatures of the IGBT modules, an electro thermal circuit is created. The Foster model described in section 5.2.3 is implemented in the DC breaker simulation model for the NTNU/SINTEF lab presented in figure 7.5. The parameters are collected from the data sheet of the respective component (IGBT and anti-parallel diode). A heat sink time constant is typically $\tau_{heatsink}$ =4-15 min which will require inefficient simulation time to reach steady state. The time constant of the heat sink is therefore set to $\tau_{heatsink} = 4$ s such that steady state simulation will be obtained faster in simulations, however still insignificantly effected internal temperature rise due to short circuits and current interruption which is in the range of ms. The P_{loss} due to short circuit currents and steady state is assumed much higher than due to IGBT switch-off, and the switching losses are therefore neglected. The ambient temperature is set to 25 °C which is equivalent to the indicated ground potential indicated in figure 7.5.

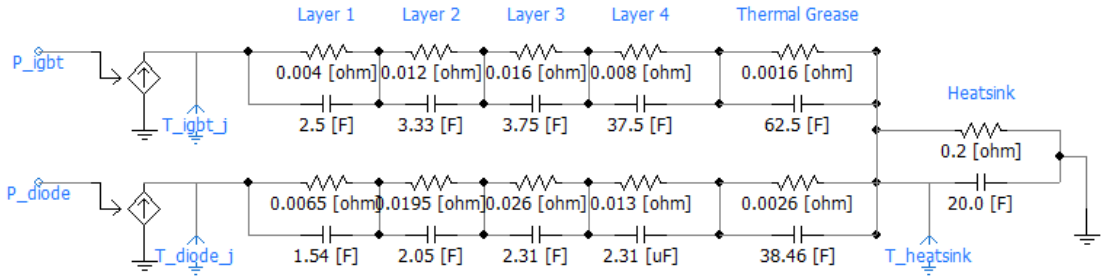


Figure 7.5: Foster electro thermal circuit for the NTNU/SINTEF lab DC breaker model in PSCAD

Chapter 8

Results

This chapter presents the main results from laboratory work with the DC breaker test model described in section 6.2 including a comparison with the preliminary simulations in PSCAD. Thereafter the PSCAD model is adjusted to match the experimental work in order to obtain a more realistic DC breaker model. The results from testing of the contactor switch described in section 6.3 is also presented. All results are processed in and plotted with MATLAB.

8.1 Objective of Results Analysis

Before presenting the results a brief discussion is carried out in order to determine what values are of interest and hence should be obtained from the experimental work.

The peak value of IGBT A+ voltage, peak V_{CE}, is examined as it may exceed the V_{CEmax}. The peak line current I_{line} should also be included. As seen in section 3.1.2 and 5.1.1, the higher currents interrupted, the higher transient overvoltages provided. The peak I_{line} may also be an indication on the stresses due to different fault currents interrupted. The energy dissipated in the energy MOV per fault clearance W_{MOV} and the instantaneous power P_{MOV} of the energy MOV is of interest. These values should be within the maximum ratings of the component to prevent deteriorating temperature rises and eventually failure. The break time t_{break} is also obtained from the results, since a DC breaker should interrupt and force the fault current to zero in the shortest amount of time.

For the contactor switch, the voltage V_{switch} and the current I_{switch} should be measured as these value provides the current breaking behaviour of the switch. The corresponding control signals is measured in the form the voltage over the electromagnetic coil V_{coil} and the auxiliary contact V_{aux}.

Tables 8.1 and 8.2 present the values which will be obtained from the experimental work. Table 8.2 presents the values calculated in MATLAB.

8.2 Laboratory Test Model Results

This section presents the main results An overview of the test model operation principles is presented initially followed by detailed analysis of different aspects of a DC breaker. The details of the test model set up is described in section 6.2.

Table 8.1: Explaination of values measured

Symbol [unit]	Explanation
I_{line}[A]	Line currnet
V_{line} [V]	Line voltage, represented as the voltage over inductor
V_{CE} [V]	Collector emeitter votage IGBT A+
I_{MOV} [A]	Energy MOV current
V_{MOV} [V]	Energy MOV voltage
T_{MOV} [°C]	Energy MOV temperature
V_{DCCB} [V]	Circuit breaker cell voltage
I_{switch} [A]	Contactor switch current
V_{switch} [V]	Contactor switch voltage
V_{coil} [V]	Contactor switch main coil voltage
V_{aux} [V]	Contactor switch auxiliary contact voltage

Table 8.2: Explanation of values calculated

Symbol [unit]	Explanation
P_{MOV} [kW]	Instantaneous power in the energy MOV , the product of V_{MOV} and I_{MOV}
W_{MOV} [J]	Dissipated energy in the energy MOV, time integral of P_{MOV} calculated with the trapezoidal method
t_{break} [ms]	DC breaker break time, the time interval from peak line current to zero line current(I_{line} = 0 A)
I_C [A]	Collector current of the IGBT A+, $I_C = I_{line} - I_{MOV}$
t_{zero} [ms]	Time interval from V_{coil} is set to 0 V to I_{switch} = 0 V
t_{aux} [ms]	Time interval from V_{coil} is set to 0 V to V_{aux} is open circuited

8.2.1 Principle of Operation

For showing principle of operation of the DC breaker test model, an initial experiment using the parameters listed in table 8.3 is undertaken.

Table 8.3: Parameter values in the initial experiment

Parameter	Value
V_{DC}	200 V
t_{pulse}	1 ms
L_{line}	1091.6 μH
Energy MOV	350 V DC

Figure 8.1 shows the entire time period from the initiation of the short circuit to the short circuit clearance. When the IGBT A+ is switched to on-state, the voltage over L_{line}, $V_{line} = V_{DC} - V_{DCCB}$. V_{DCCB} is the sum of the voltage drop over the IGBT A+ and the anti-parallel diode of IGBT A-. Seen in figure 8.1, V_{line} can be assumed constant in the duration of the short circuit. A constant V_{line} provides thus a constant positive slope of I_{line} similar to equation 3.3. After the short circuit duration of t_{pulse}, the IGBT A+ switches off and commutates the current into the energy

MOV. During this commutation seen in figure 8.2, two connected phenomena are observed: The peak voltage of IGBT A+ and the inrush current in the energy MOV. First the voltage rise over the IGBT and the initial inrush current to the varistor are observed. Due the fast change in current, the stray inductance contributes to an additional voltage rise ΔV_{CE}, explained in the theoretical background by equation 5.1. The traces of a damped oscillation in the waveform during the commutation may be explained by an interaction between the stray inductance, parasitic capacitances and the resistive property of the energy MOV. After the oscillations, the voltage over the DC breaker V_{DCCB} behaves similarly to the V-I characteristic of the MOV. In figure 8.1, it is observed that $V_{DCCB} > V_{DC}$ and thus $V_{line} < 0$, according to the discussion with the counter voltage principle described in section 3.2. The counter voltage provides at this point a negative slope of the I_{line} as long as $V_{line} < 0$ is satisfied. When I_{line} approaches zero, the V_{DCCB} drops rapidly as the energy MOV now operates in the leakage current region. Eventually $V_{DCCB} = V_{DC}$. At this point, only residual leakage current from the MOV and IGBT module will flow. This current must be interrupted by an isolation switch such as a contactor to ensure complete short circuit clearance and physical isolation.

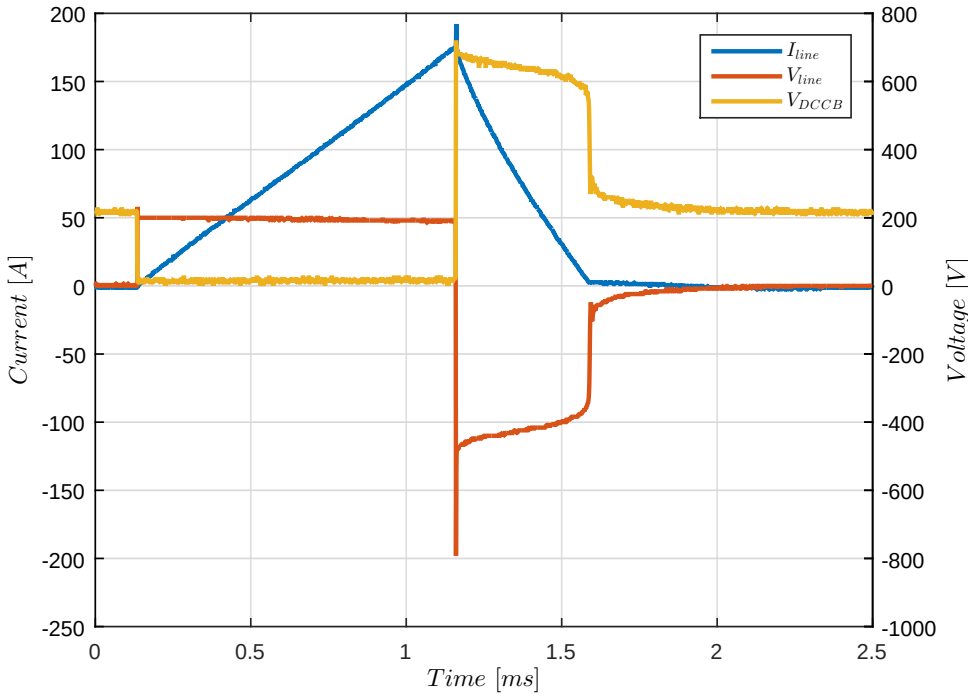


Figure 8.1: Interruption of a short circuit in the test model with V_{DC} = 200 V, L_{line} = 1091.6 μH, V_{MOV} = 350 V and t_{pulse} = 1 ms

8.2.2 Effect of Line Inductance

The purpose of the experiments discussed in this section is to investigate the effect a line inductance for the operation of a DC breaker and thus the implication of the fault location as discussed in section 6.2.4. The experiments are conducted with the fixed parameters listed in

table 8.4. The inductance L_{line} is varied between L_1, L_2 and L_3, listed in table 6.3.

Table 8.4: Fixed parameters for the test with variation of line inductance L_{line}

Parameter	**Value**
V_{DC}	50 V
t_{pulse}	0.2 ms
Energy MOV	170 V DC

Table 8.5: Results in the test with variation of line inductance L_{line}

L_{line}	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
$L_1 = 44.5\ \mu$ H	249.02	316.00	27.07	0.485	0.030
$L_2 = 119.5\ \mu$ H	78.43	282.00	13.50	0.230	0.033
$L_3 = 1091.6\ \mu$ H	10.88	240.00	4.21	0.039	0.034

It can be observed from the results in table 8.5 that a smaller inductance provides a steeper slope of the short circuit current, since the peak current is increasing with smaller L_{line} for a constant t_{pulse}. The results show some of the consequences of higher currents: A higher transient overvoltage ΔV_{CE} due to stray inductances, and higher instantaneous power and energy dissipated in the energy MOV as discussed in section 3.3. It can be seen that higher currents due to low

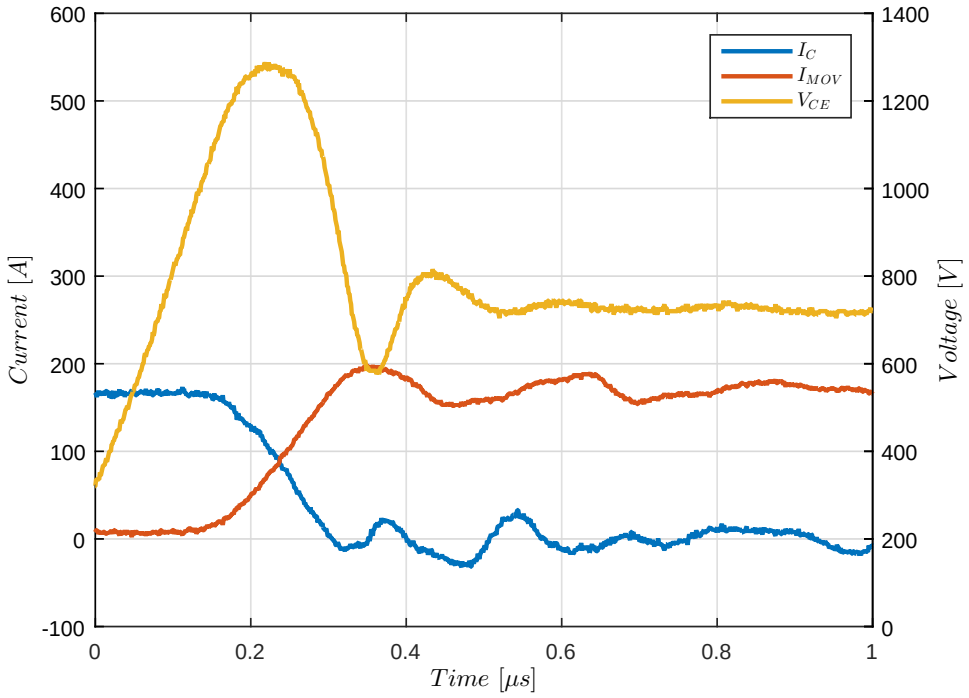


Figure 8.2: Commutation of I_{line} from the A+ IGBT into the energy MOV under a short circuit current interruption $V_{DC} = 200V$, $L_{line} = 1091.6\ \mu H$, $V_{MOV} = 350\ V$ and $t_{pulse} = 1ms$

inductance contribute significantly more to the energy dissipated in the MOV than the inductance according to equation 3.9. The results also show an insignificant variation in t_{break} due to the marginal change in the voltage of the energy MOV with the variation of the peak current seen in the V-I characteristic in figure 4.7.

Inductance and Damping

The variation of inductance affects also the damping of oscillations after the energy MOV voltage has dropped to zero. A smaller inductance, or a shorter DC line, also has lower resistance. Figure 8.3 shows that the result is voltage oscillations with poorer damping compared to figure 8.1. It can be assumed that these oscillations are caused by capacitive properties in the DC breaker such as parasitic capacitance of the IGBT modules and smaller line resistance. Besides voltage oscillations, small residual current oscillations are also observed. As mentioned a contactor is suggested to interrupt this current.

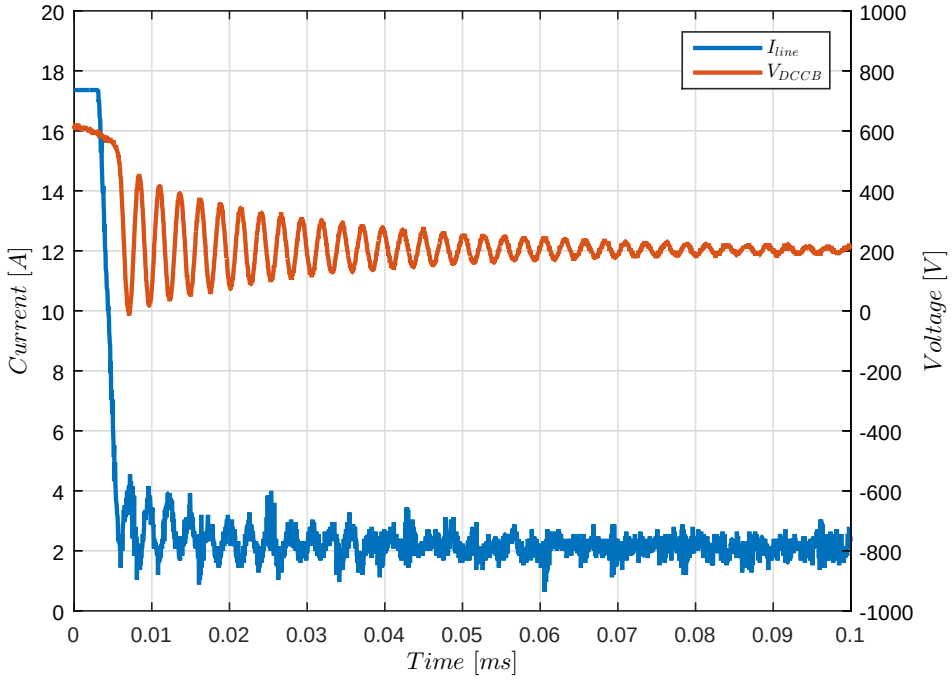


Figure 8.3: Effect of damping, inductance and residual currents after short circuit clearance with V_{DC} = 200V, L_{line} = 45 μH , V_{MOV} = 350 V and t_{pulse} = 70μs

8.2.3 Effect of Detection Time

A protection system may have a certain response time or time delay from the fault detection to the DC breaker trips. The effect of this delay is investigated in this section by varying the duration of the short circuit, by means of adjusting the pulse length t_{pulse}. The constant parameters used in the experiments are listed in table 8.6. The results presented in table 8.7 indicates that a

Table 8.6: Fixed parameters in the test with variation of detection time or t_{pulse}

Parameter	**Value**
V_{DC}	50 V
L_{line}	1091.6 μH
Energy MOV	350 V DC

longer pulse time provides a higher current to interrupt for the DC breaker. As the source voltage and inductance are constant, the rising short circuit current slope must be the same for all t_{pulse}. The effect of higher currents is similar to the discussion in section 8.2.2: Higher peak V_{CE}, higher P_{MOV} and higher W_{MOV}. The undesirable effect of overvoltages due the stray inductance is also clear in this case as $V_{CE} > V_{CEmax} = 1200\ V$ is observed. Since the line inductance is the same for all t_{pulse}, and the energy MOV voltage V_{MOV} only changes marginally, the negative current slope of I_{line} is approximately the same for all t_{pulse}. This is also according to equation 3.4 described in the theoretical background. Therefore, t_{break} increases with higher peak line current I_{line} being interrupted.

Table 8.7: Results from test with variation of detection time or t_{pulse}

t_{pulse} [ms]	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
2	92.16	970.00	46.80	3.48	0.143
4	170.59	1160.00	78.00	10.11	0.257
6	235.29	1270.00	95.04	15.85	0.331

8.2.4 Effect of Source Voltage

As the voltage of a VSC in the NTNU/SINTEF lab may be varied, variation of the source voltage V_{DC} of the test model is examined. The fixed parameters used in the experiments conducted in this section are listed in table 8.8.

Table 8.8: Fixed parameters in the test with variation of V_{DC}

Parameter	**Value**
L_{line}	1091.6 μH
t_{pulse}	1 ms
Energy MOV	350 V DC

The results listed in table 8.9 show that a higher source voltage V_{DC} provides a higher current slope. Thus a higher current is interrupted for the same duration of the short circuit. The effects of higher I_{line} are similar to the results in section 8.2.2 and section 8.2.3 in terms of the correlation between higher currents and peak V_{CE}, peak P_{MOV} and W_{MOV}. The break time t_{break} is however longer since a higher voltage V_{DC} provides a smaller negative voltage drop over L_{line}.

Table 8.9: Results from the test with variation of V_{DC}

V_{DC} [V]	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
100	98.03	970	23.76	2.318	0.160
200	215.68	1240	51.68	12.60	0.434
300	349.02	1370	67.20	32.18	0.902

8.2.5 Effect of Energy MOV

For the final DC breaker design, a suitable energy MOV should be determined. Therefore both the effect of the rated MOV voltage and the heating, discussed in section 4.2.4, will be examined.

Variation of Energy MOV

The rated voltage of the energy MOV is varied, and fixed parameters used in this experiment are listed in table 8.10. The results are shown in table 8.11.

Table 8.10: Fixed parameters in test with the variation of MOV

Parameter	**Value**
V_{DC}	200 V
t_{pulse}	1 ms
L_{line}	1091.6 μH

The peak current varies insignificantly, due to constant L_{line}, t_{pulse} and V_{DC}. The peak voltage of V_{CE} varies and increases with rising rated energy MOV voltage, and thus also provide an increasing peak instantaneous power of the energy MOV. The break time t_{break} decreases and therefore also W_{MOV} decreases. This can be explained by a higher counter voltage provided by the energy MOV due to a higher voltage rating V_{MOV} as described in section 3.2 and section 3.3.

Table 8.11: Results from the test with variation of energy MOV

Energy MOV	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
$V_{MOV} = 170\ V\ DC$	200	896	57.7280	41.36	1.8390
$V_{MOV} = 350\ V\ DC$	217.7419	1288	122.8200	20.0644	0.4144
$V_{MOV} = 560\ V\ DC$	193.5484	1424	173.0400	15.591900	0.2346

Energy MOV Temperature

For examining the temperature of the energy MOV, repetitive short circuits are undertaken with a period of 10 s between each short circuit. The MOV temperature measurement should indicate of the ability of DC breaker to interrupt current repetitively. Repeating current interruptions for a DC breaker may occur if the DC breaker has an auto-reclosure ability or in a situation of load switching between lines in a DC grid. The fixed parameters, listed in table 8.12, are

Table 8.12: Fixed parameters in the test with repetitive short circuits in Energy MOVs temperature measurement

Parameter	**Value**
V_{DC}	300 V
t_{pulse}	0.75 ms
L_{line}	1091.6 μH
Energy MOV	560 V DC

Table 8.13: Results from the test with energy MOV heating

peak I_{line} [A]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
203.92	144.17	33.81	0.602

chosen to maximise the energy dissipated without risking component failure. In the experiment the surface temperature is measured which means that the internal temperature of the Energy MOV, i.e. the temperature of the ZnO element, may increase more rapidly. An example of the values obtained, but temperature, are presented in table 8.13. Figure 8.4 depicts the surface temperature under repetitive short circuits of a period of 10 seconds.

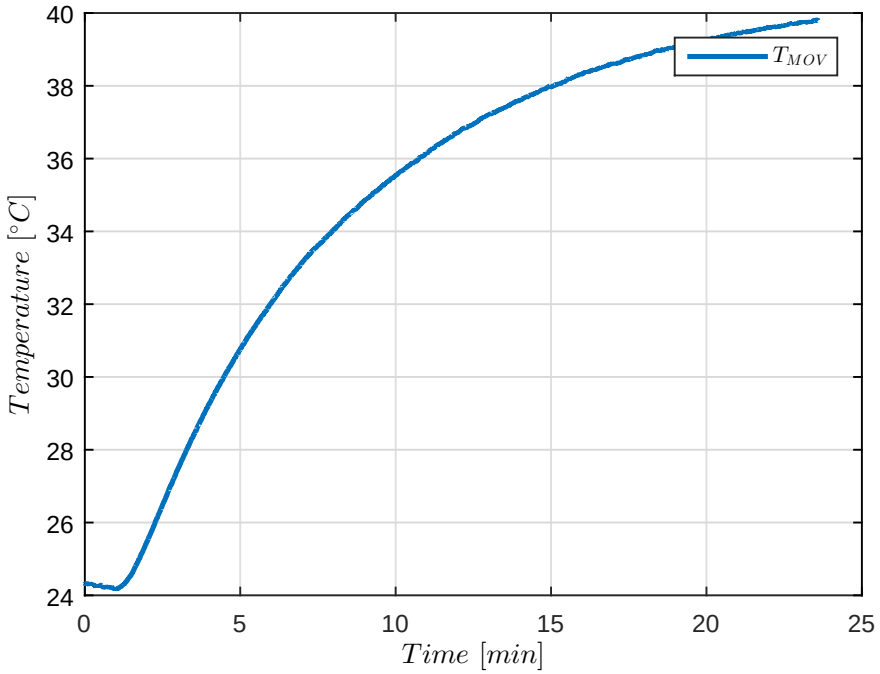


Figure 8.4: Heating of the Energy MOV V_{MOV} = 560 VDC with repetition of a 0.75 ms short circuit with period of 10 s

Figure 8.5 shows the air cooling of similar rated 560 V MOV, i.e. without auxiliary cooling equipment. The cooling curve has an exponential behaviour, and the curve fitting tool in MAT-

LAB generates the following equitation:

$$T_{MOV}(t) = 108.3e^{\frac{-t}{\tau_1}} + 19.62e^{\frac{-t}{\tau_2}} \tag{8.1}$$

Where t is the time [s], T_{MOV} [°C] the energy MOV temperature, $\tau_1 = 471.70$ s and $\tau_2 = 9727.62$ s. In figure 8.5 and equation 8.1 τ_1 is dominating. And the second term in equation 8.1 may be simplified to a constant:

$$T_{MOV}(t) = 108.3e^{\frac{-t}{\tau_1}} + 19.62 \tag{8.2}$$

The thermal time constant of cooling of the simplified curve is thus approximately between 7 and 8 minutes. Curve fitting is also possible for the heating of the energy MOV in figure 8.4. However, as the time period between repetitive pulses may change, the result will also vary accordingly.

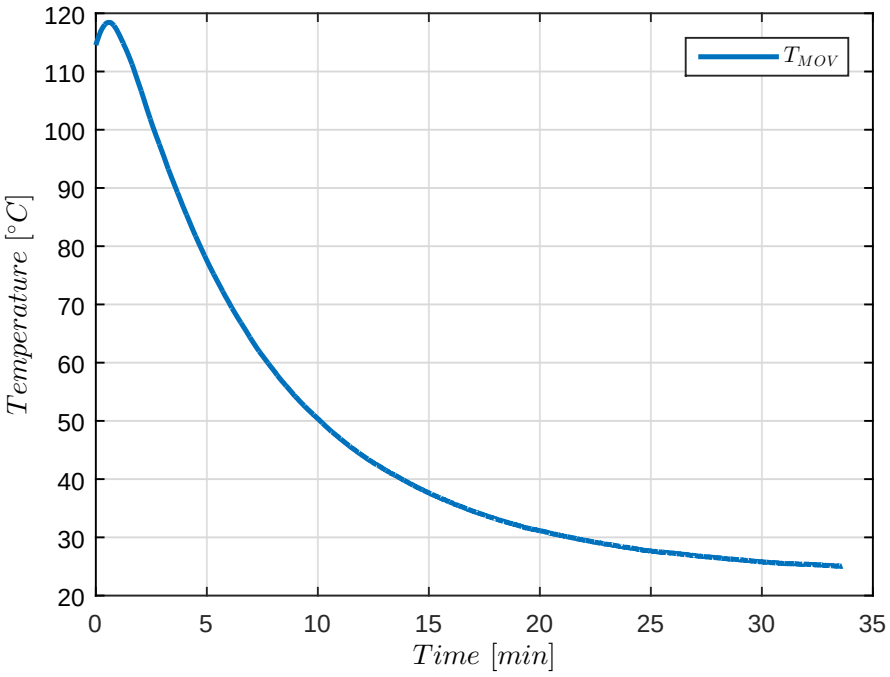


Figure 8.5: Cooling curve of the energy MOV with $V_{MOV} = 560\ V$ DC

8.2.6 Effect of a Snubber Circuit

As mentioned in section 5.1.1, the purpose of using a snubber circuit is to minimise the switching transient overvoltages occurring due to stray inductances. The conventional solution is to use a capacitor snubber over the collector-emitter terminals of the IGBT. Using an MOV as snubber has been suggested for DC breaker applications [51]. The snubber MOV should have a higher voltage rating than the energy MOV, such that the energy MOV will have a lower ohmic path and dissipate the most of the energy referred to in equation 3.9. The fixed parameters under the experiment are the same as in the initial experiment listed in table 8.3. In addition, the snubber MOV has rated voltage $V_{snubMOV} = 680$ V which is a standardD series type varistor [52].

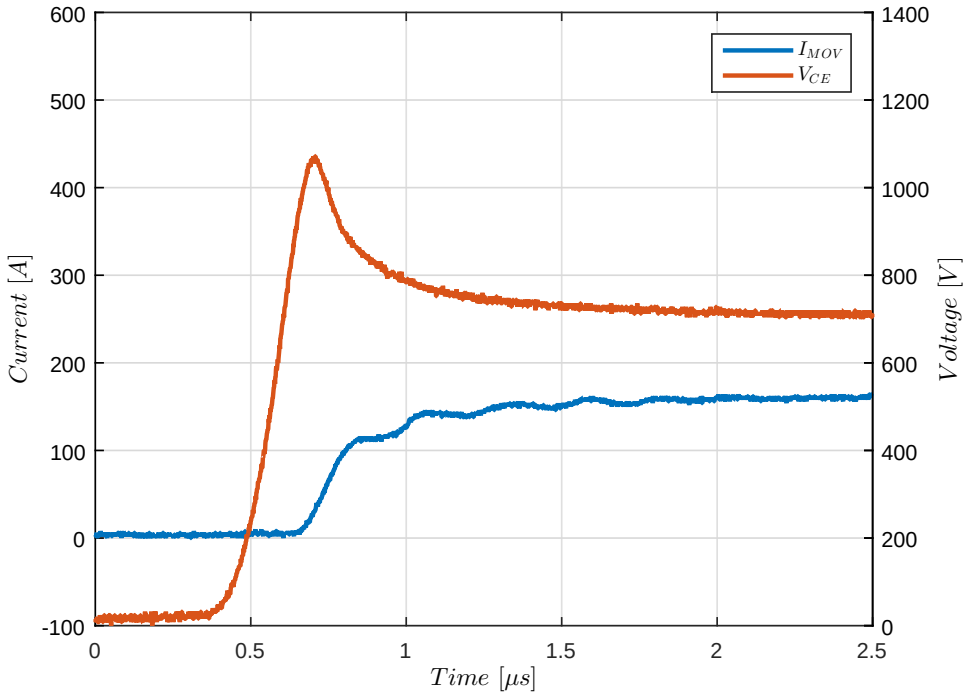


Figure 8.6: Transient overvoltage under IGBT switching with a stanard-D MOV as snubber, $V_{snubMOV}$ = 680 V DC, V_{DC} = 200 V, L_{line} = 1091.6 μH, V_{MOV} = 350 V and t_{pulse} = 1 ms

Table 8.14: Results from the test with variation of snubber circuit

Snubber Type	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
No snubber	217.7419	1288	122.8200	20.0644	0.4144
$V_{snubMOV}$ = 680 V	192.20	1072	109.88	19.3401	0.4176
C_{snub} = 100 nF	204.3011	1064	117.300	19.8381	0.4160
C_{snub} = 1 μF	188.17	832	121.800	19.7713	0.4120

The results in table 8.14 and figure 8.6 and figure 8.6 show that the use of a snubber, regardless of the type, is effective for suppression of unwanted transient overvoltages. It is observed that without a snubber peak $V_{CE} > V_{CEmax}$ = 1200 V. With all of the three snubbers tested the peak voltages satisfy $V_{CE} < V_{CEmax}$. It is observed that a higher capacitance decreases the peak voltage as the capacitor will receive a bigger part of the inrush current under the current commutation with increasing capacitance. Some current oscillations are observed in figure 8.7 which may be caused by interaction between the stray inductance, the snubber capacitor and parasitic capacitances. When comparing figures 8.6 and 8.7, it is observed that the capacitor provides a slower voltage rise. This results in a delayed inrush current to the energy MOV compared to the MOV snubber, and may be explained by the resistive properties of the snubber MOV. The MOV snubber thus suppresses the overvoltage by its non-linear resistive properties. This also means that the snubber MOV dissipates a certain amount of the total energy. The energy is stored in the capacitor snubber is expected to discharge when the IGBT A+ is switched on or dissipated

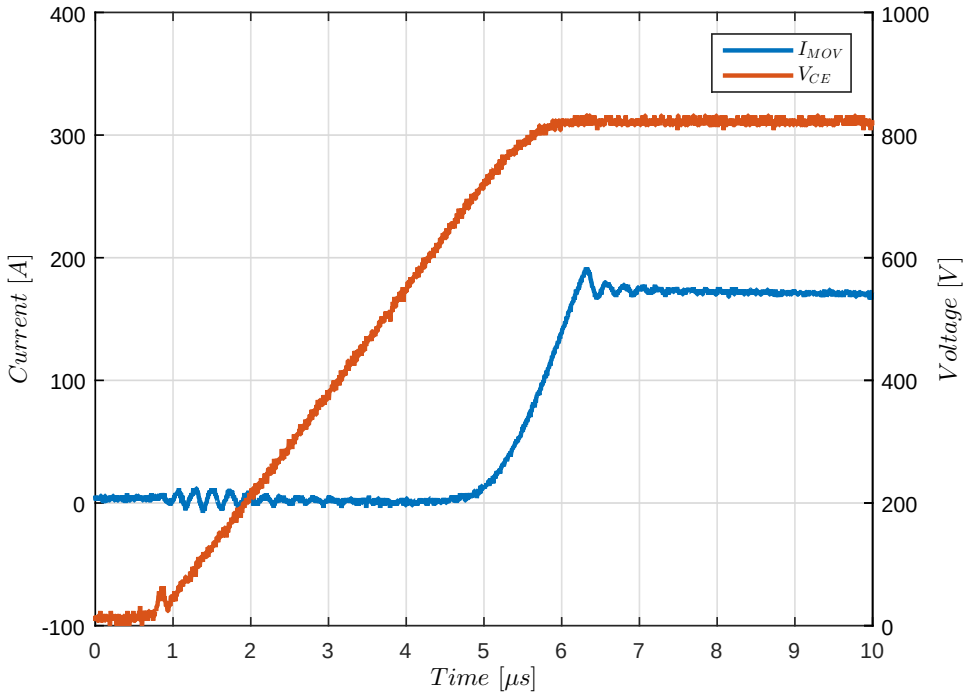


Figure 8.7: Transient overvoltage under IGBT switching with a capacitor snubber C_{snub} = 100 μF, V_{DC} = 200 V, L_{line} = 1091.6 μH, V_{MOV} = 350 V and t_{pulse} = 1 ms

in the energy MOV due to leakage currents. The energy stored in the capacitor is obtained by equation 5.2. The consequence of storing energy in a capacitor instead of dissipating energy in an MOV snubber is that the capacitor provides a slowly decreasing V_{CE} until the IGBT A+ is set to on-state again or until the energy MOV has dissipated the stored energy.

8.3 Contactor Switch Test

The experiment is described in section 6.3. The result from switching $I_{switch} = 1\ A$ is shown in figure 8.8, and from switching $I_{switch} = 0.15\ A$ is shown in figure 8.9. When comparing the figures, the time for the current to reach zero from its initial value differs significantly. An 1 A current uses approximately around 2 ms to reach zero, while a 0.15 A current uses around 100 μs. For both cases, high frequency voltage and current spikes occurs which indicates an arc is established. The voltage oscillations is approximately 500 V of magnitude which is higher than the the source voltage of 300 V. For the 1 A current switching, seen in figure 8.8, the current is steady decreasing before reaching zero and the extinction of the arc. At this point, the voltage again increases to double the source voltage 600 V. In the figure 8.9 around 450 μs, similar overvoltage is observed simultaneously as the high frequency spikes. Apparently, also residual currents occurs. This is regarded as noise as the current clamp meter may react to the magnetic field of the electromagnet inside the contactor switch.

In appendix B a switching including the voltages of the main and auxiliary contact is shown.

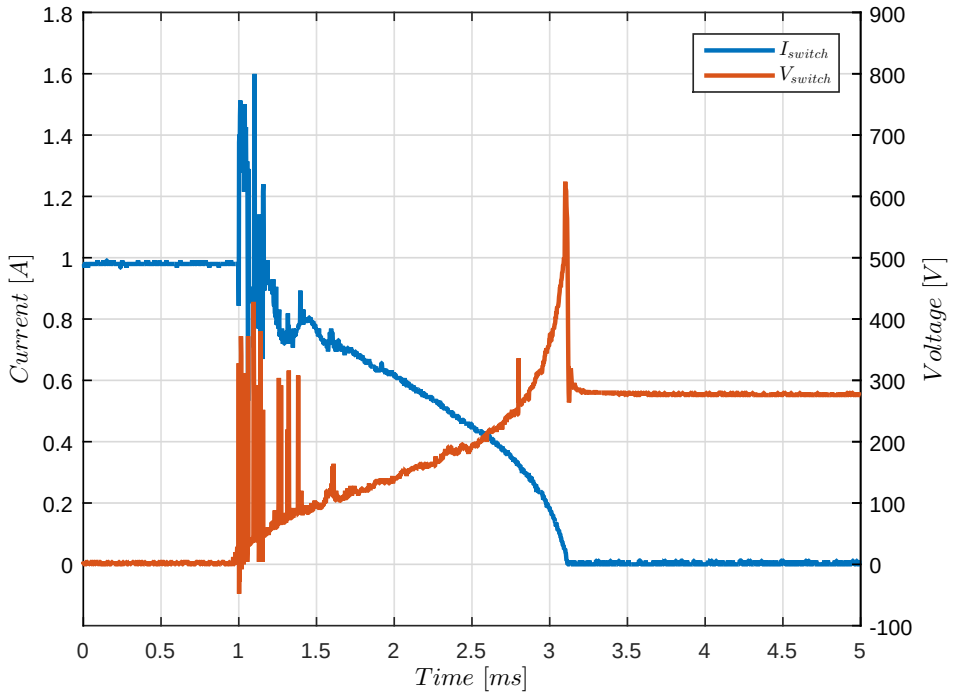


Figure 8.8: Contactor switch operates with 1 A

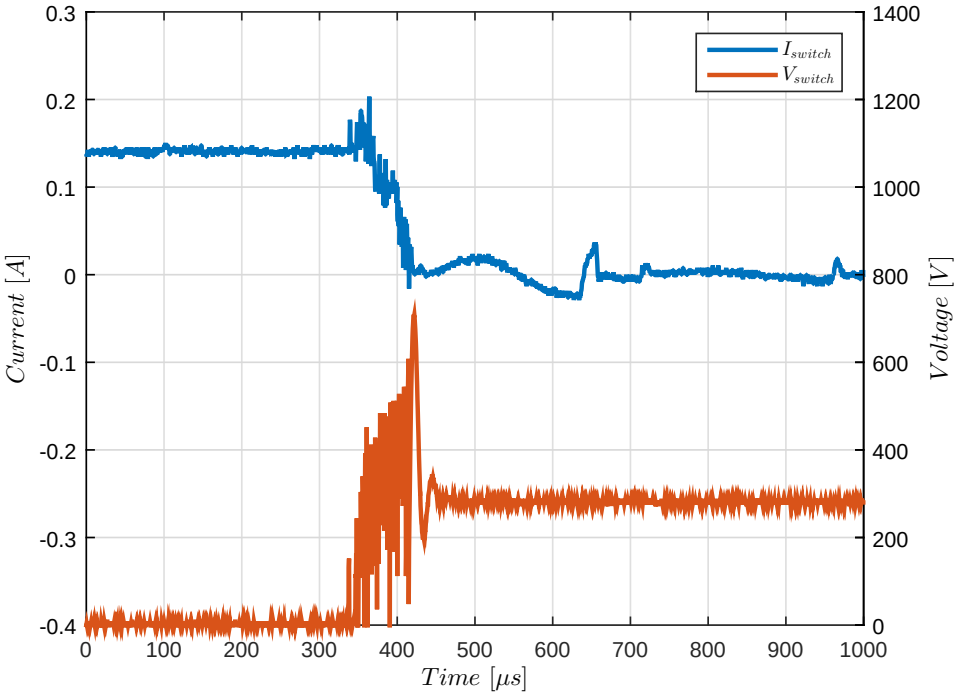


Figure 8.9: Contactor switch operates with 0.15 A

Table 8.15: Time delays for contactor switch

I_{switch} [A]	t_{zero} [ms]	t_{aux}[ms]
1	5.22	4.09
0.15	0.99	4.07

The time intervals for the signals are listed in table 8.15 where t_{zero} is the time interval from V_{coil} is set to 0 V to I_{switch} = 0 V, and t_{aux} is the time interval from V_{coil} is set to 0 V to V_{aux} is open circuited. As mentioned previously, it is clear that the switching of 1 A is more time consuming as 0.15 A current which is reflected in the difference in t_{zero}. Unlike for 0.15 A interruption, when switching 1 A current, the auxiliary contact provides a signal before the current has reached zero. The time interval t_{aux} is assumed the same for both cases as they vary insignificantly.

8.4 Comparison with the Preliminary Simulation Results

Figure 8.10 shows the PSCAD preliminary simulation result from the cosponsoring experiment, the initial experiment described in section 8.2.1, and should therefore be compared to figure 8.1.

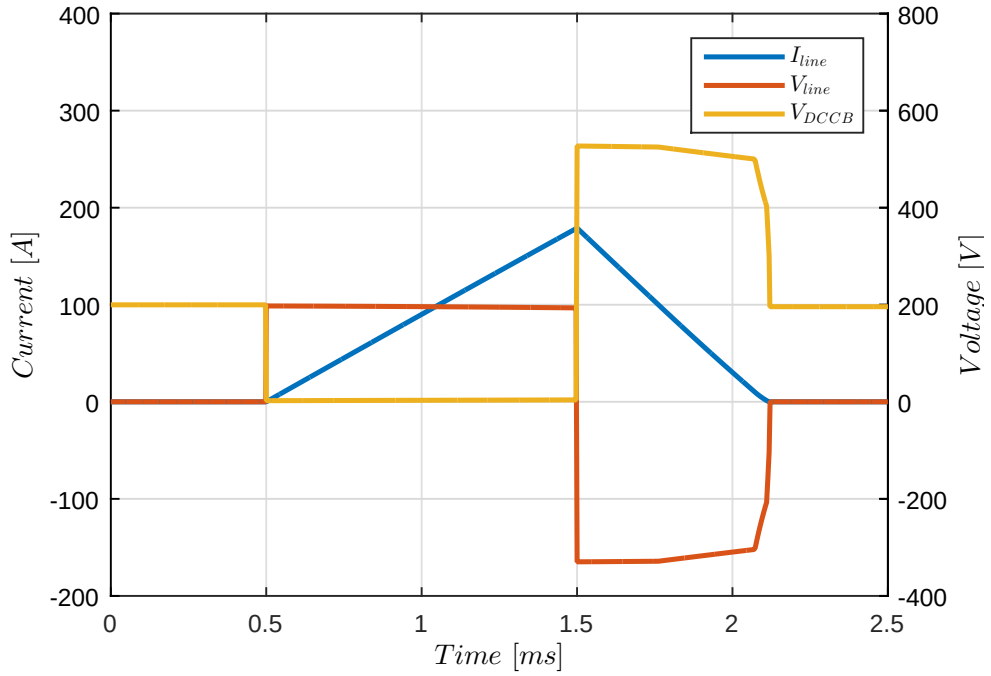


Figure 8.10: Preliminary simulation in PSCAD with V_{DC} = 200 V, L_{line} = 1091.6 μH, V_{MOV} = 350 V and t_{pulse} = 1 ms

The principle of operation in the simulation corresponds to the experimental results: A rising short circuit current with a constant slope due to V_{line}, and the current is forced to zero by the

counter voltage induced by the energy MOV after the IGBT A+ has switched off. The values of interest from the simulation and with the corresponding experiment are listed in table 8.16.

Table 8.16: Comparison of experimental work with the preliminary simulation results

	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
Experiment	217.7419	1288	122.8200	20.0644	0.4144
PSCAD simulation	179.0437	526.1323	94.3854	28.0125	0.6200

8.4.1 Deviations in the Results

When discussing the deviations in the PSCAD simulation and the experimental results, two main aspects is considered: The lack of details in the simulation model and the source of errors due to the measurement technique.

The objective is to build a simplified simulation model and therefore the values with regard to DC breaker design discussed in section 8.1 should comply with the experimental work and not the details in the particular wave form. So far, the stray inductance is not included in the PSCAD simulation model, and peak V_{CE} is significantly higher in the experiment. A higher voltage than in V-I characteristic of the diode and IGBT may also contribute to the higher V_{CE}.

Longer break t_{break} and higher energy dissipation W_{MOV} are also observed in the PSCAD simulation. This may be due to a lower counter voltage provided by the energy MOV and its VI characteristic in the PSCAD model. Some of the energy may also be dissipated in the line in the experiments since the inductor and the wires have a certain resistance. The peak I_{line} is lower in the simulation and may be due to the omission of oscillatory response during the line current commutation from the IGBT to the energy MOV in PSCAD. In the experimental results, these oscillations are observed in figure 8.2.

The measurement techniques may implicate a certain degree of inaccuracy to the results. The oscilloscope, TEKTRONIX TDS 2014, may contribute to calibration errors as well as the instrument has different sample rates. Transient voltage and current peaks may be omitted when using a higher time resolution. Regarding the current transducer LEM module, the current is measured via the output voltage and a linear ratio determined by a measuring resistor. This module has a certain linearity error. Some of the results are measured with an current clamp meter unable to catch the fast changes in I_{MOV} under the commutation from the IGBT to the energy MOV. Therefore, the slow reacting transducer is replaced by a rogowski coil in some of the results. These improved results are used for comparison with the simulation results.

The environment temperature in the laboratory may vary and give rise to some minor errors as some of the components used have a temperature dependency of their performance e.g. diode, IGBT and MOV.

The wires used in the experiments also have an resistive property, and provide both damping and losses to the results which is not found in the preliminary simulation.

8.5 PSCAD Simulation Model Adjustment

8.5.1 Adjustments in PSCAD

The simulation model in PSCAD is adjusted to obtain a more realistic model. The objective is to obtain a similar operational behaviour of the DC breaker and values within a 10 % deviation to the experimental work. The updated model has the following adjustments:

- Stray inductance of $L_\sigma = 0.55$ μH implemented.
- Apply a smaller solution time step $t_{step} = 0.4$ μs to obtain the effect of the stray inductance.
- VI-characteristic of the energy MOV is adjusted according to the experimental work which means adding more data points to the characteristic and apply a worst case 10 % tolerance band.
- VI-characteristic of the diodes and IGBTs is adjusted according to the experimental result.
- An auxiliary line resistor R_{line} =100 mΩ is implemented for adjusting the energy dissipation and break time t_{break}.
- An auxiliary capacitor C_{aux} =0.5 nF is implemented in order to adjust the voltage spikes in PSCAD due to stray inductance and take the capacitive property of the energy MOV into account.

The implementation of L_σ and the auxiliary capacitor is shown in figure 8.11.

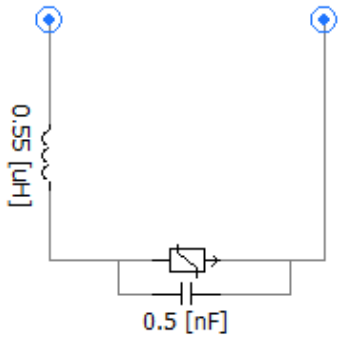


Figure 8.11: The adjusted energy MOV branch in PSCAD with stray inductance and an auxiliary capacitor

8.5.2 Results

The results from the adjusted simulation are presented in table 8.17 and in figure 8.12. It observed from the results that the obtained values, but peak line current I_{line}, in the adjusted PSCAD model deviate under 10%. As seen in figure 8.2, there are some oscillations during the current commutation from the IGBT to the energy MOV which are not captured by the simulation. In the experiment, immediately before the commutation, I_{line} = 173 A seen in figure 8.2.

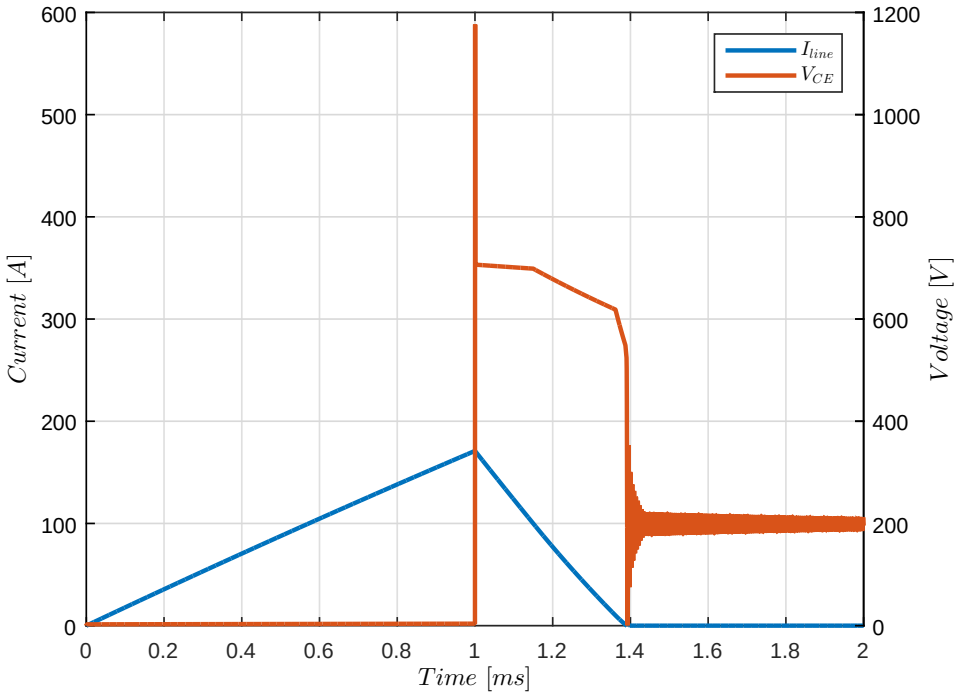


Figure 8.12: Simulation of the adjusted PSCAD model with V_{DC} = 200 V, L_{line} = 1091.6 μH, R_{line} = 100 mΩ, V_{MOV} = 350 V, t_{pulse} = 1 ms and L_{σ} = 0.55μH

I.e. is the peak line current due to the current slope provided by L_{line}. The additional contribution form the oscillation is ΔI_{line} = 44.5 A. The effect of the stray inductance is visible as a voltage spike in figure 8.12. Obtaining a more realistic damped oscillatory wave form requires

Table 8.17: Comparison of experimental work with the adjusted simulation results

	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
Experiment	217.7419	1288	122.8200	20.0644	0.4144
PSCAD simulation	170.98	1176.32	120.79	21.957	0.3900

a smaller solution t_{step} and a more detailed model. An attempt of obtaining the oscillatory responses in PSCAD for a DC breaker has been made in [50]. Some oscillations are observed after short circuit clearance in figure 8.12. These are not found the corresponding experiment, and this may due to the interaction between L_{line} the auxiliary capacitor and R_{line}.

The PSCAD simulations of the test model is assumed adequate for further design process as the operation principles are obtained and the values of importance discussed in section 8.1 deviates under a 10% limit.

Chapter 9

Development of the DC Breaker Design

This chapter aims as selecting the components for the design of the DC breaker in the NTNU/SINTEF lab and determine the corresponding ratings.

9.1 Corner Cases

The DC breaker for the NTNU/SINTEF laboratory may have to interrupt currents under several different circumstances. Therefore the following corner cases are considered for the interpretation of the results provided in chapter 8, facilitating the selection of components and determination of parameters ratings for the final DC breaker design.

1. Active region current interruption. The IGBT is operating in its active region under current interruption.
2. Instant high short circuit current interruption. Short circuits near the capacitor bank/DC link with little or zero inductance.
3. Current interruption with maximum magnetic energy. Short circuits with high inductance.
4. Auto-reclosing of the DC breaker to a permanent fault. The DC breaker is demanded to interrupt 2 short circuits within a small time interval.
5. Repetitive load switching. The DC breaker is used for sectioning loads in the DC grid.
6. DC grid black start. DC breaker used for charging DC capacitor bank on the opposite side.

Case 1 represents a corner case in which the IGBT operates in the active region described in section 4.1.2. This operating state may lead to additional power loss and subsequently undesirable heating of the IGBT. The gate driver used in the test model has implemented a protection ability which trips under excessive voltage drops over the IGBT. This case is not treated in further development of the DC breaker, since protection is already implemented in the gate driver

Case 2 represents a corner case where the current will rise rapidly due to low inductance, typically for short circuits near the converter. A certain response time between the detection of the short circuit and the trip of the DC breaker can be expected from the protection system.

The rapid rise in current continues during the response time interval, and there will be a certain risk of the current breaking capability of the DC breaker being exceeded. Accordingly the response time, the current breaking capability and minimum short circuit inductance should be considered in the DC breaker design.

In case 3 the energy in the system, described in section 3.3, may exceed the energy MOVs rated maximum energy dissipation W_{MOVmax} due to the magnitude of line inductance L_{line}. Therefore W_{MOVmax} in relation to the maximum line inductance should be considered. Case 4 stresses the ability of the DC breaker of interrupting at least two repeating short circuits promptly. The case is actual if the protection system is designed with an ability for auto-reclosing lines.

Case 5 refers to a situation in which the DC breaker switches load currents in order to section various parts of the DC grid. Therefore, the DC breaker ability to interrupt currents around 1 pu repetitively should be considered.

In case 6, the DC breaker is used for charging the capacitor bank of the VSC on the opposite side of the DC line. The case may be relevant in a black start situation where the capacitor bank inrush current during the charging may exceed the current breaking ability. Some charging series resistance in the DC line may limit this effect.

This chapter consider cases 2 and 3 in more detail as they concern the main function of a circuit break; to interrupt fault currents. A brief discussion is also given on the repetitive current interruption related to case 4 and 5.

9.2 Discussion of the Results for the Final DC Breaker Design

This section discusses the results in the previous chapter in relation to the design of a DC breaker and the limitations on the components.

9.2.1 The IGBT in Relation with the energy MOV

The energy MOV protects the IGBT from a harmful transient interruption voltage (TIV) during the current interruption as the line current is commentated into the energy MOV and providing a counter voltage. Assuming the DC breaker had consisted of IGBT modules only, the TIV may contribute to IGBT failure as the TIV would be very high as described in section 3.1.2. The experimental results indicate that a counter voltage must be higher than the source voltage with the combination of an inductance. This accounts for all current magnitudes intended to be forced to zero. Both sufficient line inductance and the counter voltage must therefore be ensured when determining an energy MOV for the DC breaker. Section 8.2.5 describes how an increase in the voltage rating of the energy MOV reduces the break time t_{break} and the energy dissipated per short circuit clearance. A high voltage rating is beneficial for a rapid short circuit clearance. However the voltage rating of the energy MOV should not be determined as high as possible in the DC breaker design. The V_{CE} also rises correspondingly with rising V_{MOV}, and V_{CEmax} may be exceeded. The line current I_{line} may also limit the rated MOV voltage. A higher interrupted current provides a higher energy MOV voltage and possible $V_{CE} > V_{CEmax}$. When the energy MOV operates in the protecting region, referred to in 4.2.2, the results shows only a marginal increase in the MOV voltage. V_{CEmax} may however be exceeded if the DC breaker interrupts currents corresponding to a situation in which the energy MOV operates in the linear region.

9.2.2 The Snubber Circuit

In order to examine the effect of a snubber type, the results in section 8.2.6 indicated that both a snubber MOV and a capacitor were effective suppressors of undesired voltage transients caused by stray inductance. The snubber MOV has the advantage of dissipating energy, as opposed to the capacitor which only stores energy. The applications of a DC breaker is not intended to switch in similar high frequencies as IGBTs in a VSC. The energy discharge is also assumed less critical. Due to leakage currents, the energy MOV in parallel may also dissipate some of the stored capacitor energy. The snubber may accordingly have a high capacitance and provide better protection capability which also was indicated in the results in table 8.14. However, it was also seen that a higher capacitance may increase the total time of short circuit clearance as the voltage rise is slower. The capacitor represents a more conventional solution than a snubber MOV for IGBT protection, and is thus the recommended solution for the final DC breaker design.

9.2.3 Thermal Considerations of the Energy MOV

Two main aspects observed in the results regarding the thermal considerations of the energy MOV: The energy dissipated per current interruption and the leakage currents.

Current Interruption

DC breaker current interruption is assumed related to both the single impulse handling capability and the thermal energy handling capability described in section 4.2.4. During current interruption a high incoming current to the MOV is observed initially and thereafter a decreasing continuous current which time duration may vary. As seen in figure 8.4, the temperature rise per current interruption is assumed insignificant since the MOV is not exceeding its critical temperature T_{MOV} = 85° C with repeating short circuit interruptions for certain time. The inductance intended to be used in DC grid in the NTNU/SINTEF lab may however be significantly higher than the inductor used in the experiments. The magnitude of inductance in relation to the number of energy MOVs related to maximum current should therefore be analysed. When considering repeating stitchings within small time intervals, it should also be ensured that the total energy dissipated is less than the rated maximum energy dissipation W_{MOVmax} and the average power within P_{MOVmax}. In section 8.2.5 the cooling time constant was calculated from experimental data to approximately 7 min. This indicates that the energy MOV needs a certain time to cool before a new high-energy interruption may occur.This is in order to avoid the risk overheat. The requirement could affect the ability of the DC breaker to conduct repetitive current interruptions.

Leakage Currents

Under normal operation of a DC grid the leakage current of the energy MOV is determined by the voltage drop over the parallel current conducting IGBTs and diodes. The voltage drop should be of such range that the leakage current is too small to generate power losses which could cause heating of the energy MOV to the critical temperature. For the DC breaker for the NTNU/SINTEF laboratory, the non-continuous operation of the DC grid will be prevent this effect. This is considered to be of greater relevance for DC breakers in an operating HVDC grid.

After the short circuit current has been forced to zero, residual currents may also provide heating. The energy MOV leakage current and high frequency current oscillations (occurring due to a low line inductance L_{line} seen in figure 8.3) both contribute to the residual currents. A contactor switch should accordingly operate, in order to provide isolation as soon as possible after the line current, excluding residual current, is forced to zero. The voltage over the DC breaker, and thereby the energy MOV, will approximately be the same as the voltage source seen in figure 8.1. At this point more leakage current will flow than under normal operating conditions described in the previous paragraphs. If the rated operating voltage of the energy MOV is less the than voltage of the source, excessive leakage current may flow and lead to heating and eventually failure if P_{MOVmax} is exceeded. The negative temperature coefficient may also imply a self-amplifying effect of the heating which stresses a recommendation for the contactor switch to operate as fast as possible.

The energy MOV may absorb some of the heat generated in the semiconductors. As such, the location of the energy MOV should ideally minimise the heat transferred into it from the IGBT modules.

9.2.4 Thermal Considerations of the IGBT/Diode modules

So far, thermal considerations of the IGBT and the diode have not been undertaken. The test model provides a limited ability to examine the thermal features of the semiconductors in a DC breaker. The thermal design elements of the DC breaker will accordingly be considered alongside the simulation and testing of the final design, before the DC breaker is assembled. The IGBT modules typically have a maximum junction temperature limitation refeered as T_{jmax} under steady state normal operation. The power loss transferred into heat may thus limit the maximum rated steady state current that could run through the DC breaker

Main Points from the Discussion

The main aspects discussed in this section can be summarised as:

- The counter voltage of the energy MOV must be higher than the source voltage.
- The counter voltage of the energy MOV must not exceed the rated collector-emitter voltage V_{CEmax}.
- The magnitude of the interruption current should be in the protecting region of the energy MOV.
- The IGBT should have a snubber circuit protecting for transient overvoltages due to stray inductances.
- The rated operating voltage of the energy MOV V_{MOV} should not exceed the source voltage.
- The contactor switch should isolate immediately after the line current is forced to zero.
- The contactor switch must interrupt the residual currents and withstand residual voltages after operating.

9.3 DC Breaker Ratings

Based upon what has been discussed so far in this chapter, the necessary ratings of the DC breaker include:

Rated current The DC breaker current under normal operation. I.e. the rated nominal current of the system.

Current breaking capability The maximum current the DC breaker is capable to interrupt.

Overload current The maximum continuous steady state DC breaker current.

Rated voltage The voltage of the system the DC breaker is designed for.

Maximum withstand capability The maximum voltage DC breaker can withstand after current interruption.

Voltage margin The minimum tolerated margin between the V_{CE} and V_{CEmax} and under current interruption.

Maximum operating temperature The maximum operating temperature of the semiconductor devices in the DC breaker.

Maximum and minimum line inductance

Repetitive current interruption capability

9.4 Selection of Components

The selection of components will first be established in a way that ensures the capability of the DC breaker to interrupt currents and minimises the risk of component failure. This is initially done by manual calculations followed by an analysis in section 9.5 including limitations and ratings of the design, partially based on PSCAD simulations

9.4.1 Selction of IGBT Modules

The test model seen in figure 6.5 and 6.4 consists of only one DC breaker cell. More cells in series may represent an alternative if a higher counter voltage is needed in order to reduce the break time and limit the energy dissipation of the energy MOV. The drawback of having a number of M breaker cells in series is that the conduction losses will be as M times as higher. This would also require more space, be more costly and require more with regard to the thermal considerations. An alternative is to use high voltage IGBTs (HVIGBT). More breaking cells or HVIGBTs generate more conduction losses and hence increase the need for a more complicated auxiliary cooling system. Active cooling for the DC breaker design, especially using other cooling media than air, may complicate the design and the control system of the breaker. Moreover the HVIGBTs are assumed to have a higher cost. Table 9.1 shows an example of a the losses of different configurations with 1 pu (100 A) of the 60 kVA lab VSC. The resistive loss approach in section 4.1.2 and

Table 9.1: Comparison of IGBT modules for the DC breaker design [53, 54]

IGBT type	**Cells**	V_{CEmax} **[V]**	**DC Breaker** P_{loss} [W]
Mitsubishi HVIGBT	1	3300	430.0
Mitsubishi HVIGBT	2	3300	860.0
Infineon IGBT	1	1700	211.93
Infineon IGBT	2	1700	423.86

the data sheets is used to estimate the loss the total DC breaker loss P_{loss}. Appendix C presents the details regarding the calculations. The conduction losses of both HVIGBT and of a 2 cell Infineon 1700 V DC breakers are assumed too high for the DC breaker intended for the DC grid in NTNU/SINTEF lab. A one-cell DC breaker design with Infineon 1700 V IGBT is therefore recommended. Whilst this would extend the breaking time, it would also minimise the space required, the conduction losses, the cost and the need for a complicated cooling system. For the recommended module, the rated maximum collector current is I_{Crm} = 1200 A=12 pu for a 1 ms current pulse.

9.4.2 Selection of Heat Sink

The thermal resistance is related to the power loss of semiconductors and is described in section 5.2.1. An electro thermal circuit may be useful in order to estimate the temperatures of the junction of the semiconductor and facilitate the selection of a heat sink and a cooling system. For the DC breaker a simple solution with an air-cooled heat sink is recommended. For the recommended IGBT module, the rated maximum junction temperature is T_{jmax} = 150 °C. Using equation 5.8, assuming a T_a = 25 °C and 1 pu continuous current, $R_{\theta ja}$ = 0.60 K/W along the heat conduction path is calculated. The data sheet provides the equivalent thermal resistance of 0.091 K/W for the diode and 0.056 K/W the IGBT. A standard extruded aluminium heat sink type SK 425 with $R_{\theta heatsink}$ = 0.2 K/W is the recommended heat sink [55]. This heat sink has one of the lowest $R_{\theta heatsink}$ in the catalogue and ensures that junction temperature T_{jmax} = 150 °C will not be exceeded with 1 pu continuous current.

9.4.3 Selction of Energy MOV

The energy MOV should have a rated operating voltage V_{MOV} higher than the source voltage. During current interruption, the counter voltage provided by the energy MOV must not exceed V_{CEmax}. The corresponding current to V_{CEmax} may accordingly limit the current breaking capability. A voltage margin V_{margin} may be included in order to ensure that V_{CEmax} is never exceeded. The 10 % tolerance of the VI-characteristic must also be taken into account in these calculations. The energy MOV recommended is a high energy MOV type B60K460 with the following ratings: V_{MOV} = 615 V, V_V = 750 V and clamping voltage $V_c(I_c)$ = 1250 V and I_c = 500. Assuming a capacitor snubber mitigates the effect of the stray inductance and using the data sheet, the selected varistor provides a voltage margin V_{margin} = 450 V when the DC breaker interrupts a 5 p.u or 500 A current. Given V_{margin} = 0 V by using equation 4.5, the maximum current capability is determined to approximately 5925 A. This current magnitude exceeds the

repetitive peak current I_{Crm}. The calculation indicates that I_{Crm} is the limiting factor for the rated current breaking capability. The calculation is attached in appendix C.

As mentioned, the rated MOV voltage V_{MOV} should be lower than the rated voltage of the converter V_{DC}. This is not the case with the selected energy MOV, meaning that after the current interruption, the MOV will conduct a certain leakage current i.e $I_{MOV}(750\ V)$ =1 mA. The contractor switch must interrupt this current and ensure $P_{MOV} < P_{MOVmax}$. At rated converter voltage 700 V the expected MOV power P_{MOV} =0.71 W which is lower than rated P_{MOVmax}. This calculation assumes that the energy MOV maintains a normal temperature. If the temperature of the energy MOV exceeds $T_{critical}$ = 85 °C, more leakage current is expected. The contactor switch should therefore operated as fast as possible.

Using two energy MOVs in parallel with the IGBT modules of the type mentioned is the recommended solution for handling higher energy dissipation due to the line inductance L_{line}. An analysis of maximum current breaking capability in relation to the line inductance will be carried out in a following section.

9.4.4 Selection of Contactor Switch

As stated in previous section, the expected leakage current is around 1 mA, and as seen in section 8.2.2, the current oscillation may be insignificant due to damping before the switch operates. A contactor switch also has a certain time-delay investigated in section 8.3 The selected contactor switch is the same as previously tested (section 8.3); KILOVAC EV200. The contactor is designed for DC applications, and the results showed that it was able to isolate and break the expected residual current despite highly a inductive load. The rated voltage of the contactor is 900 V, which is higher than the rated voltage of the DC grid. Accordingly, the switch should be able to both operate and isolate. According to the data-sheet, the recommended contactor also tolerates a current of 2000 A for 12 ms not risking contact welding and failure [47].

Selected Components

Based on the discussion and investigations undertaken, the recommendations for the design of the DC breaker in terms of components are summarised as follows:

IGBT module V_{CE} =1700 V FZ600R17KE3 IGBT/Didoe-module [54]

Heat sink SK425 extruded aluminium [55]

Energy MOV V_{MOV} = 615 V DC B60K460 EPCOS HighE series block varistor [56]

Contacor switch KILOVAC EV200 [47]

9.5 PSCAD Simulations and Determination of Ratings

PSCAD simulation of the DC breaker will be used to calculate the ratings of the DC breaker listed in section 9.3. The details regarding the outline of the PSCAD simulation model is described in chapter 7. The PSCAD model is also adjusted using conservative component parameters in the simulations in order to ensure the results obtained. In the adjusted simulations,

described in section 8.5.1, the VI-characteristic is observed more conservative than using the VI-characteristic of T_j = 25 °C. The IGBT and diode VI-characteristic for operation at T_j = 125° C is implemented. The MOV VI-characteristic is implemented with a 10% tolerance band from the data sheet (I.e. maximum voltage is assumed for a given current). The temperature of the energy MOV is assumed $T_{MOV} < T_{critical}$ = 85°C such that no de-rating applies. A source voltage V_{DC} = 700 V or 1 pu, is assumed for all simulations, and stray inductance is omitted as a capacitor snubber is assumed with C_{snub} = 0.1 μF. The removal of stray inductance also provides efficient simulation time since the time t_{step} may be increased accordingly.

9.5.1 Principle of Operation

Table 9.2: Parameters used in PSCAD for validation of the selected components

Parameter	**Values**
L_{line}	10 mH
$t_{response}$	0.1 ms
Pre fault I_{line}	1 pu
I_{trip}	3 pu
R_{line}	1 mΩ
C_{snub}	0.1 μF

The following case listed in table 9.2 is simulated in PSCAD order to validate the selection of components. Plots of the voltage of the switching IGBT is shown in appendix D. The values obtained is listed in table 9.3. The currents and voltages obtained form the simulation is shown in figure 9.1 and the temperature rise in the same time interval is shown i figure 9.2. With this simulation, the consequence of having only one breaker cell is seen as the break time t_{break} is 6.4 ms. The counter voltage is lower, and therefore also longer t_{break} provided and more energy is dissipated in the energy MOV. Regarding the the temperature rise, it is observed that the short circuit generated a temperature rise in the IGBT and the anti-parallel diode. The diode is rising faster and higher as the time constant is the lowest for the the corresponding heat conduction path. The heat sink temperature is not effected as the time constant $\tau_{heatsink}$ is higher.

Table 9.3: Values obtained in PSCAD with the selected components for the DC breaker

peak$T_{j\ diode}$	peak$T_{j\ IGBT}$	peak I_{line} [A]	peak V_{CE} [V]	peak P_{MOV} [kW]	W_{MOV} [J]	t_{break} [ms]
76.57	70.67	307.2	1210.97	371.13	1136.4	6.4

9.5.2 Current Breaking Capability

Consideration of Line Inductance

The repetitive peak current I_{Crm} which has been discussed as a limitation for the current breaking capability – represents the starting point for the determination of the maximum current capability. The next step is to evaluate the limitation of the line inductance L_{line} corresponding

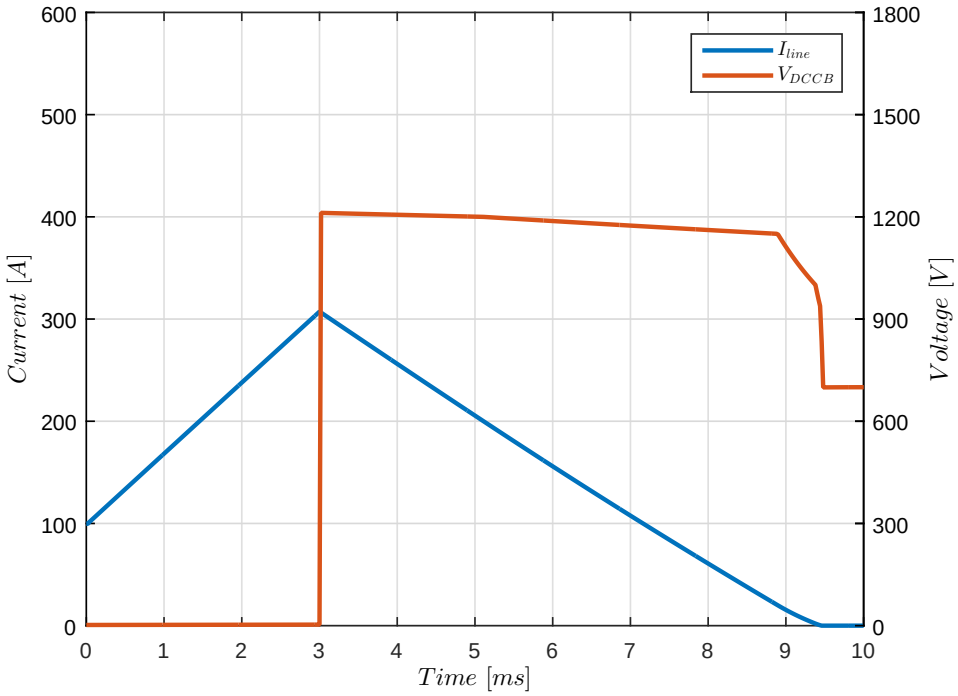


Figure 9.1: Simulation of short circuit current interruption with the selected components

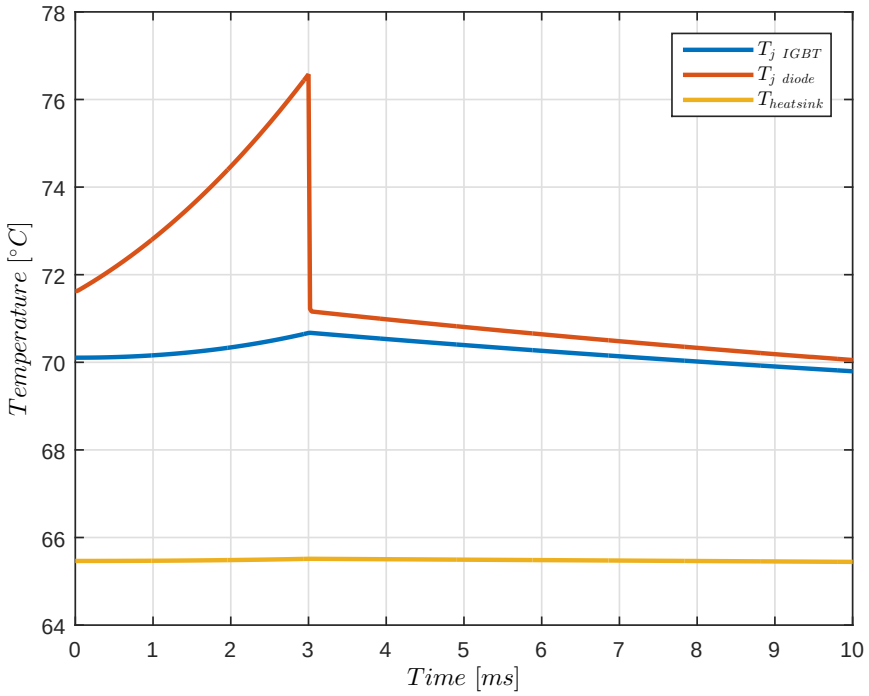


Figure 9.2: Temperature rise under short circuit current interruption

to the energy MOV W_{MOVmax} in terms of peak I_{line}. Equation 3.9 expresses theoretically the total energy the MOV needs to dissipate if no resistive elements in the DC line is assumed. For worst case consideration, the resistive element is also neglected in the following simulations. The selected energy MOV has rated W_{MOVmax} = 1650 J. Since the MOV may have some leakage current prior to DC breaker trips, such that W_{MOVmax} = 1600 J is assumed in further simulations. Two parallel energy MOVs results in W_{MOVmax} = 3200 J. The maximum current breaking capability I_{max} with 2 parallel energy MOVs as a function of the line inductance L_{line} obtained from PSCAD is shown in figure 9.3. Here, I_{Crm} is taken into account, while the voltage margin is analysed later point on. The figure also presents the detection level of the overcurrent protection I_{trip}, where the response time is assumed $t_{response}$ = 0.1 ms. Corresponding figures with other $t_{response}$ are attached in appendix E.

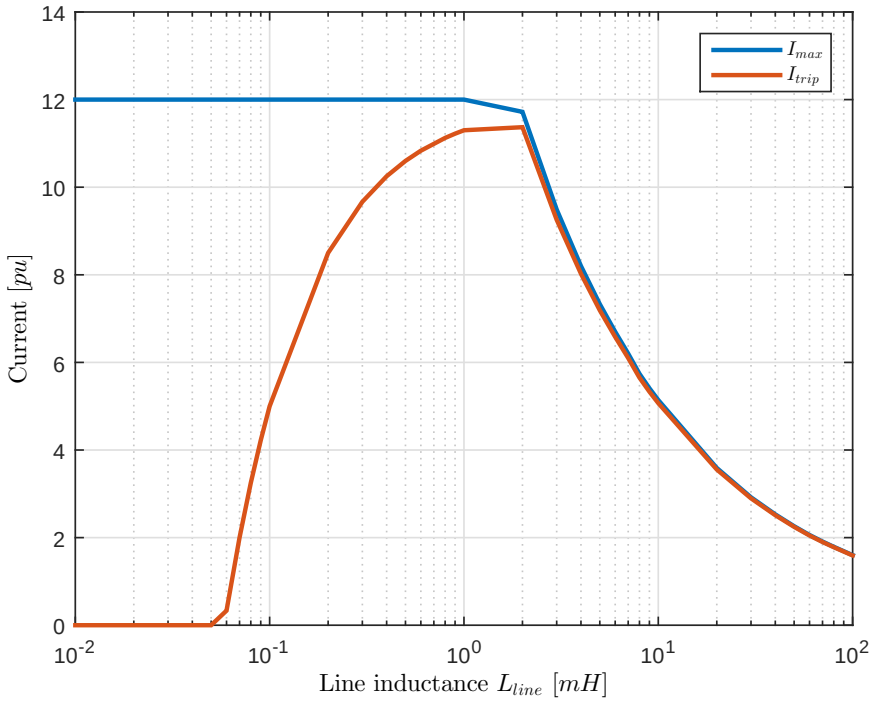


Figure 9.3: The current breaking capability I_{max} as a function line inductance L_{line}, I_{max} is the peak current interrupted and I_{trip} is the maximum detection level of the protection system, $t_{response}$ = 0.1 ms

It is observed that there are 2 areas of I_{max}. For L_{line} > 2 mH, the MOVs ability to dissipate energy W_{max} determines I_{max}. And for L_{line} <2 mH, I_{Crm} =12 pu determines I_{max}. If more MOVs were placed in parallel, the area in which $I_{max} = I_{Crm}$ is expected to shift to the right in the figure, as the DC breaker will be able to dissipate more of the energy. For $L_{line} > 2\ mH$, I_{max} decreases with an increasing L_{line}. As seen in the experiments with the test model, the voltage drop over the energy MOV or the DC breaker only changes marginally with respect to the current when operating in the protective region. By considering equation 3.9, I_{line} decreases with the square root of the current I_{max} as the V_{CB} only changes marginally. In the left area, where L_{line} < 2 mH, also a significant effect of $t_{response}$ is observed. The inductance determines the

slope of the short circuit current seen in 3.3. If the L_{line} is relatively small, and the the response time has a certain magnitude, the detection level and the peak current will differ significantly. In figure 9.3 at L_{line} < 0.05 mH, the current will rise so fast such that I_{Crm} is exceeded before the short circuit current is interrupted. This also illustrates the importance of determining minimum line inductance. Assuming $t_{response}$ =0.1 ms, the recommended minimum line inductance is 0.7 mH. Here the detection level must be set to 2 pu and the DC breaker will interrupt 12 pu.

Consideration of Energy MOV Voltage

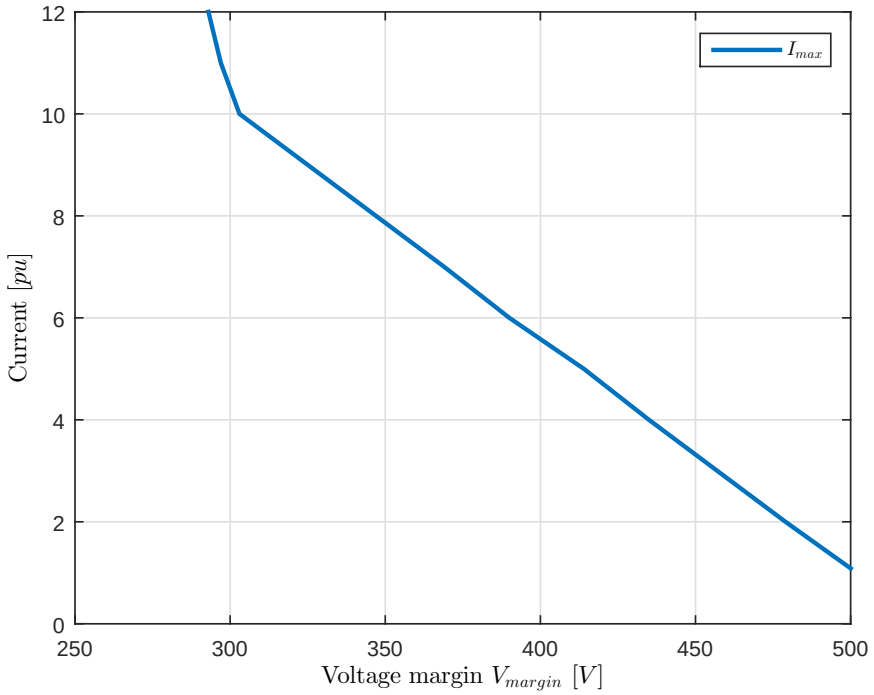


Figure 9.4: The current breaking capability I_{max} as a function of the desired voltage margin V_{margin}

Figure 9.4 shows the voltage margin V_{margin} obtained from simulations. For the selected MOV and IGBT, 250 < $V_{margin}(I_{Crm})$ < 300. The voltage margin only determines the current breaking capability if V_{margin} >300 V. A voltage margin V_{margin} = 250 V should be sufficient as the capacitor snubber worked effectively in the experiments described in section 8.2.6. As stated in section 9.4, interruption of a 5 pu current provides V_{margin} = 450 V. According to figure 9.4, the $V_{margin} \approx$ 425 V which is explained by the MOV VI-characteristic implemented in PSCAD may lack details. However, since it is already stated that the I_{Crm} will be the limiting factor if V_{margin} = 250 V, adjustments in PSCAD are not considered necessary. Since two dependencies are observed in figure 9.3 and L_{line} may be varied in the DC grid, two types of rated maximum current capability are determined according to figure 9.3. One value for high energy current interruption and another for lower energies/lower L_{line} is determined. The high energy type:

L_{line} = 20 mH and I_{max} = 3.5 pu. Low energy type: L_{line} = 1 mH and I_{max} = 12 pu.

9.5.3 Maximum Continuous Current

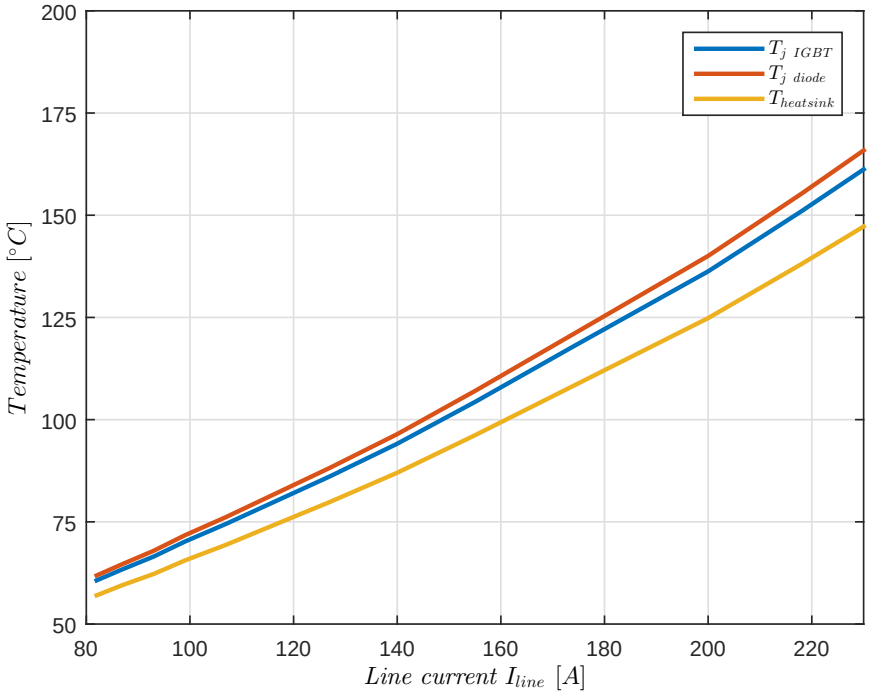


Figure 9.5: DC breaker temperatures as a function of the continuous line current I_{line}

The maximum continuous current is found by simulating a steady state case of the DC grid with continuous line current I_{line} and finding the corresponding I_{line} in which the $T_j = T_{jmax}$ = 150 °C. The electro thermal circuit described in section 7.5 is used. In figure 9.5 the temperature of the heat sink $T_{heatsink}$, diode junction T_{jdiode} and the IGBT junction T_{jIGBT} is shown. T_{jdiode} exceeds the maximum contentious temperature at I_{line} = 210 A. The recommended maximum continuous current is thus 2 pu with a safety margin of 10 A. However, a fan may decrease the thermal resistivity of the heat-sink and also contribute to avoid excessive heat transfer to the energy MOV. The fan may be started by a temperature relay placed on the heat sink surface. This will start air-cooling when needed if the $T_{heatsink}$ exceeds a certain level.

9.5.4 Maximum Voltage Withstand Capability

As seen in the results of from contactor test experiment, under and after current interruption residual transient voltages occurs. The contactor switch must be able to withstand this in order to prevent the arc from re-ignition. The rated withstand voltage of the selected contactor switch is V_w = 2200 V.

9.5.5 Repetitive Current Interruption Capability

As discussed in section 9.1 the DC breaker may be used to interrupt currents more than once within a given time frame. It is suggested that P_{MOVmax} and W_{MOVmax} for the energy MOV may be used to determine the repetitive current interruption capability. It is assumed that the DC breaker can interrupt currents as long as the average power of the energy MOV is kept within P_{MOVmax}, and the temperature is below the critical temperature T_{MOV} = 85 °C. For switching load currents, 1.5 pu current interruption with L_{line} = 10 mH is assumed. The values may be adjusted later. For the selected energy MOVs in the suggested parallel configuration, the ratings are: P_{MOVmax} = 3.2 W and W_{MOVmax} = 3200 J. The residual current contribution before the contactor switch opens should also be considered as it may contribute to the P_{MOV}. Simulation in PSCAD provides P_{MOV} = 1.5 W. The delay time of the of the contactor switch is measured to 4 ms in which the total energy dissipation is assumed insignificant. Simulation of the mentioned load current switching provides W_{MOV} = 282 J per switching. In theory, this means that the time duration between the switching should be $t = 282\ J/3.2\ W = 88.1$ s, almost 1.5 minute between each switching. Therefore the suggested solution to obtain the repetitive current interruption capability is to measure the temperature of the energy MOV under repetitive load currents and short circuits while ensuring $T_{MOV} < T_{critical}$ = 85 °C . Most likely, the surface temperature of the MOV is measured and must be taken into consideration.

Given that the main function of a DC breaker is to interrupt fault current, and taking into account the ratings related to the short circuit interruption have been obtained, the repetitive current interruption is of less importance.

9.5.6 Summary of DC Breaker Ratings

The following list summarizes the main results form this section.

Rated current 100 A

Current breaking capability Low inductive: 1200 A High inductive: 350 A

Overload current 200 A, expected to decrease with active cooling.

Rated voltage 700 V

Maximum Withstand Capability 2200 V

IGBT Voltage Magin 250 V

Maximum operating temperature 150°C

Maximum and Minimum Line Inductance Maximum:20 mH and minimum: 0.7 mH

Repetitive Current Interruption Capability Determined when DC breaker is tested.

Chapter 10

Implementation of the DC Breaker

This chapter describes the implementation of the DC breaker for the NTNU/SINTEF lab.

10.1 Configuration of the DC Breaker

Two similar DC breakers is implemented, one for the positive pole and one for the negative pole of the 60 kVA laboratory converter. The components used are the selected components in previous chapter. The final DC breaker configuration consist of the following:

Solid state DC breaker Two IGBT modules in anti-series, capacitor snubbers C_{snub} and a parallel MOV.

Isolator Switch Contactor switch referred to as IS for physical isolation

Bypass Switch Contactor switch referred to as BS to bypass the DC breaker when not in use.

Charging circuit Contacor switch referred to as CS and charging resistor R_c.

The circuit diagram is shown in figure 10.1. The DC breakers has a bi-directional current interruption possibility as the IGBT modules are placed in anti-seires. The configuration has included functionality for charging the adjacent DC capacitor bank, and the parallel charging resistor R_c = 22 kΩ will reduce the inrush current. In parallel with the solid state breaker, a bypass path is implemented in order to operate the DC grid in the NTNU/SINTEF lab without the DC breaker and also for emulating a hybrid DC breaker topology at a later point. The snubber circuit is added to each IGBT with C_{snub} = 0.1 μF. In appendix F, a detailed circuit diagram is illustrated with the control system. The control system is based on simple 24 V DC electro mechanical relays. This is expected to be developed further as the DC breaker is tested. E.g. A field programmable gate array (FPGA) is attached to the control system, but not currently in use.

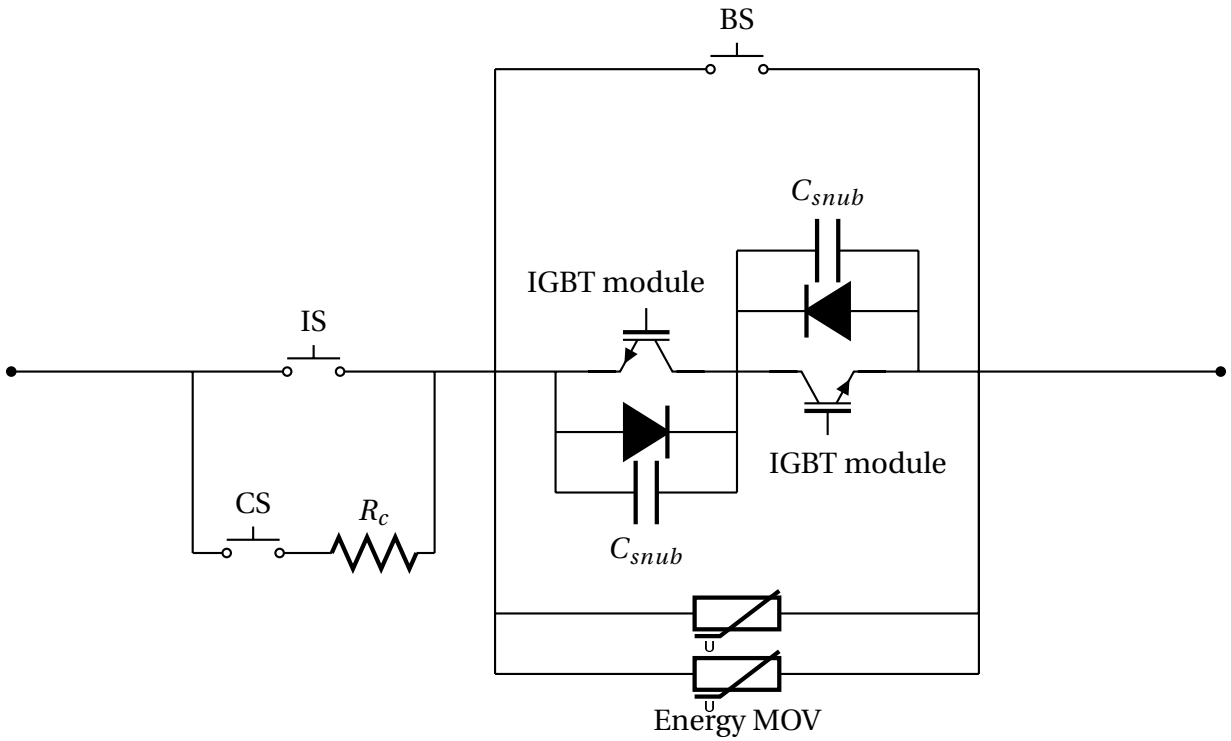


Figure 10.1: Configuration of the DC breaker in NTNU/SINTEF lab

10.2 Construction of DC breaker

The DC breaker is separated into three parts in the construction: One backside steel plate with the contactor switches attached, the middle with heat sink, the breaker cells, R_c and gate driver cards and the front side steel plate with the control system and auxiliary power supply. An overview of the parts is given in figures 10.2, 10.3 and 10.4

10.3 Function Test

Figures 10.5, 10.6 and 10.7 shows the oscilloscope picture of initial testing of the DC breaker. The set up is the same as in the test model described in chapter. $V_{DC} = 300$ and $L_{line} = L_3 1091.6\mu$ H as the 60 kVa converter is not currently available. Unfortunately, there was no time for further testing.

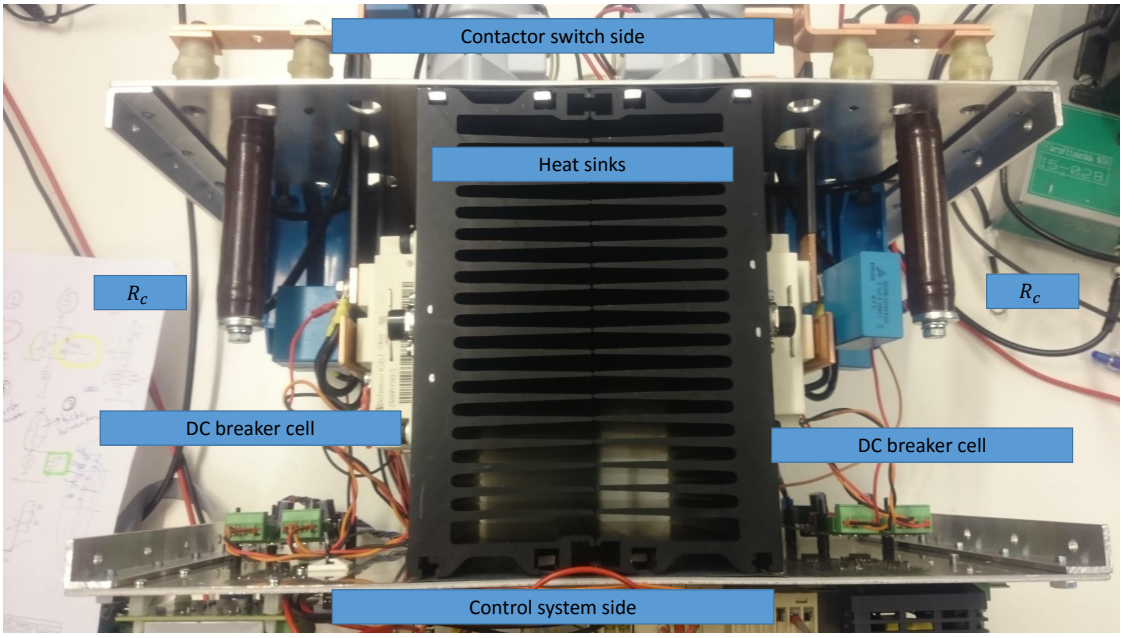


Figure 10.2: Overview of the DC breaker construction, two identical breaker cells on each side of the heat sink

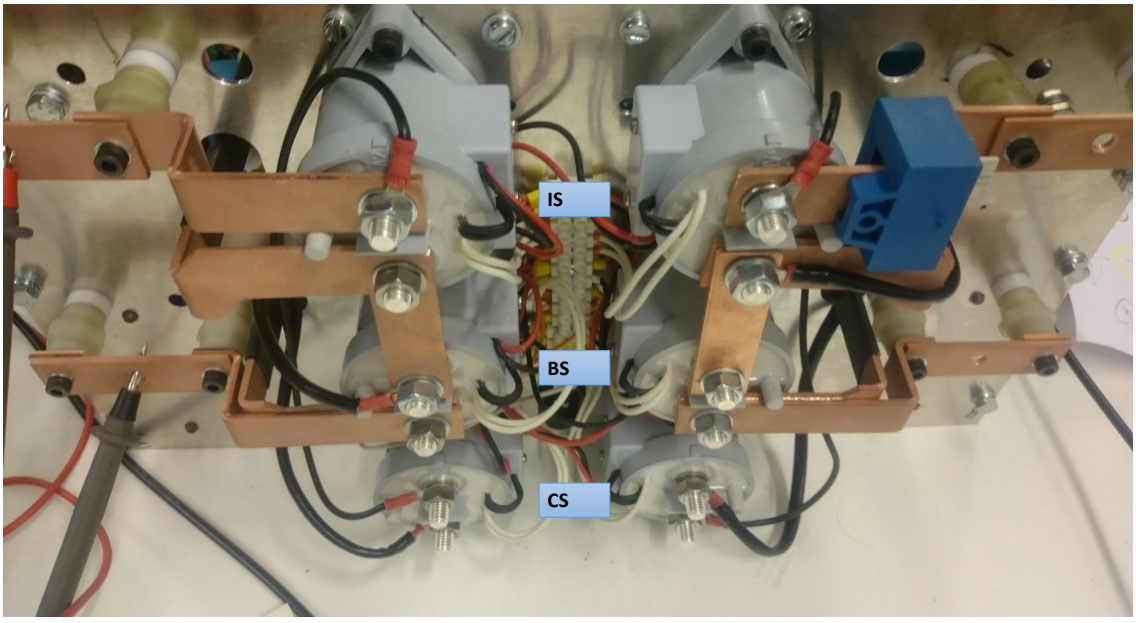


Figure 10.3: Back side of the DC breaker with the contator switches indicated as isolator switch (IS), bypass switch (BS) and charging switch (CS)

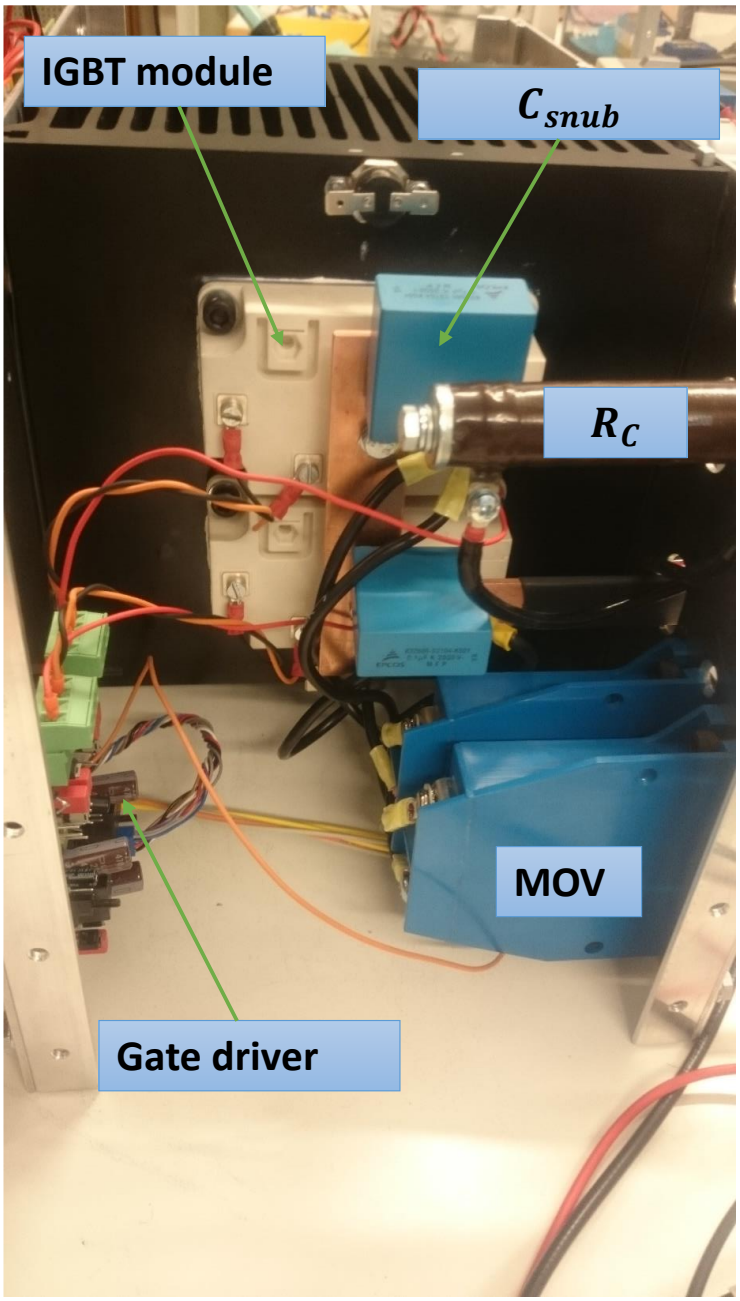


Figure 10.4: One side of the middle part of the DC breaker

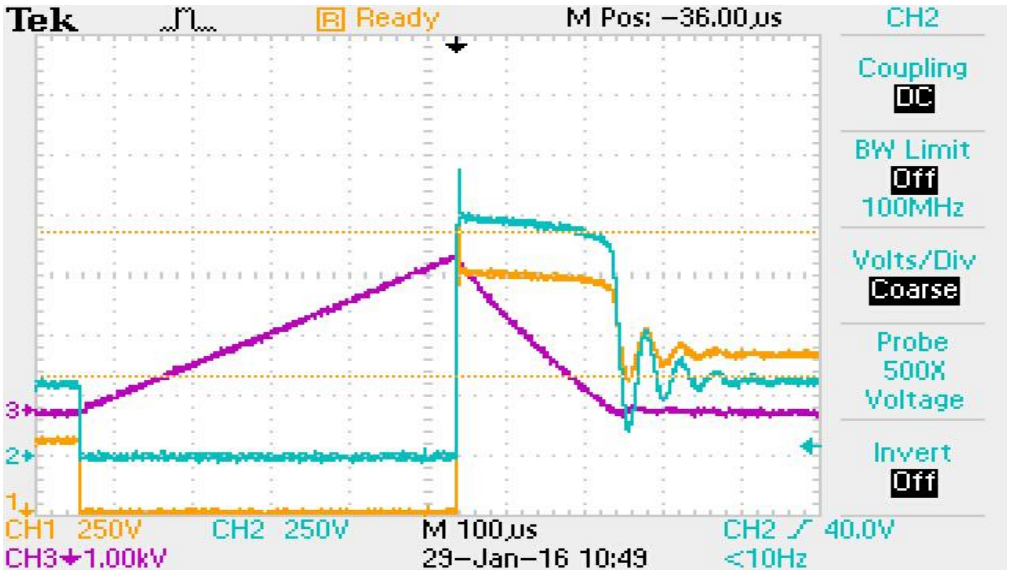


Figure 10.5: Current interruption in final breaker design, CH1 depicts the IGBT voltage, CH2 the breaker cell voltage and CH3 depicts the current measured as voltage from the LEM-module (ratio: 1/20)

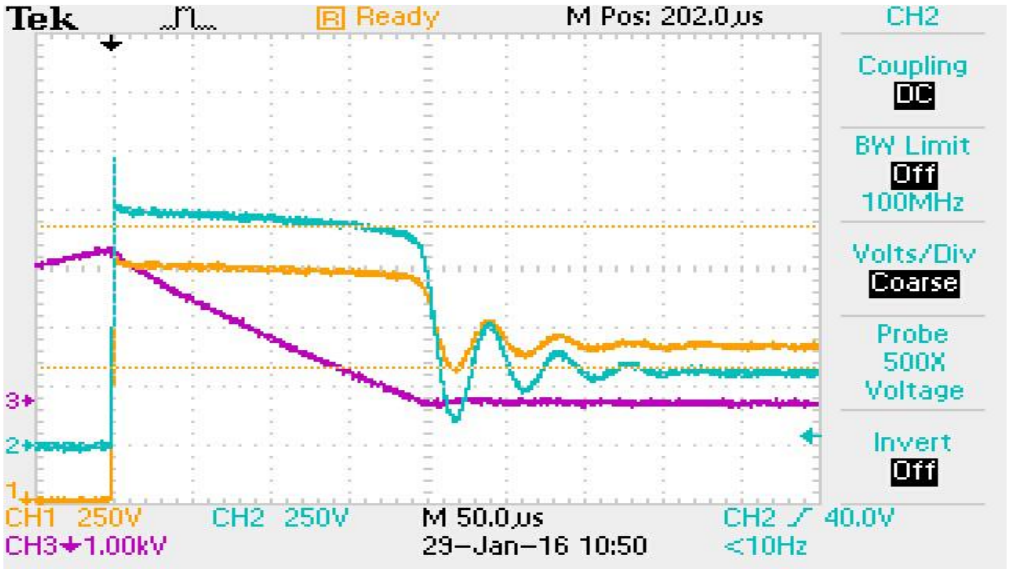


Figure 10.6: Current interruption in final breaker design, CH1 depicts the IGBT voltage, CH2 the breaker cell voltage and CH3 depicts the current measured as voltage from the LEM-module(ratio: 1/20)

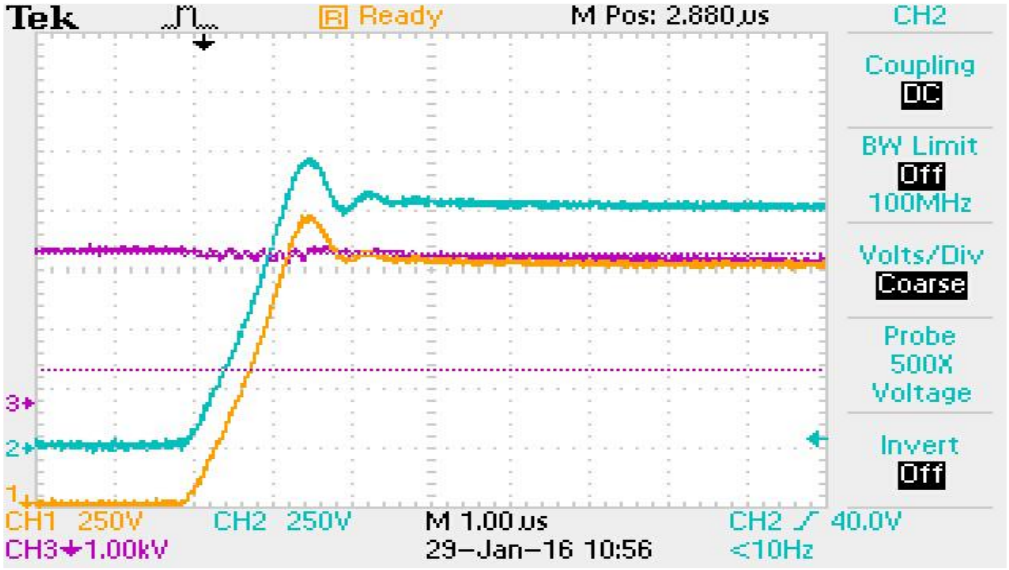


Figure 10.7: Transient overvoltage under current interruption in final breaker design, CH1 depicts the IGBT voltage, CH2 the breaker cell voltage and CH3 depicts the current measured as voltage from the LEM-module (ratio:1/20)

Chapter 11

Guidelines for DC Breaker Design

The purpose of this chapter is to provide design guidelines for HVDC breakers. The basis is the development of the solid state DC breaker in previous chapters and put the experiences in the context of a HVDC transmission system.

11.1 Circuit Breakers for HVDC Applications

The DC breaker for the NTNU/SINTEF lab is a solid state DC breaker. In the experimental work and simulations, one of the main advantages of the topology is observed. The type of DC breaker has the capability to interrupt currents fast e.g. the results provided a break time t_{break} under 1 ms in in chapter 8. The disadvantage of the topology is the on-state conduction losses as the semiconductors must be placed in the series with DC line. As mentioned, the counter voltage must be higher than the system voltage in order to force the current to zero. The semiconductor devices have a recommended voltage drop limit, V_{CEmax} for the IGBT, and must be able to tolerate a voltage magnitude equal or bigger than the counter voltage. For a higher system voltage of the DC grid, the higher amount of semiconductors is needed in series with the line and thus provide a significant amount of losses. Ratings from the CIGRE DC grid test system is used to illustrate the number of semiconductors needed [57]. The examples assumes a bi-directional current interruption application. If a solid state DC breaker shall provide a counter voltage of 1.3 pu of a 400 kV overhead line (OHL) in the DC grid, the requirement is at least 158 breaker cells consisting of two 3.3 kV Mitsubishi IGBT modules each in series with the DC line. As seen in section 9.4 for a 100 A current, the loss is P_{loss} = 430 W per breaker cell. For the actual IGBT the maximum rated continuous current is I_{Cmax} = 400 A. If the rated current of the OHL is 3.5 kA, a parallel IGBT configuration with at least 9 IGBTs is needed in order to tolerate a contentious rated current level. The total on-state losses of the solid state breaker is thus assumed to be unacceptable. Despite the losses, the solid state topology is a technically feasible solution for high voltage applications [2, 13]. As mentioned in section 2.5.3, the challenges related to the conduction losses of the solid state topology have been handled by introducing a nominal current path with mechanical switchgear in addition to a solid state breaker. This type is referred to as the hybrid HVDC breaker topology. The solid state breaker in a hybrid topology is referred to as the main breaker and seen in figure 2.7. This hybrid HVDC breaker concept has several different suggested topologies with different semiconductor devices such as IGBTs, MOSFETs and

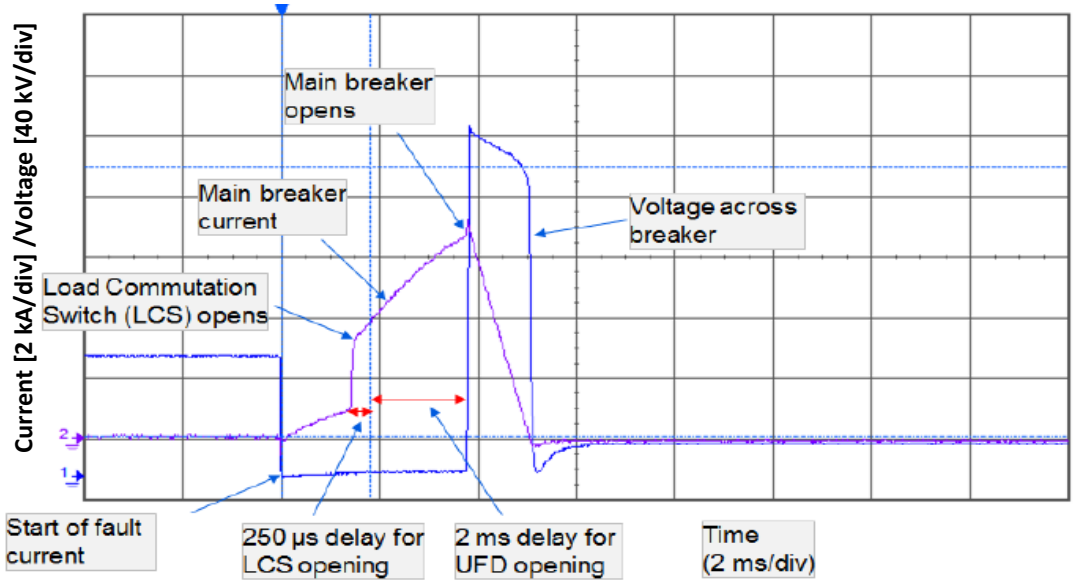


Figure 11.1: Current and voltage under current interruption of the ABB hybrid HVDC breaker topology [5]

thyristors. An overview of the topologies is given in [16]. Since the IGBT has been used in the DC breaker for the NTNU/SINTEF lab, an IGBT based topology will be used in further discussion of design guidelines. Nevertheless, the guidelines may be useful for other types of semiconductors suggested for HVDC breakers, as there are similarities between the different types of semiconductors.

The nominal current path of a hybrid consist of significant fewer number of IGBTs, than the main breaker, and a low resistive UFD which keeps the conduction losses at a acceptable level. The LCS consists of fewer numbers of IGBTs sufficient to commutate the current into the main breaker under current interruption. It is the main breaker of the hybrid HVDC breaker, which actually forces the current to zero with the similar operation as the breaker developed for the NTNU/SINTEF lab. Thus may the experiences from the development of the DC breaker in previous chapters also be used for the design of the main breaker of the hybrid topology. The UFD is one of the key components in the hybrid topology. According to ABB, the switch is able to establish a dielectric insulation in 2 ms or less [58]. After switching, the UFD must withstand the counter voltage provided by the energy MOV in the solid state breaker protecting the LCS from failure. The counter voltage, which is provided by the main breaker, may exceed the tolerated voltage level of LCS reflected in V_{CEmax} for a single IGBT. Figure 11.1 shows an example of a current interruption of the hybrid HVDC breaker shown in figure 2.7 for illustrating the latest discussion.

11.2 HVDC Breaker Design

11.2.1 Location

The desgin outline of the HVDC breaker may be determined of the location of the HVDC breaker. If the HVDC breaker is located offshore, the required space for the DC breaker is assumed more critical compared to if the DC breaker is placed onshore in HVDC substation. The space available for the HVDC breaker should be assessed prior to the design process. If smaller space is required, it may provide limitations on the number of components and their size.

11.2.2 Electrical Features

Breaker Cells

The IGBTs in the breaker cells of the DC breaker can be arranged in a matrix configuration, where its size may be adjusted according to the capabilities of the DC breaker. A breaker cell in this context is shown in figure 11.2. The energy MOV is omitted as they may be arranged different configurations than in parallel with each breaker cell. The maximum current capability

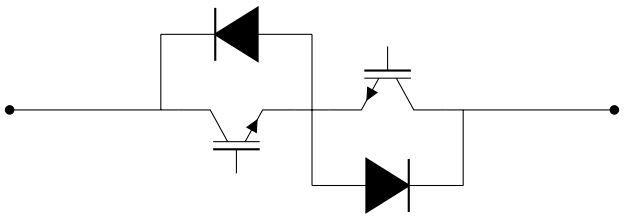


Figure 11.2: Definition of a DC breaker cell in chapter 11

is determined the number of parallel IGBTs. This also depends on the rated maximum current magnitude I_{Crm} of the IGBT and formulated as:

$$MI_{Crm} = I_{max} \tag{11.1}$$

Where I_{max} is the maximum current capability, and M is the number of breaker cells in parallel. As mentioned in the introduction, the DC breaker should be able to interrupt current in the range of ms. The results in chapter 8 showed that this is dependent on the counter voltage induced by the energy MOVs. A higher counter voltage results in smaller, thus improved break time t_{break}. As discussed in chapter 9, V_{CEmax} limits how high the counter voltage can be. More breaker cells must be placed in series in order to achieve a higher counter voltage and thus faster interruption. The desired voltage margin must also be taken into account. The number of breaker cells in parallel may be expressed as:

$$NV_{CEmax} - NV_{margin} = V_{CBmax} \tag{11.2}$$

Where the V_{CBmax} is the highest counter voltage provided by the energy MOVs and V_{margin} the desired voltage margin. The number of breaker cells in total n is given by:

$$n = MN \tag{11.3}$$

Figure 11.3 illustrates the latest discussion with regard to the number of semiconductors required for the main breaker of the hybrid topology.

If the magnitude of the counter voltage provides a line voltage higher than the insulation co-

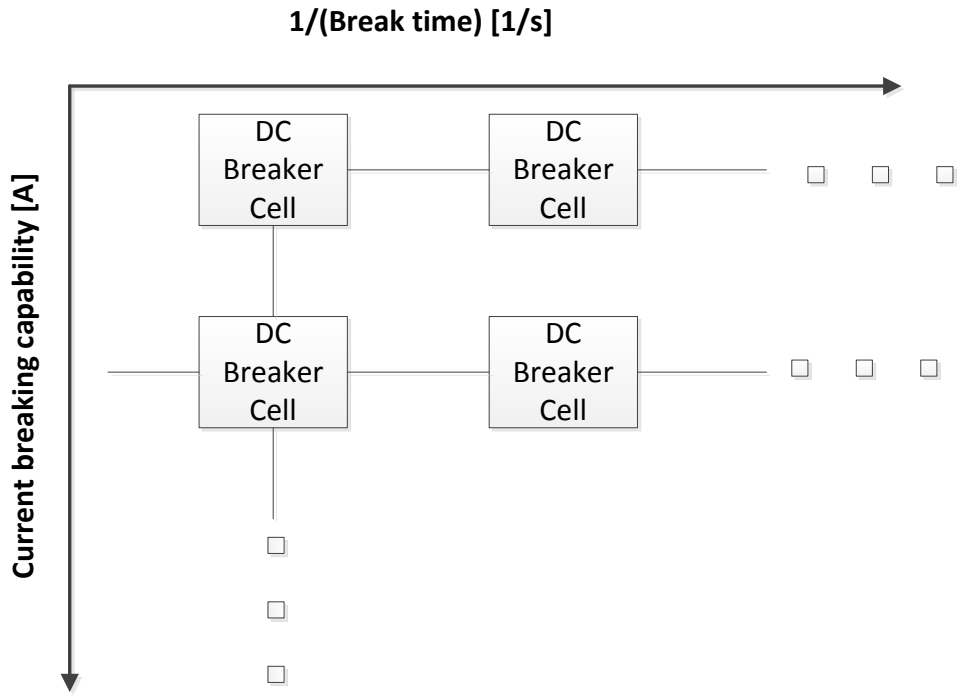


Figure 11.3: The relation between the properties of the DC breaker and the number of breaker cells

ordination, there will be a risk of insulation breakdown. Secondary faults may be initiated. The magnitude of the counter voltage is therefore limited by the insulation coordination $V_{I.C.}$ of the DC grid, expressed as:

$$V_{CBmax} < V_{I.C.} \tag{11.4}$$

The reliability of the DC breaker may increase with the number of breaker cells, but may as well complicate the control system and demand space which is not available particularly in an offshore location. Therefore, the type of IGBT should be considered in order to tolerate higher power densities. For the ABB hybrid circuit breaker topology a Bi-mode Insulated Gate Transistor (BIGT) is suggested which is an integrated state of the art diode and IGBT solution [59].

Current Limiting Devices

In the experiments and in the design of the DC breaker for the NTNU/SINTEF lab, the effect of the line inductance L_{line} is stressed. In case of short circuits with small L_{line}, the current may have a steep rise, and the maximum breaking capability is exceeded due to the time response $t_{response}$ of the protection system. In figure 11.1, it is observed that the current will rise additionally due to the commutation from the nominal current path and into the main breaker. In order

to avoid an unacceptable current rise, inserting a current limiting reactor (CLR) in series with the DC line is suggested. In figure 2.7 a CLR is indicated. The reactor should provide sufficient inductance such that the current will not exceed the current breaking capability under current interruption. Assuming zero resistance and insignificant line inductance in fault current path, the minimum inductance of the limiter reactor L_{CLR} needed may be expressed as:

$$L_{CLR} \leq V_{DC} \frac{t_{response}}{I_{max} - I_{trip}} \tag{11.5}$$

$$\text{where } I_{trip} > I_{load\ max}$$

Where $I_{load\ max}$ is the estimated maximum load current under normal operation of the DC line. The trip level of the protection system I_{trip} must be higher than $I_{load\ max}$ in order to ensure that the DC breaker trips under faulted states of the DC grid only. In addition to a reactor, superconducting fault current limiters are also suggested [4, 13].

Snubber Circuit

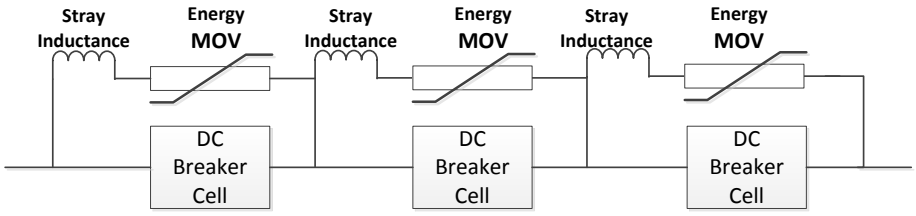
A snubber to protect the semiconductor may be essential for a DC breaker in order to avoid component failure due to transient overvoltages. In the experimental work described in section 8.2.6, one of the effects of a higher capacitance was longer time of the counter voltage rise. The effect may thus contribute to delay the total fault clearance time. As the time is crucial for the HVDC breaker operation, the capacitance of snubber may be too high. Investigating other options to a pure capacitor snubber is recommended for HVDC breakers. E.g. using an MOV snubber may provide the same protective properties [51]. The use of an MOV as a snubber may provide a faster voltage rise time of the counter voltage due to its non-linear resistive properties. Other more complicated snubber circuits for the LCS for the hybrid topology is described in [60]. These snubber configurations may also be an alternative for the main breaker as well.

Energy MOV

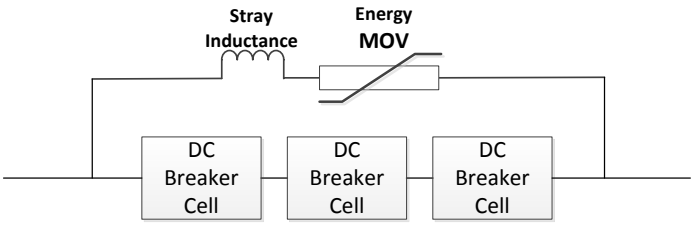
In section 9.5.2 the relation between the line inductance L_{line}, the maximum energy dissipated in the energy MOV $W_{MOV\,max}$ and the current capability were investigated. It was discussed that the current breaking capability is limited by the number of energy MOVs. For the HVDC breaker, the recommendation is to ensure sufficient $W_{MOV\,max}$ in order to dissipate the energy cosponsoring to the maximum line inductance and the desired current breaking capability. In the theoretical background, a simplified approach to calculate the energy the DC breaker needs to dissipate was provided. Using equation 3.9 and assuming no resistance in the system and a constant counter voltage, the requirement for $W_{MOV\,max}$ can be expressed as:

$$W_{MOV\,max} \geq \frac{1}{2}(L_{line} + L_{CLR}) I_{max}^2 (1 + \frac{V_{DC}}{(V_{CB\,max} - V_{DC})}) \tag{11.6}$$

The energy MOVs can be arranged in different configurations. One configuration is similar to the DC breaker in the NTNU/SINTEF lab with a parallel MOV for each DC breaker cell. It can be assumed that the energy MOV contributes with a certain stray inductance, which is seen in the equivalent circuit in figure 4.8. The electrical connection from the breaker cell to the energy MOV may provide some stray inductance as well. Therefore, the energy MOVs should be



(a) Energy MOV in parallel with each DC breaker cell



(b) Energy MOV in parallel with three DC breaker cells

Figure 11.4: The relation between the configurations of energy MOVs and the stray inductance

arranged in a way the effect of stray inductance is minimised. Having energy MOVs for each breaker cell may contribute to increase the stray inductance. This is illustrated in figure 11.4a. Another solution with three breaker cells in series per energy MOV may reduce the stray inductances. This is illustrated in 11.4b. Also more than three breaker cells in series may be actual as long as the voltage rating of the energy MOV is adjusted accordingly. However, the reliability of the DC breaker may decrease if the number of energy MOVs is minimised. If a energy MOV fails, the DC breaker may not to operate adequately if there are fewer and larger energy MOVs.

11.2.3 Control System and Thermal Features

In this section, the control system is referred to the internal DC breaker control system. The IGBTs needs to be controlled by gate drivers, with typical gate emitter voltage $V_{GE} = 15$ V. Operating a DC-line in high voltage near the IGBT must be handled very carefully. As with the implementation of the lab test model, galvanic isolation is needed to avoid ground potential contact with the DC-line. Ground potential contact inside the high voltage parts of the DC breaker may also be regarded a fault in the DC grid, but also a DC breaker failure. Besides galvanic isolation in the control system, the control system should have the minimum amount of time delay in order to minimise the response time.
Similar to the DC breaker in the NTNU/SINTEF laboratory, thermal considerations will be part of the HVDC breaker design process. The nominal current will flow through the LCS and active cooling is assumed needed. The type of cooling medium should also be considered as they may reduce the thermal heat resistivity further than with air-cooling fans. The analysis may be also provided by more sophisticated software for thermal analysis, e.g thermal modelling in 3

dimensions, in order to provide accurate results. Besides the semiconductors, the temperature of the energy should be under surveillance to ensure that the HVDC breaker is able to dissipate the energy in case of a fault.

11.2.4 Cost

The cost of the components should also be assessed in the design process. As the construction of the DC breaker may have a limited budget, the HVDC breaker must be designed accordingly. E.g. the number of semiconductors in series may be reduced and a longer break time must be tolerated.

Chapter 12

Discussion, Conclusion and Further work

12.1 Discussion and Conclusion

12.1.1 Theorethical Background

Chapters 2 to 5 were targeted at developing a theoretical background as a basis for the further work in terms of simulations,the design process, developing guidelines and assembling a DC breaker. The aspects of fault behaviour, current interruption, the components of a solid state breaker were explained. The explanations were based on what is expected to be relevant in the DC breaker design for the DC grid NTNU/SINTEF lab. Therefore, also simplifications were necessary in order to limit the scope of work. E.g. the DC grid was represented by a fixed voltage source with an inductor and a resistor, and semiconductor physics were very briefly considered. In order to analyse the results from the test model, design the final DC breaker, the theoretical background was used and referred to in several occasions. E.g explaining the forcing of the current to zero with the counter voltage and considerations of stray inductance. Also ratings of both the MOV and the IGBT were widely used in further chapters such as V_{CEmax} was mentioned in order to avoid failure of the IGBT.

12.1.2 Test Model

Chapter 6 described the assembly of the test model, and chapter 8 presented the main result from the experimental work with the test model. The test model was mainly used to examine the electrical features and some particular thermal features of a solid state DC breaker. The experimental testing undertaken examined the different aspects of the operation of a solid state breaker such as inductance, snubber and the source voltage. The interaction between the main components, the energy MOV and the IGBT module, were stressed, as these are the components which interaction forces the current to zero. The results also showed the advantages of fast current interruption of the solid state breaker, as the break time was mainly under 1 ms. The temperature of the energy MOV was also examined; cooling characteristics and the heating due to the repetitive short circuit. In chapter 9 it was assumed a 1 second time interval between the repetitive short circuit. A test with this time interval should also have been tested experimentally in order to provide better predictions on the behaviour of the energy MOV due to repetitive currents. Also some leakage current tests could be undertaken. However, the result was able to

provide the main aspects regarding the short circuit interruption which was considered as the main function of a DC breaker.

The results also showed some aspects regarding the measurement techniques. A rogowski coil and LEM sensors provided accurate results for fast changing currents during the line current commutation from the IGBT and into the energy MOV. The current clamping meter used was not able to measure the fast changes in the current. The results measuring with a rogowski coil were therefore eventually compared to the PSCAD simulations.

12.1.3 PSCAD Simulations

Chapter 7 described both the implementation of the test model and the final DC breaker in PSCAD. The simulations were presented in chapters 8 and 9. The PSCAD model of the test model needed adjustment since the preliminary result had unacceptable errors in the results compared to the experimental results from the test model. Therefore adjustment of the PSCAD model were carried out according to the observations of the experimental results. Especially, the MOV was adjusted to its maximum expected voltage according to the 10 % tolerance band, a certain line resistance and stray inductance was added. The adjusted PSCAD simulations were in an acceptable range when compared to the experimental results. These experiences were used when the final DC breaker model in PSCAD in order to ensure the validity of these results. In this model, the implementation had a conservative approach, in order to ensure the results. The simulation work was based on simplifications, and PSCAD simplifies the VI-characteristic of the semiconductors as linear. The assumptions of a capacitor snubber in the final design mitigating the overvoltage transients, allowed for more sufficient simulations as the time step could be increased.

An electro thermal equivalent circuit was also developed for the final DC breaker design. As the model assumes a one-dimensional heat transfer path, the values were used as an indication and evaluated the need for a simple cooling fan. The thermal aspects have many dependencies which is not accounted for in the electro thermal model such as the movement of air around the heat sink. The thermal resistance and the thermal time constant of the heat sink may subsequently vary. Further investigations may be carried out in order to validate the results regarding the thermal aspects of the DC breaker. For more accurate results, three-dimensional heat transfer simulation software may be used. This also may be actual for the thermal modelling of the varistor.

12.1.4 DC Breaker Design

In chapter 9, the components for the final design were selected and the corresponding DC breaker ratings were determined. Chapter 10 described the final configuration and the assembly of the DC breaker for the NTNU/SINTEF lab.

The selection of components was based on a discussion on the corner cases and the experimental activities undertaken with the test model. The corresponding expected ratings of the DC breaker were determined with the help of manual calculations and PSCAD simulations. In order to ensure the calculations and simulations, the approach with the regard to selection of components was conservative. This was regarded as necessary as the calculations are based upon assumptions and simplifications. A particular analysis of the line inductance in relation

to maximum energy dissipated stressed the importance to considerer the line inductance when designing a DC breaker. For the repetitive current, the calculation conducted was not corresponding to what was observed in the test model. In the test model, the results indicated a high tolerance for repetitive currents of the energy MOV. This was not the case with the calculations. Temperature surveillance was therefore suggested in order to ensure if the DC breaker is ready for current interruption, as the temperature should be under its critical level. An analysis of the limitations of the components were also carried out, such as the rated expected voltage of the energy MOV must not exceed the maximum tolerated voltage drop of the IGBT modules.

12.1.5 Design Guidelines

Chapter 11 described the development of design guidelines for HVDC circuit breakers, and the approach was to put the experiences previously made in the context of HVDC applications. The solid state breaker was assumed the same function as the main breaker in hybrid HVDC breaker topology. It was stated that a realisation of a solid state DC breaker in HVDC grid would provide unacceptable losses. As the electrical features were investigated mostly in the theoretical background, the test model and for the final DC breaker. However, some more general guidelines could be made for the control system, thermal considerations, cost and reliability.

12.1.6 Main Conclusions

- A theoretical background was established and provided a basis for the rest of the work.
- The test model assembled provided insight of a solid state DC breaker operation and to the design process with emphasis on the electrical features. The thermal experiments undertaken may be improved to provide better insight of the thermal features of MOVs in DC breakers.
- The results from the test model illustrated that the interaction between a MOV and the IGBT is an essential aspect for the operation of DC circuit breakers. The interaction forces the current to zero by commutating the current and providing a counter voltage.
- A simplified PSCAD model was established and was used in order to design a DC breaker after adjustments.
- A lab-scaled DC breaker was assembled. Still remains experimental validation and further testing.
- A DC breaker has design aspects as control system, thermal considerations, location and cost apart from the electrical aspects.
- Guidelines for a hybrid topology is possible to be carried out using insight from designing a solid state DC breaker

12.2 Further Work

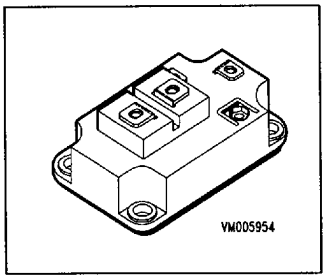
- Experimental validation of the electro thermal considerations of the semiconductors.
- Test the DC breaker for the ratings determined.
- Implementing temperature surveillance of the energy MOVs in the DC breaker.
- Further development of design guidelines for HVDC breakers in relation to experimental activities with the DC breaker assembled for NTNU/SINTEF lab.
- Use the bypass switch in the DC breaker to emulate the hybrid topology.
- Development of a protection system for the DC in the NTNU/SINTEF lab.
- Development of a distributed parameter line models for the DC grid in the NTNU/SINTEF lab in order to investigate a realistic interaction of a DC breaker with the DC grid.
- Develop electro-thermal models or 3-dimensional in PSCAD for the energy MOV for DC breaker applications.

Appendix A

SIEMENS IGBT: BSM 300 GA 120 DN2

IGBT Power Module

- Single switch
- Including fast free-wheeling diodes
- Package with insulated metal base plate



Type	V_{CE}	I_C	Package	Ordering Code
BSM 300 GA 120 DN2	1200V	430A	SINGLE SWITCH 1	C67076-A2007-A70
BSM 300 GA 120 DN2 S	1200V	430A	SSW SENSE 1	C67070-A2017-A70

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE}	1200	V
Collector-gate voltage R_{GE} = 20 kΩ	V_{CGR}	1200	
Gate-emitter voltage	V_{GE}	± 20	
DC collector current T_C = 25 °C T_C = 80 °C	I_C	430 300	A
Pulsed collector current, t_p = 1 ms T_C = 25 °C T_C = 80 °C	I_{Cpuls}	860 600	
Power dissipation per IGBT T_C = 25 °C	P_{tot}	2500	W
Chip temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	-55 ... + 150	
Thermal resistance, chip case	R_{thJC}	≤ 0.05	K/W
Diode thermal resistance, chip case	R_{thJCD}	≤ 0.125	
Insulation test voltage, t = 1min.	V_{is}	2500	Vac
Creepage distance	-	20	mm
Clearance	-	11	
DIN humidity category, DIN 40 040	-	F	-
IEC climatic category, DIN IEC 68-1	-	55 / 150 / 56	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Gate threshold voltage $V_{GE} = V_{CE}$, I_C = 12 mA	$V_{GE(th)}$	4.5	5.5	6.5	V
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 300 A, T_j = 25 °C V_{GE} = 15 V, I_C = 300 A, T_j = 125 °C	$V_{CE(sat)}$	- -	2.5 3.1	3 3.7	
Zero gate voltage collector current V_{CE} = 1200 V, V_{GE} = 0 V, T_j = 25 °C V_{CE} = 1200 V, V_{GE} = 0 V, T_j = 125 °C	I_{CES}	- -	4 16	5.6 -	mA
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	-	-	320	nA
AC Characteristics					
Transconductance V_{CE} = 20 V, I_C = 300 A	g_{fs}	124	-	-	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	-	22	-	nF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	-	3.3	-	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	-	1.2	-	

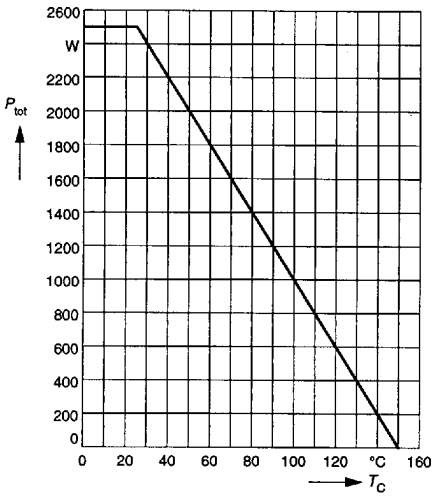
Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Switching Characteristics, Inductive Load at T_j = 125 °C					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 300 A R_{Gon} = 3.3 Ω	$t_{d(on)}$	-	100	200	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 300 A R_{Gon} = 3.3 Ω	t_r	-	110	220	
Turn-off delay time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 300 A R_{Goff} = 3.3 Ω	$t_{d(off)}$	-	600	800	
Fall time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 300 A R_{Goff} = 3.3 Ω	t_f	-	80	120	
Free-Wheel Diode					
Diode forward voltage I_F = 300 A, V_{GE} = 0 V, T_j = 25 °C I_F = 300 A, V_{GE} = 0 V, T_j = 125 °C	V_F	- -	2.3 1.8	2.8 -	V
Reverse recovery time I_F = 300 A, V_R = -600 V, V_{GE} = 0 V dI_F/dt = -2500 A/µs, T_j = 125 °C	t_{rr}	-	0.55	-	µs
Reverse recovery charge I_F = 300 A, V_R = -600 V, V_{GE} = 0 V dI_F/dt = -2500 A/µs T_j = 25 °C T_j = 125 °C	Q_{rr}	- -	14 40	- -	µC

Power dissipation

$P_{tot} = f(T_C)$

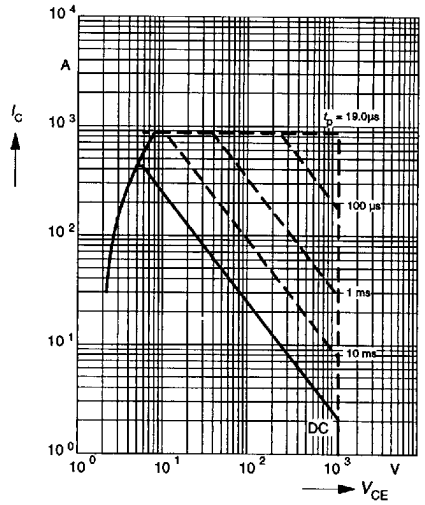
parameter: $T_j \leq 150$ °C



Safe operating area

$I_C = f(V_{CE})$

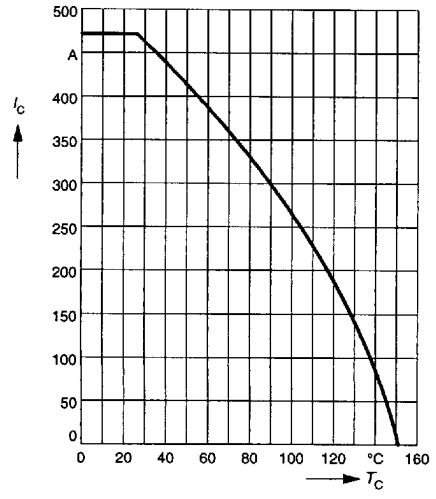
parameter: $D = 0$, $T_C = 25$°C , $T_j \leq 150$ °C



Collector current

$I_C = f(T_C)$

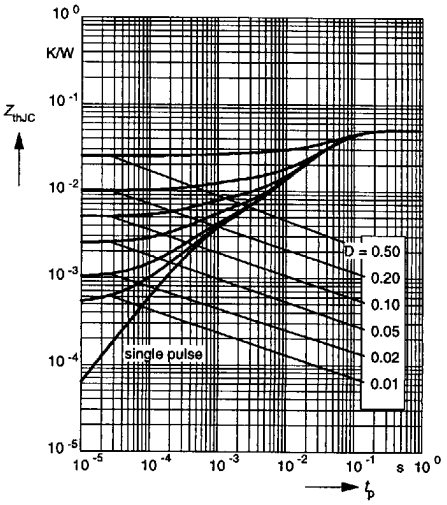
parameter: $V_{GE} \geq 15$ V , $T_j \leq 150$ °C



Transient thermal impedance IGBT

$Z_{th\,JC} = f(t_p)$

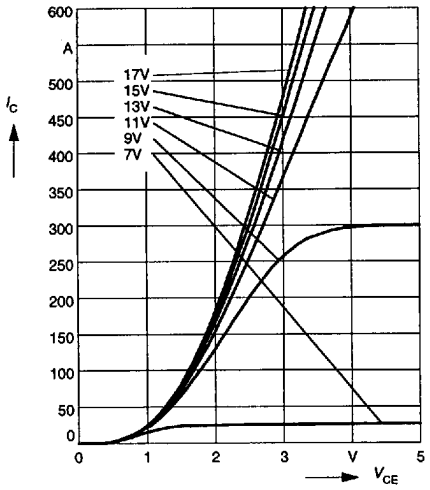
parameter: $D = t_p / T$



Typ. output characteristics

$I_C = f(V_{CE})$

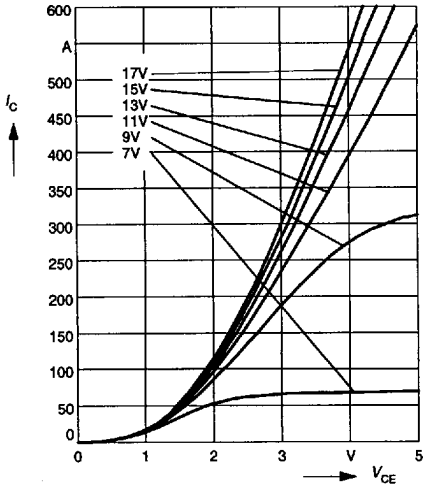
parameter: $t_p = 80\ \mu s$, $T_j = 25\ °C$



Typ. output characteristics

$I_C = f(V_{CE})$

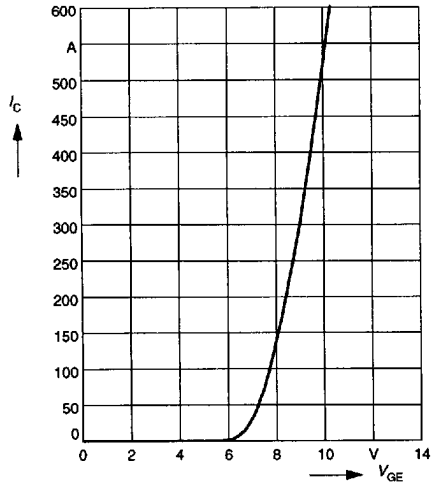
parameter: $t_p = 80\ \mu s$, $T_j = 125\ °C$



Typ. transfer characteristics

$I_C = f(V_{GE})$

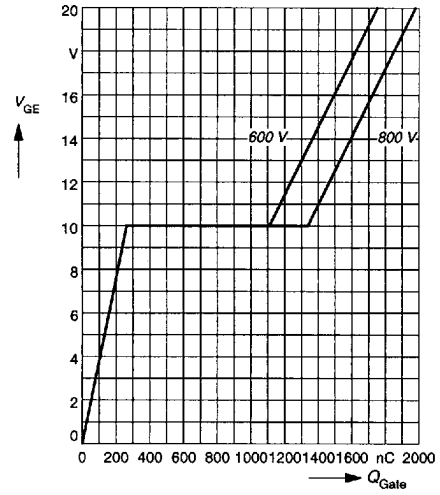
parameter: $t_p = 80\ \mu s$, $V_{CE} = 20\ V$



Typ. gate charge

$V_{GE} = f(Q_{Gate})$

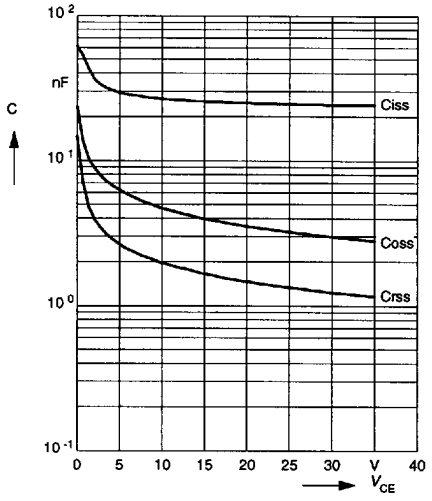
parameter: $I_{C\ puls}$ = 300 A



Typ. capacitances

$C = f(V_{CE})$

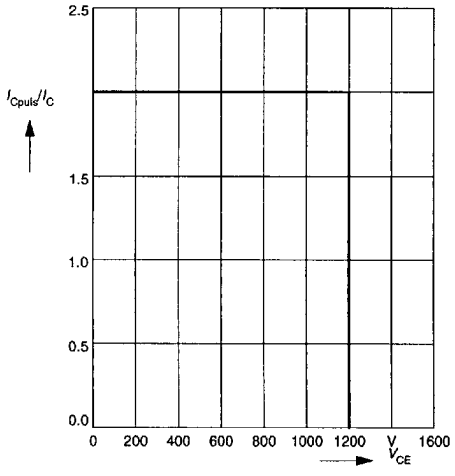
parameter: V_{GE} = 0 V, f = 1 MHz



Reverse biased safe operating area

$I_{Cpuls} = f(V_{CE})$, T_j = 150°C

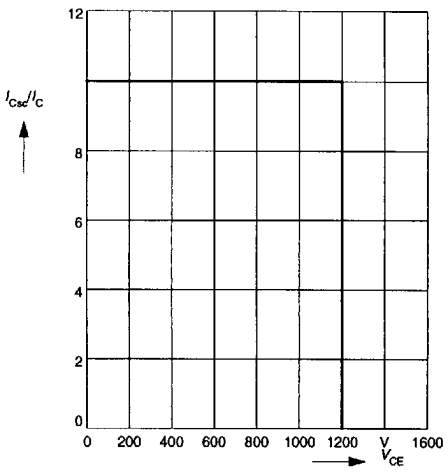
parameter: V_{GE} = 15 V



Short circuit safe operating area

$I_{Csc} = f(V_{CE})$, T_j = 150°C

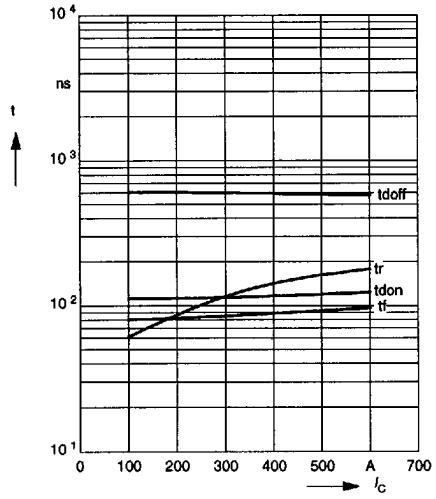
parameter: V_{GE} = ± 15 V, t_{SC} ≤ 10 µs, L < 20 nH



Typ. switching time

$I = f(I_C)$, inductive load, $T_j = 125°C$

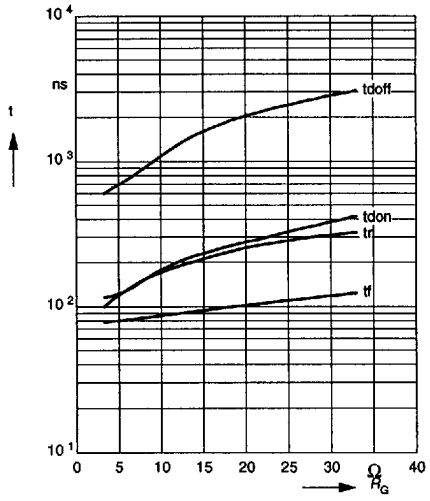
par.: $V_{CE} = 600$ V, $V_{GE} = \pm 15$ V, $R_G = 3.3\ \Omega$



Typ. switching time

$t = f(R_G)$, inductive load, $T_j = 125°C$

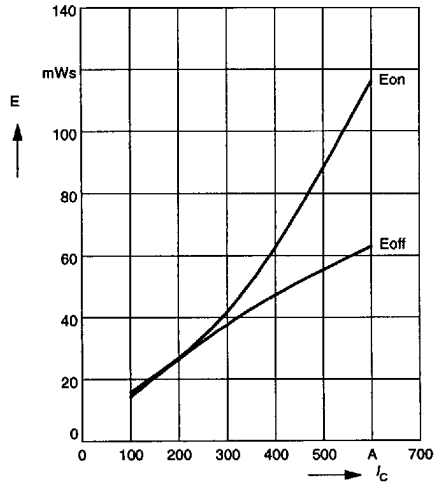
par.: $V_{CE} = 600$ V, $V_{GE} = \pm 15$ V, $I_C = 300$ A



Typ. switching losses

$E = f(I_C)$, inductive load, $T_j = 125°C$

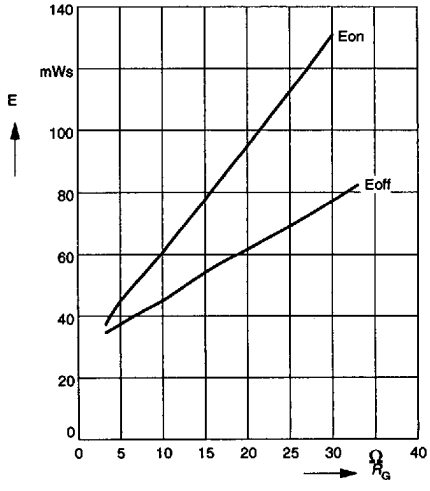
par.: $V_{CE} = 600$ V, $V_{GE} = \pm 15$ V, $R_G = 3.3\ \Omega$



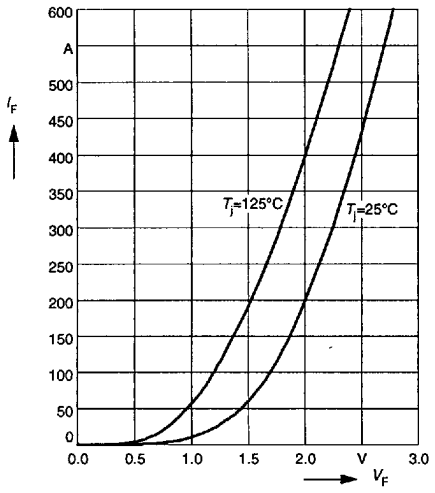
Typ. switching losses

$E = f(R_G)$, inductive load, $T_j = 125°C$

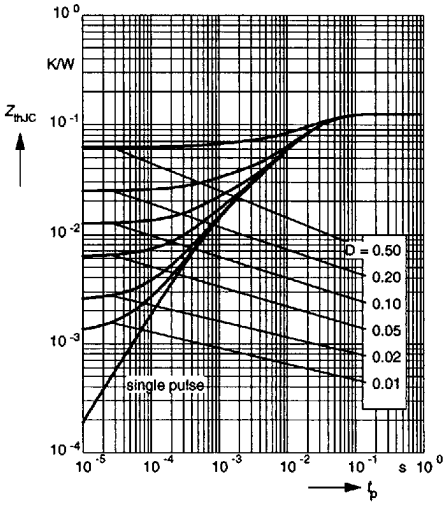
par.: $V_{CE} = 600$V, $V_{GE} = \pm 15$ V, $I_C = 300$ A



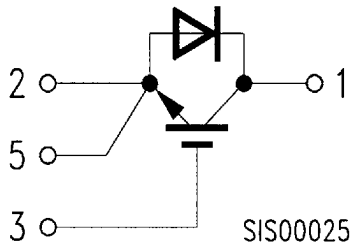
Forward characteristics of fast recovery reverse diode $I_F = f(V_F)$
parameter: T_j



Transient thermal impedance Diode
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



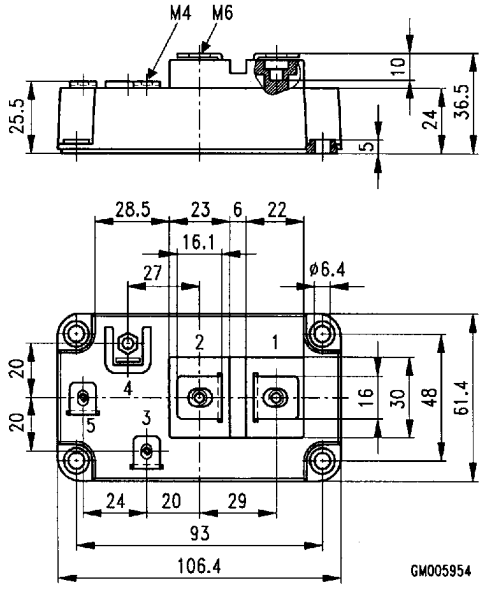
Circuit Diagram



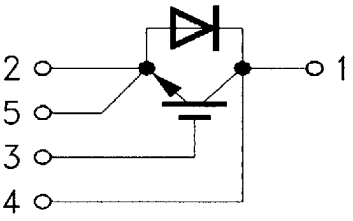
Package Outlines

Dimensions in mm

Weight: 420 g



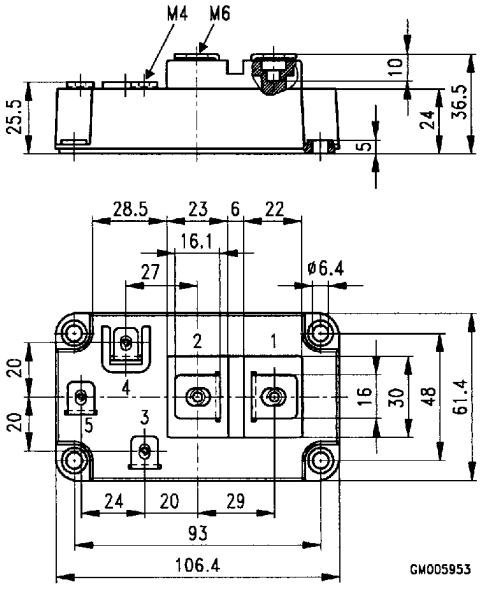
Circuit Diagram



Package Outlines

Dimensions in mm

Weight: 420 g



Appendix B

Time Delay of Contactor Switch

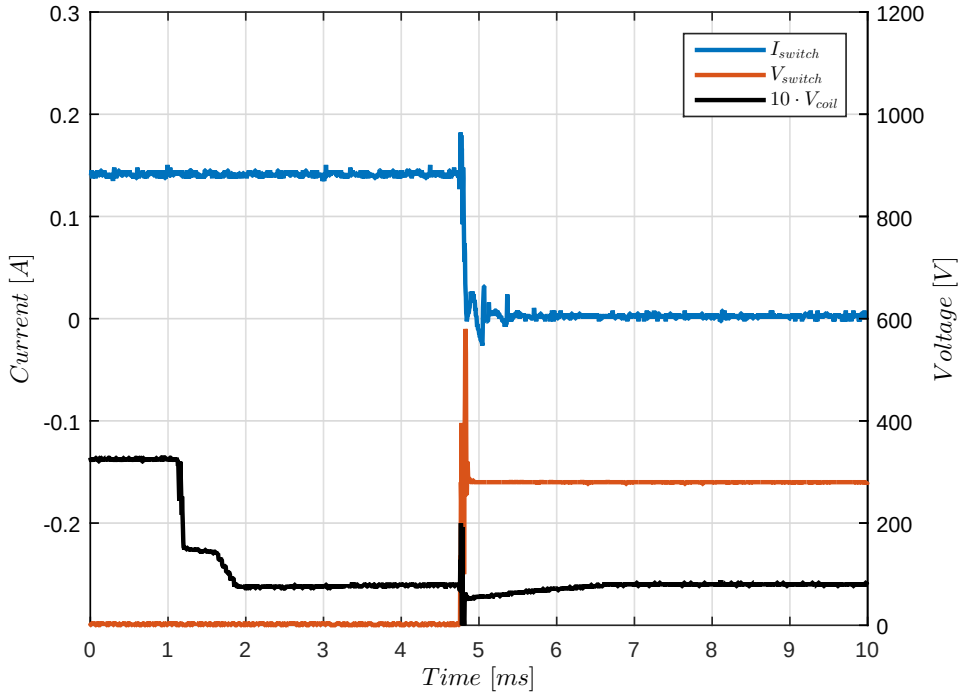


Figure B.1: Contactor switch operates with 0.15 A including the coil voltage

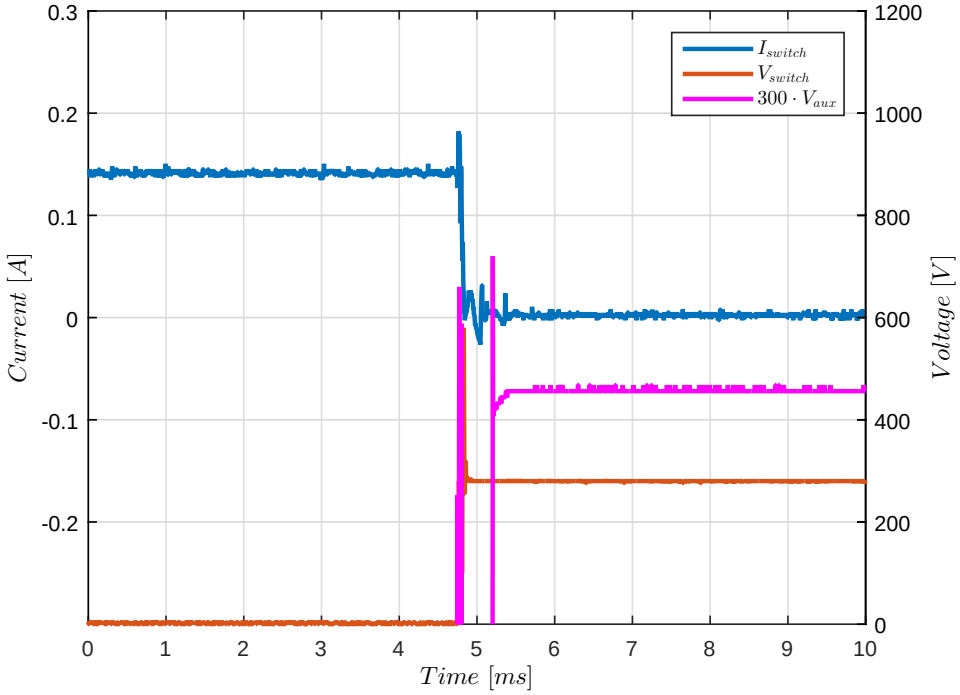


Figure B.2: Contactor switch operates with 1 *A* including the auxiliary contact voltage

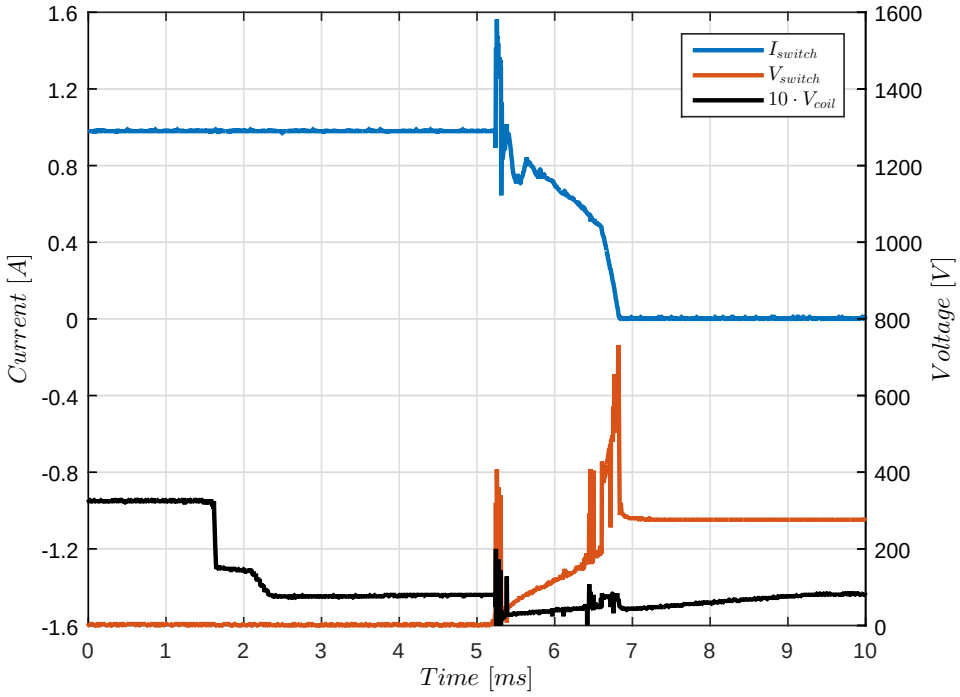


Figure B.3: Contactor switch operates with 1 *A* including the coil voltage

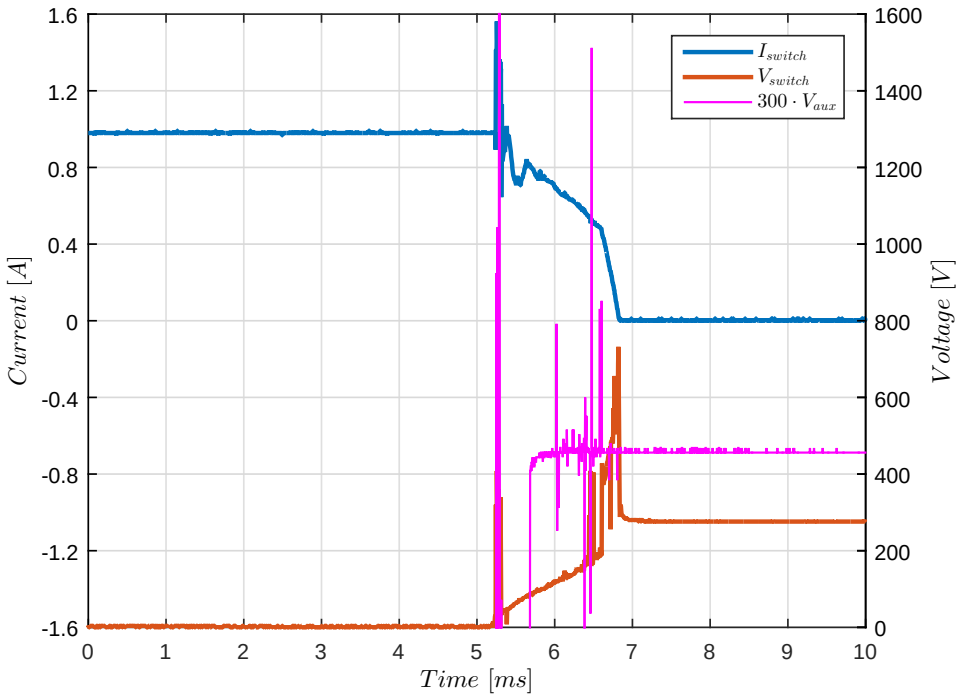


Figure B.4: Contactor switch operates with 1 A including the auxiliary contact voltage

Appendix C

Calculations

IGBT Module Power Loss

Infineon IGBT

Assumptions: $V_{GE} = 15\ V$ and $T_j = 125\ °C$
From the data sheet [54]: $(V_1, I_1) = (1.12, 100)$ and $(V_2, I_2) = (1.64, 300)$

$$\frac{\Delta I}{\Delta V} = \frac{200}{0.52} = 385.62\ \text{S}$$

$$V_{CE}(I_C) = \frac{I_C}{385.62} + 0.86$$

Infineon Anti-Parallel Diode

Assumptions: $V_{GE} = 15\ V$ and $T_j = 125\ °C$
From the data sheet [54]:$(V_1, I_1) = (1, 100)$ and $(V_2, I_2) = (1.44, 300)$

$$\frac{\Delta I}{\Delta V} = \frac{200}{0.44} = 454.55\ \text{S}$$

$$V_{CE}(I_C) = \frac{I_C}{454.55} + 0.78$$

Mitsubushi HVIGBT

Assumptions: $V_{GE} = 15$ V and $T_j = 125$ °C
From the data sheet [53]: $(V_1, I_1) = (2.7, 100)$ and $(V_2, I_2) = (4.1, 300)$

$$\frac{\Delta I}{\Delta V} = \frac{300 - 100}{4.1 - 2.7} = 142.86\ \text{S}$$

$$V_{CE}(I_C) = \frac{I_C}{142.86} + 2.00$$

Mitsubushi Anti-Parallel Diode

Assumptions: $V_{GE} = 15$ V and $T_j = 125$ °C
From the data sheet [53]: $(V_1, I_1) = (1.6, 100)$ and $(V_2, I_2) = (2.9, 300)$

$$\frac{\Delta I}{\Delta V} = \frac{200}{2.9 - 1.6} = 153.85 \text{ S}$$

$$V_{CE}(I_C) = \frac{I_C}{153.85} + 0.95$$

Maxium Current with Respect to the Energy MOV

Energy MOV: V DC B60K460 EPCOS HighE series block varistor
Rated voltage:$V_{MOV} = 615$ V DC[56]
Assumtions: $T_{MOV} < T_{critical} = 85$°C
From the VI-characteristic in data sheet VI-characteristic: $(V_1, I_1) = (10^3, 1400)$ and $(V_2, I_2) = (10^4, 1800)$

$$\alpha = \frac{\ln 10^4 - \ln 10^3}{\ln 1800 - \ln 1400} = 9.16$$

$$K_{MOV} = \frac{I_2}{V_2^{\alpha}} = 1.52 \cdot 10^{-26}$$

$$I = K_{MOV} V^{\alpha} = 5925.92 \text{ A}$$

Appendix D

Snubber Capacitor Discharge

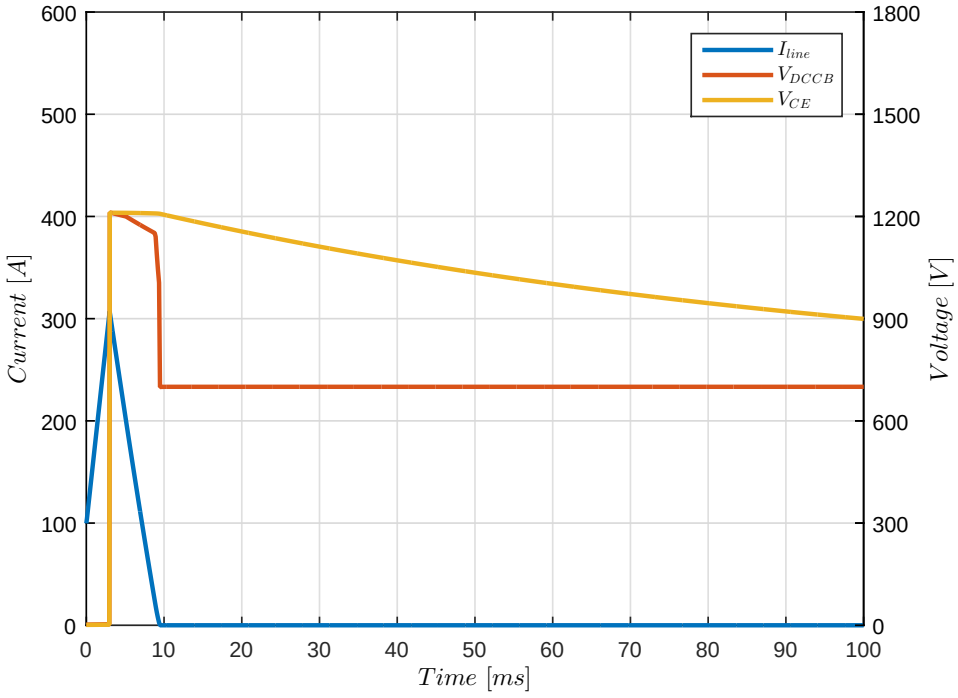


Figure D.1: Current interruption and discharge of the snubber

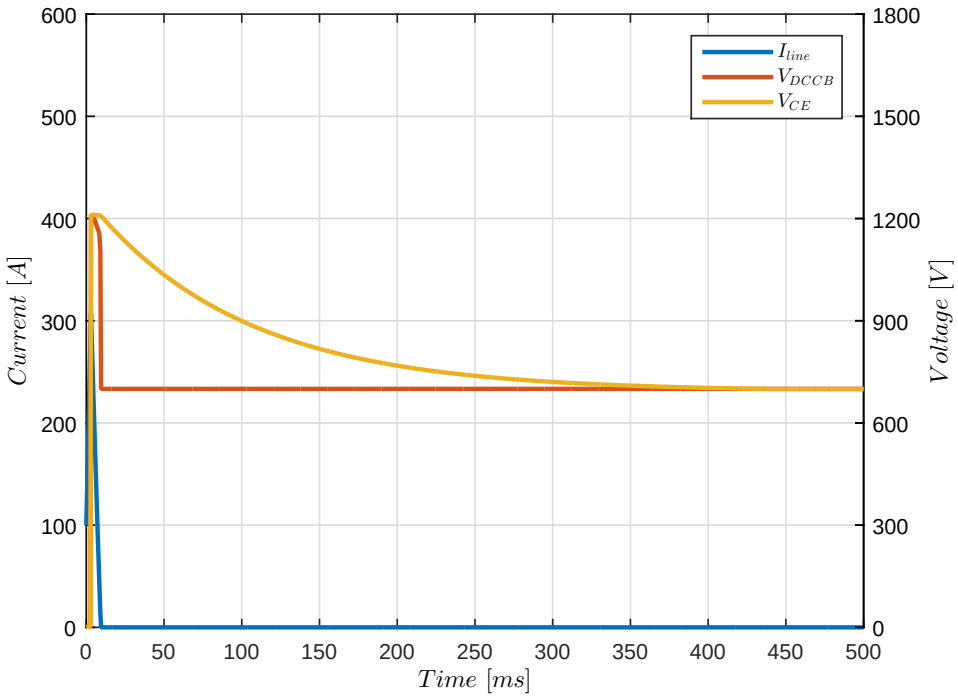


Figure D.2: Current interruption and discharge of the snubber

Appendix E

Maximum Current Breaking Capability

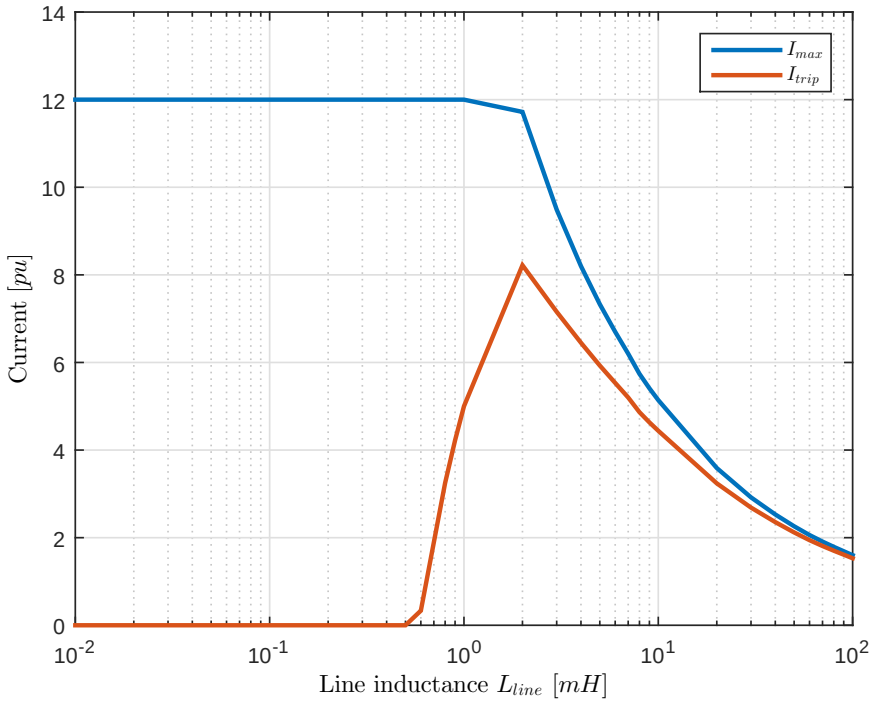


Figure E.1: The current breaking capability I_{max} as a function line inductance L_{line}, I_{max} is the actual current interrupted and I_{trip} is the maximum detection level of the protection system, $t_{response} = 1\ ms$

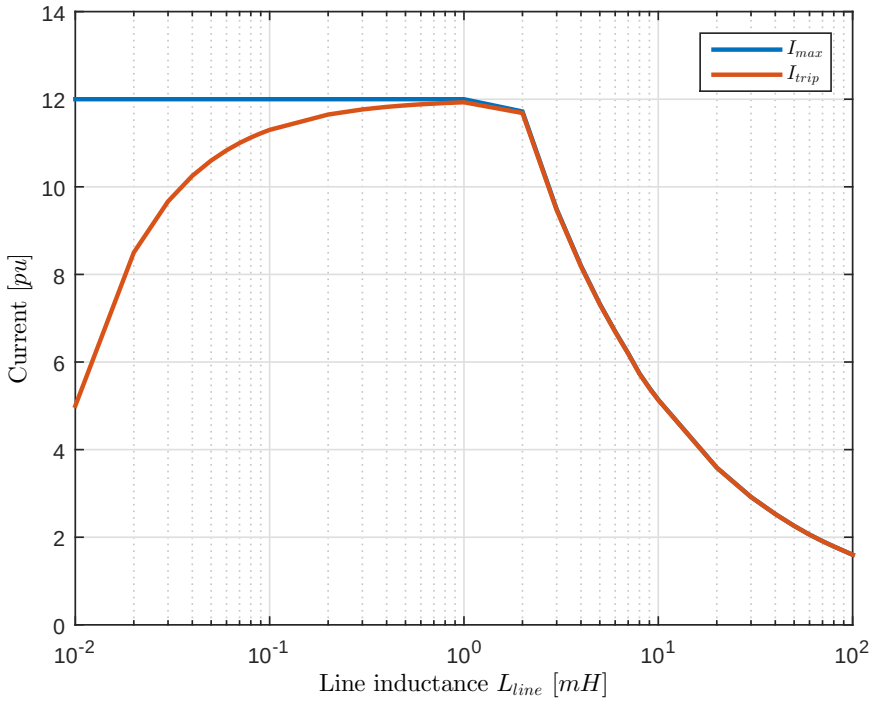


Figure E.2: The current breaking capability I_{max} as a function line inductance L_{line}, I_{max} is the actual current interrupted and I_{trip} is the maximum detection level of the protection system, $t_{response} = 0.01\ ms$

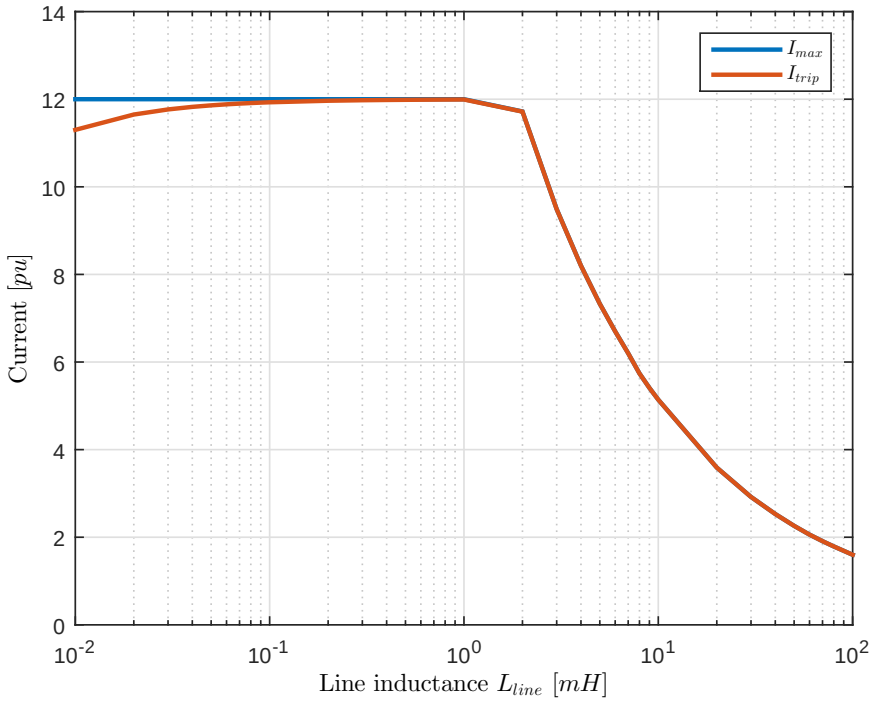
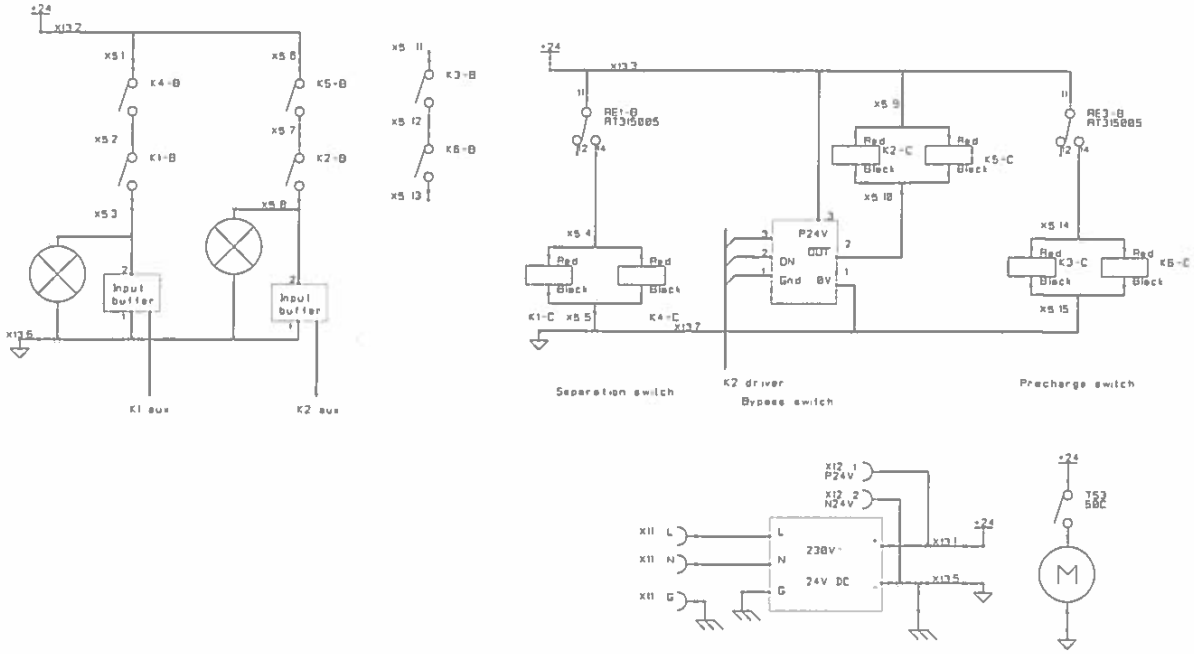


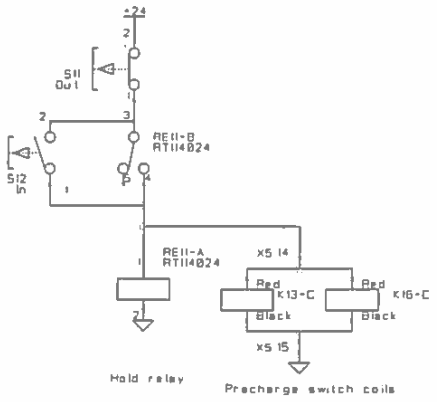
Figure E.3: The current breaking capability I_{max} as a function line inductance L_{line}, I_{max} is the actual current interrupted and I_{trip} is the maximum detection level of the protection system, $t_{response} = 0.0001\ ms$

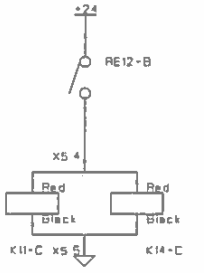
Appendix F

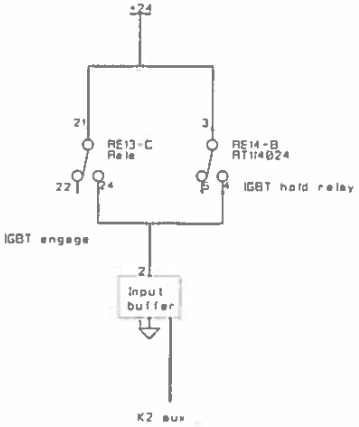
DC breaker circuit diagrams

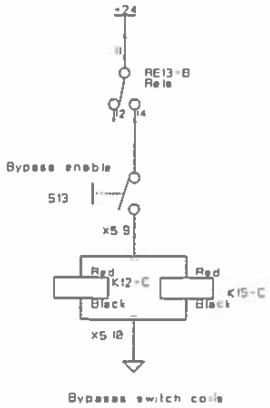


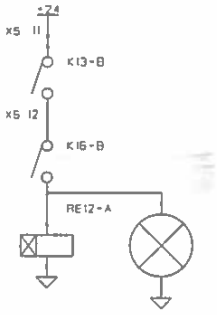
FIL DC circuit breaker.sch			
UTLEGG	PROSJ 502000004	ARK 2 av 4	
KONSTRUERT K Ljokelsoy	DATO 25.8.2016		
SINTEF Energi AS	DC circuit breaker Control circuit		

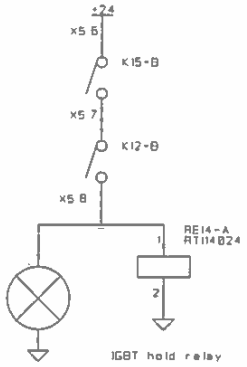


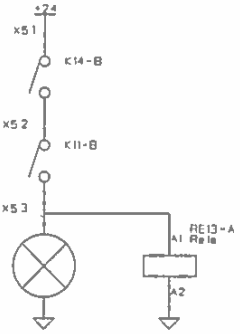


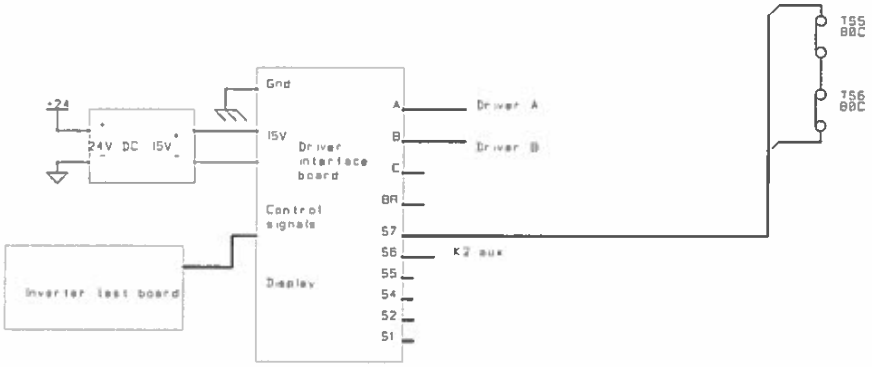


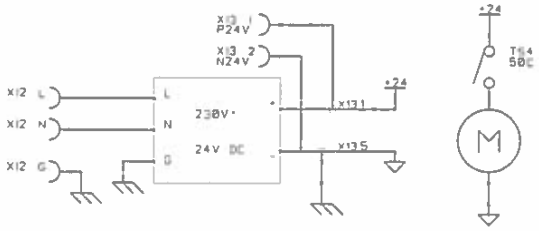




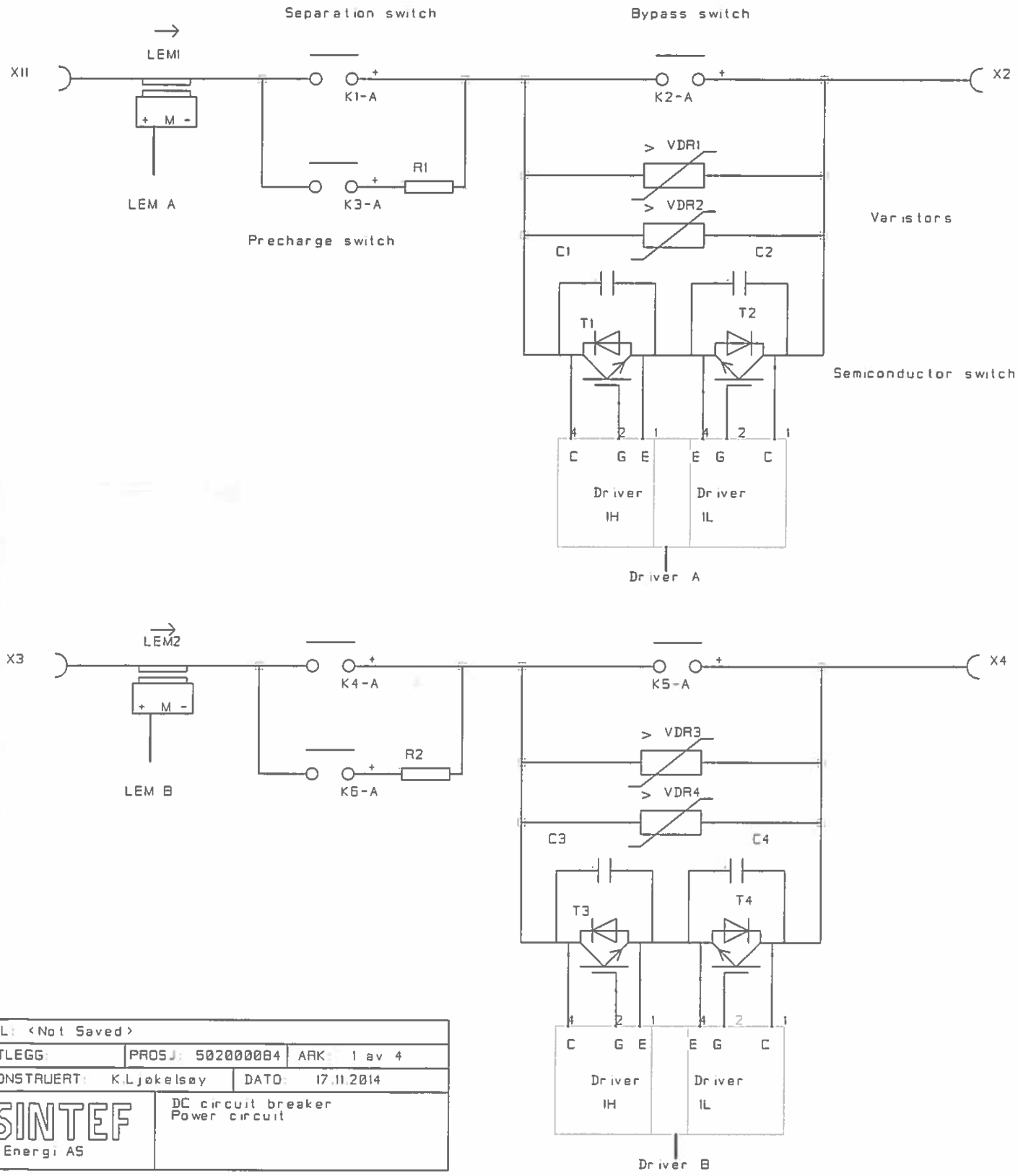








FIL: DC circuit breaker scm			
UTLEGG:	PROSJ 502000084	ARK 4 av 4	
KONSTRUERT K Ljokelsoy		DATO 26 01 2016	
SINTEF Energi AS	DC circuit breaker Relay control variant		



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KONSTRUERT: K.Ljøkelsøy	DATO: 17.11.2014		
SINTEF Energi AS	DC circuit breaker Power circuit		

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