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Ultra-Low Power SAR-ADC in 28nm CMOS Technology

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Master of Science in Electronics
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Problem description

The project goal is to design a 10-bit, sub-nanowatt SAR ADC in 28nm FD-SOI technology with a sampling frequency of $1kS/s$. Main performance characteristic is power consumption; with secondary characteristics being resolution and energy efficiency (FOM).

The project tasks are as follows:

- Confirm validity of previous work in the new technology
- Improve on previous work
- Do design and layout of the ADC at transistor level
- Characterize performance through simulation.

Design specifications are as follows:

Parameter	Value
CMOS technology	28nm FD-SOI
Supply voltage	$< 1V$
Maximum input level	$1V_{pp}$
Sampling frequency	$1kHz$
Resolution	10-bit

The project was given on January 19, 2015. It was supervised by Trond Ytterdal, IET , together with assistant supervisior Carsten Wulf ,IET , and Snorre Aunet, IET .

Abstract

This thesis presents an improved ultra-low power 10-bit 1 kS/s successive approximation register (SAR) analog to digital converter (ADC) building on the work performed by Simon Josepshen in 2013. The improved ADC has a supply of 450mV and operates at almost half the power consumption of previous work; achieving a consumption of 691.5 pW in post-layout simulation. This is possibly the best power consumption found in available literature. Higher resolution and lower power consumption is achieved with incremental changes to the original design and by exploiting the benefits of new technology. The design differs from the previous in some key ways; having a different comparator topology, different switching procedure and asynchronous operation. The effective resoultion is found to be around 9.4-bit, giving a figure-of-merit of 1.0 fJ/conversion-step.

Sammendrag

Denne masteroppgaven presenterer en ultra-laveffekt 10-bit 1 kS/s suksessivt-tilnærmingsregister (SAR) analog til digital converter (ADC) som bygger på tidligere utført arbeid av Simon Josephsen i 2013. Den forbedrede ADCen har en spenningsforsyning på 450 mV og opererer med tilnærmet halvparten av effektforbruket til forrige design; med et forbruk på 691.5 pW i simulering etter utlegg. Dette er muligens det beste strømforbruket som finnes i tilgjengelig litteratur. Høyere oppløsning og lavere effektforbruk er oppnåd gjennom inkrementelle forandringer til det originale designet og ved å utnytte fordeller med ny teknologi. Designet skiller seg fra forrige design i noen nøkkelområder; den har en annen komparator topologi, annen tilnærminsprossedyre og asynkron operasjon. Den effektive oppløsningen ble funnet til å være rundt 9.4-bit, noe som gir et godhetstall på 1.0 fJ/konverterings-steg.

Preface

This thesis is submitted in partial fullfillment of the requirements for the degree of Master of Science (MSc) at the Department for Electronics and Telecommunication (IET), Norwegian University of Science and Technology (NTNU). The work was carried out in the period of January to July 2015, under the supervision of Professor Trond Ytterdal, who is with the IET at NTNU .

Acknowledgements

I would like to thank Professor Trond Ytterdal for suggesting the project and for providing his insight and advice. Another thanks to Carsten Wulff for providing insightfull advice and technical support.

Thanks to all the analog-guys in the reading room; Endre Larsen Spydeberg, Harald Garvik and Erlend Strandvik Reindalen, its been nice sharing this last part of the master-degree with you. The previous experience you guys had was a great help. Extra thanks to Harald Garvik for supplying the load capacitors used in this project.

I would also like to thank Professor Snorre Aunet and Aslak L. Holen Lom for pointers and advice regarding the digital portion of the project.

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Abbreviations

ADC	*analog to digital converter*
CMOS	*complementary metal-oxide-semiconductor*
DAC	*digital to analog converter*
DIBL	*drain-induced barrier lowering*
ENOB	*effective numbers of bits*
FD-SOI	*fully depleted silicon-on-insulator*
FOM	*figure-of-merit*
IET	*Department for Electronics and Telecommunication*
MSc	*Master of Science*
NTNU	*Norwegian University of Science and Technology*
SAR	*successive approximation register*
SCE	*short channel effects*
SNR	*signal noise ratio*
SOI	*silicon-on-insulator*
SOTB	*Silicon on Thin BOX*

Chapter 1

Introduction

The device that bridges the analog and digital world is known as an analog to digital converter (ADC). Digital systems are not able to read an analog signal unless they are converted from an analog quantity into a digital number. This is the jobb of the ADC , and it is used in most applications where digital systems are "sensing" the real world in a non-binary way[1]. Some examples are; radio recievers, cameras, audio recorders, gyroscopes and touchscreens.

As technology scales down, digital circuits see significant performance improvements in speed and power consumption. This is true, to a lesser extent for analog circuits. A rule of thumb is that an analog device consumes more power than a comparable digital device. ADCs are partially analog and partially digital; with the latter becomming more important in the future. Today most of the afforementioned devices and sensors can be found on a cell-phone or tablet, and as a consequence, improvements in ADC power consumption play a key role in extending battery life and functionality of wearable electronics. New medical applications become available as battery life is extended. Wireless sensor nodes are often mentioned as a motivation for reducing ADC power usage. Increased life for sensor nodes enables long term monitoring of patients and can eliviate risks associated with severeal cronic medical conditions. Other emerging fields such as energy harvesters [11] will benefits greatly from any power reduction in analog components.

1.1 Project specifications

This master's thesis aims to implement an ultra-low power ADC in 28nm fully depleted silicon-on-insulator (FD-SOI) technology with a sampling frequency of 1 kS/s, 10-bit resolution, asynchronous operation and sub-nanowatt power consumption. It builds on a previous master's thesis from 2013 by Simon Josephsen [10] ; in which, he designed and simulated a 9-bit ultra-low power ADC in 65nm technology. His work resulted in world class ultra-low power performance, obtaining a power consumption of 1.2 nW.

Since comparing different analog designs against each other is not straight forward, designers usually adopt some figure-of-merit (FOM). These equations can be seen as weights that prioritize different strengths of a system. When referring to FOM in this thesis, it will be the in the form shown below:

[1] A keyboard is a binary input device since it only detects two levels.

$$FOM = \frac{P_{\text{total}}}{2^{\text{ENOB}} \cdot f_{\text{s}}} \, [J/\text{conversion-step}] \tag{1.1}$$

The formula provides a way to measure the effectiveness of a given design based on a few parameters: P_{tot} being the total power consumed by the system, ENOB is the effective numbers of bits and f_s is the Nyquist sampling frequency.

1.2 Main contributions

This thesis presents a ADC design which improves on previous work by achieving, to the authors knowledge, the lowest published power consumption, and world class FOM . Improvements to the power consumption and resolution of the design is achieved by:

- changing the clocking scheme from synchronous to asynchronous,
- choosing a more optimal switching scheme,
- changing the topology of logic gates and replacing large clusters of gates with dedicated circuits,
- reducing overall capacitance use,
- change of comparator topology,
- increasing the supply voltage.

1.3 Report outline

The report will be organized as follows:

1. **Chapter 2** provides background theory relevant to the later chapters in this report. It covers some general non-idealities and some application specific non-idealities, power consumption, technology properties, digital power saving and a short description of typical SAR ADCs building blocks.
2. **Chapter 3** covers the current state-of-the-art in ultra low power design, general trends and typical topologies.
3. **Chapter 4** describes the full ADC from a top level perspective and covers each sub-component in detail. It will also elucidate design considerations an justify the changes made to the previous design.

4. **Chapter 5** presents the ADC layout and briefly comments on design considerations and problems associated with the work.
5. **Chapter 6** presents the results from circuit simulations; both pre and post-layout.
6. **Chapter 7** provides a discussion around the results in chapter 6.
7. **Chapter 8** presents the conclusion.

Chapter 2

Low power digital design

This chapter will present theory that is relevant to the digital portion of the design process. Important concepts such as dynamic and static power consumption will be explained as well as the different design techniques available for low power design.

2.1 Noise

Noise is always present in electronic circuits. There are two sources of circuit noise. One is the inteference from the outside world; in which case it can be eliminated through carefull design optimization, the other is inherent noise which can never ble eliminated as they are occur due to the structure and function of the components in the circuit. The two main types of inherent noise are: thermal and flicker noise.

2.1.1 Thermal noise

Capacitors do not generate noise, but instead accumulate it. The effect of noise from other devices can be reduced by connecting larger capacitances to their nodes. In a circuit consisting only of passive devices and MOSFETS in their triode region, the squared rms noise on each capacitor is as in [6] :

$$V_{no(rms)}^2 = \frac{kT}{C} \tag{2.1}$$

where k is the Boltzmann's constant, T is the temperature in Kelvin and C_s is the capacitor where noise is accumulated.

2.1.2 Flicker noise

Regarding flicker noise; [12] says that "This has perhaps been the most widely studied and debated phenomena in the history of noise." while descibing the 50-year history of MOSFET noise studies. There has been some debate regarding the source of the 1/f fluctuations in transistors. The two main theories have been that they are either caused by carrier trapping and deptrapping at the oxide-semiconductor interface (number fluctuation) or mobility fluctuations due to bulk effects. The former has the most consensus. The flicker noise model for MOSFETs used in most simulators is as follows:

$$i_n^2 = \frac{K}{f}\frac{g_m^2}{WLC_{\text{ox}}^2}\Delta f \tag{2.2}$$

K is a konstant dependent on the device type, g_m is the transconductance, W and L are the gate dimensions, C_{ox} is the gate capacitance per unit area, f is the frequency, and Δf is the bandwidth of observation [12], [6] .

2.2 Process variation and mismatch

Several of the variations of the transistor parameters are a result of the fabrication procedure. For example; dopant consentration and oxide thickness vary considerably and result in significant variations in V_{t} and capacitances. In order to design for these variations, factories provide several transistor models that represent different process corners.

The reproduceability of any fabrication process will have limits, making it impossible to produce transistors that are perfectly identical. This mismatch between transistors exists even in the absence of the previously mentioned process variations.

The doping used in several modern technologies is a good example. Transistors are made using a small number of dopants, as few as a hundred, and will vary with the location on the substrate. This changes parameters such as treshold voltage.

$$\sigma^2(\Delta P) = \frac{A_{\text{P}}^2}{WL} + S_{\text{P}}^2 D^2 \tag{2.3}$$

The above equation describes the expected Gaussian variation in device parameter P between two devices. W and L denote the device dimensions and D is the distance between them. S_P and A_P are proporsonal constants derived through experimental measurement. Variations in V_{t} and $K' = \mu_n C_{ox} W/L$ are often the most important when doing analog design.

2.3 Power dissipation

There are three main sources of power dissipation; short circuit power, dynamic power and static power. An expression for the total power consumption in digital CMOS circuits is presented as described in [13] :

$$P_{\text{total}} = p_t(C_L \cdot V \cdot V_{dd} \cdot f_{clk}) + I_{sc} \cdot V_{dd} + I_{\text{leakage}} \cdot V_{dd} \tag{2.4}$$

Dynamic power consumption comes from the charging and discharging of internal capacitances in a circuit. Dynamic power increases with the number of transitions during circuit operation and scales with the supply voltage. The first term in Equation(2.4) describes the

dynamic power consumption. p_t is the probability of a transition occuring. The voltage swing is defined by V; usually the supply voltage, but it can be lower. C_L is the switching capacitance being charged or discharged during a transition; as illustrated in Figure 2.1. f_{clk} is the switching frequency.

The second term in Equation(2.4) comes from the short circuits that occur in during switching of CMOS circuits. Consider the inverter shown in Figure 2.1. As the input signal transitions from low to high, at one point both transistors are on, creating a temporary short between supply and ground. Shorts can increase power consumption if rise and fall times are uneven or the input signal transition is too slow. Low power circuits will usually have slower transition speeds than a conventional circuit. This is due to the reduced supply voltage and the way transistors are sized for low power. Because of this, short circuits become a larger contributor to the total power consumption in low power circuits [14] . The effect can be largely ignored if correct transistor sizing is employed, meaning that rise and fall times are approximately equal.

The third term is the leakage power, which is consumed when transistors are in their off state. Retaining the same performance while lowering the supply voltages is done by reducing the treshold voltage (V_t); ensuring the similar current drive. This comes with a penalty in the form of increased leakage currents; increasing static power consumption.

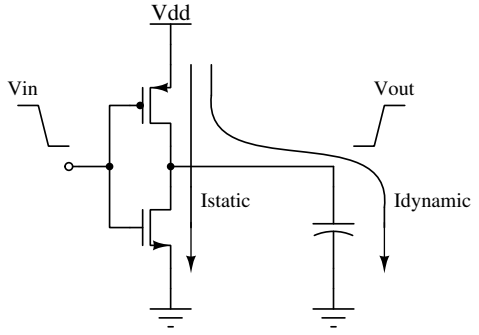

Figure 2.1 Switching power in a conventional inverter.

2.4 CMOS thyristor

A thyristor is a circuit element quite similar to a transistor. In its simplest form it has three nodes: an anode, cathode and gate. What differentiates the thyristor from a transistor is that once a voltage or current has been applied to its input, causing it to conduct, removing this input will not stop it from conducting. Simply put; it is a latch and once it is conducting, the

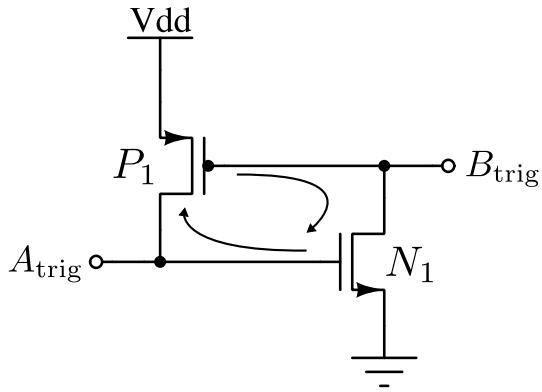

Figure 2.2 The basic concept of a CMOS thyristor [1] .

only way stop it is to remove the supply [15] . Figure 2.2 shows the concept of implementing a thyristor using regular CMOS transistors. The positive feedback effect is illustrated by the arrows.

2.5 Voltage scaling in analog CMOS

Digital circuits have benefited greatly from the continued downscaling of CMOS technology, achieving increased integration density, greater performance and lower power consumption. A downscaling of supply voltage has followed; compensating for the increased thermal power dissipated in these circuits. At the same time, development has shifted from independent integrated circuits over to system on chip type designs. Meaning that analog and digital components frequently need to be integrated on a single die using the same technology. This presents issues for analog design in modern and future ultra deep submicron CMOS processes [2].

Analog performance is closely linked to the power consumption; an increase in performance will need an increase in power. The required signal integrity (SNR or SINAD) puts limits on the lowest possible power consumption in a circuit. This limit is essensially the energy required to keep the signals above that of the thermal noise. [16]. In [17] this requirement is epxressed as the minimum power per pole:

$$P/f = 8kT\left(\frac{V_S}{V_N}\right)^2 [J] \tag{2.5}$$

Here, f is the signal frequency bandwidth, k is the Boltzmann constant, T is the temperature in Kevlin and the last part is the signal to noise ration (SNR). This limit is independent

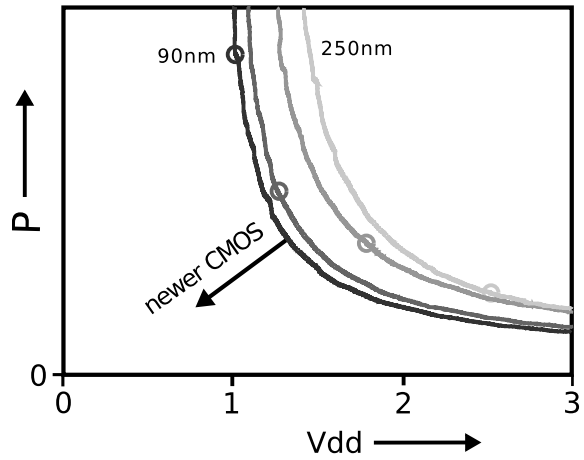

Figure 2.3 Illustration of how voltage scaling affects power consumption over four technology generations. The plot shows the minimum power consumption for an (arbitrary) analog circuit and the circles correspond to the power consumption in a technology at the nominal supply voltage for each CMOS process [2] .

of technology and corresponds to a 10-fold increase in power for each 10dB increase in S/N [16]. The minimum power consumption of digital circuits is given by the number of logic gate transitions m, each using a certain amount of energy E_{tr}. The m transitions are proporsonal to a power of the number of bits N_{bit} and is therefore only weakly dependent on the SNR.

$$P = m \cdot f \cdot E_{tr} + P_{stat} \quad (2.6)$$

The general trend is that moving to a new technology causes a drop in performance; given the same power budget [2] . For an analog design, a decrease in supply voltage, leads to and increase in the minimum power consumption. If the supply voltage can be held constant; moving to a new technology reduces power consumption.

2.6 Fully Depleted Silicon-on-Insulator (FD-SOI)

SOI processes are considered more suitable for ultra low power applications compared to the conventional bulk CMOS processes; enabling higher density integration, speed and reduced power consumption. Figure 2.4 shows the general build-up of a FD-SOI type transistor. The use of an insulator below a thin layer of silicon eliminates a large portion of the capacitances found in bulk CMOS [18].

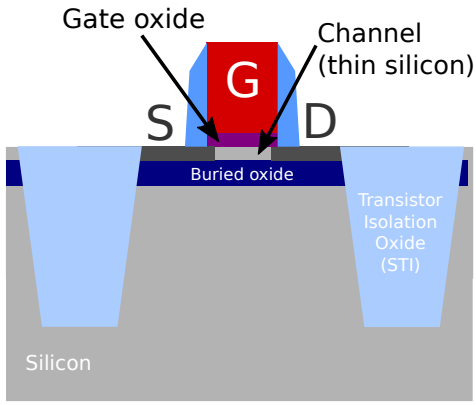

Figure 2.4 Planar FD-SOI transistor [3]

As technology scales down, the variations in V_{th} become increasingly significant and difficult to negate. The shorter gate lengths also lead to an increase in short channel effects (SCE). Such an effect is the drain-induced barrier lowering (DIBL); resulting in a higher number of charge carriers injected into the channel from the source. This increases the drain off-current (I_D) and reduces the gate voltages ability to control drain current[19] [20] . These are challenges facing conventional bulk MOS-FET processes in the sub 100nm era.

The fully depleted silicon-on-insulator (FD-SOI) process has less V_{th} variation compared to bulk MOS-FET; while also having, reduced soft-error-rates, pn-junction leakage, node capacitance and reduction in SCE . The latter has been linked to some interesting dynamics where SCE unique to SOI interact with effects such as DIBL resulting in some performance improvements [19] . The influence on threshold voltage through the body effect is significantly reduced in SOI; providing higher possible swing and gain [21] . A recent advancement in FD-SOI is the use of Silicon on Thin BOX. A very thin buried oxide (BOX) layer, only 10nm thick, enabling easy voltage adjustment of the back gate; similar to the substrate bias in bulk-MOS device [20] [22] [23] .

2.7 Transistor current drive in ultra low power

The typical tuning parameters are the same in sub-threshold as they are in above threshold, but the relationships between them are quite different. As the effective voltage (V_{eff}) becomes negative, the transistor enters the sub-threshold region. Its drain current can then be approximated using the following relationship [6] :

$$I_{D(sub\text{-}th)} \cong I_{D0} \left(\frac{W}{L} \right) e^{(qV_{eff}/nkT)} \tag{2.7}$$

In sub-threshold, the linear relationship W/L has a direct influence on the V_{th} of the transistor [24]. This means that W/L sizing does not have the same effect as in above threshold. The sizing of W for example; has a smaller effect on the transistor driving power due to the reverse narrow channel effect (RNCE).

A given technology will usually provide transistors with either low or high threshold voltage (V_t) . This is a more efficient way to increase current drive than scaling the transistor due to the exponential relationship shown in Equation(2.7). Going from a high V_t transistor to a low V_t transistor can increase current drive about 18 times [24]. Body biasing also has a similar this relationship and can further be used to increase current drive of a transistor. The available tuning parameters in the order of effectiveness in sub-threshold:

- using low V_t/high V_t transistors,
- bulk voltage tuning,
- tuning the aspect ratio W/L.

2.8 Gated Clock Routing

A digital power reduction method that gained attention at the end of 20th century was the use of clocked gating[2]. The method uses the fact that in a typical digital system; such as a microprocessor; only some parts of the system are active at any given time. An un-gated system might experience redundant switching in some nodes, leading to uneccessary power consumption [4] . As can be seen in Figure 2.5, clocked gating isolates internal module nodes from the a clock line using buffers. These are enabled and disabled based on the system state. Since the combinatorial logic inputs are kepts static in the idle state, less dynamic power is consumed.

2.9 Sampling switch

At higher voltage and oxide thickness, boosting the input voltage to $2V_{DD}$ provides a way to increase current drive of a transistor. This is done using what is commonly called a charge-pump or clock boosting; combining the sampled voltage of two capacitors and adding them together to make a higher voltage. But as technology scales, this method becomes less attractive; applying large voltages at the gate of a modern transistor is less reliable than before; and can cause permanent gate oxide breakdown [26] .

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[2] It was extensivly used in the design of the Intel Pentium IV processor [25] .

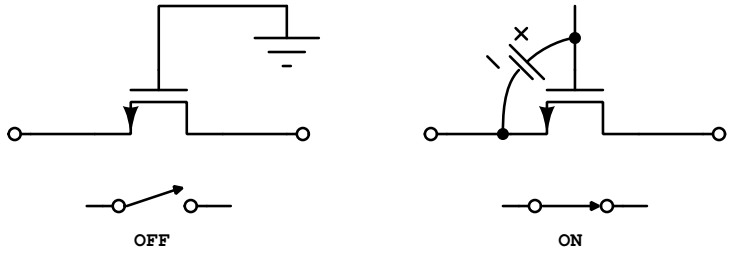

Figure 2.6 Basic function of a bootstrapped switch

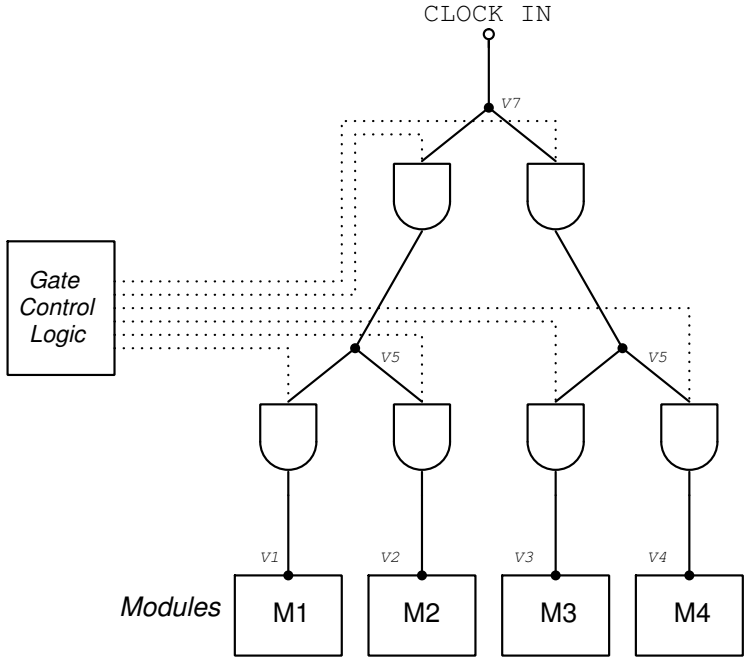

Figure 2.5 Gated clock tree [4]

Bootstrapped circuits approach the problem from another angle and in stead provide a constant voltage at the gate, independent of the input voltage. The basic function is illustrated in Figure 2.6. This improves linearity significantly compared to CMOS gates and clock boosting, in which the gate voltage varies quite a lot.

In order to use the bootstrapped method, each individual switch needs dedicated bootstrapped circuitry. The bootstrapped method generates a voltage $V_{in} + V_{dd}$. During the

OFF state, the supply voltage is "sampled" onto a capacitor and the transistor gate is connected to ground. In the ON state, the capacitor is connected between the gate and source of the transistor.

2.10 Transistor leakage in sub-treshold

Gate oxide thickness is reduced in each technology generation in order to mantain current drive and to counter the effect of SCE . This has lead to a significant increase in the gate leakage of modern transistors. The infinite impedance that most designer associate with the gate of a transistor is no longer a valid assumption. Oxide tunneling and injection of hot carrier from substrate to the gate oxide contribute significantly to the power consumption in modern circuits [27] . [28] presents a simplified equation for gate-oxide leakage:

$$I_{ox} = K_2 W \left(\frac{V}{t_{ox}}\right)^2 e^{-\alpha t_{ox}/V} \tag{2.8}$$

K_2 and α are experimental values and t_{ox} is the oxide thickness. As can be seen from the formula, increasing oxide thickness reduces the gate leakage. This is generally not an option in short channel transistors as they will se an increase in SCE .

In order to ensure that the SCE does not become a problem, sufficient aspect ratio is required. In a MOSTFET, this ratio can be described using the following relation:

$$AR = \frac{L}{\left[t_{ox}\left(\frac{\epsilon_{si}}{\epsilon_{ox}}\right)\right]^{1/3} W_{\mathrm{dm}}^{1/3} X_j^{1/3}} \tag{2.9}$$

Where ϵ_{si} and ϵ_{ox} are silicon and oxide permittivities. L is the channel length, t_{ox} is the oxide thickness, W_{dm} is the depletion depth, and X_j is the junction depth [27] .

2.11 Placement using Weinberger image

Routing considerations in a complex digital system must be considered early on in a design. It is usually a balance between high freedom in placing transistors or high density. One way; that gives a lot of freedom; is to place transistors rows in parallell and to allocate space between them for the wiring. This of course leads to very low logic density [5] .

A method that results in high density, is one where the supply and ground rails are alternated and shared with cells above and below. The transistor cells are also alternated; inverterd based on their placement. The layout results in whats called a Weinberger image. Figure 2.7 illustrates the difference between the two approaches.

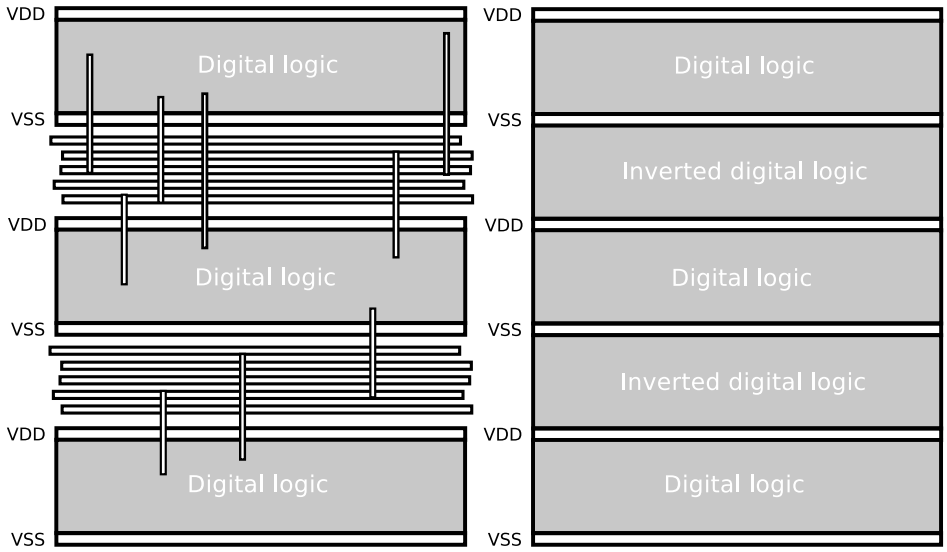

Figure 2.7 Different transistor row placement techniques. High freedom placement to the left and high density placement on the right [5] .

2.12 Successive Approximation Register

A successive approximation register (SAR) is a simple kind of ADC that has a low power consumption and at the same time, many applications. These Nyquist-rate ADC types usually range from low frequency to moderately high frequency sampling, with high to medium resolution. They are considered simple because of the fact that a SAR can be realised using only a comparator, capacitor bank with switches and a small amount of digital control logic.

The input value is found using a binary search algorithm. Digital words close to the input value is found iteratively. In each cycle of the algorithm, a simple comparison provides a binary yes or no answer, which in turn halves the possible values the input can have. The general SAR implementation is shown in Figure 2.8, where the value is found by comparing known values with the sampled input value. In the illustration, a DAC is used to provide the known values after they are calculated by the digital logic.

Instead of using a dedicated DAC , the typical approach today, which has become almost synonomous with SAR ADC circuits, is the charge-redistribution capacitor array. The sample and hold, DAC and value generation is combined into a single circuit as shown in Figure 2.9. Input values are sampled onto the capacitor array and based on the initial state of the capacitor switches and their consequtive switching, different search algorithms can be implemented. Capacitor topology can also be changed in order to perform different kinds

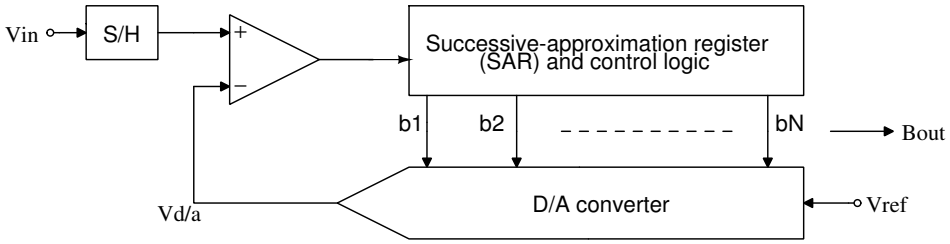

Figure 2.8 D/A converter-based successive-approximation converter [6] .

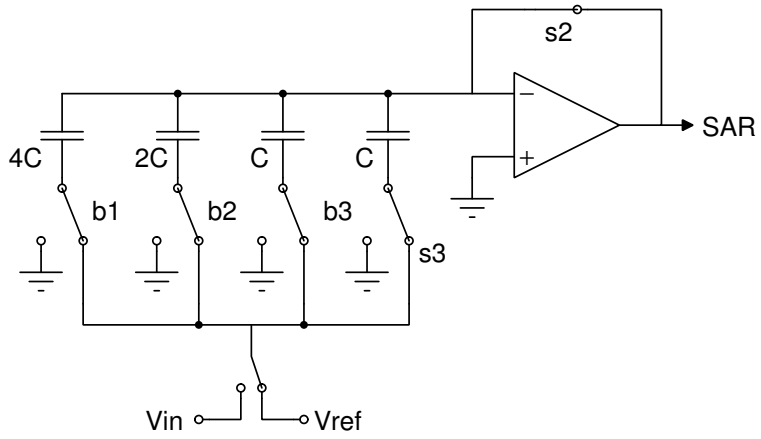

Figure 2.9 Charge-Redistribution A/D in a sampling phase [6] .

of searches or to meet requirements to power consumption, area etc. Several algorithms will be covered later in this thesis.

2.13 Comparator

Comparators compare two signals levels against each other and then generate a digital value that indicates which one has the greatest or smallest amplitude. They are some of the most widely used electronic components, only surpassed by amplifiers. Most ADC types are based on comparators, but they also have uses in other applications, such as data transmission and switching regulators.

Though there are many types of comparators, this thesis will only cover the theory for track and latch types, as these are the most prevalent in ultra low power design.

A popular dynamic track and latch comparator is shown in Figure 2.10 . The circuits dynamic property means that it can enter a "sleep" mode where it consumes very little power.

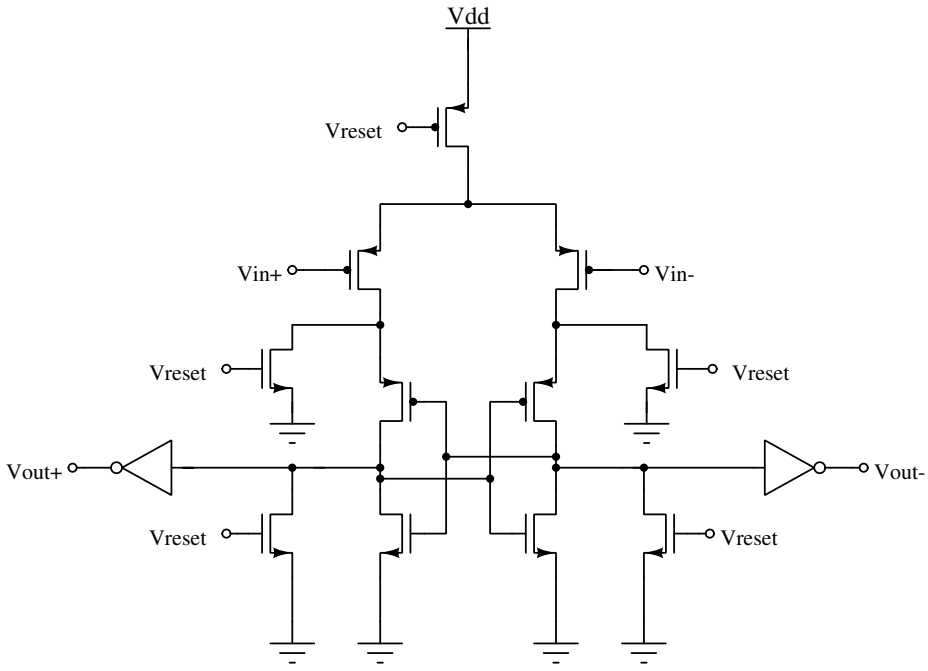

Figure 2.10 The popular StrongARM dynamic track and latch comparator.

The circuit consists of differential input transistors and track and latch stage consisting of two back to back inverters and several reset switches. The difference between the inputs is amplified during the track stage and then amplified again during the latch phase due to the positive feedbak taking over. This regenerates the analog value into a full scale digital value.

If high-speed is required, a pre-amplifier will usually be used in front of the comparator. The typical amplification is usually limited by a factor of 2 to 10 times. This improves several performance characteristics like noise and speed, and also significantly reduces some non-ideal effects like kickback, which in turn increases the resolution of the comparator.

This circuit uses a dynamic comparator without a pre-amplifier. Most low power designs ommit the pre-amplifier in order to reduce power consumption. Pre-amplifiers improve comparator performance, but due to their static power consumption, are not well suited for ultra low power design. A dynamic comparator only consumes dynamic power during conversion, allowing it to "sleep" in order to reduce power.

2.13.1 Kickback effect

Coupling through the parasitic capacitances of the input transistors of a comparator due to voltage variations in the regenerative nodes is known as kickback noise. This effect is especially prevalent in dynamic comparators. Known to be fast and power efficient, these types generally have more internal voltage variation than other types. Some will have regenerative nodes that transition from rail to rail; meaning the input transistors can enter both saturation and triode-operation during a single conversion, resulting in a second source of the kickback effect.

2.13.2 Latch offset

Random and systematic mismatch introduces an input offset voltage in dynamic latches that can be significant, sometimes in the order of $10mV$. When the two half circuits of a latch don't conduct the same current or the loads of the differential outputs are different, an offset will be present. The output will introduce a difference between the latch time constants.

2.13.3 Hysteresis

Hysteresis refers to a charge stored on internal capacitances in a comparator that create a "memory" effect. Most topologies have input tresholds that are dependent on previous values. This effect is often a non-ideality that should be minimized, but it can also be beneficial in some applications.

2.13.4 Metastability

Sometimes the difference between the two signals is too small for to the comparator, so it takes too long to regenerate the signal, and it is not able to do this in the given time period.

Chapter 3

The state of ultra low power

3.1 State-of-the-art

[7] is a compilation of ADC papers published in international Solid-State Circuits Conference (ISSCC) and Symposia on VLSI Technology and Circuits (VLSI). [10] presented ADC statistics from these papers in the form of two graphs; showing the nyquist sample rate against the power consumption and FOM respectivly. This thesis presents an updated version of these graphs in Figure 3.1 and Figure 3.2. A breif look at the graphs show that little has changed in the last two years, and SAR ADC architectures still dominate in the published ultra-low power designs.

In the provious work [10] , [29] was cited as the most energy efficient ADC the author could find. Having a power consumption of 3nW and a 10-bit resolution using 65nm technology. Other papers have been published in the two years since that paper, but none have gone below the 3nW power consumption found in [29]. The most interesting performance gain was found in [30]. This is a SAR ADC that achieves a 0.85fJ/conversion-step, 10-bit resolution and 200kS/s in 40nm CMOS. This is similar to the expected efficiency of this project, but at a much higher power consumption of 84nW.

3.2 General trends in low power design

In order to give the reader an understanding of the current trends in ADC design, brief summary based on [31] is presented in this section.

ADC designs have become incredibly efficient over the last decade. This improvement can be attributed to technology scaling and the trend of using simplified analog sub-circuits with digital correction. Performance improvements have taken a backseat as the power consumption of ADCs have halved every 2 years. As a consequence, circuits published today, could have similar performance as ADCs published ten years ago.

Modern designs try to deal with the constantly falling voltage headroom that accompanies newer technologies. As the voltage falls; circuit noise must also be reduced in order to attain the same SNR . This trend has made lower resultion designs more attractive, as it is the high resolution designs that eventually get limited by noise. Power efficiency is also achived by avoiding high frequency operation. Pushing a circuit in a given technology to

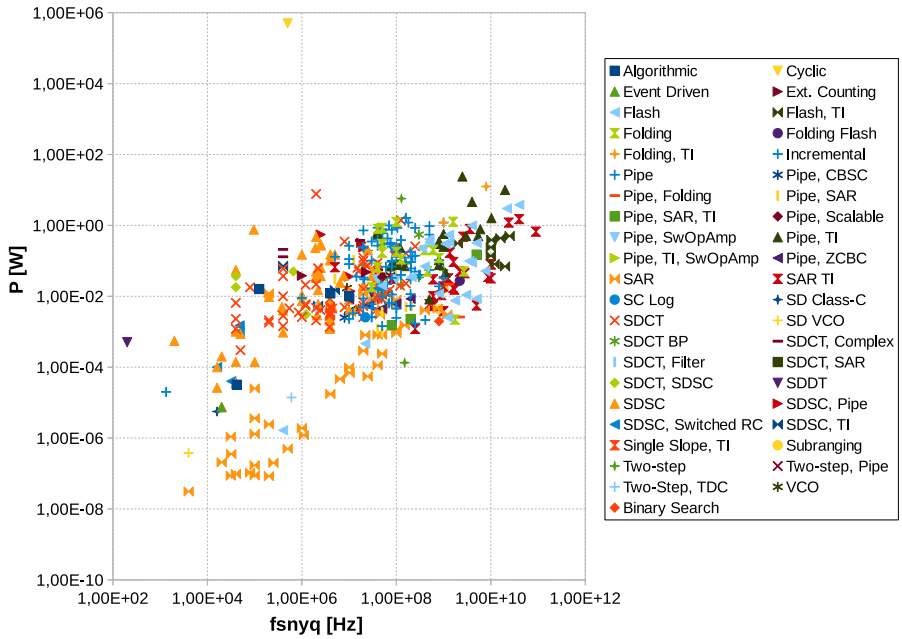

Figure 3.1 The power consumption of different types of ADC architectures published in [7] compared against the nyquist sampling frequency.

run at the maximum possible speed makes it likely that it will be less efficient and not benefit from the power improvements associated with scaling.

Innefficient components, such as op-amps, are replaced by much simpler, efficient and less noisy designs. SAR ADCs have become incredibly popular in ultra-low power and fitt nicely into the performance space of low power.

SAR ADCs are moving into the digital realm. Traditionally, the digital filtering in ADCs have been used in high resoultion sigma-delta converter, but now there is an increasing interest in using oversampling in regular Nyquist rate converters. Digital power consumption is less dependent on the SNR than analog power consumption and could boost efficiency as SAR ADCs approach the limits of analog efficiency.

New technologies allow aggresive downsizing of circuit components; as the transistor matching is usually improved. Increasingly common is the use of digital mismatch correction, compensating for enabling further downsizing.

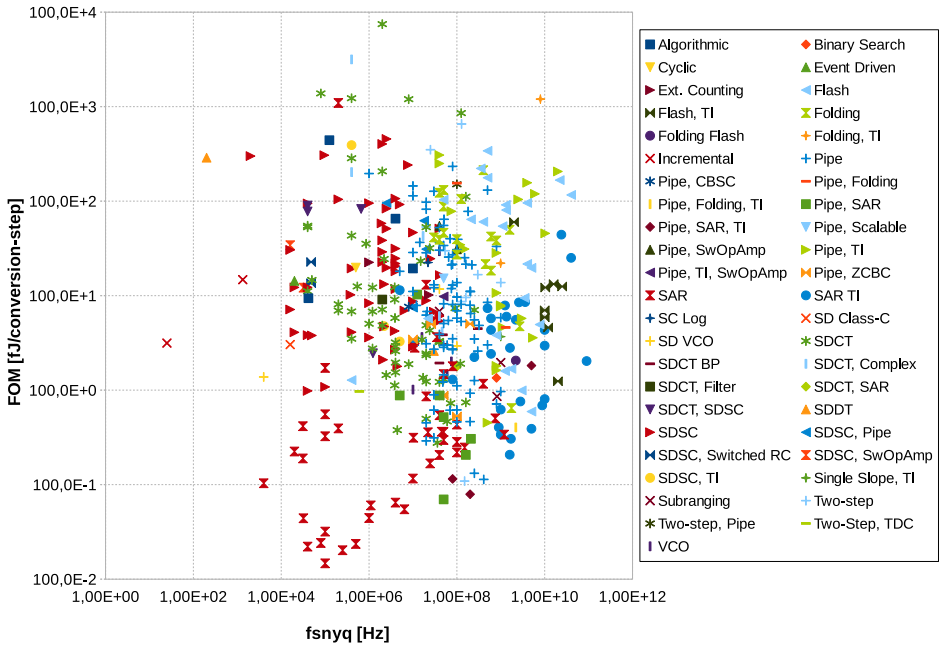

Figure 3.2 A plot of FOM against the nyquist frequency for the different SAR architectures published in [7].

3.3 Successive approximation algorithms

The following section presents the relevant switching procedures. The procedures are described in [10] with a thorough comparison of their power consumption. Such an evaluation will not be presented in this thesis, but a short summary of their properties is given below.

3.3.1 Monotonic switching procedure

Ever since its presentation in [32] , the monotonic switching procedure has been popular. Compared to the conventional, it provides significant power savings, minimal control circuitry, a 50% reduction in the capacitor array and faster settling speed. It was used in the previous work [10] where it provided near optimal power consumption; deviating only slightly from the theory, due to lekage currents in the capacitor array. It was somewhat unique since it only switches a single capacitor for each bit and always in the same direction. This means that the common mode voltage is always decreasing or increasing based on the configuration.

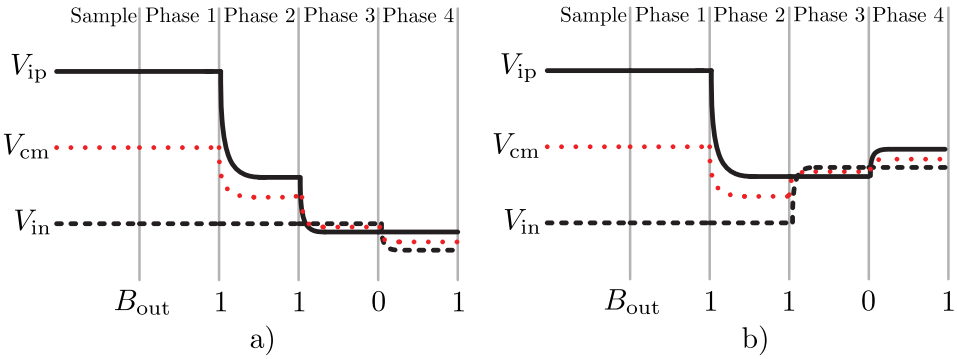

Figure 3.3 Illustration of the common mode variation in monotonic (a) and switchback (b) [8].

3.3.2 Switchback procedure

The switchback procedure builds on the monotonic procedure; using the same number of switches and reference voltages and by only switching a single capacitor each bit cycle. The first two conversions are the same as well; the first is sampled directly without switching, and the second results in a downward transition of the common mode voltage. The difference is that further switching results in an upward transition of the common mode voltage, as shown in Figure 3.3. This limits the common-mode voltage to a minimum of $1/4V_{ref}$ and means that the common-mode voltage moves towards the common-mode voltage of the input signal [8]. Benefits from this procedure is that dynamic offset and parasitic capacitance variation is reduced in the comparator.

Accounting for sampling and conversion, the switchback procedure can consumes more power than the monotonic procedure, but avoids adding extra references.

3.3.3 Merged capacitor switching

A method that provides even better efficiency than both the afforementioned procedures is the merged capacitor switching [33] [34] . It can provide higher accuracy and switching speed compared to the monotonic procedure, as well as increased margins on mismatch and process variations. A doubling of the unit capacitor is possible due to the decrease in power consumption.

Compared to the monotonic and switchback procedure, the merged capacitor switching requires an external common mode reference and more digital driving circuitry in order to be implemented. It is also reliant on transmission gates in order to connect the bottom plate of the capacitors to the common mode voltage during sampling.

Chapter 4

System design and methodology

This chapter starts with the top-level operation operation of the ADC . The system itself can be divided into three parts: the DAC consisting of the capacitor array and sampling switch, the digital control circuits and the comparator. The division is highlighted in figure Figure 4.1.

4.1 System overview

An overview of the ADC is presented in Figure 4.1, showing the system divided into three parts: the comparator, digital control logic and the capacitor array with sampling switches. This separation will be used throughout this thesis.

The ADC is asynchronous and requires an external clock that runs at the sampling frequency in order to operate. A high external clock signal puts the circuit into reset. Though it is not shown in Figure 4.1, any component that needs external reset is connected to the external clock. The design has been done with a 50% clock duty cycle in mind.

Sampling of the input signals V_{in+} and V_{in-} begins at the negative transition of the clock. The *sampling logic* (SL) block will then provide a sample signal to the sampling switches, while simultaneously providing a busy signal to the *clock feedback control* (CFC) block. The busy signal is also enabled during reset. When the ADC is finished sampling, the busy signal is released and the CFC-block enables the comparator. From this point on, the comparator compares the values of the top plate of the capacitor arrays and provides a trigger for the internal clock generation.

The comparator has equal outputs during reset and unequal outputs after it has arrived at a decision. The *internal clock generation* (ICG) block uses the state of the comparator outputs to generate an internal clock. This clock is used to drive the *SAR control logic* (SCL) block and is fed back to the comparator through the CFC-block. If the busy signal from the SL-block is high, the CFC-block will hold the comparator in reset.

As the name suggests, the SCL-block implements the successive approximation algorithm. It holds the system state, stores the comparator results and provides the necessary switching signals for the capacitor array.

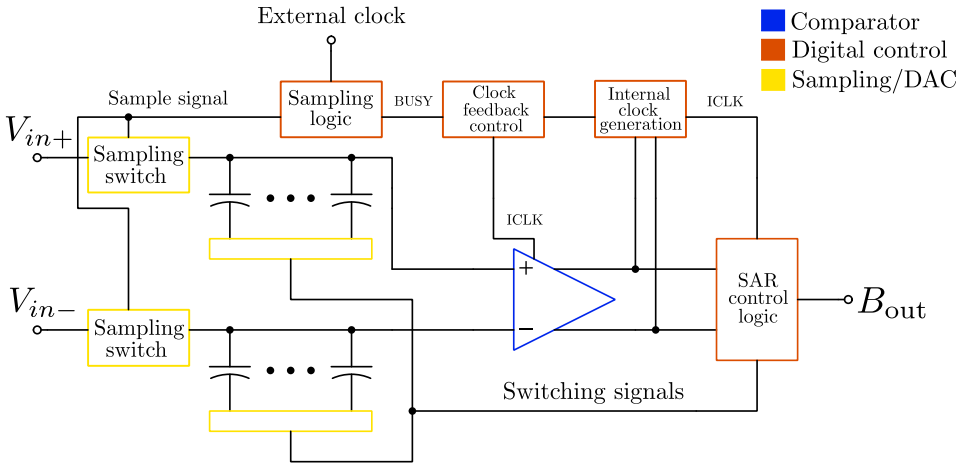

Figure 4.1 Abstract overview schematic of the ADC. Component colors correspond to the system division used in this thesis.

4.2 Design strategy

The introductory part of this project was to confirm the validity of previous work and then to improve upon it. The 28 nm FD-SOI technology used in this project is not a new generation, but a radically different technology compared to the 65 nm bulk-CMOS process. But as mentioned in Section 2.6, recent advances have made the two technologies more similar and they do provide similar components. For example; High and low V_t transistors are available in both technologies as well as bulk/substrate contacts. The starting point of this project was a direct translation of the previous design from the old technology to the new.

4.2.1 Framework

Improvements were made within the framework of the previous design; meaning that design decisions such as the type of comparator, DAC and control logic is already established. No fundamental change should be made unless the design is somehow incompatible with the current technology, or performs worse than it did in previous work. After completion of this task, further improvements were made.

4.2.2 Ideal system models

As mentioned above, the system is divided into three logical parts; the DAC , the comparator and the digital control logic. Building ideal versions of these parts using the *veriloga*

language has been a design strategy from the start. Ideal components represent the functionality of the circuit, but have none of the nonidealities. This is beneficial when trying to identify problems that arise due to the interconnection of system parts. Another reason for using this approach is the vastly reduced simulation times. The *veriloga* code is presented in appendix A.

4.2.3 External circuitry

This project aims to make an ultra low power ADC , and external driving circuitry was considered a part of that effort. Several techniques that reduce the ADC power consumption, increase the power consumption of the external driving circuits. For example; using multiple voltage references for the digital and analog parts can decrease digital power consumption, but adding another voltage reference could from a top level perspective consume more power than the entire ADC ; the same can be said for designs that require a common mode reference. As such, it was preferred to avoid using these techniques, unless necessary.

4.3 Digital transistor sizing

Static leakage is a component that becomes a more significant part of power consumption in low-power designs and a good understanding of how much leakage can be expected from different transistor types is useful. Figure 4.2 presents the leakage current for all the different transistor types available in the current technology given different values of V_{DS}. The dimensions are not the same as in a similar graph presented [10], so a direct comparison is not valid, but it is observed that the leakage varies less between the different transistor types compared to the previous technology.

Since operating frequency of the ADC is relatively low; regular V_t type transistor should be used where possible, as they have the lowest static current. The smallest possible transistor width should also be used in order to reduce gate capacitance and dynamic power consumption in the digital circuits. If the designer want to follow the recommended layout rules, this means a minimum transistor width of 180 nm.

Another graph is presented in Figure 4.3 shows the leakage currents for the regular V_t nfet and pfet type transistors for different channel lengths. Looking at the pfet, it is clear that channel lengths longer than 60 nm does not significantly reduce leakage. The nfet type needs lengths up to >100 nm before the reduction in leakage currents subsides. This provides an indication on the largest transistor dimensions that are reasonable in order to optimize static power consumption in the digital part of the system.

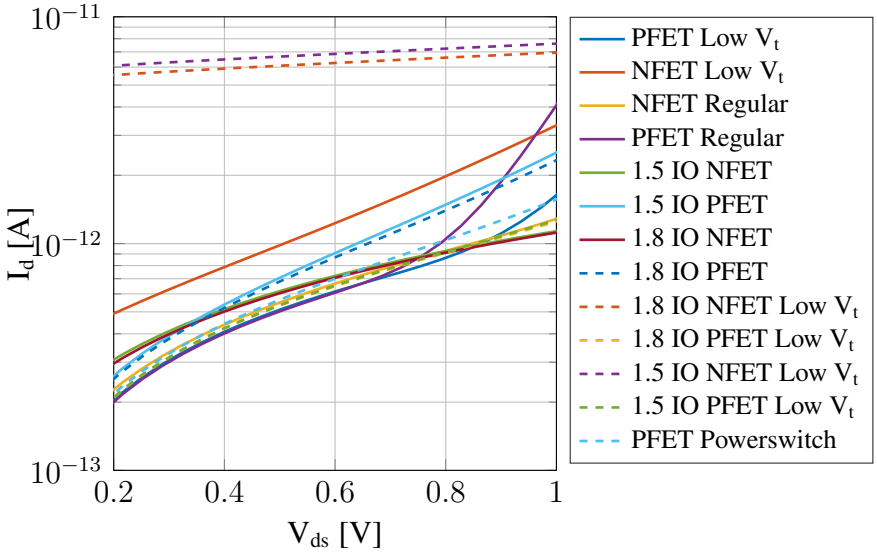

Figure 4.2 The leakage currents for all transistors in the current technology. Transistors gate voltages are set to the OFF state and current is measured through the drain. All transistors have the same dimensions based on the largest default value.

4.4 Clocking scheme

The ADC is driven asynchronously, with the comparator used as the source of the internal clock. This lessens the requirements on the external clock; which can run at the sampling rate. An asynchronous architecture provides several benefits over a synchronous one. One is that it avoids the critical path problem, where fast parts of a circuit idle for longer than necessary. It allows dynamic adjustment of the sampling frequency with a one to one relation to the external clock. Top level power should also be reduced since the external clock runs slower. The running time of the circuit can be increased by adjusting the duty cycle of the clock, leaving more time to do the conversion. Though; latter would have a negative effect on the power consumption; as it would increase complexity.

Asynchronous clocking makes it more applicable in large VLSI type designs where clocking requirements and distribution are a large part of the design effort.

The major drawbacks is that the handling of multiple signal becomes more difficult, due to so called race conditions. There are two signal paths in the ADC design that must propagate with correct timing constraints; as shown in Figure 4.4. The internal clock signal

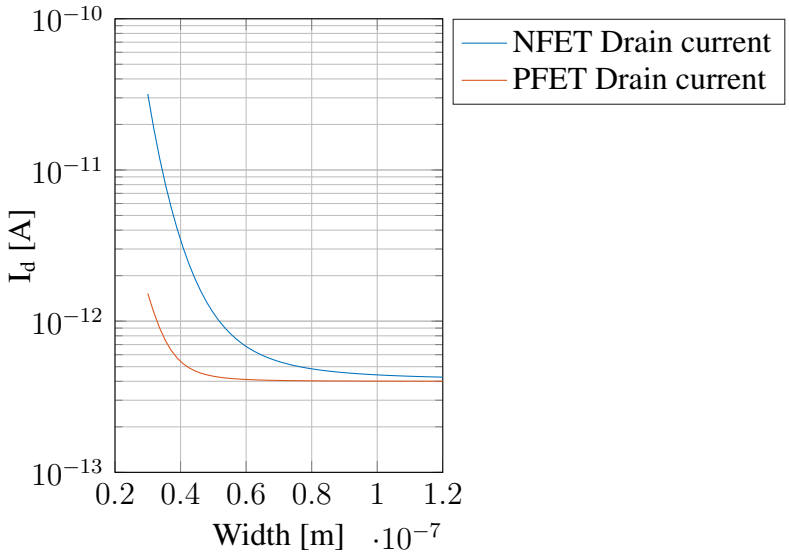

Figure 4.3 Adjusting the length of regular V_t pfet and nfet transistors at a constant supply of 0.4V and a width of 80nm. The graph shows the resulting static current.

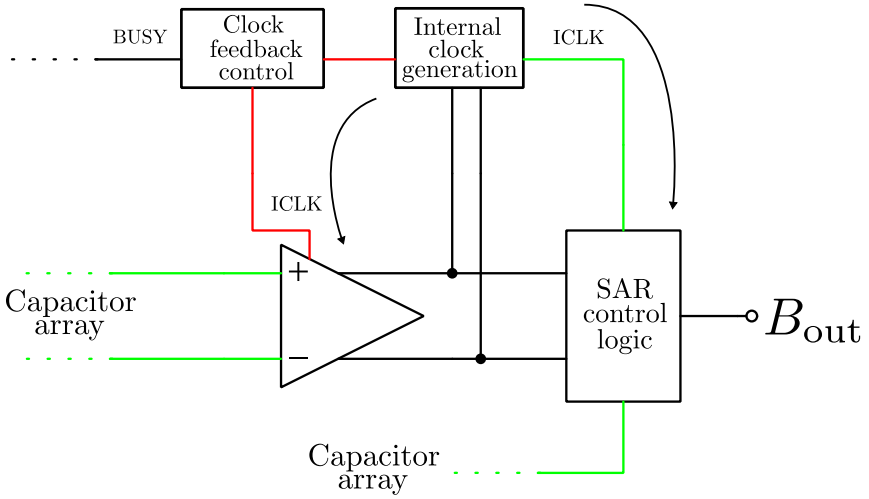

Figure 4.4 Paths in the system that could case a race condition. Green must propagate before red.

must not initiate the comparator before the capacitor array has settled to a new value. A synchronous circuit could use buffers to ensure proper timing; but this is not possible in asynchronous circuits. Control logic could be used to check if signals have settled, but they would exponentially increase circuit complexity and power consumption. The only way to ensure proper timing is through a more extensive design effort.

4.5 Sampling signal generation

Asynchronous generation of the sampling signal, as shown in Figure 4.5, is used in order to reduce the bootstrap circuits sampling capacitance. In [10], the sampling time corresponds to a single period of the clock; this could be done in this design as well by enabling sampling when the ADC is in reset. However; the bootstrap circuit would then have to store enough charge to drive the sampling transistor for half the external clock cycle. Since the bootstrapped sampling switch enables sampling of the ADC inputs in a much shorter time, this becomes wasteful. With the decrease in voltage and technology scaling, keeping a charge for a long period is becoming increasingly difficult.

As shown in Figure 4.6; the sampling is triggered by the external clock (CLK) going low. The low signal starts the sampling, but also propagates through a delay element, keeping the low signal from reaching both inputs of the XOR gate at once. This results in a logic high on the XOR output. The NAND gate ensures that SAMPLE only goes high on the negative edge of the external clock. Once the delayed clock signal (DCLK) reaches the gate, the sampling stops and the $\overline{\text{BUSY}}$ signal is released. The entire sampling procedure is triggered by a single transition of the external clock.

4.6 Delay element

The conventional delay element is a string of current starved inverters, sometimes loaded with capacitors (RC-element). These are known provide a predictable delay that scales with corners and are simple to implement. Buffer delays where used at the start of the

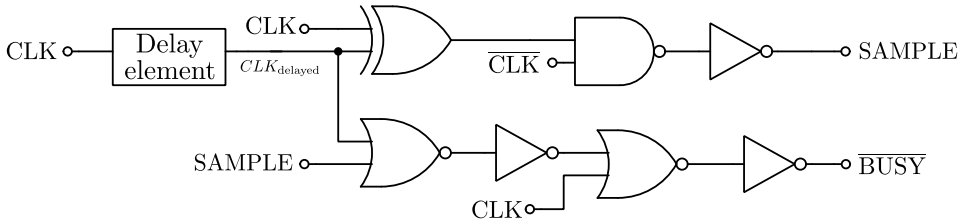

Figure 4.5 The sample logic block (SL) that is used to generates the SAMPLE and BUSY signal in the ADC .

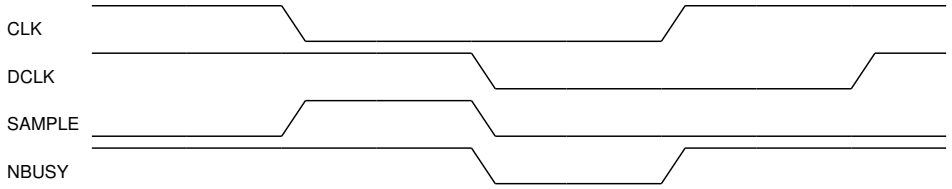

Figure 4.6 Timing diagram for the sampling logic block shown in Figure 4.5.

project, but where replaced by a different delay element later on due to a need for frequent changes in supply voltage.

[35] proposes a mathematical model for sub-threshold operation and subsequent formulas for calculating the delays of an inverter in sub-threshold. These formulas suggest that the buffer delays become exponentially inversely dependent on the supply voltage in sub-threshold. This seems to corresponds to the behaviour observed during the design process and might suggests that inverter buffers see less scalability and reliability in ultra-low power designs; becoming more sensitive to voltage variations.

A study of delay elements for use in CMOS VLIS design is found in [36] . Guidelines are presented for each delay element in regards to their applications. Two element types stand out by having much larger delay range than others: transmission gate with Schmitt trigger and thyristor based delays. The Schmitt triggered transmission gate is cited as having the worst power consumption of all types, while the thyristor based delay is comparable to most of the other delays. A low-voltage thyristor based delay element found in [1] is shown in Figure 4.7. Its delay can be estimated by the following equation:

$$t_d = \frac{C_1 V_{T1}}{I_{\text{ctrl}}} + \sqrt[3]{\frac{6C_2C_1^2}{K_1 I_{\text{ctrl}}^2} V_{T2}} + \delta t \tag{4.1}$$

Subscripts 1 and 2 are for the driving transistor and the driven transistor respectively. I_{ctrl} is the current flowing through the current source and δt is the regeneration time between transitions [1].

The circuit uses the positive feedback of two thyristors in order to generate quick logic transition. There is one thyristor for each of the two possible transitions, up and down. A current source (I_{ctrl}) is used to limit current sink on the thyristor nodes, essentially controlling the delay. The less current the current source conducts, the larger the delay (t_d) becomes. Equation(4.1) shows that the thyristor delay is only mildly dependent on the supply voltage through δt; as higher voltage leads to faster regeneration. This dependency is lessened with a reduction in the value of I_{ctrl}.

Using a current mirror, or similar, to generate I_{ctrl} is avoided due to the static power consumed by these types of circuits. Since the delay precision requirements are quite relaxed,

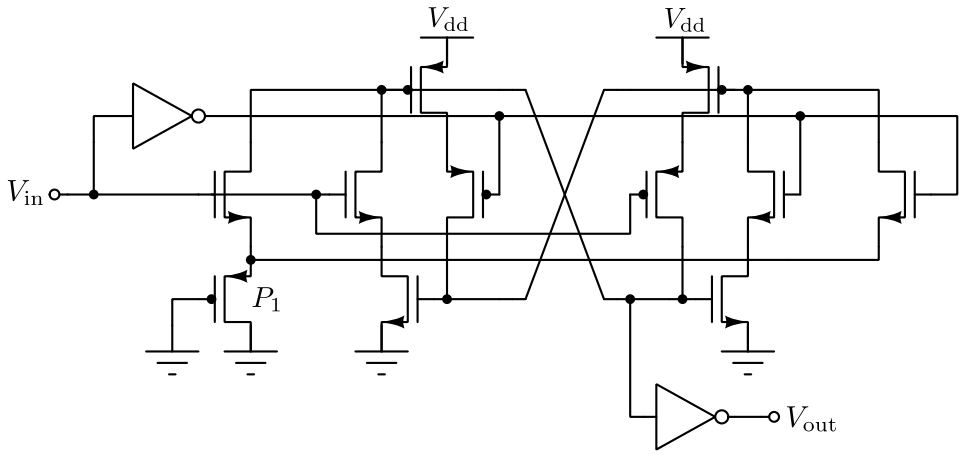

Figure 4.7 Statically triggered thyristor based delay element from [1].

this current source is simply implemented using a single pfet (P_1 in Figure 4.7)[3] .The transistor has its gate connected to ground and is dimensioned with a long channel length.

4.7 Bootstrapped sampling switch

The bootstrap circuits for the sampling switches is as shown in Figure 4.8, where V_{in} is the external signal being sampled and V_{out} is the node connected to the capacitor array and V_{sample} is the sample signal generated in the SL-block shown in Figure 4.1. Here is a brief explanation of the circuit:

A low V_{sample} turns the sampling switch off. In this state the sampling capacitor (C_{b}) is charged by the current passing through M_{P2} and M_{N1} until it reaches the supply voltage (V_{DD}). M_{P1} is off and isolates V_{b} from the voltage over C_{b}. At the same time, M_{N5} and M_{N6} pull V_b to ground. If V_{sample} goes high; M_{N1} turns off and M_{P1} turns on. The aftereffect is that M_{P2} turns off due to an increasing V_{b}; effectivly isolating C_{b} from supply and ground. C_b top-plate is connected to the gates of the sampling switch transistors through M_{P1} and the bottom plate is connected to the source of M_{N2} through M_{N7}. The voltage sampled on C_{b} should generate a voltage close to (V_{in} + V_{DD}) at V_{b}.

The bootstrap circuit used in [10] is the same as in [37]. Both designs were made in a bulk CMOS process (28 nm CMOS and 65 nm CMOS respectively). Distortions due to the body effect of the sampling transistor became a problem in [37], and a bulk switching

[3] An nfet type transistor in its OFF state could also be used, using its leakage currents to create and even longer delay.

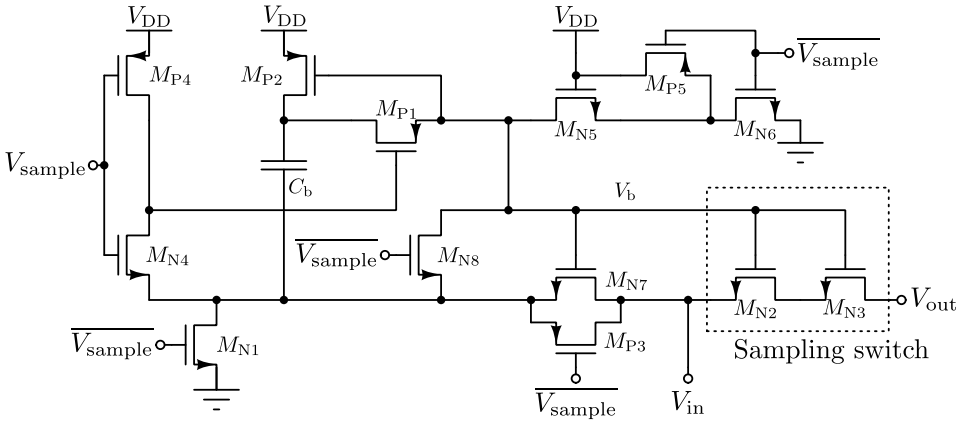

Figure 4.8 The boostrapped nfet-type switch used in the ADC design.

technique was used to solve the problem; [10] used the same technique. Most likely due to the reduced body effect in the FD-SOI process; such a problem was not observed and consequently there was no need for the additional circuitry.

Another noteworthy change is the absence of any triple-well type bulk connections, as they were also not required to attain sufficient performance. The motivation behind their omission was to remove problems encountered in layout.

A recent published paper [38] proposes several improvements on the traditional bootstrap design. It cites lower voltage operation, higher speed and higher linearity than the original. The transistors M_{P5}, M_{N8} and M_{P3} in Figure 4.8 are added based on the suggestions in this paper. Reduced sampling switch gate capacitance is attained with M_{P5}, which pulls the source of M_{N5} to V_{DD} during a high value of V_{sample}. This turns it off, and as a result, a reduction in leakage and capacitance is seen from the V_b node. The transistors M_{N8} and M_{P3} increase the speed of the "turn-on, turn-off" transition.

4.8 Comparator

The comparator used in [10] is the popluar "strongARM" comparator. It is the same shown in Figure 2.10. This comparator is popular because of its low power and high conversion speed. Noise analysis in the previous work revealed that the comparator had the most negative impact on overall system performance. Large load capacitors where used to reduce noise, resulting in power consumption 10 times that of the original design.

Noise reduction in the new design is achieved in several ways. The first is the use of relatively large transistor dimensions that reduces the noise generated in the comparator

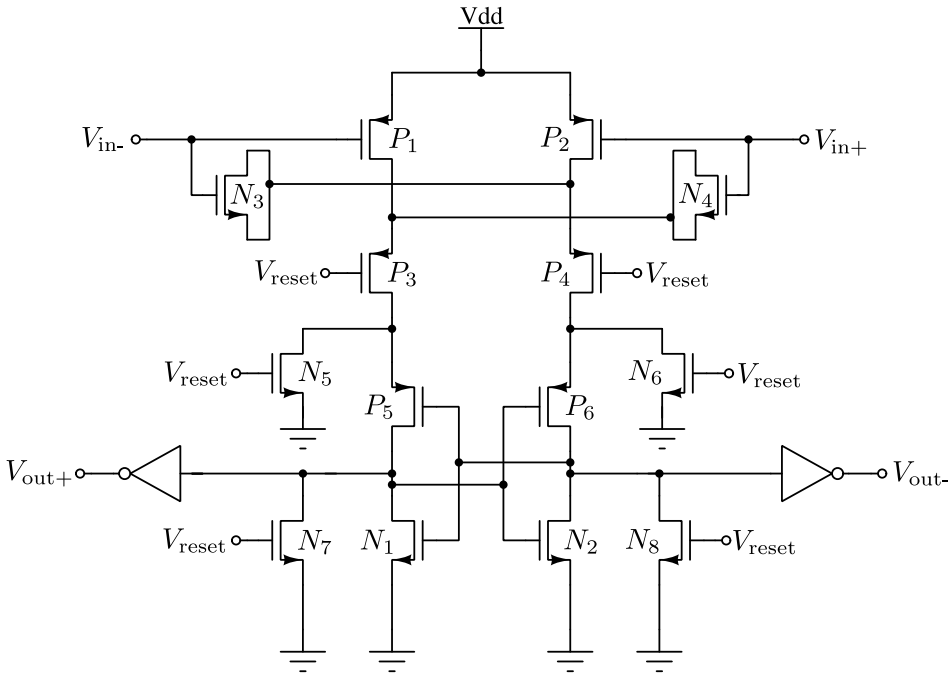

Figure 4.9 The dynamic latched comparator used in the ADC .

itself. The second is by increasing the gain in the comparator. Transistor dimensions ensure high values of g_m and by chosing a new switching procedure (switchback), the V_{eff} is kept much smaller than in the previous procedure (monotonic), ensuring higher intrinsic gain in the input transistors. A small increase in the supply voltage, from 0.4 V to 0.45 V, improves noise margins and speed. Like the previous design, this also uses load capacitors in order to reduce noise, but these are now 17 fF instead of 99 fF.

Increasing the resolution by one bit requires the use of twice as many unit capacitors in the DAC array. Reducing the unit capacitance in half (or more) would ensure that the power dissipated in the DAC stays the same. This reduction puts more stringent demands on the comparators isolation from its inputs. Kickback effects change the amount of charge stored on the capacitors during conversions; as the unit size is reduced, the resulting voltage change increases. [39] presents a dynamic comparator with a reduced kickback effect; claiming an effect 23 times lower than the conventional one. This is shown in Figure 4.9 and is the topology used in this project. The improvmenet are achieved by reducing the voltage swing at the drains of the input transistors (regenerative nodes). Excitation is from rail to rail in the conventional comparator, while it limited between $V_{\text{DD}}/2$ to V_{DD} in the new topology.

The comparator works as follows; as the reset voltage goes high, the input transistors P1 and P2 are isolated from the rest of the circuit by P3 and P4. The latch, which consists of P5,P6,N1 and N2 is reset by N5-N8 which pull all the latch nodes to ground. This causes the output, which is inverted, to go high on both the positive and negative ouput nodes. Other parts of the ADC use this behaviour to determine the state of the comparator, since this is the only time both outputs are equal.

Going out of reset, the transistors N5-N8 are turned off as the transistors P3 and P4 are turned on, connecting the input transistors to the latch. The current flow is regulated by the input transistor voltage difference. The nodes connected to the output inverters are then charged until one of them goes to V_{tn} of one the cross coupled nfet transistors N1 and N2. The voltage difference caused by the unequal currents is then regenerated and eventually the latch amplification will cause one of the nodes to go high and another to go low. This produces the digital output values of one and zero.

Other kickback reduction techniques where also investigated [40]. Many of the existing techniques tries to isolate the inputs from the capacitor array when the kickback effects occur. This is accomplished by using moderately complex clocking and a series of switches connected to the inputs of the comparator. Such methods do not fit within the suggested framework since they increase complexity and alter the top-level topology. A technique mentioned in several papers is the neutralization technique. Using two capacitors implemented using transistors (moscap), the kickback noise is canceled out. This method is said to have moderate effect. Transistors N_3 and N_4 in the schematic implement this technique.

Performance degrading gate leakage was observed through the input transistors. During reset, the input transistors are in a state where both the source and drain are connected to V_{DD} and subsequently, the gate leakage becomes quite large (100 to 200fA). This resulted in a constant voltage increase on the DAC arrays that could sometimes result in erroneous conversion of the voltage amplitude. Using the low Vt high t_{ox} available in the current technology almost eliminates this effect. In essense the added capacitors provide the charge that would otherwise by drawn from the DAC capacitor array.

Due to the relatively large fanout of the comparator, two extra inverters are added to each output node; further isolating the internal node swings from the output. Measurements showed that with a single inverter, outputs could drop below $2/3V_{DD}$ before a decision was made; dissipating charge in every node connected to them. The comparator inverters have more current drive and differ in topology compared to the regular digital inverters. Their default state is high, so stacked nfet transistors are used to reduce leakage. Schematics are presented in appendix B.4.

[10] employed the use of high V_t in the comparator latch and reset switches, with the intent of reducing static power consumption. This was not used in this comparator due to metastability problems; every transistor in this comparator is a low V_t type transistor.

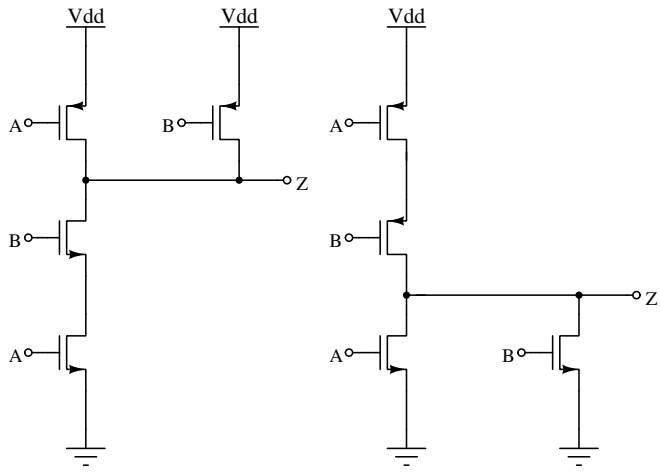

Figure 4.10 The conventional 4 transistor NAND (left) and NOR (right) gate

Dynamic comparators do not neccessarily have very good common mode rejection and dynamic offset can become an issue. The previous work was limited by this type of offset which forced a reduction in the input voltage. [32] suggests some measures to improve common mode rejection, describing a biased transistor between the comparator and supply as the simplest and most effective way to reduce the offset.

4.9 Switching procedure

The monotonic switching procedure has an ever decreasing common mode. This means that as you approach the LSB, the intrinsic gain of the comparator inputs are reduced with the increasing V_{eff}. By using the switchback algorithm, the V_{eff} decreases as it is approaching the LSB. The intrinsic gain will be higher at what will usually be the conversion with the worst noise margin. Worst case intrinsic gain is found when the common mode is $V_{\text{DD}}/4$.

Improving the gain of the input transistors not only helps with reducing the effects of noise, but also increases the resolving power of the comparator.

4.10 Digital logic gate implementation

The circuit only uses a few logic gates in order to implement the neccessary control logic. The previous design relied on NAND and NOR gates, but due to the new sampling logic,

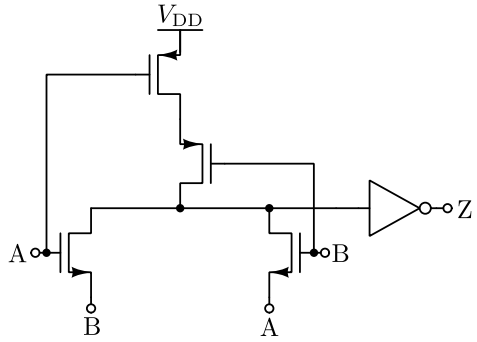

Figure 4.11 A XOR gate based on both pass logic and static logic [9].

a XOR gate has been added to the mix. It would be possible to use four NOR gates to implement the logic, but a design was found in [9] for a XOR gate where the tranistor count and power consumption is similar to conventional static gates. Its based on a combination of pass and static logic. NAND and NOR gates are implmented using the conventional four transistor static logic design as shown in Figure 4.10. The XOR gate is shown in Figure 4.11.

Previous work used a design method [41] that reduces the effects of mismatch and process variations in logic gates. This method has been researched in 65nm technology and there is indication that it reduces the variation in delay times and logic tresholds. The proposed design method uses extra transistors in order to implement standard gates in a very uniform manner, but there is no such research for 28 nm FD-SOI at this time. The variation in the current technology should be less than in 65nm CMOS bulk technology and due to the long conversions times, varying circuit delays should not be an issue. Use of this technique would result in increase gate capacitance and add to the dynamic power consumption of the ADC .

4.11 Digital control logic

An illustration of the high level interconnection of the SAR control logic is shown in Figure 4.12. Flip-flops are connected so they form a shift register where the $\overline{\text{RESET}}$ signal is the external clock. When the flip-flops are reset, the output (Q) goes high. System state corrolates to the propagation of the low (ground) signal connected to the first flip-flop in the string. The internal clock is used to drive the flip-flops.

The C²MOS flip-flops used in the previous work are used in this work as well. A schematic is presented in appendix B.3 for reference. A small change was made based on mismatch

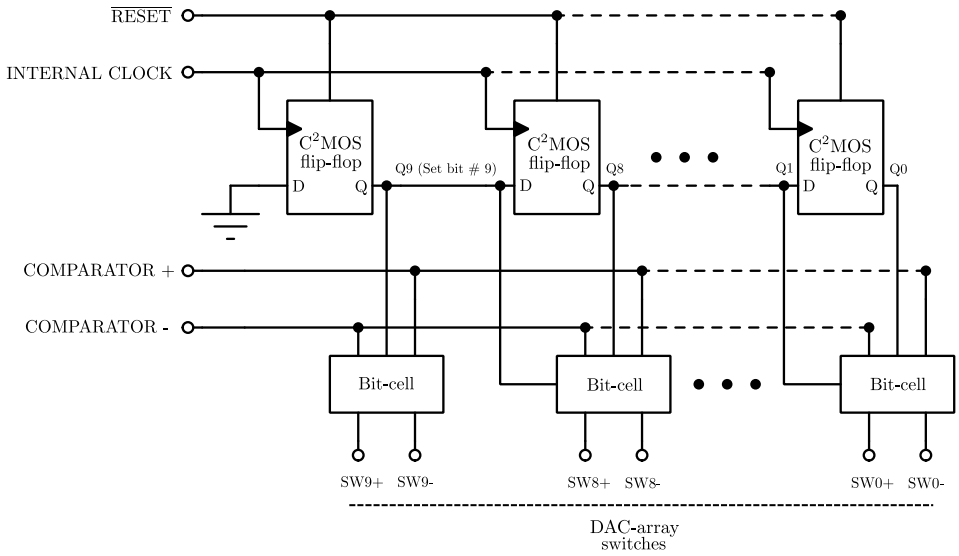

Figure 4.12 The flip-flop-based shift register and bit-cells used to implement the successive approximation algorithm.

simulations. The reset switch is changed from a high V_t to a low V_t type transistor. Mismatch would cause the reset transistor to have insuficient current drive which resulted in an undefined output.

4.12 Bit cell

The system state is kept by the flip-flops, but the actual storage of comparator outputs is done by the bit cells. [4] describes the use of masking gates that isolate idle circuits from the clock. Although this paper talks about microprocessors, the principle of reducing switched gate capacitance is applicable to most digital circuits. The comparator output nodes have the largest fanout in the ADC . If every bit-cell connected to the comparator output have multiple nodes following it, energy is wasted on discharging and charging of the internal node capacitances.

With this in mind; a look the previous bit-cell design in Figure 4.13 shows that both NAND gates have active outputs before the bit-cell is latched. This means that the output node (V_{i+} or V_{i-} in the figure) of 10 NAND gates are switching on the first conversion with a reduction of one for every consecutive conversion.

The new design in Figure 4.14 reduces the number of transistors and uses masking gates to isolate the bit cell when it is not needed. The PSET signal is the SET (Q) signal from the

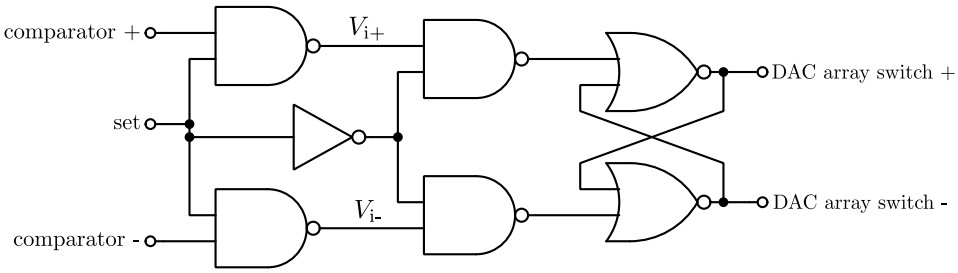

Figure 4.13 The bit-cell used in previous work [10] .

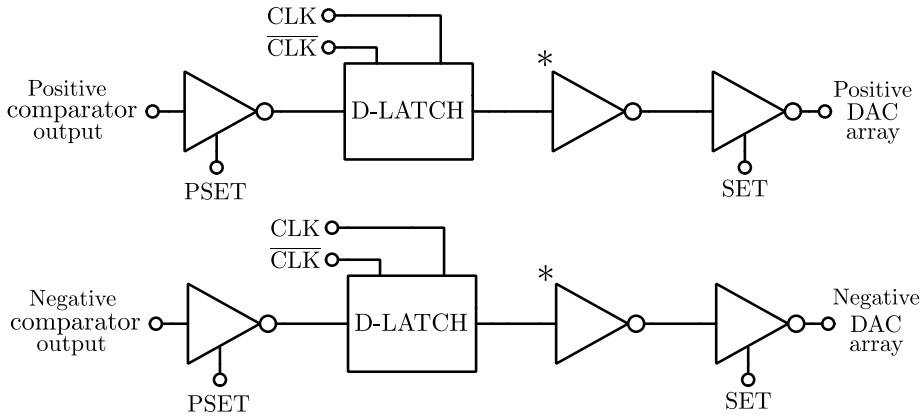

Figure 4.14 The bit cell circuit.

leading bit cells flip-flop. In order to store the comparator results, inverter based latches are used together with modified tri-state inverters. The latches are controled using transmission gates that crosscouple the inverters in the hold phase and isolates them in the track phase. A schematic is shown in Figure 4.15. The tri-state inverters are used to reduce the switching activity in the circuit during conversion and to provide a known output when waiting for a comparator value. The tristate inverter is enabled when the latch preceding it has settled on a value. This means that at any time, only two pairs of latches are tracking the input.

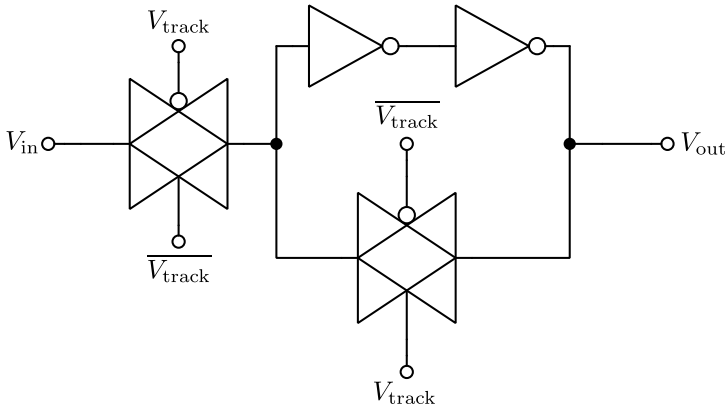

Figure 4.15 The D-latch used in the ADC bit cells.

Chapter 5

Layout

The layout was done using Layout XL in Cadence Virtuoso with the purpose of confirming that the chosen circuit topology is capable of running with a power consumption less than a nanowatt and with sufficient resolution. Results of the parasitics extraction after layout is presented in the results chapter.

5.1 Digital routing

Digital circuits have been placed in a Weinberger image. This layout method was chosen since it ensures high density and provides a uniform layout [5] . It provides convenient access to the power and ground metals for each transistor while keeping the interconnect relatively low. Creating individual cells is easier due to the regular nature of the layout. A portion of the digital layout that illustrates the Weinberger placement is shown in Figure 5.1.

Placements of the digital blocks that implement the SAR algorithm is illustrated in Figure 5.3. The "bit-blocks" are a flip-flop and bit-cell. All the bit-block are connected on a "string" that could be placed in a long line starting with bit-block #9 and ending with bit-block #0. The "string" is instead looped back at bit-block #5; saving area and reducing the interconnects.

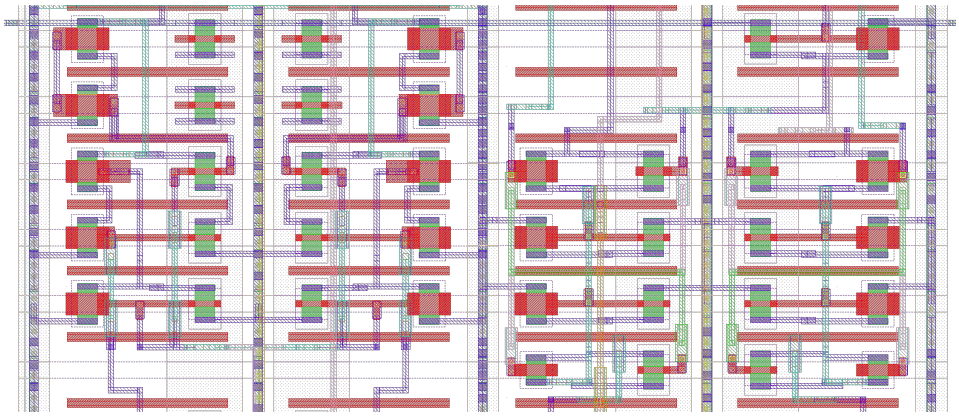

Figure 5.1 Digital logic layout in a Weinberger image.

Figure 5.2 A $4C_u$ (8fF) capacitor used in the DAC capacitor array.

5.2 Custom capacitors

As in [10], the DAC capacitors are implemented by using custom-designed metal-metal capacitors based on [42]. In this work, the sample and hold capacitors where made in metal layer 5 and 6 in order to reduce parasitics in the DAC. Previous work used the same common centroid approach as in [42] for the capacitor interconnects and had to reduce the input swing slightly due to the gain error.

This was found to be problematic in this work. The DAC array proved to be extremely sensitive to the bottom plate parasitics and would introduce significant gain errors in the SAR ADC. The problem is commented on in [42] regarding their DAC array implementation; attributing most of the redundant 251 fF (with a total of 377 fF in the array) on the parasitics introduced by the common centroid approach. It also states that improvements to the interconnection or grouping of elements need to be made before any further downscaling should be attempted.

A more simplistic or "dumb" approach was used in this work (mostly due to time constraints). Unit capacitors are not evenly distributed, but instead concentrated to a single location. Interconnect between them is kept minimal, as shown in Figure 5.2, and the switching inverters are connected directly to them. This can be seen in Figure 5.4 as the string of inverters between the digital logic and capacitor array. The grouping of capacitors shown in Figure 5.3 makes it possible to place the inverters as close and with as little interconnect as possible. The grouping also corresponds to the bit-block placement. For example; bit-block #1 would be connected to the single C_u capacitor.

Even with the reduction in interconnection wiring, the unit capacitor still had to be increased from 1 fF to 2 fF in order to achieve a decent voltage space.

The load capacitors in the comparator and bootstrap switches where provided by Harald Garvik and have a value of about 17 fF each.

5.3 Final layout

The full layout of the ADC is presented in Figure 5.4. Different parts of the system are color coded and there are several lines indicating scale.. The area consumption is 0.01mm^2, but small adjustment of the bootstrap switches orientation would reduce this to 0.0063mm^2.

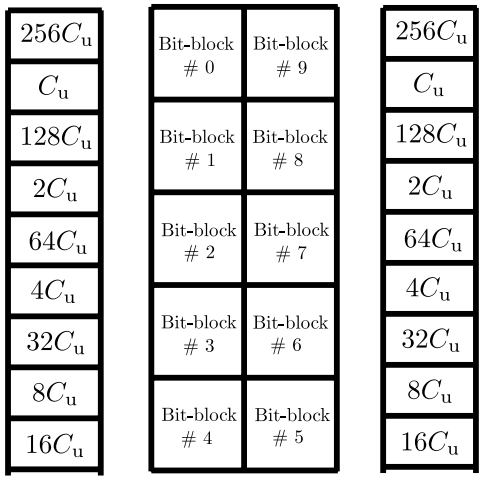

Figure 5.3 The organization of the digital "bit-blocks" and the grouping of the DAC array capacitors.

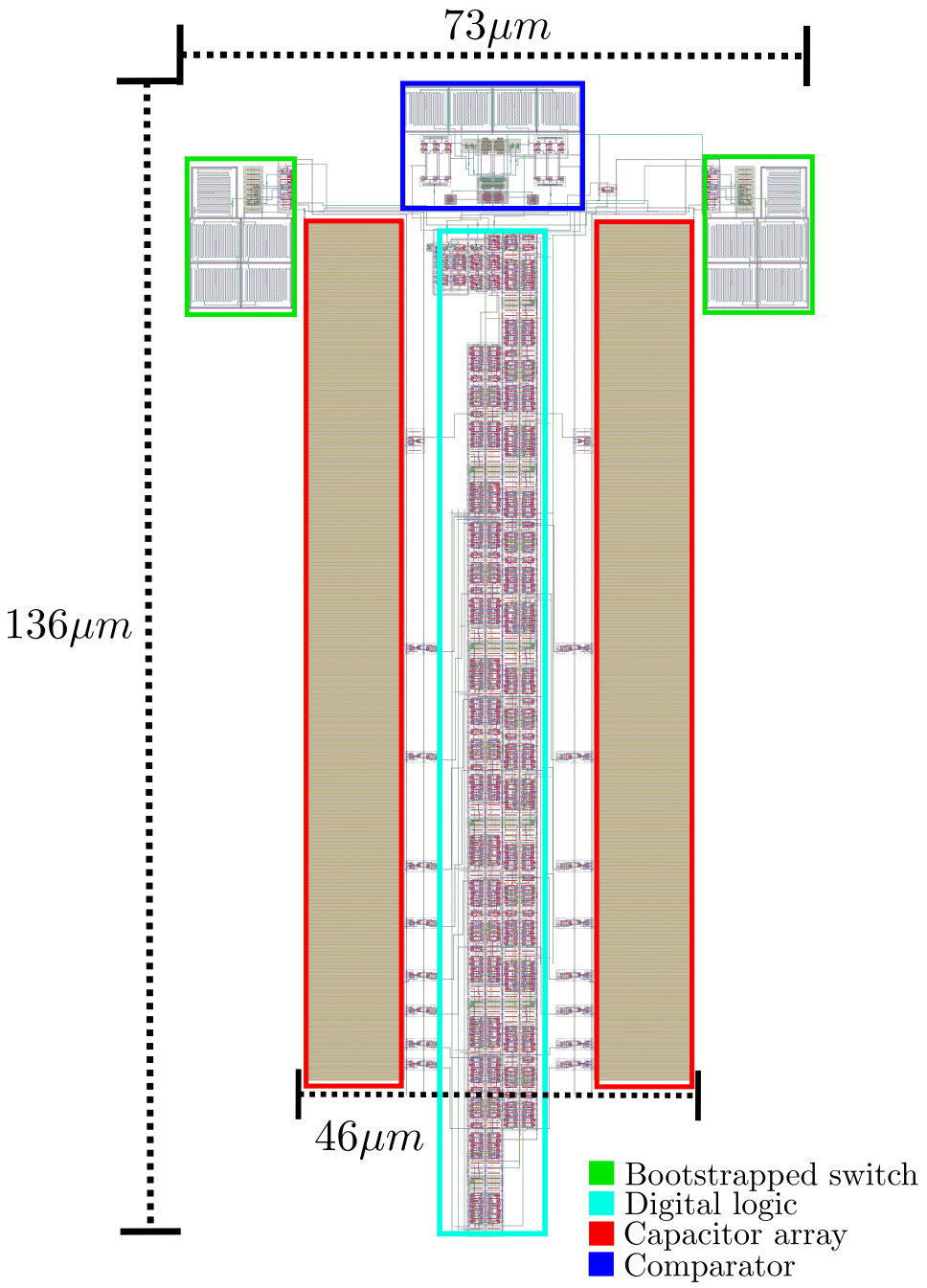

Figure 5.4 The complete SAR ADC layout.

Chapter 6

Results

This chapter presents the results at the end of the master thesis project. Simulations on the schematic will be presented before the post-layout simulations. Transient noise analysis is used to confirm resolution and power consumption over different process corners. Monte Carlo simulation provides and indicator on how robus the circuit is against mismatch. The difference in power consumption between pre-layout and post-layout is shown at the end of this chapter.

6.1 Pre-layout simulations

Some of the simulations in this section where performed before layout and use smaller unit capacitors (C_u) in the DAC. Therefore, the power consumption will not always be comparable to layout. Proper functioning of the schematic was confirmed by with a 10.0-bit ENOB value during transient simulation. Noise performance for the typical corner was simulated and the results are shown in Table 6.1. The 64 sample transient noise analysis gave an effective numbers of bits of 9.4-bit.

Table 6.1 Schematic transient noise analysis. (C_u = 1 fF)

Output	Value
ENOB	9.4-bit
SNDR	58.4dB
SNR	58.4dB
SFDR	67.1dB
Comparator power	121.7 pW
Digital power	139.9 pW
SH/DAC power	88.81 pW
Total power	350.4 pW
Input swing	430 mV_{pp}

Static power was measured for the individual parts of the system both in the schematic and in layout. Schematic measurements are presented in Table 6.2. The static consumption before and after layout was the same.

Table 6.2 The static power consumption in the ADC (C_u = 2 fF) .

	Power [pW]
Comparator	13.0
Digital logic	62.5
SH/DAC	11.1
Total	86.5

Monte Carlo mismatch transient simulation on the schematic is shown in Table 6.3. No noise is enabled in these simulations. The mean value ENOB for the noiseless circuit is 10.06-bit. Mismatch caused an offset in the comparator and this is compensated for by reducing the input swing from 450 mV_{pp} to 430 mV_{pp}.

Table 6.3 Results of 60 Monte Carlo runs of 64 sample transients simulating mismatch. These simulations where made before layout and used a 1 fF unit capacitor and 430mV_{pp} input.

Parameter	Mean	Median	Std Dev
Total power [W]	356.1p	356.2p	1.963p
Comparator power [W]	121.1p	121.0p	1.275p
Digital power [W]	144.4p	143.9p	1.51p
SH/DAC power [W]	90.61	90.73p	586f
ENOB [bit]	10.06	10.1	221.7m
SFDR [dB]	71.3	71.15	1.533
SNR [dB]	62.31	62.54	1.335

6.2 Post-layout

The post simulations have similar ENOB resoultion as the schematic with 9.4-bits. Power consumption is increased and the input swing had to be reduced to 400mV_{pp} due to the gain error caused in the SH/DAC. A transient noise analysis investigating the change in ENOB over corners is presented in Table 6.4.

A summary of the post-layout performance characteristics is given in Table 6.5. The graph in Figure 6.1 shows the resulting spectrum of a 256-sample transient noise analysis when the ADC is measuring a input signal close to the nyquist frequency. Table 6.6 shows the pre and post layout power consumption where the scehmtaic C_u = 2fF; giving a accurate comparison.

Table 6.4 Transient noise analysis post layout used to check the ENOB variation over corners. Supply voltage was 450 mV for all corners.

Process corner	Samples	ENOB [bit]
TT	64	9.4
TT	128	9.5
FFA	64	9.4
SSA	64	9.4
SFA	64	9.5
FSA	64	9.3

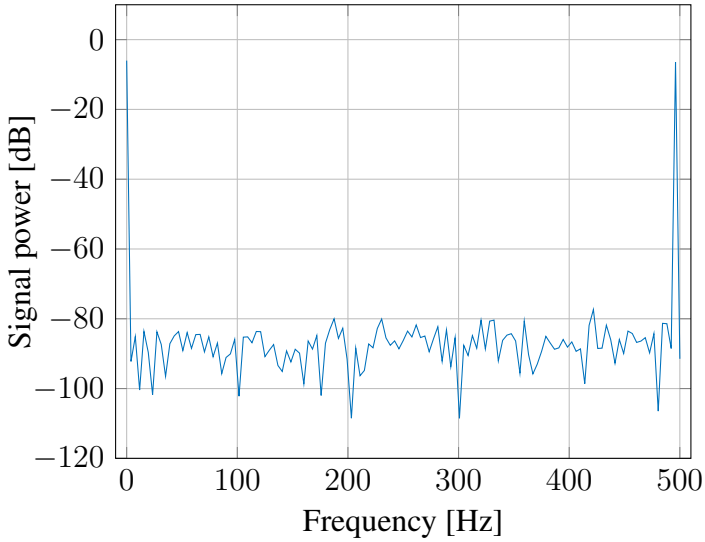

Figure 6.1 Spectrum of a 256 sample transient noise analysis after layout.

Table 6.5 Post-layout performance summary

Technology	28 nm FD-SOI
Area	0.01 mm^2
Sampling rate	1 kS/s
Supply voltage	450 mV
Common-mode level	225 mV
Input range	400 mV_{pp}
SNDR	58.3 dB
SFDR	70.9 dB
SNR	58.3 dB
ENOB	9.4-bits
Comparator power	153.6 pW
Digital logic power	367.3 pW
Sampling/DAC power	170.7 pW
Leakage power	86 pW
Total power	693 pW
FOM	1.0 fJ/conv.

Table 6.6 The power consumption in the ADC before and after layout (C_u = 2 fF for both) .

	Pre-layout	Post-layout
Comparator	121.2 pW	153.6 pW
Digital logic	143.2 pW	367.3 pW
Sampling/DAC	166.7 pW	170.7 pW
Total power	430.1 pW	691.5 pW

Chapter 7

Discussion

This chapter comments on the results of chapter 6 and the different design choices and shortcomings that could be of interest in further work.

7.1 System power consumption

The power consumption was measured before and after layout. Before the capacitance extraction, the circuit had a power consumption of 430pW; putting it almost perfectly at half the consumption of the previous work. After layout, the power consumption increased to 691.5pW. That is a 61% increase in power consumption. For comparison; previous work had a 45% increase from 843pW to 1.22nW. This increase can be attributed to the increased power supply or that the layout parasitics play a larger part in the overall power consumption.

Simon Josephsen postulated that the reason for the almost doubling in power consumption was a result of increased parasitics in the digital control logic. He was; however, not able to do a proper measurement. In this thesis, power consumption for each system part is accounted for; both pre and post-layout. Looking at Figure 7.1 his assumptions seem to be correct. The digital logic consumes 33% of the pre-layout power and this is then increased to 53% post-layout.

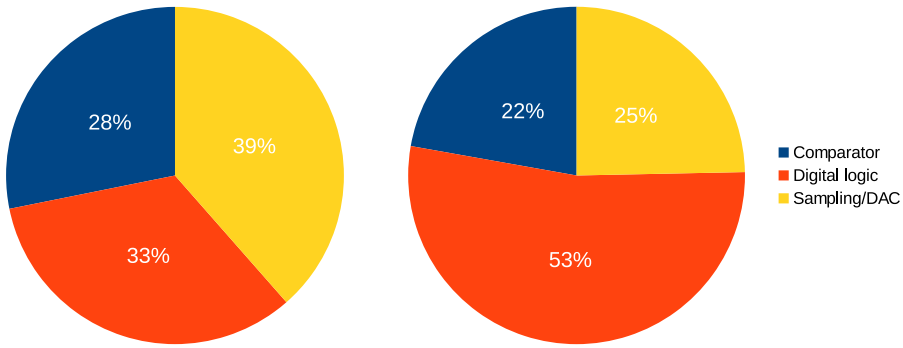

Figure 7.1 The power distribution in the ADC pre-layout (left) and post-layout(right) based on the values in Table 6.6.

The comparator and DAC array see a small increase in power consumption, but this is minor in comparison to the digital logic. It seems that when designing further revisions of this ADC, it will be reasonable to assume that the analog circuits (the ones with the most load capacitance) , will have roughly the same consumption before and after layout; while at least a doubling of consumption in the digital part should be assumed.

7.2 DAC

The original unit capacitor was chosen to be $1fF$ but was increased to $2fF$ in order to reduce the gain offset error that was caused by the bottom plate parasitics after layout. Due to time constraints, the DAC was made in a very simple fashion, omitting the common centroid layout.Switching inverters where connected directly, with very little routing to each capacitor.

It is difficult to comment on how this would affect the influence of process variation, but it is possible that it would reduce the averaging effect seen in a layout, such as common centroid, where each capacitor covers the "entire" area of the DAC array.

The end result is a gain offset of 50mV, in which 30mV can be attributed to bottom plate parasitics, and 20mV to the input parasitics of the comparator. This is worse than previous work, but due to the increased supply voltage the rail to rail voltage range is better.

7.3 Changing to the switchback algorithm

Using the switchback procedure has shifted some of the comparators power consumption over to the DAC array at a smaller cost than adding more load capacitors. Shifting from the monotonic procedure to the switchback procedure improved the noise behaviour in the comparator.

Comparing the two procedures, there are no obvious downsides to the switchback procedure; other than its increased power consumption. Before layout, the monotonic procedure would dissipate roughly 60 pW with a 1 fF unit capacitor. After the change to the switchback procedure, this consumption rose to just under 90 pW. Since it allowed the removal of half of the load capacitance in the comparator, this resulted in a reduction of the total power consumption.

The implementation of the switchback procedure resulted in almost no change in the ADCİnverters where the only thing added in order change how the bit-cells switch the DAC array capacitors.

7.4 Comparator

It is difficult to say whether or not the new comparator topology is better than the previous one. It does however provide the necessary performance, and was shown to work with $1fF$ unit capacitor in the DAC. The focus on reducing kickback in order to push for smaller unit capacitors might have been unnecessary since the unit capacitor ended up being similar to the one used in the previous work.

The sizing of the comparator might not be aggressive enough. Looking at the Monte Carlo simulation results Table 6.3; it seems clear that the mismatch is much better than it needs to be. The transistor dimensions are actually larger in this work compared to the previous. This is due to some design decisions based on faulty simulations; resulting in over-design against mismatch. A downsizing could probably also remove the gain offset due gate parasitics, as this is not mentioned in the previous work.

The speed of the comparator is not as good as previous work; requiring increased voltage for both of the slow corners after layout[4]. Again, this could be attributed to the over-design; a smaller sizing of the transistors might improve speed.

7.5 Digital logic

Changing from synchronous to asynchronous operation went rather smoothly. [10] commented that a large portion of the logic could easily be ported to an asynchronous design. This was definitely the case as most of the SAR logic has stayed the same. The main work was to make the sampling logic work correctly and to make the asynchronous clock feedback controller logic. The latter was mostly to ensure that it had enough delay so that the DAC array value would settle before the comparator was enabled again.

Overall, the logic complexity has gone down. Comparing the new digital logic to the previous one, shows that it uses fewer flip-flops and that that it is possible to do a reset independent of the ADC state.

7.6 Asynchronous operation

The choice of going for an asynchronous architecture was made in order to reduce the top level power consumption and lessen the demand on external circuitry. This transition was achieved using less logic than the previous design and accompanied with the reduction of capacitor area of the two bootstrapped sampling switches. This asynchronous operation

[4] The corners used by the author might be more pessimistic than the ones used to simulate corners in the results chapter, as they were simulated on a different machine.

provides a power reduction in both a top level point of view and a system point of view as well as it provides a smaller circuit. Asynchronous also increases the duty cycle or active cycle the comparator can have. Reset is done when the clock is low, meaning that it only needs to be in that state for a short while. This could potentially be used to triple or quadrouple the sampling frequency of the comparator.

The negative aspects is that there might be a need for proper biasing of the delay elements if the comparator is to be used outside a controller enviroment with correct temperature. Currently there is no temperature rejection in the circuit as this is outside the scope of the project.

7.7 Choice of delay element

Making use of inverter buffers delays proved cumbersome in this work. Creating delays that were sufficiently large required transistors with very long channel lengths combined with large capacitors ranging in the 60-80 fF range. These types of delays would also vary considerably with supply voltage changes; meaning, that for any voltage change during the development of the ADC , these elements would need to be redesigned.

The thyristor based delay enables the generation of really long delays with minimal design effort; and at the same time, measurements showed that it consumed less power and area[5] compared to the previous delay elements. Mismatch simulation on schematic also showed that it had less delay variation compared to the RC-element. This fits well with the claim made by [1] that the circuit gets less sensitive to V_t variance as the delay time increases.

There really is little to complain about with this delay element.

7.8 Future work

A disappointing change was the increase of the unit capacitor in the DAC array. It might be that other topologies should be investigated; perhaps the split dac array used in [29] is a good way to increase the unit capacitor while keeping the total capacitance low.

Here are some thoughts and ideas regarding further work on the ADC :

- The speed of the ADC should be improved to a point where it works well in all corners,
- Improved speed could be used to lower the supply voltage,
- Investigate if the danger of race conditions can be eliminated through the use of low V_t type transistors.

[5] The area of the 17 fF load capacitor is almost the same as the total size of the thyristor delay element.

- Investigate if the capacitor array switches realised with low V_t could achieve faster settling with sufficent leakage.
- Investigate if an increase in resolution or a reduction in power become possible through the use of digital noise reduction.
- Improve the digital layout by using techniques that reduce parasitics and by improving the topology to reduce parasitics.

7.9 Bootstrapped

Using a edge triggered pulse in order to generate the sampling signal reduced the time the bootstrapped circuit needs to be active. This has lead to a reducation of the bootstrap capacitor by half. Even

7.10 Comparison with previous work

The new design improves on the previous design in almost every way. It provides higher resolution at almost half the power consumption and consumes less area. The FOM is improved by a factor of four. Table 7.1 shows the performance of both designs.

Table 7.1 Comparison of this work with the previous work

Parameter	[10]	[This work]
Technology	65 nm	28 nm
Area [mm²]	0.0138	0.0100 (0.0063)
Sampling rate [kS/s]	1	1
Resolution [bit]	9	10
Supply voltage [V]	0.40	0.45
Power [nW]	1.22	0.69
ENOB [bits]	8.16	9.40
FOM [fJ/conv.]	4.27	1.00

Chapter 8

Conclusion

In this project, a 10-bit 1kS/s SAR ADC with sub-nanowatt power consumption has been successfully designed and simulated in both schematic and with extracted parasitics after layout. The ultra-low power consumption is achieved by using the ADC topology developed in [10]. Increased resolution is achieved by carefull alterations to the same topology.

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A Verilog code

A.1 Ideal comparator

```
1   // VerilogA for HAZELBURN_ST28N, COMPARATOR_IDEAL, veriloga
2
3   `include "constants.vams"
4   `include "disciplines.vams"
5
6   module COMPARATOR_IDEAL(VIP,VIN,RESET,VOP,VON,SUPPLY,GROUND);
7
8   input VIP,VIN,RESET,SUPPLY,GROUND;
9   electrical VIP,VIN,RESET,SUPPLY,GROUND;
10
11  output VOP,VON;
12  electrical VOP,VON;
13
14  parameter real delay_ = 10u, trise = 40p, tfall = 40p;
15
16  real positive_output;
17  real negative_output;
18
19  analog begin
20      @(initial_step) begin
21          positive_output = V(SUPPLY);
22          negative_output = V(SUPPLY);
23      end
24
25      @(cross(V(RESET) < V(SUPPLY)/2,-1,1f)) begin
26          positive_output = V(SUPPLY);
27          negative_output = V(SUPPLY);
28      end
29
30      @(cross(V(RESET) > V(SUPPLY)/2,-1,1f)) begin
31          if ( V(VIP) >= V(VIN) ) begin
32              positive_output = V(SUPPLY);
33              negative_output = V(GROUND);
34          end
35          else begin
36              positive_output = V(GROUND);
37              negative_output = V(SUPPLY);
38          end
39      end
40
41      V(VOP) <+ transition(positive_output,delay_,trise,tfall);
42      V(VON) <+ transition(negative_output,delay_,trise,tfall);
```

```
43      end
44
45      endmodule
```

A.2 Ideal capacitor array

```
1       // VerilogA for HAZELBURN_ST28N, CAP_ARRAY, veriloga
2
3       `include "constants.vams"
4       `include "disciplines.vams"
5
6       module CAP_ARRAY_VERILOG(OUT, CTRL, GROUND, IN, SAMPLE, SUPPLY);
7       output OUT;
8       electrical OUT;
9       input [1:9] CTRL;
10      electrical [1:9] CTRL;
11      input GROUND;
12      electrical GROUND;
13      input IN;
14      electrical IN;
15      input SAMPLE;
16      electrical SAMPLE;
17      input SUPPLY;
18      electrical SUPPLY;
19
20
21      parameter real delay_ = 0, trise = 20p, tfall = 20p;
22
23      real vref;
24      real sampled;
25      real sub[1:9];
26
27      analog begin
28          @(initial_step) begin
29              vref = V(SUPPLY);
30              generate ii (1,9,1) begin
31                  sub[ii] = V(GROUND);
32              end
33          end
34
35          @(cross(V(SAMPLE) > V(SUPPLY)/2,-1,1f)) begin
36              sampled = V(IN);
37              generate ii (1,9,1) begin
38                  sub[ii] = V(GROUND);
39              end
40          end
```

```
41
42          // Switchback
43          @(cross(V(CTRL[9])<V(SUPPLY)/2,-1,1f)) begin
44                  sub[9] = vref/pow(2,10-9);
45          end
46
47          generate ii (1,8,1) begin
48              @(cross(V(CTRL[ii])<V(SUPPLY)/2,-1,1f)) begin
49                  sub[ii] = vref/pow(2,10-ii);
50              end
51          end
52
53          //V(OUT) <+ transition(sampled-sub[1]-sub[2]-sub[3]-sub[4]-sub[5]
54      -sub[6]-sub[7]-sub[8]-sub[9],delay_,trise,tfall);
55          V(OUT) <+ transition(sampled+sub[1]+sub[2]+sub[3]+sub[4]+sub[5]
56      +sub[6]+sub[7]+sub[8]-sub[9],delay_,trise,tfall);
57      end
58
59      endmodule
```

A.3 Ideal control logic

```
1       // VerilogA for HAZELBURN_ST28N, CTRL_LOGIC, veriloga
2
3       `include "constants.vams"
4       `include "disciplines.vams"
5
6       module CTRL_IDEAL(CTRL_N, CTRL_P, CLK, COMP_N, COMP_P, NCLK,
7        NRESET,SUPPLY,GROUND);
8
9       output [0:9] CTRL_N;
10      electrical [0:9] CTRL_N;
11      output [0:9] CTRL_P;
12      electrical [0:9] CTRL_P;
13      input CLK;
14      electrical CLK;
15      input COMP_N;
16      electrical COMP_N;
17      input COMP_P;
18      electrical COMP_P;
19      input NCLK;
20      electrical NCLK;
21      input NRESET;
22      electrical NRESET;
23      input SUPPLY;
24      electrical SUPPLY;
```

```
25      input GROUND;
26      electrical GROUND;
27
28      parameter dac_size = 10;
29
30      // Temporary storage of outputs
31      real p_switch_array [0:dac_size-1];
32      real n_switch_array [0:dac_size-1];
33      real pcal_switch_array [0:dac_size-1];
34      real ncal_switch_array [0:dac_size-1];
35
36      // For use in for loops
37      integer i;
38      integer reset_counter;
39
40
41      // Which bit is being detected
42      integer bit_number = dac_size-1 from (0:dac_size-1);
43
44      parameter real delay_ = 0, trise = 20p, tfall = 20p;
45
46      analog
47      begin
48          // At the beginning all outputs should be zero
49          @(initial_step) begin
50              bit_number = dac_size-1;
51              reset_counter = 0;
52              for ( i=0; i<dac_size; i=i+1) begin
53                  p_switch_array[i] = V(GROUND);
54                  n_switch_array[i] = V(GROUND);
55              end
56          end
57
58          @(cross(V(CLK) < V(SUPPLY)/2,-1,1f)) begin
59              if ( V(NRESET) > V(SUPPLY)/2 ) begin
60
61                  // SWITCHING LOGIC
62                      if ( bit_number < dac_size ) begin
63                          if ( V(COMP_P) > V(COMP_N) ) begin
64                              p_switch_array[bit_number] = V(SUPPLY);
65                              n_switch_array[bit_number] = V(GROUND);
66                          end
67                          else begin
68                              p_switch_array[bit_number] = V(GROUND);
69                              n_switch_array[bit_number] = V(SUPPLY);
70                          end
71                      end
72
73                      if ( bit_number > 0 ) begin
```

```
74                      bit_number = bit_number - 1;
75                  end
76              end
77          end
78
79          // Due to the flip-flops, reset requires two clock cycles.
80          @(cross(V(NRESET) > V(SUPPLY)/2,-1,1f)) begin
81              bit_number = dac_size-1;
82              for ( i=0; i<dac_size; i=i+1) begin
83                  p_switch_array[i] = V(GROUND);
84                  n_switch_array[i] = V(GROUND);
85              end
86          end
87
88
89          V(CTRL_P[9]) <+ transition(p_switch_array[9],delay_,trise,tfall);
90          V(CTRL_N[9]) <+ transition(n_switch_array[9],delay_,trise,tfall);
91          generate ii (0,8,1) begin
92          //generate ii (0,9,1) begin
93              // Husk aa bytte koblinger ved switchback
94              //V(CTRL_P[ii]) <+ transition(p_switch_array[ii],delay_,trise,tfall);
95              //V(CTRL_N[ii]) <+ transition(n_switch_array[ii],delay_,trise,tfall);
96              V(CTRL_N[ii]) <+ transition(p_switch_array[ii],delay_,trise,tfall);
        //Switchback
97              V(CTRL_P[ii]) <+ transition(n_switch_array[ii],delay_,trise,tfall);
        // Switchback
98          end
99      end
100     endmodule
```

B Schematics

Circuit schematics not covered in the thesis are presented here. A short description of each block is given.

B.1 Clock feedback control

The feedback loop between the comparator output and reset is controlled by the block shown below. There are several redundant inverters in the circuit which serve as delays to avoid race conditions. The delay element is optional and was not used in the project, but might be usefull in other designs. The INTERNAL CLK is the clock signal generated by the outputs of the comparator. The $\overline{\text{BUSY}}$ is the busy signal from the sampling logic block and the SW0$\pm$ is the switch control signals for the final bit.

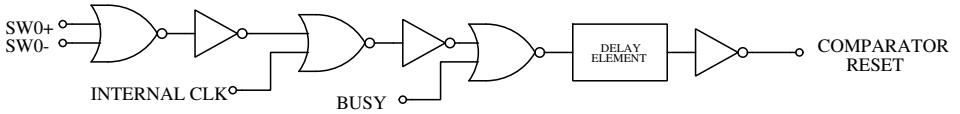

Figure B.I Asynchronous loop control logic.

B.2 Internal clock generator

The internal clock is generated by detecting when the outputs of the comparator are different. Based on the state of the comparator; the internal clock will either be high or low.

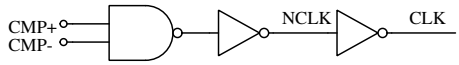

Figure B.II Internal clock generating logic.

B.3 C²MOS flip-flop

The flip-flop used in [10]. It is used to implement the shift register that holds the the system state. The reset transistor is replaced with a low-V_t type transistor in order to ensure enough current drive for all mismatch conditions.

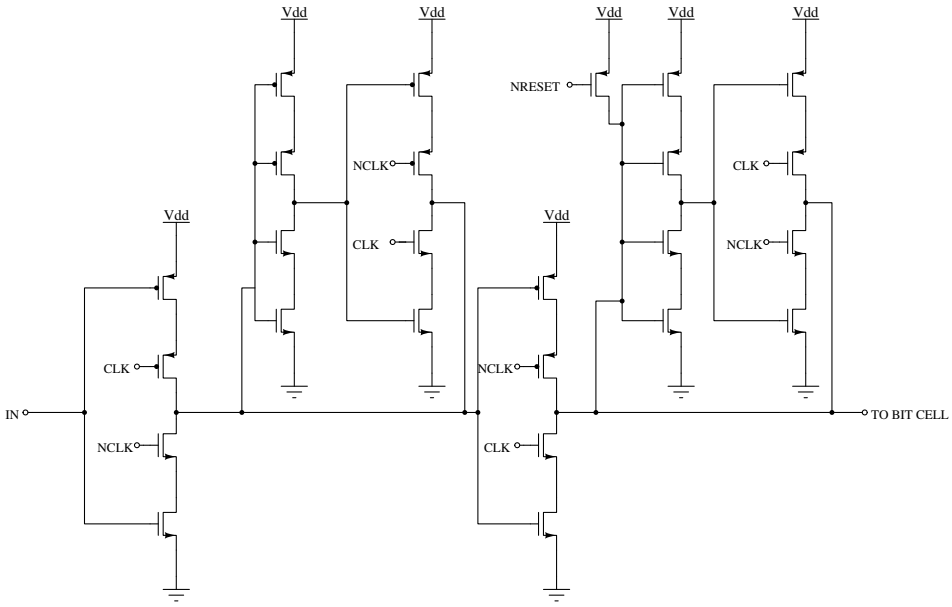

Figure B.III The C²MOS flip-flop schematic [10] .

B.4 Tri-state inverter

Shown in Figure B.IV, the tri-state inverter provides normal inverter operation with the possibility of entering a high impedance state with a known output value. As the V_{enable} goes low, the inverter input enters a high impedance state and the output node is pulled to ground.

B.5 Comparator output inverters

Shown in Figure B.V, these inverters are used to buffer the output of the comparator. They provide higher current drive than digital inverters and low leakage in the high state.

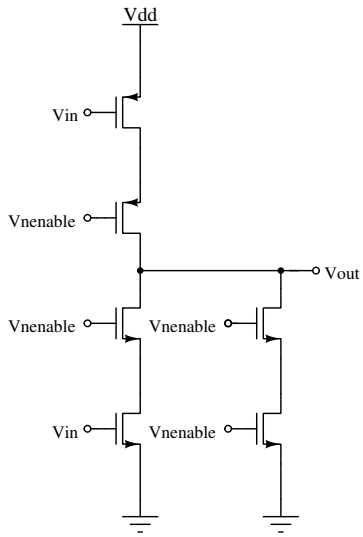

Figure B.IV Inverter with three states. Normal operation and high impedace input and low output.

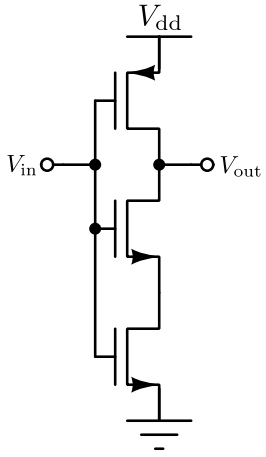

Figure B.V Inverter used in the comparator.