TPE_RAM_1536X8X4HS_AT110N_N1

AT110N - 1536x32 RAM block - SPECIFICATION

MAIN FEATURES

- Single port Static RAM
- Fully synchronous
- 2 operation modes : read, write
- 32 bit separated I/Os
- Read and Write byte access
- Power supply: 1.08V - 1.40V
- Temperature range : -40°C - 105°C
- High density
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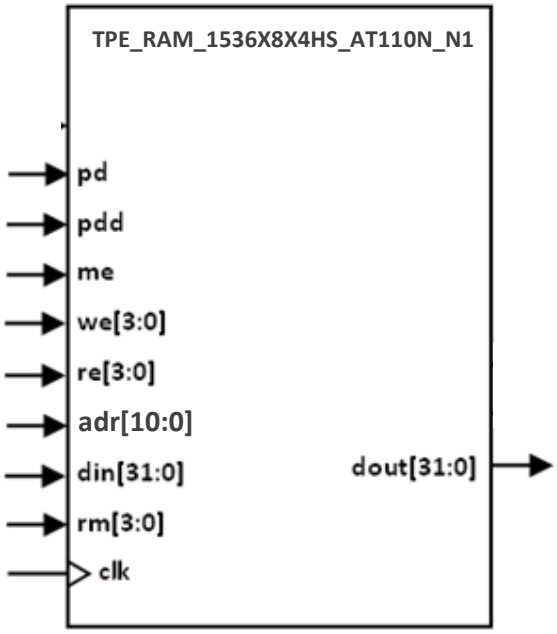
DESCRIPTION

TPE_RAM_1536X8X4HS_AT110N_N1 operates in single-edge clock controlled mode during read and write operations. Addresses (***adr***) are clocked internally on the rising edge of the clock signal (***clk***). Any change of address without rising edge of ***clk*** is not considered.
The memory can be de-activated when memory enable (***me***) is low. This reduces the consumption when the memory is not accessed.

USER INTERFACE

SIGNAL	TYPE	FUNCTION	COMMENTS
clk	Input	Clock	Active on rising edge
me	Input	Memory Enable	Active High
we[3:0]	Input	Byte Write Enable Masks	Active High
re[3:0]	Input	Byte Read Enable Masks	Active High
adr[10:0]	Inputs	Address bus	Used in write/read mode
din[31:0]	Inputs	Input data bus	Used in write mode
rm[3:0]	Inputs	Read margin adjustment	Default 4'b1111[1]
dout[31:0]	Outputs	Output data bus	
pd	input	sleep enable	Active High
pdd	input	sleep enable	Active Low

Note1:RM[3:0] setting is from 0001(low speed with higher reliability) to 1111(high speed with lower reliability). 1111 is default setting. 0000 is forbidden setting that might cause function fail.



Memory Symbol

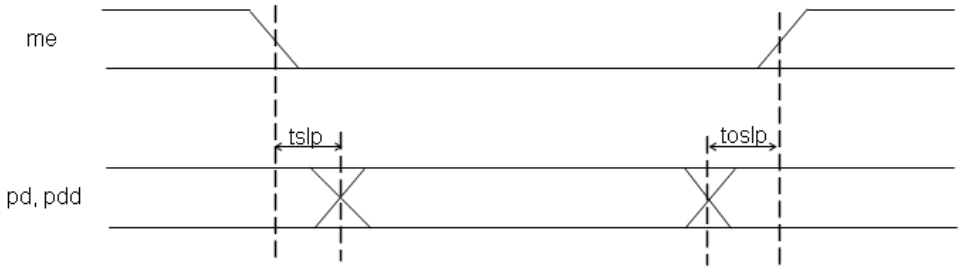
FUNCTIONAL DIAGRAMS

Sleep Mode

In the sleep mode the ***me*** signal must be low, pd and pdd pin follow the table below to get in source-bias, drain bias or both. Source bias raises the SRAM cell pull down NMOS source voltage. Drain bias descends the SRAM cell pull up PMOS source voltage. During sleep mode the ***dout*** pins rest in the state of the last read operation.

Truth table

me	pd	pdd	state
0	0	0	Active drain bias.
0	0	1	Without source and drain bias
0	1	0	Active source and drain bias
0	1	1	Active source bias
1	0	1	When me=1,pd and pdd must be 0 and 1

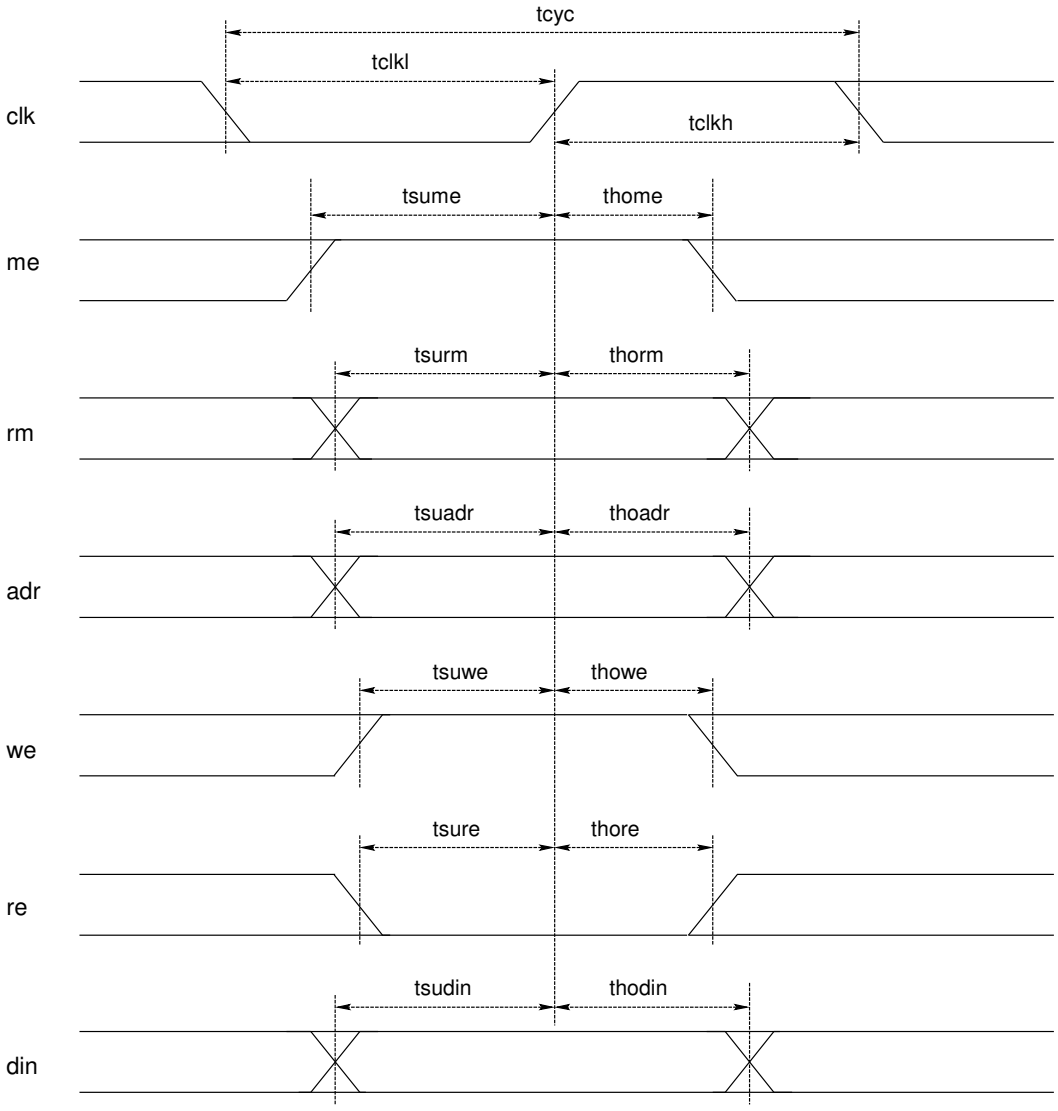


Sleep Mode: timing diagram

Write Mode:

In the write mode the ***me*** signal must be high, ***we*** must be high, and ***re*** must be low (simultaneous read/write is forbidden). The ***adr*** input pins are set up and decoded to select the desired word. The ***din*** are latched on the rising edge of ***clk*** and stored in the ram. During the write operation the ***dout*** pins rest in the state of the last read operation. Write operation can be done on a byte, using ***we[3:0]*** write enable masks:

we[3]	active high : write operation din[31:24]
we[2]	active high : write operation din[23:16]
we[1]	active high : write operation din[15:8]
we[0]	active high : write operation din[7:0]

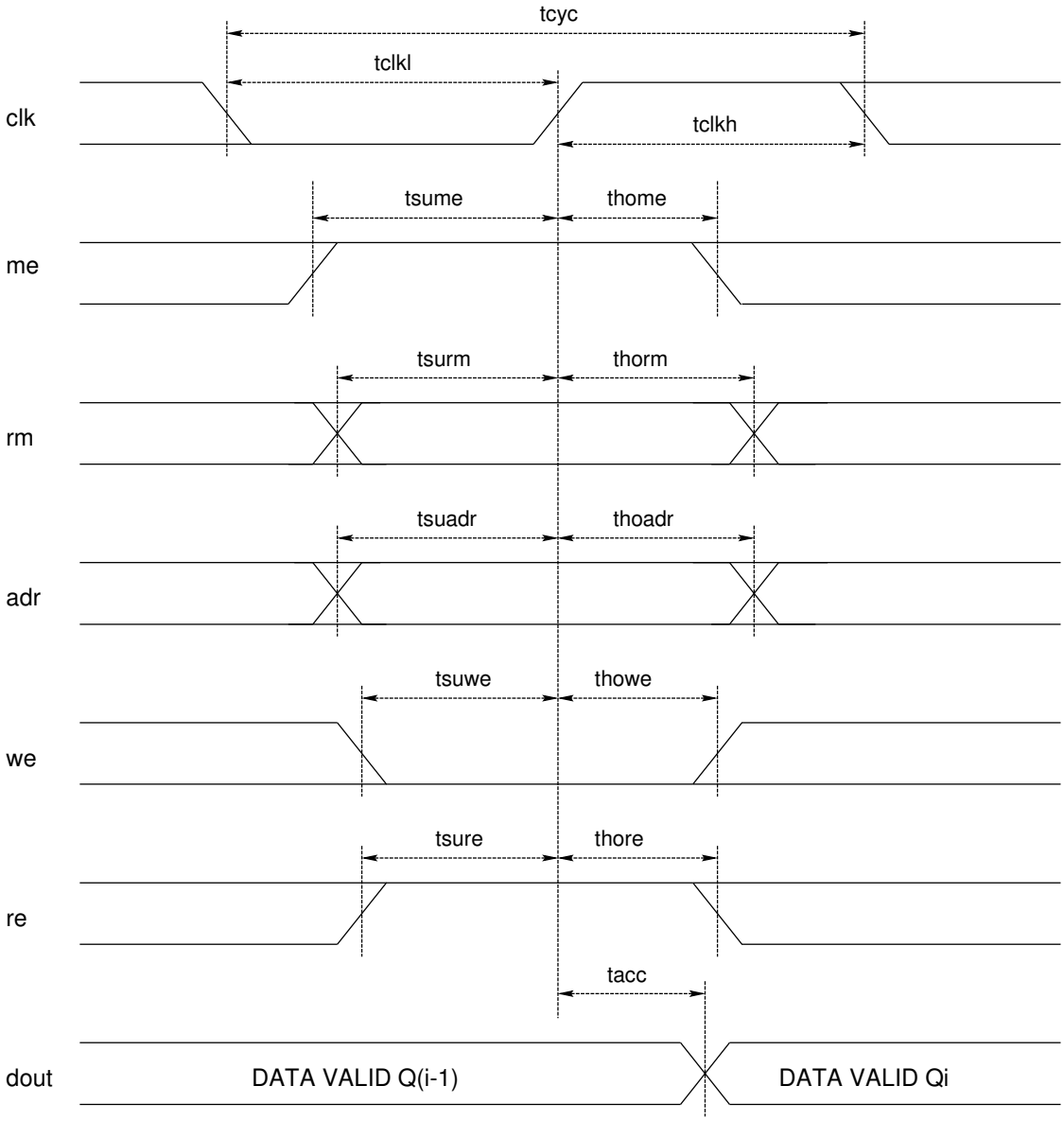


Write Mode : Timing Diagram

Read Mode:

For the read mode the ***me*** signal must be high, ***re*** must be high and ***we*** must be low (simultaneous read/write is forbidden). In the read mode the ***adr*** inputs are set up and decoded to select the desired word (row and column). When ***clk*** changes from low to high the internal timing of the ram starts and some time later the data is latched onto the ***dout*** bus. Read operation can be done on a byte, using ***re[3:0]*** read enable masks:

re[3]	active high : read operation dout[31:24]
re[2]	active high : read operation dout[23:16]
re[1]	active high : read operation dout[15:8]
re[0]	active high : read operation dout[7:0]



Read Mode : Timing Diagram

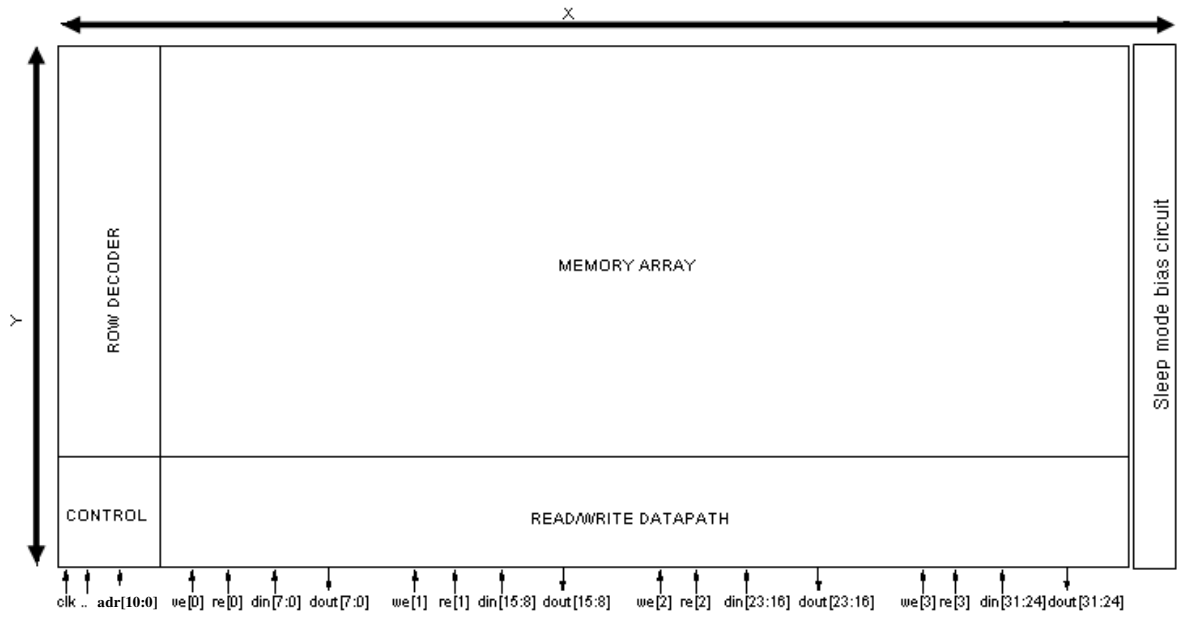
OPERATING MODE TRUTH TABLE

MODE	INPUTS					OUTPUTS
	clk	me	we[3:0]	re[3:0]	din[]	dout[]
Disabled	X	L	X	X	X	Q-1
Idle	L	H	X	X	X	Q-1
Idle	H	H	X	X	X	Q-1
Read	L-H	H	L:L:L:L	H:H:H:H	X	$Q_3/Q_2/Q_1/Q_0$
Read	L-H	H	L:L:L:L	H:H:H:L	X	$Q_3/Q_2/Q_1/Q_0$-1
Read	L-H	H	L:L:L:L	H:H:L:H	X	$Q_3/Q_2/Q_1$-1/Q_0
Read	L-H	H	L:L:L:L	H:H:L:L	X	$Q_3/Q_2/Q_1$-1/Q_0-1
Read	L-H	H	L:L:L:L	L:L:H:H	X	Q_3/Q_2-1/Q_1/Q_0
Read	L-H	H	L:L:L:L	H:L:H:L	X	Q_3/Q_2-1/Q_1/Q_0-1
Read	L-H	H	L:L:L:L	H:L:L:H	X	Q_3/Q_2-1/Q_1-1/Q_0
Read	L-H	H	L:L:L:L	H:L:L:L	X	Q_3/Q_2-1/Q_1-1/Q_0-1
Read	L-H	H	L:L:L:L	L:H:H:H	X	Q_3-1/$Q_2/Q_1/Q_0$
Read	L-H	H	L:L:L:L	L:H:H:L	X	Q_3-1/$Q_2/Q_1/Q_0$-1
Read	L-H	H	L:L:L:L	L:H:L:H	X	Q_3-1/Q_2/Q_1-1/Q_0
Read	L-H	H	L:L:L:L	L:H:L:L	X	Q_3-1/Q_2/Q_1-1/Q_0-1
Read	L-H	H	L:L:L:L	L:L:H:H	X	Q_3-1/Q_2-1/Q_1/Q_0
Read	L-H	H	L:L:L:L	L:L:H:L	X	Q_3-1/Q_2-1/Q_1/Q_0-1
Read	L-H	H	L:L:L:L	L:L:L:H	X	Q_3-1/Q_2-1/Q_1-1/Q_0
Write	L-H	H	H:H:H:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	H:H:H:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	H:H:L:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	H:H:L:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:L:H:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	H:L:H:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	H:L:L:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	H:L:L:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:H:H:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:H:H:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:H:L:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:H:L:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:L:H:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:L:H:L	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:L:L:H	L:L:L:L	Data-in	Q-1
Write	L-H	H	L:L:L:L	L:L:L:L	Data-in	Q-1
No operation	L-H	H	L:L:L:L	L:L:L:L	X	Q-1

Note :
Q represents dout[31:0] ; Q_3 ⇔ dout[31:24]; Q_2 ⇔ dout[23:16]; Q_1 ⇔ dout[15:8]; Q_0 ⇔ dout[7:0]
-1 means the previous read values

PHYSICAL PARAMETERS

Estimated SRAM area	X (mm)	Y (mm)	Area (mm^2)
TPE_RAM_1536X8X4HS_AT110N_N1	0.3447	0.3805	0.13116



Memory Floorplan

Memory layout information:

- Bit-lines are designed using vertical metal2 lines
- Word-lines are designed using horizontal metal3 lines
- Power rails (mesh topology) are designed using horizontal metal3 lines

Power/Ground Connection Guideline:

- All power and ground pins MUST be connected to VDD and GND, respectively.
- Fully populate the intersections of power rails and power pins with VIAs.
- Special attention should be made to the power connections close to the bottom of the memory array to power the IO buffers.
- Multiple connections along each power pin are recommended to further reduce IR drop.
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ELECTRICAL PARAMETERS

DESCRIPTION	MIN	TYP	MAX1	MAX2	UNIT
Process Corner	Fast	Nom	Slow	Slow	-
Supply Voltage	1.40	1.33	1.20	1.08	V
Temperature	-40	25	105	105	°C (junction)

TIMING/POWER

Slopes are measured from 10% to 90% of the power supply. All timings are measured from a logic threshold at 50% of the power supply. Timings and Power consumptions are evaluated at three timing conditions to produce three timing libraries with min, typ and max case timings.

NAME	DESCRIPTION	MIN	TYP	MAX1	MAX2	UNIT
tcyc	Cycle time	2.78	3.42	4.82	5.67	ns
tclkh	Minimum pulse high for clk	1.59	2.22	3.63	4.34	ns
tclkl	Minimum pulse low for clk	1.19	1.19	1.19	1.33	ns
tacc	Access time	1.56	2.19	3.58	4.30	ns
taciso	iso to dout go low delay	0.00	0.00	0.00	0.00	ns
tsudin	Data-in setup time	0.22	0.22	0.22	0.22	ns
thodin	Data-in hold time	0.35	0.40	0.49	0.55	ns
tsuadr	Address setup time	1.32	1.65	2.44	2.45	ns
thoadr	Address hold time	0.38	0.40	0.42	0.44	ns
tsume	Memory enable setup time	0.31	0.33	0.40	0.42	ns
thome	Memory enable hold time	0.22	0.22	0.22	0.22	ns
tsuwe	we setup time	0.22	0.22	0.22	0.22	ns
thowe	we hold time	0.34	0.39	0.49	0.54	ns
tsure	re setup time	0.22	0.22	0.22	0.22	ns
thore	re hold time	0.34	0.38	0.48	0.54	ns
tsurm	rm setup time	0.55	0.55	0.55	0.61	ns
thorm	rm hold time	1.19	1.19	1.19	1.32	ns
tslp	Get in sleep mode time	10.00	10.00	10.00	10.00	ns
toslp	Out of sleep mode time	100.00	100.00	100.00	100.00	ns
Pread	Typical read power	55.98	47.13	35.71	28.53	uW/MHz
Pwrite	Typical write power	54.21	46.02	35.18	28.32	uW/MHz
Ioff	Leakage current	899.80	1767.30	6021.20	5599.20	nA

Ioff (with S.B.)	source bias	251.52	771.03	3601.20	3303.40	nA
Ioff (with US.B.)	Ultra source bias	-	-	-	-	nA
Ioff (with US/D.B.)	Ultra source/drain bias	-	-	-	-	nA
Ioff (with S/D.B.)	source/drain bias	172.02	628.47	3171.40	2900.30	nA
Ioff (with D.B.)	drain bias	742.48	1539.30	5394.60	5007.50	nA
Ioff (with ISO)	ISO (Ultra source/drain bias)	-	-	-	-	nA
Maxload	Maximum output load	0.55	0.55	0.55	0.55	pf

Note : bias voltage for data retention VddDR=0.50V,