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Design av GaN basert effektforsterker

i aktiv X-bånd radars TX/RX-modul

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Elektronisk systemdesign og innovasjon
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Dedication

I would like to thank the people at FFI for their help realizing my plans for this thesis. The things shown in this thesis would not have been possible without Ottar Opland, Ulv Skafle and Geir Zakariassen. This thesis would have the same quality without the help of my advisor Asgeir Nysæter. I would also like to thank Morten Olavsbråten for designing bias tees used in the measurements. Finally I would like to thank NTNU for the learing experience I have had the last five years

-Morten Gunnerud

Summary

Four Power Amplifier designs have been designed based on a CREE bare die transistor, for use in an X-band active electronically scanned array radar. As the signal used in the system is a 50 MHz orthogonal frequency division multiplexing(OFDM) signal, it was important for the power amplifier design to have as good efficiency and linearity as possible. It was also desired to have at least 50W of output power. A big issue for the design was the possibility of odd-mode oscillations due to the large periphery of the transistor. To prevent this, four feeding networks were designed using well-known combiner/divider topologies. The feeding networks were measured, and the two with the best characteristics were used as the base for the power amplifier designs. Unfortunately, measurements of the finished power amplifier designs were inferior to the simulations. Some of the possible reasons for this is the production process variations and the transistor model used in simulations not beeing able to characterize each input and output port of the transistor.

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Abbreviations

Al	=	Aluminum
Cu	=	Copper
CuW	=	Copper-Molybden
Mil	=	milli-inch
HPA	=	High Power Amplifier
X-band	=	8-12GHz
GaAs	=	Gallium Arsenide
GaN	=	Gallium Nitride
ADS	=	Agilent Advanced Design System[6]
PNA	=	Programmable Network Analyzer
PA	=	Power Amplifier
RFPA	=	Radio Frequency Power Amplifier
IMD	=	Intermodulation Distortion
ACPR	=	Adjacent Channel Power Ratio
IF	=	Intermediate Frequency
RF	=	Radio Frequency
DAC	=	Digital-to-Analog Converter
ADC	=	Analog-to-Digital Converter
T/R	=	Transciever/Reciever
MAG	=	Maximum Available Gain
MIMO	=	Multiple Input-Multiple Output
OFDM	=	Orthogonal Frequency-Division Multiplexing
BLC	=	Branch-Line hybrid Coupler
MIM	=	Metal-Insulator-Metal
MMIC	=	Monolithic Microwave Integrated Circuit
MIMO	=	Multiple Input Multiple Output
AESA	=	Active Electronically Scanned Array

Chapter 1

Introduction

The Norwegian Defense Research Establishment (FFI) conducts different research projects related to future Norwegian Navy needs. This master thesis is a part of a research project to build an active, phase controlled radar for research on MIMO(Multiple Input-Multiple Output) / OFDM (Orthogonal Frequency-Division Multiplexing) radar processing algorithms.

The radar system will consist of 64 transcievers, which are connected to the 8×8-array antenna shown in figure 1.1.

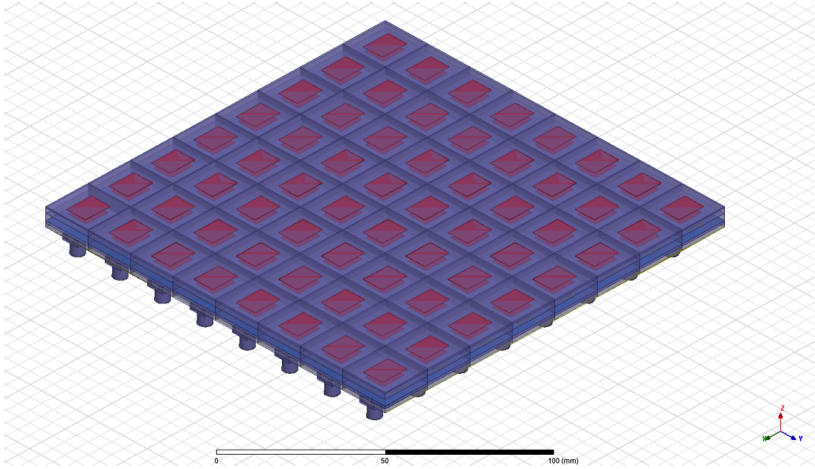


Figure 1.1: The layout of the 8×8 patch-element, aperture coupled active electronically scanned array(AESA)-antenna used in the radar system

The system overview of a single tranceiver is given in figure 1.2, where the digital Intermediate frequency(IF) signal is digital-to-analog converted and upconverted to radio frequency(RF). In the transceiver/receiver(T/R) module, the signal is amplified in the transmitter and sent to the antenna. The reflected signal from the target is received by the antenna and the receiver part of the T/R-module amplifies the signal before downconversion and sampling in the analog-to-digital converter(ADC).

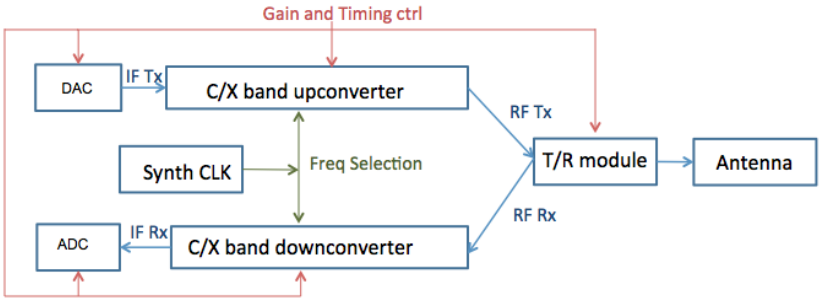


Figure 1.2: A block diagram of the transceiver part of the radar system, including DAC, upconverter, T/R-module, downconverter, ADC and antenna.

This thesis will discuss the design of a Gallium Nitride(GaN) Power

Amplifier(PA) which will be used in the T/R-module of the radar system shown in figure 1.3. The desired output power is 50W(47dBm), and due to the large amount of power the reflection coefficient must be low, especially at the output, in order to reduce the stress on the components connected to the amplifier.

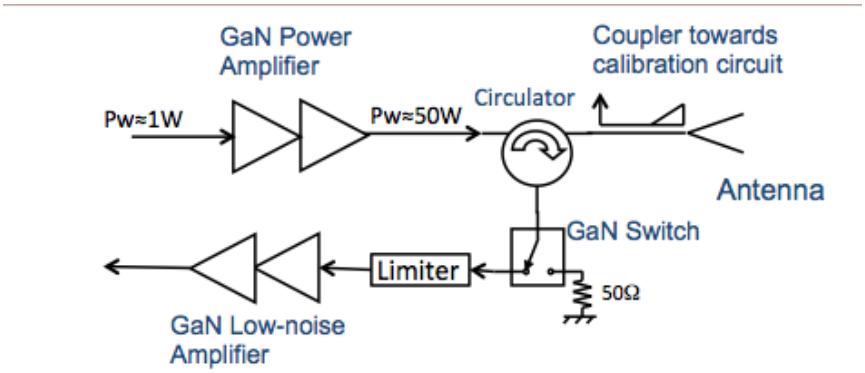


Figure 1.3: A block diagram of the transmitter and receiver module of the radar, including front-end amplifier, circulator, antenna, switch and low noise receiver amplifier.

One of the main problems that will be discussed in this thesis is the use of large periphery transistors, such as the transistor used in this design. It will be seen that special measures must be taken in order to ensure maximum power transfer and prevent odd mode oscillations. In this design four power splitting techniques were investigated in the project thesis (design procedure can be seen in Appendix B), and this master thesis will utilize the feeding networks in four power amplifier designs. The wanted specifications for the power amplifier design are described in table 1.1.

It was desired to have a 500MHz bandwidth with a center frequency of 8.25GHz, in order to have possibility of changing the center frequency of the intended 50MHz signal. Special considerations should be taken due to the high power levels of the transistor. Other wanted specifications are qualities typically desired by power amplifiers.

Table 1.1: Specifications for the PA design

Description	Requirements
Frequency band	8-8.5 GHz
Drain Voltage (V_D)	48V
Input VSWR	$< 1:2$
Output VSWR	$< 1:1.5$
Stability	Unconditionally stable
Maximum Output Power P_{out} (@30-33dBm in)	50W(47dBm)
Linearity	Maximize
Power Added Efficiency	Maximize
3rd order Intermodulation Distortion	Minimize

1.1 Outline

This Master thesis is structured as follows:

1st Chapter: Introduction introduces the thesis, what is the main objectives, and the PA's place in a final radar-system.

2nd Chapter: Theory gives a short presentation to all theoretical knowledge that is needed to understand the system and choices done later in the thesis. It also includes references to get a more thorough presentation of the subjects.

3rd Chapter: Device Technology gives an overview of the components and materials used and considerations made in choosing them.

4th Chapter: Design and Measurements of Feeding Networks gives a small presentations of the feeding networks who are more thoroughly presented in Appendix B. Then realization and measurements of a test card containing the feeding networks are presented. The results of the measurements are presented, compared to simulation results, and discussed.

5th Chapter: Design presents the design of the power amplifier designs based on the feeding networks that was measured in chapter 4.

6th Chapter: Measurements and Results presents measurements of a test card, and the results from these measurements are compared with simulation results.

7th Chapter: Discussion discusses the design, measurements, and results of the finished power amplifier designs.

8th Chapter: Conclusion concludes the discussion and hence the report, and gives some pinpoint as to what can be improved in the next generation of this power amplifier design.

Chapter 2

Theory

2.1 Wave Transmission

The voltage and current of travelling waves at a posititon z on a transmission line are a solution of the telegrapher's equation[44], and are given by

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.1}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}. \tag{2.2}$$

V_0^+ and I_0^+ are the amplitude of the forward travelling voltage and current wave, V_0^- and I_0^- are the amplitude of the backward travelling voltage and current wave, respectively. $e^{-\gamma z}$ represents the wave propagation in +z direction, $e^{\gamma z}$ represents the wave propagation in -z direction, and γ is the complex propagation constant given by

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}. \tag{2.3}$$

From Appendix F the characteristic impedance of the transmission line is defined as

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-}. \tag{2.4}$$

where R and L are the series resistance$[\Omega/\mathrm{m}]$ and inductance$[\mathrm{H}/\mathrm{m}]$ per unit length, while G$[\mathrm{S}/\mathrm{m}]$ and C$[\mathrm{F}/\mathrm{m}]$ are the shunt conductance and capacitance per unit length for the transmission line. ω is the angular frequency in Hz.

A load with impedance Z_L is connected to a transmission line with characteristic impedance Z_0. The reflection coefficient Γ is derived in Appendix F and is the relationship between the transmitted and reflected voltage wave amplitude at the load. This is given by

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{2.5}$$

The Voltage Standing Wave Ratio(VSWR) is another way to describe the ratio between the transmitted and reflected wave. It is widely used in data sheets for many RF components, and gives a indication on how closely matched a device is to the system impedance. The definition of the VSWR in Appendix F is given by

$$\mathrm{VSWR} = \frac{V_{\max}}{V_{\min}} = \frac{1 + |\Gamma|}{1 - |\Gamma|}. \tag{2.6}$$

If $Z_L = Z_0$ then all the power will be delivered to the load, and the $VSWR = 1$. On the other hand, If Z_L is different from the system impedance waves will be reflected at the load. This could be prevented by placing an impedance matching network which eliminates the reflections caused by the impedance mismatch of the load. By doing this no waves are reflected to the signal source, although there will be an increase in reflections between the load and the matching network[38, p. 55].

2.2 S-Parameters

The scattering parameters[19, pp. 23-31][21] are the most used parameters to characterize networks at microwave frequencies. The scattering parameters use the magnitude and phase of the incoming and reflected voltage waves rather than measuring the total voltages and currents at the ports, which makes them better suited for measurements at high frequencies. For a N-port network, the S-parameter S_{ij} is given by

$$S_{ij} = \frac{V_i^-}{V_j^+}|_{V_k^+=0 \ for \ k \neq j}. \tag{2.7}$$

V_i^+ is the outgoing wave at port i, and V_j^- is the incident wave at port j. Thus S_{ii} is the reflection coefficient (2.5) and S_{ij} is the transmission coefficient from port j to i. It should be stated that for a reciprocal network, $S_{ij} = S_{ji}$.

The S-matrix for the 2-port network shown in figure 2.1 is defined as

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.8}$$

where a_n is the amplitude for of the indicent wave at port n, and b_m is the amplitude of the reflected wave at port m.

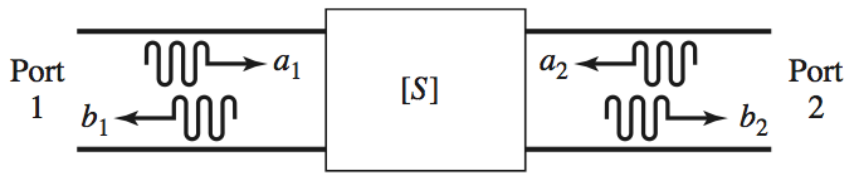


Figure 2.1: A two port network showing incident and reflected waves. [39, p. 195]

2.3 Matching of Active Elements

The input- and output impedance of a transistor amplifier should be matched to the characteristic impedance of the system. By adding a matching network consisting of lumped or distributed elements the input and output impedance seen looking towards the transistor can be altered to achieve optimum noise figure, gain, PAE or output power. This is often necessary due to the fact that the transistor rarely is matched to the system impedance.

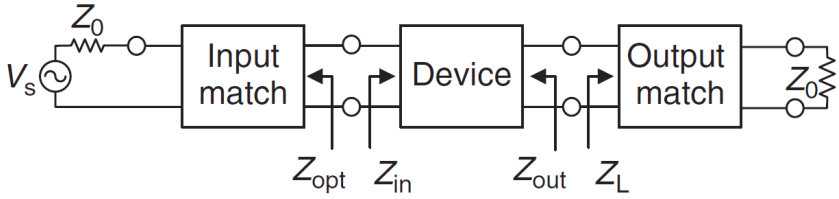


Figure 2.2: An active two port network.[19, p. 51]

The two-port power gains for the active two-port network[33] shown in figure 2.2 are given by

$$G = \frac{P_{load}}{P_{delivered\ from\ source}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{\left(1-|\Gamma_{in}|^2\right)|1-S_{22}\Gamma_L|^2}, \tag{2.9}$$

$$G_A = \frac{P_{available\ in\ network}}{P_{available\ from\ source}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)}{|1-S_{11}\Gamma_s|^2\left(1-|\Gamma_{out}|^2\right)}, \tag{2.10}$$

$$G_T = \frac{P_{load}}{P_{available\ from\ source}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_s\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2}. \tag{2.11}$$

Where G is the power gain, G_A is the available gain(often called maximum available gain(MAG)) and G_T is the transducer power gain, which is

the actual amplification of the signal from the source at the load. Γ_s and Γ_L are the reflection coefficients at the source and load respectively, while Γ_{in} is the input reflection coefficient and Γ_{out} is the output reflection coefficient given by

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}, \tag{2.12}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}. \tag{2.13}$$

The expressions for G,G_A,G_T,Γ_s,Γ_L,Γ_{in} and Γ_{out} are derived in appendix G.

As the gains of an active two-port is dependent on the matching networks, transforming the source- and load impedance through the input- and output matching networks of the transistor changes the behaviour of the two-port.

To match for the highest possible transducer power gain, Γ_s should be equal to Γ_{in}^*, and Γ_L should be set equal to S_{22}^*. As Γ_{in} changes with Γ_L, matching becomes an iterative procedure.

A power amplifier can ideally be seen as a unilateral circuit, meaning there will be no backwards transmission, but in the reality S_{12} will never be equal to zero. Therefore matching of a PA can be complex, as the best possible input network for gain changes as the output network changes and vice versa, as can be seen from (2.12) and (2.13).

There are a large number of different methods to do impedance matching, and important factors in choosing the right one is bandwidth, frequency response, complexity and ease of implementation[19, p. 149].

It should be noted that the matching for maximum small signal gain often will result in lower maximum output power and a less linear characteristic than other types of matching procedure, as e.g. doing load-pull measurements[19, pp. 113-121] and design for maximum output power or efficiency.

2.4 GaN HEMT Technology

Gallium-Nitride High Electron-mobility transistors(GaN HEMTs)[37] are the latest addition to high-power Radio Frequency(RF)-transistors, but have now become well-established as a mainstream technology. The usage of GaN on Silicon Carbide(SiC) substrate has enabled transistors with larger power densities and breakdown voltages than earlier. This make them ideal for high-power and high efficiency designs. The development of the technology started in the 1990s, and transistors have been available as commercial off-the-shelf products since 2005 [37, p.1764]. A cross section of a typical GaN HEMT Monolithic Microwave Integrated Circuit(MMIC) process is shown in figure 2.3. In addition to a transistor, a metal-insulator-metal (MIM) capacitor, a resistor, and substrate vias are utilized to make versatile, high-performance MMICs.

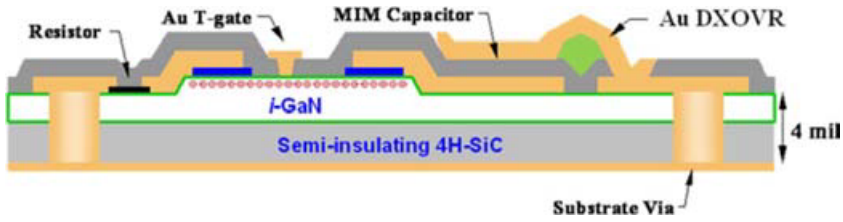
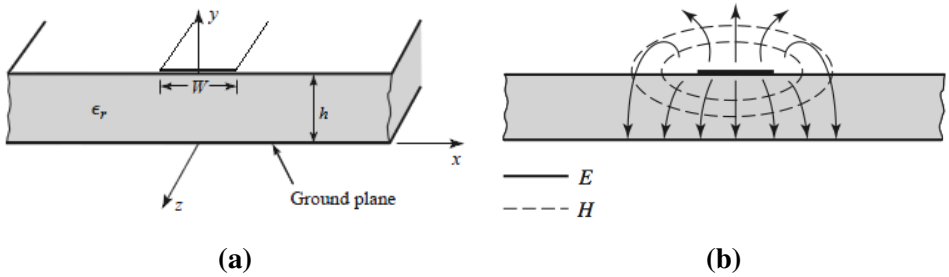


Figure 2.3: Cross section of a GaN HEMT MMIC process as shown in [37, p. 1765] including resistor, MIM capacitor and substrate via.

2.5 Microstrip Lines

Microstrip lines[18],[39, pp. 147-153] are often used as transmission lines in passive microwave circuits as they are simple and cheap to make, integrate easy with lumped components and chip devices, and take up little space. A microstrip consists of a conductor strip on top of a dielectric plate with dielectric constant ϵ_r, and a ground plane conductor sheet on the bottom as shown in figure 2.4a.



(a) **(b)**

Figure 2.4: The geometry(a) and electric- and magnetic field lines(b) of a microstrip transmission line[39, p. 147]

From figure 2.4b it can be seen that the electric and magnetic field of the microstrip will propagate partially through the dielectric, and partially through air, which will result in a quasi-TEM(Transverse electromagnetic)-mode [40, pp. 58-59]. Therefore, the effective dielectric constant ϵ_{eff} will be different from ϵ_r, and an empirical expression for it is given by [18, p.175]

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}(1 + \frac{1}{\sqrt{1 + 12(h/W)}}) \tag{2.14}$$

for $W/h \geq 1$, and

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}(1 + \frac{1}{\sqrt{1 + 12(h/W)}} + 0.04(1 - W/h)^2) \tag{2.15}$$

for $W/h \leq 1$ [18, p.175].

W is the width of the conductor strip and h is the height of the dielectric sheet as denoted in figure 2.4. It can be observed that the value of ϵ_{eff} will be $1 < \epsilon_{eff} < \epsilon_r$. The expressions in (2.14) and (2.15) has less than 1% maximum relative error for $0.05 \leq W/h \leq 20$ and $\epsilon_r \leq 16$[27, p. 269].

The characteristic impedance of the microstrip line is given by

$$Z_0 = \frac{60}{\sqrt{\epsilon_{eff}}} ln(8h/W + 0.25W/h) \tag{2.16}$$

for $W/h \leq 1$, and

$$Z_0 = \frac{120\pi/\sqrt{\epsilon_{eff}}}{W/h + 1.393 + 0.667ln(W/h + 1.444)} \tag{2.17}$$

for $W/h \geq 1$ [27].

These expressions have a maximum relative error of 0.8% for $0.05 \leq W/h \leq 20$ and $\epsilon_r \leq 16$[27, p. 269]. From the expressions stated above it can be noted that the characteristic impedance increases with decreasing width, and a line with impedance Z_0 with large ϵ_{eff} will have smaller width than a line with the same impedance and small ϵ_{eff}. The resulting wavelength for a electromagnetic wave in a microstrip is shorter that it is in air as the wavelength decreases with increasing dielectric constant. This is given by

$$v_p = \frac{c}{\sqrt{\epsilon_{eff}}} \tag{2.18}$$

$$\lambda_g = \frac{v_p}{f}, \tag{2.19}$$

where v_p is the phase velocity, c is the speed of light and f is the frequency. λ_g is the resulting wavelength on the microstrip line.

The loss in microstrip lines is dependent on both the conductor loss and the dielectric loss. Conductor loss decreases with increasing substrate thickness or characteristic impedance, and increases with the square root of frequency[18, p. 178], while the dielectric loss increases with increasing loss tangent[22, p. 342].

$$\tan\delta \cong \frac{\sigma}{\omega\epsilon_{eff}}, \tag{2.20}$$

where σ is the conductivity of the substrate.

Of the two losses, the conductor loss is often dominant. The peak power handling of the microstrip is poor, and is difficult to calculate accurately[18, p. 182]. The power handling limitations is related to the temperature rise

of the conductor and substrate, and therefore better power capability is obtained using a substrate with low loss tangent and large thermal conductivity.

2.6 Efficiency

The efficiency is a cruicial parameter for many electronic circuits, and this is definitely the case for power amplifiers. With power levels of tens, or even hundereds of watts, the amount of power converted to heat can be very large, and may cause problems and the need for extra design conciderations. The two most common ways of defining the efficiency of a power amplifier is drain efficiency and Power Added Efficiency (PAE). Drain efficiency is the ratio of RF output power to input DC power, given by[19, p.39]

$$\eta_D = \frac{P_{out}}{P_{DC}}, \tag{2.21}$$

where η_D is the drain efficiency, P_{out} is the output power and P_{DC} is the direct current power.

PAE is the most used figure of merit concerning efficiency. The PAE takes, in difference to the drain efficiency, the RF input power into account. The PAE is defined by[19, p.39]

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}, \tag{2.22}$$

where P_{in} is the input power.

The difference between drain efficiency and PAE decreases with increasing gain, but a general rule of thumb is that the difference is significant when the gain is lower than $10\ dB$.

2.7 Radio Frequency Power Amplifiers

Radio frequency power amplifiers(RFPAs or PAs) are commonly used in radio transmitters to amplify a signal before it's sent to the transmitting antenna. Their topology consist of an amplifing transistor and circuitry to make the PA as good as possible for parameters like efficiency, gain, output power and intermodulation effects. PA's are small signal devices, but often with some, or considerate, nonlinearities. This makes small signal simulations useful, but when the transistor operates close to saturation other types of analysis is needed to be able to show the amplifier nonlinearities.

2.7.1 Weakly Nonlinear Effects

A matched PAs nonlinearities can be modeled by a power series, as shown in (2.23), where v_o is the output AC-voltage, v_i is the input AC-voltage, and a_n are coefficients.

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + ... + a_n v_i^n \tag{2.23}$$

The power series is an easy way of modeling the low level nonlinear effects, but have limitations as it does not allow any difference in timing of the output components. An expansion of the power series, called the Volterra series, takes phase-difference into account, and hence is a much stronger formulation. The coefficients of the power series are very sensitive to changes in the matching networks and DC operating point, but can still be a useful for characterizing low level nonlinear effects as e.g. intermodulation distortion at levels lower than 30 dBc[23, p. 6]. When the PA approaches its $1\ dB$ compression point, the nonlinearities become stronger and other effects as e.g. the clipping of the signal start to dominate, and these effects need to be modeled more exact.

2.7.2 Strongly Nonlinear Effects

When a transistor is operated close to its maximum output power, strong distortion of the signal will occur. This is due to the limitations of the

transistor, where the drain current reaches cut-off, and a further voltage increase on the gate will not result in any rise in the drain current, as shown in figure 2.5

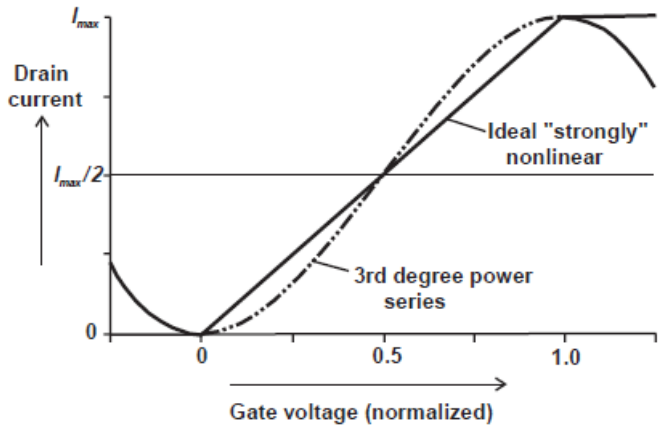


Figure 2.5: Ideal(solid line) and realistic(dashed line) I/V characteristic of a FET transistor.[23, p. 6]

In contrast to the weakly nonlinear effect, the strongly nonlinear effects can be modeled over the full operating range, and if the gate voltage between cutoff and saturation is normalized to a range between 0 to 1, it can be shown [23, p.7] that a model for the more realistic drain current shape shown as the dashed line in figure 2.5 can be expressed as

$$I_d = +3V_g^2 - 2V_g^3, \tag{2.24}$$

where I_d is the drain current and V_g is the gate voltage. This model does not model the fully cutoff and saturation regions without adding many higher order terms to (2.24), so a different model called the ”strong-weak” model can be used by combining the weakly nonlinear effects with suitable if-statements for the cutoff and saturation regions. This model is shown in figure 2.6

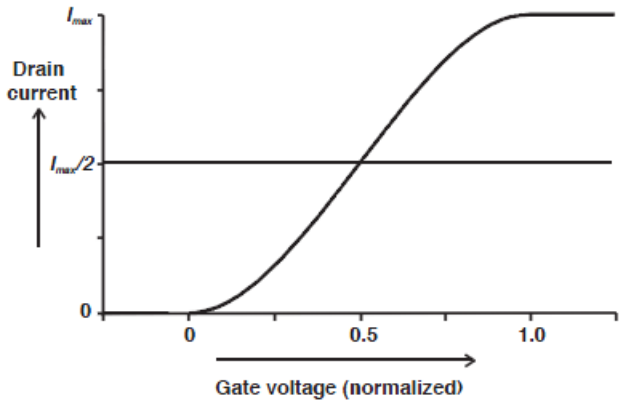


Figure 2.6: The strong-weak model for FET-transistor characterisation plotted with drain current vs. normalized gate voltage[23, p. 8]

2.7.3 Intermodulation Distortion

For a single tone the output signal of a PA is distorted as discussed in 2.7.1 and 2.7.2. For two tone or wideband signals however, Intermodulation Distortion(IMD)[28] comes into play due to mixing of the frequency components. The IMD signal components are much closer to the signal band than the harmonic components, and thus they are more problematic. If a two tone signal is put into the power series in (2.23) the result is

$$v_o = a_1 V_0(\cos(\omega_1 t) + \cos(\omega_2 t)) + a_2 V_0^2(\cos(\omega_1 t) + \cos(\omega_2 t))^2 + a_3 V_0^3(\cos(\omega_1 t) + \cos(\omega_2 t))^3 \ldots \quad (2.25)$$

where v_o is the output voltage, a_n are coefficients, V_0 is the input voltage amplitude, while ω_1 and ω_2 are the angular frequency of the two tones. The resulting output for the tree first terms become

$$
\begin{aligned}
v_o &= a_1 V_0(\cos(\omega_1 t) + \cos(\omega_2 t)) \\
&+ \frac{1}{2} a_2 V_0^2 (1 + cos(2\omega_1 t)) + \frac{1}{2} a_2 V_0^2 (1 + cos(2\omega_2 t)) \\
&+ a_2 V_0^2 \cos((\omega_1 - \omega_2)t) + a_2 V_0^2 \cos((\omega_1 + \omega_2)t) \\
&+ a_3 V_0^3 (\frac{3}{4} \cos(\omega_1 t) + \frac{1}{4} \cos(3\omega_2 t)) + a_3 V_0^3 (\frac{3}{4} \cos(3\omega_2 t) + \frac{1}{4} \cos(\omega_1 t)) \\
&+ a_3 V_0^3 [\frac{3}{2} \cos(\omega_2 t) + \frac{3}{4} \cos((2\omega_1 - \omega_2)t) + \frac{3}{4} \cos((2\omega_1 + \omega_2)t) \\
&+ a_3 V_0^3 [\frac{3}{2} \cos(\omega_1 t) + \frac{3}{4} \cos((2\omega_2 - \omega_1)t) + \frac{3}{4} \cos((2\omega_2 + \omega_1)t).
\end{aligned}
\tag{2.26}
$$

In (2.26) the IMD products are seen at the frequencies of $N\omega_2 - M\omega_1$, and the odd-order IMD products are placed close to the frequency of the carrier signals. The closest IMD products are thus the 3rd order IMD products. A sketch of the IMD products can be seen in figure 2.7. The IMD products are denoted in dBc, meaning decibels relative to the carrier signal.

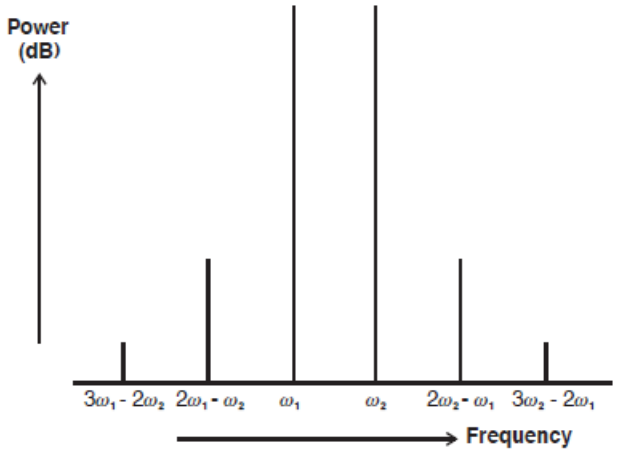


Figure 2.7: Two tone signal and in-band intermodulation distortion products[23, p. 235].

For modulated signals there is need for an other definition of the distortion effects. The most used definition is Adjacent Channel Power Ratio(ACPR) which is also denoted in dBc and compares the power spectral

density in the signal band with the power spectral density in the neighbouring channels.

2.7.4 Transistor Models

Today computer aided design-tools are extensively used in amplifier design. Manufacturers and foundries give S-parameter files and transistor models for their products. These help make the design procedure easier, and increase the amount of first time pass designs. The transistor models are often based on an equivalent circuit model, as the example shown in figure 2.8, where the parameters are extracted by doing measurements. These models are valid for a large range of biases and operating temperatures. The models also include non-linearities in drain- and gate current, voltage variations caused by parasittic capacitances, drain-source breakdown, self heating and other effects. These models have shown to produce accurate results for both small signal and large signal analysis, and also to accurately model intermodulation effects[41].

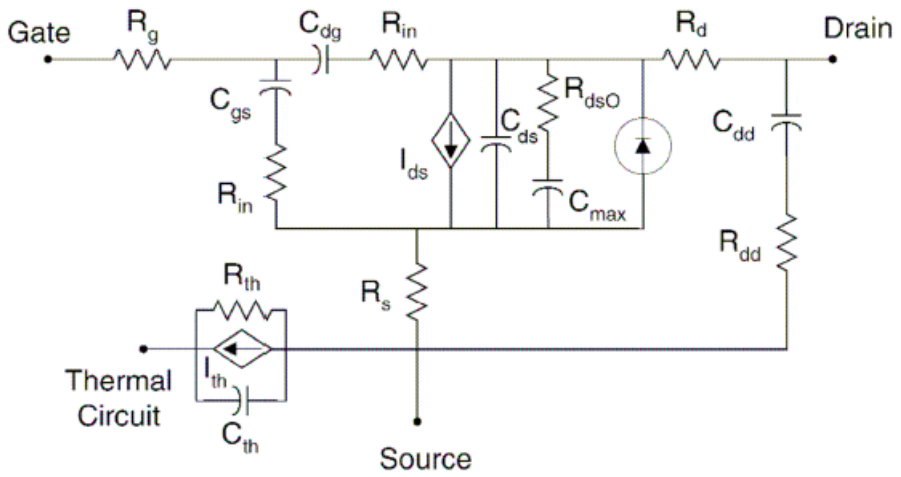


Figure 2.8: An equivalent circuit model for Cree's GaN HEMT transistors, including modeling of self heating and drain-source breakdown. Schematic from [41, p. 7]

2.7.5 Class A Amplifier

RFPAs are often classified after their drain current duty cycle, meaning how much of the gate voltage is above the cut-off threshold of the amplifier and hence reproduced in the drain current. Class A Amplifiers are often used as transmission amplifiers in systems where linearity is crucial. Especially in systems with amplitude modulated signals, or a combination of both amplitude and phase modulation, class A amplifiers are wanted. By biasing the transistor with a drain current equal to $I_{\max}/2$(seen in figure 2.9) the amplifier can drive the signal for the entire duty cycle even close to compression . By doing this the amplifier will be highly linear, but a class A amplifier can not have a theoretical efficiency above 50% [23, p. 24]. Low-noise amplifiers are often biased as class A.

2.7.6 Class AB Amplifier

A class AB amplifier is biased with a lower bias current than a class A amplifier. By having a conduction angle between 180-360 degrees, as e.g. in figure 2.9, the signal will be cut when below threshold, and thus create more unlinearities than the class A amplifier, but with possibilites to obtain a higher efficiency. Class AB amplifiers have a theoretical maximum efficiency between 50% and 78.5%[19, p. 186]. The class AB amplifier is a nonlinear amplifier as the concuction angle is a function of the input signal. At lower power levels the class AB amplifier will behave as Class A amplifier, but when the input power is increased the conduction angle will decrease. By running an amplifier in the mid-AB conduction angle region the fundamental RF output power is a few tenths dB higher than class A or class B[23, p. 46]. Class AB are often used as transmitting amplifiers.

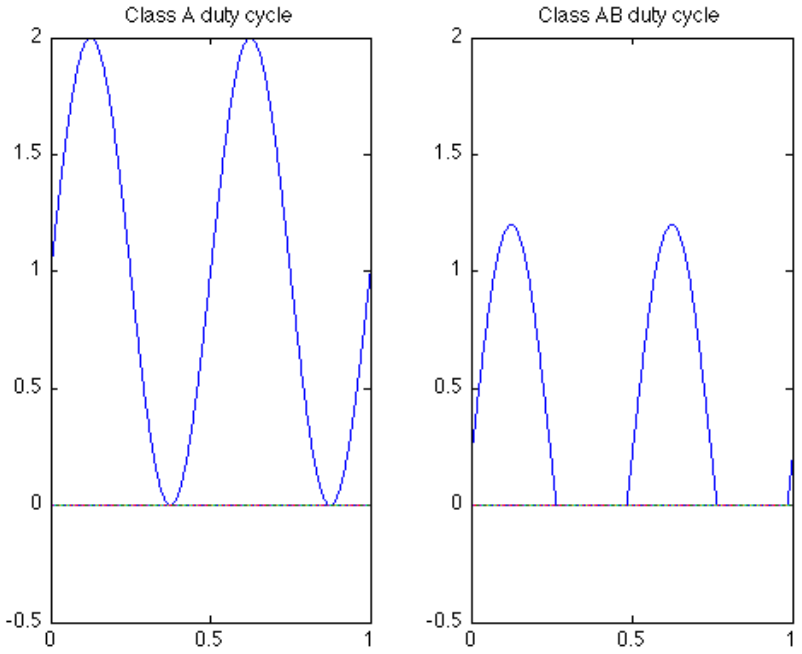


Figure 2.9: Drain current duty cycles for class A(left) and AB(right) RFPAs.

2.7.7 Class F Amplifier

The standard class AB rectifed sine waveform will have an overlap between current and voltage which is nonideal with regard to efficiency. An optimal drain voltage would be a square wave containing only odd harmonics, giving no overlap and ideally 100% efficiency. The Class F amplifier[23, pp. 143-155] is a theoretical approach to do this, by adding open load-termination for the odd harmonics and short load-termination for even harmonics. This will cause the voltage waveform to become a square wave, and the current will become a rectified sinusoidal waveform as shown in figure 2.11. By doing this type of harmonic termination, as can be seen from figure 2.10, the peak voltage is lowered. This allows higher output power before the saturation level is reached. In practice this type of termination is often only added up to the 3^{rd} harmonic, achieving a maximum theoretical efficiency of 90.7%. The ideal amount of third harmonic added

is either $1/9 \times V_1$ which will give the maximum flat voltage waveform, or $1/6 \times V_1$ which will give the most effective voltage waveform.

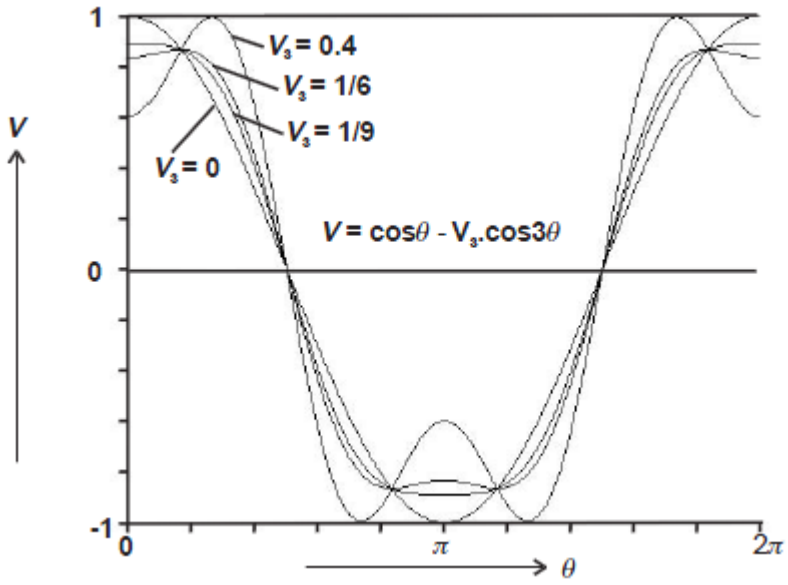


Figure 2.10: Output waveform of a Class F with a notated amount of third harmonic (V_3) relative to the main signal (V_1). Figure from [23, p.143]

Adding of odd-harmonic open load-terminations causes the edges of the signal to become steeper. This yields a higher efficiency, as there is less overlap between voltage and current waveforms as can be seen in figure 2.11.

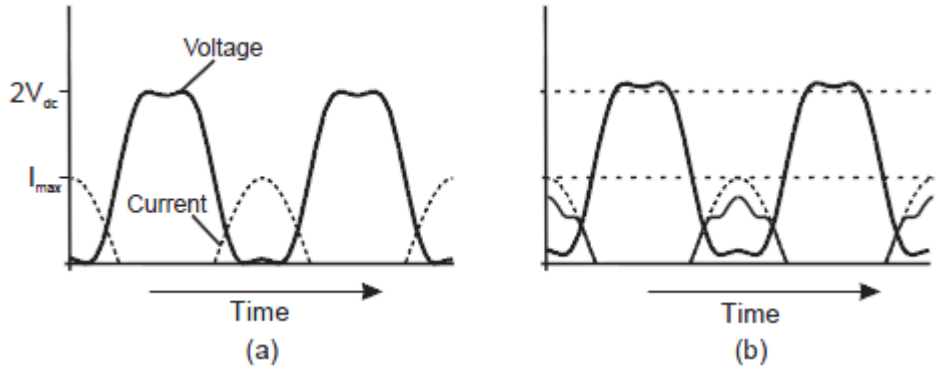


Figure 2.11: Voltage- and Current-waveforms plotted together vs. time. (a) shows ideal characteristics, and (b) shows the more realistic characteristic due to the device knee effect[23, pp. 59-61].

An inverse class F amplifier is the opposite of a class F amplifier, meaning short-load termination is added to the odd harmonics and open-load termination is added to the even harmonics. Thus, ideally, the drain current waveform will be a square wave and the drain voltage will be a rectified sinusoidal waveform. Results presented in [46] show that the inverse class F outperforms the class F in terms of power efficiency and output power with increasing on-state resistance. The drawback of the inverse class F is that it can have very large voltage peaks, which in worst case could exceed the breakdown voltage of the transistor.

2.8 Stability

An amplifier can begin to oscillate if the input reflection coefficient Γ_{in} or the output reflection coefficient Γ_{out} is greater than 1[38, p. 199]. Thus, from (2.12) and (2.13) the stability is dependent on the matching networks. An amplifier can be either unconditionally stable, that means, stable for all source and load impedances, or it can be potentially unstable, which means that for some source or load impedances Γ_{in} or $\Gamma_{out} > 1$.

To stabilize an amplifier, three strategies are mainly used; introducing loss on the input with the use of a series or shunt resistor, introducing loss

on the output, or applying a feedback to the transistor.

There are many ways to determine the stability of a PA. One is to display the borders for Γ_{in} and $\Gamma_{out} = 1$ in a Smith chart. These stability circles show the source and load impedance region where the circuit is stable.

An amplifier circuit should be unconditionally stable, and in addition to the stability circles there are a number of tests to determine if the amplifier circuit is stable. The Rollet stability criterion[43] can show whether or not the circuit is stable. K and Δ are defined by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} > 1 \tag{2.27}$$

and,

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \tag{2.28}$$

If both these conditions are met, the circuit is stable.

What the $K-\Delta$ test does not say anything about however, is if the circuit is on the verge of being unstable, or if it is stable with a good margin. The μ-test[24] has the property that an increase in the single test parameter μ is proportional with the added stability. This gives the posibility of comparing the relative stability of two circuits. The parameter for stability in the μ-test is given by

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1. \tag{2.29}$$

2.8.1 Odd-Mode Oscillations

When multiple transistors are coupled together in parallell, as they often are in power amplifiers, odd-mode oscillations can occur. Odd-mode oscillations[26][19, pp. 490-501] happen when a signal from one transistor travels back through another transistor and in this way causes a feedback loop. These oscillations can occur due to device mismatch caused by fabrication variations, or due to differences in each transistors matching network.

However, they can also be a function of input-power and bias levels, and independent of source- and load-impedances[34]. Odd-mode oscillations are not modeled by the stability tests discussed in 2.8, but other test using odd-mode analysis, the Nyquist stability criterion[29][36] and global stability analysis[35][42] have been developed for this purpose.

To prevent odd-mode oscillations the designer should use as well matched devices as possible with regard to source inductance, signal amplitude and phase and balanced matching networks. If this is not possible the devices should have gate and drain ports connected together by the shortest possible distance, or have isolation resistors connected between them in sizes determined by odd-mode analysis. Typical size range is 10-50Ω.

2.9 Bode-Fano Criterion

Any RF designers dream is to make a RFPA design with large gains over great bandwidths. Unfortunately this is not always possible, especially when efficiency and reflections must be taken into account. The Bode-Fano criterion[20][25] gives a theoretical limit for what bandwidth it is possible to achieve a given reflection coefficient with a N^{th} order ideal matching network. This is very useful as it shows what is optimally possible to achieve, although it can only be approximated in practice. The bandwidth of the matching network is limited by the load impedance of the network. The input and output impedances of the transistor can be approximated by lumped components. The Bode-Fano criterion is given by

$$\int_0^\infty \ln|\frac{1}{\Gamma}|d\omega \leq \pi\omega_0 RC, \tag{2.30}$$

where Γ is the reflection coefficient of the matching network, ω_0 is the center frequency, and R and C are the impedances of the equivalent series RC-circuit. If the reflection coefficient is approximately constant over the bandwidth $\Delta\omega = \omega_b - \omega_a$ the expression in (2.30) becomes

$$\Delta\omega \ln|\frac{1}{\Gamma_m}| = \pi\omega_0 RC, \tag{2.31}$$

where Γ_m is the constant reflection coefficient over the bandwidth.

In turn this gives

$$\mathrm{BW} = \frac{\pi R}{X_C \ln|\frac{1}{\Gamma_m}|}, \tag{2.32}$$

where the maximum bandwidth BW is defined as $\mathrm{BW} = \frac{\Delta\omega}{\omega_0}$ and X_C is the impedance of the series capacitor.

Equation (2.32) shows that for loads with large reactive values relative to resistive values, also known as quality-factor(Q-factor), the maximum possible matching bandwidth is smaller than for loads with lower Q-factors.

2.10 Bonding Wires

Bonding wires are extensively used in RF and microwave systems to interconnect integrated circuits and other circuitry. These wires have mainly an inductive impedance, but also a resistance.

The resistance of the bondwire is given by[19, p.142]

$$R = \frac{4l}{\pi\sigma d^2}\left[0.25\frac{d}{\delta} + 0.2654\right], \tag{2.33}$$

l and d are the length and diameter of the wire in microns, σ is the conductivity of the wire, while δ is the skin depth given by

$$\delta = \frac{1}{\sqrt{\pi\sigma f\mu_0}} \tag{2.34}$$

where μ_0 is the permeability in vacuum.

The inductance L of a single bondwire in free space is given by[19, p. 142]

$$L = 2\times10^{-4}l\left[\ln\left\{\frac{2l}{d} + \sqrt{1+\left(\frac{2l}{d}\right)^2}\right\} + \frac{d}{2l} - \sqrt{1+\left(\frac{2l}{d}\right)^2} + C\right] \tag{2.35}$$

where C is a correction factor, given by [19, p. 142]

$$C = 0.25 \tanh(4\delta/d). \tag{2.36}$$

Using the method of images[22, p. 159], a bondwire stretched at a height h over a ground plate gives a mutural inductance with a wire at $-h$ relative to the ground plane. The resulting inductance of the wire is

$$L_e = L - L_{\mathrm{mg}}, \tag{2.37}$$

and it can be shown that L_e becomes[19, p. 143]

$$L_e = 2 \times 10^{-4} l \left[\ln \frac{4h}{d} + \ln \left(\frac{l + \sqrt{l^2 + d^2/4}}{l + \sqrt{l^2 + 4h^2}} \right) + \sqrt{1 + \frac{4h^2}{l^2}} - \sqrt{1 + \frac{d^2}{4l^2}} - 2\frac{h}{l} + \frac{d}{2l} \right]. \tag{2.38}$$

Often multiple wires are used, e.g. to reduce wire inductance or improve current handling. In the case of two parallel wires carrying the same current, the total inductance is given by

$$L_{ep} = (L_e - L_m)/2. \tag{2.39}$$

The mutural inductance L_m is given by[19, p. 143]

$$L_m = 2 \times 10^{-4} l \left[\ln \left\{ \frac{l}{S} + \sqrt{1 + \left(\frac{l}{S} \right)^2} \right\} + \frac{S}{l} - \sqrt{1 + \left(\frac{S}{l} \right)^2} + \frac{S}{l} \right], \tag{2.40}$$

where S is the spacing between the wires. It can be seen that the decrease in inductance by adding wires in parallel is dependent of the spacing between the lines.

The maximum current handling of a single bonding wire is given by[19, p. 145]

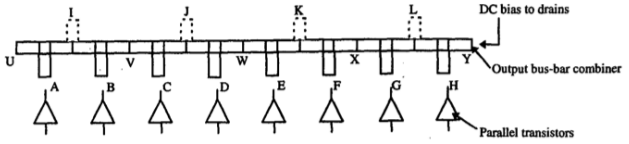
$$I_f = Kd^{1.5}, \tag{2.41}$$

where d is the diameter of the wire in mm, while K is a constant dependent on what material is used. For gold K is 183.

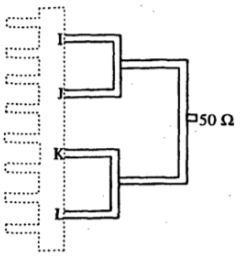
2.11 Power Dividers and Directional Couplers

2.11.1 Bus-Bar Combiner

The bus-bar[31, p. 6/5] is commonly used as power combiners for connecting large periphery active devices in an MMIC circuit. It gets the name from the bar connecting all the devices together as shown in figure 2.12, where often the DC-bias is fed to the devices. The RF-power is tapped at the symmetry points, and combined using a tree structure combiner. The symmetry of the bus-bar combiner makes it possible to combine 2^N-devices[32, p. 164]. The main advantages with using the bus-bar is the ease of feeding DC to active devices, and that the short path between devices reduces the risk of odd-mode oscillations[26].



(a) An example design of a bus-bar [32, p. 167]



(b) The corresponding tree combining structure to figure 2.12a [32, p. 168]

Figure 2.12: An example of a bus-bar combiner design with the bus-bar and tree combining structure

2.11.2 Wilkinson Divider

The Wilkinson divider is a n-way equiphase and equiamplitude power divider, which was first presented by E.J. Wilkinson in 1960[45]. The 2 way Wilkinson divider shown in figure 2.13 consists of two quarter wave lines with impedance of $\sqrt{2}Z_0$, and an isolation resistor with a value of $2Z_0$. The main advantages of the Wilkinson divider is its broad bandwidth and equal phase characteristics, and it is one of the most commonly used $3\ dB$ power dividers. In a Wilkinson divider, all ports are matched, and the output ports are isolated. The Wilkinson divider can also be used as a combiner, as it is passive and hence reciprocal.

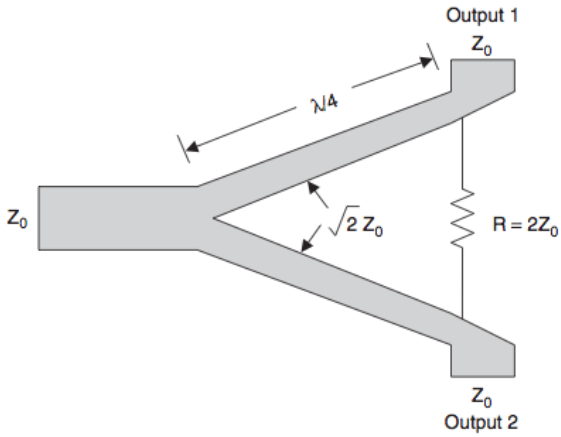


Figure 2.13: A conseptual drawing of the Wilkinson power divider.[19, p.538]

2.11.3 Branch Line Coupler

The branch-line coupler[40] is a 3 dB, 90-degree hybrid coupler, where one of the two output ports is 90 degrees phase shifted relative to the other. Hybrid couplers have relatively large area and narrow bandwidth, but are commonly used in millimeter wave circuits. In figure 2.14 port 1 is the input port, port 2 and 3 are the output ports where port 3 is 90 degrees phase shifted relative to port 2.

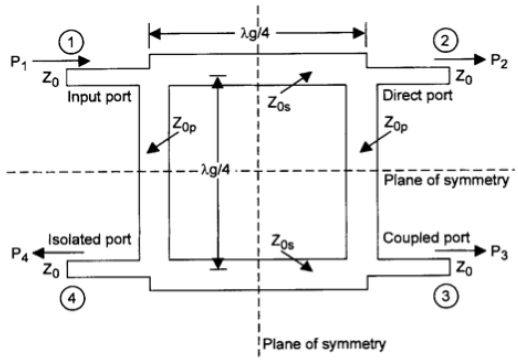


Figure 2.14: A conseptual drawing of the branch-line hybrid coupler.[40, p.220]

Chapter 3

Device technology

3.1 Transistor

The transistor selected for this thesis was the CREE CGHV1J070D GaN HEMT die[3], a transistor with saturation at 70W made for use from DC to 18GHz and designed for a drain voltage of $40\ V$. As there is need for a very compact design the use of a transistor die is prefered to a packaged transistor. The CGHV1J070D is made up by 12 6W transistors in parallel, and thus have 12 input and output ports. The design utilized the CREE transtor model for the CGHV1J070D in Agilent Advanced Design System(ADS)[6].

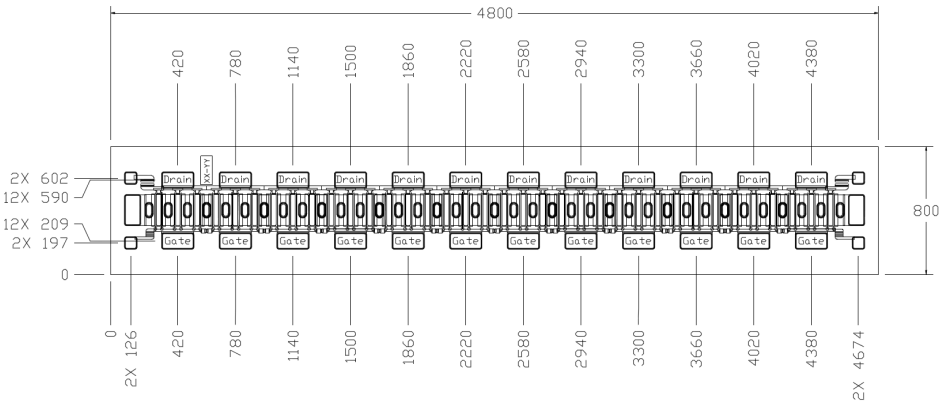


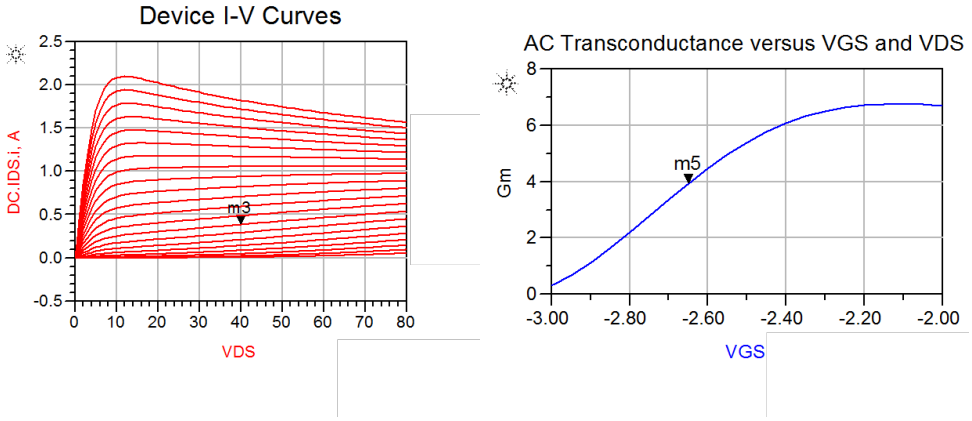
Figure 3.1: Footprint of the CGHV1J070D with dimensions. Drawing from [3, p. 3].

The die has a total width of 4.8 mm with a distance of 4.16 mm from the outer border of the bonding pads of the 1st to the 12th transistor as shown in figure 3.1. This makes the die wide with regard to the wavelength, which on a FR4 substrate[5] at 8.5 GHz is $\lambda/4 \approx 4.3mm$. A large deviation in phase could occur if the feeding of the transitor is not carefully though out. If the bonding wires from the die is connected directly to a 50Ω line the resulting difference in phase on the output between the two middle transistors and the two outer transitors on the die would be approximately 75 degrees, which would result in a power loss of about 0.87 dB, calculated in Appendix E.1. Appendix E.2 and E.3 show that by having a second feeding point or using a tapered line for feeding the transistor the loss is cut to 0.195 dB or 0.145 dB, respectively. As a result of this it was decided to design different feeding topologies in an attempt to feed the signal to the transistor die as ideally as possible.

3.1.1 Quiescent Point

The drain voltage for the transistor was set to 48V due to demands to follow certain telecom standards. The drain current was set to 360 mA, which corresponds to a Class AB. This gives the possibility of a higher efficiency than class A, while maintaining the same gain. At the same time it opens

possibilities to design the circuit as a Class F amplifier. The quiescent point is shown in figure 3.2.



(a) Drain current in amperes vs. drain voltage in volts, plotted for a number of gate voltages, and with the chosen quiescent point annotated.

(b) Transconductance(Gm) $[A/V]$ vs. gate voltage in volts for the chosen drain voltage, and with chosen quiescent point annotated

Figure 3.2: Plots of the quiescent point.

3.2 Substrate

A number of desired characteristics were emphasized in the choosing of substrate for the circuit. It was wanted to make the concequences of the large device periphery as small as possible, and thus it was desired to have a low dielectric constant(ϵ_r). This would mean that the wavelength would be longer (see (2.19)) making the die as small as possible relative to the wavelength at the conductors on the substrate, and thus the phase differences between the different transistors on the die are minimized.

As the output power of the transistor could be very high, an other advantage of using a substrate with low dielectric constant is that the width of a $50\ \Omega$ line would be wider than on a substrate with higher dielectric constant (seen in (2.16) and (2.17)) as an increase in ϵ_{eff} would mean that the W/h must decrease to maintain the same impedance. This would make the power handling of the line better, reducing the risk of the substrate becom-

ing very hot. As a precaution due to the high output power of the transistor the output network will not utilize line widths corresponding to impedances higher than $50\ \Omega$, but it is highly wanted to be able to use $50\ \Omega$-lines, as this is the characteristic impedance of the system. In addition to the line width, a low line loss will result in less power lost to heat along a line, and therefore a thin substrate and low loss tangent was wanted. With these wanted characteristics the Rogers Tech/Duroid 5880 substrate was chosen, with characteristics as shown in table 3.1

Table 3.1: Specifications for the RT/Duroid 5880 substrate [9].

Substrate values	
ϵ_r	2.2
$\tan_\delta$	0.0009
Height	0.508 mm
Metal sheet thickness	$35\mu m$

3.3 Capacitors

The capacitors used in this thesis are from Johanson Technologies R14S series, these are ceramic multilayer capacitors made for RF and microwave purposes. These capacitors have NP0 characteristics, meaning that the temperature coefficient is zero and the capacitance vary little with different operating temperatures[1]. The capacitors can also withstand 250V, which is a benefit as there are possibilities for large output voltages. Higher frequency parasitic effects causes resonance and resistance, even for RF and microwave capacitors such as the Johanson Technologies R14S series. An equvivalient circuit schematic for a capacitor at higher frequencies is shown in figure 3.3.

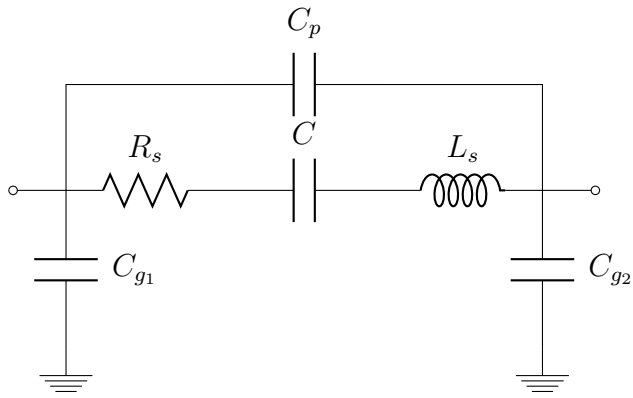


Figure 3.3: Equivalent circuit of a capacitor, with parasitic shunt capacitances(C_g) between the pads and ground, parasitic parallel capacitance between the pads(C_p), series parasitic resistance due to the contacts(R_s), and series inductance due to the ceramic layers(L_s).

The size of the capacitors are standard EIA size 0603 to keep the dimensions below $\lambda/20$ so that the components can be defined as lumped components[19, p. 134].

Chapter 4

Design and Measurements of Feeding Networks

4.1 Methodology

To simplify the design procedure the input and output networks have been divided into 3 different segments. The three segments are the feeding network, the stabilization network, and the matching network, shown in figure 4.1.

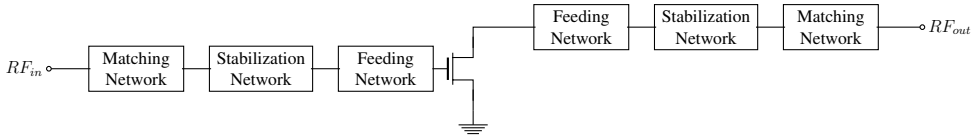


Figure 4.1: The divided structure of the circuit.

The design procedure has been to work from the center and outwards, meaning that the stabilization and matching networks have been based on the feeding network. Due to design considerations regarding the behaviour of the power amplifier circuit, and due to the fact that the transistor has different input and output impedances, the stabilization and matching networks will be different on the input and output of the transistor. The main

goal and motivation of having this design methodology, besides dividing the problem into subproblems, is to avoid iterations in the design process. This means that the design of an outer segment, e.g. the matching network, will be dependent on the inner segments(in this case the stabilization network, feeding network and transistor) but will never require changes in the inner segments.

4.2 Design Topologies

The task of the feeding networks is to divide and combine the signal from the 12 transistors on the transistor die with as little loss as possible, meaning the signals should be equal in phase and amplitude. In addition the feeding network should try to prevent odd-mode oscillations[26]. In the project exercise four topologies with feeding and stabilization networks which would make the bases of a PA design were designed using Agilent Advanced Design System(ADS)[6]. These topologies have been simulated to compare the stable topologies maximum available gain(MAG), which gives a clear indication of which topologies that can be utilized to make the best possible design in terms of small signal gain. Four feeding networks were made, a Bus-bar, a Wilkinson coupler, a taper and a Branch-line hybrid coupler(BLC), these are presented in detail in appendix B. Of the four, the Bus-bar and Wilkinson designs showed the largest MAG, shown in table 4.1.

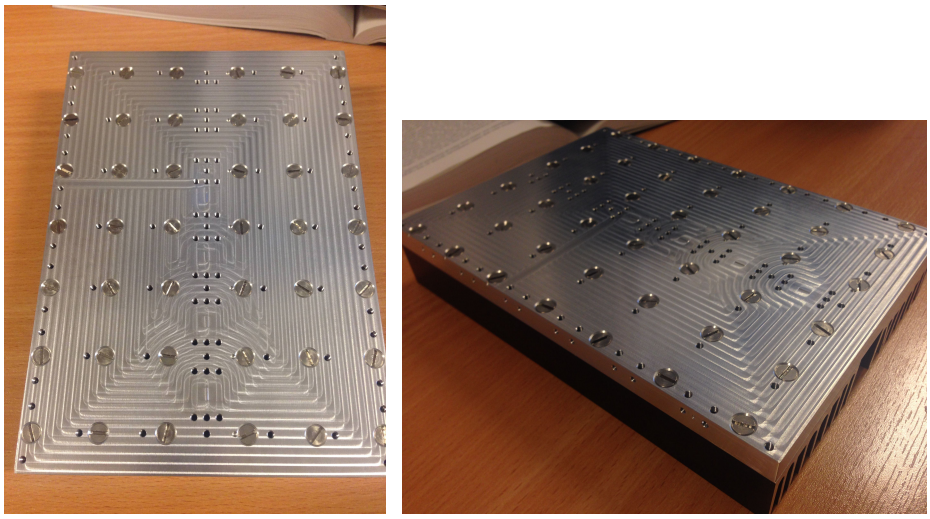
Table 4.1: Maximum available gain(MAG) and deviation in maximum available gain in the frequency band of 8-8.5GHz.

Design performance @ 8-8.5GHz		
	MAG (dB)	σ (dB)
Bus-bar	15.21	0.541
Wilkinson	15.69	0.582
Taper	11.75	0.369
BLC	-3.07	0.475

4.3 Realization

4.3.1 Cooling Plate

When designing a plate for cooling of the power amplifier circuits, consideration was taken on the possibly extreme amounts of heat produced by the die. A cooling plate would have to be large and dissipate heat effectively. Therefore the cooling plate was cut from a piece of aluminium(Al), and cooling ridges in aluminium were mounted on the underside of the plate to maximize the effective area of the cooling plate. By making the cooling plate $148mm \times 210mm$, and with the possibility of connecting 12 SMA-connectors, enough space was made to measure several circuits in the same sitting. Four elevations of $0.4\ mm$ were included in order to mount the transistors directly to the cooling plate in the same height as the top of the substrate. This will maximize the heat dissipation, while making a well defined ground plane for the source of the transistor. Two pictures of the cooling plate are shown in figure 4.2

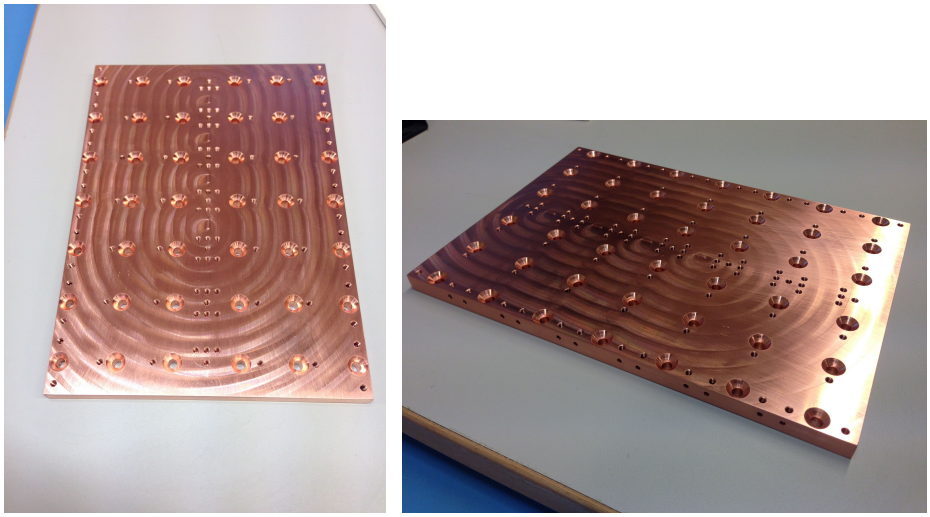


(a) **(b)**

Figure 4.2: The cooling plate, from above(a), and from the side(b).

Initial soldering tests on the cooling plate showed that solder paste does not flow well on Al. This was solved by making an identical cooling plate

in copper(Cu). This is not ideal for long term reliability, as Cu has a large temperature expansion coefficient than GaN. However, it should not be any concern for measuring purposes, as the circuit only will be measured over a short time period. The new Cu plate is shown in figure 4.3.

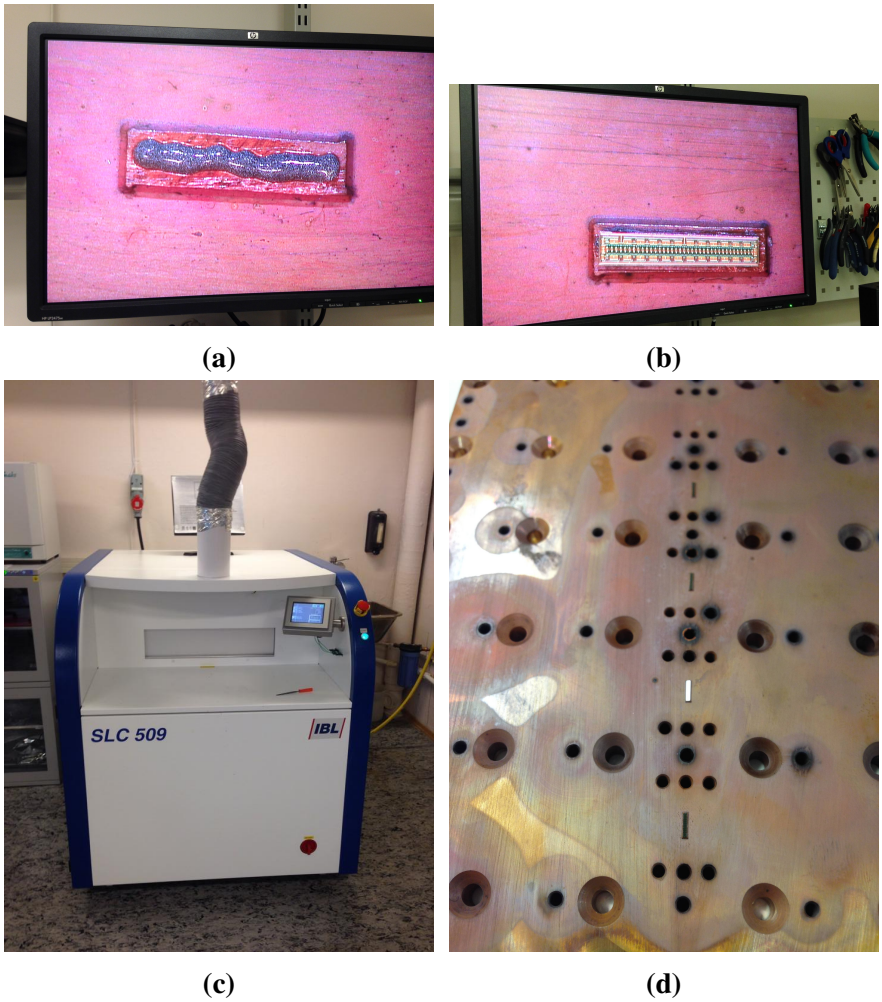


(a) **(b)**

Figure 4.3: The new Cu cooling plate, from above(a), and from the side(b).

4.3.2 Test Card

The test card was milled at the NTNU workshop and gold plated in the FFI laboratory. Gold plating was done both to prevent oxidation and to enable gold wire bonding of the transistor. The transistors were mounted directly to the Cu plate using a lead-based solder paste. Although this does not follow the application note for eutectic die attach procedure for the CGHV1J070D[4] it should be sufficient for short term operations such as testing. Solder paste was placed on the top of the elevations of the Cu plate, and the transitor was placed on top of the solder paste. The Cu plate was then put in a solder oven, heating the Cu plate to 240 degrees C and using Galden heat transfer fluid[14] to decrease oxidation. The die attach procedure is shown in figure 4.4.



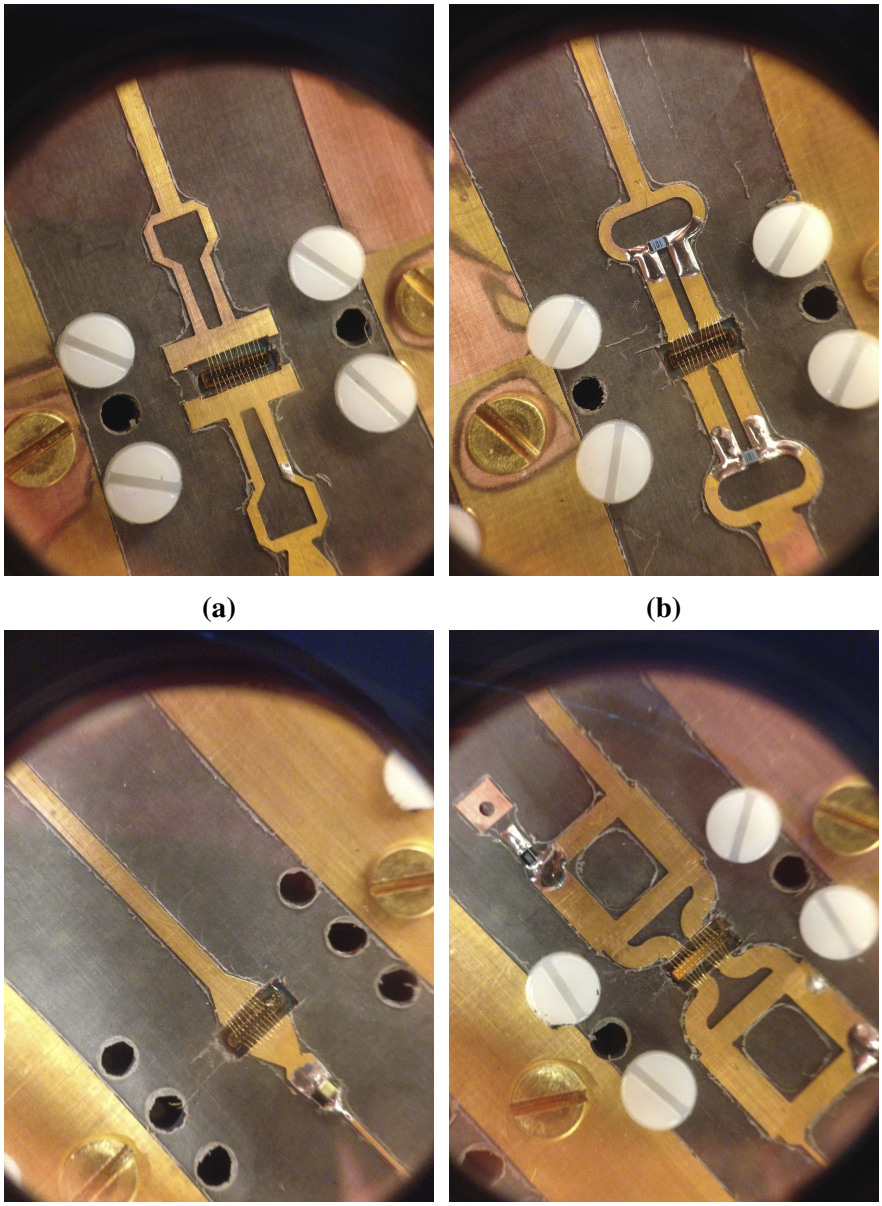
(a) **(b)**

(c) **(d)**

Figure 4.4: The die attach procedure step-by-step: (a): solder paste placed on the Cu plate, (b): transistor placed on top of solder paste, (c): solder heated in soldering machine, (d): finished result.

The test card was attached to the Cu plate using screws. During this process the transistor being used in the taper-design was damaged, unabling measurements of this circuit. When the test card was attached to the cooling plate and the needed components were soldered it was sent back to the lab for wire bonding. The bonding procedure used 20 mil gold wires and was done to resemble the model for the bonding wires used in the computer aided simulations of the design in Agilent Advanced Design System(ADS)

as good as possible. However, inaccuracies in the milling had caused the pads that were to be used as bonding surfaces to be milled away entirely(see figure 4.5). As a consequence, the bondwires had to be attached longer away than originally intended.



(a) **(b)**

(c) **(d)**

Figure 4.5: Close up of transistor and card showing lost detailes in layout due to the milling. (a): Bus-Bar design, (b): Wilkinson design, (c): Taper design, (d): Branch line coupler design

Due to the thickness of the substrate the plan of using via barrels to make the via holes proved hard to realize. As a concequence if was not possible to measure the BLC-design, as it needs 50Ω terminations to function properly. The finished test card with transistors connected is shown in figure 4.6.

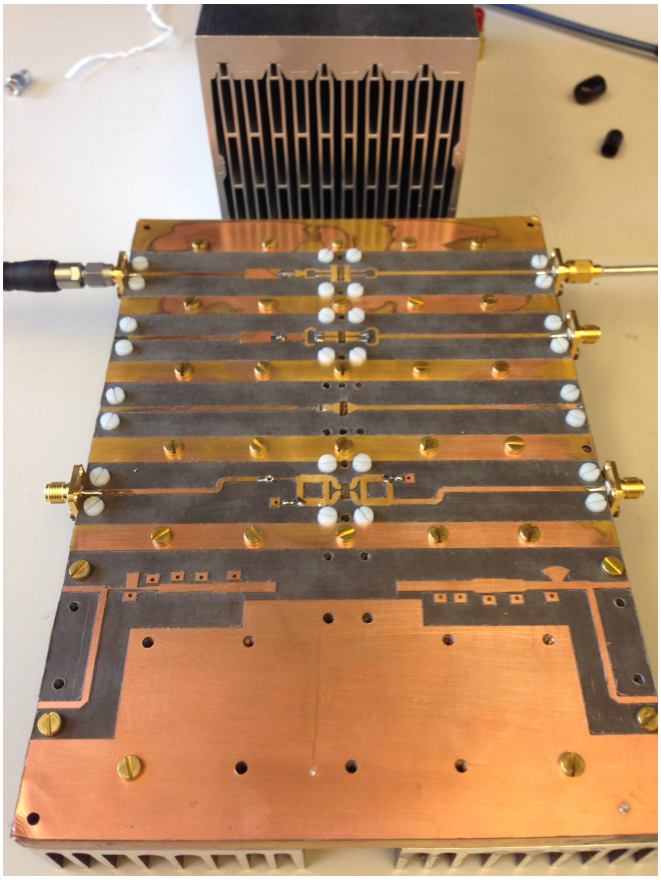


Figure 4.6: Finished test card placed on cooling plate.

4.3.3 Bias Tees

Biasing of the transistors on the test card was done externally. Bias tees designed by Morten Olavsbråten at NTNU were used. The bias Tee design is based on a RF-filter towards the DC-port, and a capacitor as DC-block used between the biased port connected to the circuit, and the unbiased port

connected to the test equipment, as shown in figure 4.7. Small signal measurements of the design showed that the bias-tees were working as designed, having one port isolated from RF over a large frequency band, including X-band, and one port isolated from DC. Results of the measurements can be seen in Appendix A.

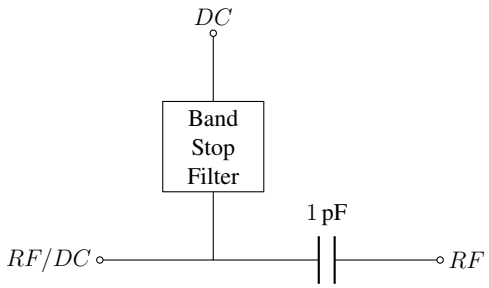


Figure 4.7: The build-up of the bias tees. It has one port with combined RF and DC, one for DC input and one RF output which is DC blocked.

4.4 Measurements

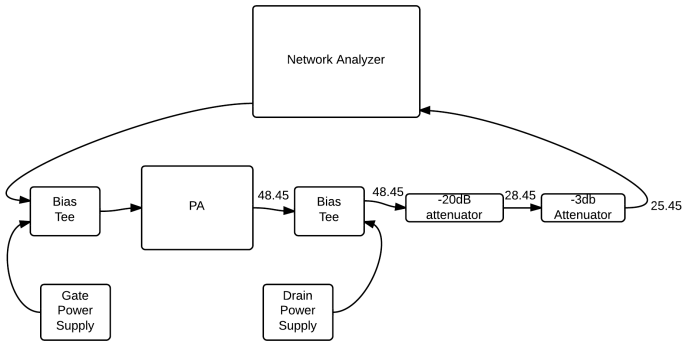
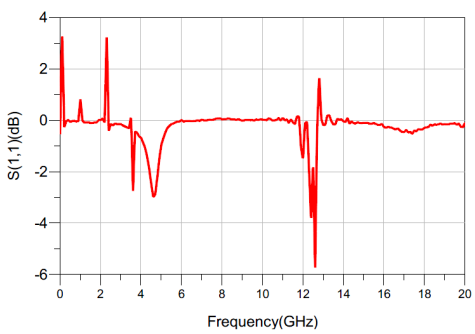


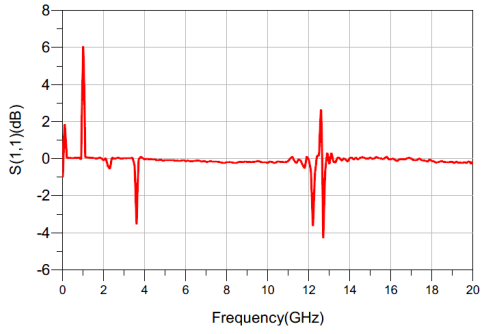
Figure 4.8: Test setup for measurements with a network analyzer. All numbers are absolute maximum power levels in dBm.

Measurement were performed at a microwave lab in FFIs facilities at Kjeller. The motivation was to measure the S-parameters of the topologies and

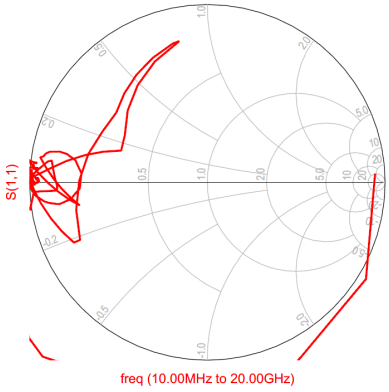
compare them with the simulations performed in ADS. Measurement-setup was done to prevent damage to measurement equipment. In a worst-case-scenario the transistor could oscillate with an output power of $47\,\mathrm{dBm}(70\,\mathrm{W})$. As the Network analyzer(Agilent N5245A)[11] and Spectrum analyzer(Rohde Schwarz FSUP)[17] only handles $30\ \mathrm{dBm}$ the output was attenuated by $23\,\mathrm{dB}$ using a 100W 20dB attenuator[13] in series with a 2W 3dB attenuator[15]. Bias Tees were attached between the PNA and test card at the input, and between the test card and attenuators at the output. Measurement setup is shown in figure 4.8. The test frequency range was set to $10\ \mathrm{MHz} - 20\mathrm{GHz}$ using 1001 measuring points. Calibration was performed using an Agilent N4693-60001 Electronic Calibration Module(ECal)[10] calibrating between the two bias tees, where the test card would be placed. By doing this, the other effects in the measurement setup (bias tees, cables and attenuators) would be calibrated away, and only the effects of the test card would show on the measured S-parameter data. In addition a delay was set on the PNA using a short calibration component. In the Smith chart, the delay was adjusted until it made a good short over the entire frequency range. This was done to eliminate the effects of the connectors, moving the reference plane outside the connectors, and thus only measure the component. Afterwards the quality of the calibration was controlled using short and open calibration components. The measuring results can be seen in figure 4.9.



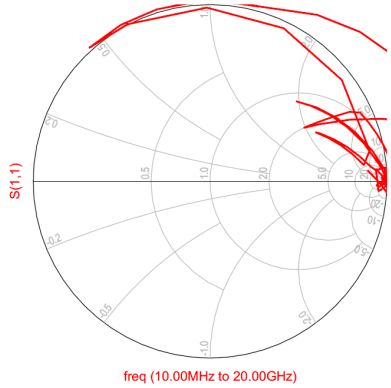
(a) S_{11} of port 1 on the PNA in dB with a short calibration component connected, measured over the frequency range of 0-20GHz.



(b) S_{11} of port 1 on the PNA in dB with an open calibration component connected, measured over the frequency range of 0-20GHz.



(c) S_{11} of port 1 on the PNA in the Smith chart with a short calibration component connected.

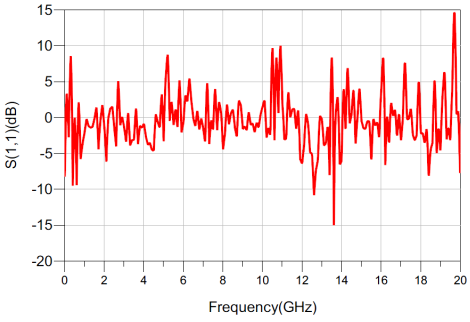


(d) S_{11} of port 1 on the PNA in the Smith chart with an open calibration component connected.

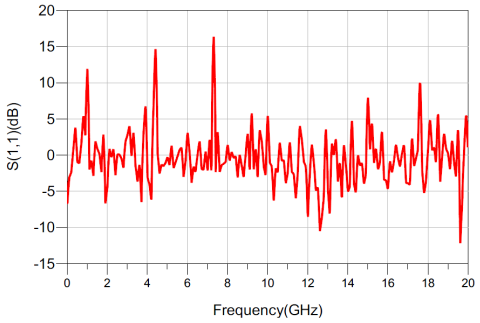
Figure 4.9: S_{11} measurements of short and open calibration components at port 1 of the PNA.

From figure 4.9 the calibration was good for most of the frequency range, with some important exceptions. Expecially in the frequency band around 12 GHz the calibration was bad, in addition to some points at 1, 2, and 3.5 GHz. This can be put in context with the measurements of the bias tees in appendix A where it is shown that the bias tee has very poor transmission at these frequencies. The short and open measurements had good characteristics within a band of $4 - 11$ GHz, which should indic-

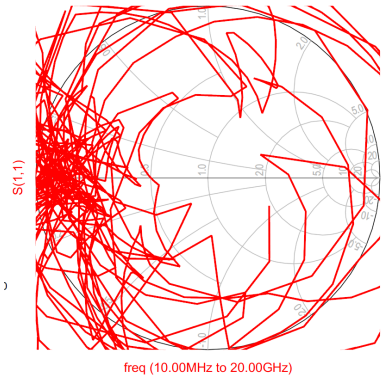
ate good measurements in this frequency range. It was also observed that the S-parameters measured at port 2 were much more variable than the S-parameters measured at port 1, which is shown in figure 4.10. Because of the attenuators at port 2, the reflection here was attenuated by an additional 46 dB and hence the measurement data are more dominated by noise.



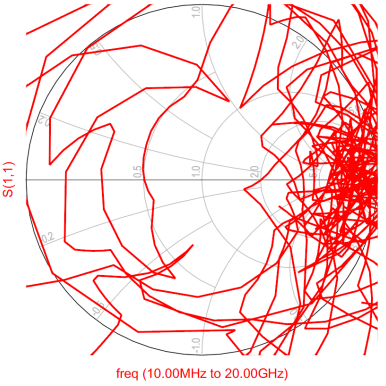
(a) S_{11} of port 2 on the PNA in dB with a short calibration component connected, measured over the frequency range of 0-20GHz.



(b) S_{11} of port 2 on the PNA in dB with an open calibration component connected, measured over the frequency range of 0-20GHz.



(c) S_{11} of port 2 on the PNA in the Smith chart with a short calibration component connected.



(d) S_{11} of port 2 on the PNA in dB with a short calibration component connected, displayed in a smith chart.

Figure 4.10: S_{11} measurements of short and open calibration components at port 2 of the PNA.

The measurements of the short and open components in figure 4.10 were

so noisy that the measurements of the backward travelling waves(S_{22} and S_{12}) were not performed for the designs, but there were no problem measuring the forward travelling waves(S_{11} and S_{21}). Biasing of the transistor was done with proper sequencing for GaN devices[12, p. 3]. The gate voltage was decreased below -3V (the cut off voltage for the transistor). The drain voltage was increased to 48V, and then the gate voltage was increased. Just above cutoff the transistor started to oscillate, this was easy to observe as the displays indicating the gate voltage and current on the power supply started to flicker, and the fan connected to the other port on the same power supply lost power. By connecting the test card to the signal analyzer, it was confirmed that the transistor was oscillating, as can be seen by figure 4.11.

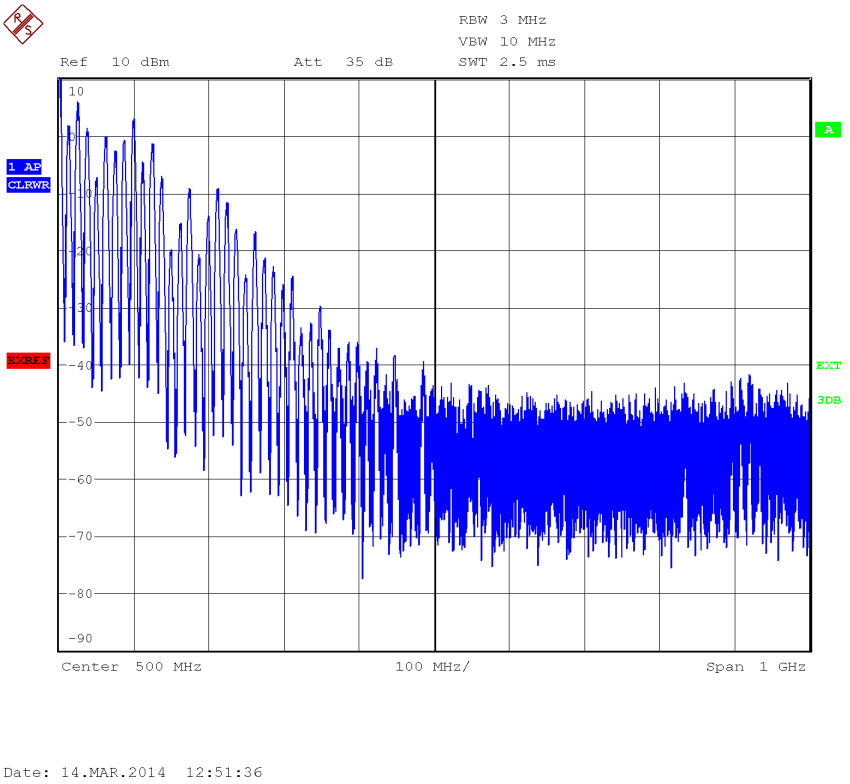


Figure 4.11: Oscillations from the testcard measured at the signal analyzer over a frequency range of 0 to 1GHz, with a power range from 10dBm to -90(not compensated for the output loss of the circuit).

The oscilliations were probably caused by the noise coming from the power supply. In an attempt to stop the oscillations, 3 large decoupling capacitors($10\mu F$, $4.7\mu F$ and $0.47\mu F$) were connected between the DC output and ground at the gate bias network. This would filter out some of the noise coming from the power supply. When biasing the transistors the next time no oscillations occured and the measurements were carried out without further problems.

4.5 Results and Discussion

Measurements of S-parameters of the Bus-bar and Wilkinson circuit were performed as explained in 4.4. The results will be presented next and compared to the simulation results. Deviations between the simulations and measurements will be discussed.

4.5.1 Bus-bar

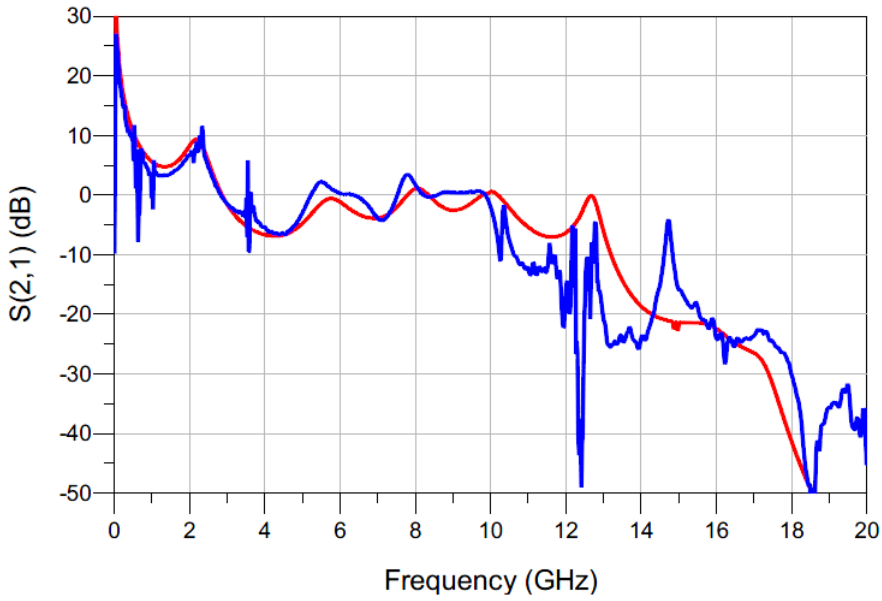


Figure 4.12: The measured S_{21}(blue) and simulated S_{21}(red) of the Bus-bar design over a frequency of 0 to 20GHz.

Measured and simulated results for the S_{21} parameter of the Bus-bar design are compared in figure 4.12. It can be seen that the measurements fluctuate around the same frequencies as the short and open measurements in 4.4, meaning that the attenuation here is so large that the signal is close to the PNAs dynamic range limit, and thus these frequencies could have large deviations and should be ignored. Overall, the tendensies of the S_{21} measurements are quite comparable with the simulated results. The simulated results have some peaks(at 2.2, 5.5 and 8 GHz). For the measured results these peaks are also visible, but are shifted lower in frequency(2.2, 5.25 and 7.75GHz).

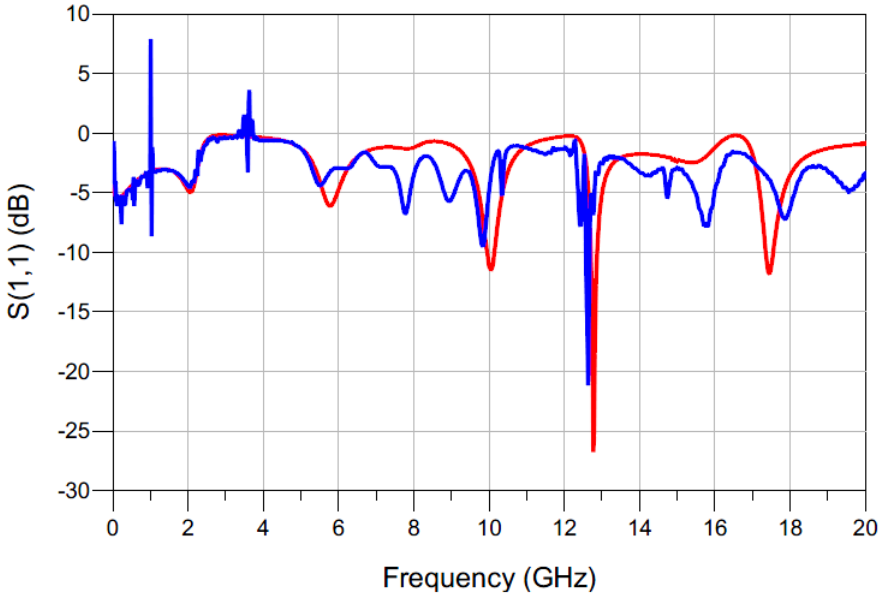


Figure 4.13: The measured S_{11}(blue) and simulated S_{11}(red) of the busbar design over a frequency of 0 to 20GHz.

The measured and simulated S_{11} parameter results are shown in figure 4.13, and show a good consistency between measured and simulated results. As was the case for the S_{21} parameter the measured results are slightly frequency shifted compared to the simulated results, but there are also some more fluctuations present in the measured results which are not seen in the simulated result.

Summed up, there are some differences between the measured and simulated results. This might be due to inaccuracies in the milling, e.g. the small bonding pads that was supposed to be in the layout is non-existent, as can be seen in figure 4.5. As a direct consequence of this, the length of the bonding wires are over twice the length as the bonding wire model used in ADS. Also, the milling seems to have removed some of the substrate in addition to the metal, this might have caused the effective dielectric constant of the microstrip lines to become marginally lower(see (2.14) and (2.15)).

4.5.2 Wilkinson

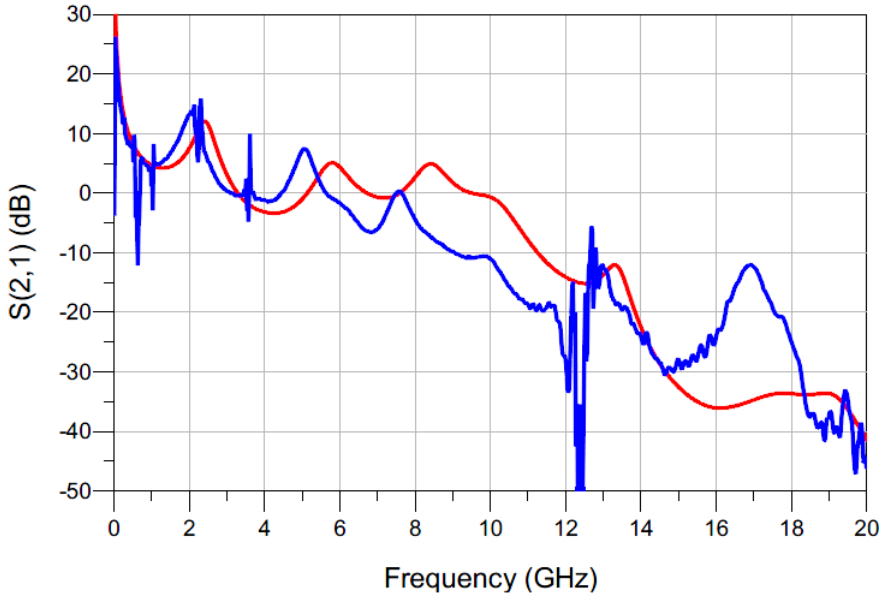


Figure 4.14: The measured S_{21}(blue) and simulated S_{21}(red) of the Wilkinson design over a frequency of 0 to 20GHz.

In figure 4.14 a comparison is done between the simulated and measured S_{21} parameter of the Wilkinson design. Comparing the simulated S_{21} peaks at 2.5, 5.5 and 8.5 GHz with the measured peaks, there are larger differences than for the Bus-bar design. The measured peaks increasingly precede the simulated results in terms of frequency(2, 5 and 7.5 GHz), and is inconsistent with the simulated results in amplitude.

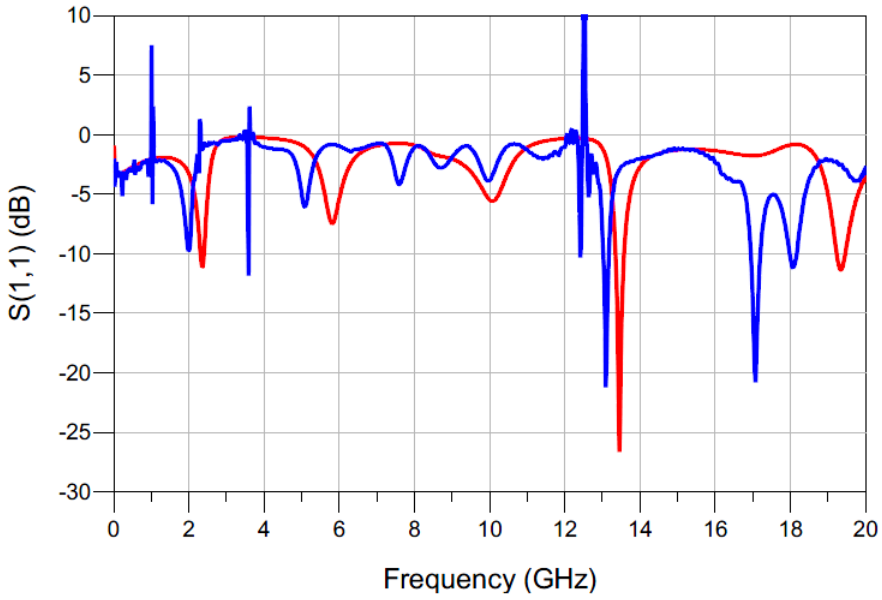


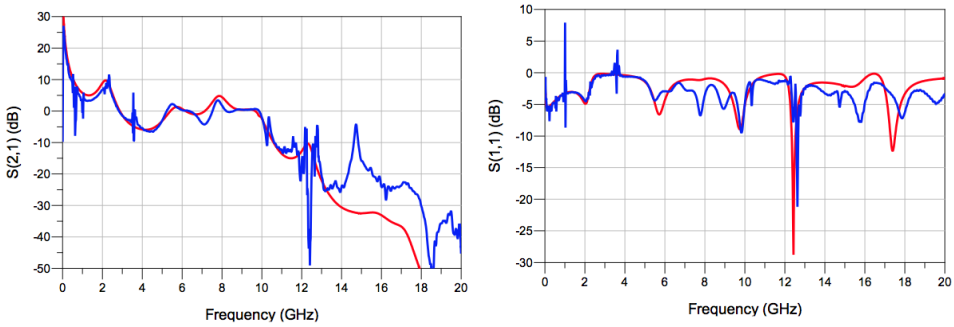
Figure 4.15: The measured S_{11}(blue) and simulated S_{11}(red) of the Wilkinson design over a frequency of 0 to 20GHz.

The comparison of the reflection(S_{11}) is much better than for the S_{21}, as can be seen in figure 4.15. The curves are more equal, but there are still differences between measured and simulated S_{11} minima. The minimum at 5.75 GHz in the simulations is seen at 5 GHz in the measurements. Also, the same kind of fluctuations in S_{11} that was measured on the Busbar design can be seen in the band around 8GHz on the Wilkinson design.

There are a better match between simulations and measurement for the Bus-bar design than for the Wilkinson design. For the Wilkinson design the milling seems to be even deeper as this design is located closer to the middle of the card. It seems as if the card may have been flexing during the milling process and that the middle of the card have been milled deeper than the edges. The effect of the inaccuracies in modelling of the bonding wires have had a more drastic effect on the design, and an attempt was made to match the bonding model to the lengths of the bonding-wires on the test card.

4.6 Revised Simulations Due to Faulty Bonding Wire Lengths

Because of the milling inaccuracies the bonding wires had to be connected to the substrate further away from the transistor than what was originally intended. The bondwire model was therefore modified after measurements to see if the deviations between measured and simulated values could be removed. The bondwire model was changed so that it as good as possible resembled the bondwires that being used on the test card.

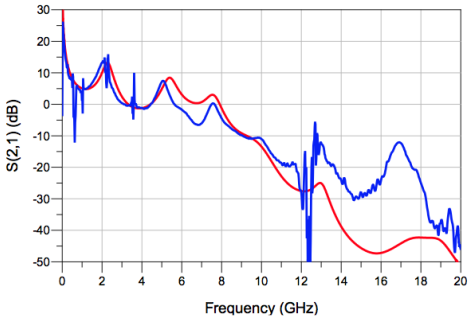


(a) S_{21} measurements and revised simulations in dB of the Bus-bar design, over the frequency range of 0-20 GHz.

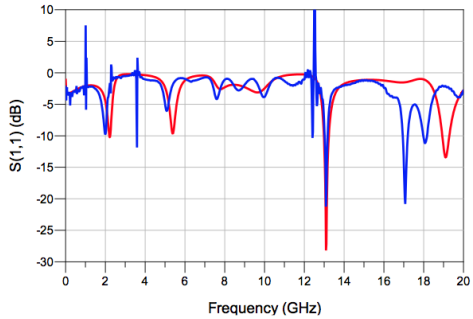
(b) S_{11} measurements and revised simulations in dB of the Bus-bar design, over the frequency range of 0-20 GHz.

Figure 4.16: Forward travelling S-parameters of the Bus-bar design with revised simulations.

As can be seen from figure 4.16, the simulated results for the Bus-bar design with the correct bondwire model is a better fit than with the original bondwire model. Although there are still deviations for some frequencies, the simulation result are following the measured results very closely. Also for the Wilkinson design, the simulation results better resembled the measurement results.



(a) S_{21} measurements and revised simulations in dB of the Wilkinson design, over the frequency range of 0-20 GHz.



(b) S_{11} measurements and revised simulations in dB of the Wilkinson design, over the frequency range of 0-20 GHz.

Figure 4.17: Forward travelling S-parameters of the Wilkinson design with revised simulations.

The simulation results are now much closer to the measured results than what was the case with the original bondwire model. Still, there are some inaccuracies, especially in the band between 5 and 8 GHz. Either the bondwire model is still not good enough, or there are some other effects happening on the test card that is not being included in the simulations. The results strengthen the need for a bondwire model that can be realized as accurate as possible.

Chapter 5

Design

The measurements in 4.5 and the comparison of the bonding wire model in 4.6 showed good enough similarity between simulated and measured result so that the design procedure could be continued. The measurements had shown that more accuracy in the realization was needed than what was the case for the first test card. Therefore a professional PCB-producer was contacted and the bonding wire model for the circuit was revised.

5.1 Revised Bonding Wire Model

The bonding wire model was revised to better reflect the bonding wires that would be used on the finished circuit board. This was done by having test bonding done on a sapphire plate showing the range of lofts and shapes that could be produced by the bonding machine. Measurements of the bonding wires were performed using an X-ray machine. The results from these measurement, which are depicted in figure 5.1, served as a base for the new revised bonding wire model.

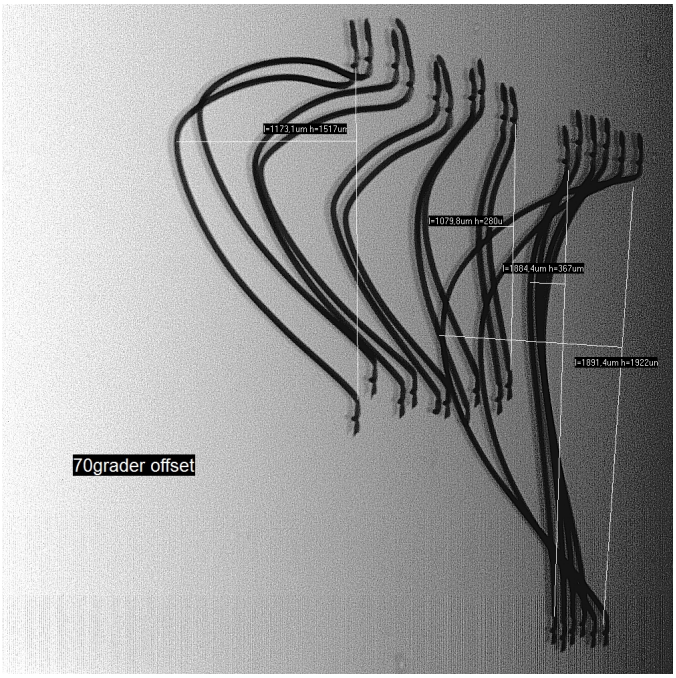


Figure 5.1: Picture taken from an X-ray machine showing test bonding wires with different lengths and lofts (measurements not readable).

In ADS the bonding wire model has input parameters of tilt section, strech section, start and stop heigth, and gap width as shown in figure 5.2. By examining the test bonding wires, these parameters were changed as indicated in table 5.1. Start and stop height are both 0, as the transistors has been mounted on elevations in the cooling plate to make them align with the top of the substrate.

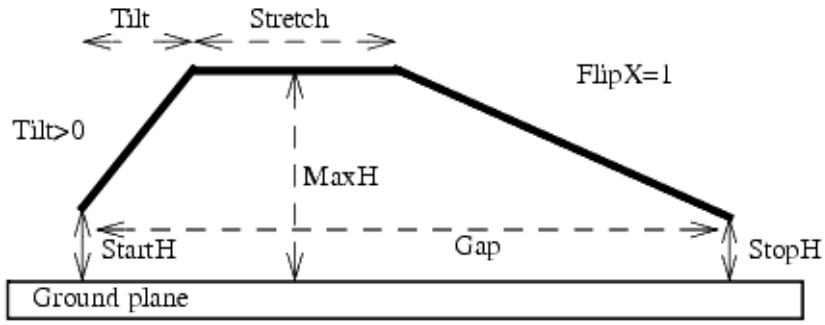


Figure 5.2: The computer bond wire model with denoted parameters.

Table 5.1: Old vs. new bonding wire model

Parameter values		
	Old	New
Tilt Width	300μm	500μm
Strech	300μm	400μm
Height	300μm	500μm
Gap Width	900μm	1400μm

5.2 Revised Feeding Networks

Due to the change of the bonding wire model the parasitic effects of the bonding wires will change as explained in 2.10. This means the impedance seen at the outside of the bonding wires will change. As the Wilkinson divider is closely matched to 50Ω there is little effect on the MAG of the system, but for the Busbar topology this is not the case, and the Bus-Bar design was changed to maintain an as large as possible MAG in the desired frequency range.

5.2.1 Revised Bus-Bar

For the Bus-Bar design the bar section was kept the same, but the T-splitter length was altered to give as large as possible MAG. This resulted in slightly longer lines. The layout of the revised busbar design is shown in figure 5.3.

Figure 5.3: The layout of the new Bus-bar feeding network

5.3 DC-Biasing Networks

The bias networks have been designed to be isolated from the fundamental frequency range of 8-8.5 GHz. This has been done by using two transmission lines with length equal to a quarter wave of the fundamental frequency. Using a quarter wave open stub line combined with a quarter wave transmission line to the output of the bias networks make the impedance at the bias network output equivalent to an open circuit for the fundamental frequency. In addition there are capacitors of different sizes to decouple lower frequency signals such as noise from the power supplies, and thus improving the stability performance of the circuit. In addition to the designed and simulated capacitors in the bias networks there have been added more pads to be able to attach more decoupling capacitors if necessary.

Some special design considerations have been made: For the gate bias network shown in figure 5.4, the quarter wave line on the output of the bias network has been made thinner than a 50Ω line(1 mm vs. 1.569 mm) to make an additional inductive effect, and hence increase the isolation for the fundamental frequencies. Also, a 200Ω resistor was added at the output to increase stability and isolation of the bias network. Layout of the gate bias network are shown in figure 5.5. The gate bias network was simulated to see how a signal on a transmission line was affected if the gate bias network was connected to it. The simulation characteristics are summarized in table

5.2.

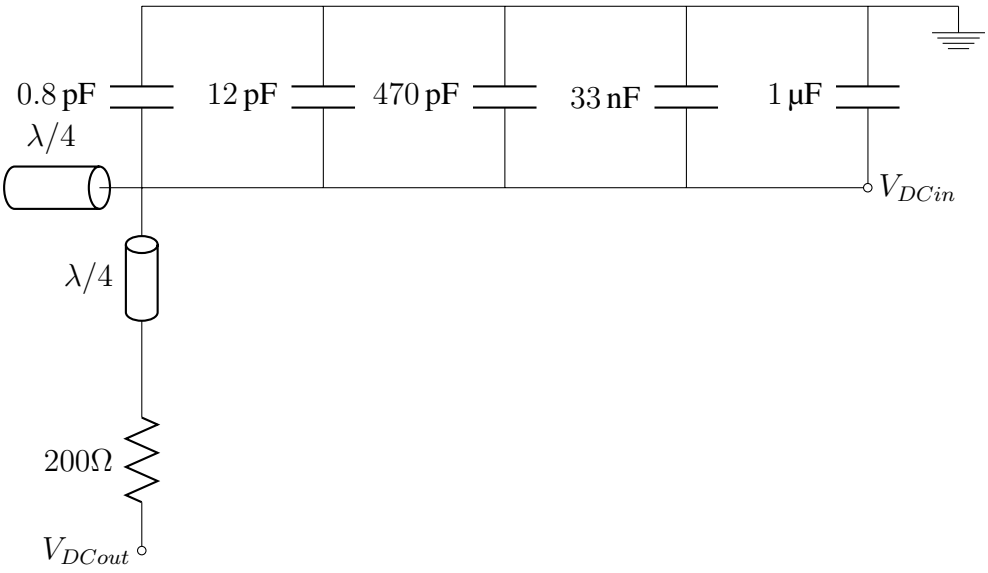


Figure 5.4: A schematic of the designed gate bias network. The line lengths are relative to the fundamental frequency.

Figure 5.5: Layout of the gate bias. Extra pads have been added to connect extra capasitors if needed, and allowing easy access to the ground plane for the wires from the power supply.

Table 5.2: Simulated specifications for the gate bias network

Isolation values	
Max S_{21}	-0.129 dB @ 8.11 GHz
-1 dB S_{21} bandwidth	5.96-9.59GHz

For the drain bias network in figure 5.6, different design considerations were taken. Due to the amount of power being distributed through the bias network, it was desided to not make the line widths smaller than 1 mm. In addition to this the quarter wave open stub was made into a widened line, increasing the width at the outerpoint to prevent a very large, concentrated electromagnetic field which can cause the transmission line to be burned off. The widened open stub line also makes the isolation bandwidth larger. Layout of the drain bias network is shown in figure 5.7. Simulations were performed on the drain bias network in the same fashion as for the gate bias network, and the key characteristics are shown in table 5.3.

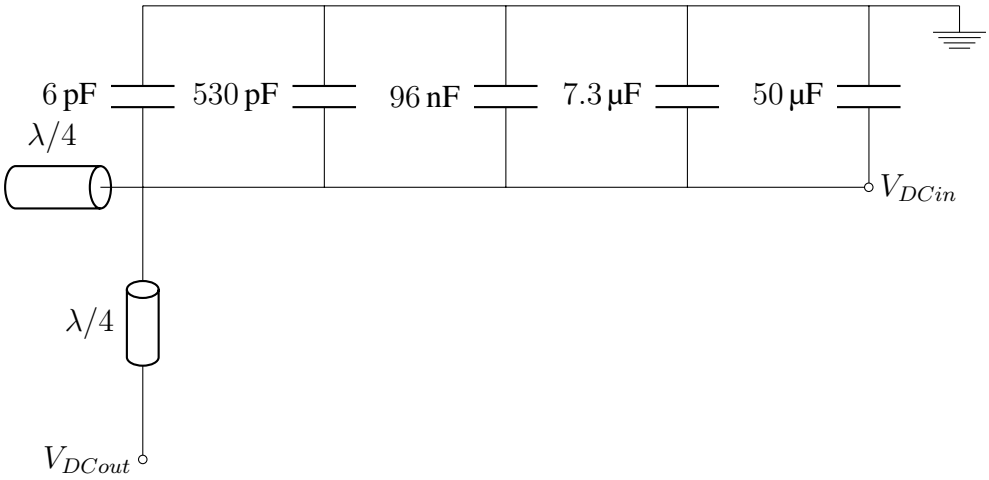


Figure 5.6: A schematic of the designed drain bias network. The line lengths are relative to the fundamental frequency.

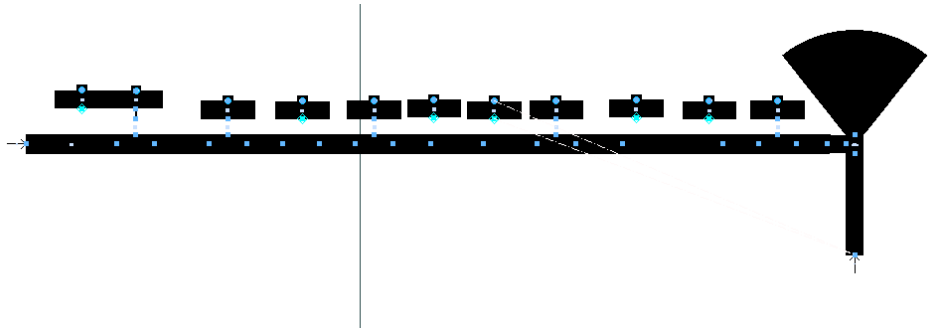


Figure 5.7: Layout of the drain bias. Extra pads have been added to be able to connect extra capasitors if needed, in addition to easy access to the ground plane for the bias network.

Table 5.3: Simulated specifications for the drain bias network

Isolation values	
Max S_{21}	-0.116 dB @7.85 GHz
-1 dB S_{21} bandwidth	4.65-11.11GHz

For the Wilkinson design, the bias networks were placed directly outside the feeding networks. On the drain side two drain bias networks were used to help the transmission lines to manage the power being feeded through the bias network. The layout of the Wilkinson design with biasing networks attached is shown in figure 5.8.

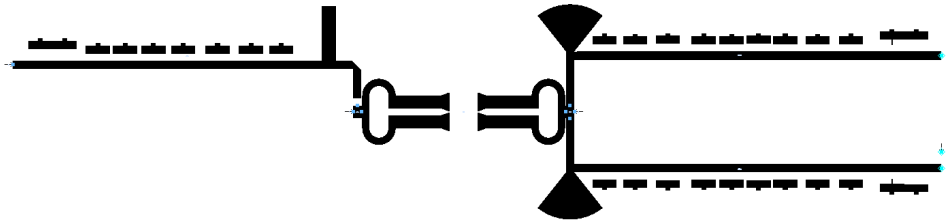


Figure 5.8: Layout of the Wilkinson feeding network with gate and drain bias networks connected.

For the Bus-bar design the bias networks were connected directly to the bus-bar itself to decrease the distance from the DC feed to the transistor. For

the Bus-Bar only one drain bias network was connected, not because there is less chance of overheating due to power here, but due to the fact that the circuit showed better behavior with only one drain bias network connected. This does not necessarily mean that the Bus-Bar design is unable to handle maximum power. That could only be proved through measurements. The layout of the Bus-bar design with bias networks is shown in figure 5.9.

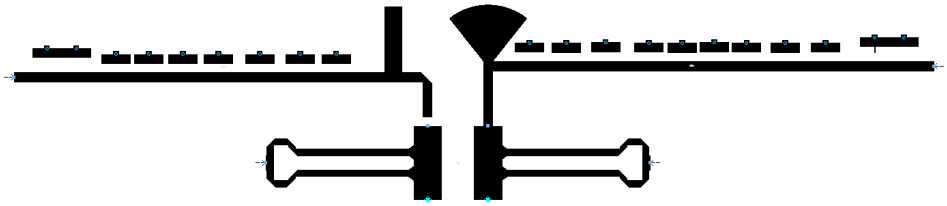


Figure 5.9: Layout of the Bus-bar feeding network with gate and drain bias networks connected.

5.4 Harmonic Tuning

Due to the high power levels, having an efficient PA is crucial. Harmonic tuning was performed in an attempt to increase the efficiency, and hence make a Class F PA, which typically has a higher efficiency than a Class AB PA. Harmonic tuning was performed by using two open stubs with length $\lambda/4$ of 2^{nd} and 3^{rd} harmonics respectively. This will give a short circuit for 2^{nd} and 3^{rd} harmonics at the end of the stubs. By tuning the lengths from the output of the transistor to the stubs the impedances for 2^{nd} and 3^{rd} harmonics can be changed from open to short circuit, and hence make either a class F or inverse class F PA. A principal schematic of the harmonic termination circuit is shown in figure 5.10. Since the voltages and currents directly at each of the output pads of the transistor could not be measured the harmonic tuning is left to optimalization, where the lengths of the transmission lines from the transistor to the stubs are optimized with regard to efficiency.

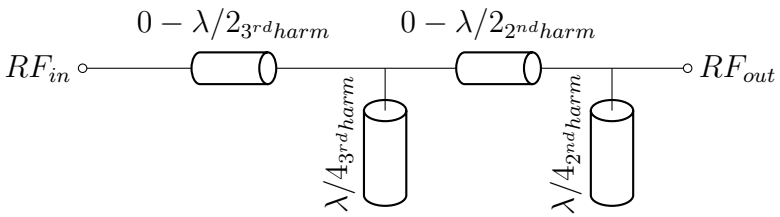


Figure 5.10: Schematic of harmonic tuning network made with open-circuit microstrip stubs

The harmonic tuning circuitry has been added to all designs at the outside of the feeding networks on the output of the PA.

5.5 Stability and Matching

Matching the PA for the entire bandwidth of 500 MHz proved quickly to be a more difficult task than first anticipated. Attempts were performed using open stub matching with 5th and 6th order matching networks and quarter wave stepped impedance matching networks, but although there was possible to achieve matching over the desired bandwidth, poor gain levels were achieved with high reflection coefficients both on the input and output. In an attempt to find the reason why the matching was unsatisfactory, the Bode-Fano criterion was used to calculate gain-bandwidth limitations. The following calculations are for the Bus-bar design. With matching impedances of

$$Z_{\text{source}}* = Z_0(0.119 - j6.821)$$
$$Z_{\text{load}}* = Z_0(0.447 - j10.191),$$

using (2.32) to calculate the maximum available bandwidth for reflection coefficients of 0.2($\text{VSWR} = 1.5:1$) and 0.333($\text{VSWR} = 2:1$) gives

$$\text{BW}_{\text{source}}\Big|_{\Gamma_m=0.2} = 3.405\% \tag{5.1}$$

$$\mathrm{BW_{load}}\Big|_{\Gamma_m=0.2} = 8.5\% \tag{5.2}$$

$$\mathrm{BW_{source}}\Big|_{\Gamma_m=0.333} = 4.984\% \tag{5.3}$$

$$\mathrm{BW_{load}}\Big|_{\Gamma_m=0.333} = 12.53\%. \tag{5.4}$$

The results in (5.1)-(5.4) show that the bandwidth is very limited, and for some cases lower than the wanted 500 MHz, which is equal to 6% bandwidth. It should also be emphasized that the Bode-Fano criterion gives a theoretical maximum bandwidth, only possible to obtain with an $\mathrm{N^{th}}$-order ideal matching network.

Since it seemed impossible to make a good match over the entire bandwidth, a decision was made to decrease the bandwidth to be able to increase the quality of the matching over that bandwidth, and thus be able to get as much efficiency, gain and power out as possible. The signal bandwidth of 50 MHz is the absolute minimum bandwidth acceptable, but it should be made as wide as possible without compromising the characteristics of the PA. As a step in narrowing the bandwidth the order of the matching networks was reduced, as lower order matching networks are more common to match for smaller bandwidths.

All designs were designed for a number of parameters including efficiency, linearity and gain. These were simulated through small signal simulations, single-tone harmonic balance simulations and two-tone harmonic balance simulations with a 100 kHz tone spacing. The resulting design characteristics are shown in table 5.4-5.7.

5.5.1 Design 1: Wilkinson Feeding With Quarter Wave Stepped Impedance Matching

First the stability network shown in figure 5.11 was added at the gate side of the Wilkinson divider. It is wanted to only do stabilization at the gate side of the circuit as stabilization at the output would result in loss of output power. The geometry and component values of the stabilization network had to be

altered from the previous design in appendix B to ensure unconditional stability.

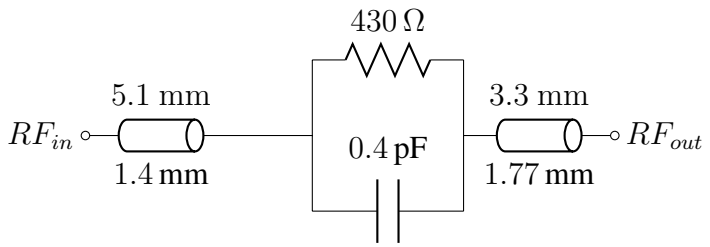


Figure 5.11: Schematic of the stabilization circuit for the Wilkinson feeding network. For the transmission lines the dimension over the line denotes width, while the dimension under the line denotes length.

As a result of the calculations done in 5.5 changes were made to an already existing quarter wave stepped impedance matching network. The quarter wave stepped impedance matching network is mostly used as a wideband matching network, but as the wideband matching was unsatisfactory it was altered in order to do matching for a narrower band with the same network. The finished circuitry includes both stabilization, harmonic tuning and matching is shown in figure 5.12. Simulated specifications for the design are shown in table 5.4.

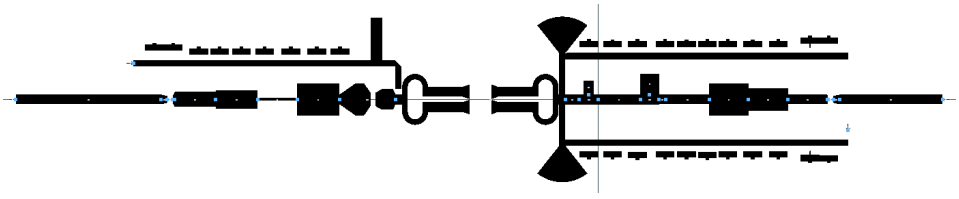


Figure 5.12: Layout of the design based on a Wilkinson divider, with stabilization circuitry and quarter wave stepped impedance matching.

Table 5.4: Simulated specifications of Design 1

Small signal test	
Small Signal Gain	14.40 dB
-3dB bandwidth	8.175-8.280 GHz
Single tone test	
-3dB compression point @ 8.20 GHz (Output power)	45.75 dBm
Power Added Efficiency @ 8.20 GHz	42.2 %
Two tone test	
3^{rd} order IMD (47 dBm output power) @ 8.20 GHz	low: -14.35 dBc
	high: -14.31 dBc
Power Added Efficiency @ 8.20 GHz	36.46 %

5.5.2 Design 2: Wilkinson Feeding With Short-circuit Stub Matching

Since the matching was done for a relative narrow band, it was no reason to use wideband matching techniques. Instead a microstrip matching network with short-circuited stub lines was used. Short-circuited stubs were used instead of open-circuited stubs, as it is easier to obtain a good short-circuit than a good open circuit[19, p. 162]. It was also observed that short-circuited stubs ensure low-frequency stability in the RFPA-circuit. Because of this, the use of stability networks was considered unnecesary, as simulations proved that the circuit was unconditionally stable for all frequencies. This allowed for lower loss in the circuit and should thus allow for better efficiency. The finished layout of design 3 is shown in figure 5.13. Specifications for the design are shown in table 5.5.

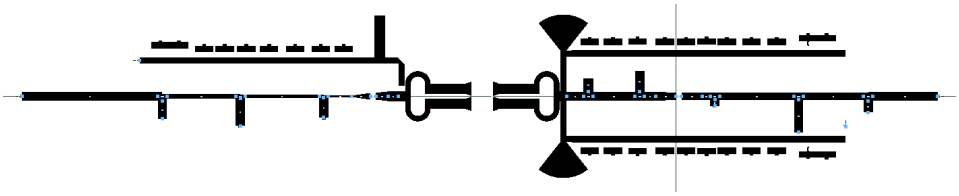


Figure 5.13: Layout of the design based on a Wilkinson divider, without stabilization circuitry and with short-circuit stub matching.

Table 5.5: Simulated specifications of Design 2

Small signal test	
Small Signal Gain	14.525 dB
-3dB bandwidth	8.145-8.265 GHz
Single tone test	
-3dB compression point @ 8.20 GHz (Output power)	45.4 dBm
Power Added Efficiency @ 8.20 GHz	42.4 %
Two tone test	
3rd order IMD (47 dBm output power) @ 8.20 GHz	low: -15.62 dBc high: -15.54 dBc
Power Added Efficiency @ 8.20 GHz	37.57 %

5.5.3 Design 3: Stabilized Bus-Bar Feeding With Short-circuit Stub Matching

A new stability network was placed at the input side of design based on the new Bus-Bar divider. A schematic of this network is shown in figure 5.14, and ensures unconditional stability for the RFPA.

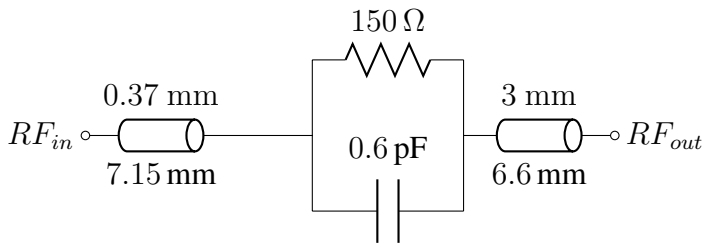


Figure 5.14: Schematic of the stabilization circuit for the Bus-bar feeding network. For the transmission lines the dimension over the line denotes width, while the dimension under the line denotes length.

The matching network was chosen to be a short-circuit stub network for the same reason as descibed for the Wilkinson design. By matching for a more narrow band, it was seen that higher gain and efficiency was achieved than what was possible with the 500MHz bandwidth. The finished layout of design 3 is shown in figure 5.15. Specifications for the design are shown in table 5.6.

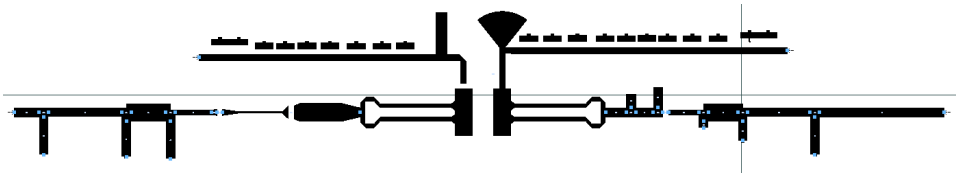


Figure 5.15: The layout of the design based on the Bus-Bar divider, with stabilization circuitry and stort-circuit stub matching.

Table 5.6: Simulated specifications of Design 3

Small signal test	
Small Signal Gain	14.60 dB
-3dB bandwidth	8.18-8.30 GHz
Single tone test	
-3dB compression point @ 8.28 GHz (Output power)	45.5 dBm
Power Added Efficiency @ 8.28 GHz	44.65 %
Two tone test	
3^{rd} order IMD (47 dBm output power) @ 8.28 GHz	low: -16.24 dBc high: -16.16 dBc
Power Added Efficiency @ 8.28 GHz	39 %

5.5.4 Design 4: Unstabilized Busbar Feeding With Short-Circuit Stub Matching

As for the Wilkinson design, it was observed that the short-circuit shunt lines stabilized the design based on the Bus-Bar feeding network to such extent that even without a designated stabilization network the circuit was unconditionally stable. Because of this the stabilization network was removed, and the matching network was redesigned and should thus yield a higher efficiency than in the design with stabilization circuitry. The finished layout of design 4 is shown in figure 5.16. Specifications for the design are shown in table 5.7.

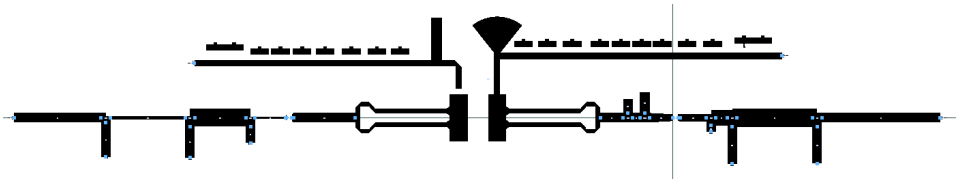


Figure 5.16: The layout of the design based on the Bus-bar divider, without stabilization circuitry and with short-circuit stub matching.

Table 5.7: Simulated specifications of Design 4

Small signal test	
Small Signal Gain	13.03 dB
-3dB bandwidth	8.095-8.275 GHz
Single tone test	
-3dB compression point @ 8.18 GHz (Output power)	45.75 dBm
Power Added Efficiency @ 8.18 GHz	45.73 %
Two tone test	
3^{rd} order IMD (47 dBm output power) @ 8.18 GHz	low: -16.51 dBc high: -16.59 dBc
Power Added Efficiency @ 8.18 GHz	40 %

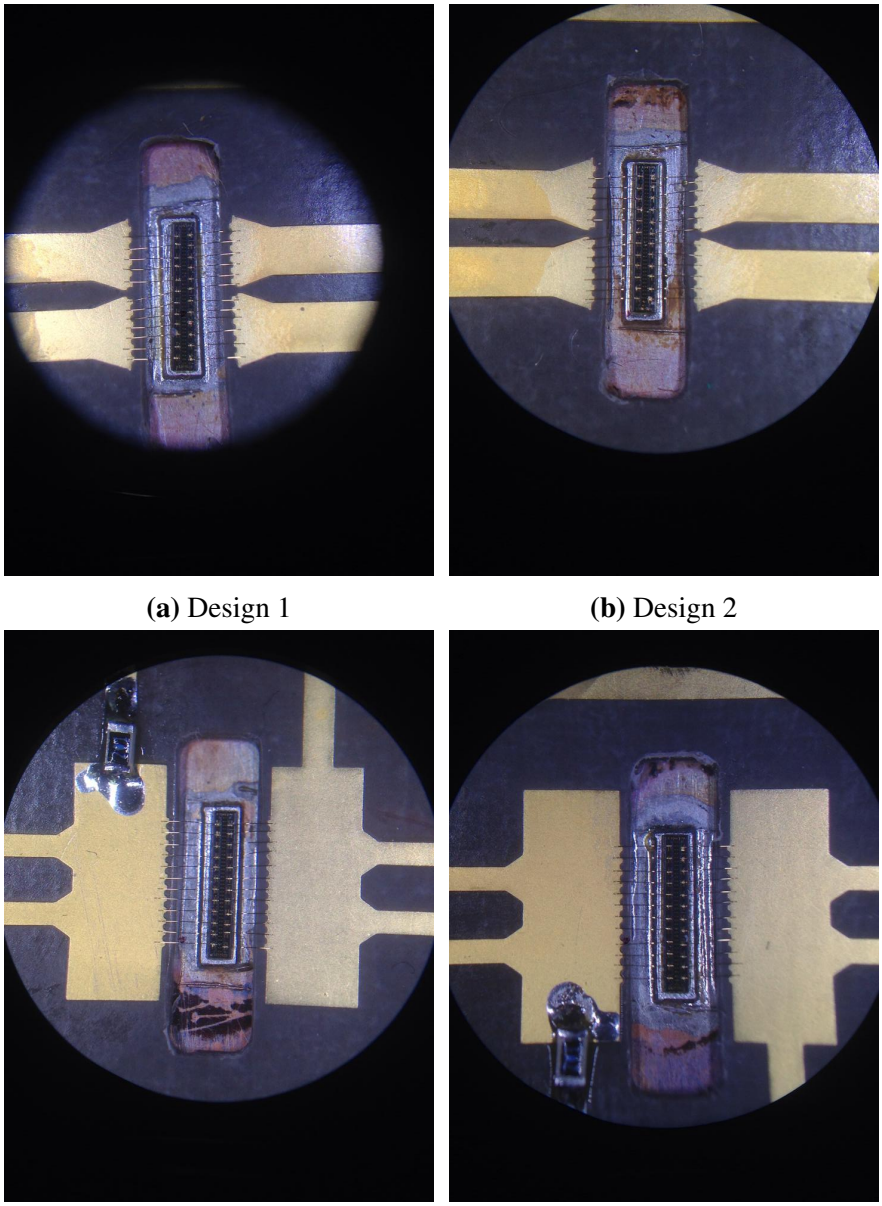
5.5.5 New Test Card

Due to the unsatisfactory production of the test card in 4.4 it was decided to use a professional PCB manufacturer. The new test card was produced by Multech PCB Technologies Co. Limited on assignment from Elmatica AS, following production standards as described in Appendix D. The Cu on the card was surface finished using ENEPIG[30] to enable gold wire bonding and prevent oxidation. The bottom side of the test card was partially covered by a solder mask to make the production costs lower, but at the same time openings in the solder mask were made to ensure connection between the card and cooling plate, and make a well defined ground plane on the bottom side of the card. All screw holes are 3 mm in diameter and have been side plated to ensure electric contact between the cooling plate and the card. All via-holes are 0.3 mm in diameter and have been filled with epoxy.

Chapter 6

Measurements and results

The new test card was prepared in the same way as the previous test card, meaning the same Cu-cooling plate was used, and new transistors were soldered to the elevated pads. Etching of the PCB led to a much higher detail level and thus enabled use of the bonding pads originally designed in the Bus-bar and Wilkinson feeding topologies. This resulted in bonding wires which resembled the bonding wire model to a much higher extent than earlier. In addition the etching did not remove any of the substrate in difference from the milling process on the first test card. This can be seen in figure 6.1. Thus there should be much more consistency between the inteded circuit and the finished PCB manufactured by Multech PCB Co. Ltd. Together with the manufactured test card followed a measurement table showing the actual thickness of the sheets on the substrate(seen in Appendix C), and these parameters were changed in the simulations, so that the simulations use the actual manufactured parameters. For the simulations this only resulted in very small, neglectable changes in simulation results.



(a) Design 1 **(b)** Design 2

(c) Design 3 **(d)** Design 4

Figure 6.1: Close up of transistor and card showing how much better detail level was obtained using etching istead of milling.

Measurements of S-parameters were performed using the Agilent N5245A

Programmable Network analyzer(PNA)[11] in FFIs microwave lab at Kjeller. Since the PA circuits were made with internal DC-biasing circuits there were no need for external bias tees. To prevent damage on laboratory equipment a total of 23 dB attenuation was added to the output port, using a 100W 20dB attenuator[13] in series with a 2W 3dB attenuator[15]. The maximum possible output power was then reduced to $25.45\ \mathrm{dBm}$, $4.55\ \mathrm{dB}$ below the maximum input power of the PNA. The full measurement setup is shown in figure 6.2

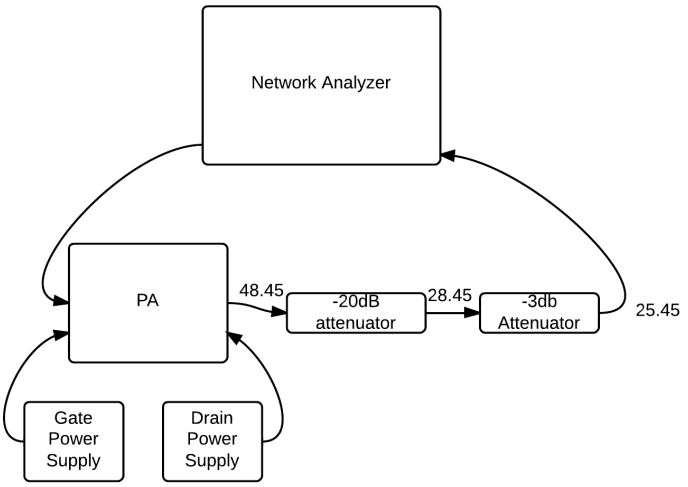
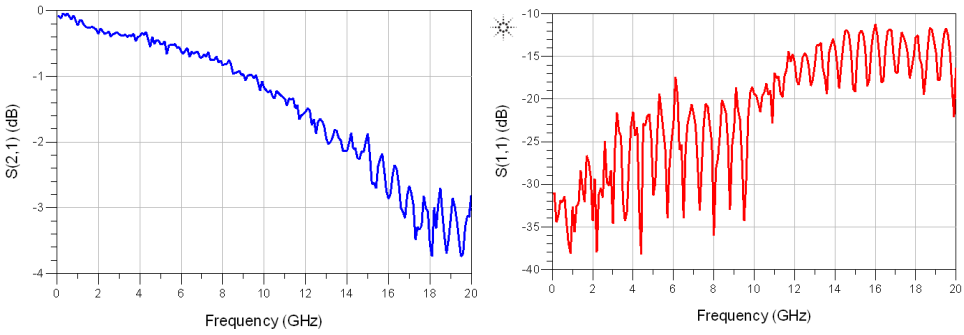


Figure 6.2: Test setup for measurements with the PNA. All numbers are absolute maximum power levels in dBm.

The test frequency range was set to $10\ \mathrm{MHz} - 20\mathrm{GHz}$ using 1000 measuring points and an IF-bandwidth of $10\mathrm{kHz}$. Calibration was performed using an Agilent N4693-60001 Electronic Calibration Module(ECal)[10], calibrating away the attenuators and wires used in the measurement setup. As a test for both the calibration and the production quality of the PCB, measurements of the thru line at the bottom of the test card were performed before measuring the rest of the circuits.



(a) S_{21} measurements in dB of the thru line on the test card, over the frequency range of 0-20 GHz.

(b) S_{11} measurements in dB of the thru line on the test card, over the frequency range of 0-20 GHz.

Figure 6.3: Forward travelling S-parameters of the thru line on the test card.

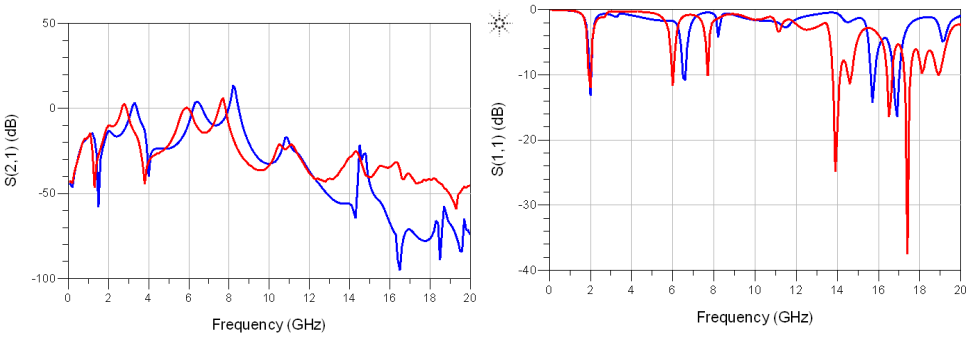
The measurements in figure 6.3 show expected behaviour and the signal is transmitted over the 50 Ω line with increasing loss as the frequency increases, which is to be expected. These measurements serve as a good validation of the calibration. The measurement results of the four PA designs are summarized in table 6.1.

Table 6.1: Results from small signal measurements of the power amplifier designs.

Small signal measurements		
	Gain	-3dB bandwidth
Design 1	6.365 dB	7.58-7.77 GHz
Design 2	2.638 dB	7.56-7.72 GHz
Design 3	2.279 dB	7.82-8.11 GHz
Design 4	4.5dB	N/A

6.1 Design 1

Measurements and simulations of design 1 with a Wilkinson divider and stepped impedance matching networks are shown in figure 6.4



(a) S_{21} measurements(red) and simulations(blue) in dB of design 1 on the test card, over the frequency range of 0-20 GHz.

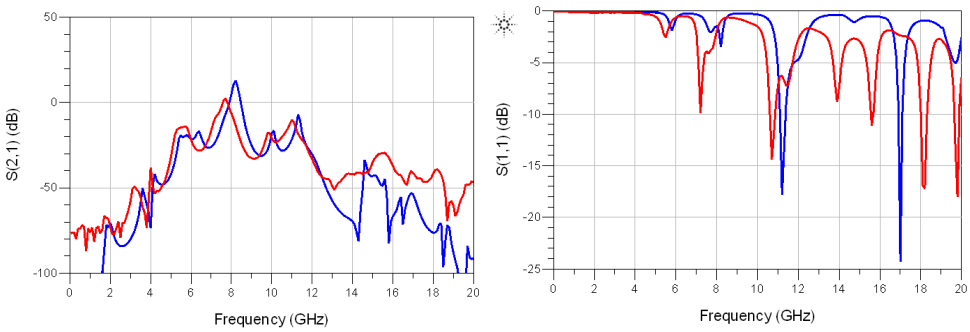
(b) S_{11} measurements(red) and simulations(blue) in dB of design 1 on the test card, over the frequency range of 0-20 GHz.

Figure 6.4: Forward travelling S-parameters of design 1 on the test card.

It can be seen from figure 6.4a that measurements are shifted in frequency compared to the simulations, and that the wanted amplification in band is not met. The measurements precede the simulations in terms of frequency for the entire measurement bandwidth, and the largest gain seen in the measurements is 6.365 dB at 7.68 GHz. This gives approximatel 8 dB lower gain and at a frequency over 500 MHz lower than what was simulated.

6.2 Design 2

Measurements and simulations of design 2 with a Wilkinson divider and short circuit stub matching networks are shown in figure 6.5



(a) S_{21} measurements(red) and simulations(blue) in dB of design 2 on the test card, over the frequency range of 0-20 GHz.

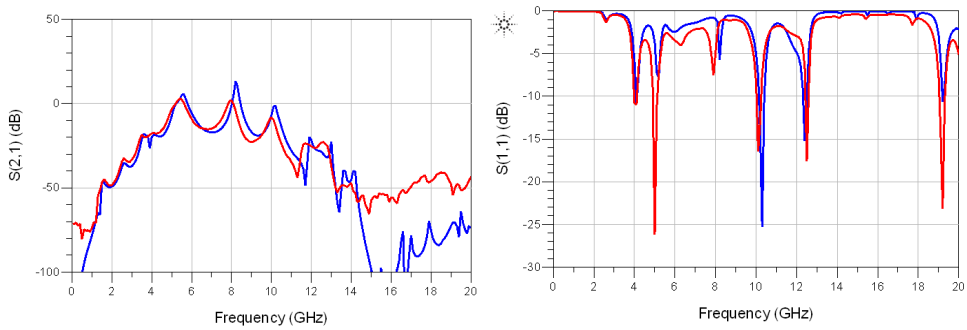
(b) S_{11} measurements(red) and simulations(blue) in dB of design 2 on the test card, over the frequency range of 0-20 GHz.

Figure 6.5: Forward travelling S-parameters of design 2 on the test card.

Measurements precede the simulation results in frequency, as was the case for design 1. The measurement show a maximum gain of 2.638 dB at 7.65 GHz. The gain in the frequency band of interest is negative.

6.3 Design 3

Measurements and simulations of design 3 with a Bus-bar divider and stabilized short circuit stub matching networks are shown in figure 6.6



(a) S_{21} measurements(red) and simulations(blue) in dB of design 3 on the test card, over the frequency range of 0-20 GHz.

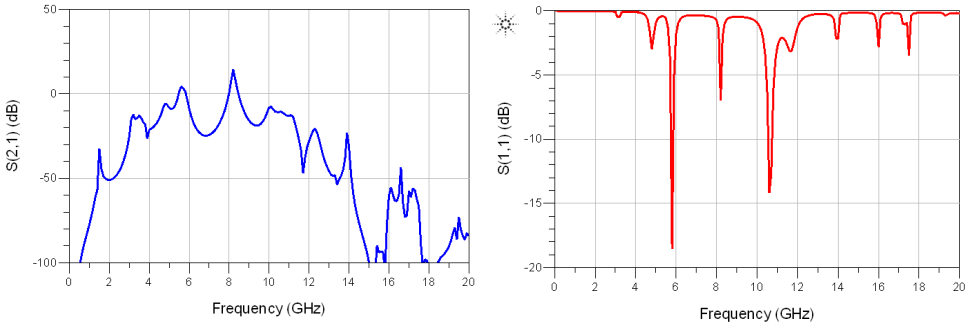
(b) S_{11} measurements(red) and simulations(blue) in dB of design 3 on the test card, over the frequency range of 0-20 GHz.

Figure 6.6: Forward travelling S-parameters of design 3 on the test card.

These measurement follow simulations much closer than what was the case for the Wilkinson based designs(design 1 and 2). However, the deviations increase with frequency, and the gain in band is not as indicated in simulations. The highest gain obtained for this design was 2.279 dB at 7.9 GHz.

6.4 Design 4

Due to a mishandling causing a short circuit between the bias network and ground, the capacitors in the bias network discharged over a small area of the microstrip line and this caused it to vapourize. Due to this it was no longer possible to use the circuit and no measurement results were saved. Therefore only simulation results of design 4 with a Bus-bar divider and stabilized short circuit stub matching networks are shown in figure 6.7



(a) S_{21} simulations in dB of design 4 on the test card, over the frequency range of 0-20 GHz.

(b) S_{11} simulations in dB of design 4 on the test card, over the frequency range of 0-20 GHz.

Figure 6.7: Forward travelling simulated S-parameters of design 4 on the test card.

Before the damage the main results were visually confirmed by looking at the display of the PNA. The design followed the same tendencies as for the other Bus-bar design, and had about 4.5 dB gain at at approximately 8 GHz.

It was the initial intention to perform large signal measurements on the PA designs, but with no gain in the desired bandwidth and too large deviations between simulated and measured results these were not performed. This was due to the fact that non of the designs worked as intended.

Chapter 7

Discussion

The inaccuracies in the first measurements were believed to be caused by inaccuracies in the milling of the substrate which removed the bonding pads in the designs and thus forced the bonding wires to be much longer than intended. By modifying the bondwire model after the measurements in chapter 4, a quite good correspondence was obtained between the measured and simulated S-parameters for both the Wilkinson and Bus-bar designs. The remaining differences in the first measurements were believed to be due to the milling altering shapes of the microstrip and removing part of the substrate. It was therefore assumed that a better bonding wire model and better production accuracy would improve measurement to simulation correlation.

During the design procedure of the PAs it became clear that the desired bandwidth would be difficult to achieve. It is believed that the distance between the transistors and matching network could cause this to happen, as standing waves between the matching network and transistor could occur. It is also possible that the feeding networks make a non-beneficial impedance transformation, making a very high-Q impedance seen towards the transistor outside the feeding network. A better design procedure to have would probably be to match each of the 12 transistors on the die seperately, before the feeding network. This would not have been possible using the RT/duroid 5880 substrate, but an other substrate with large dielectric constant or thin film matching could have been used. This was however considered as very time consuming and expensive, and was hence not per-

formed. This would also require use of a more precice transistor model, having 12 input and output ports.

The second test card produced by Multech PCB Co. Ltd. showed that etching gave much better quality and detail level, and the card was much better than the first test card. Due to this the bonding wire model was better approximated to the actual bonding wires on the test card. The producer provided measurements for actual copper trace thickness and substrate thickness, and other parameters, shown in appendix C. These values were incorporated in the simulations, and the difference was very small from what was originally intended. Despite this, the measurement results were inferior to the simulation results. For design 1 and 2, the Wilkinson divider based designs, the measurements preceded the simulations in terms of frequency, seen both in the S_{21} and S_{11} measurements. The designs show very low gain and at a lower frequency than what was intended. For the Bus bar based designs (Design 3 and 4) the measurement results are much more consistent with the simulation results, but the gain peaks that is present in the simulations are not present in the measurements. This resulted in 4 PA circuits not behaving as they were designed to do. It is the authors belief that the fact that it was only possible to match the PA to a very narrow band made the designs vulnerable to small changes, and thus caused a number of small innaccuracies to change the characteristics of the circuit enough to contribute to at least some of the deviation between measurements and simulations.

One problem that did not occur however, was odd-mode oscillations. It seems that the measures taken to prevent these by using the feeding networks have succeeded in stopping these oscillations from occuring. But, since only small signal measurements were executed there is no way of guaranteeing that oscillations would not occur if the power level was increased.

EM-modelling of the feeding networks were performed on the finished designs. This was done to increase the accuracy of the simulations and better resemble the reality. However, this was not done for the matching network and DC-biasing networks, as the iterative procedure of making a matching network or bias network would go very slow with EM-simulation of the networks for each time. An EM-simulation of the feeding network

used approximately 4 hours, and with the data power available it would be too time consuming to do a design procedure based on EM-simulations. The matching and biasing networks were therefore made using known microstrip models in ADS. This should be sufficient, but some deviations could have occured because of this.

Plextek RFI have made a PA design based on CREEs $0.25\mu m$ transistors and developed a distributed transistor model of the CGHV1J025D[2]. This was again utilized in their PA design. Compared to the single-input-single-output transistor model delivered by CREE used in this design, a transistor model like this has great benefits. The designer have more control over the impedances displayed at each port in adddition to being able to split and combine signals. Also the distributed model will be a much better approximation when the periphery gets large compared to the wavelength. The design team at Plextek RFI have used this information to their advantage and made a PA design based on the CGHV1J025D at 11 GHz[16]. The transistor model of the CGHV1J070D transistor provided by CREE Inc. only has one input port and one output port, despite the fact that the transistor itself has twelve input ports and output ports. With regard to the measurements done in this thesis, it is reasonable to believe that a transistor model such as the one developed by Plextek RFI is crucial, if not vitally necessary in order to model the transistor correctly. Especially for frequencies where the periphery of the transistor die is electrically large an approximation with one input and output will not be sufficient. It could also enable stability analysis that could make it possible for the designer to prevent odd-mode oscillations. Unfortunately a distributed transistor model was not available.

Although the problem of this master thesis evolved around the CGHV1J070D transistor die it should be noted that a design with another transistor(or a parallel topology with several transistors) could serve the same purpose as the current transistor. The CREE CGHV96050F1[7] or CMPA5585025D[8] could be good alternative transistors. To make a design based on these transistors would probably be a much easier job for the designer, as these transistors are pre-matched to 50Ω. This thesis has shown that to make a power amplifier design based on the CGHV1J070D is very difficult, and even with very high production precision there is no guarantee of success.

Chapter 8

Conclusion

Four different feeding networks were presented as a way of combining signals from the CGHV1J070D transistor die as ideally as possible. The feeding networks based on a Wilkinson divider and Bus bar showed the best properties and potential, and four PA designs were made based on these two feeding topologies.

During measurements none of the four PA designs showed expected characteristics, and none of them fulfilled the desired specifications. Different reasons for the deviations have been discussed, including the impedance transforming properties of the feeding networks, the distance between the matching network and transistor, the production inaccuracies and the single input- single output transistor model.

In essence, the thesis fail to present a functioning PA design based on the CGHV1J070D transistor. It has been proved to be very difficult to present measurement results that fully reflect what have been modeled and simulated, and with the extensive work and amount of money put into making test cards this is most probably due to the fact that the simulations were unable to fully reflect the real life situation.

What have been shown however, is that it is possible to create a PA design which does not have any odd-mode oscillations, even for higher frequencies. This is due to the feeding networks connecting all of the 12 transistors together at input and output.

Future work on the PA module should, in the view of the author, consist of finding other transistors that could serve the same purpose as the CGHV1J070D. Examples as CMPA5585025D and CGHV96050F1 have been presented, and these two transistors have large benefits over the present transistor as they are pre-matched to 50Ω, and thus the design procedure would be much easier.

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Appendix A

Bias Tees

The bias tees used in the measurements were made by Morten Olavsbråten using a band stop filter and a capacitor as the main components. It should be able to handle an as high power as the circuit itself, and the isolation between the RF path and the DC input should be as large as possible for an as large as possible bandwidth around 8 GHz. The circuit can be seen in figure A.1

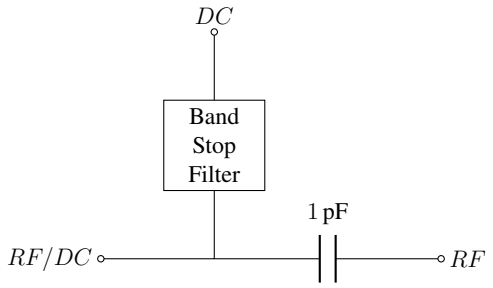
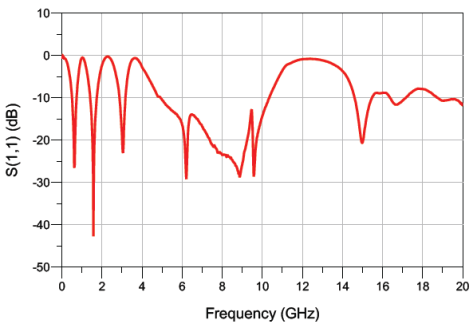
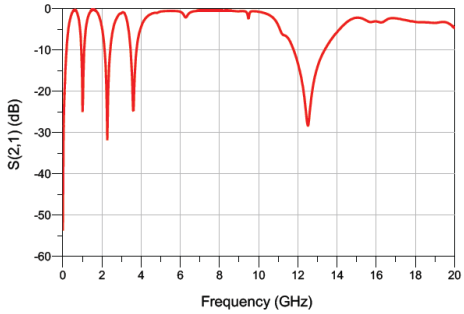


Figure A.1: The build-up of the bias tees. It has one port with combined RF and DC, one for DC input and one RF output which is DC blocked.

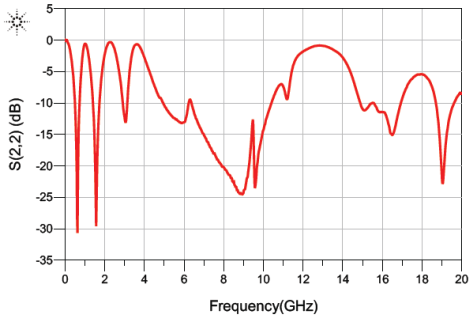
The S-parameters of the RF-path were measured by the PNA on both bias tees to ensure that there was a good isolation between the RF-path and DC path. The results are shown in figure



(a) S_{11} of the drain bias network in dB over the frequency range of 0-20GHz

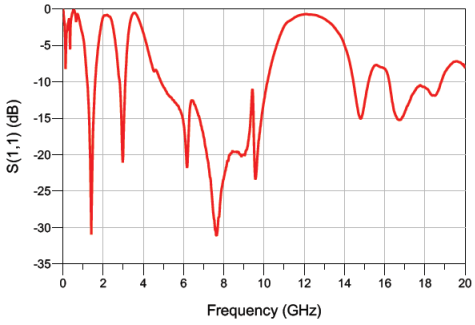


(b) S_{21} of the drain bias network in dB over the frequency range of 0-20GHz

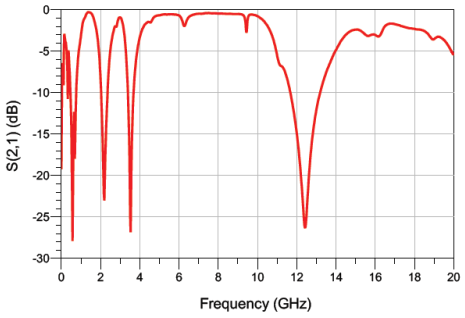


(c) S_{22} of the drain bias network in dB over the frequency range of 0-20GHz

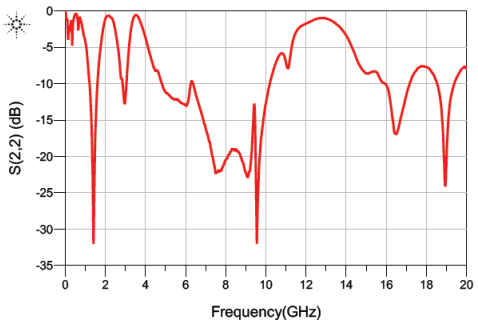
Figure A.2: S-parameters for the drain bias network



(a) S_{11} of the gate bias network in dB over the frequency range of 0-20GHz



(b) S_{21} of the gate bias network in dB over the frequency range of 0-20GHz



(c) S_{22} of the gate bias network in dB over the frequency range of 0-20GHz

Figure A.3: S-parameters for the gate bias network

In the measurements port 1 is the RF/DC port, while port 2 is the RF port.

As can be seen from the measurements above, the bias networks has a good transmission(S_{21}) over the band of 4-11 GHz, but there are some fluctuations and dips in the frequency responce, just above 6 GHz and at 9.5 GHz. These dips seem to be larger for the gate bias network and can infect the measurements in these frequencies. The gate bias was equiped with some large decoupling capacitors due to oscillations, and these can be seen to have an effect on the frequencies below approximately 0.5GHz. Also there are large dips in the transmission in several frequencies(0.5, 2, 3.5 and 12.5 GHz) that will affect the measurement in the way that the loss on these frequencies are so large that the signal might be close to the lower

edge of the dynamic range of PNA.

Appendix B

Feeding Networks

B.1 Bus-Bar Combiner

The bus-bar circuit was designed using a design procedure described in [32]. Although the bus-bar is originally designed for a number of 2^N transistors, an approximation has been done in this case, viewing a bunch of 3-and-3 transistors as a single transistor. This should be a valid approximation as the symmetry of the bus-bar is still obtained. Designing the bus-bar to be wide(2.1mm) opens for the posibility to connect the bias network directly onto it. The tree combiner uses two combining points, as this is the maximal amount with the approximation of $12/3 = 4$ devices. The signal is combined at the transistors symmetry points, so that, ideally, no power is lost in the combination procedure. The combination points have also been widened in an attempt to further validate the 4-transistor assumption by decreasing the phase-difference for the 3 ”bundled” transistors. The finished design of the bus-bar is shown in figure B.1.

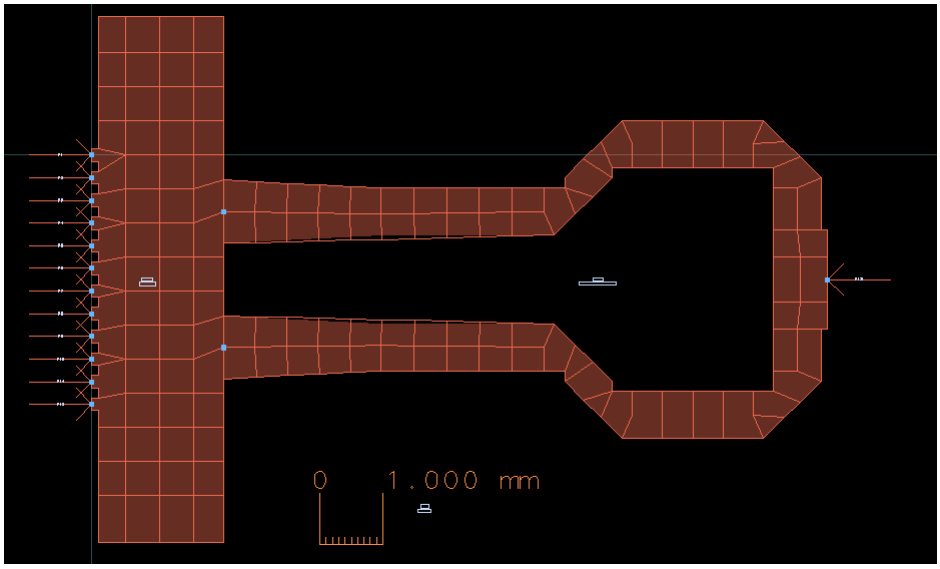


Figure B.1: The layout of the bus-bar design, with the 12 inputs from the transistors on the left, and output to the rest of the circuitry on the right.

The bus-bar was utilized as both output feeding and input feeding to the transistor, and the transistor has been stabilized using the stabilization circuit in 2.8. The circuit schematic is shown in figure B.2. The finished design layout was adapted to test-card dimensions and is shown in figure B.3, where the stabilization circuitry can be seen to the left of the bus-bar on the input of the die.

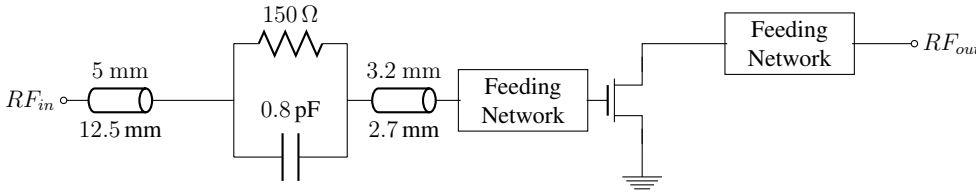


Figure B.2: The final circuit schematic of the bus-bar design. Value over transmission line denotes width, while value beneath denotes length.

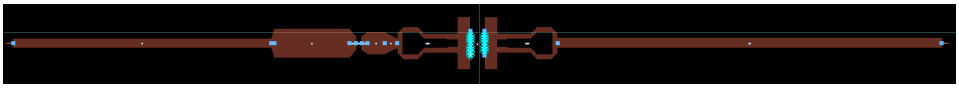


Figure B.3: The layout of the PA design based on the bus-bar feeding topology, input to the left and output to the right.

B.2 Wilkinson Combiner

By using the well known Wilkinson coupler topology, the signal is divided into two branches, and feed half the transistor with each branch in equiphase. This makes the feeding of the die much more in-phase than with a single feeding point, as has been shown in Appendix E. In addition to the Wilkinson divider which consist of two 70.7Ω lines and a 100Ω resistor, each branch has 50Ω lines which had to be widened in the end to make room for the bonding wires. The circuit can be seen in figure B.4.

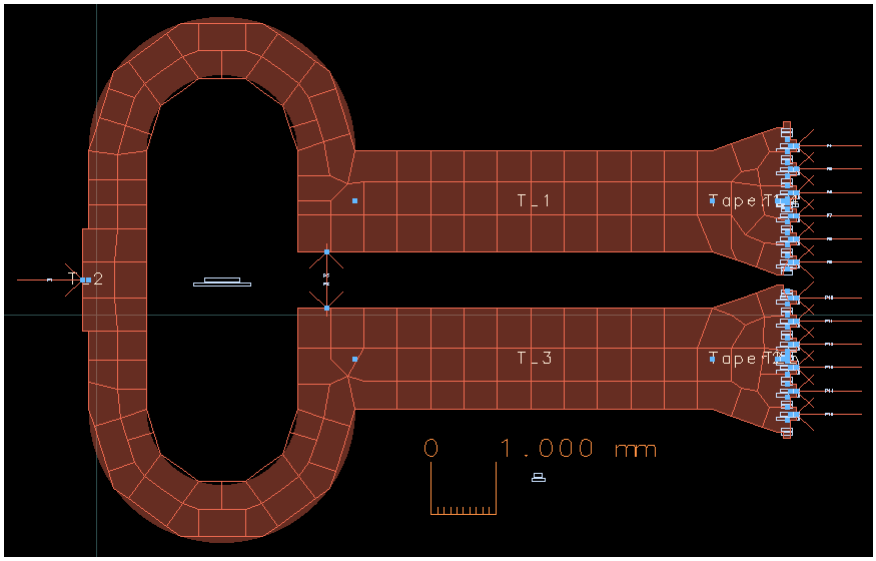


Figure B.4: The layout of the Wilkinson combiner design, with the input to the left, and the 12 outputs to the die to the right. Note that a 100Ω resistor will be placed between the two ports in the middle of the layout.

The Wilkinson combiner was used as the feeding topology on both sides

of the die. The design has been stabilized using the stabilization circuit in 2.8 on the input side of the die, and the finished design schematic can be seen in figure B.5, while its layout is shown in B.6.

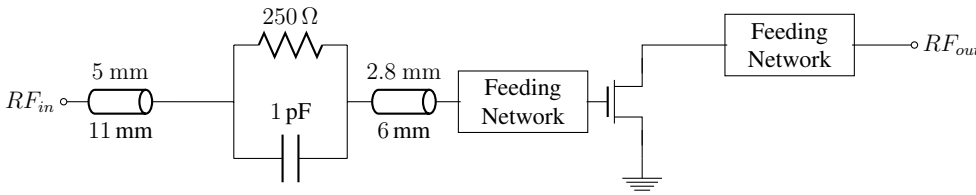


Figure B.5: The final circuit schematic of the Wilkinson design. Value over transmission line denotes width, while value beneath denotes length.

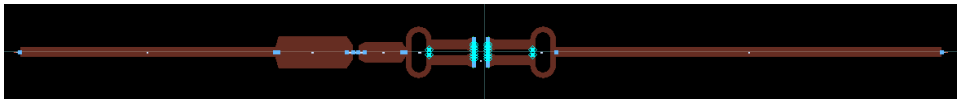


Figure B.6: The finished design based on the Wilkinson combiner feeding topology, input to the left, output to the right.

B.3 Taper

A design was made using a simple tapered microstrip line i.e. a widening of the line. This should be able to give less phase differences, shown in Appendix E.3. The topology uses a line that increases from 1.569 mm to 4.16 mm over a length of 2.5 mm. The layout of the design is shown in figure B.7.

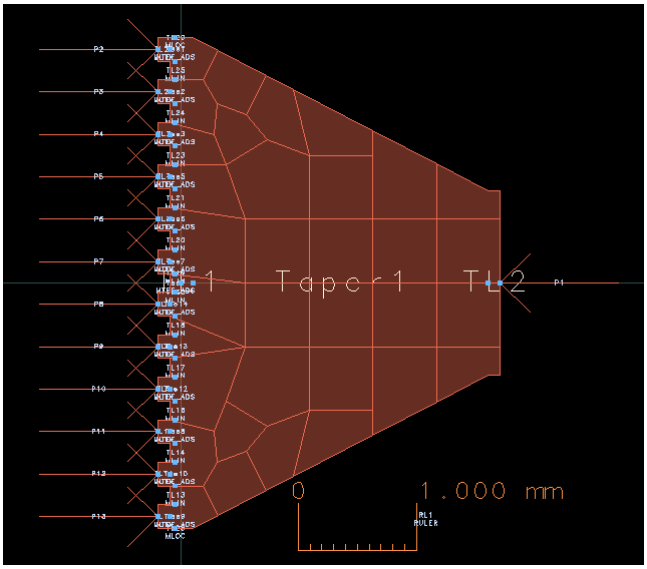


Figure B.7: The simple taper topology, with input to the right, and the 12 outputs to the die to the left.

The taper topology was utilized to in a PA design, with the stabilization circuit shown in 2.8 with values adapted to make the design unconditionally stable. The finished design schematic is shown in figure B.8. The design was adapted to test-card dimentions, and the layout is shown in B.9

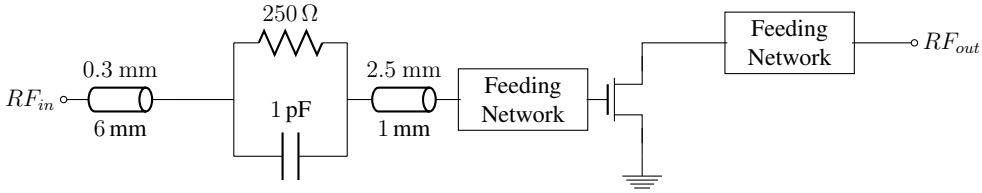


Figure B.8: The final circuit schematic of the bus-bar design. Value over transmission line denotes width, while value beneath denotes length.

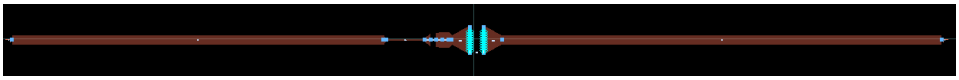


Figure B.9: The PA design based on the taper feeding topology, with stabilization to the left of the tapers. Input to the left, and output to the right.

B.4 Branch-Line Coupler

A design based on the branch-line coupler was made. The difference from the other feeding topologies previously designed, is that the branch -line coupler gives a balanced output, where the main output port and the coupled port have signals that are 90 degrees out of phase. The 50Ω termination of the isolated port is realized by a 50Ω resistor in series with a $1pF$ capacitor to ground, where the capacitor acts as a DC-block. The design of the branch-line coupler is shown in figure B.10.

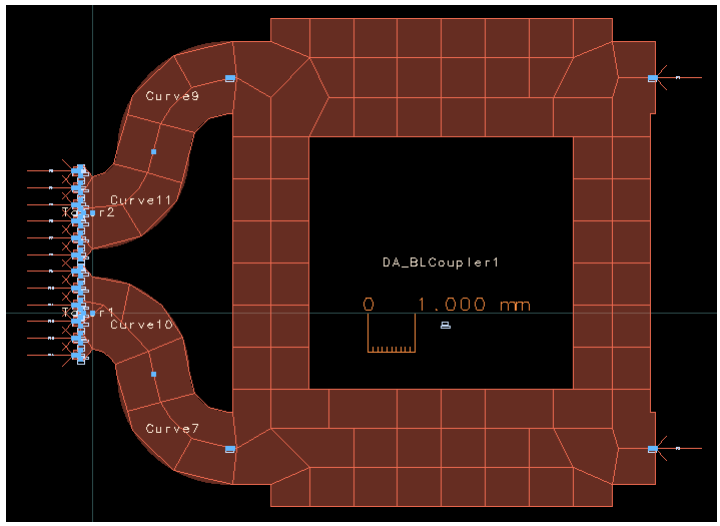


Figure B.10: The layout of the branch-line coupler design, with the 12 outputs to the transistors on the left, and output to the rest of the circuitry on the top right(dividing port) and bottom right(combining port).

The branch-line coupler has been used in a PA design shown in figure B.11. The circuit is stabilized to be unconditionally stable. Since the transistor model for the die only has one input and output, it is impossible to model the balanced signal, as the signal would have to be combined at the input and output of the transistor model. To be able to simulate the balanced feeding of the die, two instances of the transistor model for the CREE CGHV1J025D[2] was used as a approximation, as it is a smaller die based on the same $0.25\mu m$ gate length production process. The layout of the circuit is shown in figure B.12.

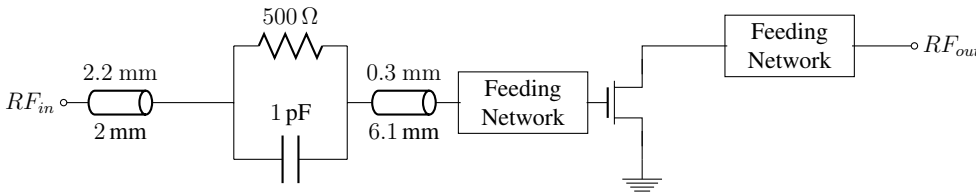


Figure B.11: The final circuit schematic of the bus-bar design. Value over transmission line denotes width, while value beneath denotes length.

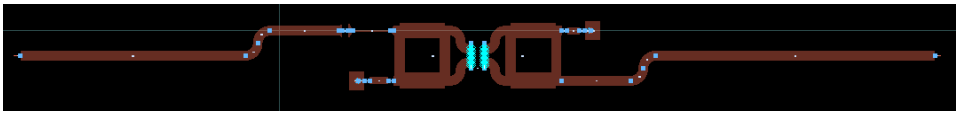


Figure B.12: The layout of a PA design based on the branch line coupler. Input to the left, ouput to the right, and stabilization circuitry to the left of the branch line coupler.

Appendix C

Production Report

MULTECH PCB TECHNOLOGIES CO.,LIMITED
艾尔特线路科技(HK)有限公司
Homepage: www.multech-pcb.com
E-mail:marketing@multech-pcb.com UL:E320829

样品承认书
First Article Report

客户名称：
Customer name A002

客户型号：
Customer P/N RT5880 20mil

产品编号：
Product No

交货日期：
Date of Shipment 2014-5-26

供应商承认(Approved by Supplier)		供应商签章 (Stamp by Supplier)	客户承认 (Approved by customer)			客户签章 (Stamp by customer)
部门(Dept)	品质 (QA)		部门 (Dept)	工程 (Engineering)	品质 (QA)	
签名 (Signature)	WILLAIM					

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艾尔特线路科技(HK)有限公司
Homepage: www.multech-pcb.com
E-mail:marketing@multech-pcb.com,UL:E320829

CERTIFICATION OF COMPLIANCE

Dear Customer:

This is to certify that the enclosed material have been manufactured and inspected in . accordance with customer drawing and specification.All units have found to meet, or exceed the required specifications which include the construction, dimension and raw material. And the following parameter(s) of testing is performed on 100% basis in compliance with customer specification.

ITEM/项目	DESCRIPTION/说明	ACTUAL/结果
1	Customer name/客户名称	A002
2	Customer P/N/客户型号	RT5880 20mil
3	Internal P/N/厂家生产编号	
4	Customer P/0/客户订单号	OR0013189
5	Shipment quantity/交货数量	2 PCS
6	Inspection standard/检查标准	IPC-6012C CLASS2、IPC-A-600H CLASS2
7	UL plame class/UL 耐燃级别	94V-0
8	Our UL designation/UL 标示("兄"字)	
10	Laminate type/板材类型	RO5870/5880 (Rogers)
11	Date code /生产周期	2014
12	Ship date / 出货日期	2014-5-26
13	Where is the product made in /产品出产地	China
14	Where compliant ROHS request/是否满足客户ROHS要求	Yes
15	Customer DWG/客户资料	

Thanks for your attention !!

Certified by : **ZHONGXING**

Quality Assurance Manager

WILLIAM

Signature

Date : 2014-5-26

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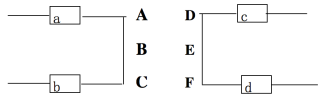
E-mail:marketing@multech-pcb.com,UL:E320829

Microsection Test Report

PROD P/N :		DATE CODE:	2014
CUSTOMER P/N :	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :	/	QUANTITY :	2 PCS

1.0 Thickness of copper/孔铜厚测试(unit:um)

Speciment location/采样位置

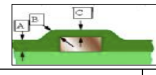


Thickness copper/铜厚 unit/单位 ：um								
Test point/测试点	request/要求	Actual/实际				surface copper thickness /表铜		
		1	2	3	4	Point/测试点	Request /要求	Actual/实际
A	≥20.3AVE25	29.6				a	≥35	45.6
B	≥20.3AVE25	26.3				c	≥35	46.3
C	≥20.3AVE25	28.9				b	≥35	43.5
D	≥20.3AVE25	29.7				d	≥35	44.8
E	≥20.3AVE25	26.1						
F	≥20.3AVE25	28.7						
Max		29.7						46.3
Min		26.1						43.5
Aver		28.2						45.05

2.0 Roughness/孔壁粗糙度 unit/单位 ：um

Request/要求	Actual/实测	ACC	Rej
≤25.4	16.3	ACC	

3.0 阻焊厚度(单位：um) **Soldermask thickness (Unit:um)**

采样位置 Speciment Location				
测试点	要求 Request	实测 Actual	ACC	Rej
A	8-30	26.3	ACC	
B	8-30	12.3	ACC	
C	8-30	20.5	ACC	

4.0 Tin/lead thickness/锡铅厚度 unit/单位：um

Request/要求	Actual/实测	ACC	Rej
无	无		

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Microsection Test Report

5.0 Medium Layer thickness/介质层厚度测量 unit/单位：um

铜厚 CU Thickness			介质层厚度 Medium Layer thickness unit/单位：um			ACC	Rej
层数	要求	实际	层数	要求	实际	ACC	
L1			L1~L2				
L2			L2~L3				
L3			L3~L4				
L4			L4~L5				

6.0 Au thickness/金厚 unit/单位：um

Request/要求	Actual/实测	ACC	Rej
Au：0.05--0.1 um	0.059	ACC	
Ni：3--5 um	3.58		
Pd： 0.05um	0.058	ACC	

7.0.Defects Inspection/缺陷检测

Item/项目	Request要求	Actual/实际	Acc	Rej
镀层裂纹 plating crack	Not found	Not found	Acc	
树脂内缩resin recession	Not found	Not found	Acc	
镀层空洞 plating void	Not found	Not found	Acc	
分层 delarmination	Not found	Not found	Acc	
钻污 smear	Not found	Not found	Acc	
铜裂缝 copper crack	Not found	Not found	Acc	
起泡 blistering	Not found	Not found	Acc	
连接面分离 interconnection separat	Not found	Not found	Acc	
基材空洞 laminate void	Not found	Not found	Acc	
灯芯 wicking	＜0.1mm	＜0.03mm	Acc	
钉头 nail heading	Not found	Not found	Acc	

Finial result : ☑ **Acc** ☐ **Rej**

Prepared by: ZHONGXING **Approved by:** WILLIAM

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ROHS COMPLIANCE CERTIFICATE

Dear Customer,

This is to certify that the Printed Circuited Boards we manufactured are complied with ROHS compliance.

PROD P/N :		DATE CODE:	2014
CUSTOMER P/N	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :	/	QUANTITY :	2 PCS

NO.	Test Item	Unit	Result
1	Chromium VI(Cr+6)	Ppm	Not detected
2	Cadmium(Cd)	Ppm	Not detected
3	Mercury(Hg).	Ppm	Not detected
4	Lead (pb)	ppm	Not detected
5	DecaBDE (Deca Brominated Diphenyl Ether)	ppm	Not detected

Checked by: ZHONGXING **Approved By:** WILLIAM

Date : 26-May-14 **Date :** 26-May-14

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ELECTRIC TEST REPORT

PROD P/N :		DATE CODE	2014
CUSTOMER P/N :	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :	/	QUANTITY	2 PCS

Quantity/数量	Test time/时间		Test Condition /测试条件	Test type/测试类型
☑ Electric ☐ Fly probe	2min/1PCS		正常条件 (温度23℃, 湿度52. 5%)	飞针
Test condition 测试条件	voltage 测试电压	250V	Conductive resistance 导通电阻	20Ω
	electricity 测试电流	10mA	Insistance resistance 绝缘电阻	20MΩ
Test Result 测试结果	Total 总数	2 PCS	Pass 合格	2 PCS
	Open 开路	0	Short 短路	0
	Thru no 导通不良	0	Insulation no 绝缘不良	0

Checked by:	**ZHONGXING**	**Approved By:**	**WILLIAM**
Date :	**26-May-14**	**Date :**	**26-May-14**

Note:we are willing to supply PCB to our customer,after get our shipment,please confirm the quality feedback within 3 months.more than 3 month's complaint from customer side,we have the right to refuse it and reject compensation. For PCBA complaint we can only accept Max.3 times of bare PCB value to afford everything consequential cost in customer side if we supplied defective PCBs to customer.please kindly note.

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Products final audit report

生产报告

PROD P/N :		DATE CODE:	2014
CUSTOMER P/N :	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :	/	QUANTITY :	2 PCS

1.0 Material/物料

Item 项目	Inspection Method 测试方法	Requirement 要求	Actual 实际	Acc	Rej
Laminate type 板材	Visual 目检	☑ FR-4 RO5870/5880 (Rogers)	☑ FR-4 RO5870/5880 (Rogers)	Acc	
		☐ PTEE	☐ PTEE		
		☐ 高-Tg	☐ 高-Tg	Acc	
		☐ 其它	☐ 其它		
Soldermask type 绿油类型	Visual 目检	☐ Tamura Dsr-2200	☐ Tamura Dsr-2200		
		☑ Nanya	☑ Nanya	Acc	
		☐ LP-4G/G-05	☐ LP-4G/G-05		
		☐ 其它	☐ 其它		
Soldermask color 绿油颜色	Visual 目检	☑ Green 绿色	☑ Green 绿色	Acc	
		☐ red 红色	☐ red 红色		
		☐ black 黑色	☐ black 黑色		
		☐ dark green 亚色绿油	☐ dark green 亚色绿油		
		☐ 其它	☐ 其它		
C/M Type 字符	Visual 目检	☑ KSM-388	☑ KSM-388	Acc	
		☐ ASR-150	☐ ASR-150		
		☐ 其它	☐ 其它		
C/M Color 字符颜色	Visual 目检	☐ Yellow 黄色	☐ Yellow 黄色		
		☑ white 白色	☑ white 白色	Acc	
		☐ 其它	☐ 其它		
Peelable soldermask 可剥离兰胶	Visual 目检				

2.0 Board thickness Measurement/板厚测量 unit/单位：mm

Item 项目	Inspection Method 测试方法	Requirement 要求	Actual 实际	Acc	Rej
Thickness 板厚	Micrometer 千分尺	0.578+/-0.1	0.581	Acc	
Size 尺寸	three-D 三次元	147.25*166.82+/-0.13	147.26*166.83	Acc	

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PROD P/N :		DATE CODE:	2014
CUSTOMER P/N :	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :	/	QUANTITY :	2 PCS

3.0 Marking 标记

Item 项目	Inspection Method 测试方法	Requirement 要求	Actual 实际	Acc	Rej
Multech logo 艾尔特标记	Visual 目检	☐ By Etch 蚀刻	☐ By Etch 蚀刻		
		☐ By S/M 阻焊	☐ By S/M 阻焊		
		☑ By C/M 字符	☑ By C/M 字符	Acc	
		☐ By Etch 蚀刻	☐ By Etch 蚀刻		
		☑ By Comp side 元件面	☑ By Comp side 元件面	Acc	
		☐ By Solder side 焊接面	☐ By Solder side 焊接面		
Additional Marking 附加标记	Visual 目检				
UL logo UL标记	Visual 目检	☑ 94V-0	☑ 94V-0	Acc	
		☐ By S/M 阻焊	☐ By S/M 阻焊		
		☑ By C/M 字符	☑ By C/M 字符	Acc	
		☐ By Etch 蚀刻	☐ By Etch 蚀刻		
		☑ By Comp side 元件面	☑ By Comp side 元件面	Acc	
		☐ By Solder side 焊接面	☐ By Solder side 焊接面		
Date code 日期标记	Visual 目检	☑ WWYY 周年	☑ WWYY 周年	Acc	
		☐ YYWW 年周	☐ YYWW 年周		
		☐ By S/M 阻焊	☐ By S/M 阻焊		
		☑ By C/M 字符	☑ By C/M 字符	Acc	
		☐ By Etch 蚀刻	☐ By Etch 蚀刻		
		☑ By Comp side 元件面	☑ By Comp side 元件面	Acc	
		☐ By Solder side 焊接面	☐ By Solder side 焊接面		
Customer P/N 客户型号	Visual 目检	☐ P/N 型号	☐ P/N 型号		
		☐ By S/M 阻焊	☐ By S/M 阻焊		
		☐ By C/M 字符	☐ By C/M 字符		
		☐ By Etch 蚀刻	☐ By Etch 蚀刻		
		☐ By Comp side 元件面	☐ By Comp side 元件面		
		☐ By Solder side 焊接面	☐ By Solder side 焊接面		

4.0 Line wide/space measurement（线宽线隙测试） unit/单位：mm

Item 项目	Inspection Method 测试方法	Requirement 要求		Actual 实际	Acc	Rej
Line wide 线宽	100倍放大镜 100times magnifier	Comp side 元件面：	0.228	0.225	Acc	
		Solder side 焊接面：	0.228	0.226	Acc	
Line space 线隙	100倍放大镜 100times magnifier	Comp side 元件面：	0.165	0.169	Acc	
		Solder side 焊接面：	0.165	0.167	Acc	
SMT&BGA side	100倍放大镜 100times magnifier					
Annularring 焊环	100倍放大镜 100times magnifier					

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Products final audit report

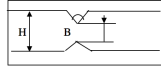
生产报告

PROD P/N :		DATE CODE:	2014
CUSTOMER P/N :	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :	/	QUANTITY :	2 PCS

5.0 Warpage Measurement（板曲度测量）

Inspection Method 测试方法	Requirement 要求	Actual 实际	Acc	Rej
IPC II	≤0.75%	0.15%	Acc	

6.0 V-CUT Measurement（V-CUT测量）

Inspection Method 测试方法	Requirement 要求：	Actual 实际	Acc	Rej
	H:/	/		
	B:/	/		
	/	/		

7.0 Gold finger Measurement（金手指角度测试）

Inspection Method 测试方法	Requirement 要求	Actual 实际	Acc	Rej
Measurement by angle magnifier 角度镜测试				

7.0 Visual inspection（外观检查）

Inspection Method 测试方法	Requirement 要求：	Actual 实际	Acc	Rej
IPC-A-600 /Customer request	NO visual defects 无外观不良	☑ No defects 无缺陷	Acc	
		☐ have defects 有缺陷		

8.0 Hole size method（孔径检查）

Inspection Method 测试方法		By pin Gauge（用针规） unit/单位：mm					
NO.	Requirement 要求	Actual 实际				PTH & NPTH	Result
		1	2	3	4		
1	3.00 ±0.076	3.00	3.01	3.02	3.00	PTH	ACC

Finial result : ☑ **Acc** ☐ **Rej**

Prepared by: ZHONGXING **Approved by:** WILLIAM

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艾尔特线路科技(HK)有限公司
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E-mail:marketing@multech-pcb.com,UL:E320829

SOLDERABILITY TEST REPORT

PROD P/N :		DATE CODE:	2014
CUSTOMER P/N :	RT5880 20mil	LOT NO. :	/
CUSTOMER :	A002	JOB CODE :	/
REF.NO :		QUANTITY :	1PCS

TEST METHOD : IN ACCORDANCE WITH MULTECH-A1-05
APPARATUS : SOLDER POT ,THERMOMETER .FLUX: HF-268
TEST CONDITION : BANKING TEMP: 0℃ , TIME: 0 HOURS
SOLDERING TEMP: 255℃ 3s*1T
TEST METHOD : ☐ Wave solder ☐ Dip solder ☑ Float solder

After tested specimen and defect:

1. Discolor : NO
2. Wrinkles : NO
3: Delamination: NO
4. Delamination : NO
5. Measling : NO
6. Blow-hole : NO
7. Solder mask peel off: NO
8. Solder filled into holes-wall not completely : NO

Remarks:

Dispositon : ACC ☑ TIME: HOURS REJ ☐

TEST BY : ZHONGXING Date: 2014-5-26

Approved by : WILLIAM Date: 2014-5-26

Appendix D

Production Query

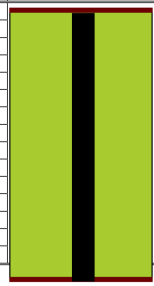
DESIGN

PCB ID	
RoHS Compliant Design	YES
Date	30.04.2014
FFI Layout Responsible	Morten Gunnerud

PB SPECIFICATION

No. of Layers	2		
Thickness	Nom.: 0,578mm	Min.: 0,338mm	Max.: 0,6 mm
Base material	IPC-4101/21	Rogers RT5880 0,508	Minimum Tg : 170°C
	Minimum Td : 350°C	Z-axis CTE < 50 ppm/°C below Tg and < 250 ppm/°C above Tg	
Flammability (as laminated)	Specification = V-0	Test Method = UL94	
Metallic Finish	**ELECTROLESS NICKEL/IMMERSION GOLD** Ref. IPC-4552 Au 0.05 - 0.12 µm / Ni 3 - 7 µm		
Solder mask	IPC – SM-840 **Class T** Color: **Green**		
Component Notation	Screen-printed Color: White		
Minimum values on PB	Trace = 0,2 mm		
	Clearance = 0,1 mm		
	Via	**Nom. hole diameter**	**Min. pad diameter**
	Layer **1-2** thruhole	0,3 mm	0,60 mm

STACKUP SPECIFICATION

Layer #	Symbol	Material	Thickness after processing		Usage
1		Cu foil or single sided Cu clad laminate	(35um)	Cu: 0,35 µm	Sig
		RO5880 0,508	0,508 mm		
2		Cu foil or single sided Cu clad laminate	(35um)	Cu: 35 µm	Sig

NOTES

1.	The PCB must be RoHS process compatible and suitable for lead free assembly
2.	The PCB manufacturer must not make any changes to the design or make any deviations from this PCB specification without written permission from FFI.
3.	Nominal thickness includes plating on outer layers, but not solder mask

4.	Nonfunctional pads on inner layer(s) may be removed
5.	Teardrops may be added to the pads as long as insulation is maintained
6.	Pattern registration: Displacement is required to be less than 0,1 mm in any direction for board size up to 200 x 200 mm
7.	Each individual board shall be marked with the date code and manufacturer's identification.
8.	Each individual board shall be clearly marked as RoHS compliant.

GENERAL SPECIFICATIONS

IPC code	Description
IPC-6011	Generic Performance Specification of Printed Boards
IPC-6012C-2010	Qualification and Performance Specification for Rigid Printed Boards. **Performance class:2**. **See Note A below**.
IPC-A-600H	Acceptability of Printed Boards. **Performance class: 2**. **See Note A below**.
IPC-SM-840E	Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards
IPC-4101C	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-4121	Guidelines for Selecting Core Constructions for Multilayer Printed Wiring Board Applications

Note A - Bow and Twist:
Max bow and/or twist on this board shall be 0.50%, measured using any of the procedures described in IPC-TM-650, Method 2.4.22.
The bow and twist of finished board must fulfil the above requirement after a heat treatment.

Appendix E

Phase Error Calculations

E.1 Single Feeding Point

These calculations are made as an example concequences of the difference in phase due to unideal feeding of a CGHV1J070D transistor, which has a large periphery. The calculations are based on a FR4 substrate[5] and at a frequency of 8.5 GHz.

The wave velocity in FR4 is given by (2.18) and is $146.385 \times 10^6 m/s$, and the wavelength is given by (2.19) to be $17.22\ mm$, a quarter wave is then $4.3\ mm$.

As a worst case, the feeding point will be centered close to the transistor. In that case, the phase difference is proportional to the distance between the input ports on the transistors. The distances from center is equal to:

```
d1=0.18; %closest transistor pair
d2=0.54;
d3=0.9;
d4=1.26;
d5=1.62;
d6=1.98; %most distant transistor pair
```

Note that for symmetry reasons the two transistors at equal length from center is modeled as one. The difference in phase is given by 2 times the distance(input and output) divided by the wavelength, or

```
phi1=pi*d1/W;
phi2=pi*d2/W;
phi3=pi*d3/W;
phi4=pi*d4/W;
phi5=pi*d5/W;
phi6=pi*d6/W;
```

Where W is the quarter wavelength.

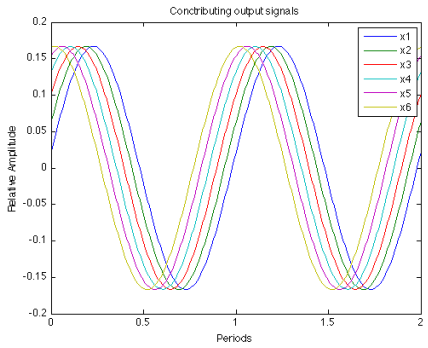
The answers recalcultad from radians to degrees are

```
phi1=7.5349
phi2=22.6047
phi3=37.6744
phi4=52.7442
phi5=67.8140
phi6=82.8837
```

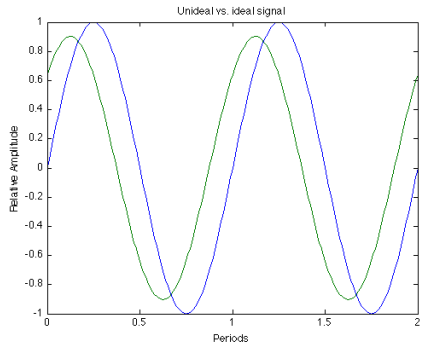
The resulting contributions to the output signal is

```
x1=(1/6)*sin(2*pi*t+phi1);
x2=(1/6)*sin(2*pi*t+phi2);
x3=(1/6)*sin(2*pi*t+phi3);
x4=(1/6)*sin(2*pi*t+phi4);
x5=(1/6)*sin(2*pi*t+phi5);
x6=(1/6)*sin(2*pi*t+phi6);
```

The contributions to the output signal is shown in figure E.1a, and the sum of the contributions is plotted together with the ideal output in figureE.1b.



(a) contributing signals in relative amplitude plotted over two periods



(b) unideal and ideal signal plotted over two periods

Figure E.1: Difference between unideal and ideal feeding

The resulting loss in dB is given by

```
y=sin(2*pi*t);
x=x1+x2+x3+x4+x5+x6;

loss=10*log10(mean(x.^2)/mean(y.^2));
```

and equals $0.8739\ dB$.

E.2 Two Feeding Points

The reasoning will be very much like in Appendix E.1, but instead of 6 different phase contributions, there will be 3, because of the creation of two new symmetry points. The distances from the two feeding points to the transistors are now

```
d1=0.18; %closest transistor pair
d2=0.54;
d3=0.9; %most distant transistor pair
```

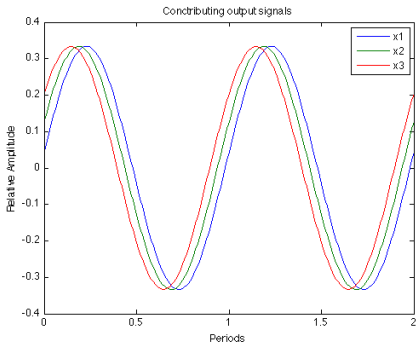
and the corresponting phase differences in degrees are

```
phi1=7.5349
phi2=22.6047
phi3=37.6744
```

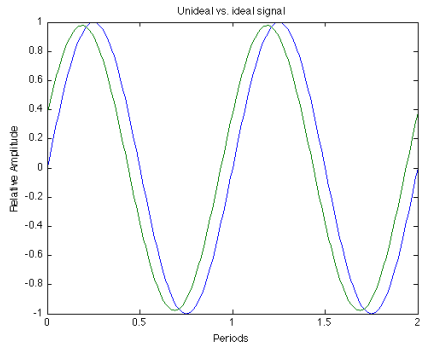
This gives:

```
x1=(1/3)*sin(2*pi*t+phi1);
x2=(1/3)*sin(2*pi*t+phi2);
x3=(1/3)*sin(2*pi*t+phi3);
```

The contributions to the output signal is shown in figure E.2a, and the sum of the contributions is plotted together with the ideal output in figureE.2b.



(a) contributing signals in relative amplitude plotted over two periods



(b) unideal and ideal signal plotted over two periods

Figure E.2: Difference between unideal and ideal feeding

The resulting loss in dB is given by

```
y=sin(2*pi*t);
x=x1+x2+x3;

loss=10*log10(mean(x.^2)/mean(y.^2));
```

and equals $0.1950\ dB$.

E.3 Moving the feeding point back from the transistor

By putting the feeding point at a distance from the transistor, the distance from the feeding point to the transistor will become.

```
c1=sqrt(a^2+d1^2);
c2=sqrt(a^2+d2^2);
c3=sqrt(a^2+d3^2);
c4=sqrt(a^2+d4^2);
c5=sqrt(a^2+d5^2);
c6=sqrt(a^2+d6^2);
```

and the corresponting phase differences in degrees are

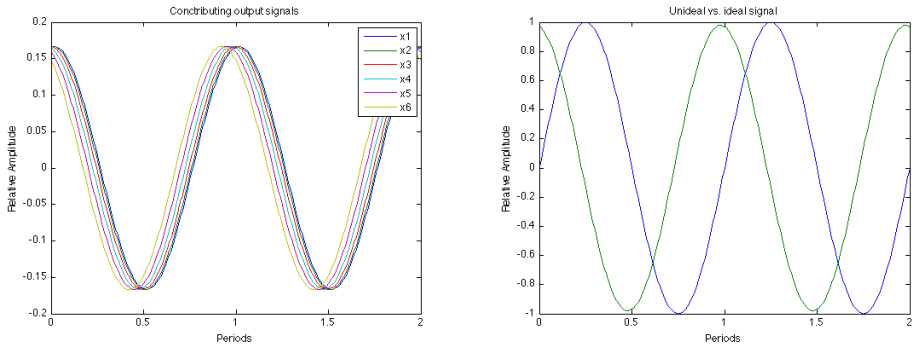
```
phi1=84.0593
phi2=86.7189
```

```
phi3=91.8072
phi4=98.9502
phi5=107.7401
phi6=117.8088
```

This gives:

```
x1=(1/6)*sin(2*pi*t+phi1);
x2=(1/6)*sin(2*pi*t+phi2);
x3=(1/6)*sin(2*pi*t+phi3);
x4=(1/6)*sin(2*pi*t+phi4);
x5=(1/6)*sin(2*pi*t+phi5);
x6=(1/6)*sin(2*pi*t+phi6);
```

The contributions to the output signal is shown in figure E.3a, and the sum of the contributions is plotted together with the ideal output in figureE.3b.



(a) contributing signals in relative amplitude plotted over two periods

(b) unideal and ideal signal plotted over two periods

Figure E.3: Difference between unideal and ideal feeding

The resulting loss in dB is given by

```
y=sin(2*pi*t);
x=x1+x2+x3;

loss=10*log10(mean(x.^2)/mean(y.^2));
```

and equals $0.1453\ dB$.

Appendix F

Wave Propagation on a Transmission Line

This derivation is the same that can be followed in [22, pp. 439-463]. If the telegraphers equation is solved to give a single wave equation fot either $V(z)$ or $I(z)$, we get

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{F.1}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0. \tag{F.2}$$

$V(z)$ is the Voltage at point z in a transmission line, $I(z)$ is the current at the same point.

The traveling wave solutions of the one-dimentional Helmholtz equation for a transmission line are

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{F.3}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}. \tag{F.4}$$

$e^{-\gamma z}$ represents the wave propagation in +z direction, and $e^{\gamma z}$ represents the wave propagation in -z direction, and

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{F.5}$$

is the complex propagation constant. R and L is the series resistance$[\Omega/m]$ and inductance$[H/m]$ per unit length, while G$[S/m]$ and C$[F/m]$ is the shunt conductance and capacitance per unit length for the transmission line. ω is the angular frequency in Hz. The current on the line is given by (F.2) and (F.3) to be

$$I(z) = \frac{\gamma}{R + j\omega L}\left[V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}\right] \tag{F.6}$$

this compared with (F.4) gives the characteristic impedance Z_0 of the transmission line

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-}. \tag{F.7}$$

Then (F.4) can be rewritten as

$$I(z) = \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{\gamma z} \tag{F.8}$$

If a transmission line is terminated with a load impedance Z_L at the point $z = 0$, the ratio of voltage and current at the load must equal to Z_L, which gives the following expression

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} Z_0 \tag{F.9}$$

solving for V_0^- gives

$$V_0^- = \frac{Z_L - Z_0}{Z_L + Z_0} V_0^+ \tag{F.10}$$

The amplitude of the reflected voltage wave divided by the incident voltage wave is defined as the voltage reflection coefficient, Γ:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{F.11}$$

If the load matched to the line, $\Gamma = 0$ and the magnitude of the voltage on the line is $|V_0^+|$. But if the load is mismatched, the presence of a reflected wave leads to standing waves with varying magnitude. The maximum and minimum value of the voltage is given by

$$V_{max} = |V_0^+|(1 + |\Gamma|) \tag{F.12}$$

$$V_{min} = |V_0^+|(1 - |\Gamma|) \tag{F.13}$$

From these two expressions the term Voltage Standing Wave Ratio(VSWR) is defined as

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{F.14}$$

Appendix G

Active Two-Port Networks

The same derivation as the one that follows can be found in [38, pp. 194-197].

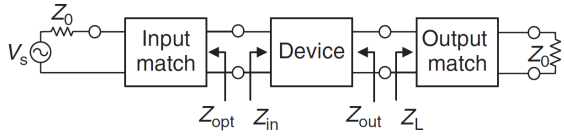


Figure G.1: An active two port network.[19, p. 34]

From (F.11), the reflection coefficient seen towards the load is

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{G.1}$$

likewise, the reflection coefficient seen towards the source is

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}. \tag{G.2}$$

Solving the S-parameter matrix for a two port(2.8) gives

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ = S_{11}V_1^+ + S_{12}\Gamma_L V_2^- \tag{G.3}$$
$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ = S_{21}V_1^+ + S_{22}\Gamma_L V_2^-. \tag{G.4}$$

This gives

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{G.5}$$

and

$$\Gamma_{out} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}. \tag{G.6}$$

By voltage division

$$V_1 = V_S\frac{Z_{in}}{Z_S + Z_{in}} = V_1^+ + V_1^- = V_1^+(1 + \Gamma_{in}) \tag{G.7}$$

and solving this for (G.5) gives

$$Z_{in} = Z_0\frac{1 + \Gamma_{in}}{1 - \Gamma_{in}}. \tag{G.8}$$

By combining the two previous and solving for V_0^+ we get

$$V_1^+ = \frac{V_S}{2}\frac{(1 - \Gamma_S}{1 - \Gamma_S\Gamma_{in}}. \tag{G.9}$$

Then, finally, if peak values are assumed for the voltages, the average power delivered to the network is

$$P_{in} = \frac{1}{2Z_0}|V_1^+|^2(1 - |\Gamma_{in}|^2) = \frac{|V_S|^2}{8Z_0}\frac{|1 - \Gamma_S|^2}{|1 - \Gamma_S\Gamma_{in}|^2}(1 - |\Gamma_{in}|^2). \tag{G.10}$$

The power delivered to the load is

$$P_L = \frac{|V_2^-|^2}{2Z_0}(1 - |\Gamma_L|^2). \tag{G.11}$$

By solving this for V_2^- we get

$$P_L = \frac{|V_S|^2}{8Z_0}\frac{|S_{21}|^2(1 - |\Gamma_L|^2)|1 - \Gamma_S|^2}{|1 - S_{22}\Gamma_{in}|^2|1 - \Gamma_S\Gamma_{in}|^2}. \tag{G.12}$$

Then we can define the power gain as

$$G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2(1 - |\Gamma_L|^2)}{\left(1 - |\Gamma_{in}|^2\right)|1 - S_{22}\Gamma_L|^2} \tag{G.13}$$

The power available from the source is the power delivered to the network when the input impedance of the terminated network is conjugately matched to the source impedance, or

$$P_{avs} = P_{in}|_{\Gamma_{in}=\Gamma_S^*} = \frac{|V_S|^2}{8Z_0}\frac{|1 - \Gamma_S|^2}{(1 - |\Gamma_S|^2)}. \tag{G.14}$$

Likewise, for the load

$$P_{avn} = P_L|_{\Gamma_L=\Gamma_{out}^*} = \frac{|V_S|^2}{8Z_0}\frac{|S_{21}|^2|1 - \Gamma_S|^2}{|1 - S_{22}\Gamma_{out}^*}. \tag{G.15}$$

And we can define the available power gain as

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2(1 - |\Gamma_s|^2)}{|1 - S_{11}\Gamma_s|^2\left(1 - |\Gamma_{out}|^2\right)}. \tag{G.16}$$

and the transducer power gain as

$$G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2(1 - |\Gamma_s|^2)(1 - |\Gamma_L|^2)}{|1 - \Gamma_s\Gamma_{in}|^2|1 - S_{22}\Gamma_L|^2} \tag{G.17}$$