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Wideband Efficiency in a Class-F Power Amplifier

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Electronics System Design and Innovation
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Problem Description

Assignment title: Wideband Efficiency in a Class-F Power Amplifier

In many radio systems the efficiency of the power amplifier is extremely important. When a power amplifier is driven near its maximum output power, it will generate higher order harmonic frequency components. A way to increase the efficiency in the amplifier is to tune these components to a desired outcome. In class-F and class-F^{-1}, also called harmonic tuned power amplifiers, the impedance of these components are tuned at the output of the amplifier. This will adjust the shape of the current and voltage, making the amplifier as efficient as possible.

The tasks of this assignment are:

- Study the principles of class-F and class-F^{-1} power amplifiers.
- Learn to use electronic design automation software (Agilent ADS).
- Design and characterize a power amplifier with high efficiency over a relatively large bandwidth.
- Tune the harmonic impedances using load pull, to get as high efficiency as possible in the bandwidth.
- Manufacture one or more prototypes.
- Measure and characterize the amplifiers.

Specifications:

Center frequency (f_0)	2.4 GHz
Bandwidth (3 dB)	1.2 GHz
Output Power (P_{out})	$>$ 40 dBm within the bandwidth
Gain	$>$ 12 dB within the bandwidth
Input Match (S_{11})	$<$ -10 dB within the bandwidth
Efficiency	as high as possible

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Summary

In this thesis, the design of a class-F/F^{-1} amplifier with high efficiency in a 1.2 GHz bandwidth and center frequency at 2.4 GHz is presented. The harmonic tuning is done by using a CAD load pull test bench in Agilent ADS. The optimal impedances at f_0, and at the harmonics $2f_0$ and $3f_0$, which gives the best performance is found by using the test bench. These impedances are realized in matching networks with passive components, microstrip lines and open circuit stubs. Two identical amplifiers were manufactured and characterized with small signal, large signal and two tone measurements. The design is based around a Cree 10 W GaN HEMT transistor and printed on a FR-4 substrate.

Simulations using the lossless load pull test bench resulted in a drain efficiency higher than 80% and PAE higher than 75% through the bandwidth while the output power was larger than 10 W with a maximum of 11.9 W. This is the optimal performance of the amplifier and set the impedances to obtain in the matching networks.

The final design with realized matching networks resulted in a decrease in efficiency of 5-15% and an increase in output power by about 0.5 dBm while operating at the 1 dB compression point. The decreased efficiency is due to imperfect matching and loss in components and microstrip lines. In the simulations, the amplifier achieved a 3 dB bandwidth of 1.8 GHz in the small signal gain.

The measurements concluded that the most optimal bandwidth of operation is from 1.6 - 2.8 GHz, a 200 MHz shift from the bandwidth given in the assignment. The measurements results show a drain efficiency from 55-66% in the bandwidth and a PAE higher than 50%, delivering an output power of 14.2 W operating at 1 dB compression. The measured 3 dB bandwidth of the amplifier was 2.57 GHz.

The measured results are good as power amplifiers covering large frequency bands rarely has good efficiency throughout the whole bandwidth. Possible applications include cognitive radio transceivers, radios which use frequency hopping or as a buffer amplifier for lab purposes.

Sammendrag

I denne oppgaven presenteres en metode for design av en klasse-F/F^{-1} effektforsterker med senterfrekvens på 2.4 GHz og høy virkningsgrad i en båndbredde på 1.2 GHz. Dette gjøres ved å utføre harmonisk tilpasning ved hjelp av en "load pull" testbenk i simuleringsprogrammet Agilent ADS for radiosystemer. De optimale impedansene ved f_0 og de harmoniske komponentene ved $2f_0$ og $3f_0$ som vil gi de beste resultatene kartlegges ved bruk av testbenken. Disse impedansene blir deretter realisert i tilpasningsnettverk ved bruk av passive komponenter og transmisjonslinjer. To like forsterkere ble produsert og deretter karakterisert ved bruk av småsignal-, storsignal- og totonemålinger. Forsterkeren er designet rundt en Cree 10W GaN HEMT transistor og frest ut på et FR-4 substrat.

Simuleringene utført med de tapsfrie "load pull" testbenkene gir en "drain efficiency" høyere enn 80% og PAE høyere en 75%, samt utgangseffekt høyere enn 10 W i hele båndbredden med en maks uteffekt på 11.9 W. Dette er den optimale ytelsen til forsterkeren med tanke på virkningsgrad.
Det endelige designet med realiserte tilpasningsnettverk resulterte i en 5-15% nedgang i virkningsgrad og en økt utgangseffekt med gjennomsnittlig 0.5 dBm mens forsterkeren opererer ved 1 dB kompresjon. Den lavere virkningsgraden kan skyldes feil i tilpasningen av nettverkene med de optimale impedansene, samt tap i passive komponenter og transmisjonslinjer. Den simulerte 3 dB båndbredden i småsignal gain var 1.8 GHz.

Resultatet av målingene konkluderte med at den mest optimale båndbredden er fra 1.6 - 2.8 GHz, dette er en 200 MHz forflytning i båndet. Målingene resulterte i en "drain efficiency" mellom 55-66% og en PAE høyere enn 50% samtidig som den maksimale utgangseffekten var på 14.2 W ved 1 dB kompresjon. Forsterkeren oppnådde en målt 3 dB båndbredde på 2.57 GHz.

Forsterkeren oppnådde god virkningsgrad som ikke er vanlig i konvensjonelle effektforsterkere med like stor båndbredde. Mulige bruksområder for forsterkeren er kognitive radioenheter, radioer som benytter frekvenshopping og bruk til laboratorieformål som en driverforsterker.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of master of science (MSc) at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU). The work was carried out in the period January to June 2014.

Acknowledgment

I would like to thank my supervisor, Associate Professor Morten Olavsbråten, for his valuable input and help with this thesis. His commitment and passion for the topic of RF power amplifiers combined with enthusiasm has been a source of motivation during my work on this thesis. I would also like to thank PhD cand. Dragan Mitrevski for help with my measurements as well as head engineer Terje Mathisen for his help with the production of the PCB. Finally, a special thanks to my friends and fellow students for valuable input and insight during this period.

Trondheim, Norway, June 2014.
Andreas Berg Stenstrøm

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Abbreviations

AM	=	amplitude modulation
ADS	=	Advanced Design Systems
DUT	=	device under test
GaAs	=	Gallium Arsenide
GaN	=	Gallium Nitride
GPIB	=	general purpose interface bus
HB	=	harmonic balance
HEMT	=	high electron mobility transistor
IMD	=	intermodulation distortion
MAG	=	maximum available gain
PA	=	power amplifier
PAE	=	power added efficiency
PCB	=	printed circuit board
PM	=	phase modulation
PNA	=	programmable network analyzer
RF	=	radio frequency
RFPA	=	radio frequency power amplifier
Si	=	Silicon
SMA	=	SubMiniature version A
SMD	=	surface mounted device
SOLT	=	short-open-load-thru
TRL	=	thru-reflect-line
VNA	=	vector network analyzer

Chapter 1

Introduction

The power amplifier (PA) is a critical component in a wireless communication system. It accounts for a significant portion of the costs in both development and production of radio equipment, making improved power amplifier architectures and design topologies desired in the industry. With later years rapid increase in the number of wireless communication systems, the already high linearity requirements the power amplifier must satisfy have become even tougher. In addition to linearity, requirements regarding power efficiency are also present for some applications. In portable devices it is the power amplifier that drains the battery the most, while in base station equipment the power amplifiers often require large and expensive cooling systems, increasing the running and total costs for the operator.

With the introduction of Gallium Nitride (GaN) high electron mobility transistors (HEMT) in the last decade, the problem of high efficiency operation seem to have a brighter future. The GaN HEMT technology provides some advantageous properties, such as increased power density, higher operating voltages, and improved thermal properties [6]. These properties combined allows for less complex designs, higher power efficiencies, and a reduced requirement for large cooling systems. A way to implement a design for high efficiency operation is to carry out load pull measurements to find the optimal operating conditions of the device.

To achieve high efficiency operation in power amplifiers, the transistor needs to be driven into nonlinear operation, which in turn will generate higher order harmonic frequency components in the output signal. The class-F amplifier is a reduced angle amplifier with load harmonic modulation control to shape the drain voltage in a way that it in theory does not overlap with drain current, thus greatly reducing the power dissipated in the amplifier which increases the efficiency. The theory on class-F operation is well explained by Cripps [1] and Raab [7].
Design of a class-F amplifier involves matching network design at the fundamental frequency, and load harmonic tuning network design up to certain order harmonics. The common practice is to present a short circuit at the even order harmonics, and an open

circuit at the odd order harmonic. In most cases only the second and third order harmonics are considered, since higher order harmonic control would lead to more complexity and possibly further loss [4].

In this thesis, the design of a class-F amplifier using a load pull test bench in microwave/RF CAD software will be performed. The load pull test bench will be used to find the optimal impedances, both for the source and load matching networks, to be realized using passive components and microstrip lines. This requires studying the principles of power amplifier classes F and F^{-1}, and design procedures of power amplifiers in CAD software Agilent ADS. The given specifications for the amplifiers are listed in table 1.1.

Table 1.1: Specifications given in the assignment text for the thesis.

Center frequency (f_0)	2.4 GHz
Bandwidth (3 dB)	1.2 GHz
Output Power (P_{out})	$>$ 40 dBm within the bandwidth
Gain	$>$ 12 dB within the bandwidth
Input Match (S_{11})	$<$ -10 dB within the bandwidth
Efficiency	as high as possible

Chapter 2

Theory

2.1 S Parameters

The scattering matrix is a mathematical method that quantifies how RF energy propagates through a multi-port network. The S-matrix allows us to accurately describe the properties of very complex networks by viewing them as a simple box. For an RF signal incident on one port, some fraction of the signal is reflected, and some is scattered and exits other ports and some maybe lost to heat or radiation. The S-matrix for an N-port contains N^2 coefficients called S-parameters, each one a complex value (magnitude and phase) representing a possible input-output path.

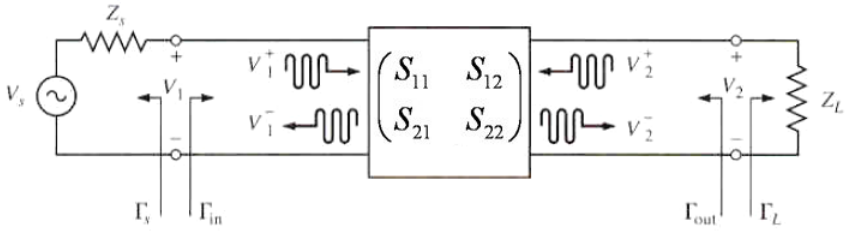


Figure 2.1: Generalized two-port network with source and load impedances. [4]

Figure 2.1 shows a generalized two-port network. S_{11} and S_{22} are the input/output reflection coefficients, while S_{12} and S_{21} are the forward/reverse voltage gain. If we assume that each port is terminated by an impedance $Z_S = Z_L = Z_0$, the network can be described as shown in equation 2.1 and 2.2. An expression for each of the parameters can be derived from these equations [4].

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \times \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix} \tag{2.1}$$

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+$$
$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \tag{2.2}$$

Figure 2.1 also displays the four reflection coefficients together with the two-port S-parameters. The reflection coefficient seen looking toward the load is

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{2.3}$$

while the reflection coefficient looking toward the source is

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}, \tag{2.4}$$

where Z_0 is the characteristic impedance reference for the s-parameters of the two-port network. Γ_{in} and Γ_{out} is the reflection seen from the matching networks looking toward the terminated network. With reference to figure 2.1 and equation 2.2 they are defined as

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}, \tag{2.5}$$

and

$$\Gamma_{out} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0}, \tag{2.6}$$

S parameters are a vital instrument in understanding and designing RF circuits. It is used to describe gain, stability and matching. In CAD software the parameters are used in simulating small signal applications.

2.1.1 Gain

Gain is defined as the amplifiers ability to increase the power or amplitude of a signal from the input to the output by adding energy to the signal from a power supply. For a power amplifier, there are three different definitions of gain, *Power Gain*, *Available Gain* and *Transducer Power Gain*.

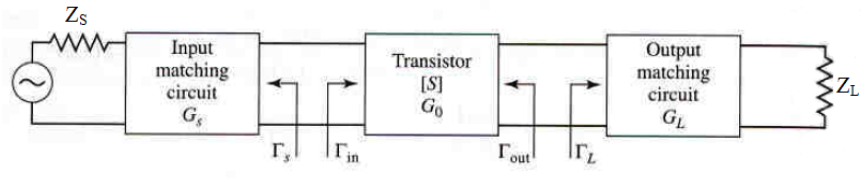


Figure 2.2: A general transistor amplifier circuit. [4]

Power Gain is defined as the ratio of power dissipated in the load Z_L to the power delivered to the input of the two-port network and is not dependent on Γ_S [4]. It is defined as

$$G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2}. \tag{2.7}$$

Available Gain is defined as the ratio of the power available from the two-port network to the power available from the source. This assumes that both the source and load are conjugately matched and does not depend on Γ_L [4]. It is defined as

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|\Gamma_{out}|^2)}. \tag{2.8}$$

Transducer Power Gain is defined as the ratio of the power delivered at the load to the power available from the source and is dependent on both source and load reflection coefficients [4]. Equation 2.9 shows the expression for the transducer power gain.

$$G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} \tag{2.9}$$

For a general transistor amplifier in figure 2.2 you can divide this expression into three parts.

$$G_S = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S\Gamma_{in}|^2} \tag{2.10a}$$

$$G_0 = |S_{21}|^2 \tag{2.10b}$$

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{2.10c}$$

The three equations above show how the transducer power gain accounts for both source and load mismatch, as well as the transistor gain.

2.1.2 Stability

Stability in an amplifier circuit is related to the risk of oscillations occurring at different frequencies. Oscillations can present in both large signal and small signal applications with varying effects, but are in both cases unwanted as it will cause problems in the amplifier. For a transistor amplifier circuit this can occur if either the input or output port impedance has a negative real part, i.e the reflection $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. Since Γ_{in} and Γ_{out} depends on the source and load matching networks, the stability also depends on Γ_S and Γ_L from the matching networks. There are two main categories of stability, conditional and unconditional [4].

- Conditional stability: When the circuit presents a mismatch, making the stability condition $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ only valid for a certain range of load and source impedances. This condition is also referred to as potentially unstable.
- Unconditional stability: The stability condition $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ is valid for all passive source and load impedances (i.e $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$) and the real part of the impedance is positive.

To determine if an amplifier circuit is stable, there are two tests used. One of these is the K-Δ test, where it can be shown that a device is unconditionally stable if "Rollet's Condition" is met. It is defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \ , \tag{2.11}$$

where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \tag{2.12}$$

If equations 2.11 and 2.12 are simultaneously satisfied, there is unconditional stability in the amplifier. It has to be regarded that since the source and load matching networks are generally frequency dependent, the stability has to be calculated for a wide frequency band to avoid oscillations. The K-Δ test has its shortcoming when it comes to comparing the relative stability of two or more devices because the magnitude of K does not indicate the margin of stability, just that it is stable. The other option is the μ test. The advantage of this test is that it only dependent one parameter, μ. It is defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.13}$$

Where $\mu > 1$ indicates unconditional stability. In addition, larger values of μ implies a greater margin of stability [4].

2.1.3 Matching

From equation 2.10 for a single stage amplifier we can se that if the source and load are matched to the characteristic impedance Z_0, the total gain of the amplifier would be the fixed gain of the transistor $G_0 = |S_{21}|^2$. So when designing an amplifier, the source and load matching, G_S and G_L, must be designed according to the application of the amplifier. For a power amplifier you want maximum gain in the source matching and maximum power transfer for the load matching.

With reference to figure 2.2, maximum gain and power transfer from the source matching network to the transistor will occur when the input impedance Γ_{in} seen by the transistor is conjugately matched with the impedance Γ_S from the source matching network.

$$\Gamma_{in} = \Gamma_S^* \tag{2.14}$$

For maximum power transfer at the output, Γ_L should be matched to provide as high P_{out} as possible.

$$\Gamma_{out} \Rightarrow max(P_{out}) \tag{2.15}$$

2.2 Power Amplifiers

Power amplifiers (PA) are generally divided in two categories, linear and non-linear. Linear power amplifiers generate output power proportional to the input power, with a small

amount of harmonics generated. Non-linear amplifiers operate near the cut-off region of the transistor which results in a large amount of harmonics generated together with the fundamental signal at the output. The result of the added harmonics is a non-linear relationship between the input power and output of the device.

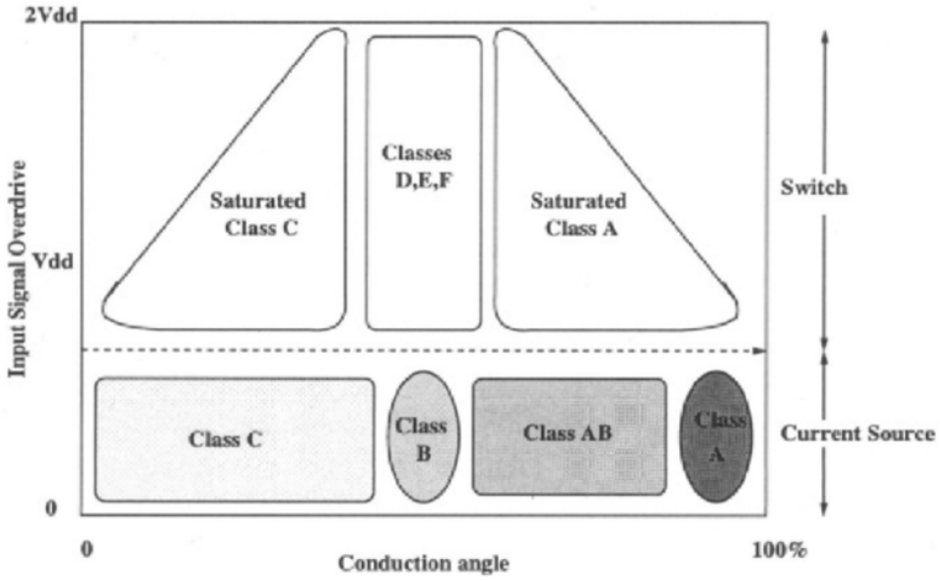


Figure 2.3: Comparison of different PA classes with respect to input signal overdrive and conduction angle. [8]

Linear and non-linear amplifiers can be further divided as biasing class and switching class. Linear class A, B, AB and C are classified based on their bias and conduction angle. The conduction angle is defined as the fraction of RF input drive signal where non-zero current is flowing through the device.

Switching amplifiers are implemented as high-efficiency PA's with true switching mode operation (class-D and E) at frequencies from VLF through lower VHF. The drain waveforms of these amplifiers are not sinusoidal, which means they will contain harmonics. Even class-B operation requires the presence of harmonics to produce the half-sinusoidal current waveforms. While the output network prevents the harmonics from reaching the load, it must allow their presence at its input. The harmonics in turn requires the correct drain/collector impedance, open or shorted, at the harmonic frequency. If the output network does not permit any harmonic voltages or currents, only class-A operation which has low efficiency is possible. Chapter 2.2.3 and 2.2.4 will further explain the different classes of power amplifiers.

2.2.1 Efficiency

The efficiency is one of the most important figure of merits describing the performance of a low-power amplifier and is often used in small signal amplifiers. Drain efficiency is defined as the ratio of the RF output power to the DC power dissipated in the amplifier.

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.16}$$

To increase efficiency, the amount of DC power consumed by the amplifier has to decrease while outputting the same amount of power. The power that is not converted to useful signal is dissipated as heat. Thus PA's that have low efficiency have high levels of heat dissipation, which is a limiting factor in many applications.
For large signal RF applications, the drain efficiency is no longer the most precise way to describe the efficiency. In this case equation 2.17 gives a more accurate description.

$$\eta_{\text{PAE}} = PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\frac{P_{out}}{P_{DC}} = \left(1 - \frac{1}{G}\right)\eta \tag{2.17}$$

Power Added Efficiency (PAE) takes into account the input RF power as it defines how efficiently the amplifier is able to convert DC power to RF power. The gain (G) in the equation above is the *power gain* of the amplifier.

2.2.2 Linearity

Linearity in a RF amplifier can be described as the ability to increase the power level of an input signal without otherwise altering the content of the signal. The term linearity derives form an amplifier's linear relationship of input power to output power which, in an ideal amplifier, is directly related to the gain. One of the trade-offs in power amplifiers is between output power and bandwidth. Active devices are inherently limited in bandwidth by internal parasitic capacitance. That means that every transistor reaches a frequency at which signal gain drops to a point where it no longer useful as an amplifier. Smaller transistor geometries can lead to higher operating frequency, but this will result in a reduced current and power capacity.

To achieve good efficiency in an amplifier, linearity is the trade-off. When the amplifier is driven into compression it becomes nonlinear, which creates intermodulation distortion (IMD), also called harmonics, in the output signal. The IMD products that fall within the bandwidth of the signal will create distortion and have to be attenuated in the output network of the amplifier. A two-tone test is a common way to test linearity in amplifiers. A signal with two carriers (eq.2.18) is applied to the amplifier and can be described using the power series in equation 2.19. Note that the following equations assumes a weakly nonlinear amplifier, whose output and input voltage can be related using a standard power series [1].

$$v_{in}(t) = V_0(cos\ \omega_1 t + cos\ \omega_2 t) \tag{2.18}$$

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \ .... \tag{2.19}$$

$$v_{out}(t) = a_0 + a_1 V_0(cos\ \omega_1 t + cos\ \omega_2 t) + a_2 V_0^2(cos\ \omega_1 t + cos\ \omega_2 t)^2 + a_3 V_0^3(cos\ \omega_1 t + cos\ \omega_2 t)^3 + \ ....$$ (2.20)

The resulting series in equation 2.20 shows the three first degrees of distortion. Each degree generates a number of distortion products, which have either the same or lower orders. The even order distortion terms will be well outside the band of the signal and are off less importance than the odd order products. Figure 2.4 illustrates that the products of most interest are the intermodulation products in the band because of their potentially disruptive effect on the signal. The third order products at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ with amplitudes of $a_2 \cdot V_0^2 = \frac{3}{4}$ also has a contribution of amplitude $a_5 \cdot V_0^5 = \frac{25}{8}$ from the fifth degree term. The other large product comes from the fifth degree terms at $3\omega_1 - 2\omega_2$ and $3\omega_2 - 2\omega_1$ with amplitude $a_5 \cdot V_0^5 = \frac{5}{8}$. These products become dominant when the amplifier is operating in the compression or saturation region [1].

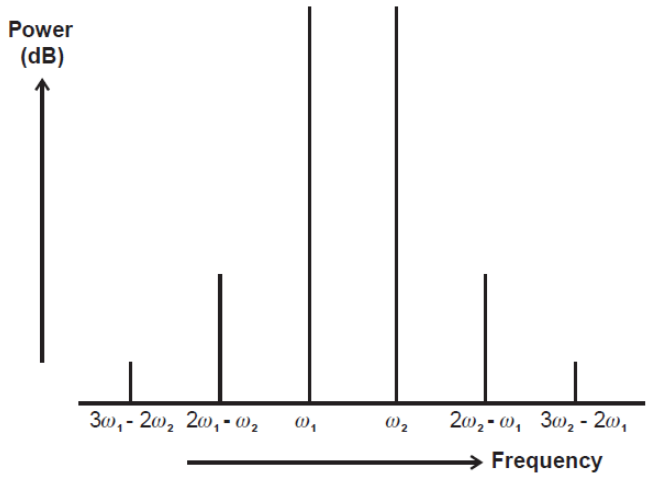


Figure 2.4: Two-tone intermodulation spectrum. [1]

The intermodulation product are dependent on frequency. The fifth order products is not affected by the third order nonlinearities, but the third order products are functions of both third- and fifth order (and higher) terms. This means that at low signal amplitudes, where the fifth order products can be neglected, the amplitude of the third order product is proportional to the third order term $a_2 \cdot V_0^2$ of the input amplitude. With larger amplitudes, the fifth order products will be a factor and increase the third order product. Since it is difficult to change the amount of nonlinearities, distortion is most effectively minimized by optimizing the impedances seen by the distortion current sources.

In all power amplifiers, the output level is a ”compressive” or ”saturating” function of the input level. The gain of the PA approaches zero for sufficiently high input levels. In RF circuits this effect is quantified by the 1 dB compression point, defined as the input

signal level that causes the small-signal gain to drop by 1 dB. Figure 2.5 shows the 1 dB compression point as well as the third order intercept point, which is a fictitious point where the linear gain meets the linear line of the third order harmonic.

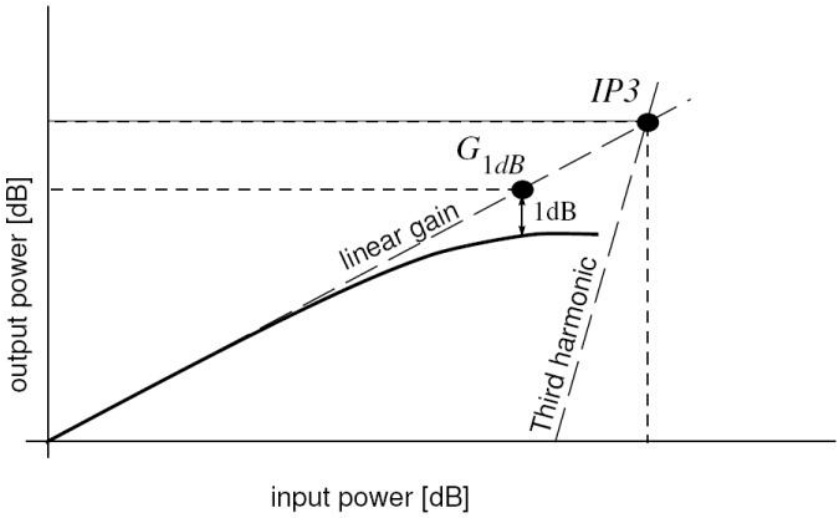


Figure 2.5: 1 dB compression point and third order intercept point (IP3) in log scale. [1]

2.2.3 Amplifiers Classes

The different biasing points of the classes of power amplifiers are displayed using I-V characteristics in figure 2.6.

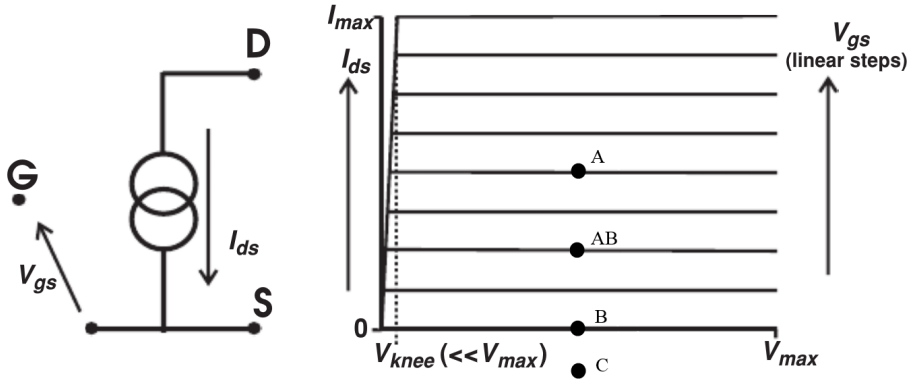


Figure 2.6: I-V characteristic showing the bias point of different PA classes. [14]

Class-A is a linear amplifier in the biasing class. The biasing point is in the middle of active region, ideally at $\frac{1}{2}V_{max}$ and $\frac{1}{2}I_{max}$. The conduction angle is 360° which means that the transistor is turned on and conducting during the entire sinusoidal cycle. The class-A amplifier is most commonly used in small signal operation because of its simplicity and linear qualities. The maximum theoretical drain efficiency is 50% and is the lowest of the power amplifier classes. The low efficiency makes it unsuitable for high power applications as the high amount of power dissipated in the amplifier would generate too much heat.

Class-AB is a compromise between class-A and B in terms of efficiency and linearity. It is biased in the region between class-A and B and the conduction angle is 180°- 360° with a theoretical drain efficiency is between 50% - 78.5%. Conventional class-AB operation creates odd harmonics in the process of improving efficiency. Theoretically to increases efficiency all the way up to 78.5%, the device shall generate only even order harmonics as it will not create undesirable close-to-carrier intermodulation distortion.

Class-B operation is also determined by the biasing point, which is close to the cut-off region of the transistor. The conduction angle is 180° which means that conducts a half cycle of the input signal. The theoretical drain efficiency is 78.5% and much better than class-A. However, since the transistor generates higher order harmonics near cut-off the linearity is not good. Linearity can be improved by either using two transistors in a push-pull configuration or by controlling the harmonics using resonators.

Class-C is biased below the cut-off region with a conduction angle less than 180°. The transistor is biased such that under steady-state conditions no drain current flows. In order to survive class-C operation, the transistor should have a drain voltage breakdown that is at least three times the active devices own DC voltage supply. For this reason true class-C operation is not often used in solid-state at higher RF and microwave frequencies.

2.2.4 Class-F Amplifier

Class-F and F^{-1} amplifiers use harmonic tuning on the amplified signal (fig.2.7) to control the harmonic content of the drain-voltage or current-drain waveforms. The drain voltage waveform includes odd harmonics and approximates a square wave, while the drain current waveform includes even harmonics and approximates a half sine wave (fig.2.8). The harmonics contribute to flatten the waveforms which allows he majority of the drain current to flow when the drain voltage is low, reducing the power dissipation. Ideally, this leads to a power efficiency of 100% as these waveforms do not overlap at all, but since only a finite number of harmonics can be used in the generation of the waveforms, there will be some overlap between the current and voltage waveforms, and the power efficiency will decrease. In practical realization of microwave/RF class-F, normally only the first three harmonics are considered, as tuning higher harmonics does not yield a significant improvement in efficiency compared to the complexity of implementing it.

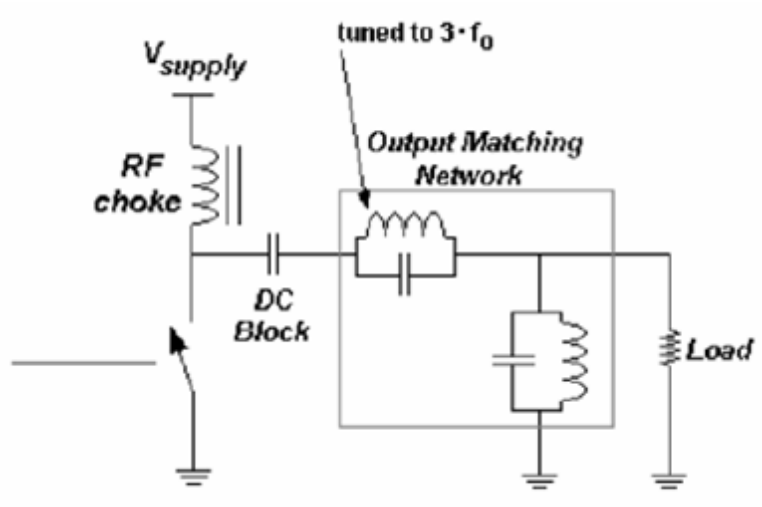


Figure 2.7: Resonators at the output to control the odd and even harmonics. [8]

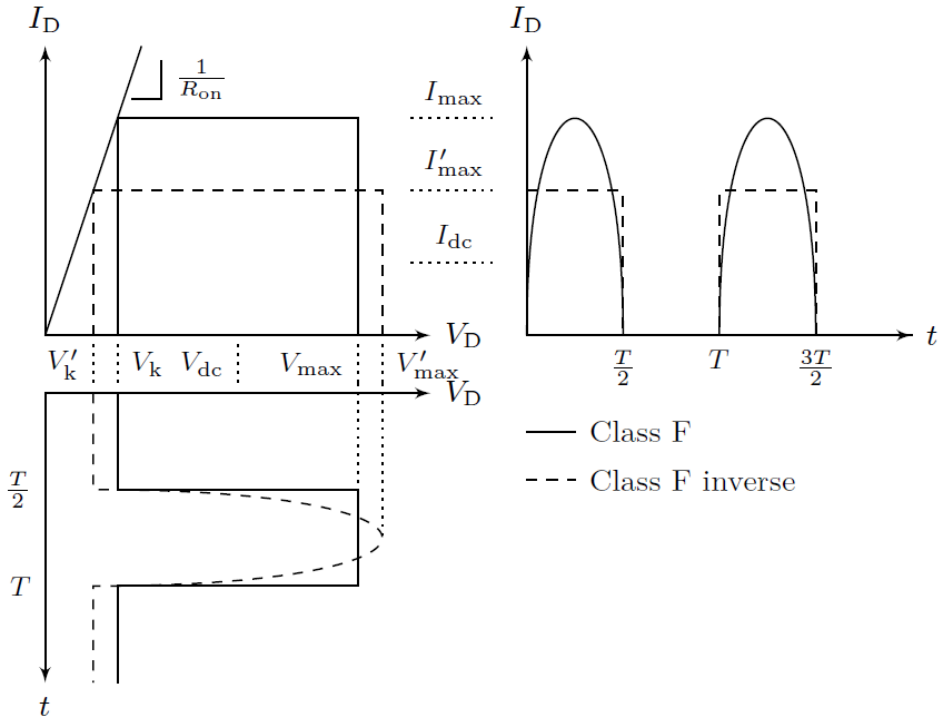


Figure 2.8: Ideal time domain current and voltage waveforms for class-F and class-F^{-1} under equal biasing conditions and for same output power. [3]

Inverse class-F (F^{-1}) is tuned to be short at odd harmonics and open at even harmonics which means that the drain current includes odd harmonics and approximates a square wave, and the drain voltage contains even harmonics and approximates a half sine-wave. It is important that the fundamental and second harmonic drain voltage is in-phase in order to properly shape the voltage waveform.

The efficiency of an ideal PA increased from 50% (Class-A) up to an ideal 100% depending on the amount of harmonics that can be controlled. In contrast to class-C, which also has a theoretical efficiency of 100%, the output power capability is also increased. Class-F is is one of the oldest techniques for improving efficiency of an RF PA, yet is still perhaps one of the least understood methods.

The ideal time domain current and voltage waveforms for class-F and F^{-1} are presented in figure 2.8. V_k denotes the knee voltage, V_{dc} the drain voltage bias and I_c the DC current and inverse class-F parameters are denoted with a prime (ex. I'_D). The waveforms can be analyzed using their Fourier series expansion and for a class-F amplifier waveforms, which include the effect of the on-state resistance are given by [16]

$$I_D(\theta) = I_{max}\left[\frac{1}{\pi} + \frac{1}{2}sin(\theta) - \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{cos(2n\theta)}{4n^2-1}\right] \quad [A], \tag{2.21}$$

$$V_D(\theta) = V_{dc} - \frac{4(V_{dc}-V_k)}{\pi}\sum_{n=1}^{\infty}\frac{sin((2n-1)\theta)}{2n-1} \quad [V], \tag{2.22}$$

where $\theta = \omega t$ and ω is the fundamental frequency of the desired output. For a class-F^{-1} power amplifier, the Fourier series expansion of the waveforms are given by

$$I'_D(\theta) = \frac{I'_{max}}{2}\left[1 + \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{sin((2n-1)\theta)}{2n-1}\right] \quad [A], \tag{2.23}$$

$$V'_D(\theta) = V'_k + (V'_{max} - V'_k)\left(\frac{1}{\pi} - \frac{1}{2}sin(\theta) + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{cos(2n\theta)}{4n^2-1}\right) \quad [V], \tag{2.24}$$

where

$$V'_{max} = \pi V_{dc} - (\pi - 1)V'_k. \tag{2.25}$$

Using these equations, expressions for the output properties of each class (power efficiency, fundamental output power, etc) can be derived. In [16], equations are derived for the power efficiency, output power, and the load resistance, all as a function of the on–state resistance. The results show how the class-F^{-1} mode amplifier outperforms the class-F mode amplifier with increasing on–state resistance.

2.2.5 Load and Source Pull

Load/source pull consists of varying or "pulling" the load or source impedance seen by a device while measuring the performance. They are used to measure a device in actual operating conditions. This method is important for large signal, nonlinear devices where the operating point may change with power level or tuning. Load pull is not usually needed for linear devices, where performance with any load can be predicted from small signal S parameters [1].

The load pull systems is used to find optimum loading conditions experimentally, while physically changing load reflection coefficient Γ_L for the extraction of design parameters, such as output power, the DC to RF power conversion efficiency, the operating power gain, gain compression and the power added efficiency for transistor devices. It can thus be concluded that the load pull system or technique allow the analysis of active device performance under varying loading conditions and leading to the design of matching circuits [1].

2.3 GaN Transistor Technology

Power amplifiers using Gallium Nitride (GaN) transistors are an active area of research. The performance of these transistors can be represented in terms of some important properties such as electron mobility, hole mobility, band gap and thermal conductivity. GaN has a wider band gap and a higher thermal conductivity than both Silicon (Si) and Gallium Arsenide (GaAs). These properties provides a relatively high power density, which has been shown to be one order of magnitude greater than its counterparts in Gallium Arsenide (GaAs) and Silicon (Si) [15]. Hence, for the same output power, a ten-time reduction of the size of the device can be realized using GaN HEMT technology.

A wider band gap allows the device to have a higher operating temperature and lower vulnerability to external noise such as shot noise because it requires more energy for the electrons to escape from the valence band to the conduction band. A wider band gap also provides a higher breakdown voltage and higher power density so that the transistor is able to output higher power in smaller physical size [6]. Over the last decade, GaN HEMTs have become more and more popular for microwave applications, and especially in base stations, where the properties of the GaN technology can be utilized to their full potential.

The 10W Cree GaN transistor used in this project operates at 28 V and up to 48 V. The higher efficiency that results from this high operating voltage reduces power requirements and simplifies cooling, an important advantage, since cost and weight of cooling systems is a significant fraction of the cost of a high power microwave transmitter.

2.4 Agilent ADS

All the simulations were performed in Agilent Technologies simulation software Advanced Systems Design (ADS). Agilent ADS supports every step of the design process,

from schematic capture, layout, frequency-domain and time-domain circuit simulation, and electromagnetic field simulation. This allows the user to fully characterize and optimize a complete RF design within the same design tool. For small signal simulations a predefined design guide which simulates the s parameters, noise figure, stability, and group delay of any two-port network versus frequency.

2.4.1 Large Signal Simulations

The large-signal simulations are performed in ADS using a method called ”Harmonic Balance”. Harmonic balance is a frequency-domain analysis technique for simulating nonlinear circuits and systems. It is well-suited for simulating analog RF and microwave circuits, since these are most naturally handled in the frequency domain. Harmonic balance simulation calculates the magnitude and phase of voltages or currents in a potentially nonlinear circuit which makes it possible to simulate circuits with multiple input frequencies. This includes intermodulation frequencies, harmonics, and frequency conversion between harmonics. Not only can the circuit itself produce harmonics, but each signal source can also produce harmonics or small signal sidebands. Designers are usually most interested in a systems steady-state behavior. Many high-frequency circuits contain long time constants that require conventional transient methods to integrate over many periods of the lowest-frequency sinusoid to reach steady state. Harmonic balance, on the other hand, captures the steady-state spectral response directly [9].

2.4.2 Optimization Algorithms

The optimization algorithms used in Agilent ADS uses the least squares error function to calculate the error. The least-squares error function is calculated by evaluating the error for each specified goal at each frequency or power point individually. The magnitudes of these errors are then squared, and the squared magnitudes are then averaged over frequency or power. The three types of algorithms used were ”Random”, ”Gradient” and Quasi-Newton”.

The Random optimizer arrives at new parameter values by using a random-number generator by picking a number at random within a range. Starting from an initial set of parameter values for which the error function is known, a new set of values is obtained by perturbing each of the initial values, and the error function is re-evaluated. Then the error function is re-evaluated by reversing the algebraic sign of each parameter value perturbation. These two values, corresponding to positive and negative perturbations, are compared to the value at the initial point. If either value is less than the initial value, then the set of parameter values for which the error function has its least value becomes the initial point for the next iteration. If neither value is less than the initial value, then the initial point remains the same for the next iteration. Since random search uses a pseudo-random generator, the results can be different for two optimization procedures [10].

The Gradient optimizer arrives at new parameter values using the gradient information of the networks error function. The gradient of the error function indicates the direction to move a set of parameter values in order to reduce the error function. For each iteration, the

error function and its gradient is evaluated at the initial point. Then the set of parameter values is moved in that direction until the error function is minimized. A single iteration usually includes many function evaluations and therefore, an iteration in the gradient search method takes much longer than the random search method [10].

The Quasi-Newton optimizer uses the second-order derivatives of the error function and the gradient to find a descending direction. The second-order derivatives are estimated by the Davidson-Fletcher-Powell (DFP) formula or its complement. Appropriately combined with the gradient, this information is used to find a direction and an inexact line-search is conducted. Much like the optimizers using the gradient search method, an iteration in the optimizers using the Quasi-Newton search method consists of many function evaluations. Therefore, a single iteration using the Quasi-Newton search method takes longer than an iteration in the optimizers using the Random search method [10].

2.4.3 Load-Pull Test Bench

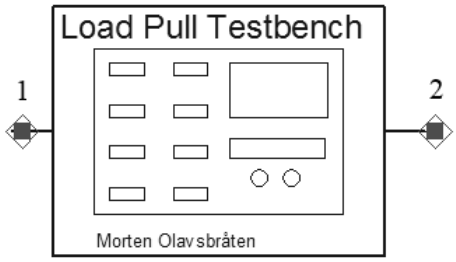


Figure 2.9: Load pull test bench block used in the simulations.

To tune the impedance at f_0 and the harmonics at $2f_0$ and $3f_0$, the load pull block in figure 2.9 was used in ADS. It is a load pull test bench made by Morten Olavsbråten, which allows the user to tune the impedances at f_0, $2f_0$ and $3f_0$ individually without affecting each other. In normal load-pull techniques, these impedances are dependent of each other which makes tuning more complex. The test bench will interpolate between the frequencies specified and the harmonics, either using linear or cosinus interpolation. The user specifies the fundamental frequency, bandwidth of the baseband, and the reflection coefficients magnitude and phase for baseband, f_0, $2f_0$ and $3f_0$. It is designed to find the impedance at port 1 and should be placed at the drain of the transistor so that this impedance translates to Γ_L in a two-port network. The next step is to manually tune the values of the reflection coefficients while looking at the simulation of PAE, output power and transducer gain. The fundamental frequency f_0 is tuned to achieve maximum output power, while $2f_0$ and $3f_0$ is tuned to achieve high efficiency (PAE).

2.5 Measurements

The following section briefly presents measurement methods and uncertainties related to them.

2.5.1 Network Analyzer

To measure the s-parameters of a device, a vector network analyzer (VNA) is used. This type of network analyzer consists of a sweep oscillator, a test set which includes two ports, a control panel, an information display and RF cables connected to the DUT. Each port of the test set includes dual directional couplers and a complex ratio measuring device.

Only perfect test equipment does not require some kind of correction. Imperfections exist in even the finest test equipment and cause less than ideal measurement results. Some of the factors that contribute to measurement errors are repeatable and predictable over time and temperature and can be removed, while others are random and cannot be removed. All measurement systems, including those employing network analyzers, can be affected by three types of measurement errors [11]:

- **Systematic errors:** Caused by imperfections in the test equipment and test setup. If these errors do not vary over time, they can be characterized through calibration and mathematically removed during the measurement process. Errors are typically caused by signal leakage, signal reflections, and frequency response.
- **Random errors:** Varies randomly as a function of time. Since they are not predictable, they cannot be removed by calibration. The main contributors to random errors are instrument noise and switch/connector repeatability.
- **Drift errors:** Occurs when a test systems performance changes after a calibration has been performed. They are primarily caused by temperature variation and can be removed by additional calibration and by having the test equipment in an environment with controlled temperature.

2.5.2 Calibration

There are two basic types of calibration used to correct for systematic errors. The two types are SOLT (*short*, *open*, *load*, *thru*) and TRL (*thru*, *reflect*, *line*). The differences in the calibrations are related to the types of calibration standards they use and how these standards are defined. They each have their advantages, depending on frequency range and application.

SOLT calibration is the most widely used choice for coaxial measurements. *Short*, *open* and *load* calibration consists of two one-port impedance calibrations, while *thru* provides forward and reverse transmission and reflection measurements. It is easy to perform and is used in a broad variety of environments. It provides broadband calibrations, essentially from DC to the upper frequency limit of the connector type being used.

TRL calibration was developed for making accurate measurements of non-coaxial devices at microwave and millimeter-wave frequencies. It is commonly used for in-fixture and on-wafer environments.

2.5.3 Measuring Power Amplifiers

With DUTs such as power amplifiers, the output power of the DUT may exceed the linear input range of the VNA. As an example, an amplifier has an output power of 20 W is measured on a VNA that has a limit of 0.2W at the test input port. Then a 20 dB attenuator between the amplifier output and test port 2 should be sufficient to prevent any overdrive, but using an attenuator creates a source of error. The reflection measurements will be affected as the signal passes the attenuator up to 3 times for a measurement. The attenuation in it self is removed in calibration, but every time the signal is attenuated it approaches the noise floor in the VNA which makes the measurement of S_{12} and S_{22} noise affected. By setting the analyzer to average the measurements by a high factor the results may be usable, but the process will become very time consuming [14].

2.5.4 Two-Carrier Characterization

The two-carrier, or two-tone test is a convenient method of generating an amplitude-modulated carrier with essentially no distortion. Any attempt to create AM using some form of modulator runs into the problem that the signal will have distortion due to the nonlinearity of the modulator. In modern communications applications, the two-carrier test has been largely replaced by tests using the actual modulation system in use. This kind of testing is essential, both during development and in production, for determining specification compliance on a product and characterizing the amplifier.
Asymmetries in the amplitudes of upper and lower intermodulation distortion (IMD) products of power amplifiers are found when performing a two-tone test. This means that the IMD at $2\omega_2$-ω_1 is different from the one at $2\omega_1$-ω_2. This type of asymmetry can create false results when measuring intermodulation ratios (IMR), third order intercept point (IP3) or other type of distortion figures of merit.

Chapter 3

Design

This chapter presents the design process and technology used in the amplifier. The technology used in simulations and on the PCB is presented with the key parts of the design following. The last section describes how the measurements were performed with a detailed overview of the setup.

3.1 Design Technology

In this section, the design technology used in the simulations and on the PCB is presented. This includes a short overview of the transistor, the capacitors and resistors, and the substrate used.

3.1.1 Transistor

The 10 W Cree CGH40010 transistor is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). It operates from a 28 volt rail, and offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMT offers high efficiency, high gain and wide bandwidth capabilities making the transistor ideal for both linear and nonlinear amplifier circuits.

3.1.2 Passive components

Johanson Technology surface mounted (SMD) capacitors are used in the amplifier. The Multi-Layer High-Q gives an ultra-high Q performance, and exhibit NP0 temperature characteristics. NP0 refers to the shape of the capacitors temperature coefficient graph which is how capacitance changes with temperature. NP0 means that the graph is flat and the device is not affected by temperature changes. The size of the capacitors used is 1608 mm and has a rated maximum voltage of 250 VDC.
Murata SMD capacitors is used as DC-blocks and in the bias networks. They are general purpose ceramic capacitors with high dielectric constant type in a smaller size with a

higher capacitance value. The size of the capacitors used is 1608 and 3216 mm and has a rated maximum voltage of 50 VDC.

The resistors used were basic 1608 mm SMD following the E12 series where each succeeding resistor falls within the +/- 10% of the previous value resulting in 12 values in logarithmic steps per decade.

3.1.3 Substrate

The substrate used for the amplifier is FR-4 which is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant. FR-4 glass epoxy is a popular and versatile high-pressure thermoset plastic laminate grade with good strength to weight ratios. With near zero water absorption, FR-4 is most commonly used as an electrical insulator possessing considerable mechanical strength. The material is known to retain its high mechanical values and electrical insulating qualities in both dry and humid conditions. These attributes, along with good fabrication characteristics, lend utility to this grade for a wide variety of electrical and mechanical applications. The parameters used in the ADS simulations are shown in table 3.1.

Table 3.1: FR4 Substrate Parameters.

H	Er	Mur	Cond	T	tan(δ)
$1.6 \times 10^{-3}\ m$	4.4	1.0	5.96×10^{7}	$36 \times 10^{-6}\ m$	0.02

3.2 DC-Bias operating point

The quiescent operating point of a class-F amplifier must be close to the cutoff region in order to generate significant amounts of harmonics. The class-F amplifier is usually biased around a class-B or AB amplifier, which naturally causes the drain waveforms to be similar. The difference is that because of the harmonic control in class-F, it has a larger voltage swing and the same clipping of the drain current.

From the documentation of Cree's ADS model for the CGH40010 transistor [12], the valid range of gate voltage V_{GS} is from -1.5 V to -3 V and the pinch-off voltage is at -2.9 V. The valid range of drain voltage V_{DD} is from 28 V to 48 V. To find the operating point, a IV-Curve design guide for FET transistors available in ADS was used. The gate voltage V_{GS} was set to sweep from -1.5 V to -3 V and the drain voltage V_{DD} from 0 V to 48 V. The result of the simulation is presented in figure 3.1.

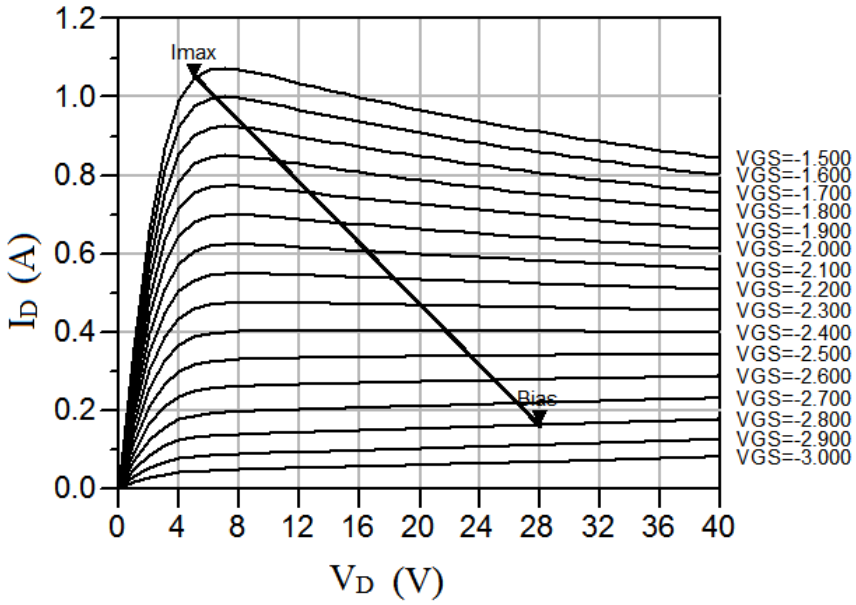


Figure 3.1: I-V characteristics of the Cree CGH40010 transistor with bias point and maximum current indicated.

The drain voltage was set to be 28 V and from the IV-characteristic a bias point at marker "Bias" was set. The result is an quiescent operating point at gate voltage $V_{GS} = -2.8\,V$ with resulting drain current $I_{DS} = 163\,mA$. As seen from figure 3.1 the chosen bias point will result in a voltage swing from 28 V to 5 V with a maximum current of $I_{DS_{max}} = 1.049\,A$.

3.3 Small Signal Design

S-parameter simulations are essential in characterizing the performance parameters of an amplifier, so the basic design of the circuit are characterized by using small signal simulations.

3.3.1 Bias Network

With a chosen operating point, a basic design can be set up to stabilize and match the input of the transistor for maximum gain. The first step is to design the drain and gate bias networks. In an amplifier it is very important that the bias networks are designed to avoid leakage of RF signal into the bias network or unwanted DC components into the output signal which can cause oscillations. The main concern for this is in the drain bias because of the large amount of DC voltage applied. When looking from the circuit into the bias network you wish to see infinite impedance at the fundamental frequency, limiting the chance of leakage drastically.

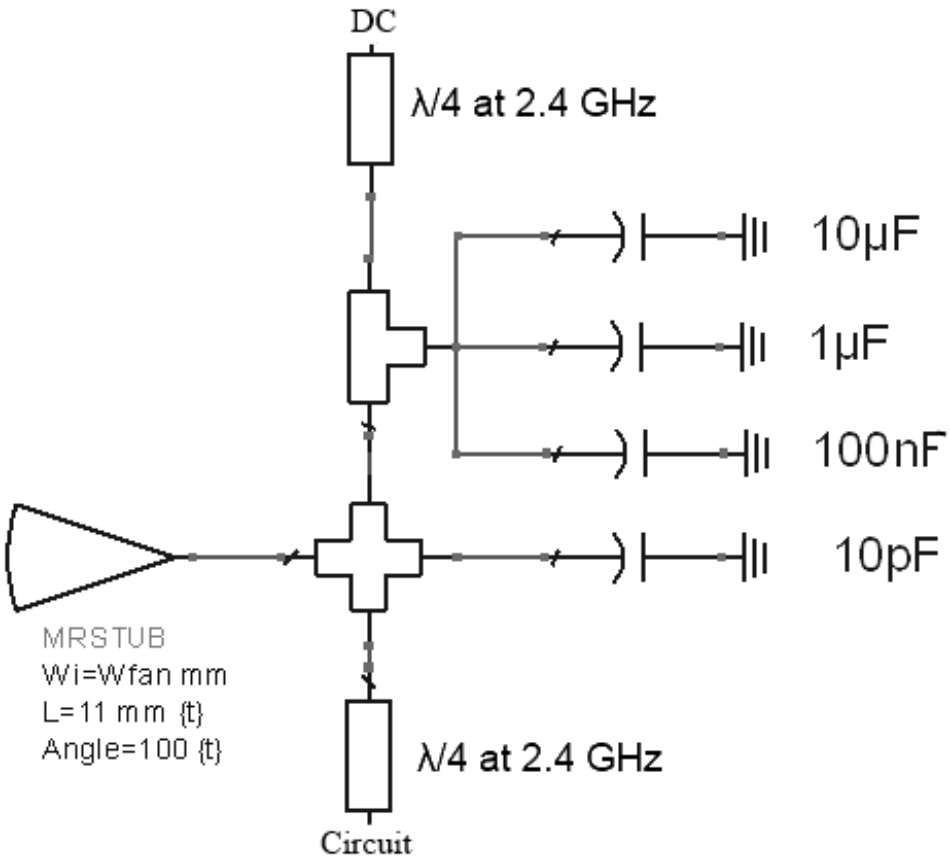


Figure 3.2: Bias network schematic.

Figure 3.2 shows the bias network at the drain of the amplifier. It is designed so that looking from the circuit you see infinite impedance, and at the base of the fan it sees a short circuit at the fundamental frequency.
The gate bias network is identical except for a resistor on the output to the circuit is added as recommended by Cree in the data sheet for the transistor [13] to help with stabilization. The capacitors at the base af the fan will help to suppress any RF signal from getting into the DC supply while providing high impedance at the drain/gate in order to maintain optimal in-band RF gain.

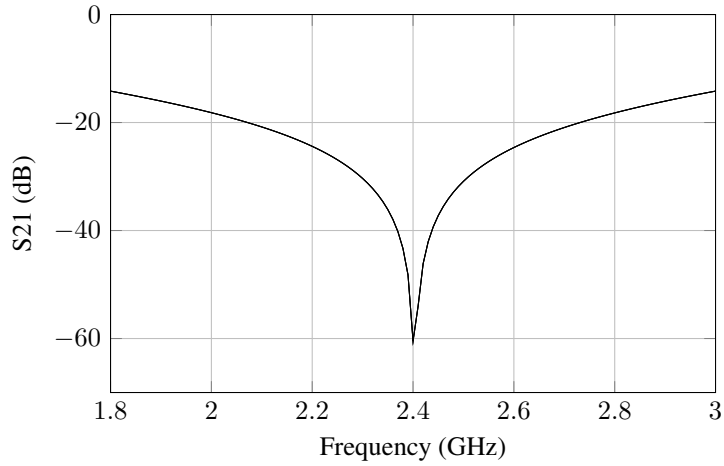


Figure 3.3: Attenuation of the RF signal to prevent leakage to the DC source.

Figure 3.3 shows the attenuation through the bias from circuit to DC source. It is designed so that the maximum attenuation is at the center frequency with as high as possible attenuation towards the edges of the frequency band. This will prevent the RF signal from leaking into the DC source.

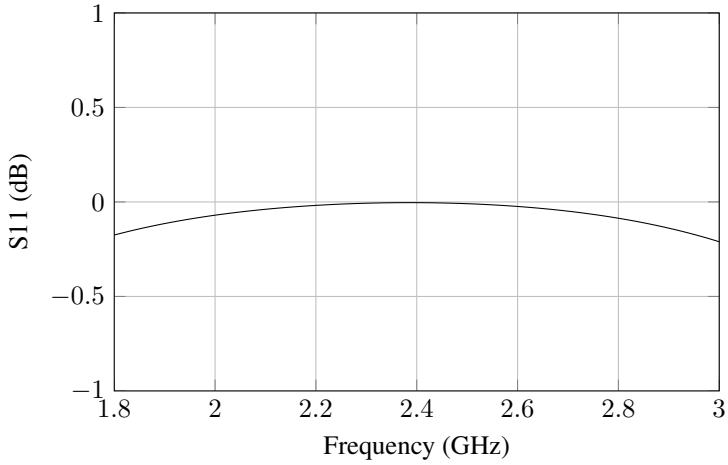
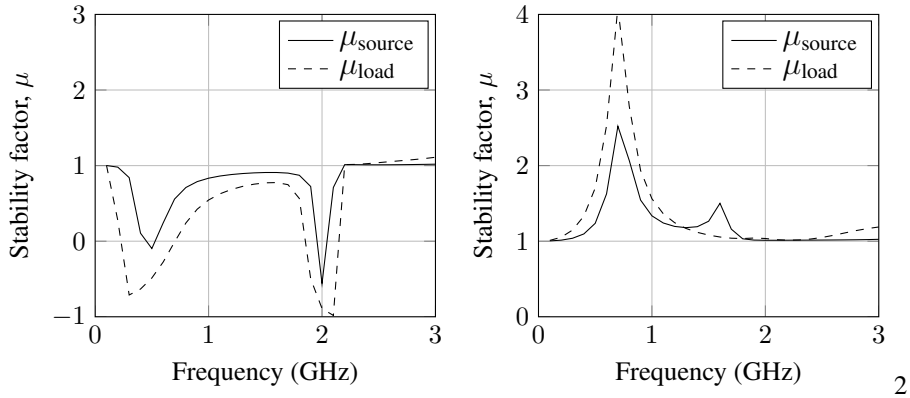


Figure 3.4: Simulated reflection

In figure 3.4, the reflection of the RF signal from the circuit is presented. The reflection should be as high as possible so the RF signal is prevented from leaking into the DC supply. Full reflection is when $\Gamma = 1$ (0 dB).

3.3.2 Stabilization

For stabilization at the gate of the transistor, a series-parallel RC network was inserted at the gate of the transistor along with a resistor at the base of the gate bias network (see appendix A). This is called a frequency selective method of stabilizing as this network will introduce loss at low frequencies ($f < \frac{1}{RC}$).



(a) Before stabilization.

(b) After stabilization.

Figure 3.5: Simulated stability factor μ before and after stabilization.

Figure 3.5b shows that the circuit meets the criteria of the μ-test described in chapter 2.1.2 which states that $\mu > 1$ indicates unconditional stability. The stability factor is very close to the limit from 2 - 3 GHz in μ_{load} and does not indicate a good margin of stability. When inserting the matching networks, the margin is expected to improve.

3.3.3 Matching Networks

The first approach to designing the source matching network was a combination of microstrip lines and stubs to keep the network gain flat over the bandwidth and then inserting the load pull test bench presented in chapter 2.4.3 at the drain of the transistor to find the optimal load impedances. When tuning the impedances of the load matching network, the optimal impedance at the source will change slightly, creating the need to adjust the source matching impedance to achieve the best possible result. This was solved by inserting the test bench at the source instead of a realized network. The test bench had to be reversed so that port 1 is facing the transistor gate (fig.3.6). This created the possibility to do both load and source pull on Γ_S and Γ_L simultaneously to more efficiently find the optimal impedances.

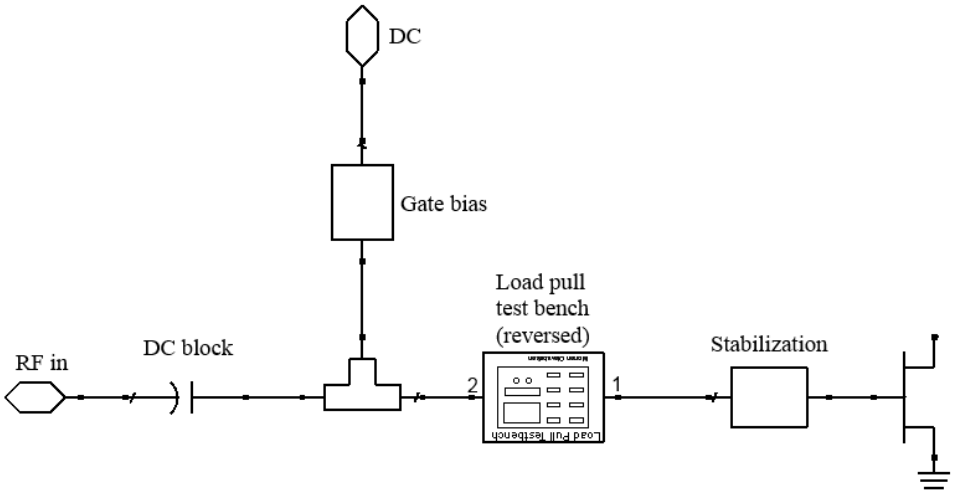


Figure 3.6: Using the test bench reversed to find optimal impedances for the source matching network.

Figure 3.6 shows the test bench inserted before the stabilization network. The source test bench was optimized for maximum gain where $\Gamma_{in} = \Gamma_S^*$. The goals in table 3.2 were set to achieve this, where stability was set as the highest priority.

Table 3.2: Optimization goal to match for maximum gain at the source matching network.

	Goal	Frequency range
Gain (S_{21})	≥ 15 dB	1.8-3 GHz
Stability	> 1	0.1-3 GHz
Input Reflection (S_{11})	< -10 dB	1.8-3 GHz

After obtaining a satisfying small signal results from the source test bench, the load test bench was inserted at the drain and the circuit could be further optimized using large signal harmonic balance simulations. Since the impedances found at the source should be the most optimal for the transistor, they were allowed only to move $\pm\ 5\%$ in the optimization since it is expected that they will need to change a little as the load impedances changes. The test benches were set to tune $\Gamma_S\ (f_0)$ and $\Gamma_L\ (f_0)$ with optimization goals that will maximize gain and output power. With the fundamental frequency tuned to optimal impedances, the harmonics $\Gamma_L\ (2f_0)$ and $\Gamma_L\ (3f_0)$ were tuned to maximize PAE. These simulations were done for the bandwidth frequencies from $1.8 - 3$ GHz with 200 MHz steps. The result are presented in table 3.3.

Table 3.3: Optimal impedances from load pull test bench simulations.

	Source	Load		
Frequency	$\Gamma_{opt}\,(f_0)$	$\Gamma_{opt}\,(f_0)$	$\Gamma_{opt}\,(2f_0)$	$\Gamma_{opt}\,(3f_0)$
1.8 GHz	$0.69\angle -141°$	$0.44\angle 124°$	$1\angle 115°$	$1\angle -55°$
2.0 GHz	$0.7\angle -119°$	$0.49\angle 128°$	$1\angle 128°$	$1\angle -24°$
2.2 GHz	$0.72\angle -95°$	$0.54\angle 135°$	$1\angle 130°$	$1\angle 12°$
2.4 GHz	$0.71\angle -68°$	$0.59\angle 137°$	$1\angle 138°$	$1\angle 40°$
2.6 GHz	$0.67\angle -46°$	$0.59\angle 140°$	$1\angle 155°$	$1\angle 61°$
2.8 GHz	$0.68\angle -24°$	$0.63\angle 145°$	$1\angle 156°$	$1\angle 180°$
3.0 GHz	$0.72\angle 5°$	$0.63\angle 150°$	$1\angle 167°$	$1\angle 94°$

A representation of the impedances in table 3.3 are plotted in a Smith chart in figure 3.7. Both source and load impedances move counterclockwise with increasing frequency in the Smith chart. This is in theory impossible, but can be solved by either moving clockwise in loops or with a negative transmission line. The complexity of trying to implement negative transmission lines, which require a large network of capacitors and inductors, was decided as not necessary as the looping method is a better solution in this assignment.

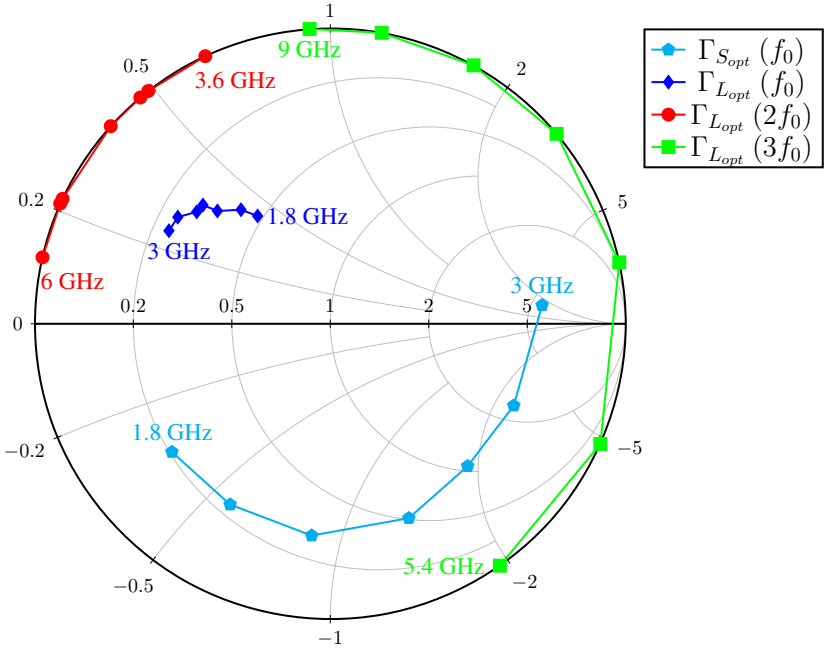


Figure 3.7: Optimal source impedances for source and load matching networks with increasing frequency moving counterclockwise.

3.3.4 Realizing Test Bench Results

With the optimal impedances for the two matching networks found, the process of realizing them in microstrip lines and passive components can be done. The source matching network is the easiest to match, as it only has to take into account the impedances at f_0. The impedances can be inputted as separate goals so that ADS can try to match each point exactly, but since a looping method must be used it will not be able to achieve perfect matching. By using each points gain circles it is easier to achieve better results as the simulation program can be set to try and match each point, for example within the circle with 1 dB loss in gain. A way to calculate the gain difference between the optimal impedance and the simulated is to use equations 2.9 and 2.10 in chapter 2.1.1. Equation 2.10a. shows the gain condition for the source matching network and together with the optimal impedances found in table 3.3 it can be used as a simulation goal in ADS. The expression will then be written as

$$G_S = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{opt}^* \Gamma_S|^2} = \frac{1 - |S_{11}|^2}{|1 - \Gamma_{opt}^* S_{11}|^2}, \tag{3.1}$$

where S_{11} is calculated continuously in ADS to match Γ_{opt}. Maximum gain is achieved when $S_{11} = \Gamma_{opt}$ and the resulting expression will be

$$G_{S_{max}} = \frac{1 - |\Gamma_{opt}|^2}{|1 - \Gamma_{opt}^* \Gamma_{opt}|^2} = \frac{1}{|1 - \Gamma_{opt}|^2}. \tag{3.2}$$

By combining equation 3.1 and 3.2 the difference between the simulated gain and the optimal gain can be written as

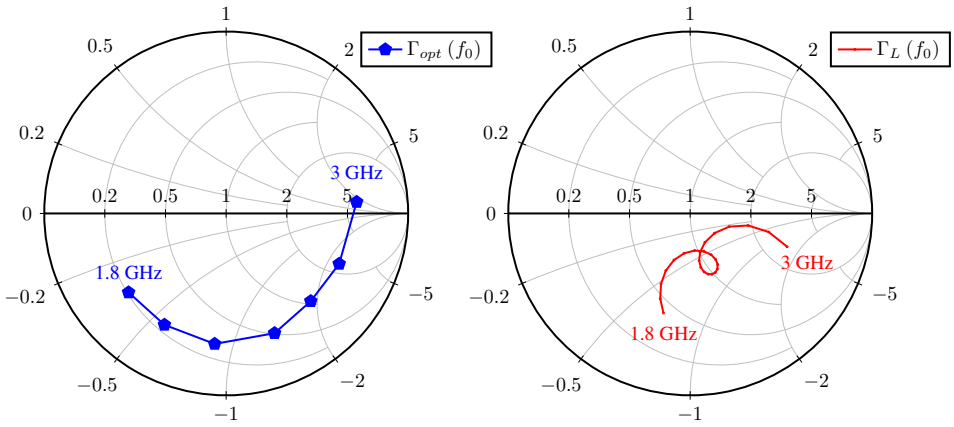
$$\Delta G = \frac{G_S}{G_{S_{max}}} = \frac{1 - |S_{11}|^2}{|1 - \Gamma_{opt}^* S_{11}|^2} \cdot (1 - |\Gamma_{opt}|^2). \tag{3.3}$$

This makes it possible for ADS to continuously calculate the gain difference while simulating. By using equation 3.3 and creating an expression for each frequency of Γ_{opt} from table 3.3, the optimization goals in table 3.4 were used to create the matching network.

Table 3.4: Optimization goals used when realizing the source matching network.

	Goal	Frequency range	Weight
ΔG (for each freq. step)	< -1 dB	1.8-3 GHz	High
Average ΔG	$= 0$ dB	1.8-3 GHz	Medium

The "Average ΔG" goal was added as a way to ensure an even error distribution as ADS tended to favor the points which were easier to match making the gain difference very high at other frequencies. After experimenting with different combinations of microstrip lines and open circuit stubs, the network that was chosen had the impedances presented in the Smith chart in figure 3.8b.



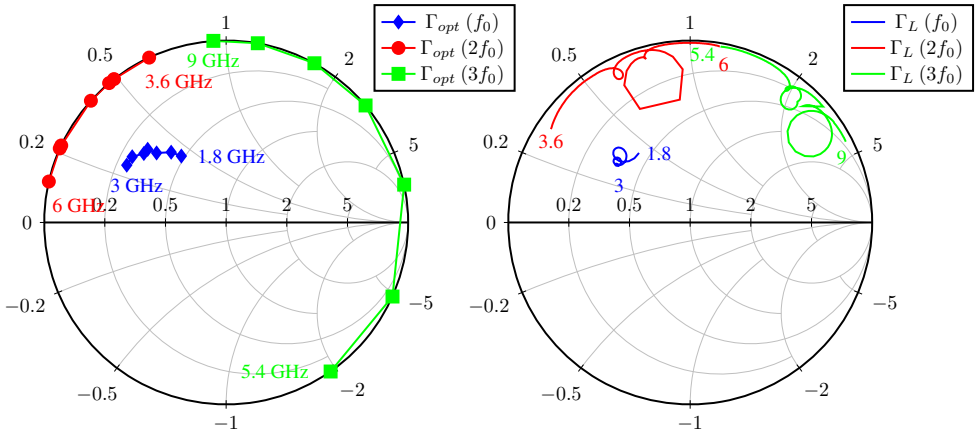
(a) Optimal source impedances.

(b) Impedances from the realized source matching network.

Figure 3.8: Comparison of the optimal impedances from the test bench and the realized network.

Figure 3.8b illustrates the looping characteristics of the realized network. From the optimization in ADS it was found that each point could be matched individually, but it was not possible to get closer to the optimal impedances when matching all the points together. So the highest frequencies were prioritized, as this is where the gain is lowest and most vulnerable to a large gain difference. The result was an average gain difference of around 3 dB lower than the optimal case.

The load matching network is more complex to match, as the harmonics at $2f_0$ and $3f_0$ are included. These harmonics are created when the transistor is driven into compression, making the output non linear. This makes equation 3.3, which was used at the source matching optimization, no longer valid. To create a set of optimization goals for ADS which can be used effectively, the load network impedances in table 3.3 were individually tuned to find the limits where the PAE were at $\pm 5\%$ of its maximum value. With these limits mapped, the matching is easier because the areas of where each impedance is allowed to be in can be set as optimization goals.



(a) Optimal source impedances.

(b) Impedances from the realized load matching network.

Figure 3.9: Comparison of the optimal impedances from the test bench and the realized network.

After experimenting with combinations of microstrip lines and open circuit stubs, the impedances presented in the Smith chart in figure 3.9b were found to give the best results. The matching at f_0 was prioritized in the optimization since it is most important, while $2f_0$ and $3f_0$ were allowed to have more error. The looping worked as planned as it is able to move in the "wrong" direction in the Smith chart.

3.4 Measurements

In this section the measurement setup used for the small and large signal measurements are presented. Two PCBs were manufactured using a LPKF circuit board plotter by the workshop at NTNU. The rest of the assembly with soldering the components and transistor was performed and tested at the ANA lab. The PCBs were then mounted on 85x85 mm heat sinks which provides a common ground for the amplifier. All measurements were performed at the ANA lab at with assistance from PhD. candidate Dragan Mitrevski.

3.4.1 Small Signal

The small signal setup used to measure the S parameters of the amplifier is shown in figure 3.10. The S parameters were measured with an Agilent E8364B PNA network analyzer. Since the PA can potentially output several watts, a directional coupler and an attenuator, which provided a total attenuation of 23 dB, was used between the RF output of the amplifier and port 2 on the analyzer. This will ensure that the power level is below the maximum input level of 30 dBm for the PNA.

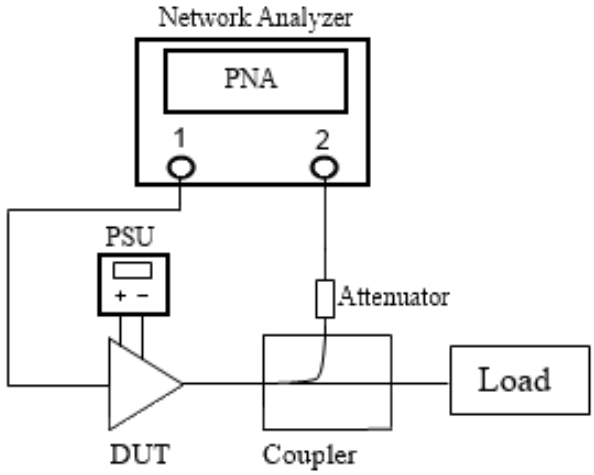


Figure 3.10: Schematic for the small signal measurement setup.

To ensure correct measurements, a SOLT calibration was performed. The DUT was removed and calibration parts were placed on the SMA connectors of port 1 and the coupler (port 2) so that both the coupler and attenuator was included in the calibration. Performing the calibration with the coupler and attenuator attached ensures that the effects of the attenuation on the S_{21} measurements are removed. The reflection measurements S_{22} and S_{12} will still be distorted by noise as discussed in chapter 2.5.3. As a result of the calibration, the reference and measurement plane is now between the input and output SMA connectors of the amplifier.
Table 3.5 gives an overview of the equipment used in the small signal measurement setup.

Table 3.5: Overview of the small signal measurement equipment.

Manufacturer	Model	Description
Agilent Techn.	PNA (E8364B)	General purpose vector network analyzer (VNA) used for multi-port measurements.
HP Agilent	Calibration kit (85052D)	Calibration kit, DC to 26.5 GHz, 3.5 mm.
Narda	Broadband Coupler (5292)	Broadband high directivity coupler (1-18 GHz) with 13 dB attenuation.
Narda	Load Termination (374BNM)	20W AVG load termination from DC-18 GHz.
TTi	Power Supply (EL302Tv)	Power supply to drive the amplifier.

3.4.2 Large Signal

The schematic for the large signal measurement setup are shown in figure 3.11. Both amplifiers that were manufactured are used in the measurements.

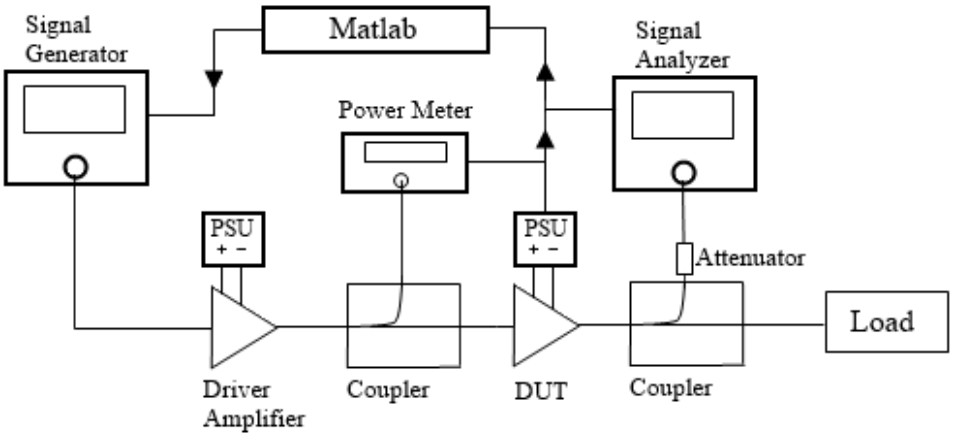


Figure 3.11: Schematic for the large signal measurement setup.

A predefined Matlab script controls the signal generator to output the desired signal and frequency sweep for the measurement. Since the signal generator has a maximum output power of 26 dBm it is amplified in a driver amplifier before reaching the DUT. A power meter is connected after the driver amplifier to get accurate power readings of the input power to the DUT. After amplification the signal is terminated in a 20 W load and coupled through an attenuator before reaching the signal analyzer. The attenuation of the signal is to protect the measuring equipment as previously discussed. The signal analyzer feeds the measurement data back to Matlab through a GPIB[1] interface and is stored for further processing. The power meter measurements and current measurements from the power supply are also connected through the same interface.

The raw data received from the signal analyzer needs to be processed before the correct measurements can be found. Since the attenuator, cables and couplers introduce loss to the signal, they were separately measured at the same frequency range as the DUT. These losses are used to correct the data to acquire the actual performance measurements of the DUT. With reference to figure 3.11, the input cable and coupler to the power meter were measured separately, while the coupler, attenuator and cable at the output were measured together.

Looking at the schematic from figure 3.11, the input power delivered to the DUT can be found by using the power meter reading and correcting for loss. This is found by adding the loss from the coupling to the power meter and then subtracting the throughput loss

[1] GPIB is an acronym for *general purpose interface bus* and is an IEEE standard (IEEE–488) for short range digital communication.

to get the power level at the input of the DUT. To find the output power, the loss of the coupler, attenuator and cable at the output is added to the measurement from the signal analyzer. The corrected data can now be used together with the data from the power supply to calculate gain, PAE, drain efficiency etc.

Table 3.6 lists all the equipments used in the large signal measurements.

Table 3.6: Overview of the large signal measurement equipment.

Manufacturer	Model	Description
Rhode & Schwarz	Vector Signal Generator (SMU200A)	Signal generator used in large signal 1- and 2-tone measurements.
Rhode & Schwarz	Signal Analyzer (FSQ40)	Analyzes and records the measured data from the DUT.
Anritsu	Power Meter (ML2438A)	Power meter used for precise measurements of the output power from the driver amplifier.
TTi	Power Supply (EL302Tv & QL355TP)	Power supply to drive the amplifiers.
Narda	Broadband Coupler (5292)	Broadband high directivity coupler (1-18 GHz) used at load termination and to power meter.
Narda	Load Termination (374BNM)	20W AVG load termination from DC-18 GHz.
Huber+Suhner	Sucoflex cable (104P)	Cables used to connect the DUT to signal generator and analyzer.

Chapter 4

Results

In this chapter the results of the simulations and the measurements of the manufactured amplifier are presented. The chapter is divided into two sections and the results will only be commented briefly as they will be discussed and analyzed in chapter 5.

4.1 Simulations

This section presents the results from the simulation of the amplifier done in Agilent ADS and is dived into three parts. The test bench results is with the optimal impedances and represents the best result achievable in this design. The simulation results from the final design are presented together with the final stabilization factor. The last section presents the simulated performance when the amplifier is operating at 1 dB compression. This is included as it is an important performance parameter in characterizing a PA.

4.1.1 Test Bench

The output power with lossless test benches are shown in figure 4.1. The figure indicates an output of over 40 dBm from about 25-35 dBm input power for the frequencies shown. Since the test bench is lossless, the realized networks is expected to have less optimal characteristics.

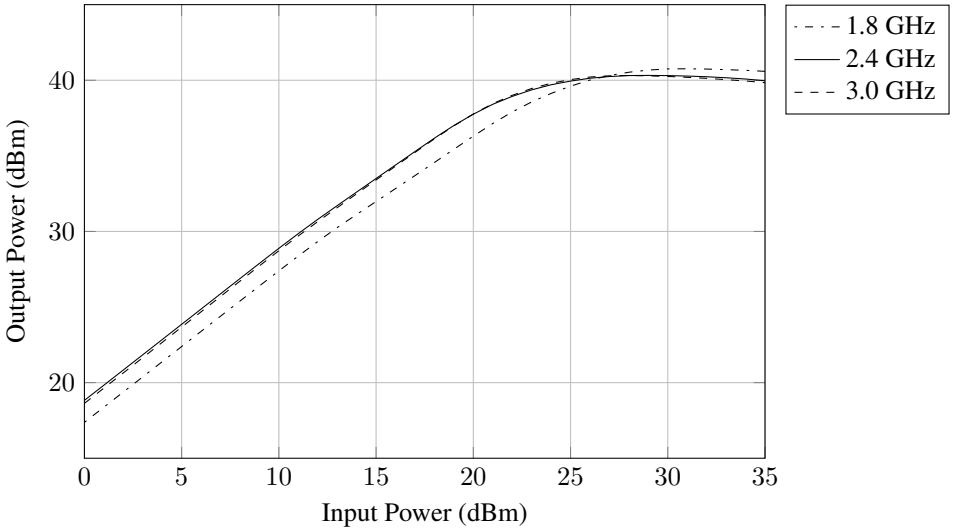


Figure 4.1: Output power with lossless test benches.

The optimal transducer gain are presented in figure 4.2. The figure shows that the gain stays above 15 dB up to around 25 dBm input power.

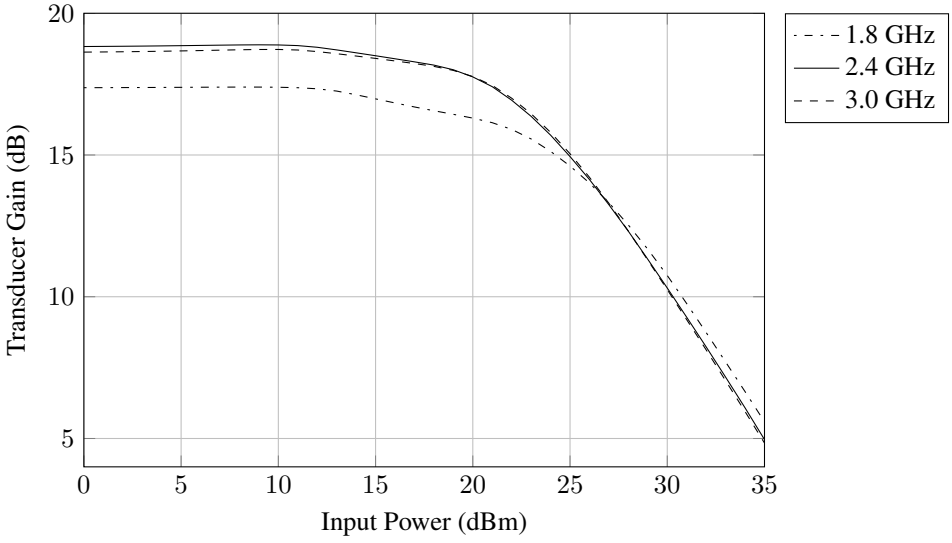


Figure 4.2: Transducer power gain with lossless test benches.

The drain efficiency using test benches is presented in figure 4.3. At the center frequency, the efficiency is above 80% at input power from 27-35 dBm.

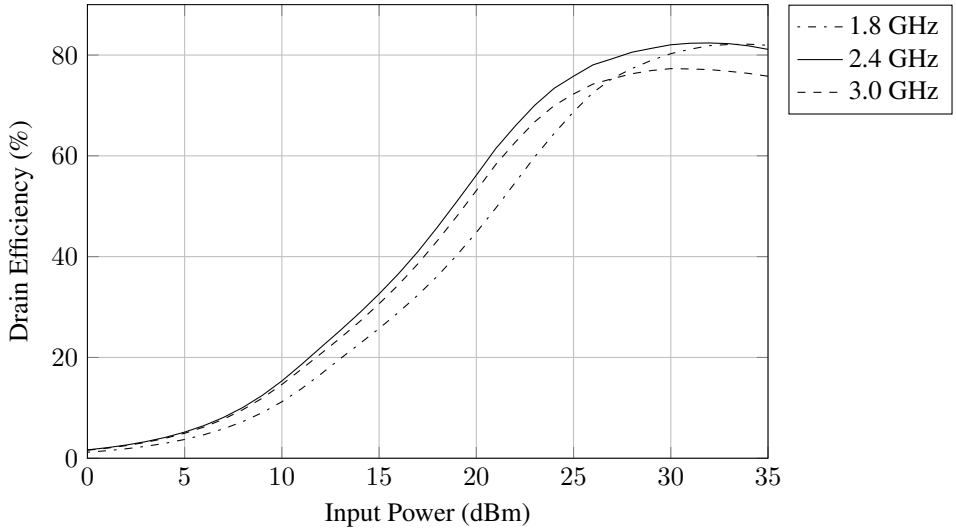


Figure 4.3: Drain efficiency with lossless test benches.

Figure 4.4 shows the simulated PAE. The graphs indicate a more narrow peak and the values are about 5% lower than the drain efficiency.

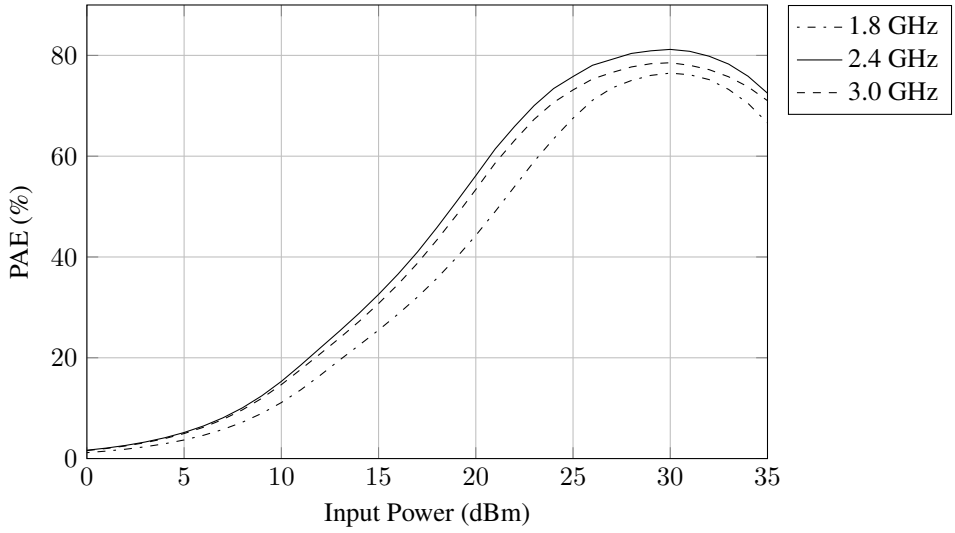


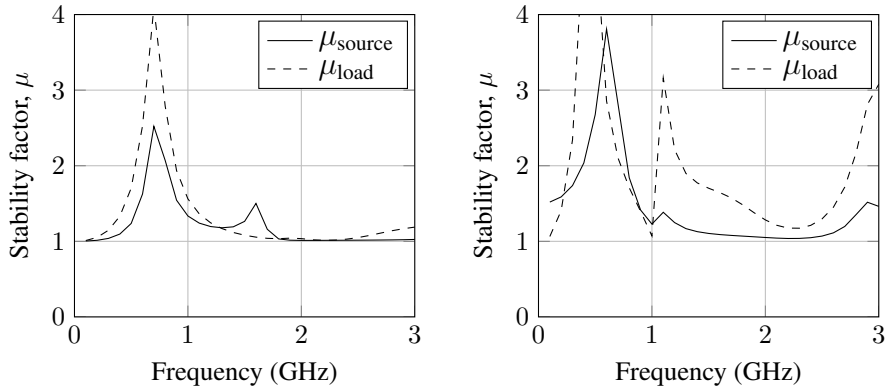
Figure 4.4: Power added efficiency with lossless test benches.

The key performance parameters using the optimal impedances of the amplifier are listed in table 4.1. The results are presented by their maximum value and the value at 1 dB compression.

Table 4.1: Key parameters of the amplifier using the load pull test bench.

	$\eta\,(\%)$		$\eta_{\text{PAE}}\,(\%)$		$P_{out}\,(dBm)$		$Gain\,(dB)$	
Frequency	Max	P_{1dB}	Max	P_{1dB}	Max	P_{1dB}	Max	P_{1dB}
1.8 GHz	80.27	72.57	76.48	71.10	40.75	40.01	10.75	14.01
2.0 GHz	81.90	75.04	79.23	74.08	40.70	40.13	10.70	14.13
2.2 GHz	82.90	77.93	81.14	77.44	40.72	40.41	10.72	14.41
2.4 GHz	82.04	78.05	81.19	78.04	40.31	40.13	10.30	14.13
2.6 GHz	81.71	78.17	82.38	78.73	40.47	40.33	10.47	14.33
2.8 GHz	80.98	77.42	82.76	78.44	40.20	40.15	10.20	14.15
3.0 GHz	77.30	74.24	77.71	73.15	40.31	40.04	12.32	15.04

4.1.2 Final Design



(a) After stabilizing the transistor.

(b) Stability with matching networks.

Figure 4.5: Comparison of stability of the transistor and the stability of the final design.

In figure 4.5, a comparison of the stability factors for the transistor and the final design is presented. It shows that the final design is unconditionally stable from 0.1 - 3 GHz, where the μ factors indicate a better margin of stability.

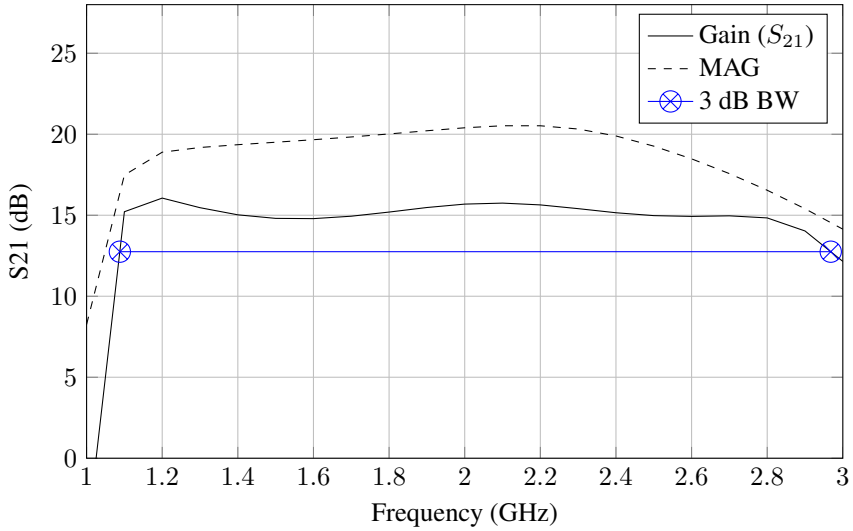


Figure 4.6: Simulated small signal gain versus maximum available gain for the realized matching networks.

The small signal gain S_{21} of the amplifier shows good performance down to 1.1 GHz as shown in figure 4.6. The gain is flat with only small variations up to 2.8 GHz. The 3 dB bandwidth is indicated in the figure and it is approximately 1.88 GHz.

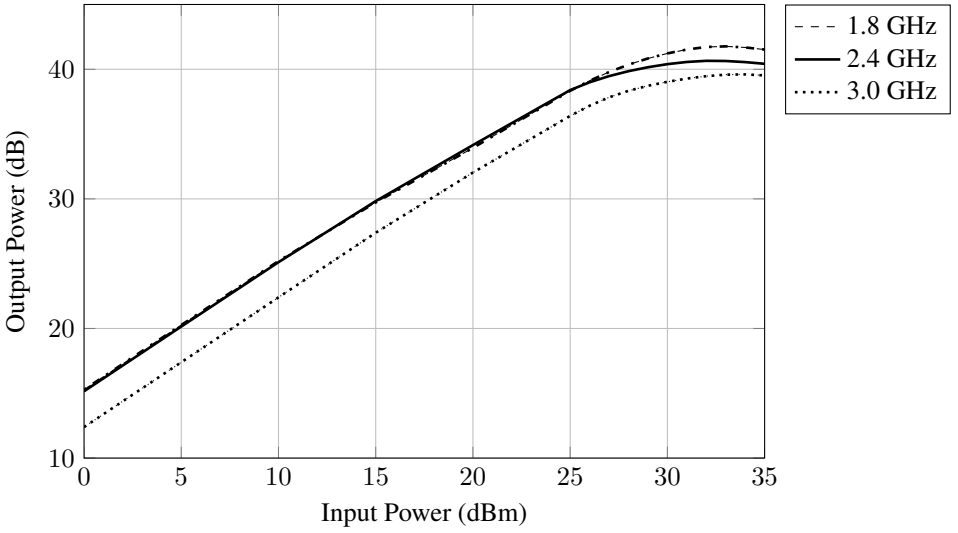


Figure 4.7: Simulated output power of the final design.

In figure 4.7, the output power for the final design with realized matching networks are presented. Compared to the optimal case, the output power is peaking at about 29-35 dBm

with 1 dB compression around 29 dBm for all three frequencies. At 3 GHz, it has dropped below 40 dBm and is 0.5 dBm lower than in the optimal results.

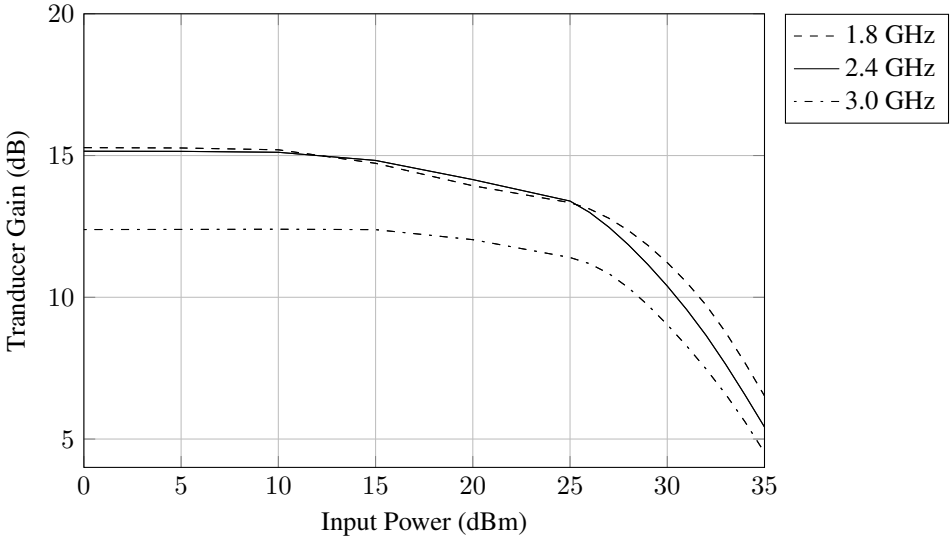


Figure 4.8: Simulated transducer power gain of the final design.

Figure 4.8 shows the transducer gain for the final design. Compared to the optimal results the gain has decreased about 4 dB.

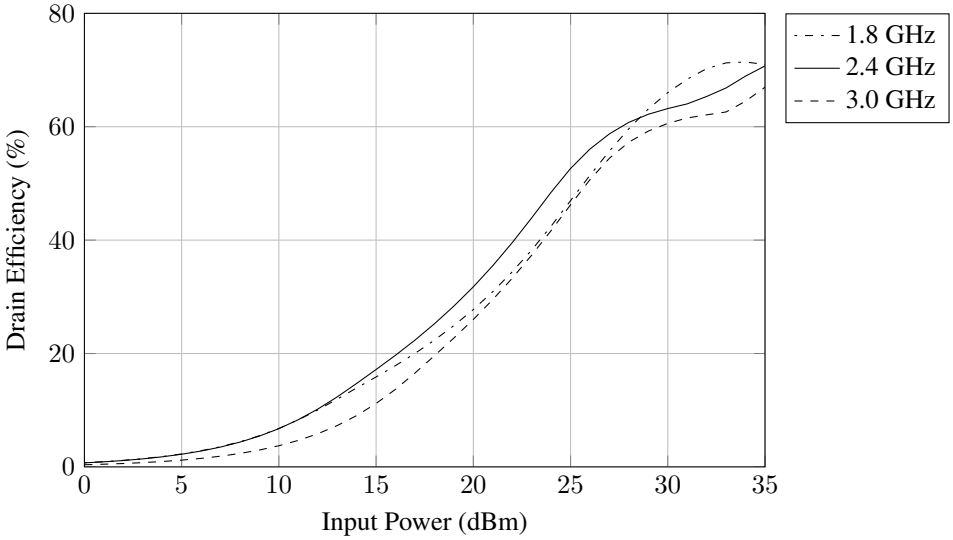


Figure 4.9: Simulated drain efficiency of the final design.

The simulated drain efficiency of the final design is shown in figure 4.9. The curvature of the graph at 2.4 and 3 GHz indicates that the amplifier is well into compression from 32 dBm and up.

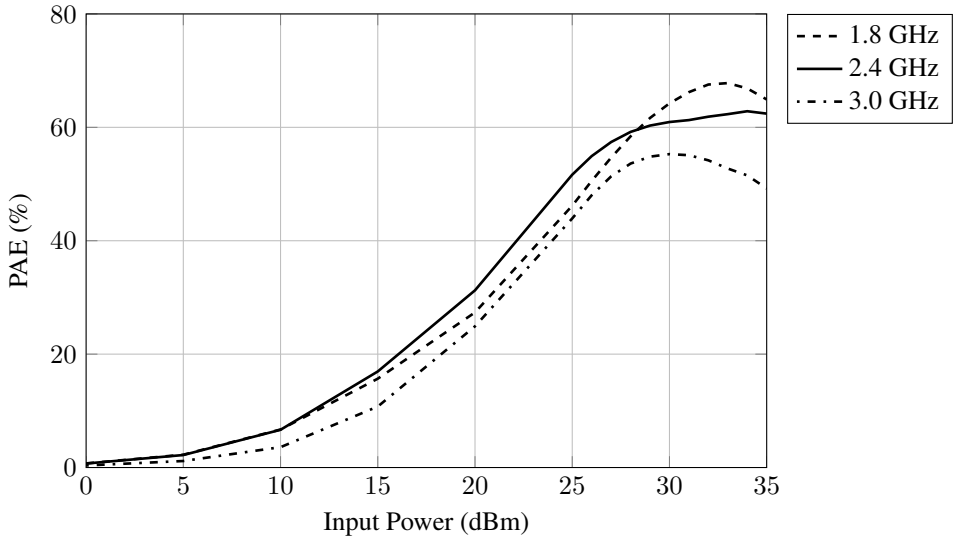


Figure 4.10: Simulated power added efficiency of the final design.

At the center frequency the simulated PAE is about 60% at an input power of 30 dBm. It is clear from the figure that as the frequency increases, the input level where maximum efficiency is achieved decreases. At 3 GHz the peak has the largest deviation from the test bench results.

The key performance parameters of the simulated final design is summarized in table 4.2. The results are presented by their maximum value and the value at 1 dB compression.

Table 4.2: Key parameters of the simulated final design.

	η (%)		η_{PAE} (%)		P_{out} (dBm)		$Gain$ (dB)	
Frequency	Max	P_{1dB}	Max	P_{1dB}	Max	P_{1dB}	Max	P_{1dB}
1.8 GHz	71.26	63.13	67.80	61.65	41.77	40.84	8.77	11.84
2.0 GHz	70.60	65.00	66.19	63.20	41.16	40.57	8.11	11.57
2.2 GHz	69.92	65.56	65.36	63.74	40.95	40.56	7.86	11.56
2.4 GHz	66.84	62.20	62.84	60.31	40.65	40.16	7.64	11.16
2.6 GHz	69.87	64.45	64.81	62.23	40.97	40.38	7.97	11.38
2.8 GHz	69.38	64.20	62.02	60.85	40.62	40.11	7.54	11.10
3.0 GHz	62.60	59.23	55.27	54.83	39.61	39.73	6.59	9.73

4.1.3 1 dB Compression

Figure 4.11 shows the output power at the 1 dB compression point versus frequency. As the amplifier was found to have good performance down to about 1.1 GHz, these frequencies are included in the figure.

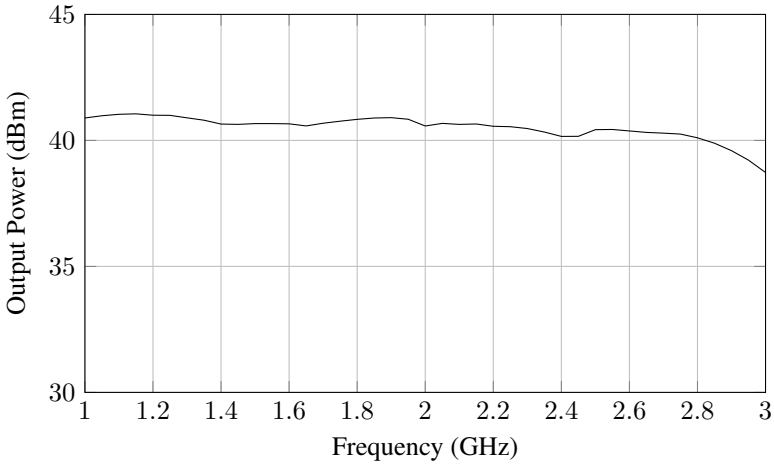


Figure 4.11: Output power versus frequency at 1 dB compression.

The transducer gain at the 1 dB compression point is plotted against frequency in figure 4.12. The gain is relatively flat from 1 GHz to 2.8 GHz and drops by a few dBs at 3 GHz. The average gain is about 12 dB from 1 - 3 GHz.

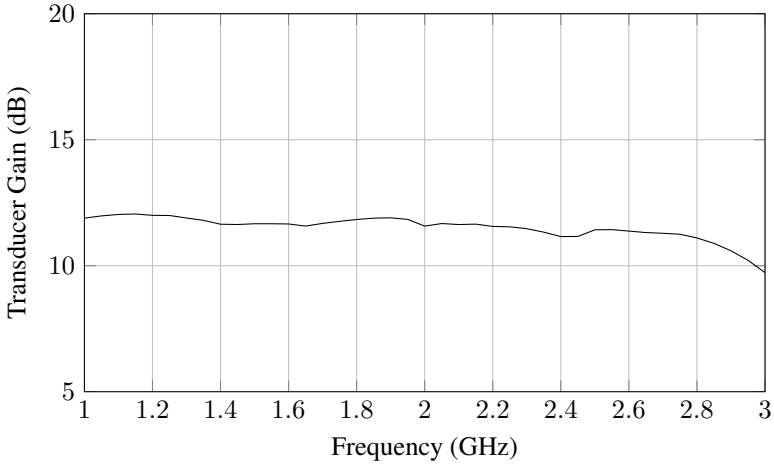


Figure 4.12: Transducer power gain versus frequency at 1 dB compression.

Simulated drain efficiency at the 1 dB compression point plotted versus frequency are

presented in figure 4.13. The average efficiency through the frequency band 1 - 3 GHz is close to 60%. In the bandwidth of the assignment the efficiency is higher than 60%.

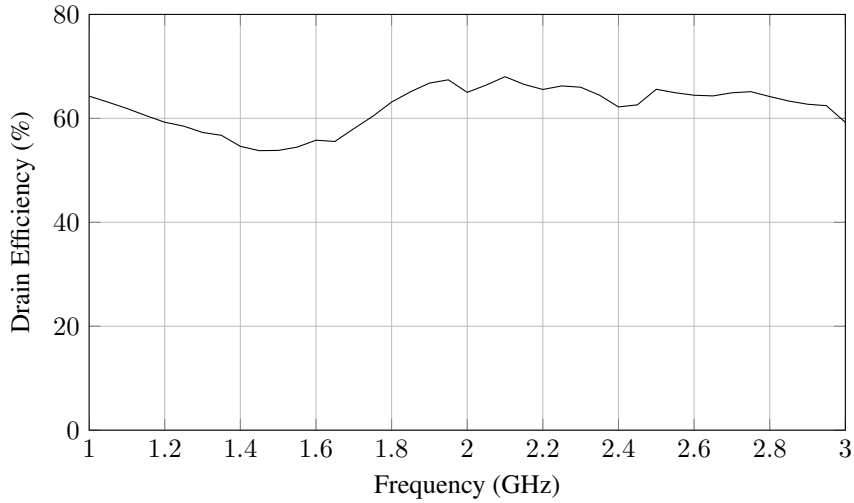


Figure 4.13: Drain efficiency versus frequency at 1 dB compression.

Power added efficiency at the 1 dB compression point is plotted versus frequency in figure 4.14. The average is around 60% for the PAE.

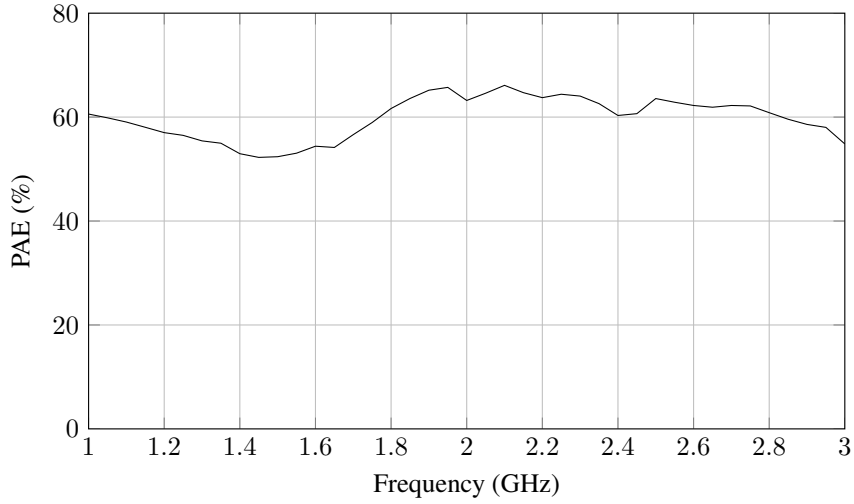


Figure 4.14: PAE versus frequency at 1 dB compression.

4.2 Measurements

In this section the measurement results from the lab is presented. The large signal data has been correct in Matlab before calculations were done. The small signal S parameter measurements are presented for the two manufactured amplifiers. The large signal measurements together with the two tone results are presented in the last section.

4.2.1 Small Signal

The measured gain is shown in figure 4.15. In the bandwidth from 1.8 - 3 GHz the result is very similar to the simulation, but there is larger differences lower in frequency.

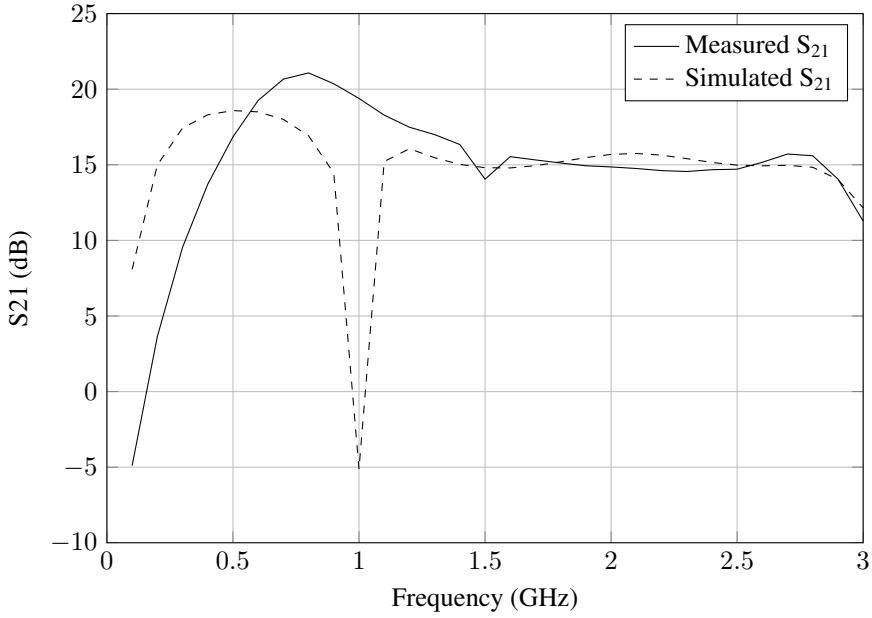


Figure 4.15: Measured versus simulated small signal gain.

The gain of two manufactured amplifiers are compared in figure 4.16. As expected they are very similar where ”Amplifier 2” has slightly less fluctuations than ”Amplifier 1”.

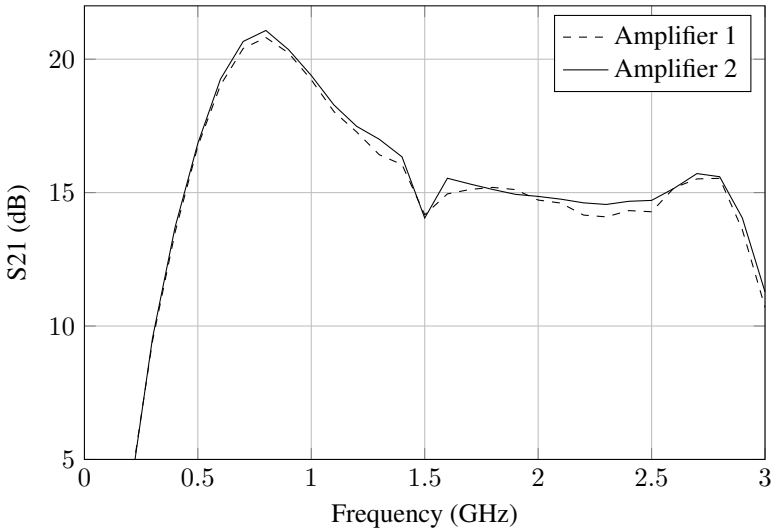


Figure 4.16: Measured small signal gain for the two manufactured amplifiers.

The bandwidth of the measured ”Amplifier 2” is presented in figure 4.17. Both the 1 dB (1.3 GHz) and 3 dB (2.57 GHz) bandwidth are indicated as both meets the requirement from the assignment text.

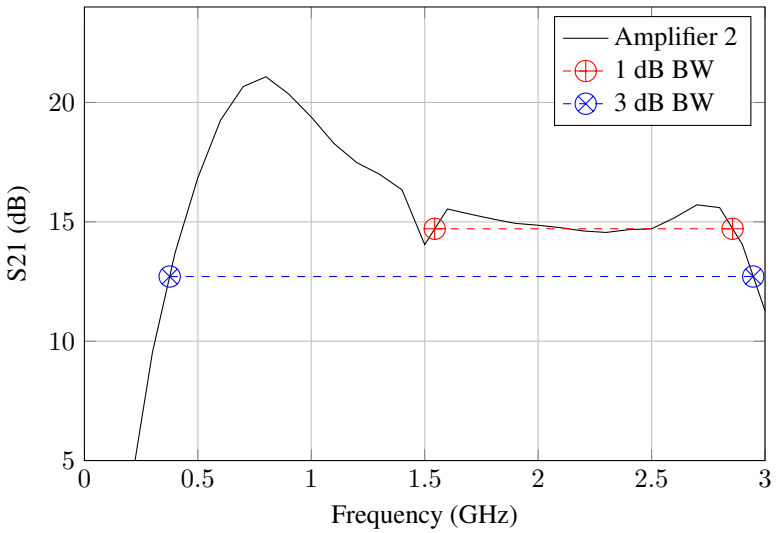


Figure 4.17: Measured gain with the 1 dB and 3 dB bandwidth indicated.

The reflection coefficient S_{11} at the input of the amplifiers are presented in figure 4.18. The measured reflection is equal or better than the simulated in the bandwidth except at 2.9 - 3 GHz. There are also some mismatches below the bandwidth where the amplifier is not matched in the design.

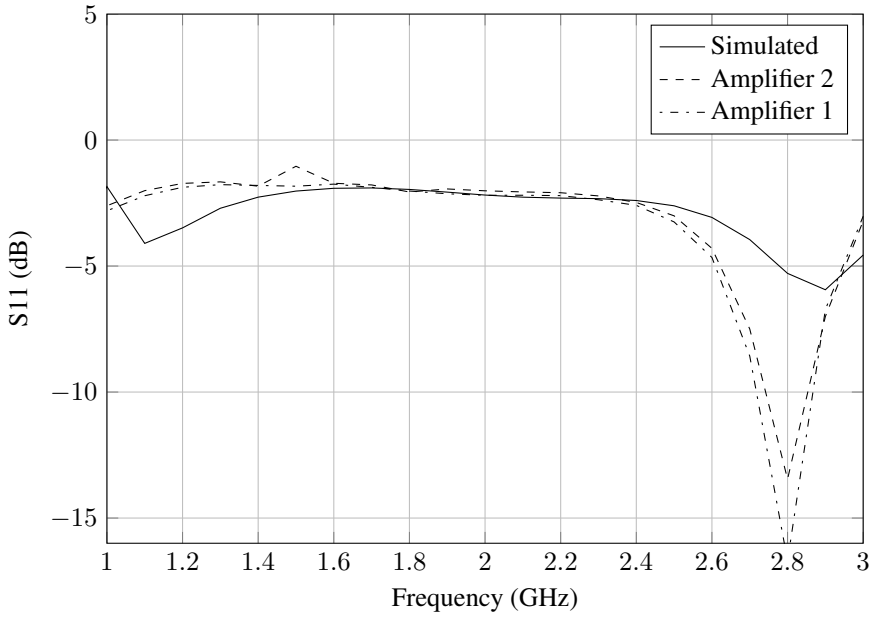
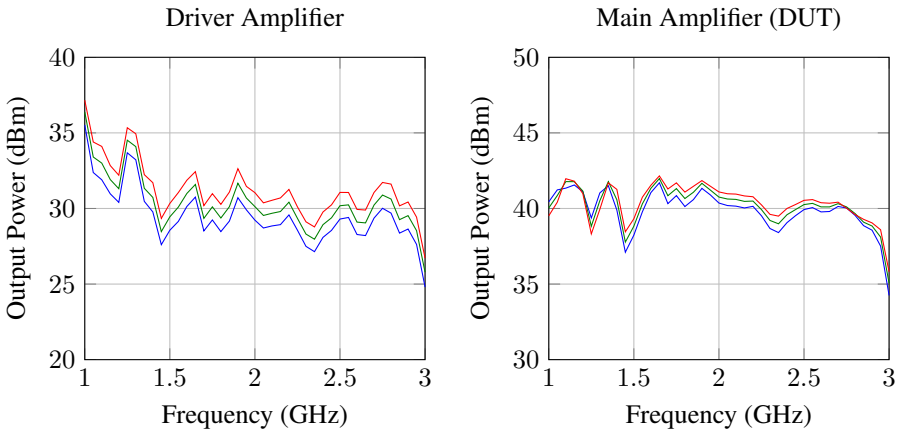


Figure 4.18: Comparison of S_{11} of the two manufactured amplifiers and the simulation.

4.2.2 Large Signal

Figure 4.19a shows the amplified output from ”Amplifier 1” which is used as a driver amplifier in the measurement setup and is the input power to the DUT (”Amplifier 2”). The graphs from bottom to top is output levels 21-26 dBm from the signal generator. Both figures show that the amplifiers perform poorly at 2.9 - 3 GHz compared to the simulations. The output power from the DUT in figure 4.19b is when the amplifier is at or around 1 dB compression.



(a) Input power delivered to the DUT.

(b) Output power from the DUT.

Figure 4.19: Comparison the output power of the driver and DUT versus frequency.

The results presented so far indicate that the amplifier is showing poor results at 2.8 - 3 GHz compared to the simulations. The rest of this section will as a result of this present the amplifiers performance from 1.6 - 2.8 GHz as this is the frequency range where the amplifier is optimal and should be utilized.

The following results is with the measurements setup where ”Amplifier 1” is the driver amplifier and ”Amplifier 2” is the DUT. There was also done measurements where the amplifiers were switched which resulted in very similar results, but marginally lower performance.

The measured output power of the DUT at different frequencies are presented in figure 4.20. The curvature above 30 dBm in the plots indicates that at 2.0 GHz and 2.4 GHz, the amplifier does not get further into compression than about 1 dB.

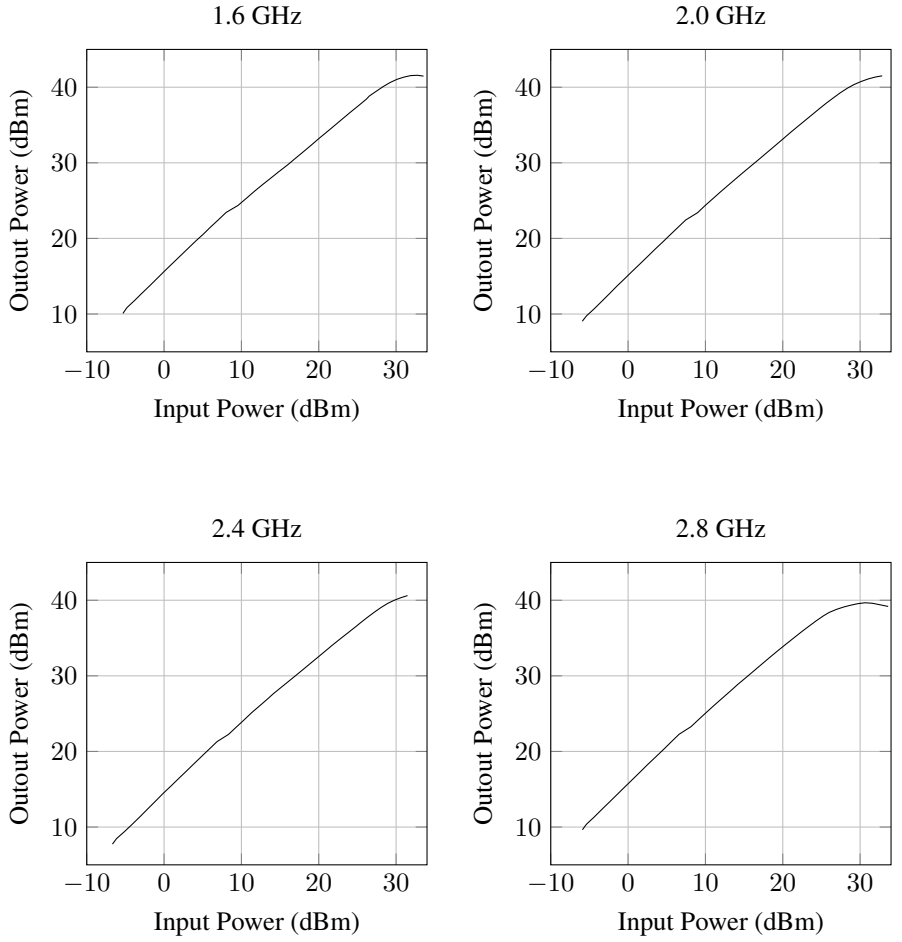


Figure 4.20: Comparison of input power versus output power at different frequencies.

The measured drain efficiency is presented in figure 4.21. At 2.8 GHz the amplifier goes far into compression around 55% as seen from the graph.

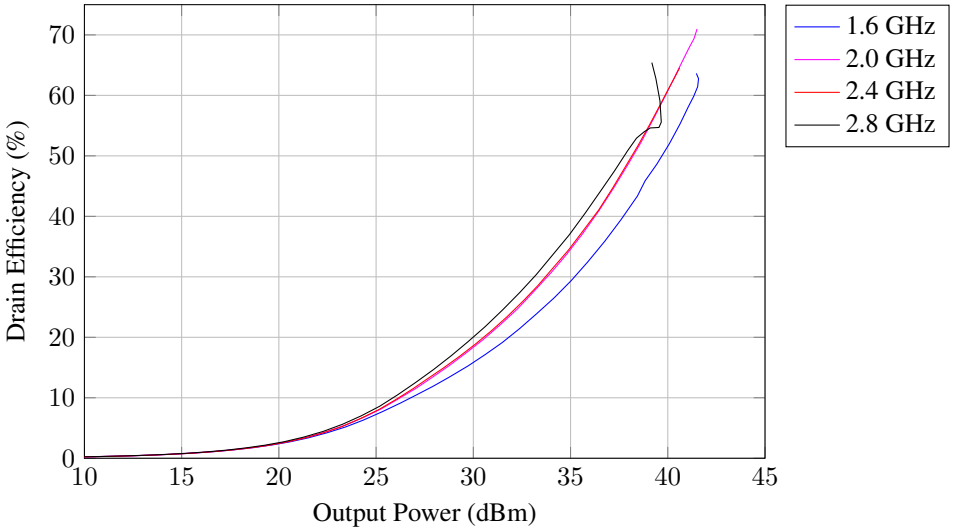


Figure 4.21: Measures drain efficiency of the amplifier.

The power added efficiency (PAE) of the DUT is presented in figure 4.22. The results are similar to the drain efficiency with a 5-10% decrease. Since the PAE include the input power in the equation it will in theory show a more realistic result than the drain efficiency, but in this case it has an uncertainty which will be discussed in the next chapter.

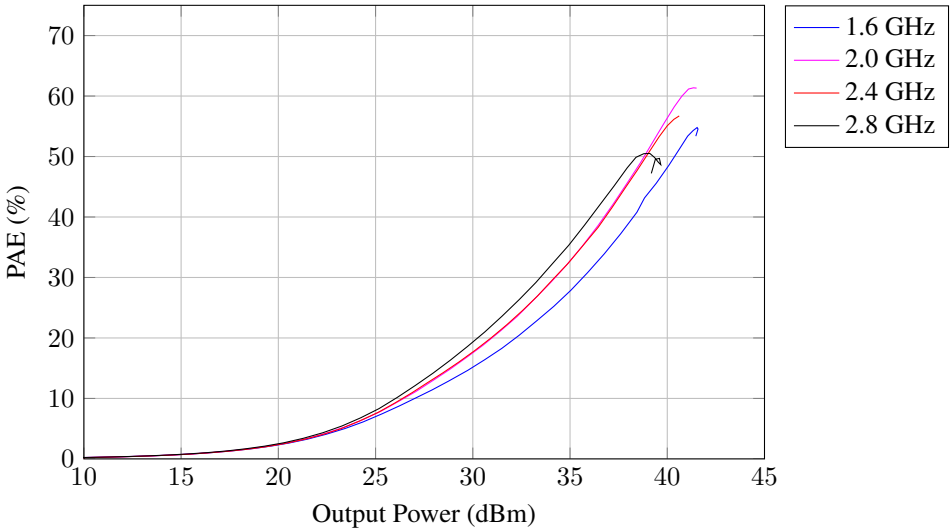


Figure 4.22: PAE of the measured amplifier.

The transducer gain of the amplifier is shown in figure 4.23. The measured gain shows similar characteristics as the simulated transducer gain.

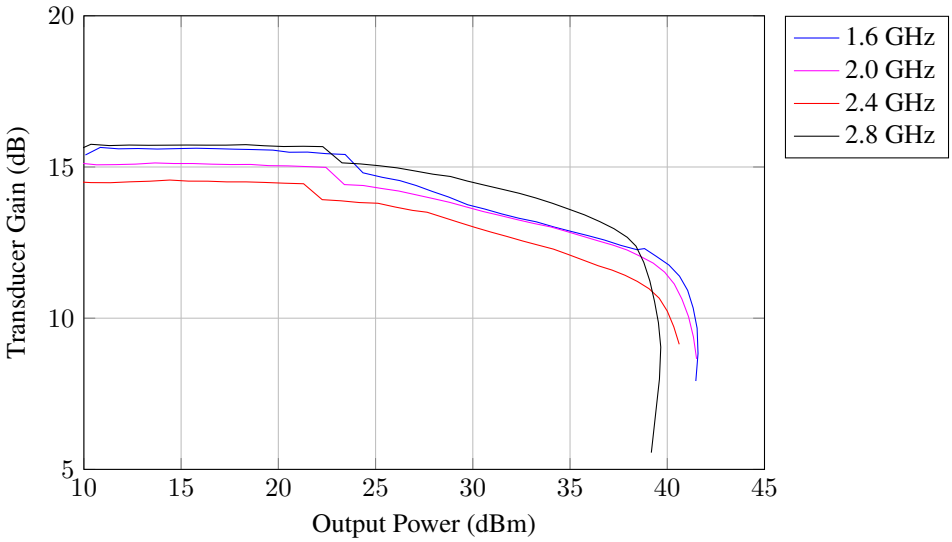


Figure 4.23: Measured transducer gain of the amplifier.

Measurements of the DC power consumption in the amplifier are shown in figure 4.24. At low frequencies the power consumption is largest and it is decreasing with frequency.

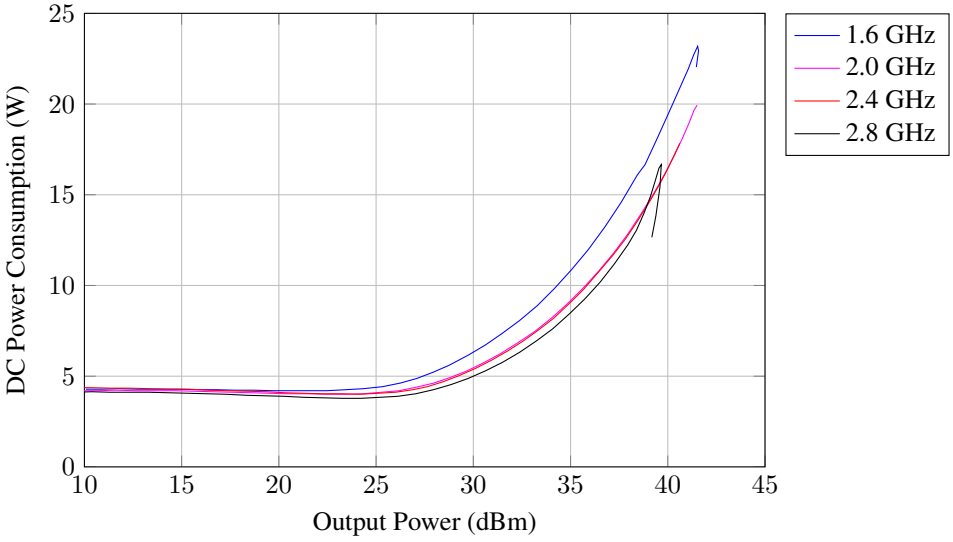


Figure 4.24: DC power consumption of the measured amplifier.

From the two-tone measurements of the amplifier, the third order IMD are presented at different frequencies in figure 4.25. The results show some asymmetries between the tones at lower frequencies.

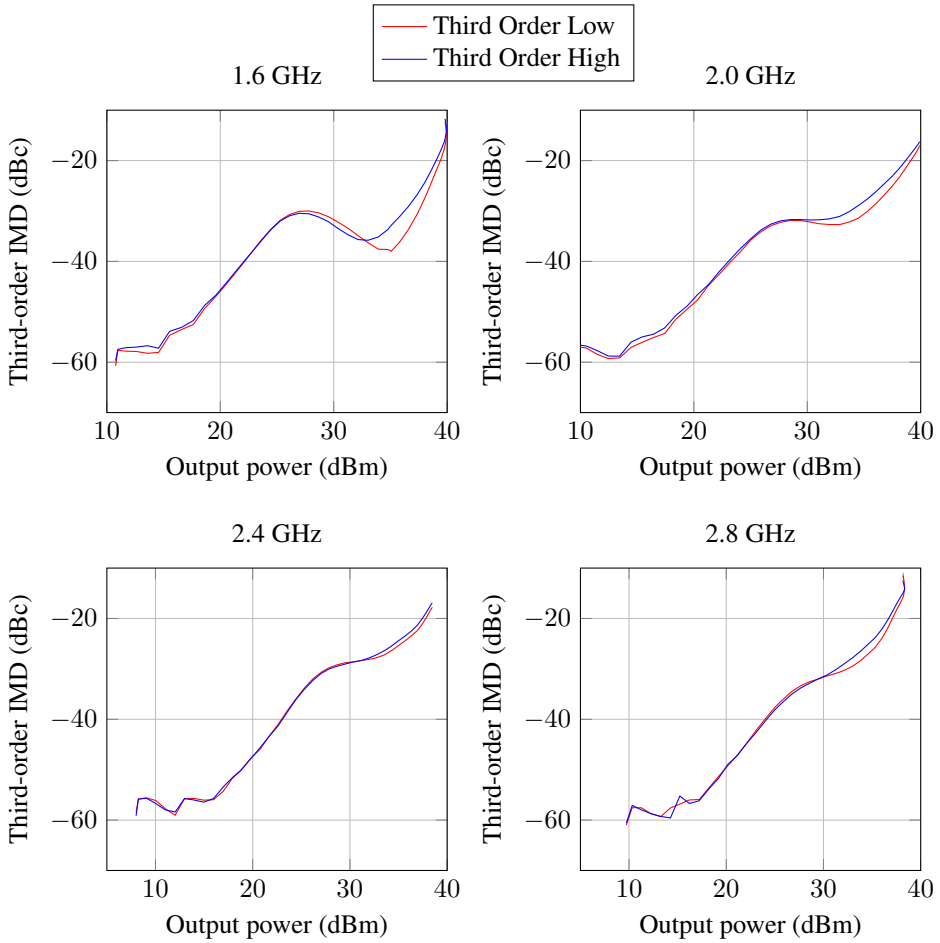


Figure 4.25: Comparison of IMD at different frequencies.

The measurement results are summarized in table 4.3, where all parameters are listed by its value when the amplifier is at 1 dB compression.

Table 4.3: Key parameters of the amplifier measurements at 1 dB compression.

Frequency	$\eta\,(\%)$	$\eta_{\text{PAE}}\,(\%)$	$P_{1dB}\,(dBm)$	$Gain\,(dB)$
1.6 GHz	62.64	54.55	41.58	8.92
1.8 GHz	62.45	57.33	41.06	10.84
2.0 GHz	66.31	60.35	40.85	10.47
2.2 GHz	61.41	54.94	40.65	9.76
2.4 GHz	63.90	56.71	40.62	9.14
2.6 GHz	59.64	53.67	40.56	9.99
2.8 GHz	54.66	49.95	39.30	10.69

Chapter 5

Discussion

In this chapter the design and results presented in this thesis will be analyzed and discussed. It is divided into three parts: design process, results of the measurements and simulations together with some proposed applications for the amplifier.

5.1 Design

The design was done in a step-by-step process with validation of results against theory after completion of each step, this design process proved to be effective as previous experience in amplifier design from projects could be utilized. From a preliminary project to this thesis, a class-F amplifier was designed and simulated with peak PAE at center frequency of 2 GHz with a bandwidth of 200 MHz using the same transistor. This provided valuable experience when designing the stabilization and bias networks in the startup phase of this assignment.

Together with the larger bandwidth, the load pull test bench was used much more extensively in the design process. Using a test bench at the source in addition to the load provided a much more flexible and better way to obtain the best results since the optimization in ADS could control both Γ_S and Γ_L at the same time. Appendix A shows the schematic for the test bench setup to find the optimal impedances. The stabilization, bias networks and some microstrip lines are the limiting factors to the lossless test benches as these could provide loss if not designed correctly.

Locating the optimal impedances using this method is a good way to visualize the S parameters you need to match to design a more efficient amplifier. The Cree 10 W transistors optimal impedances were shown to move in the counterclockwise direction in the Smith chart, making the process of matching the realized networks very challenging. To move in this direction, a looping method was used. In this method, the impedances move with increasing frequency in several clockwise loops to be able to travel in the ”wrong” direction. The method has its limitations as the loops can become large and will create loss. When

the impedance matching was performed, the amplifier had to be optimized for maximum PAE and output power because the impedances had changed as perfect matching is not achievable.

The layout of the amplifier is shown in appendix C. The drain and gate bias were designed to have the decoupling capacitors as close to the termination at the base of the fan as possible. Each capacitor has a VIA hole directly to ground to minimize parasitics. Using a wide and short open stub at the load provides a broadband capacitance effect compared to using tuned capacitors which would only be effective in a narrow frequency range.

To be able to classify an amplifier as class-F or class-F^{-1}, the drain voltage and drain current waveforms would have to be examined to see how the harmonic tuning has shaped them. The ADS model provided by Cree is measured and characterized as the physical transistor package that is mounted on the PCB. This means that the model includes the inner capacitive and inductive effects of the packaging around the transistor. As these effects will alter the current/voltage waveforms it is not possible to accurately simulate them. To be able to do that, a model of the inside of the transistor package must be available. Cree only makes this model available for certain partner schools and unfortunately NTNU is not one of them. So for this thesis, the conclusion of which class-F operation is achieved can not be said with certainty. However, the performance and efficiency of the amplifier is a good indicator if class-F is achieved or not.

5.2 Results

In this section the results of the simulations and measurements are discussed.

5.2.1 Simulations

The simulation results using the optimal and lossless test benches are presented in chapter 4.1.1. These results indicate the best performance this transistor can achieve with the stabilization and bias networks designed in this thesis. Table 4.1 shows that a drain efficiency that is larger than 80% in almost the entire bandwidth is obtained. This indicates that the device is operating in a class-F or class-F^{-1} mode. The PAE is larger than 75% in the bandwidth while delivering an output power larger than 40 dBm. These simulation results verified that the test benches were working and the that the impedances found were the optimal, or at least very close to optimal.

The 3 dB bandwidth from the simulations are shown in figure 4.6 to be approximately 1.8 GHz. The gain is flat all the way down to about 1.1 GHz before it decreases rapidly. From the requirements listed in the assignment text of the thesis, the 3 dB bandwidth is required to be 1.2 GHz. The maximum available gain is included in the figure to illustrate that when designing an amplifier to have flat broadband gain, the average gain will decrease as the bandwidth gets larger. The large signal performance of the final design indicates that the results match the test bench simulation reasonably good, but at 3 GHz the deviation is significant. It is natural that a transistor will have lower gain at the higher frequencies and

this were taken into account when matching the networks by prioritizing the impedances at these frequencies.

The performance of the amplifier operating at 1 dB compression is presented in chapter 4.1.3. These results show that the amplifier has good performance potentially down to 1 GHz, both in output power and efficiency when its in 1 dB compression. Having good performance at this operating point is a good indicator that the amplifier will be suitable for use when signals with high peak-to-average ratio are applied.

Tables 4.1 and 4.2 shows the simulation results achieved with test benches and the final design. In the final design both drain efficiency and PAE has decreased 10-15% compared to the test bench simulations. The output power is larger in the final design, and as a result the gain is lower.

5.2.2 Measurements

As mentioned in chapter 4.2.2, there is an uncertainty with the measurements regarding PAE and input power. As stated in equation 2.17, the gain in the PAE expression is the *power gain* of a two port network. The *power gain* is defined in equation 2.7 as the power dissipated in the load (P_L) to the power delivered to the input of a two-port network (P_{in}). The input power measured at the lab is the *transducer power gain* since the power measured by the power meter is the power available from the source (P_{avs}). To find the true P_{in}, the reflected power at the input of the DUT would have to be subtracted from P_{avs}, which could not be measured accurately at the lab. Obtaining the true P_{in} would result in a minor increase in PAE. Even though this would not have a large effect on the results it is important to clarify this uncertainty.

The small signal design of the amplifier including the bias networks and stabilization circuit proved to work as planned as no sign of oscillations occurred during the measurements. The small signal gain presented in figure 4.15 shows that the measured gain matches the simulated closely within the given bandwidth of the assignment.
In figure 4.16 it is shown that as expected, the two amplifiers have almost identical gain response. The small differences may be due to the soldering, component error margin or in the PCB milling. ”Amplifer 2” was chosen as the device to be measured while ”Amplifier 1” was used as the driver amplifier in the large signal measurements.

The bandwidth of the measured amplifier is presented in figure 4.17. The two bandwidths are defined from the points where the gain has decreased by a magnitude of 1 or 3 dB from the maximum gain in the bandwidth at 2.7 GHz. This results in a 1 dB bandwidth of 1.3 GHz and a 3 dB bandwidth of 2.57 GHz. Compared to the simulated 3 dB bandwidth in figure 4.6, the measured is significantly larger and both are well above the requirement set in the assignment text of 1.2 GHz.

Compared to the simulations, both amplifiers had a significant difference in performance from 2.9 - 3 GHz. The main reason is presented in figure 5.1 where the measured amplifiers present a mismatch in S_{11} from 2.93 - 3 GHz. This mismatch causes a change in reflected

signal at the input of the amplifier which in this case proved to have a substantial effect on the results.

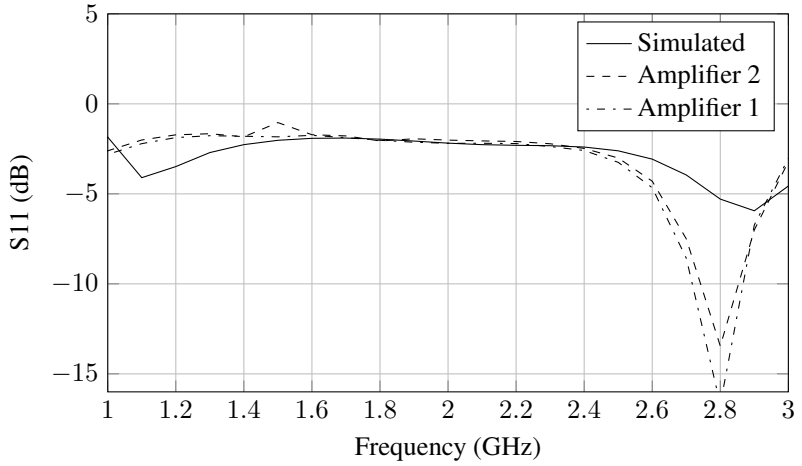


Figure 5.1: Reflection S_{11} of the measured amplifiers presenting a mismatch with simulations.

Figure 5.1 also shows that the measured response matches the simulated S_{11} down to 1.6 GHz, even though this was not considered in the design process. The mismatch is significantly affecting the performance of the amplifier from 2.9 - 3 GHz. The best operational bandwidth of the amplifier is from 1.6 - 2.8 GHz, resulting in a 200 MHz shift from the intended range. Table 4.3 gives an overview of the measurement results from 1.6 - 2.8 GHz at 1 dB compression. The results at 3 GHz is not included as the insufficient input power from the driver amplifier prevents it from reaching compression.

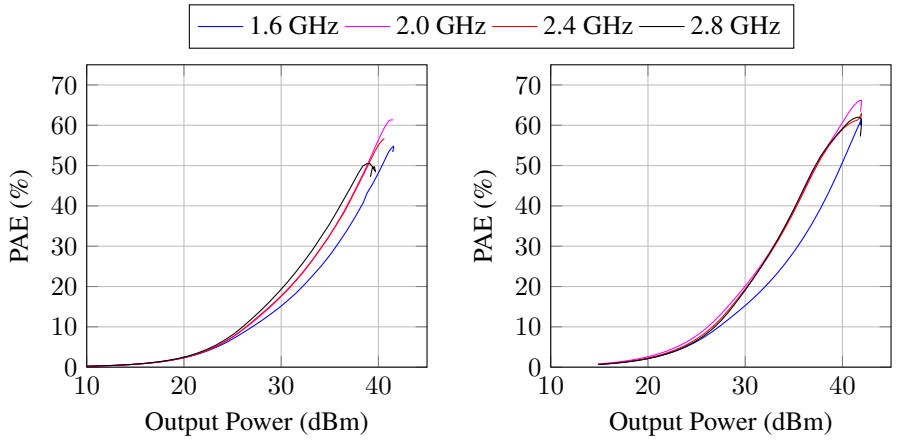
The frequency plots in figure 4.19 show that the amplifier delivers around 40 dBm of output power down to 1 GHz. Although the efficiency is poor in this range, it can still function as a good driver amplifier where delivering a steady amplified signal to a DUT is important.

The measured gain in figure 4.15 show that there is over 10 dB gain down to about 300 MHz. So the initial plan was to perform the large signal measurements from 500 MHz - 3 GHz. However, the problem was that no suitable circulator/coupler that could operate at frequencies below 1 GHz were available at the lab, so these results could not be obtained. The reason to measure the amplifier at a range this low was to see if it could produce a good output power with regards to it being used as a driver amplifier for lab measurements.

The output power plotted against frequency are presented in figure 4.19 for both amplifiers in the measurement setup. The effects of the mismatch is evident from 2.9 - 3 GHz where the power drops significantly compared to the simulations. The input levels displayed are from 21-26 dBm from the signal generator into the driver amplifier. Figure 4.20 show a comparison of output power at different frequencies which shows that the amplifier does not go far into compression at the frequencies in the middle of the bandwidth.

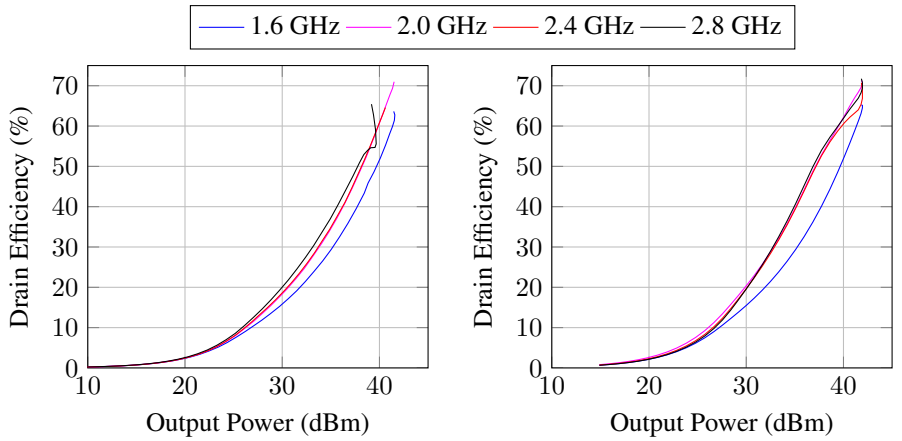
This indicates that it could be driven harder and possibly have better performance at these frequencies.

Figure 5.2 shows a comparison of the simulated and measured PAE. As discussed earlier in this chapter there is an uncertainty regarding the PAE measurement, so the measured PAE could be slightly higher. The measured PAE is 50% or higher for all frequencies which is a decrease of 5-10% from the simulations. Table 4.3 lists the results at other frequencies.



(a) Measured power added efficiency. **(b)** Simulated power added efficiency.

Figure 5.2: Comparison of the measured and simulated power added efficiency.



(a) Measured drain efficiency. **(b)** Simulated drain efficiency.

Figure 5.3: Comparison of the measured and simulated drain efficiency.

Figure 5.3 shows the measured and the simulated drain efficiency. It is 60% or higher for

all frequencies up to 2.6 GHz. At 2.8 GHz, the efficiency reaches 55% before it goes far into compression. Given the large bandwidth, these are considered to be very good results.

The transducer gain in figure 4.23 shows very similar performance as the simulations and is higher than 10 dB up to the point where the amplifier goes into compression.
The DC power consumption in figure 4.24 show that at 1.6 GHz, the amplifier uses 3-4 W more power due to the fact that it was not matched during the design process which is causing it to draw a high amount of drain current in the measurements.

The results of the two-tone measurements are presented in figure 4.25. At 1.6 GHz there is some asymmetry between the low and high side of the third order IMD around 35 dBm output power which could cause some memory effects in the amplifier. At 1.8 GHz, an IMD ”sweet spot” is present around 30 dBm output power where the response is flat which indicates an area of good signal to IMD ratio. At higher frequencies the results are good and symmetric.

5.3 Applications

There has been a surge in wireless technologies over the last decade, which has led to the crowding of existing spectrum. In order to address the resulting congestion and shortage of capacity, the cognitive radio concept has been envisioned to increase the efficiency of spectrum utilization, and improve the management, performance and coexistence of heterogeneous networks with diverse radio access technologies. Devices must be able to receive and transmit in a wide frequency range and efficiency is crucial for power consumption. The amplifier designed in this thesis should be good in applications like this, e.g. in a radio transceiver. It has high efficiency over a large bandwidth, which means it will dissipate less power than other types of power amplifiers used in radio applications.

The results proved to be best, both in efficiency and delivered power, from 1.6 - 2.8 GHz. With a little more work, this kind of amplifier could be good in military radio equipment which use frequency hopping. The amplifiers that are being used are usually tuned to have maximum efficiency at the center frequency of the band and with decreasing efficiency away from the center. The amplifier designed in this thesis have a has an average PAE over 50% through the 1.2 GHz bandwidth and would be well suited for this kind of application.

The PCB prototype made in this thesis is proven to work very well as a driver amplifier for lab testing purposes. It delivers a steady and high output power from 1 GHz up to 2.8 GHz, possibly even lower in frequency. The efficiency below 1.6 GHz is not that good, but this is not that crucial when operating as a driver.

Chapter 6

Conclusion

In this thesis a wideband class-F/F^{-1} has been designed with the main purpose to have as high efficiency as possible over a large bandwidth. The design was created using a CAD load pull technique in Agilent ADS which allows the user to perform the harmonic tuning needed to achieve Class-F operation in the amplifier. The optimal impedances found using the load pull test benches were the basis for the design of the matching networks. Since the impedances moved in a counterclockwise direction with increasing frequencies in the Smith chart, a looping method had to be utilized to try and match the impedances as closely as possible. The simulation results show that the final design had good performance and the use of this load pull technique was considered successful.

Two identical amplifiers were manufactured, one was used to amplify the output from the signal generator to get sufficient input power to the other amplifier which was the DUT. Small signal measurements were performed as well as large signal measurements with both one-tone and two-tone signals. In the large signal measurement setup, there should have been a circulator between the driver amplifier and the DUT to control the input impedance to the DUT. This was not available at the lab, so the measurements may have been affected by a small amount because of this.

The amplifier was designed to operate at 1.8 - 3 GHz with as high PAE as possible. The performance using the load pull test bench showed a drain efficiency higher than 75% while delivering an output power larger than 40 dBm throughout the 1.2 GHz bandwidth. Accurately simulating the drain voltage and drain current waveforms were not possible due to the transistor model, but from the simulation results it was concluded that the amplifier was in class-F/F^{-1} operation with harmonic tuning successfully achieved.

The simulation result of the realized amplifier showed that the average efficiency obtained was over 55% in the bandwidth while the output power was shown to be larger than 40 dBm all the way down to 1 GHz. The small signal measurements of the manufactured amplifier indicated a mismatch of the reflection S_{11} at 2.9 - 3 GHz compared to the sim-

ulations. The mismatch proved to be of significance as the measured results were poor at these frequencies.
From 1.6 - 2.8 GHz the amplifier has good performance and with an average measured PAE over 50% and drain efficiency around 60%. The output power is highest at the lower frequencies where it performs best at 41.58 dBm (14.4 W) at 1.6 GHz measured when the amplifier is operating in 1 dB compression. The performance is stable up to 2.8 GHz with a slight decrease in output power with increasing frequency. At 2.9 - 3 GHz the amplifiers performance is poor due to the mismatch at the input.

6.1 Further Work

Looking at the results it is clear that the amplifier could be matched for good efficiency even lower than 1.6 GHz. The output power is good down to 1 GHz, but since the bandwidth of the assignment started at 1.8 GHz the harmonic impedances were not matched at these frequencies and the PAE is not good. The problem with having a bandwidth so large is that the harmonic frequencies at $2f_0$ and $3f_0$ will overlap with each other and with the fundamental frequency f_0. However, because the impedances at $3f_0$ do not affect the performance as much when they are not correctly matched it should be possible to match for better efficiency at lower frequencies. As long as f_0 and $2f_0$ is matched as close as possible, the performance should be good. An effect of matching in a wider bandwidth will most likely be lower average PAE throughout the band.

Measurements with variable drain bias voltage would be of interest to perform to investigate the possibility for use in envelope tracking (ET). It is shown in [5] that the Cree transistors are suitable for envelope tracking in a RF power amplifier. In [2] a multiband envelope tracking transmitter is proposed. It has a hybrid switching amplifier connected to the drain bias of an saturated power amplifier similar to the one presented in this thesis with the same 10 W Cree amplifier, and is tested for LTE, WCDMA and m-WiMAX applications with good results.

Bibliography

[1] S.C. Cripps. *RF power amplifiers for wireless communications / Steve C. Cripps*. Boston : Artech House, 2006.

[2] J. Lee J Kim S. Jee S. Kim B. Kim J. Moon, J. Son. *A multimode/multiband envelope tracking transmitter with broadband saturated power amplifier*. In *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, pages 1–4, 2011.

[3] D. Mitrevski. *"Design and Characterization of a 6W GaN HEMT Microwave Power Amplifier with Digital Predistortion Linearization"*. Master Thesis, NTNU, March 2011.

[4] D.M. Pozar. *Microwave and RF wireless systems / David M. Pozar*. New York : Wiley, 2001.

[5] P.L Gilabert P.P. Vizarreta, G. Montoro. *Hybrid envelope amplifier for envelope tracking power amplifier transmitters*. In *Microwave Conference (EuMC), 2012 42nd European*, pages 128–131. IEEE, 2012.

[6] J. W. Milligan S. T. Sheppard R. S. Pengelly, S. M. Wood and W. L. Pribble. *A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs*. IEEE Trans. on Microwave Theory and Techniques, vol. 60, no. 6, pp. 1764-1783, June 2012.

[7] F Raab. *Class-F Power Amplifier with Maximally Flat Waveforms*. IEEE Trans. on Microwave Theory and Techniques, Vol.45, No.11, 1997.

[8] I. Rosu. *RF Power Amplifiers*. `http://www.qsl.net/va3iul/`.

[9] The University of California Santa Barbara. Harmonic balance simulation on ads. `http://www.ece.ucsb.edu/~long/ece145a/ADS_Harmonic_Balance.pdf`.

[10] Agilent Technologies, Inc. Summary of optimizers. `http://edocs.soco.agilent.com/display/support/Knowledge+Center`.

[11] Agilent Technologies, Inc. Applying Error Correction to Network Analyzer Measurements. http://cp.literature.agilent.com/litweb/pdf/5965-7709E.pdf, 2012.

[12] Cree, Inc. Cree CGH40010 ADS Model Data Sheet.

[13] Cree, Inc. Cree CGH40010 Data Sheet. http://www.cree.com/~/media/Files/Cree/RF/Data%20Sheets/CGH40010.pdf.

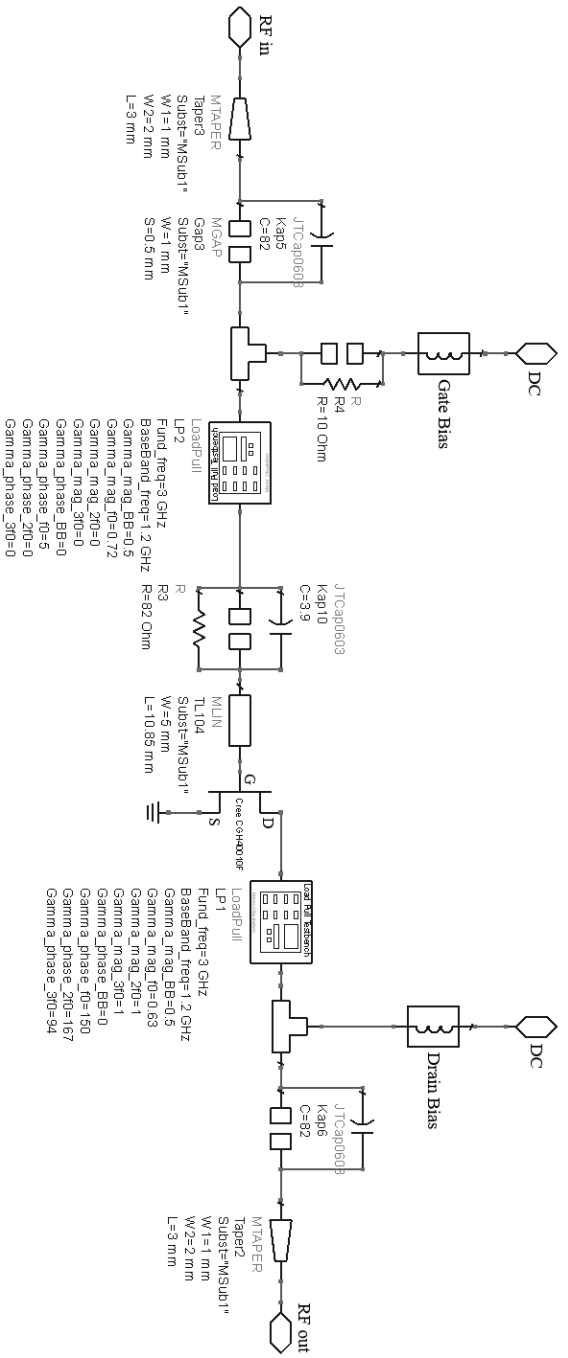
[14] John L. B Walker. *Handbook of RF and Microwave Power Amplifiers.* Cambridge University Press, 2012.

[15] M. Moore R. P. Smith S. Sheppard P. M. Chavarkar T. Wisleder U. K. Mishra Y. F. Wu, A. Saxler and P. Parikh. *"30-W/mm Gan HEMTs by Field Plate Optimization,"*. IEEE Electron Device Lett., vol. 25, no. 3, p. 117, March 2004.

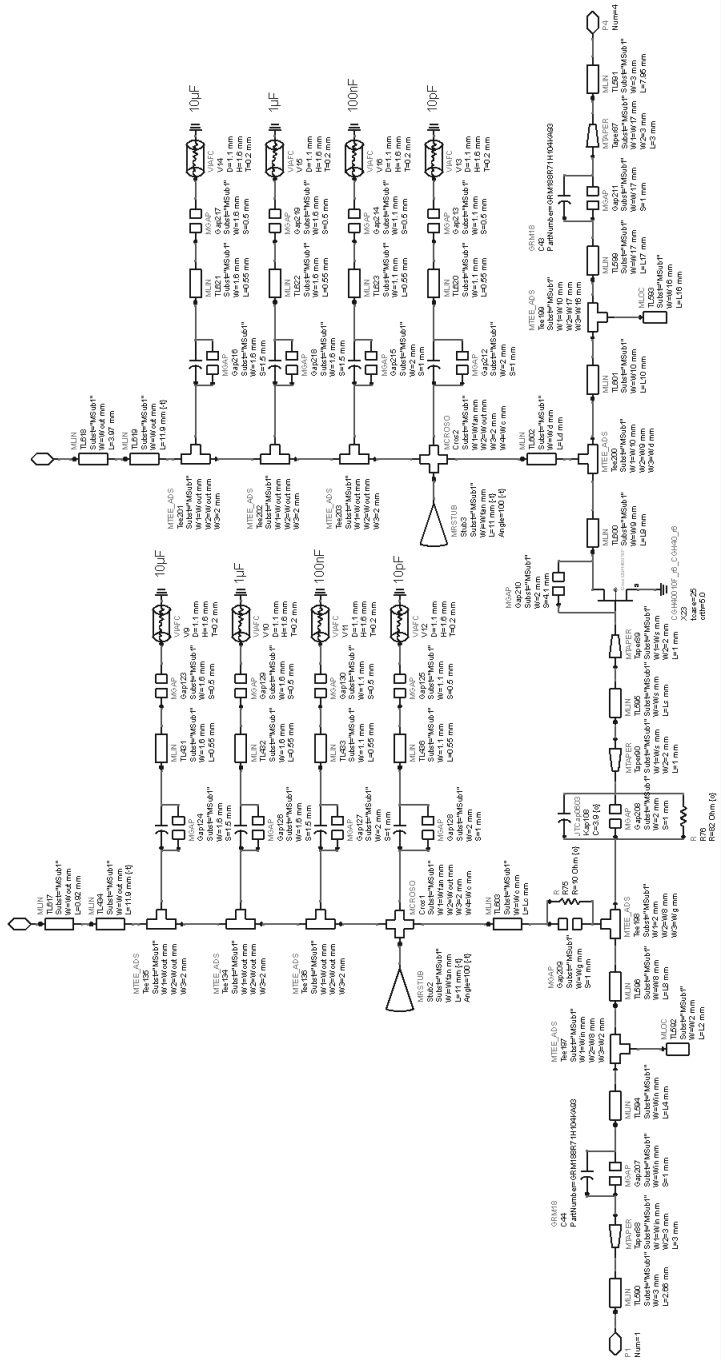
[16] B. Kim Y.Y Woo, Y. Yang. *Analysis and Experiments for High-efficiency Class-F and Inverse Class-F Power Amplifiers*. IEEE Trans. Microw. Theory Tech., vol. 54, pp. 1969–1974, May 2008.

Appendix

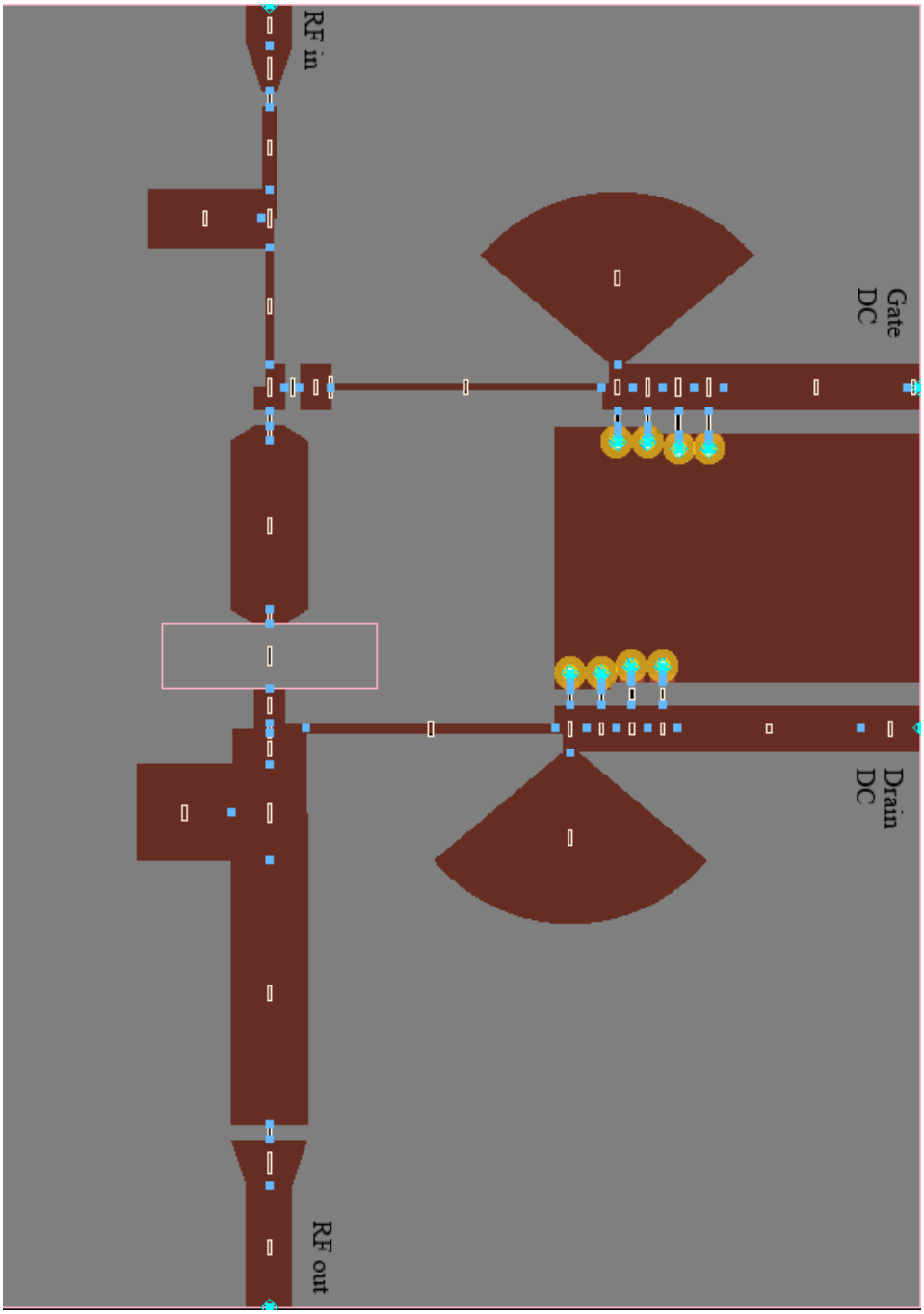
Appendix A - Test Bench Setup in Agilent ADS



Appendix B - Schematic of the Final Design



Appendix C - PCB Layout



Appendix D - Measurement Pictures

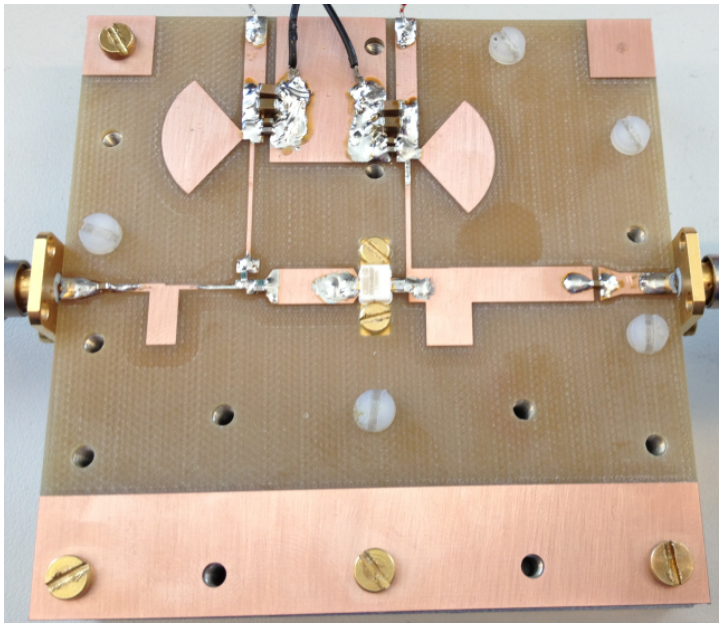


Figure D.1: Finished PCB.

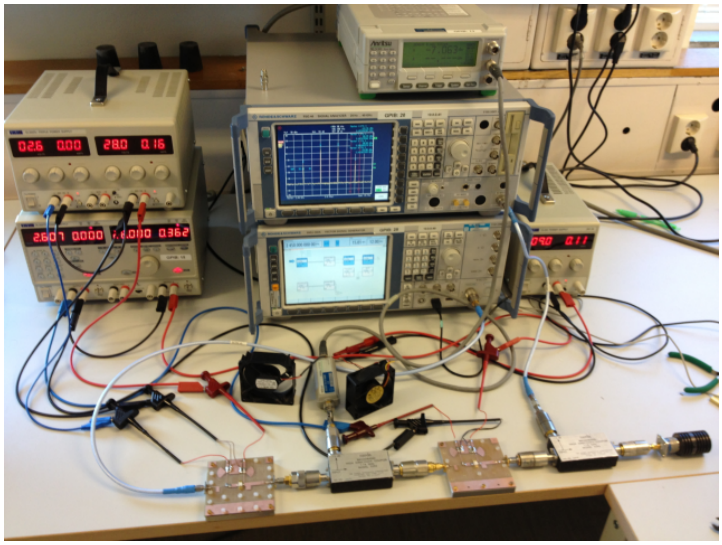


Figure D.2: Large signal and two tone measurement setup.

Appendix E - Matlab Code

Matlab script for correcting the data of the large signal measurements:

```
%clear all; close all; clc;
load InputCableLoss;    %Measured loss in the input cable.
load OutputLoss;        %Mesured loss in the from the output to analyzer.
load CouplerLoss_P1P2;  %Measured throughput loss of the coupler.
load CouplerLoss_P1P3;  %Measured loss of the coupling to the power meter.
load PA2_163mA_driverPA1_1_3GHz.mat;    %Measurement data.
%%
nP = length(pa_IP);

%The power meter reading dpa_OP is corrected by adding the loss in the
%coupling and subtracting the loss through the coupler to the input of the
%DUT.
pa2_IP = dpa_OP+ones(nP,1)*CouplerLoss_P1P3'-ones(nP,1)*CouplerLoss_P1P2';

%The output power is corrected by adding the loss in the output coupler,
%attenuator and cable to the measurement at the signal analyzer.
pa2_OP = pa_OP-ones(41,1)*OutputLoss';

%Transducer power gain of the amplifer.
pa2_gain = pa2_OP-pa2_IP;
%%
Vd = 28;

%PAE
pae_pa2 = 100*(10.^((pa2_OP-30)/10)-10.^((pa2_IP-30)/10))./(Vd*iDrain);

%Drain Efficiency
deff_pa2 = 100*(10.^((pa2_OP-30)/10)./(Vd*iDrain));

%DC Power Consumption
pdc_pa2 = Vd.*iDrain;
%%
figure
plot(pa2_OP(:,freq),pae_pa2(:,13),'b'),grid on  %1.6 GHz
hold on
plot(pa2_OP(:,17),pae_pa2(:,21),'m'),grid on    %2.0 GHz
plot(pa2_OP(:,29),pae_pa2(:,29),'r'),grid on    %2.4 GHz
plot(pa2_OP(:,37),pae_pa2(:,37),'k'),grid on    %2.8 GHz

xlabel('Output Power (dBm)')
ylabel('PAE (%)')
legend('1.6 GHz','2.0 GHz','2.4 GHz','2.8 GHz','Location','NorthEastOutside')
```

Matlab script for correcting the data of the two-tone measurements:

```
%clear all; close all; clc;
load InputCableLoss;    %Measured loss in the input cable.
load OutputLoss;        %Mesured loss in the from the output to analyzer.
load CouplerLoss_P1P2;  %Measured throughput loss of the coupler.
load CouplerLoss_P1P3;  %Measured loss of the coupling to the power meter.
load PA2_163mA_driverPA1_1_3GHz_TwoTone.mat;  %Measurement data.
%%
f = 1:0.05:3;
[~,fIdx] = arrayfun(@(x)min((RFfreq*1e-9-x).^2),f,'uni',1);
%%
nP = length(pa_IP);

%The power meter reading dpa_OP is corrected by adding the loss in the
%coupling and subtracting the loss through the coupler to the input of the
%DUT.
pa2_IP = dpa_OP+ones(nP,1)*CouplerLoss_P1P3'-ones(nP,1)*CouplerLoss_P1P2';

%The output power is corrected by adding the loss in the output coupler,
%attenuator and cable to the measurement at the signal analyzer.
pa2_OP = pa_OP-ones(41,1)*OutputLoss';

%Transducer power gain of the amplifer.
pa2_gain = pa2_OP-pa2_IP;
%%
Vd = 28;

%PAE.
pae_pa2 = 100*(10.^((pa2_OP-30)/10)-10.^((pa2_IP-30)/10))./(Vd*iDrain);

%Drain Efficiency.
deff = 100*(10.^((pa2_OP-30)/10)./(Vd*iDrain));

%Third-order IMD low side.
ThirdOrderIMD_l = pa_TOIMDpow_l-pa_OPf1;

%Third-order IMD high side.
ThirdOrderIMD_h = pa_TOIMDpow_h-pa_OPf2;
%%
freq=13; % 13 = 1.6 GHz ,21 = 2.0 GHz, 29 = 2.4 GHz, 37 = 2.8 GHz
figure
plot(pa2_OP(:,freq),ThirdOrderIMD_l(:,freq),'r'),grid on
hold on
plot(pa2_OP(:,freq),ThirdOrderIMD_h(:,freq),'b'),grid on
xlabel('Output power (dBm)')
ylabel('Third-order IMD (dBc)')
%title('Interpolated low- and high-side third-order IMD')
legend('Third Order Low','Third Order High','Location','NorthEast')
```