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En variabel bit lengde 9-bit 50MS/S SAR ADC

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Master Thesis

Circuit and system design

A Variable Bit Length 9-bit 50MS/s SAR ADC

by

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A Variable Bit Length 9-Bit 50MS/s SAR ADC

Abstract

A 9-bit 50MS/s SAR ADC with a simulated power consumption of 24.5 μW was designed for this thesis. Specifications were made for application with in-probe electronic as part of an ultrasound system. A novel switching-scheme - employing variable bit length encoding – was introduced in order to simplify successive approximation. Pre-layout results reported a FoM of just 1.37 fJ/conversion step, which is favorable to all published designs to date.

Recent technology advancements has seen the ultrasound field expanding into handheld markets [33]. More power efficient solutions, in addition to existing enhanced resolution 3-D technology both place strict requirements for analog/mixed-signal design. Composite electronics within the probe casing - allowing close-to-source signal processing - is believed to be the future of ultrasound devices. ADC designs suitable for in-probe technology require ultra low power and noise characteristics towards supporting multiple channels on a single SoC.

Excellent performance of recent SAR ADCs make them a viable alternative for in-probe technology [2, 7, 12, 4]. Work in this thesis show the flexibility of the SAR algorithm. The relatively simple implementation/decoding of the VBL approach, complimented by the accuracy dependency of the level detection range makes the ADC reconfigurable by digital signal processing.

Recent published design has reported relatively low power consumption for the comparator [15, 7]. A motivation for the thesis was to see whether multiple operated comparators could reduce power in remaining circuitry. Im-

plementation of a level-detector - supporting the VBL switching-scheme - has lead to improvements in: Power efficiency, speed and metastability-induced errors. The device consists of two comparators operated in parallel, with a relative DC-offset generated by difference in the capacitive load. Decision points of the comparators shift with DC-offset, and are atoned for a range desired by the modified SAR algorithm.
An extensive literary search of recent methodologies and results was conducted, and a summery presenting state-of-the-art designs is included with the work. An approach using no external references where chosen as a basis for the DAC design. Emphasize was made on constant common-mode voltage suitably for comparator design eliminating pre-amplifiers or buffers.
Digital logic consisting of serial connected bitslices using a novel differential approach is proposed. Level detector outputs are connected to the digital logic switching only a portion of transistors in the bitslice during conversion. Trade-off between switching activity and circuit area proves effective, with only 12.5% of overall power consumed in the digital part.
Power simulations reported the level-detector as the dominant source of consumption, thereby being subject to further optimization with regards to power. Nonetheless a proof-of-concept 8-bit ADC implementation - operated with the novel switching-scheme - produced 8.96 ENOB while dissipating less power.

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List of Abbreviations

2-D Two Dimentional

3-D Three Dimentional

AC Alternating Current

ADC Analog-to-Digital Converter

CM Common-Mode

CMOS Complementary Metal-Oxide Semiconductor

DAC Digital-to-Analog Converter

DC Direct Current

DNL Differental Nonlinearity

DSP Digital Signal Processing

DZ Deadzone

ENOB Effective Number of Bits

ERBW Effective Resolution Bandwidth

FF Fast-Fast : Used to describe process a corner in CMOS transistors

FFT Fast Fourier Transform

FoM Figure of Merit

FSR Full Scale Range

IMD Inter-Modulation Distortion

INL Integral Nonlinearity

ITRS International Technology Roadmap for Semiconductors

LSB Least Significant Bit

LVTGP Low Threshold Voltage General Purpose Transistors

MIM Metal-Insulator-Metal

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor

MSB	Most Significant Bit
NMOS	N-type Metal-Oxide Semiconductor
PMOS	P-type Metal-Oxide Semiconductor
req/ack	Request-Acknowledge
RF	Radio Frequency
RMS	Root Mean Square
S/H	Sample-and-Hold
SAR	Sucessive Approximation Register
SC	Switched-Capcitor
SFDR	Spurious-free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System on Chip
SQNR	Signal-to-Quantization-Noise Ratio
SS	Slow-Slow : Used to describe a process corner in CMOS transistors
THD	Total Harmonic Distortion
TT	Typical-Typical : Used to describe a process corner in CMOS transistors

USB Universal Serial Bus

VBL Variable Bit Length

VLC Variable Length Code

1 Introduction

The main subject of this thesis is a 9-bit, 50MS/s SAR ADC to be used in an ultrasound system. The proposed design introduce a novel variable bit length approach to analog-to-digital conversion.
In recent years SAR ADC have become increasingly popular due to their ability to adapt to the continued technology scaling. Furthermore their integration of digital logic following the trend of "digitizing the world". Increased focus on SAR ADCs has resulted in a plethora of scientific publications, rapidly advancing the field. To date the ADC achieving the best FoM use the SAR algorithm for its operation [4].
The fact that SAR ADCs achieve very good FoM at mid- to high- speeds with mid- to high- resolution make them ideal for use in Ultrasound applications. The ultrasound field is expanding with power starved handheld devices, and ultra high-resolution 3-D imaging with specification requirement that can only be met by state-of-the-art data-converter designs [33, 34].

1.1 Motivation

Recent improvements in SAR ADC performance have opened for brand new fields of use. The blooming handheld market place a constant demand for more advanced features, including additional sensors and RF receivers each requiring ADCs. This has thus far been made possible by the substantial gain to power efficiency, allowing more components to be operated using the same source of power.

In analog/mixed-signal designs ADC are often considered power hungry and noisy components. Larger systems, and/or SoCs usually have to pay special attention to ADCs with regards to placement, supply and isolation. SoCs in particular have been limited to just a few ADCs per chip, while larger systems often suffer from analog signal degradation due to extended signal path. Generally digital signals are less prone to noise, compared to their analog counterparts and for this reason it is favorable to digitize signals as close to the source as possible.
A recent survey of power consumption bounds in SAR ADCs found noise to be the limiting factor for comparator, and mismatch or noise for the DAC [12]. Generally mismatch improves with continued technology scaling as the resolution achieved by the fabrication process improves. Mismatch was found to be the limiting factor by the survey when using 065nm technology, thus still allowing improvements as $\frac{\Delta C}{C}$ and as a result feature size decrease [12, 15].
In traditional SAR ADCs the DAC dominates the power consumption. Dissipated power doubles for each additional bit of resolution. A state-of-the-art design has successfully implemented, and fabricated a SAR ADC with minimum capacitance size in the DAC as low as 400aF proving that it is possible to implement ADC almost purely limited by noise[5] .
Improvements in FoM as a function of technology scaling and new switching schemes make the SAR ADC a viable alternative when designing state-of-the-art analog/mixed-signal systems, or SoCs.

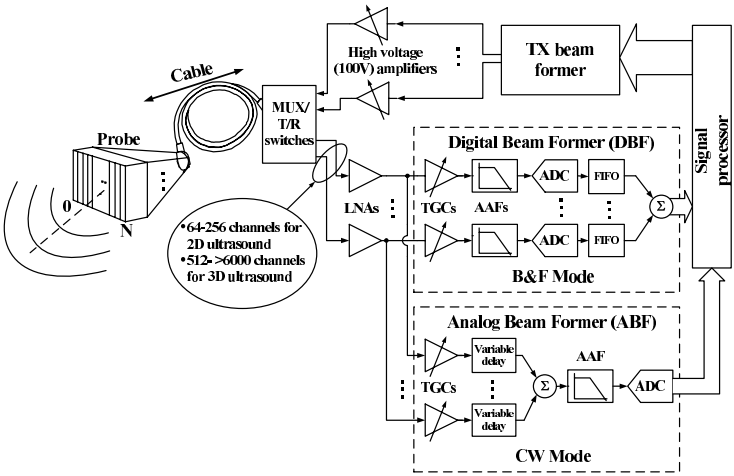


Figure 1: A typical fron-end for an ultrasound system

1.2 Ultrasound Application

The ADC implemented in this thesis is purposed for an ultrasound system. Figure 1 was originally included in the doctorial dissertation by Johnny Bjørnsen, reprinted here for illustrative purposes [14]. The typical ultrasound front-end seen use a cable from the probe to the analog and digital front-end beamformers. The channel count required is stated for 2-D and 3-D application. Generally using analog beam-forming reduce the channel count leading to increased ADC dynamic range requirements, while digital beam-forming requires one ADC per channel.

For some time it has been desirable to include more of the system inside the probe. In-probe technology will allow for better signal quality preservation by improving noise figure. Moreover digitization in-probe will allow for standardized digital communication opening for ultrasound equipment compatibility with common computer equipment, such as desktops or laptops. Such digital communication can for example be done using USB 3.0, or even wireless using standardized frequencies at 2.4 or 5.8 GHz, in combination with software.
Major challenges for in-probe technology include power efficiency and signal integrity. Isolation and minimization of interference noise limit total number of components operating in parallel. A new switch-capacitor approach to analog-beamforming shows promising results, allowing reduced channel count [26].
The medical application of the ultrasound system means there are some absolute limitations to the equipment specifications. Most notably power to the probe has an absolute limit set by heat dissipation. The probe is used against bare skin and as a result cannot become to hot. For this reason components included in the probe either have to be cooled, which result in larger probe casing, or simply dissipate less heat.

1.3 Major Contributions

This thesis has looked into alternative switching methodology, and digital coding in SAR ADCs. The main goal was to design a SAR ADC operating at 50MS/s with 9-bits of resolution achieving a FoM comparable to recent state-of-the-art converters. A novel switching scheme, and digital coding methodol-

ogy was introduced, showing results comparing favorable to all ADCs included in the extensive literary search. A list of major contributions are listed below:

- Variable bit length digital symbol coding at the ADC output, effectively limiting number of cycles needed during bit-cycling, and reducing total capacitance in the DAC by half.
- Introduce a "differential" digital logic featuring bit-slices with inherent bit-storage.
- Using three-state logic at the interface between the analog and digital part, using parallel-offset comparators, referred to as a level-detector.
- A 9-bit, 50MS/s variable bit length SAR ADC operating with a supply voltage of 0.6V. Simulated performance is

All contributions listed are based on original research proposed for this thesis. To the best of my knowledge nothing similar has been attemted in published literature.

1.4 Outline

This thesis is divided into 7 sections describing a variable bit-length SAR ADC designed for use in an ultrasound system.
Section 2 begins by describing general theory, and goes on to define terms and components specific to data converters.
Section 3 presents previous state-of-the-art designs relevant to

SAR ADCs, recounting and comparing them.
Section 4 introduce new proposed methodologies with a focus on improving upon FoM compared to previous state-of-the-art designs.
Section 5 details the implemented design, including DAC, level detector, comparator and digital logic.
Section 6 present simulated results.
Section 7 discuss the impact of design choice, simulated results, comparison to previous state-of-the-art designs and hypothesize fields of use in larger systems.
Finally the thesis is concluded based on previous discuss motivation, design strategy and results in section 8.

2 Theory

This section describes theory behind various effects and components used in data converters. Terms assosiated are listet, starting with general effects such as: Power, bandwidth, noise and SNR/SNDR. Further terms specific to data converters are discuss including: Bit-resolution, quantization noise, ENOB, INL, DNL and finally a FoM defined based on previously discuss parameters. Further general operation of components relevant to the thesis are described. Containing components are: Comparator, digital logic, sampling switch and DAC. Lastly the section is completed with a description of fundamental limitations to unit capacitance size in the DAC, with: DAC noise modeling and capacitor mismatch error.

2.1 General

General theory relevant to data-converters are presented in this section, terms are defined and described.

2.1.1 Power Consumption

Power dissipation have for some time been a major limitation in integrated circuit design. Heat dissipation, and limited battery lifetime are tightly related issues, and can only be improved by decreasing power dissipated. Heat can change properties of circuits by increasing resistance and thermal noise, in turn degenerating both bandwidth and SNDR. In some cases excessive heat dissipation can cause catastrophic failure, or damage to the

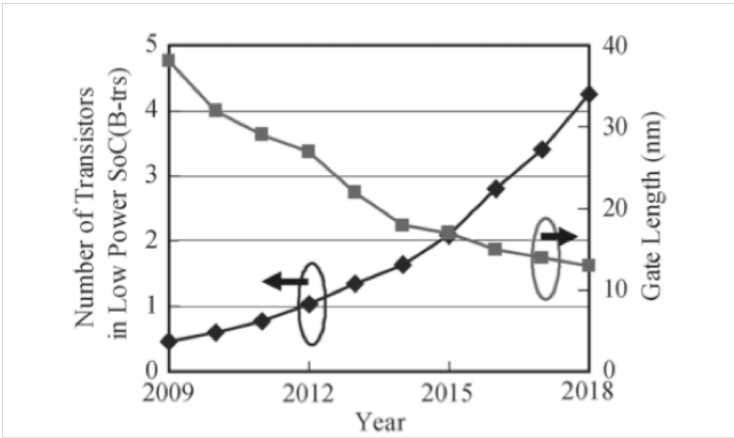


Figure 2: Technology Roadmap for number of transistors vs. gate length

circuit.
A recent technology roadmap for semiconductors released by ITRS show the relationship between number of transistors versus gate length [35]. The plot seen in figure 2 show a stangnant trend in gate length scaling, while number of transistors increase at a steady rate. A rising need for more compact designs with smaller spacing between devices, result in less space available for isolation of noise sensitive circuits.
Isolation is often required in RF and analog designs as a measure to remove unwanted signal degradation caused by $interference$ noise. Proximity of noisy circuits, such as digital logic, in layout increase power and substrate noise which may cause $interference$ to other circuits in a system if not proparly isolated. Usually seperate power nets and substrate isolation techniques are used to counter the effect, however signal degradation may still occur [18] [19].
Power noise denotes minor variations in the supply voltage caused by surges in current drawn. An example is inverters triggering on a flank, both transistors are active for a short amount of time, causing short-circuit current from supply to ground. Since power noise is caused by current, it is diminished in more power efficient circuits drawing less current.

Power Consumption in the Digital Part It is common practice to separate power dissipated in digital circuits into two categories: Static P_S and dynamic P_D power consumption. Ideal digital circuits have straight flanks, infinite impedance and no leakage current, thus dissipating no power at all. In reality

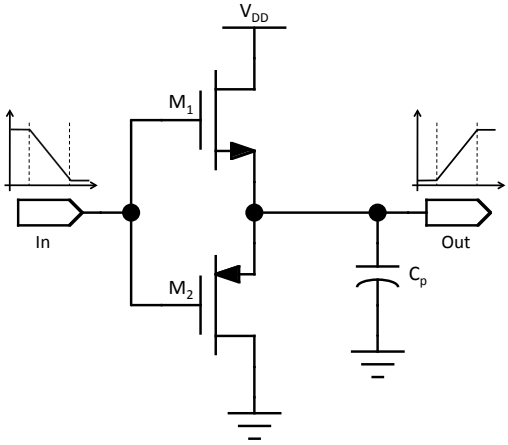


Figure 3: Transistor-level inverter with parasitic load

this is not the case; parasitic capacitances, non-ideal transistor characteristics, quiescent and leakage currents are present limiting performance and causing dissipation of power.
A simple CMOS inverter is presented in figure 3 with corresponding non-idealities included. C_p denotes the parasitic capacitance on the output of the inverter, and includes transistor channel/junction and routing capacitance.
Dissipation in digital circuits is often approximated by considering sources separately [11]:

$$P = \underbrace{P_S}_{static} + \underbrace{P_d + P_{sc}}_{dynamic} \tag{2.1}$$

Here P_{sc} is defined as short-circuit, or direct-path power consumption; a part of the dynamic consumption P_D often considered separately.
A few parameters need to be defined for static and dynamic power consumption: f, $\alpha_{0\to1}$ and t_{sc} are the clock frequency, low-high output transitions and time spent in direct-path region.
Each source of power consumption are seperable, and can be approximated by:

$$P_d = f \cdot \alpha_{0\to1} \cdot C \cdot V_{DD}^2, \quad P_{sc} = f \cdot t_{sc} \cdot I_{peak} \cdot V_{DD}, \quad P_s = I_0 \cdot V_{DD} \tag{2.2}$$

Currents I_0 and I_{peak} are the average static leakage current and the current approached when both transistors of the CMOS inverter are on, i.e. the maximum quiescent current respectively. The most efficient method for reducing overall consumption is

to lower the supply voltage V_{DD}. There are however some limitations to minimum supply voltage, perhaps most notably with regards to bandwidth. Under normal circumstances transistor in digital circuits operate with a supply voltage above threshold voltage $V_{DD} > V_{th}$, thus defining the lower limit. Sub-threshold operation has been explored successfully, however due to transistor characteristics causing severe bandwidth limitations and fluctuation in sub-threshold circuits, they are thus far not suited for mid- to high speed designs [20].
Considering threshold voltage V_{th} as the fundamental limit for supply voltage means that transistor threshold voltage must first be reduced in order to further reduce power dissipation through voltage scaling. Generally bandwidth scales with reduction of threshold voltage, however the off-resistance of devices also decrease leading to higher leakage currents I_0. High leakage currents dissipate power, and may cause loss of fidelity through the sampling switch, or in dynamic digital logic.
Assuming enough bandwidth for intended operation, a new fundamental limit arises when dynamic and static power consumption are equal $P_D = P_S$. Leakage current will increase at a progressivly higher rate when reducing V_{th}. Further voltage scaling will not affect total power consumption favorably [21].
Another method for increasing power efficiency of digital circuits is to limit switching activity during a clock-cycle. This can be done by designing more efficient logic, gating signals and clocks, combining modules and implementing dynamic logic, *see* [29] [21]. Since dynamic power dissipation usually is of higher concern than area, trade-offs can be made between switching activity and number of transistors. Combinatory logic with more

than one input should be carefully designed in order to limit or eliminate any internal switching when the output is independ of changes at the input.
The last parameter relevant to dynamic power dissipation P_D (2.2) is the capacitance C. This parameter is related to technology scaling, and decrease with the area of transistors. As an effect digital circuits should be designed with feature sized transistors to limit power consumption. Routing capacitance is becoming a major contributor to total parasitic capacitances as technology feature size decrease; layout should therefore be done with minimum routing distances.

Power Consumption in the Analog Part SAR ADCs have two main contributors to power consumed in the analog part: The DAC and the comparator. Average power dissipated in the DAC per conversion is approximated by [2]:

$$P_{DAC} = \zeta \sum_{i=1}^{N} 2^{N+1-2i}(2^i - 1)C_U V_{REF}^2 f_s \tag{2.3}$$

This equation holds for a uniformly distributed input signal between reference voltage V_{REF} and ground. The unit capacitance is denoted by C_U, f_s is the sampling frequency, N is number of bits represented in the DAC and ζ is a normalized switching-scheme dependent parameter introduced in [12]. For the traditional switching approach this parameter is $\zeta = 1$, *see* [1]. Most notably the unit capacitance C_U can be reduced for a linear power reduction in the DAC.
Unit size has a lower limits where noise, or mismatch starts to

degrade the ADC resolution. For this reason it is important to use minimum allowable to optimize power efficiency.
Another inverse propotional relationship with power is found in parameter ζ which directly affects total, and/or switched capacitance. An alternative switching-scheme must be used n order to decrease the value of ζ, and is therefore a "hot-topic" in literature [2, 4, 6, 7].
Estimating power consumption in a dynamic latched-comparator is non-trivial, and one of the main topic in [12]. Results are included here, and are based on a linear combination of power consumed in both phases of a two-phase comparator.

$$P_C = nf_s V_{DD} Q_{C,rst} + f_s V_{DD} Q_{C,reg} \tag{2.4}$$

The power is derived from the supply voltage V_{DD}, reset charge $Q_{C,rst}$ and accumulated charge during a conversion $Q_{C,reg}$. The reset charge is written as $Q_{C,rst} = C_c V_{DD}$ following the assumtion that it is mainly consumed by the capacitive load. In order to determine power consumption, the charge accumulated during a conversion must be found:

$$Q_{C,reg} = 2V_{eff} C_C (n \ln \frac{V_{DD}}{A_k V_{REF}} + \frac{n(n+1)}{2} \ln 2 + n) \tag{2.5}$$

Here V_{eff} is a defined parameter, such that $g_{m,inv} = I_D / V_{eff}$, and A_K is the gain factor from the inputs to the initial imbalance of the inverter pair. These parameters were found to have typical values ranging from $50 - 100mV$ and $0.5 - 1.8$ respectively by Dai Zhang et. al. [12]

Finally an expression for power in the dynamic latch comparator is found:

$$P_C = nf_S C_C V_{DD}^2 + 2f_s V_{DD} V_{eff} C_C (n \ln \frac{V_{DD}}{A_k V_{REF}} + \frac{n(n+1)}{2} \ln 2 + n) \tag{2.6}$$

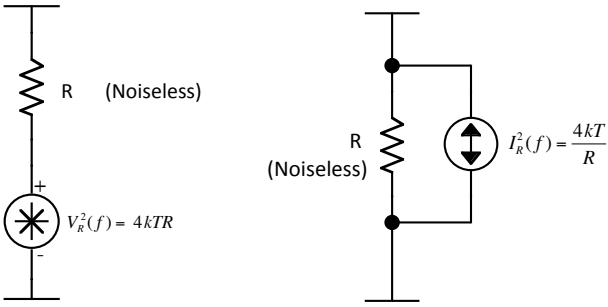
The power consumed per conversion depends on the capacitive load C_C and the supply voltage V_{DD}, and can be reduced by reducing either parameter. Noise was found to be the limiting factor for power consumption, this due to the fact that mismatch of the transistors results in mismatch in current I_D to the load C_C, which only leads to DC-offset at the output. DC-offset does not affect SNDR to the same extent as non-linearity, since it can be measured and digitally removed later. Limited dynamic range means that excessive DC-offset may cause gain compression, clipping the signal when peak values are close to rail. Such clipping cause harmonic distortion which may reduce SNDR, *see* [30].
An effective way of reducing total power consumption, without reducing power consumption per comparison is simply to reduce the number of required comparison. The relatively low static power consumption in a comparator means that there is an approximat proportional relationship between number of comparisons and power dissipated.

2.1.2 Noise

Noise in CMOS circuits contributes to signal quality degradation, and acting as a fundamental limit to performance in analog

circuits. With continued technology scaling reducing mismatch errors, approaching this limit becomes a goal when designing power-efficient nano-scale analog circuits. Noise are usually classified as $interference$ or $inherent$ depending on the source. Interference noise stems from externally generated noise, and is often classified on a system level. Two common sources are: Power noise and substrate noise. Interference noise includes a correlation factor that zeros out or add to the noise depending on phase. The proposed circuit is of relative low proportion thus only generating small amounts of interference noise. The thesis mainly focus on inherent noise, however ADCs are generally very sensitive to noise due to the usually strict dynamic-range requirements. Some thoughts should therefore be given, especially when designing layout to avoid correlated noise transferred to analog circuitery.
Inherent noise is generated in circuit elements, it is uncorrelated and include all frequencies. Major inherent noise sources are; $thermal$, $flicker$ and $shot$ noise. RMS, or power (square) spectral density values are used as a measure describing noise.

Thermal Noise Thermal noise is found in some form in all circuits, and is the major source of noise found in resistors. It appears as uniformly distributed (white) noise, and can be modeled with a noiseless resistor in series with a voltage source $V_R(f)$, or in parallel with a current source $I_R(f)$, *see* figure 4. The spectral density of thermal noise, when considering a voltage source becomes:



(a) Voltage Source (b) Current Source

Figure 4: Resistor Noise Models

$$V_R^2(f) = 4kTR \tag{2.7}$$

Here k is Boltzman's constant, T temperature in Kelvin and R the resistive value. Decreasing either resistive value or temperature will reduce thermal noise, for example [1].
Thermal noise in a MOSFET is equal to the thermal noise of a resistor if the transistor is biased in the triode region, however when the transistor is in active region the channel can no longer be considered uniform and the noise is found by integrating over small steps of the channel. A simplified model for a MOSFET bias in active region is given by:

$$I_d^2(f) = 4kT(\frac{2}{3})g_m \tag{2.8}$$

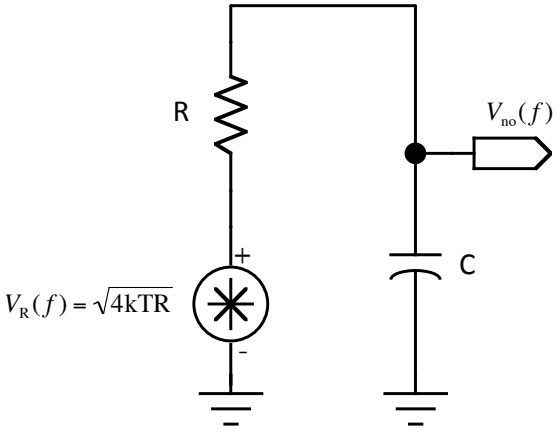


Figure 5: Noise model for a capacitor in parallel with a resistor

Capacitors and inductors does not generate any noise, however they do accumulate noise from other sources. A simple model expressing noise in a capacitor is shown in figure 5. In this model $V_{no}(f)$ is a first-order, low-pass filtered version of the input signal $V_R(f)$, resulting in a noise-bandwidth of $(\pi/2)f_0$, *see* [1]. With a white spectral density thermal noise input, the RMS value of $V_{no}(f)$ becomes:

$$V_{no(rms)}^2 = V_R^2(f)(\frac{\pi}{2})f_0 = (4kTR)(\frac{\pi}{2})(\frac{1}{2\pi RC})$$
$$V_{no(rms)}^2 = \frac{kT}{C} \tag{2.9}$$

Switch-Capacitor Circuits Noise generated in switched capacitor circuits accumulates $\frac{kT}{C}$ noise, but becomes shaped due to sampling. SC-noise can be seperated and classified as; Sampled-and-held and direct-noise, denoting noise during track- and sample-phase respectfully [9].
Noise in a typical SC-circuit is considered in order to find direct and sampled-and-held noise, figure 6. Direct noise is applied to the output for a limited period m when the switch is closed. During this period the on-resistance R_{on} accumulates thermal noise in the capacitor:

$$S_d(f) = mS(f) = \frac{4mkTR_{on}}{1 + (2\pi fT_{on})^2} \tag{2.10}$$

Here T_{on} is the time constant given by $T_{on} = R_{on}C$. Finding the RMS value by evaluating over its noise bandwidth simply

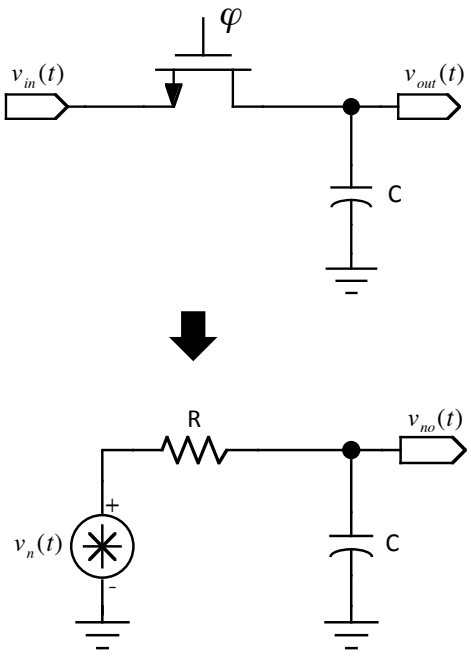


Figure 6: Model of a SC circuit

yields $V_{R,d}^2 = \frac{mkT}{C}$, implying that the direct noise act as $\frac{kT}{C}$ noise only when the switch is "on".
The sampled-and-held noise is, as the name implies, sampled at predefined intervals and held for a period of time. While the input signal is limited in frequency, the white spectral density of thermal noise contains all frequencies. Using a transistor as a switch means that the highest frequency is limited by f_0, however the thermal noise will be sampled below the nyquiest rate causing aliasing. Aliasing will in turn replicate frequencies into other frequency bands, including the baseband of the SC-circuit. An expression for the sampled-and-held noise can be found [10]:

$$S_{S/H}(f) = (1-m)^2 \frac{\sin^2[(1-m)\pi f/f_c]}{[(1-m)\pi f/f_c]^2} \frac{kT}{f_c C} \tag{2.11}$$

Because both sources of noise are uncorrelated, the PSD become:

$$\begin{aligned} S_{tot}(f) &= S_d(f) + S_{S/H}(f) = mS(f) + S_{S/H}(f) \\ S_{tot}(f) &= \frac{4kTmR_{on}}{1+(2\pi f T_{on})^2} + \frac{(1-m)^2 kT \sin^2[(1-m)\pi f/f_c]}{[(1-m)\pi f/f_c]^2} \end{aligned} \tag{2.12}$$

Finally it is worth mentioning that the ratio between sampled-and-held and direct noise show that sampled-and-held is the dominant noise source for low frequencies. The result is based on output settling within 0.1%, and a 50% duty-cycle $m = 0.5$ giving a ratio $r \geq 3.5(1/m-1)^2 > 3.5$ [10].

Flicker Noise Flicker, or $1/f$ noise is a common noise shape, and is approximated by;

$$V_n^2(f) = \frac{k_v^2}{f} \tag{2.13}$$

k_v being a constant. Dominant noise sources in MOSFETs include thermal and flicker noise. A voltage source in series with the gate models the flicker noise:

$$V_g^2(f) = \frac{K}{WLC_{ox}f} \tag{2.14}$$

The parameter K is a device characteristic-dependent constant and may vary widely for different devices in the same process [1]. The physical area of the transistor WL can be increased in order to decrease the flicker noise, which should be at or below the same value as the thermal noise floor at the design frequency.
Figure 7 illustrates a noise model for a MOSFET including both thermal and flicker noise.

2.1.3 Signal-to-Noise/Distortion Ratio

SNR/SNDR is a common characterization of signal quality in a circuit, and describes the ratio between signal and noise/distortion. It is common to state both SNR and SNDR to seperate distortion and noise. The definition of signal-to-noise ratio is:

$$SNR = 10\log[\frac{\text{signal power}}{\text{noise power}}] = 20\log[\frac{V_{x(rms)}}{V_{n(rms)}}] \tag{2.15}$$

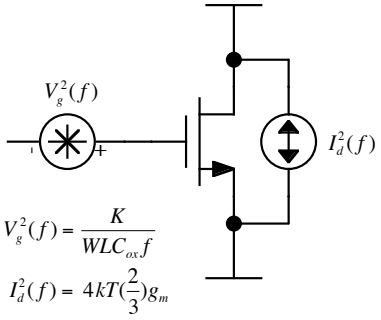


Figure 7: Noise model for a MOSFET

The values $V_{x(rms)}$ and $V_{n(rms)}$ are normalized signal and noise power based on an information signal $v_x(t)$ and a noise signal $v_n(t)$ respectively.
While noise can be shaped and/or cancelled, reducing distortion is often more complicated, and may require additional circuitry, *see* section 5.3. Distortion is defined as an input dependent non-linear effect, degrading signal quality.
Applying a sinusoid to a non-linear system generates a common form of distortion known as *harmonic* distortion. The distortion appears as power at integer multiplications of the input frequency. A common classification known as total harmonic distortion is given by the ratio between all higher order harmonics to the fundamental signal power:

$$THD = 10\log(\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}{V_f^2}) \qquad (2.16)$$

Noise power of the harmonic components are denoted $V_{h2,3,4\ldots}^2$, while power at the fundamental frequency (signal power) V_f^2, *see* [1].
Another common form of distortion is called inter-modulation distortion, and appears when a two- or multi-tone signal is applied to a non-linear system. IMD appears as frequency components close to the fundamental frequency, and thus likely in the baseband. IMD depends on the signal-power and is usually included in large-signal analysis of systems [10].

2.1.4 Scalar Quantization

Digital transmission or storage requires quantization of signals or parameters. There are two major forms of quantization; Scalar and Vector quantization. Scalar quatnization use scalar values to represent quantized signals, and is the only form relevant to this thesis.
Digital signals use quantization in order to capture quanta of an analog signal s for bit n or symbol l representation of the quantized value $\hat{s}$. Each symbol covers a finite portion, or level of the analog signal s, within a range called *quantization step−size* Δ. Total number of levels L are limited by the number of allowed, unique symbols in the code. Quantization is said to be uniform if each step size is constant, i.e. $\Delta(i) = \Delta(i+1)$. Resolution is defined as the smallest step-size covered by the quantized signal

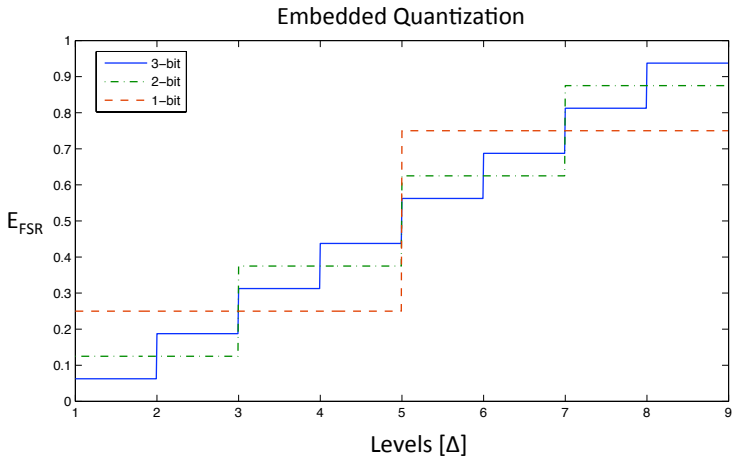


Figure 8: Embedded Quantization

$\hat{s}$, for uniform quantizers:

$$Q = \frac{E_{FSR}}{L} \tag{2.17}$$

Here E_{FSR} is the full scale range, L is the total number of levels and Q is the resolution. Bit resolution is commonly used to describe resolution of digital signals with constant bit-length code. For a digital signal with $L_{bin}(N) = 2^N$ levels, the bit resolution simply becomes $Q_{bit} = N \in [n = 0 : (N - 1)]$.

Embedded Quantization An alternative method to uniform quantization is *embedded* quantization, or *embedded* code [25]. Unlike the uniform approach, embedded quantization does not have constant step-size, and is therefore categorized as nonuniform.
Embedded code use variable bit length, with the propriety of simply discarding least significant bits. Figure 8 shows input/output relations for embedded code. The three different bit resolutions each give a different step-size, generating a subset of 16-level code. As an effect unique output-points are generated for code contained in sets of lower bit resolutions, each having an inherent available total number of levels $L_{bit}(N)$. The total number of levels for embedded code $L_{emb}(N_{emb})$ become;

$$L_{emb}(N_{emb}) = \sum_{i=1}^{N_{emb}} L_{bin}(i) = L_{bin}(N_{emb}+1) - 1 \qquad (2.18)$$

where $L_{bin}(x)$ is the total number of levels for x bits of resolution and N_{emb} is the maximum bitwidth used by the embedded code. Note that total number of levels are reduced by one compared to using constant bit representation. This is a consequence of the double step size between level 4 and 5.

2.2 Performance of Data Converters

2.2.1 Quatnization Noise

Data converters share a fundamental limit to maximum achievable SNR due to the limited bit resolution Q. The different

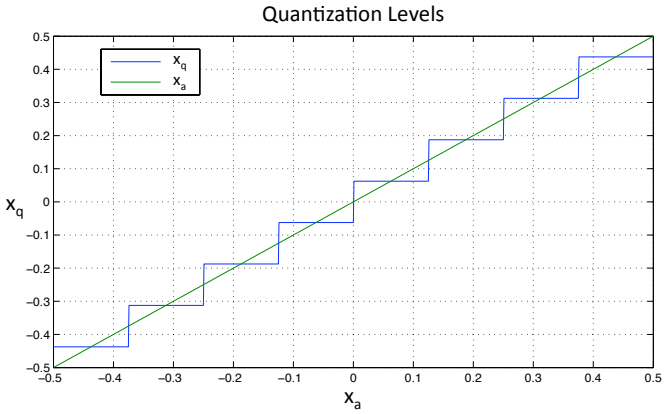


Figure 9: Quantization levels as a function of the input signal

levels of an 3-bit quantized signal x_q as a function of an analog input signal x_a is shown in figure 9. It can be shown that the minimum means square error of a uniformly distributed input signal is found with constant step-size over FSR, *see* for example [31].

The difference in value between the quantized signal x_q and the analog input x_a is called the quantization error, and can be expressed as a function of the input signal:

$$E_q(x_a) = x_a - x_q(L) \tag{2.19}$$

The resulting plot is included in figure 10 for a 3-bit example. The y-axis shows the quantization error relative to the step-size

Δ, and the x-axis shows the input signal relative to E_{FSR}. By considering the quantization error as a function of the input, it is possible to find the equivalent noise. Using either a stochastic, or deterministic method to determine the quantization noise for a uniformly quantized signal with step-size Δ, *see* [1]:

$$E_{Q(rms)} = \frac{\Delta}{\sqrt{12}} \tag{2.20}$$

The SNR of the quantized signal can be found when applied with an input knowing the power squared spectral density. For a uniform input such as a saw tooth wave:

$$\text{SNR} = 20\log(\frac{E_{in(rms)}}{E_{Q(rms)}}) = 20\log(\frac{E_{FSR}/\sqrt{12}}{\Delta/\sqrt{12}}) \tag{2.21}$$

SNR for a binary coded signal with $L_{bin}(N) = 2^N$ simply becomes:

$$\text{SNR} = 20\log 2^N = \quad 6.02N \text{ dB} \quad \text{Uniform} \tag{2.22}$$

$$\text{SNR} = 20(\log 2^N + \log\sqrt{\frac{3}{2}}) = \quad 6.02N + 1.76 \text{ dB} \quad \text{Sinusoid} \tag{2.23}$$

Here SNR is evaluated over two different input signals; a uniformly distributed and a sinusoid. Higher AC-power in the sinusoid means it achieves the best possible SNR.

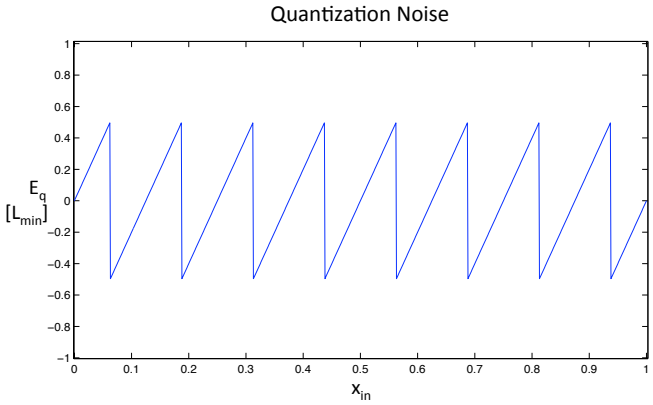


Figure 10: Quantization error for a 4-bit data converter

2.2.2 Effective Number of Bits

In data converter designs it is often important to accurately report resolution. Non-ideal converters exhibit degradation in SNR/SNDR due to noise and distortion, and as an effect can only approach the fundamental quantization noise-floor. Building on the bit dependant result in (2.22)/(2.23) a measure for effective number of bits can be found from the SNR/SNDR:

$$\text{ENOB} = \frac{\text{SNR}}{6.02} - 1.76 \tag{2.24}$$

The SNR/SNDR must be found using a sinusoid input-signal for (2.24) to be valid.

2.2.3 Bandwidth

Data converters relay on signal quantization, and are therefore limited by Nyquist's fundamental theorem for data rates [8]. The theorem states that the highest frequency $F_{MAX} = B$ contained in an analog signal x_a cannot exceed half the sampling rate F_{sample} in order to be exactly recovered from its sample values. The highest input frequency is limited by the Nyquist rate $F_N = 2B = 2F_{MAX}$.
In data converters sampling frequency is often a design variable predetermined for the field of use. It is possible to further increase the sampling frequency in order to achieve larger bandwidth. The resolution at the output of the data converter are however limited by bandwidth. Consequently it is common to plot SNDR, SFDR or SNR as a function of the input frequency, see figure 11. Effective resolution bandwidth is defined as the frequency at which the output resolution has degraded by 3 dB (0.5 ENOB) [10].
Data converters can handle input frequencies from DC to ERBW, however some data converters limit the lowest possible sampling frequency.
Minimum sampling frequency are limited by current leakage in the sampling switch and dynamic logic. The time constant of the capacitive DAC and the sampling switch are directly related to the accuracy of the ADC, therefore excessive loss of charge should be prevented. For 9-bits of resolution a loss of just 0.5% charge in the capacitors equals 1 LSB change at the outputs. To prevent loss of fidelity it is possible to increase: Capacitance of the DAC, off-resistance in the switch, and/or sampling fre-

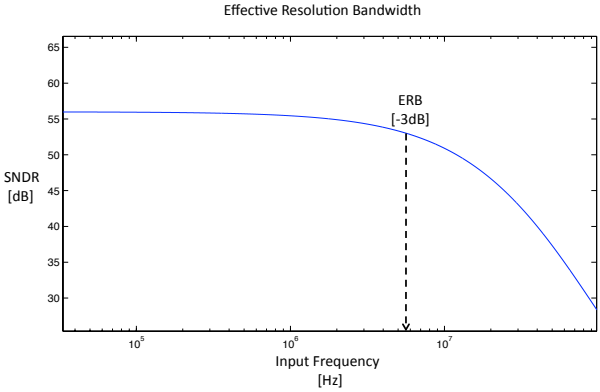


Figure 11: Effective Resolution Bandwidth

quency.
Converters relaying on dynamic logic to work will only have correct output as long as the dynamic logic maintains its value. If the signal is not latched, the limited time frame of dynamic logic affect lower possible sampling frequency. Adding latches may thus improve power efficiency by allowing sampling at a slower rate.

2.2.4 Non-Linearity

Non-linearities in data converters cause signal quality degradation, and are usually reported separately when presenting results. The two main terms used to describe non-linear behavior are integral non-linearity INL and differential non-linearity DNL. Conventionally DC-offset and gain-error are removed prior to calculating INL and DNL.
Gain error is caused when the signal gain factor A of the converter differs from 1. The output will not equal the input and an error emerge. DC-offset is the output value of the converter with common mode applied at the input, an error is caused when it is different from 0. Both gain error and DC-offset are constant and removable by digital signal processing.
INL is defined as FSR deviation from a straight line. This line can either be defined using the endpoints of the transfer response, or alternatively by using a best fit line.
DNL is defined as the variation in step-size Δ for each step in the quantization. Measured actual step-size can be used to find the deviation from Δ:

$$\Delta_{actual}(x_q) = \Delta(x_q) + DNL \tag{2.25}$$

2.2.5 Figure-of-Merit

A normalized figure-of-merit is used as a fairly good indication on the performance of ADCs. It is defined as energy per conversion-step. The formula used to calculated the FoM vary slightly with regards to sampling frequency. Lately the smallest

frequency of either ERBW or the nyquist rate are used. The formula for FoM is:

$$\text{FoM} = \frac{P_{tot}}{2^{\text{ENOB}} \cdot \min[f_s, ERBW]} \tag{2.26}$$

2.3 Comparator

Comparators are essential components in most modern ADC-designs. The latched comparator is perhaps the most popular approach, because of its low complexity design and good performance for both speed and resolutions. This section describes a typical latched comparator, along with non-ideal effects such as *kickback*, *hysterisis*, *metastability* and input-offset.

Basic principles A latched comparator requires a $track - and - latch$ stage for basic operation [1]. This stage consists of a cascode input source-follow/positive-feedback output and a reset clock. A PMOS input implementation can be seen in figure 12. Transistors M_{1-2} tracks the input signals, while the positive-feedback transistors M_{3-4} and M_{5-6} regenerate the output signals to positive rail.
Current through the source-follower transistors cause a rise in voltage at the output ports $V_{out+/-}$ gradually decreasing the resistance of the NMOS transistors M_{3-4}. The output network conforms a positive-feedback loop triggered by current through the input transistors of the source-follower. In addition, the differential output $V_{out+/-}$ limits the current into the opposing port $V_{out-/+}$, which eventually becomes latched when the

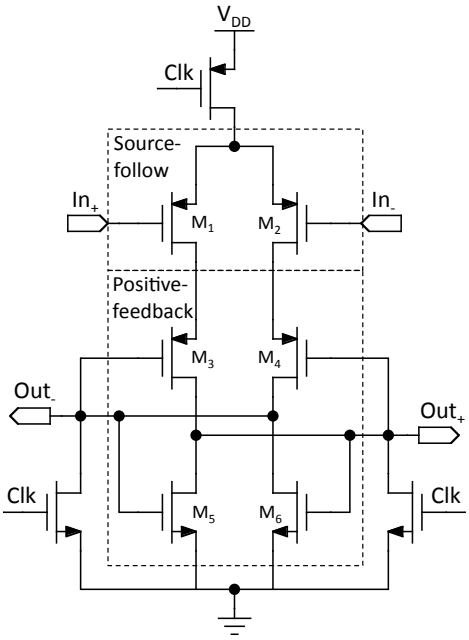


Figure 12: Track-and-latch stage

NMOS transistor starts to conduct.
The time constant for the comparator depends on the voltage difference ΔV_0 between the inputs, and can be found by analyzing a simplified circuit consisting of two back-to-back inverters [1]. Time spent regenerating the output (decision time) is given by:

$$T_{comp} = \frac{C_L}{G_M} \ln(\frac{\Delta V_{logic}}{\Delta V_0}) \tag{2.27}$$

Here ΔV_{Logic} is the voltage difference recognized as a digital signal, $\frac{C_L}{G_M}$ the time constant, and ΔV_0 initial voltage difference on the input. The result in (2.27) is derived from the solution of the input/output relationship differential equation:

$$\Delta V = \Delta V_0 \mathrm{e}^{(A_v - 1)t/\tau} \tag{2.28}$$

Metastability The necessary time for a conversion is variable with the difference in input voltage ΔV_0 (2.27). The decision time becomes large in cases with small difference in input voltage, possibly larger than allowed for the latch phase. Such cases are often referred to as *metastability*, loss of information due to indecisive result at the end of a comparison.

Kickback The term *kickback* is used about the charge transfer into or out of the input transistors during the transition time from track to latch mode. The positive-feedback transistors activate causing a transfer of charge from channel and gate when transistors turn on. Leakage to the driving circuit can cause

glitches, which may be emphasized when there are mismatch in the impedance seen looking from the inputs, see [1].

Hysteresis In order to ensure correct output from a comparator, there can be no memory of past conversion affecting the current output. Such memory may exist when nodes relevant to the output is not properly reset. If there are built up on internal nodes at the start of the regenerative latch phase, the output will be affected potentially causing a wrong decision. When the comparator exhibits such wrong decisions it is said to be in *hysteresis* [1].

Input-Offset Comparators that are not perfectly matched will have an input-offset voltage affecting output decision. Inserting constant offset at the input ($\Delta V_0 + k$) in (2.28) the output ΔV decision point will be moved by k. A simplified approximation to the input offset based on mismatch in the input transistors and the regenerative output transistors was proposed in [17]:

$$V_{OSM} = \Delta V_{TH} + \frac{1}{2}(\frac{\Delta W}{W} - \frac{\Delta L}{L})(V_{GS} - V_{TH}) + \frac{\Delta Q}{C_l} \quad (2.29)$$

where $\Delta W/W$ and $\Delta L/L$ are relative dimension mismatch, ΔV_{TH} and V_{TH} are the standard deviation and mean of the threshold voltage, ΔQ is the charge injection mismatch between input transistors and C_l is the capacitive load. Clearly any difference in the capacitive load will further affect offset by affecting the time constant τ of the regenerative output.

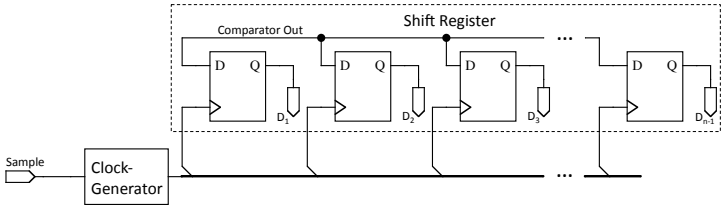


Figure 13: Block diagram of SAR ADC digital logic

2.4 Digital Logic

In recent literature asynchronous logic has been the common choice when designing SAR ADCs [7, 4]. Sequential bit determination requires oversampling the clock at a rate greater, or equal to the number of bits to be determined. The need for such a fast clock by synchronous logic means extra external circuitry that may not be readily available.
Asynchronous circuits are generally larger in area, and tend to be less energy efficient. However in SAR ADC do not require any external circuits that may well dissipate more power than the ADC itself. Moreover, asynchronous circuits are adaptable when designing application specific digital logic in that they can be designed almost entirely dynamic and with a request acknowledge procedure, eliminating otherwise essential delay generating circuits, *see* for example [32]. Furthermore the circuit could benefit from increased speed performance when handling components with variable time constants, such as comparator metastability.

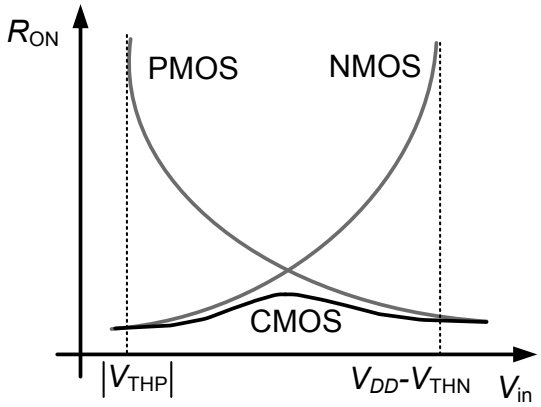


Figure 14: On-resistance for MOS-transistors

Generally a clock generator and a shift register are needed to control the analog circuit and store the output bits. A block diagram representation consisting of a shift-register and a clock generator can be seen in figure 13. The output of the comparator is stored on the flip-flops, while the clock generator clocks the shift-register and the analog circuits.

2.5 Sampling Switch

In order to minimize distortion in the ADC, a well-designed sampling switch is required. Such a switch needs to be able to track the input signal over its full range, due to factors like variable

on-resistance, non-linearity in junction-capacitances and channel leakage.
A characteristic of on-resistance R_{on} for select transistors; $NMOS$, $PMOS$ and $CMOS$ is presented in figure 14. As becomes apparent, $CMOS$ transistors exhibits overall lowest on-resistance in the range $< |V_{THP}|, V_{DD} - V_{THN} >$, while $NMOS$ and $PMOS$ transistors have their lowest value closer to the threshold voltages V_{TH} of their respective counter-parts.
In applications where peak-to-peak voltage is significantly lower than the supply voltage, single NMOS, or PMOS transistors can be utilized without worrying about increasing on-resistance. Transmission gates using CMOS-transistors can be used for input signals with larger magnitude, but require an inverted clock signal leading to extra circuitry. Non-linearity in the junctions and channel parasitic capacitances leads to distortion of the sampled signal when the capacitive value changes as a function of the input-signal. For switched capacitor circuits with sample capacitance close in value to the parasitic capacitance this distortion becomes large. Moreover, this effect is not nullified in transmission gates. A common method for operating a single NMOS transistor over the full signal range rail-to-rail is to *bootstrap*. The methodology ensures that on-resistance is kept low for all input-values, while minimizing distortion. The sampling clock is a function of the input signal with a constant offset, in some cases the sampling clock may exceed the supply voltage in magnitude. Operating transistors relayable becomes a consern when the sampling clock becomes larger than allowable by technology processes [24].

2.6 Digital-to-Analog Converter

SAR ADCs requires a DAC generating voltages necessary by the algorithmic operation. Conventional DACs consists of a binary weight capacitor array, with switches at the bottom plate of the capacitors, figure 15. Sampling of the input signal during the S/H phase is also done on the bottom plate, with a two-way switch between the input and a reference voltage. During the bit-cycle phase bottom plates of the capacitors are sequentially connected to ground. The capacitor sizes are determined based on a unit size u capacitance used to represent the least significant bit. In the 4-bit example represented by C_1, figure 15. Additional capacitors are used to represent more significant bits, and are sized based on the value of the respective bit:

$$C_{Bn} = 2^{n-1} \cdot u, \quad n = 1, 2, \ldots \tag{2.30}$$

In order to calibrate for the offset generated by the binary code, an additional unit sized capacitor is added. This capacitor samples the input, but is not switched during bit cycling. The total capacitance of the unipolar approach is given by:

$$C_{tot}(N) = u \sum_{i=1}^{N} C_{Bi} + u \tag{2.31}$$

2.7 DAC Noise Modeling

Noise is an important factor to consider when designing ADC limited by the strict SNR requirements. All the common noise

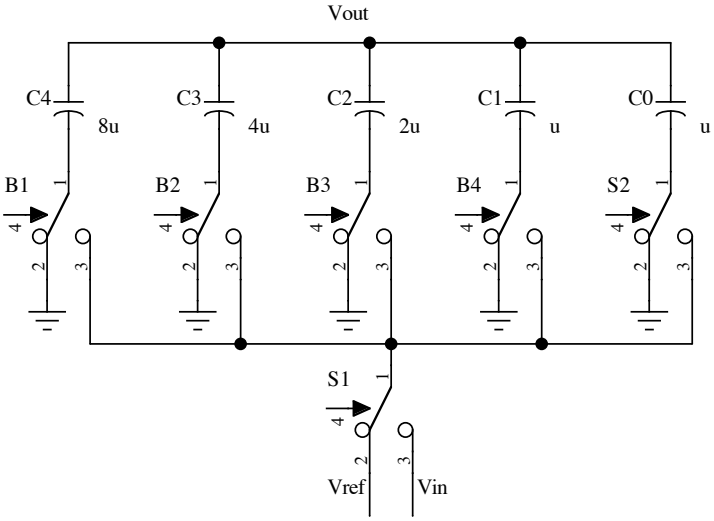


Figure 15: A unipolar capacitive charge-redistribution DAC

sources, such as shot, thermal and flicker noise must be acknowledged in order to meet the above-mentioned criteria. Noise modeled in this section is represented by its RMS-value, and are either spectral or root-spectral density in the frequency domain. The inherent noise sources are assumed to be white noise.
The most important component when modeling noise in the DAC is the capacitor, which in itself is noiseless, but accumulate noise on the form of $\frac{kT}{C}$ [1]. A simplified switch capacitor

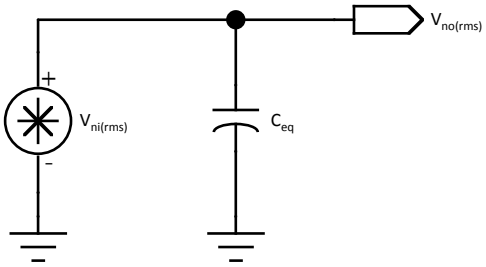


Figure 16: Equivalen capacitance seen from the samplin switch

noise model is used to model noise in the DAC, *see* figure **??**. The output noise $V_{no(rms)}$ can be calculated as a linear combination of all noise referred to the output. The general uncorrelated case:

$$V_{no(rms)}^2 = V_{n1(rms)}^2 + V_{n2(rms)}^2 \tag{2.32}$$

Noise sampled on the capacitor C_{tot} follows the same principals as the reference voltage V_{ref} in serie with a noiseless transistor when looking from the output. The square spectral density noise output voltage at $V_{no(rms)}$ becomes:

$$V_{no(rms)} = \sqrt{\frac{kT}{C_{tot}}} \tag{2.33}$$

By substituting capacitors with a standarized unity capacitance u, it is possible to find the minimum allowable unit capacitance in order to achieve dynamic-range requirements for the ADC. These requirements are met when the noise power is equal to the quantization error of the ADC, resulting in a 3dB decrease to SNR [12].

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.34}$$

Substituting (2.34) into (2.32) results in:

$$C_u = \frac{12 \cdot kT}{2^N \cdot V_{LSB}^2} \tag{2.35}$$

Since inherent noise can be added together according to (2.32), it is important to remember to include other sources of

noise, such as shot and flicker noise when finding the minimum capacitor size u. Generally the biggest noise contributor should be prioritized when minimizing noise, since it has the most effect on overall noise. However if other sources are comparable in spectral density these should either be minimized individually, or unit capacitor size could be made larger in order to meet noise requirements.

2.8 Capacitor Mismatch Error

A survey of power consumption bounds in SAR ADCs identified two main fundamental limits to unit capacitance size for the DAC: The thermal noise floor and the error caused by mismatch [12]. Mismatch errors are caused by irregularities in size and shape on the die, and are linked to the fabrication process and achievable physical resolution of a technology.
In order to determin the effects of mismatch it must be modeled. This can be done by considering a unit capacitance C_u and finding the DNL and INL standard deviation. DNL have the largest σ_{MAX} and will thus be used to determine C_u. A term expressing the standard deviation of the worst-case DNL was found in [13], following the analysis of [27]:

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1}\frac{\sigma_u}{C_u}LSB \tag{2.36}$$

A model for the mismatch of the capacitance valid for a typical MIM capacitor;

$$\sigma(\frac{\Delta C}{C}) = \frac{K_\sigma}{\sqrt{A}} \tag{2.37}$$

$$C = K_C \cdot A \tag{2.38}$$

where $\sigma(\Delta C/C)$ is the standard deviation of the capacitor mismatch, K_σ is the matching coefficient, A is the capacitor area and K_C is the capacitor density parameter. An expression for the lower bound for mismatched-limited unit capacitor was found in [13]. DNL standar deviation was chosen to fulfill $3\sigma_{DNL,MAX} < 1/2LSB$ for acceptable yields, leading to:

$$C_U = 18 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_C \tag{2.39}$$

This expression holds for a single-ended approach to the SAR ADC, for differential the unit capacitance can be reduced by half and still satisfy the requirements.

3 Previous State-of-the-Art

This section will attempt to give an overview of previous state-of-the-art SAR ADC designs. Achieved FoM will be a general pinpoint for state-of-the-art designs. Nonetheless methodologies improving on previously discuss parameters relevant to ADC performance will also be considered regardless of reported FoM.

3.1 Top-Plate Sampling

A recent paper suggests using inverters instead of switches for the bit-cycle phase [7]. This approach requires a reference voltage capable of driving the inverters, and is usually operated rail-to-rail. By eliminating the need for complicated switches, like transmission gates, and a separate generated reference voltage, this method has proven more power efficient. Noise generated in the supply net will be added to the DAC reference, and thus making the ADC more sensitive to noise from both external and internal sources. Extra care must be taken when designing the ADC to avoid signal quality degradation due to power noise. A 4-bit example is shown in figure 17, the sampling switch has been moved, and the DAC samples input on the top-plates. The bottom-plates of the capacitors are on separate nets during sampling, unlike the bottom-plate sampling of the unipolar case, this makes the DAC more sensitive to mismatch between parasitic capacitances. In the unipolar case the parasitic capacitances are connected together during sampling, and shared for both V_{in} and V_{ref} [1]. Figure 18 depicts an equivalent circuit for a capacitor including parasitic capacitances caused by wiring and fringe effects. The parasitics on the top-plate are connected in series and does not increase nonlinearities. Separate nets at the bottom-plate are sensitive to parasitic capacitance, however voltages at these nets referred to the DAC output becomes small. Parasitic effects causing incorrect settling of the DAC output voltage can be countered in layout by routing with parasitic capacitance in mind. Matching parasitic capacitances can help improve signal quality.

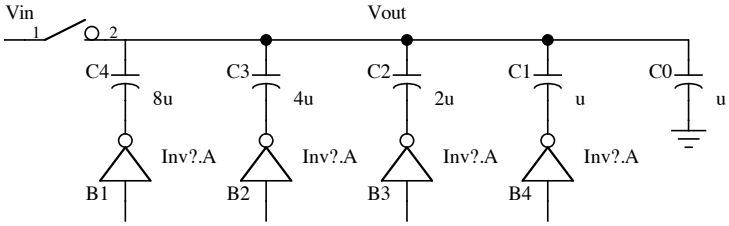


Figure 17: A single-ended charge-redistribution DAC with inverters

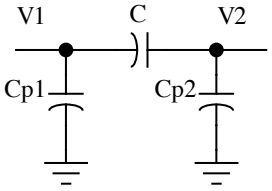


Figure 18: An equivalent circuit for a capacitor with parasitic capacitances

3.2 Differential input

A differential adaptation to the binary weight capacitor array is shown in figure 19 [7, 4, 2, 12] . Using differential inputs has been popular in late literature. The reason for this is mainly because differential inputs allow for MSB decision by the comparator without any additional switching. Inherited passive amplification by 2 is also used to decrease the accuracy requirement for the comparator when V_{LSB} is increased. V_{LSB} is related to the FSR, and V_{ref}:

$$V_{LSB}(N) = \frac{V_{refp} - V_{refn}}{FSR(N)} \tag{3.1}$$

The binary weight concept still applies to the capacitors of the differential DAC. The MSB capacitor of the single-ended version can be removed since MSB is found directly from the inputs. The 4-bit example in figure 19 shows the reduced capacitor sizes, the total capacitance can be found by applying (2.31) to both sides of the capacitor array:

$$C_{tot,diff}(N) = C_{totp}(N-1)+C_{totn}(N-1) = 2 \cdot u \cdot \sum_{i=1}^{N-1} C_{Bi}+2u = C_{tot}(N) \tag{3.2}$$

The total capacitance of the differential approach is equal to the total capacitance of the single-ended case, however power efficiency is increased due to the smaller size of the switched capacitors.

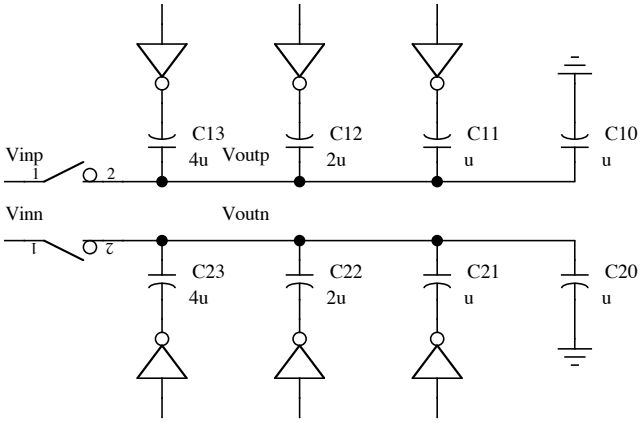


Figure 19: Differential Charge-Redistrubution DAC

3.3 Monotonic Decreasing Switching Scheme

A recent popular switching scheme employing differential DAC input/output use a monotonic increasing/decreasing output $V_{DAC,out}$ [2, 4, 22]. It works by pre-charging the binary-weight capacitances to $V_{Ref,p/n}$ during the track-phase, then cycling bits by charging/discharging either the positive or negative half of the DAC based on the comparator result. The resulting DAC outputs will monotonically decrease or increase based on nodes being charged or discharged respectively. The common-mode voltage V_{CM} of the output will also be affected, as illustrated in figure 21a. Having variable common-mode can complicated comparator design, as it may be sensitive to common-mode changes at its inputs. This often leads to the necessity of a buffer, or pre-amplifier in order to achieve high enough bit resolution [2].

3.4 Merged Capacitor Switching

A method for eliminating the need for external common-mode reference, while keeping common-mode level constant, is using merged capacitor switching [23]. Figure 20 demonstrates the principles behind the merged capacitor, as well as switching during the bit-cycle phase. Unit size of the capacitor is divided between two separate capacitors with the top-plate connected in parallel, and bottom-plate connected to separate nets. The initial state of the capacitors are shown in the top schematic of figure 20. During bit-cycling the capacitors are switched to one of two states (a, b). In state a, V_{refp} at the bottom plat of capacitor C_p is switch to V_{refn} changing the voltage potential at

V_{out} by a positive amount (3.3). In the alternative state b, the bottom-plate of capacitor C_n is switched from V_{refn} to V_{refp} causing a negative voltage shift. The potential change is given by:

$$\Delta V_{out,n}(N) = \frac{2^{n-1}}{FSR(N)} \cdot (V_{refp} - V_{refn}) = 2^{n-1} \cdot V_{LSB}(N), \quad n \leq N \tag{3.3}$$

Notably merged capacitors have three separate states. This entails that all states of figure 20 are unique, unlike traditional or monotonic decreasing where only two states are unique. Supporting three states requires 2-bit control signals, however splitting capacitors allows for smaller physical size and capacitive value.

4 Proposed

This section presents proposed methodology for the thesis, including a novel switching-scheme and digital bitslice design. The proposed methodology builds on previous state-of-the-art, but also introduces brand new procedures and circuit compositions in an attempt to improve stat-of-the-art design methodologies.

4.1 Stable Common-mode Switching Scheme

A proposed switching scheme with constant common mode, using Merged capacitors, are illustrated in figure 22.

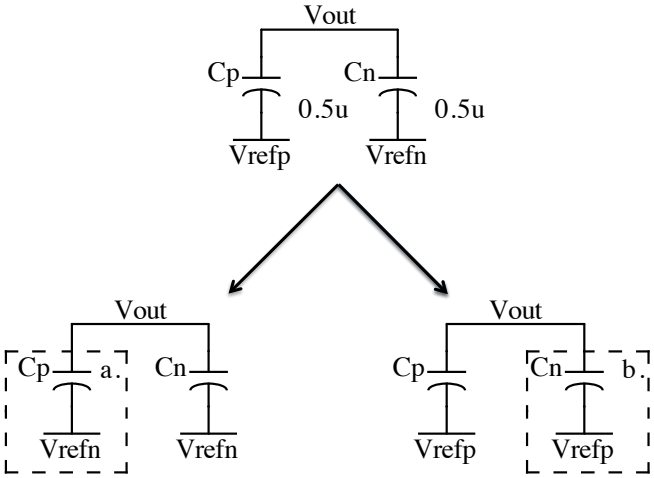


Figure 20: Split potential capacitors

Comparators typically require pre-amplifiers, or otherwise increased complex solutions to meet resolution specifications when signals applied with variation in common-mode. A symmetrical switching scheme is proposed building on the inverter based switching, and merged capacitor switching approach [7, 23]. This switching scheme eliminating any major variation in common mode, without requiring external references, figure 21b. Following the principals of differential signals both sides of the differential DAC is switched in every step of the bit-cycling phase, guaranteeing a stable common-mode voltage. DAC outputs gives the common-mode voltage:

$$V_{CM}(N) = \frac{V_{DACoutp}(N) - V_{DACoutn}(N)}{2} \tag{4.1}$$

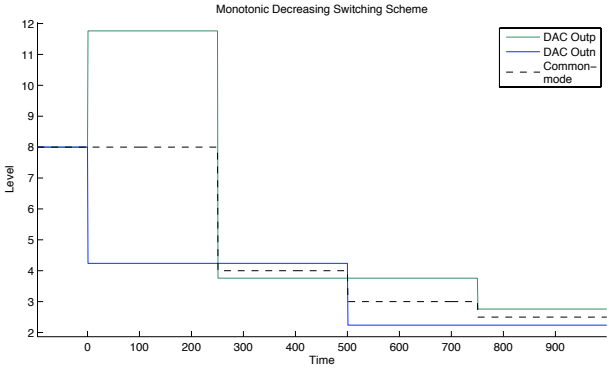
Finding a value for V_{DACout} using split potential capactitors at a point during bit-cycle:

$$V_{DACout,n}(N) = V_{in} + \sum_{N}^{i=1} \Delta V_{out,i} \cdot (b_{p,i} - b_{n,i}), \quad b_{p,i} = 0,1, \quad b_{n,i} = 0,1 \tag{4.2}$$

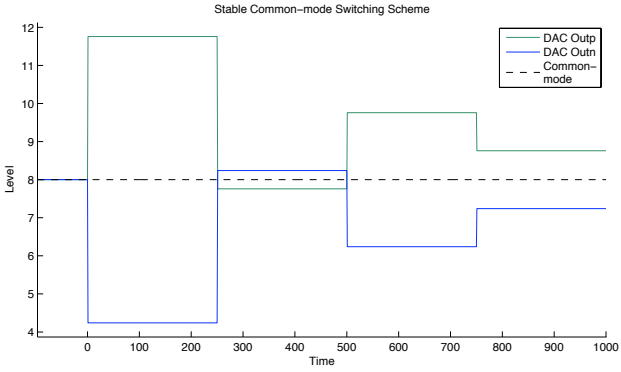
Where V_{in} is the input during sampling, $\Delta V_{out,n}$ given by (3.3), and b_n is one bit of the digital output word B. Possible states of b_n is given by:

$$b_{p,n} = \begin{cases} b_{n,n} = 1 & i > n \\ b_{n,n} & i \leq n \end{cases} \tag{4.3}$$

Recognizing that (4.2) is separable by the linear relationship of each steps in the bit-cycle. It is possible to find the common-



(a) Monotonic Decreasing Common-mode waveform



(b) Constant Common-mode waveform

Figure 21: Switchin Schemes

mode at any point by substituting (4.2) into (4.1). A proof can be written:

Proof.

$$\text{if } V_{CM,n} = V_{CM}(N = n) - (V_{CM}(N = (n-1)) + (V_{CM}(N = N) - V_{CM}(N = n))) \tag{4.4a}$$

$$\text{then } V_{CM}(N) = V_{CM,0} + V_{CM,1} + \ldots + V_{CM,N-1} \tag{4.4b}$$

$$V_{CM,0} = \frac{(V_{inp} - V_{inn})}{2} = \frac{V_{refinp} - V_{refinn}}{2} \tag{4.4c}$$

$$V_{CM,n+1} = \frac{\Delta V_{out.i} \cdot (B_{p,n} - B_{n,n}) - \Delta V_{out,i} \cdot (B_{p,n} - B_{n,n})}{2} = 0 \tag{4.4d}$$

$$V_{CM}(N) = V_{CM}(N+1) = V_{CM,0} = \frac{V_{refinp} - V_{refinn}}{2} \tag{4.4e}$$

□

Equality holds in (4.4c) because of the differential properties of V_{in}. Although any value for V_{refinp} and V_{refinn} can be chosen in theory, there is a potential gain in choosing the reference voltages of the DAC in order to prevent any unnecessary loss of charge in capacitors during bit-cycling.

The 4-bit representation of the stable common-mode implementation seen in figure 22 use merged capacitors at the differential ends of the DAC. A completely symmetrical DAC only using mered capacitors will have no systematic offset in common-mode. Splitting capacitors will affect the size of the capacitors,

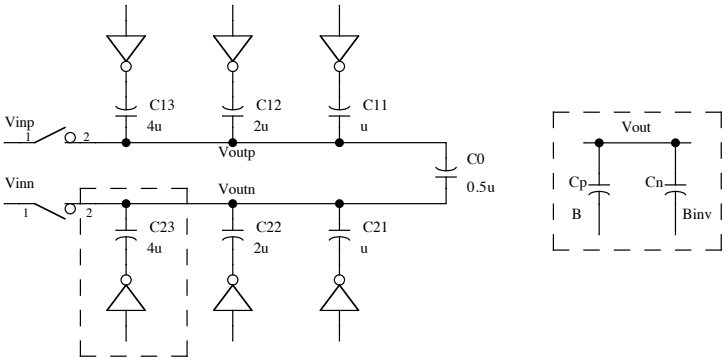


Figure 22: Differential split potential capacitor array

and if minimum achievable unit size are being used both LSB merged capacitors are limited to $C >= u$:

$$C_{Bn,split} = 2^n \cdot u \tag{4.5}$$

Having a differential output makes it possible to connect a capacitor between the outputs, effectively doubling its capacitive value in accordance with Millers theorem [1]. The total capacitance of the DAC becomes:

$$C_{tot,split}(N) = 2 \cdot u \cdot \sum_{i=1}^{N-1} C_{Bi,split} + u = 2 \cdot C_{tot} - u \tag{4.6}$$

The total capacitance of $C_{tot,split}$ is almost twice as large as

alternative switching schemes. Compared to monotonic decreasing switching, constant common-mode switching charge $C_{Bn,split} = 2C_{Bn}$ for each step during bit-cycling. This constitutes an *increase* in power dissipation for the DAC, which could be a substantial part of total power dissipated.
The total capacitance $C_{split,tot}(N)$ can be reduced by adding an asymmetrical step at LSB, figure 23 *b*. Using a single capacitor, instead of a merged capacitor, at C_1 affects common-mode reducing total capacitance. The following bit will consists of a merged capacitor using unit sizes equal to C_{B2} (2.30). The same holds for every additional bit, and the capacitive value of the binary weight capacitors becomes:

$$C_{Bn,split\ asymmetrical\ LSB} = \frac{1}{2}C_{Bn,split} = C_{Bn} \tag{4.7}$$

Substituting this into (4.6):

$$C_{tot,split\ asymmetrical\ LSB}(N) = C_{tot}(N) - \frac{3u}{2} \tag{4.8}$$

Equality holds in (4.8), however depending on the unit capacitance size, $\frac{u}{2}$ will not be achievable in cases where unit size approach feature size of the technology. In these cases the total capacitance simple become $C_{tot,split\ asymmetrical\ LSB}(N) = C_{tot}(N)$ by substituting the offset correcting capacitor C_0 with the equivalent capacitors C_{10} and C_{20} of figure 19.
The effects on common-mode by using asymmetrical step at LSB can be seen in the waveform of figure 26a. Only one of the DAC

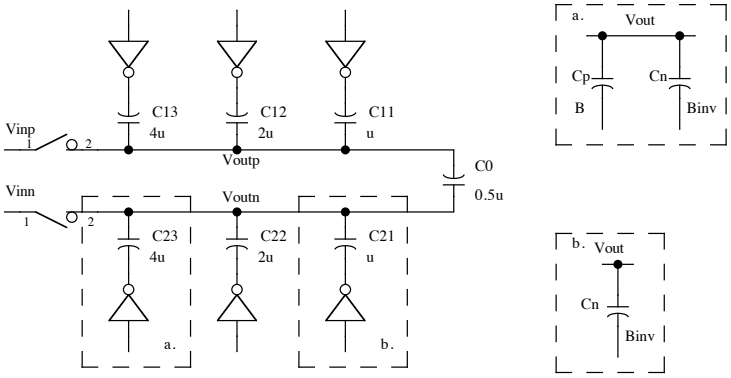


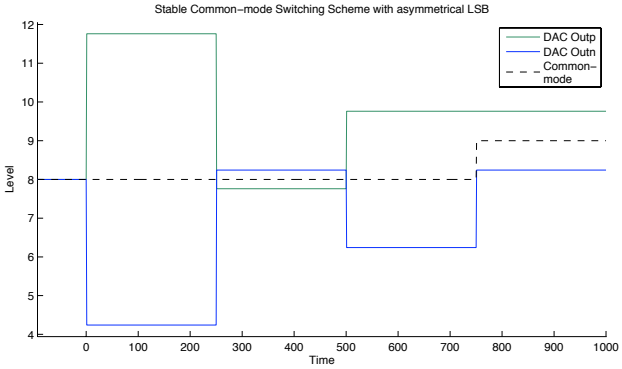
Figure 23: Differential split potential capacitor array with asymmetrical LSB

outputs are switched, and common-mode is affected according to (4.1). The change in voltage depends on the bit resolution of the DAC, and can be found using:

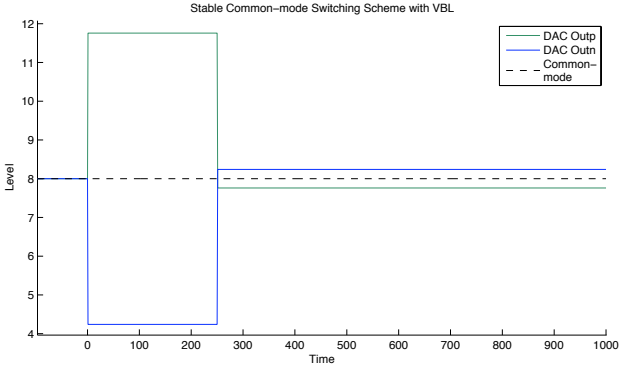
$$\Delta V_{CM}(N) = \frac{\Delta V_{out,1}(N)}{2} = \frac{1}{2} V_{LSB} \tag{4.9}$$

4.2 Variable Bit Length

Charging binary weight capacitances is one of the major contributors to power dissipation in SAR ADCs (2.30). Several approaches have been suggested to reduce the required capacitance by introducing new, or modified coding algorithms [3, 16].



(a) Constant Common-mode waveform with asymmetrical LSB



(b) Variable bit length waveform

Figure 24: Switchin Schemes

Section 2.1.4 talks about embedded quantization and its application in data compression. Embedded quantization allows for higher resolution by increasing number of decision levels (2.18) for a given number of bits, making it possible to meet higher resolution specifications with less number of bits. For SAR ADC this is favorable with regards to: area, speed and power efficiency! The novel switching methodology introduced in this thesis utilize embedded quantization and is described below.

The effects of the added decision levels in VBL code can be translated to the analog domain by considering the three-state constant common-mode switching scheme. The different voltage levels in the DAC relates to the digital words B_p, B_n and the change in voltage for a given bit $\Delta V_{out,n}(N)$, referenced to the differential input V_{in}. The voltage level on the output of the DAC $V_{DACout,n}(N)$ at any time during the bit-cycle is a sum of $\Delta V_{out,n}$ given by (4.2). Factoring in the fact that $\Delta V_{out,n}(N) = \frac{1}{2}\Delta Vout, n+1(N)$ it is possible to prove that;

$$V_{DACout,n}(N) \neq V_{DACout,r}(R), \tag{4.10}$$
$$N = 0, 1, \ldots,\ R = 0, 1, \ldots, \quad n \in [0, N],\ r \in [0, R],\ n \neq r$$

provided that state restrictions (4.3) are fulfilled. The proof shows it is not possible to return to a previous voltage level during a bit-cycle phase, with the exception of the input voltage V_{in} which is independent of the digital word B. Therefore each voltage level is unique, and can be represented by a unique value of the digital word B.

Correct output can be determined by considering the smallest voltage step of the bit-cycle phase, V_{LSB}. By definition the correct output word will cause quantization error V_Q less than, or equal to V_{LSB}. Finding the quantization error for each symbol during bit-cycling:

$$V_{Q,split}(N) = V_{DACout,n}(N) - V_{CM}(N) \tag{4.11}$$

By looking at the plotted quantization error it becomes apparent that there are ambiguity in correct output at the transition point between two preceding output values, *see* figure 10. Two correct digital outputs is found by considering V_{in} and the limits for V_Q at transition time:

$$V_{in}(\frac{T}{2} + N_{Level} \cdot T) = N_{Level} \cdot V_{LSB}(N) + \frac{V_{LSB}}{2} \tag{4.12}$$

$$V_Q(t) \lim_{a \to \pm 0} = \mp \frac{V_{LSB}(N)}{2} \tag{4.13}$$

$$a = t - (\frac{T}{2} + N_{Level} \cdot T) \tag{4.14}$$

$$\tag{4.15}$$

Using these limits it is possible to find an equation for the quantization error of the switching scheme at the transition points between two levels:

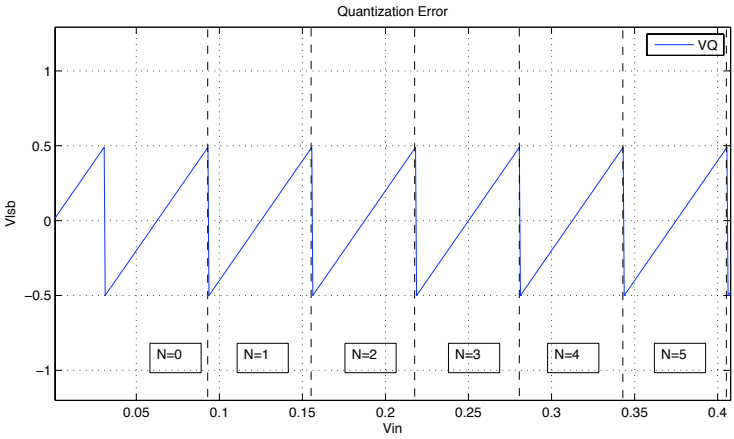


Figure 25: Decision levels in a segment of the quantization error for a 4-bit ADC

$$V_Q(N_{Level}) = V_{CM} + V_{LSB}(N) \cdot (N_{Level} + \frac{1}{2}) + \sum_{i=1}^{N} \Delta V_{out,n}(N) \cdot (b_{p,i} - b_{n,i}) \tag{4.16}$$

$$V_Q(N_{Level}) = \begin{cases} -\frac{V_{LSB}(N)}{2} & a = 0+ \\ \frac{V_{LSB}(N)}{2} & a = 0- \end{cases} \tag{4.17}$$

The code B_p and B_n can now be derived from (4.16) / (4.17)

for each unique level. Setting $V_{LSB}(N+1)$ proves the gain from VBL code by allowing additional levels compared to the traditional binary word. Table 1 shows a 4-bit table accounting for all levels with different symbol representations.

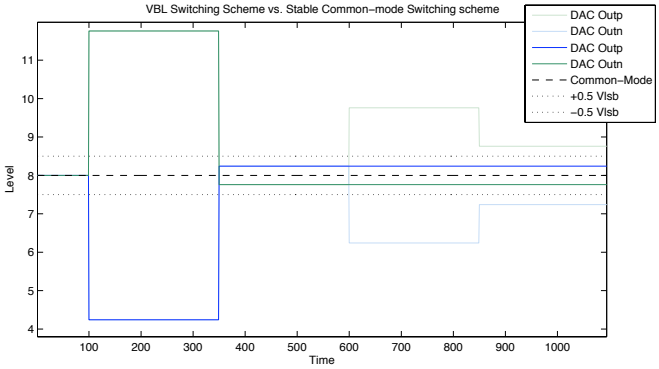
Figure 25 shows the different bit-decision levels N_{level} in the quantization error. Inputs within one level of the output word B should always return the same value, and there should be no ambiguity in decisions. Using variable length code in a sequential environment, such as the bit-cycle phase of the SAR ADC, could potentially cause ambiguity in the code when an earlier decision consume the level space of a later decision. For this reason it is important to ensure that there is no overlap in level space for any decisions.
Equation (4.10) shows that it is not possible to return to a previous state, and (4.16) that code transitions generates unique output words for each level. Defining a code unique level range as the range where a single VBL code is unique for a given number of bits:

$$\Delta = \frac{\hat{s} - \hat{s}_{prev}}{2} + \frac{\hat{s}_{next} - \hat{s}}{2} \tag{4.18}$$

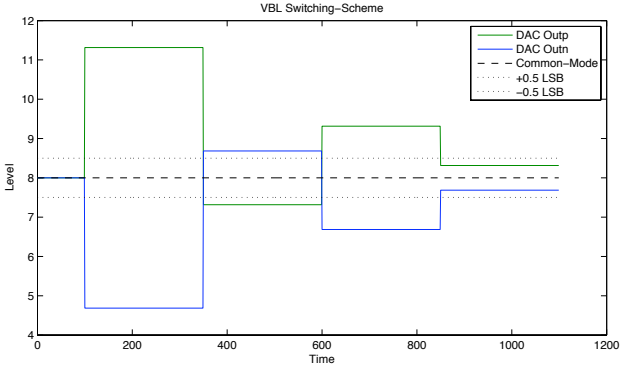
The range defined in (4.18) ensures that the quantization output $\hat{s}$ is the closest point for any input within Δ. Substituting the quantization output with the voltage levels of the DAC $V_{DACout,n}(N)$, and finding the average unique code range Δ using level code from table 1:

Decimal	Binary	3-bit	VBL
0	0000	111 000	000
1	0001	111 001	00
2	0010	110 001	001
3	0011	111 011	0
4	0100	101 010	010
5	0101	101 011	01
6	0110	100 011	011
7	0111	111 111	-
8	1000	011 100	100
9	1001	011 101	10
10	1010	010 101	101
11	1011	011 111	1
12	1100	001 110	110
13	1101	001 111	11
14	1110	000 111	111
15	1111	- -	-

Table 1: 4-bit level representations



(a) Early level detection



(b) Late level detection

Figure 26: Level detection in the VBL switching scheme

$$\hat{s}_n = \sum_{N}^{i=1} \Delta V_{out,i} \cdot (b_{p,i} - b_{n,i}) \tag{4.19}$$

$$\hat{\Delta}(N) = \frac{\sum_{i=1}^{L} \Delta_i}{L} = \frac{1 + LSB(N)}{2} \cdot V_{LSB}(N) \tag{4.20}$$

This comes very close to the resolution $V_{LSB}(N+1) = \frac{V_{LSB}(N)}{2}$ required for an additional bit. Average distortion can be calculated [31]:

$$\begin{aligned} D = 2 \sum_{i=1}^{L/2-1} \int_{(i-1)\hat{\Delta}}^{I\hat{\Delta}} g[\frac{(2i-1)\hat{\Delta}}{2} - s] f_s(s) ds \\ + 2 \int_{(L/2-1)\hat{\Delta}}^{\infty} g[\frac{(L-1)\hat{\Delta}}{2} - s] f_s(s) ds \end{aligned} \tag{4.21}$$

Where $g[*]$ is the difference between input signal s and quantized output $\hat{s}$, $\hat{\Delta}$ is the average unique code range, L is total number of levels and $f_s(s)$ is the probability density function (PDF) of the input. Table 2 presents SQNR values for different number of bits.

The SQNR and ENOB after VBL encoding the source indicate close to 1-bit of resolution gain compared to uniform quantization. A new DAC architecture intended for use with VBL code is presented in figure 27. The total capacitance has been reduced to a 3-bit implementation, and can be found using (4.6). This reduction favors both speed and power efficiency of the SAR ADC.

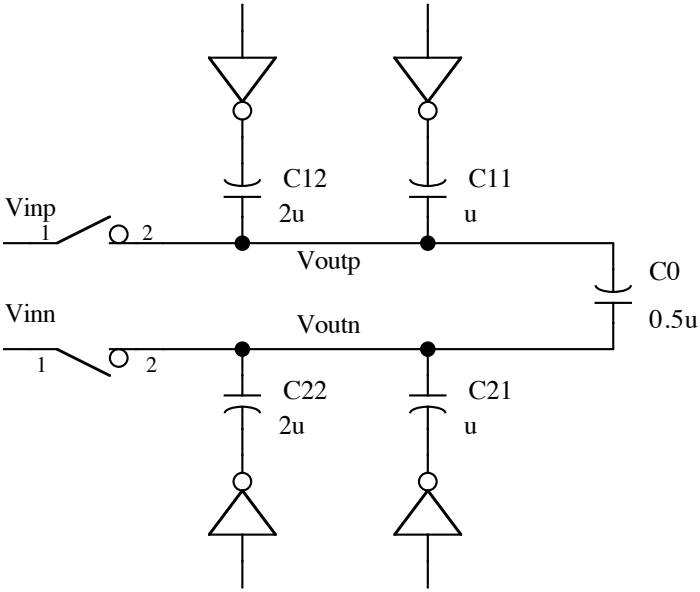


Figure 27: Differential split potential capacitor array with variable bit length code

Number of Bits(N)	Number of Levels(L)	SQNR (dB)	ENOB
3	15	25.28	3.92
5	63	37.74	5.98
7	255	49.89	7.994
8	511	55.92	8.997
11	4095	74	11.9996

Table 2: 4-bit level representations

4.3 Level Detector

The major difference in the SAR algorithm using VBL contra constant bit length code is having a variable length bit-cycle. The algorithm must detect correct output at any stage in this phase, unlike the traditional method when correct output is determined after the last cycle.
In (4.20) the average unique code range for N bits where found. Inputs within this range produced output levels with enhanced SQNR compared to traditional constant bit length approaches. The SAR ADC must then be able to detect inputs inside the range $\hat{\Delta}$, which can be done with a *level detector*.
Using a level detector to detect the output breaks with the traditional operation of the comparator used for the binary search inherit in the SAR algorithm. The variable bit length approach can no longer be said to use a "pure" binary search. The level detector can use three separate states, whereas a traditional binary search only require two. An example state table is presented in table 3 for a level detector. The three states *Undetected below*,

Output	State
00	Detected/Reset
01	Undetected *below*
10	Undetected *above*
11	Detected

Table 3: State table for a level detector

Undetected above and *Detected* are used directly with the DAC output and bit-cycle. Here *Undetected above/below* work like a traditional binary search and *Detected* results in termination of the bit-cycle phase. When operating the level detector with the split-potential capacitors, the states coincide and could be used directly to produce the appropriated voltage shift $\Delta V_{Out,n}(N)$ (3.3).

4.4 Decoding the VBL Code

The digital output word must be decoded since the output of the SAR ADC use a type of VBL encoding. The decoding is relativly simple, most notably an additional bit must be added going from 0-8-bit to a 9-bit word. Figure 28 shows the syntax for a pseudocode and VerilogA implementation of the decoding algorithm.
Consider a 4-bit output *result* and two 3-bit output words $B_{p/n}$. The VBL representation is simply obtained from the positive output word $B_p(i) \neq B_n(i)$ starting from MSB $i = 2$. As is apperent from the pseudo code, the two different combinations

PseudoCodeDecode.pseudo

```
result = 0
for(i in N downto 0)
  if (bp(i) and bn(i)) do
    result=result+(1<<i);
  else do
    result=result+(1<<(i+1)) if bp(i)==1;
end
```

(a) Pseudo code

VerilogACodeDecode.va

```
 parameter real      thres=(vdd+vss)/2;  // logic
     treshold level
...
parameter integer    dir= +1 from [-1:1] exclude 0; //
    1 for trigger on rising edge
...
@(initial_step) begin // set initial value for
    integers
  result=0;
...
@(cross(V(clk)-tresh,dir)) begin // on clk posedge
  if(V(exec)>tresh) begin
    for(i=7; i>=0; i=i-1) begin
      if(((V(bp[i]>thres)&&(V(bn[i])>thres))||((V(bp[i
          ])<thres) && (V(bn[i])<thresh))) begin
        result = result+(1<<i);
      end
      else begin
        if (V(bp[i])>thres) begin
          result = result + (1<<(i+1));
      end
    end
  end
  i_aout = result / 512.0;
  i_dout = result;
...
  result = 0;
```

(b) VerilogA code

Figure 28: Syntax for decoding VBL output

$B_p(i) = \bar{B_n}(i)$ and $B_p(i) = B_n(i)$ are handled different with a offset in bit-placement. Notice in table 1 how the LSB of the 4-bit output is given by the length of the VBL code. When all available bits are utilized the LSB become 0, subsequently $LSB = 1$ if one or more bits are left out. Furthermore the only cases where $MSB = 1$ are given by $\bar{B_n}(2) = B_p(2) = 1$. This results in LSB being determined by the equality and MSB by the inequality of of B_p and B_n. The only difference is that the inequality contains one bit of information, while the equality only contains a single state *equal*.
Similar to the level-detector, the remaining bits contains three states of information: 0, 1 and *equal*. In the output word state 0 and 1 translates to 0 and 1 at position $i + 1$, while *equal* result in 1 at position i. Following the procedure of the bit-cycle phase a *reset*-state can never be subsequented by an *Active*- or *Set*-state. An equality in $B_{p/n}$ can therefore never be followed by an inequality. This fact makes it possible to decode the symbols, although excluding a single symbol from the codebook: $result \neq$ "1111". // Decoding of the embedded VBL code is trivial and done by adding missing LSBs. Notice in table 1 how the VBL code is contained in all the binary representations. A sequence of "0111..." reconstructing the VBL word to 9-bit decodes the signal.

4.5 Digital Logic

In this thesis a novel digital asynchronous circuit integrating the clock generator and shift-register was designed. The circuit use a differential approach, using both outputs of the compara-

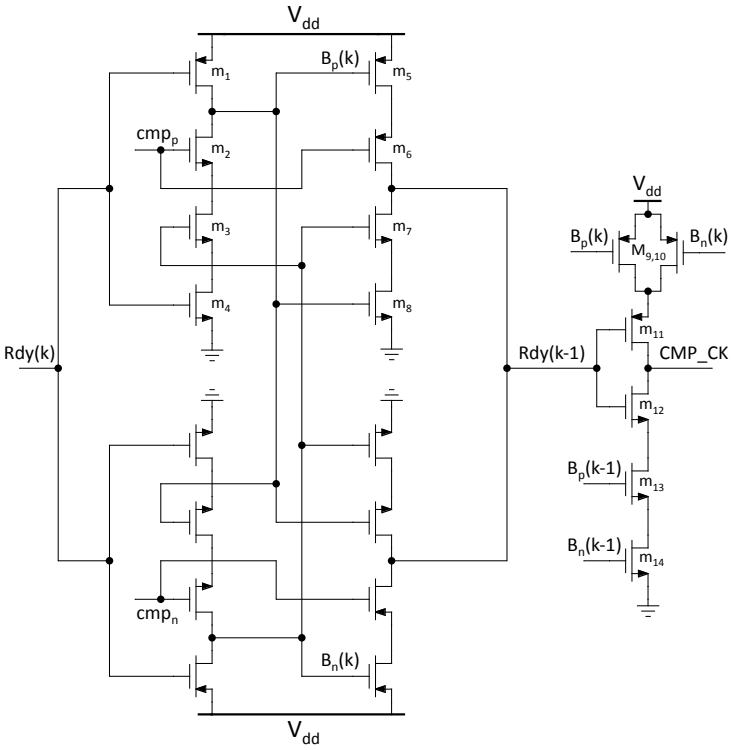


Figure 29: Bitslice schematic

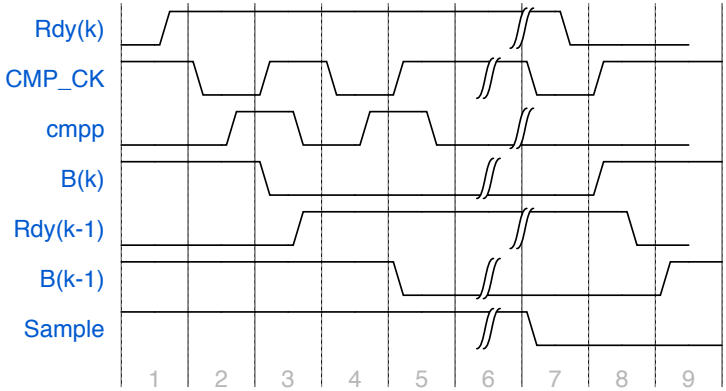


Figure 30: Select waveforms of the bitslice

tor. Individual bitslices are connected in series, each representing a single-bit. Output signals from the bitslice are used to clock the comparator, and initiate the next bitslice in the cycle. The comparator clock use parallel-connected outputs, with high impedance nodes at inactive bitslice [4]. A trade-off was made increasing circuit area and reducing switching activity in order to increase power efficiency and include bit memory in the Muller-pipeline like req/ack procedure, *see* [32].

Bitslice The transistor level schematic for the bitslice is included in figure 29. The circuits operates in three separate phases; *Reset*, *Active* and *Set*. These phases can both be seen

in the outputs and activity of the bitslice. During *Reset* phase input $Rdy(k)$ is low, and outputs $B_{p/n}(k)$ and $Rdy(k-1)$ are static with values high and low respectively. Transistors M_9 and M_{10} are both in $pinch-off$, making the node at output CMP_CK high impedance.
The *reset* phase is maintained until $Rdy(k)$ is pulled high, and *Active* phase is initialized. During this phase output $B_{p/n}(k)$ becomes dynamic when transistor M_1 goes into pinch-off. $B_{p/n}(k)$ remains in this state until a low/high transmission on input $cmp_{p/n}$ pulls the appropriate output down. The activity on $B_{p/n}$ simultaneously puts output $Rdy(k-1)$ in a dynamic state while pulling output CMP_CK high. Clocking the comparator will reset its outputs $cmp_{p/n}$ affecting the bitslice output $Rdy(k-1)$ pulling it high and initiating the last phase.
The last phase *Set* guarantees correct output on $B_{p/n}$ and clocks the next bitslice with $Rdy(k-1)$ putting it in *Active* phase. The positive flank of $Rdy(k-1)$ will set CMP_CK static low, initiating comparison for the next bit decision. This will affect the input signals B_{p/n_next} which will in turn put output CMP_CK in high impedance mode.
Figure 30 shows waveforms relevant to the bitslice. The flanks of the output signals are shown out of phase with the input signals to better illustrate the operation. It is important to note that CMP_CK shares node between all bitslices, thereby eliminating the need for any extra combinatory logic [4]. This is done to save dynamic power dissipation by reducing switching activity; however sharing nodes will greatly increase the parasitic capacitance limiting the speed of the clock. A slow flank on CMP_CK will increase leakage and short circuit current in

connected transistors. The delay inherently generated is useful for the settling of the DAC, as will be clarified later in section 5.2.
The timing diagram show bitslice k during a bit-cycle. The three phases of the bitslice is marked, with $reset$ being the initial phase. A transition on $Rdy(k)$ marks the start of the second phase $Active$.

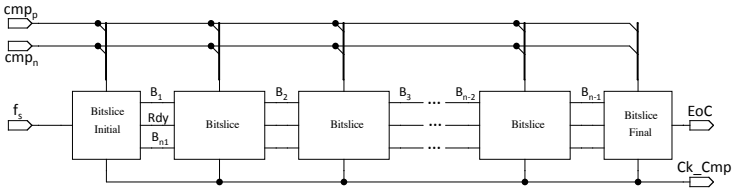


Figure 31: Block diagram for the Digital Logic

5 Design

This section describes the design evaluated, and looks at the ADC components separately. These include: Digital logic, digital-to-analog converter, bootstrapped sampling switch and level-detector. Low threshold voltage general purpose transistors were used in order to minimize the required supply voltage, and thereby power dissipation [36]. Using a uniform technology process for the entire design was a desired selling point; having "pure" technology without using multiple masks increasing fabrication costs.

5.1 Digital Logic

The digital logic is made up of bitslices connected in series, one for each bit of resolution. A block diagram representation can be seen in figure 31, both input and output signals associated with the digital logic is included. The inputs signals consist of the sampling frequency f_s and the decision bits from the level-

detector $cmp_{p/n}$, while the outputs include the digital output word B and the comparators clock Ck_{Cmp}.
The logic supports VBL operation for the SAR ADC by using the level-detector decision bits $cmp_{p/n}$ as acknowledge signals in a req/ack procedure with Ck_{Cmp}. Whenever the comparator is clocked the bitslice is put on hold until a change is made on the output on the level detector. During a *detected* decision, none of the decision bits are switched, locking the active bitslice until next reset by the sampling frequency f_s.
The initial and final bitslice differs from the remaining blocks since some of the functionality becomes redundant. Recount the transistor level schematic of figure 29 describing a bitslice. The inital bitslice will not be able to recieve bit information from a preciding slice, and similarly the final bitslice will not recieve information from a later slice. This makes the complete bit-stage and transistors $M_{9,10}$ in excess for the initial blitslice, and the comparator clock and transistors M_{5-8} in excess for the final bitslice.

5.2 Digital-to-Analog Converter

Part of the DAC implementation is depicted in figure 32. Input signal DAC_{in} are connected to the output of the sampling switch, the bit signals b_i are connected to the digital logic and DAC_{out} is connected to the level-detector. The operation is as described in section 4 and the merged capacitor-pairs are switched on either side by one of the bit signals. During bit-cycling only one of the two bit-pairs will switch for each step, therefore only three inverters and two capacitors will consume

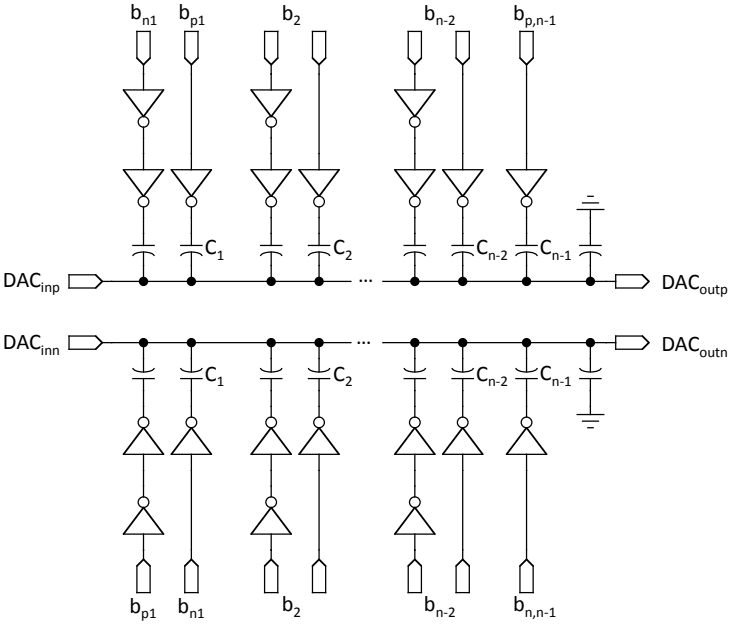
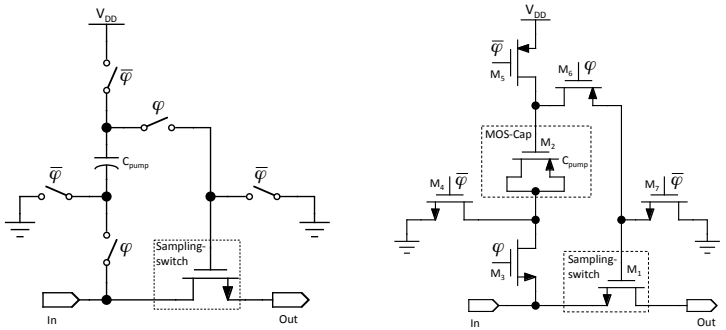


Figure 32: Digital-to-Analog Converter

dynamic energy per bit.
The relatively simple implementation is fully differential since the top half is inverted compared to the bottom half of the DAC with regards to input signals. To prevent excesisve voltage spikes at the output increasing settling time and dynamic power consumption the inverters are "slope-engineered" to have currents through the PMOS and NMOS approximatly equal during transitions in order to match the charge/discharge time of the capacitors.
DAC settling time is imperative when clocking the comparator. The output should settle within an acceptable value before comparator latch-stage. This value becomes approximatly 0.2% with 9-bits of resolution, estimated from $LSB = \frac{1}{512}$.

5.3 Bootstrap switch

One of the main incentives for this thesis is to see if it is possible to operate a SAR ADC in mid- to high-speeds (50-MS/s) and medium resolution (9-bits) at half the supply voltage listed for a technology (0.5-0.6V for ST Microelectronics 065nm technology [36]). Having a reference equal to the supply voltage at half the technology-stated value has the advantage of allowing transistors to operate with a higher voltage relative to supply, without sacrificing reliability. Designing a bootstrap switch under these conditions is simplified due to reliability issues being less of a problem.
The bootstrap design can be seen in figure 33a, represented with ideal switches and capacitor. The clock for the switch is denoted as φ and $\bar{\varphi}$ for the appropriate clock phase. The circuit operates



(a) Bootstrap with ideal components

(b) Transistor-level bootstrap switch

Figure 33: Bootstrap switch

much like a charge pump, with a pre-charged capacitor C_{pump} driven by the input signal at the bottom-plate. Pre-charging happens in phase $\bar{\varphi}$ when the bottom-plate of C_{pump} is connected to ground, while the top-plate is connected to supply V_{DD}.

When phase φ starts there is an initial voltage equal to V_{DD} across C_{pump}, this voltage is preserved throughout φ. Switches corresponding to the clock-phase φ is closed, shifting the reference potential at the bottom-plate of C_{pump} equal to the input voltage. The charge over C_{pump} maintains the voltage across the capacitor, resulting in voltage at the top-plate referred to ground:

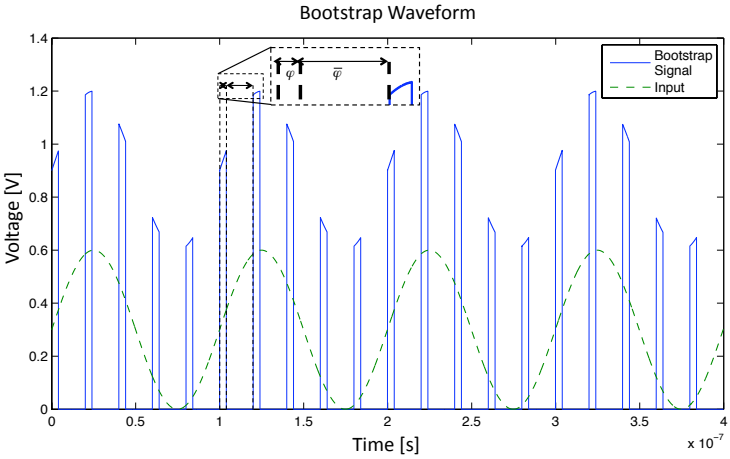


Figure 34: Bootstrap waveform

$$V_{tp} = V_{DD} + V_{in} \tag{5.1}$$

Figure 34 shows the voltage at the gate junction of the sampling switch during both clock-phases. The voltage across gate and drain for the sampling switch can be easily calculated:

$$V_{gd} = V_{DD} + V_{in} - V_{in} = V_{DD} \tag{5.2}$$

This equation holds approximately true for the gate/source voltage V_{gs} as well when the on-resistance is low. Constant voltage across the transistor junctions means no variation in parasitic capacitances, which would otherwise generate distortion.
There will be no loss of charge over the capacitor in the ideal case during phase φ, however this is not the case in reality. There are for this reason several considerations to make when designing the bootstrap switch. The proposed circuit has a simplified design approach since there are less reliability issues when using low supply voltage. Some considerations must be made with regards to loss of charge, and performance at the design frequency. Figure 33 depicts a transistor level implementation of the bootstrap switch. The off-resistance for transistor M_5 needs to be sufficiently large in order to prevent loss of charge over C_{pump}. Moreover the capacitive value of C_{pump} must be large in order to drive the sampling switch M_1.
Clocking the bootstrap switch is done with two inverted clock-signals Clk and $\bar{Clk}$; phase $\varphi/\bar{\varphi}$ decide what clock to use for transistors being active in the same phase. M_3 and M_5 share

clock signal Clk, while M_4 and M_{6-7} use the inverted clock signal $\bar{Clk}$. The most critical transistors of the design M_3 and M_5 are clocked on the same clock, and benefit from using a higher voltage in order to minimize/maximize on- and off-resistance respectably. Transistor M_3 needs to handle rail-to-rail input signal and would need to be implemented using CMOS transistor if the maximum voltage was limited by the supply. However since both M_3 and M_5 benefit from higher voltage the design is further simplified by amplifying the clock signal. Amplification by a factor 2 is easily achieved by using a simple charge-pump circuit.

5.4 Level Detector

The level detector is essential in the operation of the ADC, and is central in the algorithm. Section 4.3 define the specifications, and explain the function of the level detector during the bit-cycle phase. The range the level detector is able to detect is directly related to the accuracy of the ADC.
A possible implementation of a level detector is shown in figure 35. It consists of two comparators and a *varactor*, the comparators are connected in parallel by opposing input ports, while the inverting outputs are connected together through the varactor. The actual outputs Out of the level detector are connected to the non-inverting outputs of the comparators and operate as a differential output pair outside the voltage range detected by the circuit.
The level detector operates two comparators with a controlled DC-offset in order to generate three unique outputs *undetected*

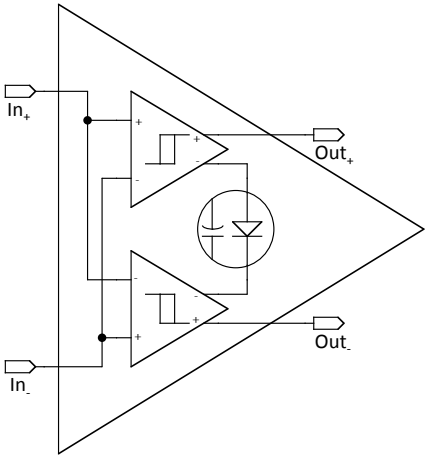


Figure 35: Implementation of a level detector

above, *undetected below* and *detected*, *see* table 3. The capacitive load C_l at the outputs of the comparators influences the decision (2.28), and can be designed to generate DC-offset when time constants at the outputs are skewed.
The *varactor* works as a variable load, changing as the voltage over it changes. For large differences in input voltage ΔV_0 the two outputs are matched when one of the output quickly regenerates. When the difference is small, voltage on both outputs raise as both output nodes regenerates. This will in turn change the characteristics of the *varactor*, increasing the capacitive load. The DC-offset generated for both comparators allow them to make contradicting decisions within a small range for the input difference ΔV_0, from here on referred to as the *Deadzone* of the level detector. The outputs will return the logic value associated with *detected* in the truth table within this range.
Difficulties while designing a level-detector include accuracy of the output, which may well only be achieved with very small differences to the capacitive load. This is the major motivation in using a varactor at the output, since it is possible to realistically implement with small changes to the capacitive load. Designing the level detector to be as symmetrical as possible is beneficial with regards to matching the outputs, and extends through layout.
Various effects such as noise and mismatch may affect the level-detector differently than a normal comparator as a result of having two decision points rather than one. This will be a consideration when simulating the circuit, and discuss in section 7.
The varactor has been implemented with the possibility of bulk

connections being operated by an external voltage V_{set}, this is done to introduce a variable tuning range V_{set}. Being able to change the load may help counter effects of mismatch and charge-injection errors (2.29), additionally the bulk connections of the input transistors can also be used for this purpose. Note that the varactor is a two-port device, and it may be misleading to refer to the three-port tunable version as a varactor.

6 Results

This section presents simulated results related to the ADC design. Simulation were done over process corners "SS", "TT" and "FF", and analyzed using FFT in combination with 1024 point coherent sampling. Noise was simulated using transient noise analysis and parasitic capacitances were added to major nodes of the design. Power was calculated by integrating the current over the full duration of the 1024 sample simulation. Mismatch simulation was planned but not completed due to time constraints of the project.

6.1 Specifications

The specifications for the design is presented in table 4 based on an ultrasound system. Some design variables - such as supply and technology process - were chosen to fit the design with regard to optimized FoM.

6.2 Overview of Main Simulated Results

Results of simulations for three process corners with noise included are presented in table 5.

6.3 Power

Power consumption was simulated seperatly for each of the ADC components, and is presented in table 6. Results are based on

Parameter	Value	Unit
Supply Voltage	0.6	V
Sampling frequency	50	MHz
Resolution	9	bit
SNDR	>54	dB
ENOB	8.66	bit
Power	Min.	W
FoM	Min.	J/conv. step
Technology	065	nm
Process	LVTGP	-

Table 4: Design Specifications

simulation done including noise, in the "TT" process corner and with 2048 samples. Energy is reported for a single conversion.

6.4 Noise

Noise for all ADC components were simulated independently in order to determine major noise contributors. Table 7 provide the results.

6.5 Non-Linearity

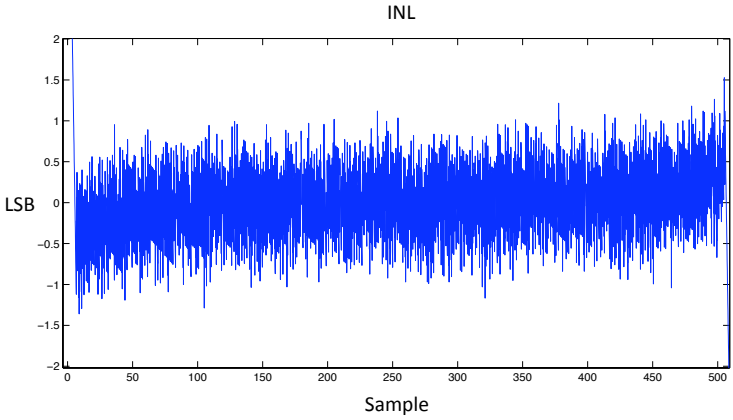
Non-linearities was simulated using a sweeping input from Gnd to V_{DD}. Best-fit line was used to determine INL, using simple linear regression. DNL was found using a histogram test. The sweep was done with 10 points per ADC level for a total of 5120

Parameter	Corners			Unit
	FF	TT	SS	
Power	32.47	24.17	22.52	μW
w/noise	-	24.5	22.79	
SNR	50.64	55.95	55.20	dB
w/noise	47.92	52.88	53.89	
SNDR	50.23	55.71	54.32	dB
w/noise	47.59	52.84	52.76	
SFDR	59.26	66.62	62.17	dB
w/noise	57.94	71.96	59.58	
THD	-59.2	-66.07	-61.01	dB
w/noise	-57.2	-70.19	-59.24	
ENOB	8.05	8.96	8.73	bit
w/noise	7.61	8.48	8.47	

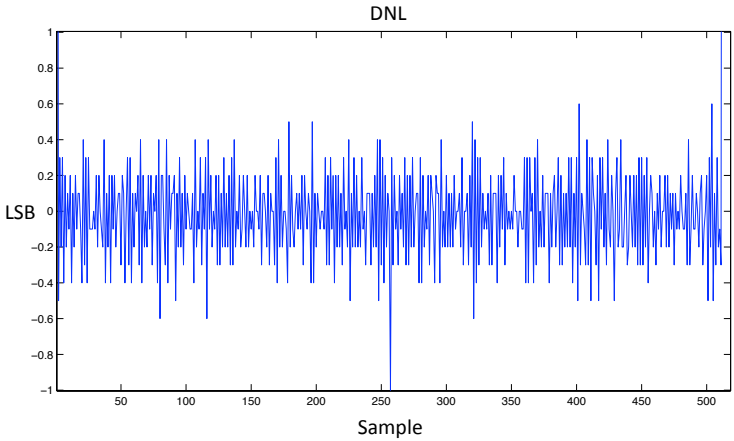
Table 5: Main Simulated Results

Component	Percent of Overall	Power	Average Current	Energy
Level Detector	63.1%	15.47 μW	25.78 μA	0.31 fJ
DAC & Sampling Switch	24.4%	5.97 μW	9.95 μA	0.12 fJ
Digital Logic	12.5%	3.06 μW	5.1 μA	0.06 fJ
Total	100%	24.5 μW	40.83 μA	0.49 fJ

Table 6: Power consumption



(a) INL



(b) DNL

Figure 36: Non-linearity analysis

Parameter	Total	Sampling Switch & DAC	Level Detector
SNR	52.88 dB	55.25 dB	53.42 dB
SNDR	52.84 dB	55.11 dB	53.31 dB
ENOB	8.48 bit	8.86 bit	8.56 bit

Table 7: Noise contribution

points. The results can be seen in figure 36.

6.6 Deadzone

Analysis of the deadzone was conducted, and simulation featuring a sweep of the deadzone is presented in figure 37. The sweep was done on a scale relative to $1/2V_{LSB}$ normalized to 2, and plotted on a logarithmic scale with base 2. The y-axis show both ENOB and power consumed in the digital part as a function of deadzone range ΔV.

7 Discussion

Results presented in section 6 are discuss here. Emphasis is made with regards to the new design approach when reviewing the results. Important aspects considered include: Impact of design choices, applicability in ultrasound systems and comparison to recent literature.

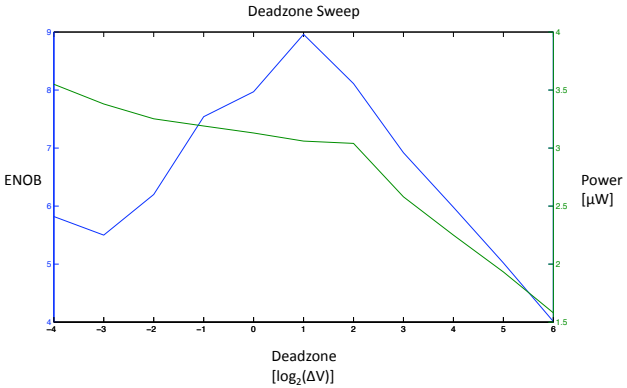


Figure 37: Deadzone Sweep

7.1 General Comments to Simulated Results

Based on the results presented in table 5 it becomes apparent that the accuracy of the design is limited by noise. This observation is based on approximately equal reported SNR/SNDR values, consequently showing that distortion does not further degrade signal quality.

Power reported show a dependency on process corner. The relative change in threshold voltage V_{th} for the different cases cause increased leakage currents through transistors. An expected rise in static power dissipation in lower threshold voltage process corners dominates expected improvement to short-circuit currents for overall power-consumption in the design. This could

be an indication that the threshold voltage approaches its lower limits, thus proving efficiency of design choices.
The "FF" corner has a substantial decrease in signal integrity, indicating improper operation. The main reason is current leakage causing digital logic to fail. Leakage current is dependant on the supply voltage, and reducing headroom could correct operation. For further work the optimal supply voltage should be determined. The current supply voltage was chosen to assure enough speed in the "SS" corner, however further optimization of the level detector and transistor size adjustment may allow the ADC to operate on a lower supply voltage.

7.2 Impact of Design Choices

The initial motivation for the VBL coded design was using additional comparators in order to increase power efficiency for remaining components. In recent literature comparator power consumption has been relatively low compared to the digital logic and the DAC [7, 15]. The simulated results show increased power efficiency in both the DAC and the digital logic, however the level-detector starts to dominate power consumption with 63.1% of total. The large capacitive load at the output of the comparators supressing the kT/C-noise is almost exclusively the reason why power consumption is high.
With more than half of the power being consumed in the level-detector further optimization of this component has the greatest effect on overall power efficiency. The design methodology using two comparators has two redundant output ports terminated in

large capacitive loads. Alternative implementations removing these redundancies can potentially greatly reduce power consumed. A thorough noise analysis should be conducted and alternative architectures explored in order to optimize the design.
The reduction of required cycles during the bit-cycling phase gives an approximately linear reduction in power for the digital logic and level detector. Leakage currents cause static power consumption that increase with the area and consequently continuously dissipate power even when circuits are not active. Reducing number of required cycles helps improve power efficiency and speed of the circuit.
Simulations conducted over the duration of the work intended to determine whether the level detector could be terminated directly to the digital circuit. The bit desicion input-port for the differential logic is one of the largest nodes of the design. Combining this node with the large capacitive load has the potential to improve power efficiency by eliminating extra buffers.
Distortion were generated as a consequence of charge transfer, and variable capacitance in the transistor gates of the digital design. The distortion could be diminished - in a similar manner to noise - by increasing capacitance. The results were inconclusive and thus not included in the thesis, however further work should attempt to conclusivly determine the viability of the design approach.

7.3 Reconfigurability of the Design

Level detector deadzone simulation presented in figure **??** show a linear relationship for bit-resolution as a function of deadzone span. Moreover power is reduced in both the digital logic and the level detector as bit-resolution is decreased. The proposed SAR ADC is reconfigurable with regards to bit resolution. The plot show an ≈ 1 bit reduction for every octave of the deadzone span, and can be approximated:

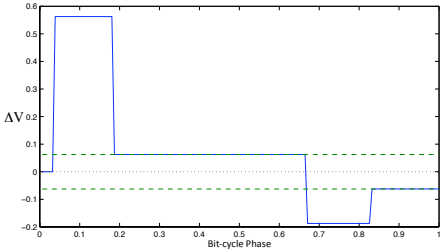
$$Q_{bit} = Q_{design} - \log_2(\Delta \mathrm{DZ}) \quad \mathrm{DZ} \geq 1 \tag{7.1}$$

Here Q_{bit} is the bit-resolution, Q_{design} the design bit-resolution and ΔDZ the ratio between actual and design deadzone span (1/2 LSB).
An interesting observation is that power consumption increase when $\Delta \mathrm{DZ} < 1$. When the level span is zero, the ADC operate in 8-bit mode similar to the traditional approach. Any further reduction of DZ cause distortion at the output as a consequence of improper operation of the digital logic.
The power reduction seen in the digital part is caused as a result of the VBL modified SAR algorithm. After the last decision any further switching would lead to an output within the level detected. Any bitslices extending bit-resolution allowed by the level span would consequently never activate, thus not dissipate dynamic power.
The fact that power consumed decreases with the bit-resolution makes the reconfigurability efficient. A power saving mode - with reduced bit-resolution - can be introduced where appropriate. Reconfigurability means that knowledge of the input signal

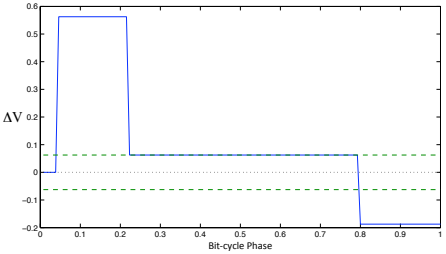
can be exploited in order to improve overall efficiency. An example would be an input with useful information only at specific intervals. The ADC could run in low-power mode in-between intervals in the interest of saving power.
Another consideration is that noise requirements are reduced as the bit-resolution decrease. The capacitive load at the level detector is responsible for a large portion of dissipated power, but could be reduced with reduced accuracy requirements. A variable capacitive load at the level detector output can further reduce power efficiency when full bit resolution is not required.

7.4 Metastability in the Level-Detector

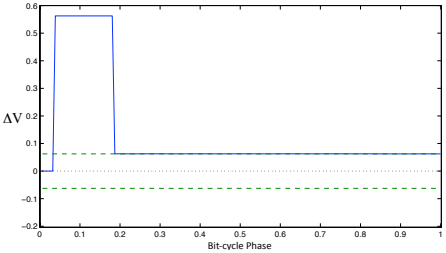
Regular single decision point comparators can suffer from *metastability* when applied with input signals with a small difference ΔV, *see* section 2.3. Ideally a level-detector should not enter metastability at all since small difference in input voltage ΔV are detected; however the proposed level-detector is simply a comparator with two decision points.
During a bit-cycle either of the two comparators in the level-detector can enter metastability, this is however mutually exclusive for each bit since outputs are offset. Consider the waveforms of figure 26, and let the $1/2LSB$ lines represent the comparator decision points. During a single bit-cycle metastability can occur twice, with the second occurrence always during the last comparison.
Metastability inherently means that an output decision is close to the transition between two levels resulting in a quantization error $V_Q \approx 1/2LSB$ regardless of level decided. If one of the



(a) Metastability during 2. and 4. comparison



(b) Metastability causing glitch



(c) Metastability during 2. comparison

Figure 38: Metastability in the level detector

comparators of the level-detector experience metastability at the last comparison, the output will not be affected and only a small DNL error appears. The only time metastability can cause severe glitching is during a comparison prior to the last, and only if it causes continuation of the bit-cycle leading to premature termination due to reset. Three different cases with approximately identical input leading to different outputs are included in figure 38 to demonstrate the effect of metastability.
Figure 38a and 38c illustrate two cases of metastability that is not causing large DNL errors. The level-detector can potentially enter metastability twice, once for each comparator. However the output will always be within the level-detector range at the end of the bit-cycle, making additional comparisons redundant. Consequently only figure 38c cause a wrong output with an insignificant DNL error.
The only case causing serious glitching is seen in figure 38b, here metastability in the 2. comparison extend the time required for a decision, pushing additional comparisons close to the end of the bit-cycling phase. The resultant output contains a glitch generating a large DNL error. Probability of the glitch is greatly reduced as a result of the first two cases; in addition none of the subsequent decisions can enter metastability and are thus significantly faster.
The level-detector and the new SAR algorithm benefits from being able to inherently code outputs even when metastability occur. Decisions can experience glitching, however probability is greatly reduced compared to ADCs that cannot decode outputs when bit-cycles are lost.

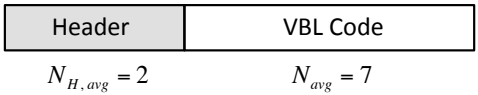


Figure 39: Variable length code

7.5 Possible Implementation with Communication Systems

Variable length code must be uniquely decipherable when transmitted in digital communication systems. There are several ways to ensure unique decipherability, one of which is to include a header containing information about the code to be transmitted, figure 39. 3-bits are required for the header to contain enough information about the 8-bit VBL code. The resulting digital word has a maximum length of 11-bits.
The average code-length of the VBL output of the ADC is easily calculated:

$$N_{avg} = \sum_{i=1}^{N} i \cdot p_{bl,i} \tag{7.2}$$

Here $p_{bl,i}$ is the probability of a bit-length and N the maximum number of bits. Assuming uniform input with equal probability for each code, $p_{bl,i}$ is given by;

$$p_{bl,i} = \frac{L_i}{L_{tot}} \tag{7.3}$$

where L_i is the number of levels associated with bit-length i, and L_{tot} the total amount of levels.

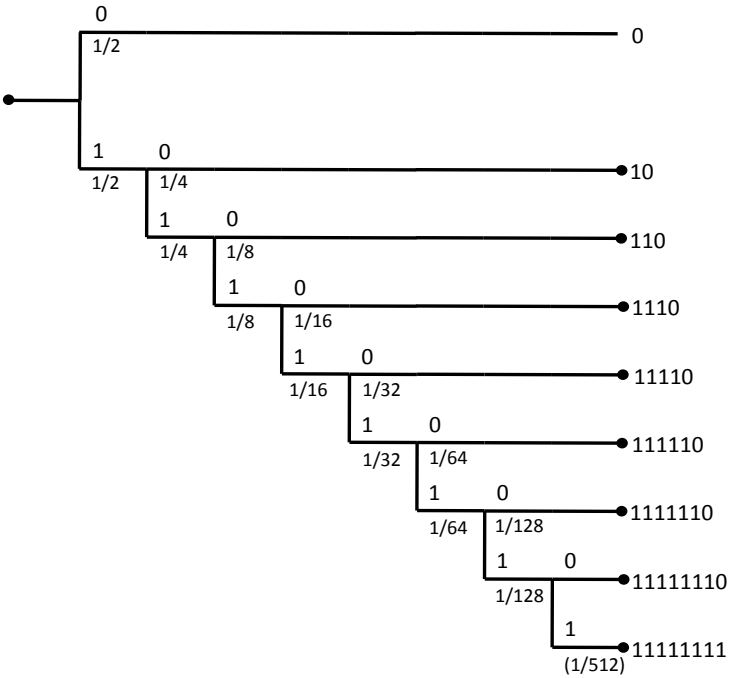


Figure 40: Huffman code for the 8-level header

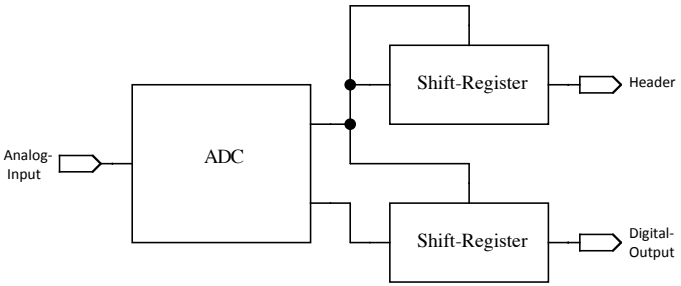


Figure 41: Block diagram of an exemplary ADC output

Average numbers of bits become $N_{avg} = 7$ for 8-bit VBL, resulting in VLC with average bit length $N_{VLC,avg} = 10$. Furthermore it is possible to code the header using VBL. Entropy rate is given by, *see* for example [31];

$$H = -\sum_j p_j \log_2 p_j \tag{7.4}$$

resulting in an entropy rate for the 8-level header of $H_{head} = \frac{251}{128}$.
A Huffman code representation can be found for the header illustrated by the binary branching tree of figure 40 [28]. Here an additional branch is added for the 0-bit code resulting from $V_{Delta0} > V_{LSB}(9)$, (2.28) and (3.1). Using (7.2) to find the average bit-length $N_{H,avg}$ result in $\frac{253}{128}$ and $\frac{251}{128}$ with, and without the additional 0-bit level respectively. Notably here the Huffman code achieves average bit-length equal to the entropy rate, and thus hit the fundamental limit of lossless encoding.
The thermometer-code nature of the header means that it will be easily implemented using for instance a shift-register. An exemplary block diagram of the ADC output is shown in figure 41. The VLC output bit-rate would be equal to;

$$R_{b,VLC} = (N_{H,avg} + N_{avg}) f_s = 448.83 \text{ Mb/s} \tag{7.5}$$

following the calculations for the VLC average bit length done for $N_{H,avg} + N_{avg}$ in (7.2). A marginal improvement compared to the 450 Mb/s output of a traditional ADC under the same conditions.
An interesting observation is that the decoded output can be

Parameter	This Work	[4]	[7]	[15]
Year Published	-	2012	2010	2012
Supply Voltage	0.6 V	0.7V	1.0 V	0.7V
Sampling Frequency	50MHz	2MHz	1MHz	1KHz
Resolution	9-bit	10-bit	10-bit	10-bit
Power	24.5 μW	3.56 μW	1.9 μW	3nW
ENOB	8.48-bit	9.3-bit	8.75-bit	9.1-bit
FOM [fJ/Conv.]	1.37	2.8	4.42	5.5

Table 8: Comparison to previous state-of-the-art

read from the left in figure 39 when it represents VLC generated in the block-diagram of figure 41. Recall that the Huffman code representation of figure 40 and LSB sequence describe in section 4.4 are equal.
Calculations done in this paragraph show that the VBL approach to the SAR ADC does not suffer from increased bit-rate compared to its constant bit length counterpart. Additionally it showed that decoded VLC is trivially obtained from the ADC output by using the approach presented in figure 41.

7.6 Comparison to Previous State-of-the-Art Designs

Table 8 comparing simulated results of the proposed SAR ADC with recent state-of-the-art publications, show that the proposed design achieves the best FoM. However reported results of the compared designs are based on measurements, and are

hence not directly comparable to simulated results.
Parasitic capacitance was added to major node, and noise was simulated for the whole circuit. The expected increase to power consumption in a prototype is as a result not as high, and may well be within the margins of the FoM reported for other designs. Furthermore power dissipation in the level detector is high compared to the remaining circuitry, and could be subject to optimization.
Some prediction for the power consumption in the level detector, DAC and digital logic can be made. Previous layout of digital logic - similar to the one proposed - resulted in an approximate doubling to power dissipated. An assumption that is also supported by the results of [15]. Moreover the DAC mostly consists of capacitors, and is for that reason adaptable with regards to parasitic capacitance. The increase in power from schematic to layout could be relatively small for the DAC. Lastly the level detector is terminated in a large capacitive load, which also could be modified to include parasitic capacitance. Added capacitance at internal nodes will dissipate some power, however relatively little compared to power consumed in the load. As long as speed requirements are met for the comparator post-layout, any additional power dissipated would be marginal.
Assuming $\approx 100\%$ increase to power in digital logic, $\approx 35\%$ in the level detector and $\approx 50\%$ in the DAC, the overall power consumed would be 35.96μW resulting in a FoM of 2.01 fJ/conv. step. Overall results are promising when compared to previous state-of-the-art. Improving on previous FoMs is feasible.

8 Conclusion

A 9-bit 50MS/s successive approximation register analog-to-digital converter was successfully implemented employing a novel variable bit length switching-scheme approach. The converter dissipates 24.5 μW achieving a FoM of 1.37 fJ/Conv. Step. Simulation showed that the design was limited by noise, was found to be most dominant in the level detector.
A level detector consisting of two comparators operated in parallel was used in the core process of the modified algorithm. A trade-off was made between area/power efficiency in the comparator and power efficiency in the remaining circuitry as part of the initial motivation for the thesis. The resulting SAR performance saw a substantial decrease in power consumed in the digital logic and DAC. Nevertheless power consumption in the level detector constituted more than 62% of overall power consumption. Most of the power was consumed in the large capacitive load needed for noise suppression. Moreover a parallel implementation means that two ports are terminated in a load without holding information usable to the ADC. Undesirable redundancies in the design - consuming a large portion of overall energy - should be subject to improvement or change. A more extensive noise analysis should be conducted for further work in order to properly optimize the level detector for FoM.
Metastability in the level-detector was discuss, and are arguably improved compare to using a single comparator. Lower probability of glitching at the output – without using digital recovery – cause the level detector to mitigate the effects of metastability-induced errors

Differential digital logic taking both output ports of the level-detector as input was implemented. The resulting circuit reduced switching activity by eliminating extra bit storage and comparator ready signal generation. The initial motivation was to remove the buffers between comparator and digital logic in order to combine two major nodes. Additional capacitance is usually added as load to the comparator for noise suppression, however matching load at the digital logic should eliminate this need. Simulation demonstrated a considerable increase to distortion arising from effects such as charge transfer and variable capacitive characteristics in transistor gates. Increasing the capacitance can diminish these effects, therefore the approach can be concluded a plausible alternative to buffers and should be a subject of further work.

The deadzone of the comparator can be used to control the bit-resolution of the ADC. Bit-resolution is reduced by one for each octave of the deadzone range above the design specification. Further bitslices extending the ENOB are not activated as a function of the modified SAR algorithm. This makes the proposed SAR ADC highly reconfigurable, without increased redundancies for the bit operation mode chosen.

A discuss possible implementation for communication systems shows that the ADC output can be trivially decoded. Bit-rate considerations found that the digital bits can be transferred at the same rate, or marginally better than the traditional approach.

References

[1] David A. Johns and Ken Martin, *Analog Integrated Circuit Design*. John Wiely & Sons Inc. Toronto, Canada 1997.

[2] Chun-Chen Liu, Soon-Jyh Chang, Guan-Ying Huang and Ying-Zu Lin, *A 10-bit 50-MS/s SAR ADC with a Monotinic Capacitor Switching Procedure*. IEEE Journal of Solid-State Circuits, April 2010, p. 731-740.

[3] Chun-Chen Liu, Soon-Jyh Chang, Guan-Ying Huang, Ying-Zu Lin and, Chung-Ming Huang, *A 10bit 10MS/s Asynchronous SAR ADC in 0.18μm CMOS*. IEEE Journal of Solid-State Circuits, April 2010, p. 731-740.

[4] Pieter Harpe, Guido Dolmans, Kathleen Philips, Harmke de Groot, *A 0.7V 7-to-10bit 0-to-2MS/s Flexible SAR ADC for Ultra Low-Power Wireless Sensor Nodes*. Proc. European Solid-State Circuit Conferance (ESSCIRC), Sept. 2012, pp. 373-376.

[5] Pieter Harpe, Ben Büsze, Kathleen Philips, and Harmke de Groot, *A 0.47-1.6 mW 5-bit 0.5-1 GS/s Time-Interleaved SAR ADC for Low-Power UWB Radios*. Proc. European Solid-State Circuit Conferance (ESSCIRC), Sept. 2011, pp. 373-376.

[6] Brian P. Ginsburg, and Anantha P. Chandrakasan, *An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC*. Proc. IEEE Int. Symp. Circuits and Systems, 2005, pp. 184-187.

[7] Michael van Elzakker, Ed van Tuijl, Paul Geraedts, Daniel Schinkel, Erik A. M. Klumperink, and Bram Nauta, *A 10-bit Charge-Redistribution ADC Consuming 1.9 μW at 1 MS/s*. IEEE Journal of Solid-State Circuits, Vol. 45, No. 5, May 2010, pp. 1007-1015.

[8] John G. Proakis and Dimitris G. Manolakis, *Digital Signal Processing - Principles, Algorithms, and Applications*. Fourth edition, ISBN 0-13-187374-1. Pearson Prentic Hall. New Jersey, USA, 2007.

[9] Gabor C. Temes and Roubik Gregorian, *Analog MOS Integrated Circuits For Signal Processing*. First edition, ISBN 0-47-109797-7. Wiley-Interscience. Canada, 1986.

[10] Mikael Gustavsson, J. Jacob Wikner, and Nianxiong Nick Tan, *CMOS Dataconverters For Communications*. eISBN 9780792377801. Kluwer Academic Publisher. MA, USA, 2000.

[11] Eric A. Vittoz, *Micropower Techniques*. Design of VLSI Circuits for Telecommunication and Signal Processing, Chapter 5. Prentice Hall, 1994, pp. 1.2.1 - 1.2.36.

[12] Dai Zhang, Christer Svensson, and Atila Alvandpour, *Power Consumption Bounds for SAR ADCs*. 20th European Conference on Circuit Theory and Design (ECCTD) 2011, p.577-580.

[13] Dai Zhang, *Design of Ultra-Low-Power Analog-to-Digital Converters*. License thesis, Department of Electrical Engineering, Linköping university, 2012.

[14] Johnny Bjørnsen, *Design of a High-speed, High-resolution Analog to Digital Converter for Medical Ultrasound Application*. Ph.D Dissertation, Department of Physical Electronics, NTNU 2005.

[15] Dai Zhang, and Atila Alvandpour, *A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s*. European Solid-State Circuits Conference, (ESSCIRC) 2012, p.369-372.

[16] Jan Craninckx and, Geert Van der Plas, *A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS*. International Solid-State Circuits Conferance, (ISSCC) 2007.

[17] Behzad Razavim and Bruce A. Wooley, *Design Techniques for High-Speed, High-Resolution Comparators*. IEEE Journal of Solid-State Circuits. Vol. 27. No. 12, Dec 1992, p.1916-1926.

[18] S. Uemura, Y. Hiraoka, T. Kai, and S. Dosho, *Isolation Techniques Against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) Process for RF/Mixed-Signal SoCs*. IEEE Journal of Solid-State Circuits. Vol. 47. No. 4, Apr. 2012, p.810 - 816.

[19] Nishath K. Verghese, and David J. Allstot, *Computer-Aided Design Consideration for Mixed-Signal Coupling in RF Integrated Circuits*. IEEE Journal of Solid-State Circuits. Vol. 47. No. 4, Apr. 2012, p.810 - 816.

[20] Alice Wang, and Anantha P. Chandrakasan, *A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology*. IEEE Journal of Solid-State Circuits, Vol. 40, Nr.1, Jan. 2005, pp.310 - 319.

[21] Anantha P. Chandrakasan, Samuel Sheng, and Robert W. Brodersen, *Low-Power CMOS Digital Design*. IEEE Journal of Solid-State Circuits, Vol. 27, Nr.4, Apr. 1992, pp.473 - 484.

[22] Bob Verbuggen, Masao Iriguchi, and Jan Craninckx, *A 1.7 mW 11b 250 MS/s 2-Times Interleaved Fully Dynamic Pipelined SAR ADC in 40 nm Digital CMOS*. IEEE Journal of Solid-State Circuits, Vol. 47, No. 12, Accepted. Dec. 2012.

[23] Sand-Min Yoo, Jong-Bum Park, Seung-Hoon Lee, and Un-Ku Moon, *A 2.5-V 10-b 120-MSample/s CMOS Pipelined Based on Merged-Capacitor Switching*. IEEE Transaction on Circuits and Systems - II: Express Briefs, Vol. 51, No. 5, May 2004.

[24] Andrew M. Abo, and Paul R. Gray, *A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter*. IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999.

[25] David J. Goodman, *Embedded DPCM for Variable Bit Rate Transmission*. IEEE Transaction on Communication, 1980, pp.1040 - 1046.

[26] Z. Yu, *A Progammable Analog Delay Line for Micro-Beamforming in a Transesophageal Ultrasound Probe*. IEEE

International Conferance on Solid-State and Integrated Circuit Technology (ICSICT), 2010.

[27] T. Wakimoto, H. Li, and K. Murase, *Statistical anaysis on the effects of capacitance mismatch in a high-resolution successive-approximation ADC*. IEEE Trans. on Electrical and Electronic Engineering, 2011, pp.89-93.

[28] David A. Huffman, *A Method for the Construction of Minimum-Redundancy Codes*. Proceedings of the I.R.E, Sept. 1952, pp. 1098-1101.

[29] Massoud Pedram and Farazan Fallah, *Power Aware Design Methodologies - Chapter 13: Circuit and System Level Power Management*. ISBN: 1-40-207152-3 Springer, 2002, pp. 373 - 411.

[30] David M. Pozar, *Microwave and RF Design of Wireless Systems*. ISBN: 978-0-471-32282-5 John Wiley & Sons. Inc, First Edition, 2001.

[31] Jerry D. Gibson, Toby Berger, Tom Lookabaugh, David Lindbergh, and Richard L. Barker, *Digital Compression for Multimedia, Principles & Standards*. Morgan Kaufmann Publishers, 1998.

[32] Jens Sparsø, *Asynchronous Circuit Design - A Tutorial*. for Technical University of Denmark, 2006.

[33] Michael I. Fuller, Karthik Ranganathan, Shiwei Zhou, Travis N. Blalock, John A. Hossack, and William F. Walker,

Experimental System Prototype of a Portable Low-Cost, C-Scan Ultrasound Imaging Device. IEEE Transaction on Biomedical Engineering, Vol. 55, No 2, Feb. 2008, pp. 519-530.

[34] A. Finster, *3-D ultrasound imaging: a review*. IEEE Engineering in Medicine and Biology Magazine, 1996, pp. 41-51.

[35] *SIA*. International Technology Roadmap for Semiconductors; 2009.

[36] ST Microelectronics, *CMOS065 technology LVT-GP MOS transistor models*. $V1.0.a\_st1$, 2009.