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A Novel Analog Front-End For ECG Acquisition

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Abstract

This paper presents a novel, low-power analog front-end aimed for electrocardiogram (ECG) data acquisition. A typical ECG acquisition circuit is composed of a preamplifier, a filter and an analog-to-digital converter (ADC). The proposed solution takes all the analog front-end (AFE) components and integrates them into the loop filter of a 10-bit continuous-time $\Delta\Sigma$-ADC.

The $\Delta\Sigma$-ADC has a 100Hz bandwidth, achieves an ENOB[1] of 9.8 bits and a DR[2] of 85dB at a power consumption of $3.6\mu W$, which is comparable with current state-of-the-art. Through dynamic programming of preamplifier gain, the ADC can maintain a high conversion performance for a wide input signal range.

The low power consumption and moderate resolution makes the AFE especially attractive for portable ECG acquisition systems that utilize wireless data transmission.

[1] Effective Number Of Bits
[2] Dynamic Range

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San Diego, September 24, 2012 Øyvind Theie

Abbreviations

- AAF - Anti-Aliasing Filter
- ADC - Analog-to-Digital-Converter
- AFE - Analog Front-End
- BJT - Bipolar Junction Transistor
- CMFB - Common-Mode FeedBack
- CMRR - Common-Mode-Rejection-Ratio
- CT - Continuous-Time
- DAC - Digital-to-Analog-Converter
- DT - Discrete-Time
- ENOB - Effective Number Of Bits
- FB - FeedBack
- FFT - Fast Fourier Transform
- FS - Full Scale
- LNA - Low Noise Amplifier
- LSB - Least Significant Bit
- MOS - Metal-Oxide-Semiconductor
- NTF - Noise Transfer Function
- OSR - OverSampling Ratio
- PDK - Process Design Kit
- PGA - Programmable Gain Amplifier
- PM - Phase Margin
- PSD - Power Spectral Density
- PVT - Process, Voltage and Temperature variations
- RMS - Root-Mean-Square
- SAR - Successful Approximation
- SFDR - Spurious-Free Dynamic Range
- SNR - Signal-to-Noise-Ratio
- SNDR - Signal-to-Noise-and-Distortion-Ratio
- SQNR - Signal-to-Quantization-Noise-Ratio
- STF - Signal Transfer Function
- THD - Total Harmonic Distortion

Model definitions

$U_T = kT/q$ Thermal voltage

n_i Intrinsic carrier concentration of silicon

ϵ_S Absolute dielectric constant of silicon

q Elementary charge

C_{ox} Gate capacitance per unit area, $C_{ox} = \frac{\epsilon_{SiO_2}}{T_{ox}}$, T_{ox} is the oxide thickness

N_B Impurity concentration in the channel

$\phi_F = U_T ln(N_B/n_i)$ Fermi potential in the substrate

V_{th0} Gate threshold voltage at equilibrium

μ Electron mobility in the channel

$\gamma = \frac{\sqrt{2qN_B\epsilon_S}}{C_{ox}}$ Substrate factor

W, L Effective electrical width and length of channel

Q_i Mobile induced charge per unit area in the channel

V_{ch} Channel "potential"

V_p The pinch-off voltage, describes the channel voltage when $Q_i \approx 0$

V_{eff} The effective channel voltage, $V_{GS} - V_{th}$

r_o The resistance looking into the drain of a MOS transistor

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1 Introduction

The trends of technological development are heavily focused on improving and expanding the integration of digital processing in every day life. This development demands that analog circuitry keep up with the phase. The interest in energy-efficient systems have become a dominant focus as more and more portable products are introduced to the market. During the past 10-20 years, many companies have begun introducing medical electronics to this trend.

This paper investigates the design of an analog front-end intended for detecting the cardiac cycle and converting it into a digital bit stream. The measured signal from the heart should be amplified and quantized, before the acquired information can be processed by a DSP. The product idea is that the DSP compresses and possibly filters the the data before sending it via bluetooth to a remote device, such as a smartphone or computer which can take care of the heavy data processing. The moderate data length combined with smart filtering and compression can make the chip very power-efficient and it may live for a long time on small batteries.

The analog front-end is composed by a *continuous-time* $\Delta Sigma$-ADC with an integrated preamplifier, which helps picking up the feint signals present in the heartbeat. The design is motivated by exploring ways to minimize the power consumption while maintaining reliability and low production cost. $\Delta\Sigma$-converters in the continuous time domain is the most popular technique for these kind of applications, closely followed by SAR.

To prove scalability and enhance integration possibilities, the AFE was implemented in 65nm technology using a supply voltage of 1.2V.

This paper is divided into 9 sections. Section 2 provides the required background theory on ECG, $\Delta\Sigma$-converters and MOS-transistors. Section 3 cover the specifications for the ECG. In section 4, the design will be presented, followed by simulations in section 5 and discussions in section 6. Lastly, plans for future work is presented in section 7 before the appendix.

2 Theory

2.1 Electrocardiography and the cardiac cycle

An electrocardiogram, ECG or EKG, records the electrical activity of the heart through the detection of electrodes attached to the skin. It can be used to measure the heart rate, the regularity of heartbeats, and possesses the ability to detect damage to the heart. Depolarization causes the membrane potential of the heart's muscle cells to change as the heartbeat progresses. This change of potential can be detected as a voltage difference between an electrode pair, which is defined as a lead. The ECG can be made out of several leads in order to measure the heart from different angles which result in different outputs that can improve the mapping of the heart. For example, in the case of a MI[3], an ECG can identify if and where the heart muscle has been damaged.

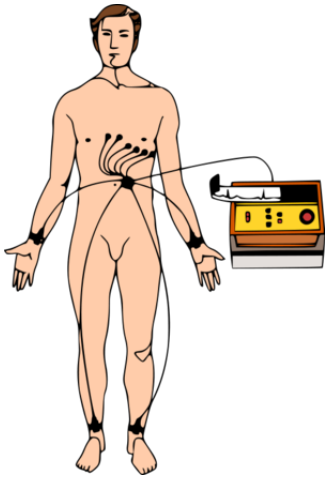
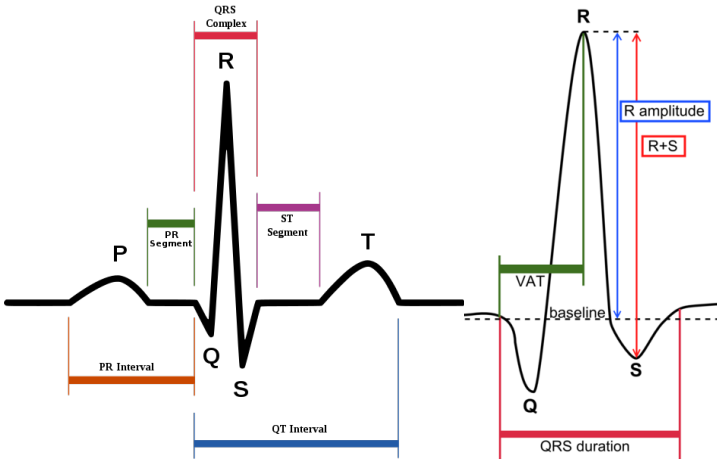


Figure 1: A patient connected to an ECG.

The output of the ECG, as seen in figure 2, describes the cardiac cycle, which consists of: a P-wave, a QRS complex, a T-wave and a U-wave. The U-wave is only visible in 50-75% of ECGs. Table 1, describes key parameters that define the frame of operation for the ECG, obtained from [1] and [2]. Tables 34, 35 and 36, describe the different time intervals in the cardiac cycle, various parameters of the QRS complex, and the different placement of leads; depicted in appendix C.

[3]Myocardial infarction



(a) The heart's sinus rhythm (b) The QRS complex

Figure 2: Schematic representation of ECG.

Feature	Description	Value
RR Interval	The interval between an R wave and the next. The normal heart rate is between 60 and 100 bpm[4]	0.6 to 1.2s ($\approx 1Hz$)
QRS amplitude	$\lvert S\rvert_{V_1} + \lvert R\rvert_{V_5}$ R+S in a precordial lead R in V5 or V6	< 3.5mV < 4.5mV < 2.6mV

Table 1: Key parameters of the cardiac cycle.

V_1 and V_5 represent two of the 6 precordial leads, which are placed directly on the chest.

The human body absorbs electric hum from power grids around us. This hum causes a large 50Hz[5] common mode, or offset, that can vary with several hundred milivolts.

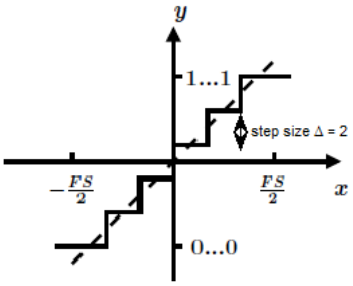
2.2 ADC fundamentals

An ideal analog-to-digital converter (ADC) performs essentially two tasks: sampling and quantization. The representation of the input signal in discrete time is normally obtained through periodic sampling. The periodic sampling frequency, f_s, must satisfy the sampling theorem in order to fully reconstruct the signal:

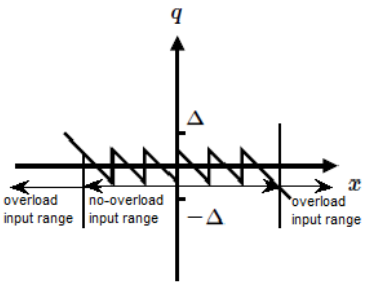
$$f_s \geq 2f_{BW} \tag{1}$$

[5]60Hz in America.

2.2.1 Quantization noise



(a) ADC transfer function, y-x.



(b) ADC quantization error, q-x.

An ADC takes discrete samples of an analog input and converts it into discrete levels at the output. For each sample a quantization error is made which is equal to the difference between the discrete output level and the actual input level. One least significant bit (LSB) is defined as the full scale range of convertible input signals divided by the resolution of the converter; $\Delta = 1\text{LSB} = FS/2^N$. The quantization error is bounded between $\pm\Delta/2$ and can be considered as uncorrelated white noise uniformly distributed between these bounds. The total quantization noise power can be calculated as:

$$\sigma_q^2 = \int_{-\infty}^{\infty} q^2 \cdot PDF(q) \cdot \mathrm{d}q = \frac{1}{\Delta} \int_{\Delta/2}^{\Delta/2} q^2 \cdot \mathrm{d}q = \frac{\Delta^2}{12} \tag{2}$$

2.2.2 ADC performance metrics

[3] provides a widely accepted basis for evaluating and comparing the performance of ADCs:

- **Signal-to-Noise Ratio (SNR)** is the ratio between the signal and the total noise power, excluding harmonics, within the maximum signal bandwidth. For an ideal ADC, the maximum SNR can be expressed as:

$$SNR = \frac{\frac{1}{2}\left(\frac{FS}{2}\right)^2}{\sigma_q^2} = 3 \cdot 2^{2N-1} \tag{3}$$

  Equation (3) can be expressed in terms of dB, and it is seen directly from (4) hat the SNR improves by 6dB for each additional bit:

$$SNR = 6.02N + 1.76[dB] \tag{4}$$

- **Signal-to-Noise-and-Distortion Ratio (SNDR)** is the ratio of the signal power to the noise power, including harmonics, within the maximum signal bandwidth.

- **Effective Number Of Bits (ENOB)** is the effective resolution relative to the SNDR:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{5}$$

- **Dynamic Range (DR)** is the ratio between the full scale input signal and the smallest detectable input signal (where SNDR=0).

- **Spurious Free Dynamic Range (SFDR)** is the ratio between the input signal and the highest noise component within the signal bandwidth. The noise component can be either a harmonic or quantization noise.

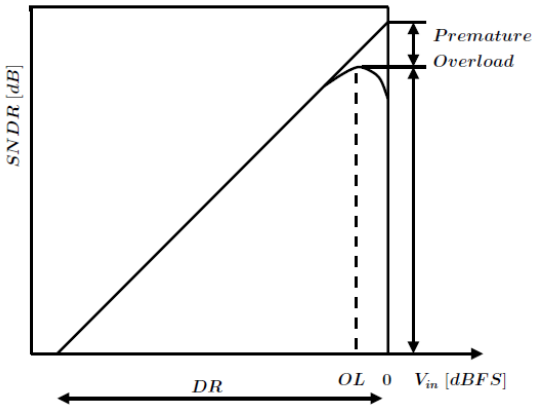


Figure 3: ADC SNDR versus input amplitude.

The figure above shows how the SNDR changes with the input signal amplitude. The premature overload is caused by increased harmonic distortion components.

2.3 Portable ECG circuits

Portable ECG circuits aim to perform low-power ECG signal acquisition combined with some signal processing and possibly wireless transmission of data. Figure 4 shows a typical block diagram of a portable ECG circuit.

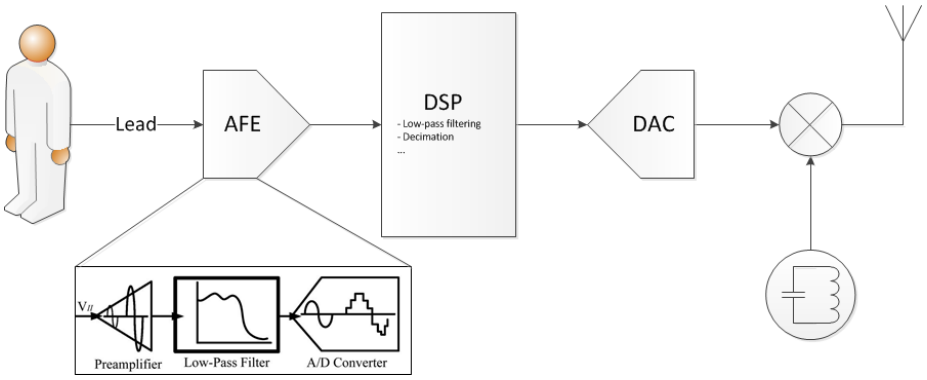


Figure 4: A typical portable ECG block diagram.

The analog front-end (AFE) is a critical component, where the most important parameters are cost, power, resolution, noise and area. The primary components of a traditional discrete ECG AFE include instrumentation amplifiers, operational amplifiers that implement active filters, and ADCs. Commonly, no less than 10-bits resolution ADCs are used in order to achieve a LSB greater than $50\mu V$. The electrodes may have motion artifacts and pacer impulses. In the presence of a pacer, software or dedicated hardware can be used to remove this interference. The software approach require higher bandwidth and ADC sampling rate. Based on the resolution of the ADC used in the signal chain, two different approaches are commonly used to process the ECG signal. The first approach is to use a low-noise, high gain preamplifier in front of the ADC. Such amplifiers usually have a gain of around 500. Both signal and noise gets amplified before a low resolution ADC of less than 14 bits convert the signal. The other approach is to use less preamplifier gain, typically in the order of 5, in front of a high resolution AGC. The preamplifier can be realized as a AGC[6] that is essentially a PGA[7] that is updated during runtime to keep the signal resolution nearly constant.

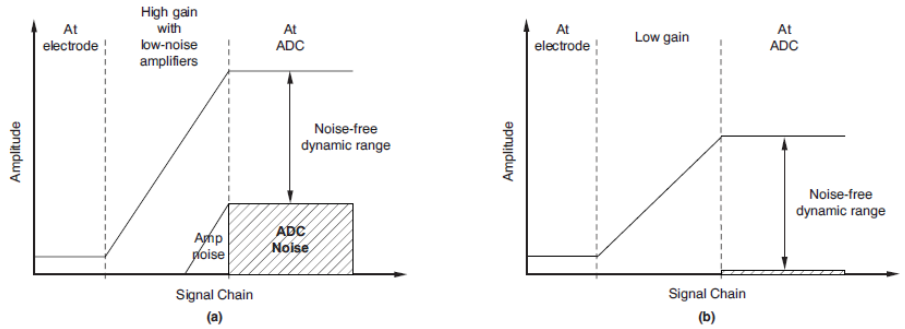


Figure 5: System approach based on ADC resolution.

[6]Automatic Gain Controller
[7]Programmable Gain Amplifier

The noise referred to the input of the system is the same in both cases. Most applications utilizing the first approach need a high-pass filter in front of the high-gain amplifier to ensure that DC components do not get amplified so that the ADC saturates. A good low-pass filter is required after the amplification to remove other components such as the 50Hz power-line interference. Alternatively the filters can be replaced with a low-noise band-pass filter in front. This might increase the input referred noise. The approach of using a low-gain preamplifier and a high resolution ADC allows for much more relaxation of the filters and preamplifier, and can also be used with low power supplies as a result of reduced signal amplification and hence less risk of saturation. However, the ADC needs higher resolution and thus becomes more difficult to design. SAR- and $\Delta\Sigma$-ADCs are most commonly used after preamplification and filtering. SAR-ADCs have the potential of extremely low power, whereas the $\Delta\Sigma$-ADCs benefit from scalability and robustness.

Some post-processing is normally performed on the output bit-stream after the ECG AFE. Whether maximum battery life or wireless transmission is the target of the application, minimizing the digital signal processing is essential in terms of power. For wireless systems, effective compression and information filtering/-pattern detection can be used to reduce the duty cycle of the RF-transmission.

2.4 $\Delta\Sigma$-Modulator fundamentals

A $\Delta\Sigma$-modulator is in its essence an active feedback filter composed of a high gain low- or band-pass loop filter, a quantizer and a feedback path. A $\Delta\Sigma$-modulator block can be seen in figure 6.

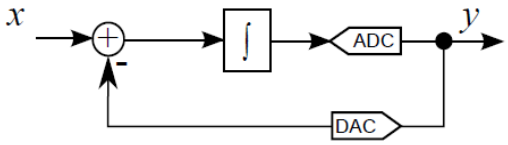


Figure 6: $\Delta\Sigma$-ADC block.

The modulator block performs a voltage-to-frequency conversion where the output represents the input signal as a pulse train. The frequency and density of the pulse train represent the frequency and amplitude of the input signal. The functional behavior of the $\Delta\Sigma$-ADC is that a low-frequency input signal is amplified and quantized. All noise is treated as a single noise source, the quantization noise. After the digital output is acquired, it is converted back into the analog domain through a DAC and subtracted from the input. After the subtraction, only residual quantization noise remains within the signal band, which can be further suppressed.

$\Delta\Sigma$-modulators have been gaining popularity, much due to their low cost, minimal power consumption and high fidelity. These modulators are frequently used as ADCs, DACs and frequency synthesizers. Through the combination of

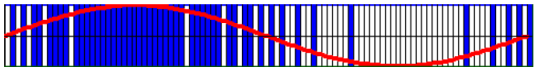


Figure 7: Voltage-to-frequency conversion using a 1-bit quantizer. Colored pulses represent 1's, white pulses represent 0's.

oversampling with noise shaping, a $\Delta\Sigma$ modulator can achieve high SQNR by spreading and shaping the noise into frequencies outside of the desired signal bandwidth. Digital post-filtering can then remove undesired frequency components outside the signal-band before a decimator performs downsampling to recover the input signal.

2.4.1 Noise shaping and oversampling

Equation (2) showed the noise power of an ADC. To see how a $\Delta\Sigma$-modulator can increase the SQNR, let us assume that the quantization noise is evenly spread across the Nyquist-band. We get that the PSD of the noise is:

$$PSD = \frac{\sigma_q^2}{f_s} = \frac{\Delta^2}{12 \times f_s} \tag{6}$$

Comparing the PSD of a Nyquist converter and an oversampling converter, where the oversampling ratio, OSR is defined as:

$$OSR = \frac{f_s}{2f_{BW}} > \pi \tag{7}$$

$$\sigma_{q,Nyquist}^2 = \frac{1}{2f_{BW}} \int_{-f_{BW}}^{f_{BW}} \sigma_q^2 \mathrm{d}f = \sigma_q^2 \tag{8}$$

$$\sigma_{q,OSR}^2 = \frac{1}{OSR \times 2f_{BW}} \int_{-f_{BW}}^{f_{BW}} \sigma_q^2 \mathrm{d}f = \frac{\sigma_q^2}{OSR} \tag{9}$$

Increasing the OSR, defined by equation (7), directly translates to the increased suppression of noise. If the OSR is lower than π, the system can be more nonlinear and unstable. Hence, an OSR lower than about 4 does not offer any advantage over Nyquist-sampling.

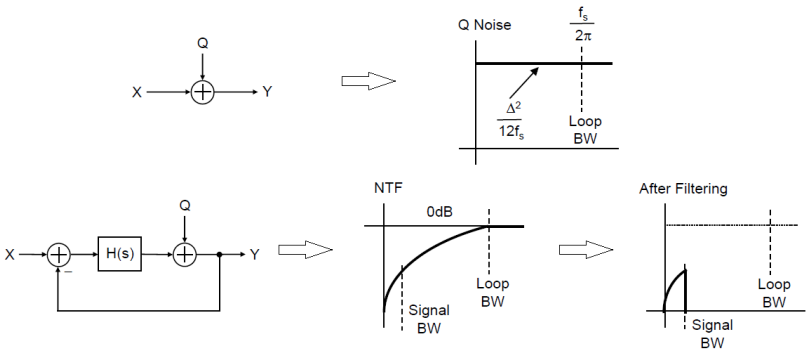


Figure 8: Noise shaping and digital filtering.

Figure 9, illustrates the shaping of the modulator's spectrum. As seen, the previous output is subtracted from the input before the residual spectrum is shaped by the filter, restoring the signal and suppressing noise.

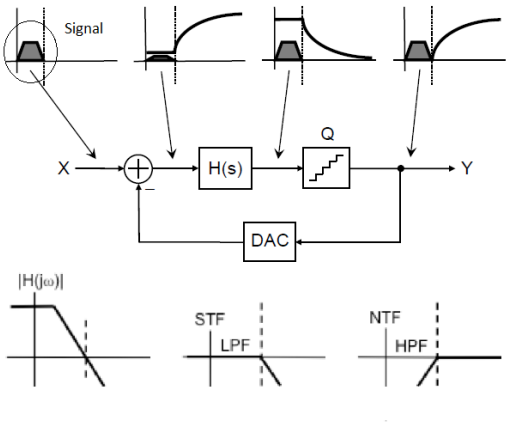


Figure 9: Spectrum shaping in $\Delta\Sigma$-modulator.

The transfer functions of the signal, X, and the noise, Q, are given by equations (10) and (11), respectively.

$$STF = \frac{H(s)}{1 + H(s)} \tag{10}$$

$$NTF = \frac{1}{1 + H(s)} \tag{11}$$

This implies that if we have a signal within the high-gain region of $H(s)$, it will pass without attenuation. The noise, appears after the filter, and it's corresponding transfer function is high-pass, implying that noise within the high-gain region of $H(s)$ is shaped.

Using a small-signal model we can obtain the relation in equation (12).

$$\begin{aligned} Y(s) &= STF \times X(s) + NTF \times Q(s) \\ &= \frac{H(s)}{1+H(s)} \times X(s) + \frac{1}{1+H(s)} \times Q(s) \end{aligned} \tag{12}$$

Where $X(s)$ is the input signal and $Q(s)$ is the quantization noise. If we assume that $H(s) \gg 1$ within the signal bandwidth, equation (12) can be further approximated to

$$Y(s) \approx X(s) + \frac{Q(s)}{H(s)} \tag{13}$$

Equation (13) suggests, that the shaping of the noise is more aggressive for a better filter. Ideally we want a block filter with infinite gain in the signal bandwidth.

Looking at the output noise in the frequency domain we have that:

$$S_q(f) = (2sin(\frac{\pi f}{f_s}))^L S_e(f) \quad , S_e(f) = \sigma_q^2 \tag{14}$$

If $S_q(f)$ is integrated over the bandwidth, the in-band noise power for an L^{th}-order filter can be approximated to be that of equation (15).

$$P_q = \frac{\pi^{2L}\sigma_q^2}{(2L+1)(OSR)^{(2L+1)}} \tag{15}$$

According to figure 8, the $\Delta\Sigma$-modulator shapes the quantization noise by means of an open loop transfer function filter, $H(s)$, with high DC gain and a negative feedback applied.

If we relate the signal power, given by equation (16), to the noise power in the means of dB, we can obtain a relation for the maximum achievable SQNR.

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 \tag{16}$$

$$
\begin{aligned}
SQNR_{max} &= 10log\left(\frac{P_s}{P_q}\right) \\
&= 10log\left(\frac{\Delta^2 2^{2N}}{8}\frac{12}{\Delta^2}\frac{(2L+1)}{\pi^{2L}}(OSR)^{2L+1}\right) \\
&\simeq 6.02N + 1.76 + 20L \times log\left(\frac{\sqrt[2L]{2L+1}}{\pi^{2L}}\right) \\
&\quad + (2L+1) \times 10log(OSR) \qquad [dB]
\end{aligned} \tag{17}
$$

The $SQNR_{max}$ for a 1^{st}- and 2^{nd}-order modulator is given by equation (18) and (19) respectively.

$$SQNR_{max,L=1} = 6.02N + 1.76 - 5.17 + 30log(OSR) \tag{18}$$

$$SQNR_{max,L=2} = 6.02N + 1.76 - 12.9 + 50log(OSR) \tag{19}$$

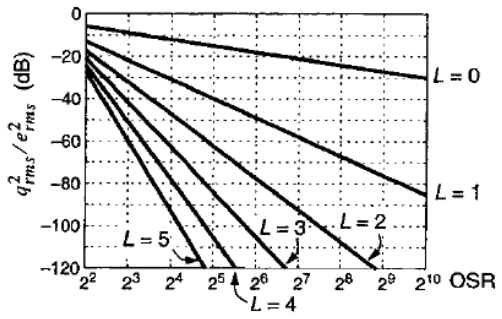


Figure 10: Theoretical in-band noise power for Lth-order $\Delta\Sigma$-modulator.

Figure 10 shows the theoretical attenuation of the noise. We can observe that doubling the OSR will increase the SQNR$_{max}$ by $(2L+1) \times 0.5$ bits/octave, or $3dB + L \times$ 6dB per octave. This value corresponds to:

- 0.5 bits (3dB) per octave if no noise shaping is used.
- 1.5 bits (9dB) per octave for a 1^{st}-order filter.
- 2.5 bits (15dB) per octave for a 2^{nd}-order filter.

Hence, equation (17) indicate that the noise is attenuated harder if a higher order filter is used, the OSR is increased, and the quantization level is reduced by increasing the number of bits in the quantizer.

2.4.2 The loop filter

As described, the resolution can be improved by cascading integrator stages. For each stage, we introduce a new DC pole which needs to be compensated in order to maintain stability. 1^{st}- and 2^{nd}-order stage filters can be stabilized by introducing one feed-forward zero, but stabilizing higher order filters can be challenging as a consequence of the need for more zeros and scaled gain. Also, to compensate for the reduced loop filter gain at the signal band edge compared to the DC gain, one can introduce non-imaginary poles to keep the gain high over the signal band by implementing resonators. Unfortunately, because of the two poles that is introduced per resonator, the loop can become unstable.

A critical parameter in the design of $\Delta\Sigma$-modulators is the unity-gain bandwidth, f_{ug}. Higher f_{ug} results in a greater in-band filter gain, but also makes the feedback loop more non-linear and may cause instability. An optimal value for the f_{ug} can be derived from the z-domain transfer function of the DT integrator:

$$\begin{aligned} H(z) =& \frac{z^{-1}}{1-z^{-1}} \\ \Rightarrow H(j\omega)|_{z\to j\omega T} =& \frac{1}{e^{j\omega T}-1} \\ =& \frac{1}{\{1+j\omega T+\frac{(j\omega T)^2}{2!}+\frac{(j\omega T)^3}{3!}+\cdots\}-1} \end{aligned} \tag{20}$$

Where T is the sampling period. As a result of the oversampling we can use the approximation that $\omega T << 1$ which gives:

$$H(j\omega) \approx \frac{1}{j\omega T} \tag{21}$$

The NTF then becomes $(1-z^{-1})$, which is the delay-and-subtraction equivalent to the differentiator transfer function of $j2\pi fT$ or $j2\pi f/f_s$ in the frequency domain. The optimum f_{ug} can therefore be related to the sampling frequency in both CT and DT integrators by equation (22).

$$f_{ug,optimal} = \frac{1}{2\pi RC} = \frac{f_s C_s}{2\pi C} = \frac{1}{2\pi T} = \frac{f_s}{2\pi} \tag{22}$$

With a relation between f_{ug} and f_s, an expression relating the OSR to f_{ug} can be derived from equation (7) and (22).

$$OSR = \frac{f_s}{2f_{BW}} = \frac{\pi f_{ug}}{f_{BW}} \tag{23}$$

2.4.3 Stability

In addition to the linear small-signal analysis for stability condition, it is also necessary to consider integrator overloading, which is caused by large quantization errors. Overloading or clipping of the integrators causes the feedback loop to become momentarily disabled. Hence, all systems, even non-linear ones, should be operated within the linear range of the integrators. For a linear system to be stable, poles should be placed in the open left-half complex s-plane, or equivalently the phase margin should be greater than zero at the unity loop-gain frequency.

2.4.4 1^{st}- and 2^{nd}-order $\Delta\Sigma$-modulators

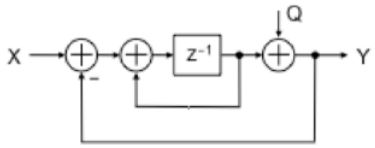


Figure 11: 1^{st}-order $\Delta\Sigma$-modulator.

The 1^{st}-order $\Delta\Sigma$-modulator, as show in figure 11, has the advantage of simplicity, robustness and stability. As long as the input signal, x, is within the range of the feedback DAC, stability is ensured due to the fact that the loop gain decreases by 6dB/octave and that the loop-phase is $-90°$.

Performing a linearized analysis of figure 11, we obtain the relation in equation (24).

$$Y(z) = X(z) + (1 - z^{-1})Q(z) \tag{24}$$

There are some drawbacks with the 1^{st}-order modulator: The resolution achievable from a single integrator is limited, and with the generation of idle-tones (see appendix B), it often becomes inadequate for the desired application. A second order can be introduced to help overcome these shortcomings. This is performed simply by replacing the first quantizer in the 1^{st}-order modulator by a replica of the modulator itself.

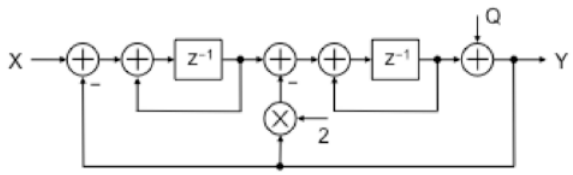


Figure 12: 2^{nd}-order $\Delta\Sigma$-modulator.

Modeling the 2^{nd}-order modulator in the linear z-domain model results in equation (25).

$$\begin{aligned} Y(z) =& Q(z) + \frac{1}{1-z^{-1}}\left(-z^{-1}Y(z) + \frac{1}{1-z^{-1}}[-z^{-1}Y(z) + X(z)]\right) \\ & \frac{(1-z^{-1})^2 Q(z) - [(1-z^{-1})z^{-1} + z^{-1}]Y(z) + X(z)}{(1-z^{-1})^2} \\ =& X(z) + (1-z^{-1})^2 Q(z) \end{aligned} \tag{25}$$

As indicated earlier, we expect that the quantization noise should be attenuated more than in the case of a 1^{st}-order modulator as the noise transfer function becomes $NTF(z) = (1-z^{-1})^2$.

Inevitably, the 2^{nd}-order modulator has its disadvantages, such as; more hardware, a slightly reduced signal range, and more care must be taken to ensure stability. The simplest way to ensure stability is to have a gain-of-2 in the feedback path that bypasses the first integrator. Figure 13 shows the the loop filter with feedback scaling coefficients. Essentially, the coefficient scaling is a trade-off between stability and bandwidth/resolution. Coefficient a_2 creates a first-order feedback path. If $a_1 = 1, a_2 = 0$ we see that the filter will give a pure second order noise-shaping. For $a_1 = 0, a_2 = 1$ a pure first order noise-shaping is created. A smaller a_2 provides better quantization noise suppression but lower maximum stable input level. If a_2 is chosen too small, the delta-sigma modulator will exhibit very low oscillation frequencies even for very small input signals, causing instability. A large a_2 provides less quantization noise suppression but a higher maximum stable input level.

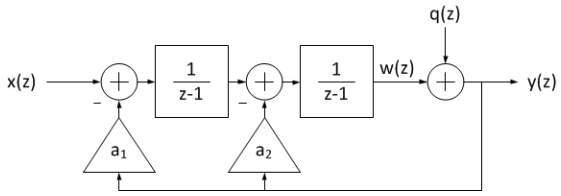


Figure 13: 2^{nd}-order loop filter coefficient scaling.

2.4.5 Summary of architectural choices and design techniques

Some other techniques for increasing the resolution of $\Delta\Sigma$-modulators include introducing multi-bit quantizers and using Multi-Stage Noise-Shaping (MASH) instead of high order loop-filters. The use of multi-bit quantizers will increase the quantization noise suppression and also reduce out-of-band-gain (OBG or NTF_{max}). Unfortunately, the multi-bit quantizer creates a new pole that needs to be compensated. Also, the multi-bit feedback DAC that is required suffers from mismatch which cause non-linearity. This effect can be observed in the FFT as a flattening of the quantization noise suppression below a level of magnitude in addition to introducing harmonics. Using MASH can be preferable

since MASH-DSMs are easier to stabilize than high-order filters. Coefficient mismatch in the different stages will reduce the order of noise-shaping for lower frequencies, i.e. a 2-1-1 MASH with mismatch will experience a ,2^{nd}-order (40dB/dec) noise-shaping at low frequencies instead of a 4^{rd}-order (80dB/dec) noise-shaping. Also, distributing in-band zeros in terms of resonators can increase the in-band NTF gain significantly.

Finally, depending on the weighing of drawbacks from the various blocks (such as the DAC), the filter can be realized either in continuous-time or discrete-time.

In summary, the resolution of the $\Delta\Sigma$-modulator can be increased by applying the following architectural techniques:

- **Increasing** f_s - Limited by stability due to parasitic poles and quantizer/DAC latency.
- **Optimizing the NTF gain** - Limited by stability.
- **Increasing the loop-filter order** - Not effective at low OSR due to stability.
- **Optimizing NTF zero locations**
- **Increasing the number of quantization bits** - Limited by matching accuracy of DAC (and quantizer).
- **Cascading multiple modulators and quantization error cancellation** - Limited by matching of analog and digital filters.

2.4.6 Continuous-Time $\Delta\Sigma$-modulators

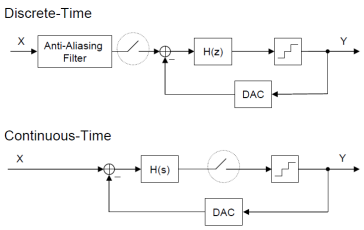
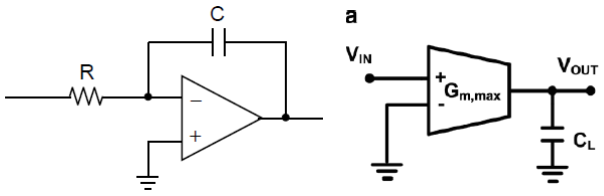


Figure 14: Discrete-Time versus Continuous-Time modulator.

The active loop filter can be implemented in both CT and DT domain. In the case of the DT, the S/H appears before the modulator, therefore an anti-aliasing filter is needed in front of the modulator. For the CT case, the S/H appears in front of the quantizer; hence the filter itself performs the anti-aliasing function. In regards to a DT system, high sampling resolution is required, which makes it sensitive to clock jitter. Comparatively, this is not much of a problem in a CT system, since clock jitter only affects the low-resolution quantizer which is placed after the filter. Due to the variations in the filter coefficients, the

CT modulator often need tuning and/or calibration. Furthermore the DAC pulse design is more important than in a DT modulator. Another drawback of the CT modulator is the signal-dependent loop delay that is caused either by comparator metastability or hysteresis.

A favorable feature of the CT modulator is that basically any sampling-related non-ideal error, such as clock jitter, aperture and non-linearity, are reduced by the loop filter gain when referred to the input. In terms of this project, the most attractive feature of the CT modulator in comparison to the DT modulator, is that power consumption can be lowered as a result of the inherent filtering and no need for high voltage switching. Jitter in the DAC feedback path is critical in CT-DSM, as is its linearity and that of the front-end integrator. The filter can be implemented using both RC and $G_m - C$ integrators. The linearity and high-swing requirements are easier to meet using an RC integrator due to less sensitivity to PVT variations. However, the G_m-C integrators use lower power.



(a) RC integrator (b) G_m-C integrator

Figure 15: CT integrators.

2.5 MOSFET devices

With increasing demand for optimized low-voltage, low-power circuits, operating MOSFET devices in moderate to weak inversion have become essential. A brief review of MOSFET physics and an introduction to the all-region EKV model can be found in appendix A and [4]. Based on [5], various trends and characteristics of the MOSFET have been analyzed to aid in the optimization of each device. Mismatch, gain and leakage in 65nm technology, as applied here, will also be addressed.

From appendix A we have that in the charge based symmetric EKV MOS transistor model, the channel current is defined as the sum of the forward and reverse current:

$$I_D = I_F - I_R \tag{26}$$

Where,

$$I_{F(R)} = I_S \ln^2 \left(1 + e^{\frac{V_P - V_{S(D)}}{2U_T}} \right) \cong I_S \ln^2 \left(1 + e^{\frac{V_G - V_{T0} - nV_{S(D)}}{2nU_T}} \right) \tag{27}$$

$$\begin{aligned} U_T &\equiv \frac{kT}{q}, \qquad n \equiv \frac{C_{ox} + C_{dep}}{C_{ox}}, \qquad V_P \equiv \frac{V_G - V_{T0}}{n} \\ C_{dep} &\equiv \frac{\epsilon_{Si}}{W_{dep}}, \qquad I_S \equiv 2n\mu C_{ox} \frac{W}{L} U_T^2 \end{aligned} \tag{28}$$

The normalized current is given by $i_{f(r)} = \dfrac{I_{F(R)}}{I_S}$ and can be inverted to express voltages instead of currents:

$$v_p - v_{s(d)} = \frac{V_P - V_{S(D)}}{U_T} = 2\ln\left(e^{\sqrt{i_{f(r)}}} - 1\right) \tag{29}$$

The overdrive voltage has been replaced with an all-region inversion coefficient, IC, which is defined as:

$$IC = max(i_f, i_r) \tag{30}$$

The different regions of operation in saturation can be defined as weak inversion if $IC < 0.1$, moderate inversion if $0.1 < IC < 10$, and strong inversion if $IC > 10$.

With a standard for inversion and an all level representation of voltages and currents, the following region characteristics and trends have been found [6]:

- V_{DSsat} approaches its minimum in weak inversion, where $V_{DSsat} \cong 4 \sim 5U_T$. In this region, the saturation voltage is independent of the threshold voltage, which explains why weak inversion is intrinsically associated with low voltage circuit design.
- g_m/i_d is maximum and almost constant in weak inversion.
- **Channel noise** is largest in weak inversion where the noise is shot noise of both forward and reverse currents with a maximum value of:

$$S_{\Delta I^2_{nD}} = 2qI_D = 4kT\frac{g_{ms}}{2} \tag{31}$$

  In strong inversion the channel noise is given by:

$$S_I = \frac{8}{3}nkTg_m \tag{32}$$

- **Flicker noise** is almost bias independent, and given by:

$$S_{\Delta V^2_{nG}} \cong \frac{KF}{C^n_{ox}WLf} = 4kT\frac{\rho}{WLf}, \qquad \rho = \frac{KF}{4kT \cdot C^n_{ox}} \tag{33}$$

  Measurements [7] show that the flicker noise approaches a minimum for $IC \simeq 0.1$ 1. For very strong or weak inversions the flicker noise increase with a factor of around 10 from moderate inversion.
- **The total harmonic distortion,** $THD \propto \frac{g_m}{i_d} \propto \frac{1}{IC}$ follows the g_m/i_d curve and is strongly degraded in weak inversion compared to strong inversion.
- **Matching of drain current and threshold voltage** is also of interest when choosing biasing conditions for devices. It can be shown that the RMS drain current mismatch $\delta I_D/I_D$ of two transistors with the same V_G, is given by :

$$\sigma_{ID} = \sqrt{\sigma^2_\beta + (\frac{g_m}{I_D}\sigma_{VT})^2} \tag{34}$$

  If the drain current is fixed, then the gate voltage mismatch is given by

$$\sigma_{V_G} = \sqrt{\sigma^2_{VT} + (\frac{I_D}{g_m}\sigma_\beta)^2} \tag{35}$$

  Where σ_{VT} is the RMS value of the threshold mismatch and σ_β is the RMS value of the minimum current mismatch. Since the g_m/I_D-ratio is greater in weak inversion than in strong inversion, it can be seen directly that transistors operated in weak inversion achieves the lowest gate voltage mismatch, but also the greatest drain current mismatch.

  With regards to technology downscaling it can be shown that the threshold voltage mismatch improves as T_{ox} decrease[8]. Since 40nm and 65nm

utilize the lowest oxide thicknesses, it is expected that the offset will be better than in other technologies. Also, the improved matching in 65nm technology compared to larger technologies implies that the comparator offset in ADCs can decrease.

- **Drain Induced Barrier Lowering (DIBL)** can significantly increase the drain current in weak inversion. It increases the output conductance in weak inversion and slightly reduces the transconductances, decreasing the maximum voltage gain indicating that intrinsic gain should peak in moderate inversion.

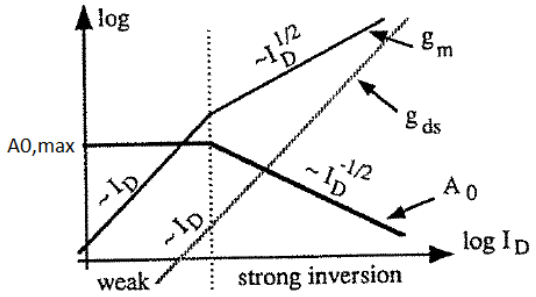


Figure 16: Change of gain, g_m, g_{ds} and inversion with respect to I_D, not accounting for DIBL.

It can be shown that operating in moderate inversion is a good trade-off for having at the same time high current efficiency and maximum gain for a given current [9].

- V_T **matching degradation due to pocket implants** increase with the channel length. For short channels, the mismatch is almost constant, while for long channel devices, A_{VT} is degraded and dependent of $v_g - v_t$.

2.5.1 Gate leakage

As the technologies have been scaled down in area, so has the oxide thickness of the gates to increase the gate capacitance and consequentially the drive current. For technologies beyond 65nm, such as Intel's 45nm technology, high-k metals like hafnium have been used to replace the silicon dioxide so that T_{ox} can be increased while still having a higher gate capacitance due to their higher dielectric constant, κ. Table 2 shows typical behavior of a S_iO_2 90nm process versus a potential high-k process:

T_{ox}	1.2nm S_iO_2	3nm high-k
C_{ox}	1×	1.6×
I_{gate}	1×	0.01×

Table 2: Typical capacitance and leakage ratios between a S_iO_2 and a high-k process.

Figures 17 and 18 indicate the expected trend of gate leakage for a transistor with $A_{gate} \approx 10\mu m^2$.

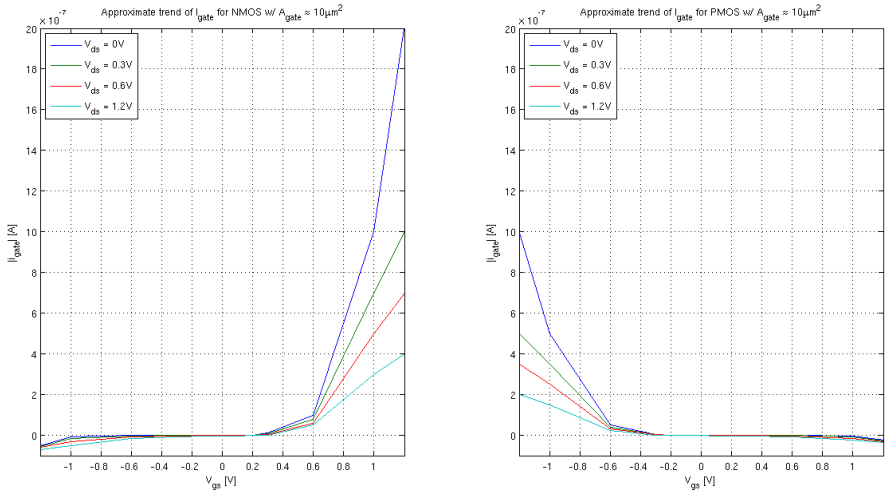


Figure 17: I_{gate} for V_{ds} versus V_{gs}.

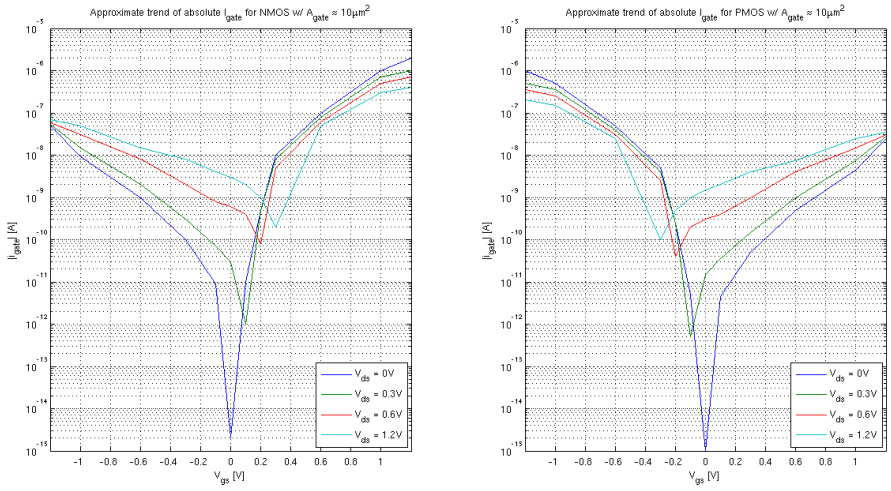


Figure 18: Absolute I_{gate} for V_{ds} versus V_{gs}.

The large majority of gate leakage consists of gate-to-channel leakage. The gate leakage increase exponentially with V_{gs} and $\frac{1}{V_{ds}}$. Also as V_{ds} increases, the V_{gs} that cause an absolute minimum leakage increases.

3 Circuit specification

AAMI[8] has made a standard which can be used as a guideline to define the specifications of electrocardiographic systems. From [10], the following specifications are found:

- The ECG should be able to detect a $50\mu V$ input signal. The input referred peak noise, $V_{n(pp)}$, of the system should therefore not exceed $50\mu V$.
- The ECG signal typically ranges from $100\mu V$ to $5mV$.
- The ECG should have a large input dynamic range. A $5mV_{pp}$ signal shall be measured with offsets up to $\pm 200mV$.
- A $6mV_{pp}$ signal should be converted with $\gtrsim$ 43.5dB resolution.
- $R_{in} > 10M\Omega$.
- The signal should be filtered to remove frequencies below 0.67Hz and above 100Hz. The electric hum should also be filtered.
- Other specifications are also used. [11] deal with a $\pm 300mV$ electrode offset, and $30\mu V_{ni(RMS)}$.

A SNDR of 54dB is typically required for 10-bit ADCs. A 10-bit system was chosen to reduce the amount of data generated in order to save power from DSP and RF. Also, a full scale reference of 50mV was chosen to provide headroom enough to ensure that instability won't be caused by the input signal (remembering the stability condition derived in section 2.4.4). With a full scale reference of 50mV, we get that a DR of 60dB is required if 50μV signals are to be detected. To relax the requirements for the OTA and reduce the effects of idle tones, using a second order filter seems favourable. Furthermore, using a 1-bit quantizer relax the requirements for the DAC and are easier to stabilize. By assuming that an ideal $2^{nd} - order$, 1-bit $\Delta\Sigma$-ADC with only quantization noise, we can find that the OSR should be larger than:

$$OSR > 10^{\frac{60 - 6.02 - 1.76 + 12.9}{50}} = 20 \tag{36}$$

A summary of the specifications are given in table 3.

[8] Association for the Advancement of Medical Instrumentation

SNDR	>54dB
Resolution	10-bit
Bandwidth	$\sim 100Hz$
$\lvert V_{in}\rvert$	$\leq 6mV$
$\lvert V_{offset}\rvert$	250mV
$V_{ni(pp)}$	$\lesssim 50\mu V$
f_{in}	0.67Hz to 40Hz
P_{total}	$< 20\mu W$
R_{in}	$10M\Omega$
Area	Minimize

Table 3: ADC Specifications

The large time-constants needed to satisfy the low-frequency operation require large capacitors. Also, since small currents and voltages are used, most transistors will have to operate in moderate or weak inversion where noise is increased. Since very low input referred noise is required, the gate area of transistors has to be large. Area should be minimized, but needs to be sacrificed in order to achieve the application specifications. Enough overdesign should be done to accommodate other noise sources as well. Doubling the OSR for a second order DSM translates to a 15dB increase in SQNR. Using an oversampling rate of 40 translates to a $\text{SQNR}_{max} = 75$dB and should be sufficient for a 10-bit resolution. A 100Hz bandwidth is chosen to make the ECG flexible. With an OSR of 40, the sampling frequency, f_s, then becomes 8kHz. The ADC is to be made in a 65nm technology with $V_{DD} = 1.2V$ and the power consumption should be minimized.

Table 4 shows some architectural specs of the $\Delta\Sigma$-ADC.

Technology	65nm
V_{DD}	1.2V
$V_{ref(FS)}$	50mV
OSR	40
Order	2
f_s	$8kHz$
N_Q	1

Table 4: DSM specifications

From equation (22) we get $f_{ug} \simeq 1273Hz$. A target phase margin of 60° was chosen to have a good trade-off between bandwidth and stability. A 100nA reference current is used, but each OTA was chosen to consume 400nA (or 200nA per branch) for reliability. For linearity, the input transistors in the OTA will be degenerated with a $1M\Omega$ resistor. Table 5 shows the summary of the loop-filter and OTA specifications.

f_{ug}	1273Hz
PM	$60°$
I_{ref}	100nA
$I_{tail,OTA}$	400nA
R_S	$1M\Omega$

Table 5: Loop filter and OTA specifications

Because the ECG ADC is aimed for portable use on patients and in close perimeter to the body, it is expected that the system seldom will be exposed for temperatures outside $25 \pm 25°$C. The variations in performance for the ADC should be minimal within this temperature range.

3.1 Noise

Noise sources in a $\Delta\Sigma$-converter includes intrinsic noise generated by the devices in the circuit, but also extrinsic noise normally picked up from on-chip digital circuitry via the substrate. The total noise at the loop-filter output can be expressed as a sum of the various noise sources. An estimate for the total noise can be made to see if the second order DSM is capable of meeting the performance specifications. The conditions in table 3 have been assumed.

3.1.1 Quantization noise

It was found that the maximum SQNR achievable by the DSM is 75dB.

The full scale signal power is:

$$P_S = (\frac{50mV \times 2^1}{2\sqrt{2}})^2 = 1.25mV^2 \tag{37}$$

SQNR_{max} then becomes:

$$P_{Q_{min}} = \frac{1.25mV^2}{75dB} \simeq 39.53pV^2 \tag{38}$$

3.1.2 Intrinsic noise

The relationship between peak-to-peak input referred noise voltage and RMS input referred noise voltage is defined as:

$$V_{ni(pp)} = \sigma \times V_{ni(RMS)} \tag{39}$$

The value of σ specifies the certainty of how often a noise voltage will exceed $V_{ni(pp)}$. Most commonly $\sigma = 6.6$ is used, which translates to 99.9% of all noise

occurrences falling within $V_{ni(pp)}$. This gives that the input referred RMS noise voltage should be smaller than:

$$V_{ni(RMS)} = \frac{V_{ni(pp)}}{\sigma} \simeq 7.58\mu V \tag{40}$$

The input referred noise power becomes:

$$P_{ni} = V_{ni(RMS)}^2 \simeq 57.39pV^2 \tag{41}$$

3.1.3 Extrinsic noise

The signal bandwidth of the ADC is limited to a 100Hz. Also, noise from digital circuitry is primarily high frequent. Therefore, extrinsic noise such as substrate noise from digital circuitry should not affect the noise performance of the ADC much. A budget of 5% noise contribution from extrinsic sources have therefore been assumed.

3.1.4 Total noise floor

The total noise floor, excluding harmonics, can be estimated as the sum of quantization noise, intrinsic noise and extrinsic noise:

$$P_{n,tot} = P_Q + P_{ni} + P_{ex} \tag{42}$$

With $P_Q \simeq 39.53pV^2$, $P_{ni} \simeq 57.39pV^2$ and P_{ex} contributing to 5% of the total noise, we get that:

$$P_{n,tot} \simeq 102pV^2, \qquad P_{ex} \simeq 5.1pV^2 \tag{43}$$

In figure 19 the theoretical SNR versus V_{in} has been plotted, assuming that no harmonics are present.

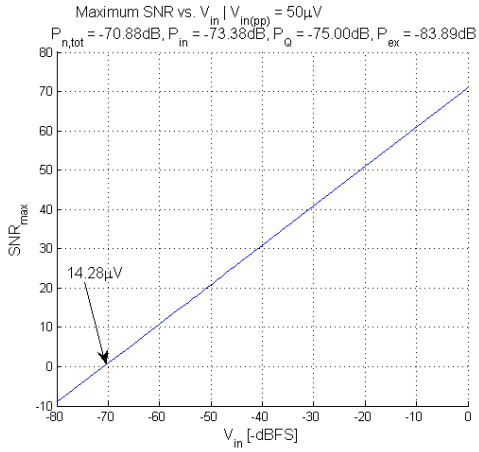


Figure 19: Ideal SNR with $50\mu V_{ni(pp)}$.

If we assume that P_Q and P_{ex} remain constant, we can find the maximum input referred RMS noise where the ADC can convert a $50\mu V$ input signal with 0 SNDR. However, for $V_{ni(RMS)} \gtrsim 7.58\mu V$, the ADC may produce $V_{ni(pp)} > 50\mu V$, which means that the signal may not be detectable.

$$P_s|_{V_{in}=50\mu V} - P_Q - P_{ex} = P_{ni}|_{max} \simeq 1.2nV^2 \tag{44}$$

$$V_{ni(RMS)}|_{max} = \sqrt{P_{ni}|_{max}} \simeq 34.72\mu V \tag{45}$$

$$V_{ni(pp)}|_{max} = 6.6 \times V_{ni(RMS)} \simeq 229.14\mu V \tag{46}$$

The input referred RMS noise voltage of the ADC should never exceed $34.72\mu V$, and should preferably be lower than $7.58\mu V$. Also because the quantization noise will be greater in a non-ideal system, the input referred noise should be aimed at being even lower. In conclusion, the noise has been over-budgeted with about 10dB, which should make the target specifications realistic to meet for a second order, 1-bit DSM with an oversampling rate of 40.

3.2 Digital post-filtering

The digital post filter and decimation specification is shown in figure 6

Input data width		1 bit
Input data rate		8000Hz
Output data width		10 bits
Output data rate		100Hz
Decimation rate		40
attenuation	$0.67Hz - 1Hz$	max. 3dB
	$1Hz - 40Hz$	max. 0.5dB
	$60Hz - 450Hz$	min. 85dB
	$450Hz - 4kHz$	min. 85dB
zeros		0Hz and 50Hz

Table 6: Digital filter specification.

The attenuation from 60Hz to 450Hz is needed to suppress disturbances from muscle activity. The filter specifications follows the standard in [10].

4 Design

4.1 Simulation tools and methodology

For design in UMC's 65nm technology, Cadence' Virtuoso Platform was used, which provides tools such as schematic entry, circuit simulation, layout and extraction. The EKV model combined with the g_m/I_D-methodology has been used to replace the square model to accommodate devices operating in weak and moderate inversion. Mapping of operating points for both NMOS and PMOS devices with different V_{th} was done to provide lookup tables that can be used to define transistor sizes. A great feature of operating with sub-μ bias currents is that unless very small W/L-ratios are used, transistors will be operating in moderate and weak inversion. In these regions, $\frac{g_m}{g_{ds}}$ is almost constant, and both are linearly proportional to I_D. This allows for fast and simple estimations of circuit behavior. From the script in appendix E it was found that the intrinsic gain of PMOS and NMOS devices are approximately the same with a slight favor for NMOS transistors. The maximum gain occurs in moderate inversion, and are in the order of 20 for low threshold devices, 40 for normal threshold devices, and 100 for high threshold devices.

4.2 Architecture and concept

A 2^{nd}-order $\Delta\Sigma$-ADC with a 1-bit quantizer and an OSR of 40 was implemented. The loop filter was realized using telescopic OTAs. A pseudo-differential signal path was chosen to reduce current consumption from biasing circuits, remove DC components, and to eliminate the need for a CMFB circuit. The goal of the chosen architecture is to combine the entire AFE into the $\Delta\Sigma$-ADC. By using a CT-DSM, the need for anti-aliasing and prefiltering is eliminated (see section 2.4). Second, by combining the input OTA of the first integrator with a AGC, the ECG AFE can be relieved of a dedicated preamplifier. The architecture takes full utilization of the continuous time loop filter and offers some unique features in terms of power, simplicity and robustness. Additional documentation on noise, small-signal analysis, scaling considerations and more can be found in appendix 10 and 9. A schematic overview of the entire ADC is depicted in figure 20.

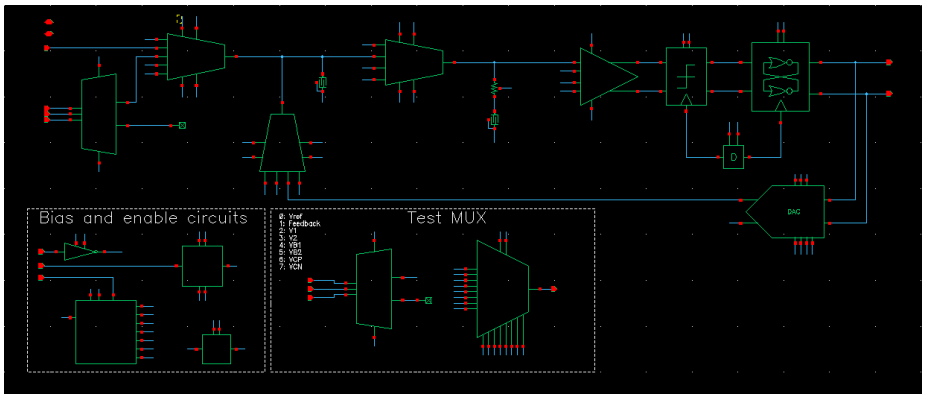


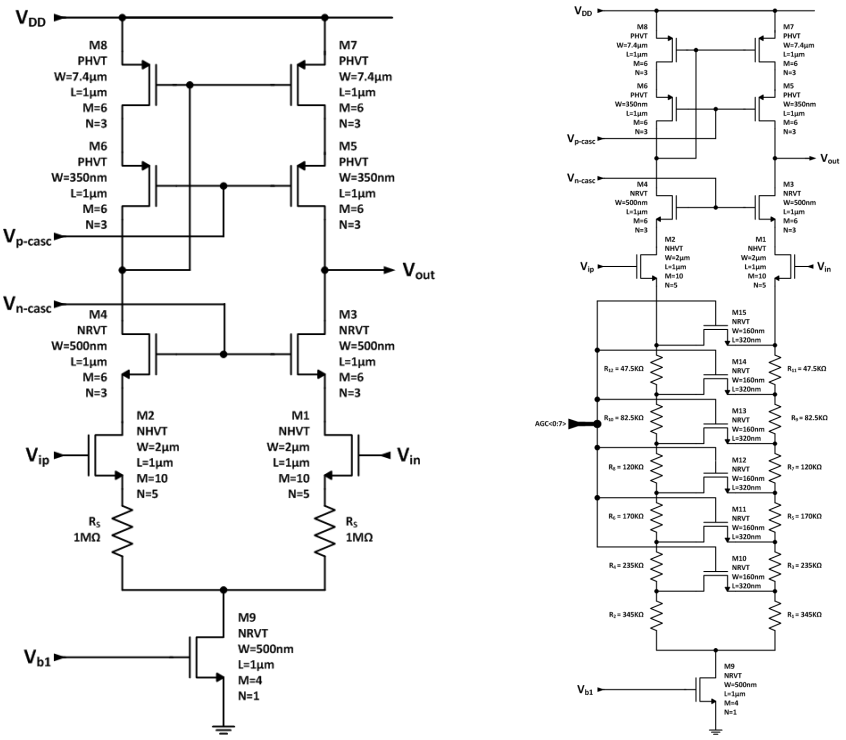
Figure 20: Schematic of the ADC in its entirety including a test MUX.

4.3 Loop filter

As specified, a target f_{ug} of 1273Hz and a PM of 60° was chosen in order to achieve a good trade-off between resolution and stability. A G_m-C filter was implemented to save more power and because OpAmps may not be able to drive the large resistors needed. Instead of implementing a first-order loop as in figure 13, the feedback OTA (a2) was replaced with a series resistor, R_Z that creates a zero around $A_{v,ol} = 2$. By using R_Z both area and power is saved. Also the output resistance of the second integrator gets reduced by 2 in the presence of a feedback OTA, so using a resistor instead also increases the loop gain by 6dB.

4.3.1 OTA and AGC

NMOS input transistors were used in the OTAs because it can be shown that they exhibit less flicker noise than their PMOS equivalents after a certain gate area, and the flicker noise is less dependent on bias current [12]. The cascodes are passively biased to reduce power consumption. The PMOS load has been scaled primarily with regards to minimize noise while still providing a large load resistance, R_L. The PMOS cascodes have been scaled to maximize the load resistance. Because three NMOS devices plus a 200mV headroom consumption by R_S are to be stacked under V_{CM}, these devices have been carefully scaled to optimize their operating conditions. The AGC was realized by dividing the source degenerating resistor, R_S, into segments that can be shorted in order to move AC ground. This effectively reduces the source degeneration, increasing the G_m of the AGC. Figure 21a and 21b depicts the schematics of the OTA and AGC, respectively.



(a) Telescopic OTA (b) AGC

Figure 21: Schematic of OTAs

The effect of varying the source degeneration of the AGC can be seen in equations (47), (48) and (49).

$$G_{m,AGC} \simeq \frac{g_{m1}}{1 + g_{m1}R_S} \tag{47}$$

$$G_{m,AGC}|_{R_S=1M\Omega} \simeq \frac{g_{m1}}{1 + g_{m1} \times 1M\Omega} \tag{48}$$

$$G_{m,AGC}|_{R_S=0\Omega} \simeq g_{m1} \tag{49}$$

For minimum AGC gain, $G_{m,AGC} = G_{m,OTA}$ and the signal loop gain is 1 for frequencies up to around f_{ug}. However, as $G_{m,AGC}$ is increased, the unity gain bandwidth seen from the AGC increases, and also the signal loop gain increases with a ratio of:

$$A_{v,STF} = \frac{G_{m,AGC}}{G_{m,OTA}} \tag{50}$$

Similarly, reducing the source degeneration also reduces the resistance looking into the drain of the NMOS cascode, R_D, and causes the loop gain to vary with AGC setting, which by the use of a telescopic OTA can be minimized.

The AGC gain is set by decoding a 3-bit word. For future reference, AGC gain settings will be used when discussing the condition of the AGC. The code word and its corresponding gain is listen in table 7.

AGC gain	
000	0dB
001	3dB
010	6dB
011	9dB
100	12dB
101	15dB
110	17dB

Table 7: AGC gain setting and the corresponding $A_{v,STF}$ in dB.

The transistors in the OTA consist of arrays of $M \times N$ unit transistors in order to increase gate area and reduce the flicker noise. The large sizes and arrays also helps improve the matching and reduce gate offset. The current mismatch will be increased since neither input or load transistors are operated in strong inversion. A more thorough analysis of the telescopic OTA is shown in appendix 10.

4.3.2 Integrator scaling

The first integrator was scaled by varying C_1 to contain a -6dBFS input signal within the feedback reference in order to increase the peak SNDR of lower input voltages. C_2 and R_Z was scaled to meet the target f_{ug} and phase margin. The final sizes and typical loop response have been listed in table 8.

C_1	117.038pF
C_2	136.554pF
R_Z	1.45525MΩ
f_{ug}	1272Hz
PM	60.1°

Table 8: Final scaling coefficients and open loop responses.

4.4 Preamplifier

A fully differential preamplifier with a triode CMFB was realized to reduce kickback and to provide a good compromise between power and performance. The schematic can be seen in figure 22.

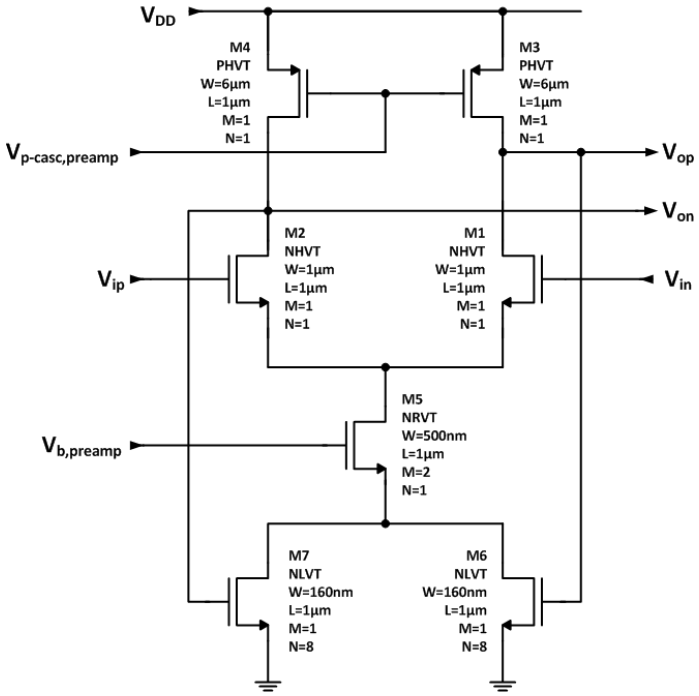


Figure 22: Schematic of fully differential preamplifier

The differential pair have been scaled for maximum gain using high threshold devices, while the triode CMFB was realized by series connected low threshold devices to achieve an acceptable performance. Because the drain currents are so low, a very low W/L-ratio is required in order to achieve good triode operation. With the limited geometry range offered by the foundry, multiple devices have to be stacked on top of each other in order to increase the effective length of the device.

4.5 Comparator

The comparator schematic is shown in figure 23.

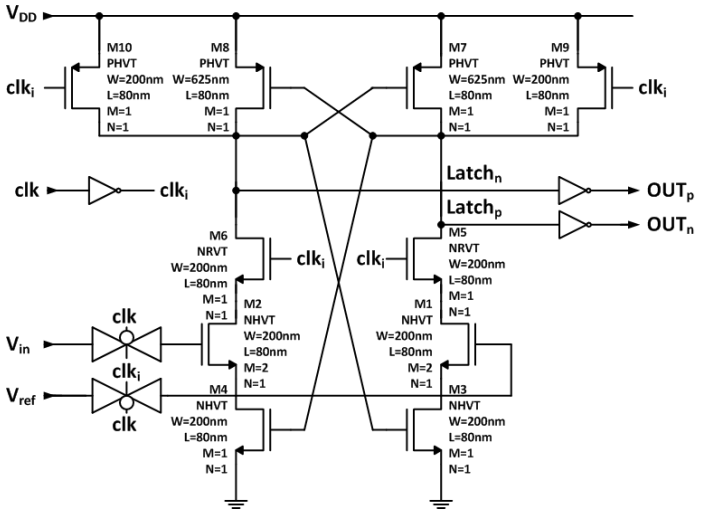


Figure 23: Schematic of comparator.

The sizing of the comparator have been based on following trade-offs:

- A_{gate} minimized for reduced gate-to-channel-leakage.
- Matching.

Though it is not preferable to use minimum lengths due to matching, it is an acceptable sacrifice as offset in $\Delta\Sigma$-ADCs are constant, and easy to calibrate digitally. In order to reduce the effect of metastability W/L-ratios greater than 1 have been chosen to improve the speed. Furthermore, this quickly implies that if a safety margin of $L = 2 \times L_{min}$ is preferred, the gate-to-channel leakage will increase dramatically as A_{gate} increases. Channel lengths of 80nm were therefore chosen in order to minimize static gate leakage. The inverter pair was realized using high threshold devices, both for gain and leakage reasons.

When clk_i is low, M9 and M10 are turned on, pulling the latch to V_{DD}, while the input signal is disconnected from the comparator via the transmission gates and M5 and M6 are turned off, disconnecting M1 and M2 from the latch. When clk_i goes high, M9 and M10 turns off while M5, M6 and the transmission gates are turned on. The indifference in gate voltage on M1 and M2 creates a different charge potential to be stored on nodes $Latch_n$ and $Latch_p$, and the positive feedback inverters start to latch. The latched signal is then buffered by the output inverters. The reason why clk_i is used to change states of the latch is because of the transmission gates. By driving the NMOS with the delayed clk_i, the slower PMOS gets compensated. This concept is used for all digital logic in the ADC.

4.6 SR-latch

The comparator is followed by a SR-latch with two cross-coupled NOR gates. SR was chosen over $\overline{\text{SR}}$ because of reduced static gate-leakage in NOR gates compared to NAND gates. The schematic is shown in figure 24.

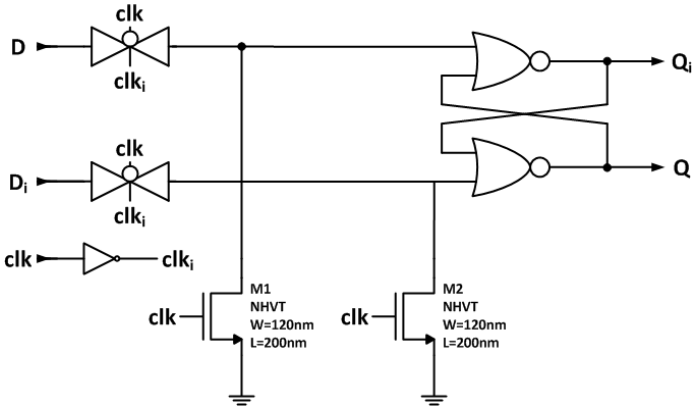


Figure 24: Schematic of SR-latch.

When the clock signal is high, the input nodes of the NOR gates are pulled to ground through M1 and M2, and the output remains unchanged. When the clock signal goes low, M1 and M2 turns off, and the transmission gates switches on. The NOR gate will then either set or reset depending on the input signals, effectively acting as a flip-flop. The lookup table for an SR-latch is shown in table 9 for convenience.

S	R	Action	Q_{next}
0	0	Hold	Q
0	1	Reset	0
1	0	Set	1
1	1	Not allowed	X

Table 9: SR-latch lookup-table

4.7 Delay element

To reduce the effects of comparator metastability and hysteresis, a constant clock delay is added to the SR-latch. This way the same excess loop delay is given every time, and the additional loop phase margin can be controlled. There are two common ways of implementing clock delay. One is to let the clock signal pass through a longer chain of inverters where the transistors can have long channels for additional delaying effect. The other is to use two or three inverters in series with a larger capacitive load after the first inverter in order to

delay the rise and fall time. The first approach results in more noise and jitter across PVT, but commonly reduces power and area consumption compared to the second approach. The second approach adds little noise, but opens up the inverters for a longer time, passing more current through it. However, the ADC uses a very low sampling frequency resulting in static gate-to-channel leakage becoming the major source of current consumption, which causes the second approach to consume less power than the first. The second approach was therefore used in this application, as shown in figure 25.

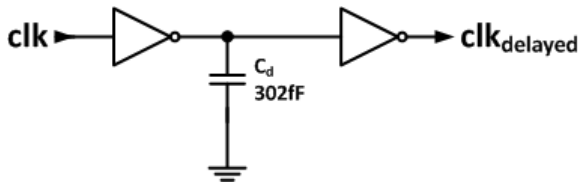


Figure 25: Schematic of delay element.

4.8 DAC

The ADC uses a 1-bit DAC which generates a reference voltage of $\pm 50mV$ from V_{ref}. The DAC tries to define three nodes which serves as as a voltage reference and feedback references. 200nA of current is mirrored into the reference branch, and the three nodes are separated by $250k\Omega$ resistors, placing them $50mV$ apart. The middle reference, V_{ref} is buffered from a reference generated in a resistor string. In order for the DAC to serve as a better voltage source and be able to settle quickly, the impedance of the feedback branch has been reduced by using an NMOS source follower as seen in figure 26. Also, a cascode current mirror has been used to increase the accuracy of the feedback references against PVT variations.

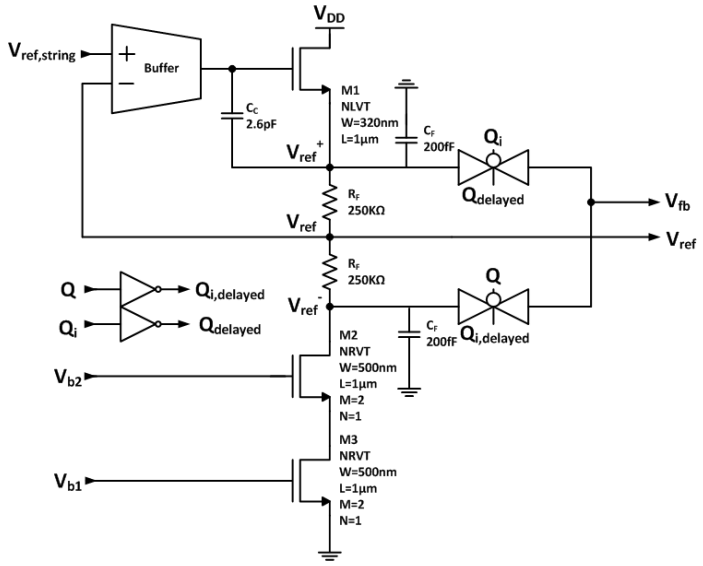


Figure 26: Schematic of DAC.

The DAC can be regarded as a two-stage amplifier with a source follower as second stage in a negative feedback configuration. A Miller compensation is needed to stabilize the amplifier so that the DAC won't oscillate when changing feedback states. A target loop phase margin of 75° was chosen, which corresponds to a Q-factor of 0.527. This should prevent overshoots from exceeding 0.008%. A summary of the AC and DC response is listed in table 10.

$A_{v,LG}$	40dB
PM	74.4°
$f_{ug,CL}$	785kHz
V_{ref}	650mV
V_{ref}^{+}	700mV
V_{ref}^{-}	600mV

Table 10: DAC AC and DC response.

4.9 Buffer OTA

The buffer is a simple NMOS differential pair, reusing the same input transistors and PMOS load as the loop filter OTAs. But in order to save area and current, the differential pair has not been source degenerated with a resistor, and does not use any cascode for improved gain. The buffer OTA is shown in figure 27. Notice that the buffer OTA consumes nominally 200nA, unlike the telescopic OTA in the loop filter, which consumes about 400nA.

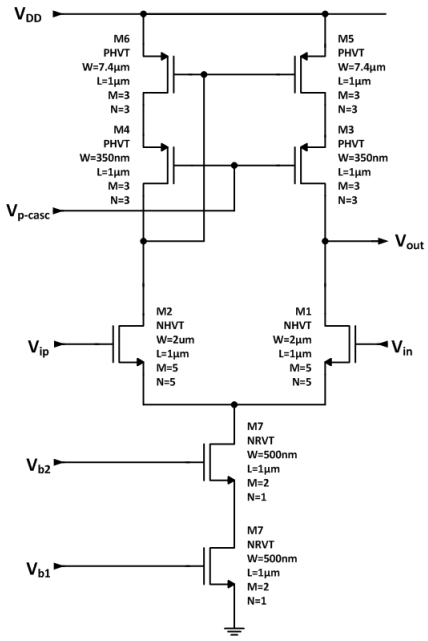


Figure 27: Schematic of buffer OTA.

4.10 Bias circuit

The schematic is shown in figure 28. The circuit uses a 100nA reference, and mirrors it via a cascode current mirror. The cascode is used to improve the accuracy of the DAC feedback reference, and is also used in the buffer OTA. In total, the following bias voltages are generated:

- V_{b1} - bias voltage for input current mirror (lower), used in AGC, OTA, buffer amplifier and to mirror currents for V_{n-casc} and V_{p-casc}.
- V_{b2} - bias voltage for cascode input current mirror (upper), used in DAC and buffer amplifier.
- V_{n-casc} - bias voltage for NMOS cascode in OTA and AGC.
- V_{p-casc} - bias voltage for PMOS cascode in OTA, AGC and buffer amplifier.
- $V_{b,preamp}$ - bias voltage for tail current mirror in preamplifier.
- $V_{p-casc,preamp}$ - bias voltage for PMOS load in preamplifier.
- V_{ref} - Reference voltage, generated from resistor string.

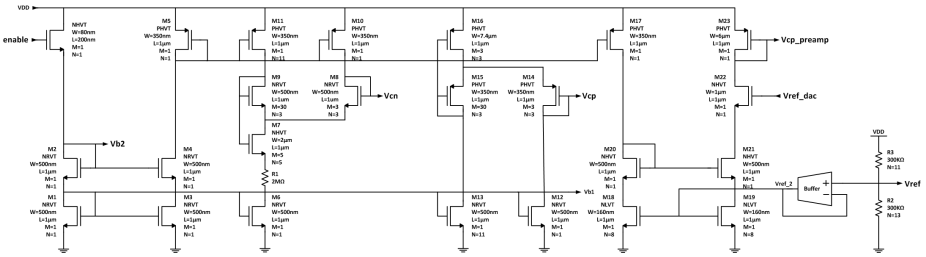


Figure 28: Full schematic view of bias circuit.

4.10.1 Generating V_{n-casc} and V_{n-casc}

The bias networks for V_{n-casc} and V_{n-casc} have been based on a low voltage cascode bias technique for all current levels which can be found in appendix 10.1. The technique is used to reduce headroom consumption of cascodes, which is very important for the OTAs used in this circuit. The technique takes use of the EKV MOS transistor model. A general schematic of the bias technique is shown in figure 29 where saturation is achieved for all current levels through the use of equation 51.

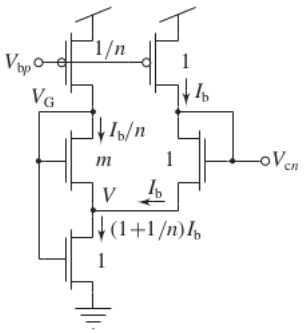


Figure 29: Low-voltage cascode bias.

$$\frac{I_{F2}}{I_{R2}} = 1 + m(1 + n\frac{I_b}{I_b}) = 1 + m(1 + n) \tag{51}$$

Where M2 is the lower transistor. The ratios m and n are implemented as parallel/series connections of m/n unit transistors. For m even, the drain/source regions of the cascode can be optimally shared. If $n = m + 1$ we get that the same amount PMOS strips as NMOS strips for a layout-driven design.

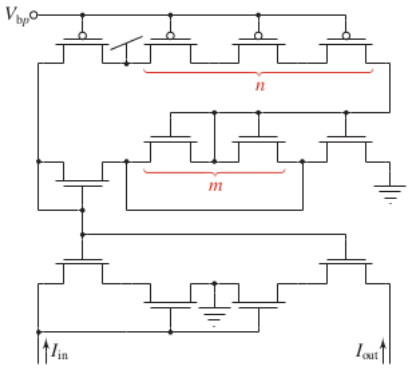
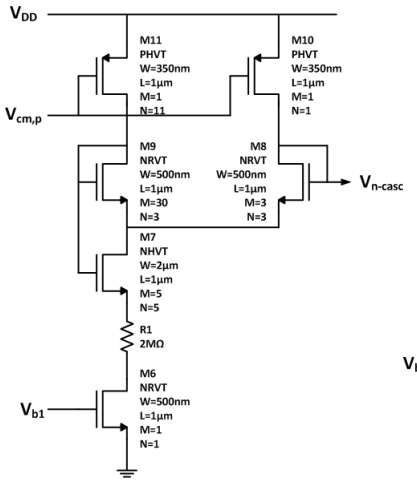


Figure 30: Layout driven design.

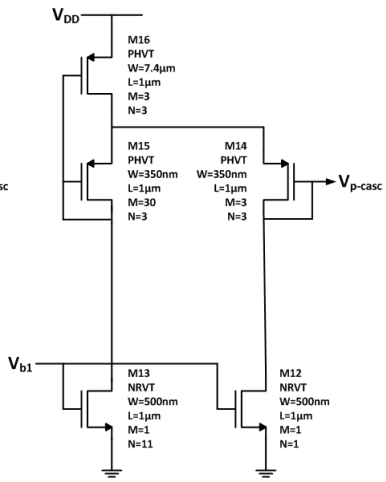
By setting $m = 10$ and $n = 11$, the ratio of (51) becomes 121, which gives good utilization of the headroom for the telescopic cascode. The technique have been used to generate both V_{n-casc} and V_{p-casc}. Because $n = 11$, the total current per bias stage is equal to:

$$I_{stage,n(p)-casc} \simeq I_b(1 + 1/n) \approx 100nA(1 + 1/11) \approx 109nA \tag{52}$$

The combined current consumption for the two stages is therefore approximately 220nA. The schematics are shown in figure 31a and 31b below.



(a) Bias network for V_{n-casc}.



(b) Bias network for V_{p-casc}.

4.10.2 V_{ref}-generation by resistor string divider

The reference voltage for the DSM is generated by the resistor string divider in figure 31. The string consists of 24 large segments of $300k\Omega$ each for simplified layout and to accommodate the implementation of switches if proven necessary for tuning the reference voltage at a later stage.

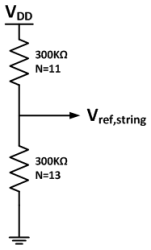


Figure 31: Resistor string for generation of V_{ref}

The reference generated is approximately $\frac{0.65}{1.2} \times V_{DD}$. This reference voltage is given to the DAC so that it can buffer it and generate the reference and feedback for the loop filter. Also, it is buffered internally in the bias circuit to drive the triode CMFB bias stage.

Because the resistor string consists of $24 \times 300k\Omega$-segments, a total of $7.2M\Omega$ is seen between V_{DD} and V_{SS}. The string consumes nominally 167nA for $V_{DD} = 1.2V$.

4.10.3 Generating bias for the preamplifier

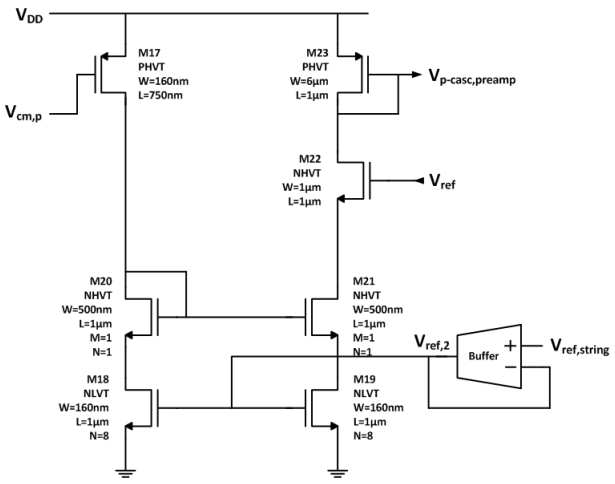


Figure 32: Bias network for preamplifier.

A separate buffer to provide V_{ref} to the triode CMFB bias stage. The buffer is the same as the one used in the DAC, and consumes 200nA. 100nA is mirrored into a diode-connected NMOS device to generate bias voltage for the preamp current mirrors. To improve the accuracy of the current mirror, the triode CMFB devices have been stacked under the source of all current mirrors associated with the preamplifier. The reference buffered in the DAC is applied to the input NMOS and a diode-connected PMOS generates $V_{p-casc,preamp}$. This stage consumes nominally 400nA in total, which includes the two bias-generating branches and the buffer. The schematic is shown in figure 32.

4.10.4 Generating V_{b1} and V_{b2}

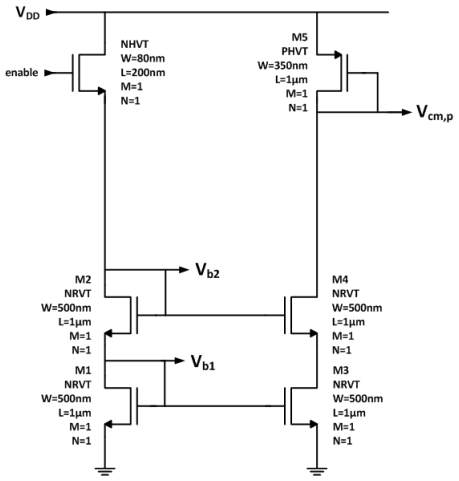


Figure 33: Zoom in of bias network for V_{b1} and V_{b2}.

Figure 33 shows the schematic of the input current mirrors. To reduce the amount of current branches, two simple diode-connected cascodes are placed in the same branch. The lower reference is used to bias the OTAs. In order to still have decent current mirrors, a cascode was added so that a cascode current mirror can be used wherever possible (buffers and DAC Source Follower) for increased accuracy. Also, the cascode mirror The two voltages are generated in the same branch by simple diode-connections. The two voltages are employed to bias another cascode current mirror used to generate a PMOS current mirror to be used throughout the bias circuit. 100nA current have been used as reference, and the two mirrors therefore consume a total of 200nA.

4.10.5 Logic gates

Logic gates in control circuitry us minimum gate sizes to minimize static gate leakage. Inverters, NOR-gates and transmission gates used to drive clock signals

or the flip-flop have been sized with the same dimensions as the transistors in the comparator:

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{625nm}{80nm}, \qquad \left(\frac{W}{L}\right)_{NMOS} = \frac{200nm}{80nm} \tag{53}$$

5 Simulations

This section is divided into subsection for each of the components in the system and finally a section for the simulations of the complete $\Delta\Sigma$-ADC. Each component will be addressed in the same order as in section 4.

5.1 Loop filter

5.1.1 Results summary

For the reader's convenience, some results for the loop filter have been summarized below:

- The loop filters linear range is almost 650mV in typical corners, reduced by approximately 50mV in fast corner.
- The signal gain of the AGC is typically 17dB, and varies $\pm 1dB$ against process and supply variations.
- The filter varies little with temperature within the expected range of operation.
- The filter response is directly proportional to the OTA current mirror which varies with $\pm 17\%$ against PVT.
- f_{ug} varies within a 75Hz range, and the phase margin within a 2.34°C range.
- NTF gain is sufficiently high against all PVT conditions.

5.1.2 Loop filter simulations

A following tests have been performed to verify proper operation of the loop filter:

- DC response of closed loop filter for $V_{in} = [-500mV, 500mV]$.
- Open loop frequency response, seen at the quantizer input, swept from 1 to 10MHz.
- Closed loop NTF from 1Hz to 10MHz.
- Closed loop STF from 1Hz to 10MHz.

Each test was performed against PVT variations. Different parameters and trends have been summarized in section 5.1. The most important results are repeated in this section, while more results can be found in appendix 11.1.

5 process corners have been simulated, and V_{DD} has been simualted from $1.2\text{V} - 10\% = 1.08\text{V}$, to 1.2V, to $1.2\text{V} + 10\% = 1.32\text{V}$.

- TT, typical corner.
- SS, slow corner.
- FF, fast corner.
- FNSP, fast NMOS, slow PMOS corner.
- SNFP, slow NMOS, fast PMOS corner.

The following corner numbering have been defined:

Process	V_{DD} [V]	$\#_1$	V_{DD} [V]	Process	$\#_2$
tt	1.08	1	1.08	tt	1
tt	1.2	2	1.08	ss	2
tt	1.32	3	1.08	ff	3
ss	1.08	4	1.08	fnsp	4
ss	1.2	5	1.08	snfp	5
ss	1.32	6	1.2	tt	6
ff	1.08	7	1.2	ss	7
ff	1.2	8	1.2	ff	8
ff	1.32	9	1.2	fnsp	9
fnsp	1.08	10	1.2	snfp	10
fnsp	1.2	11	1.32	tt	11
fnsp	1.32	12	1.32	ss	12
snfp	1.08	13	1.32	ff	13
snfp	1.2	14	1.32	fnsp	14
snfp	1.32	15	1.32	snfp	15

Table 11: Corner numbering, sorted after process to the left and supply voltage to the right.

The typical or nominal corner is defined as the corner with process tt and $V_{DD} = 1.2V$. Slow or minimum corner refers to process ss and $V_{DD} = 1.08V$. Fast or maximum corner refers to process ff and $V_{DD} = 1.32V$. These are #2, #4 and #9 when sorted after process and #2, #6 and #13 when sorted after voltage, respectively.

5.1.3 Typical corner

Figure 34, depicts the DC response of the loop for minimum and maximum AGC gain settings versus supply voltage. The worst case linearity occurs for high supply voltage due to increased tail current and hence increased g_{m1}. The abrupt change of output voltage towards V_{DD} for large input signals is caused by the input transistor going into triode region when the condition $V_{eff} \gtrsim V_{DS}$ becomes true.

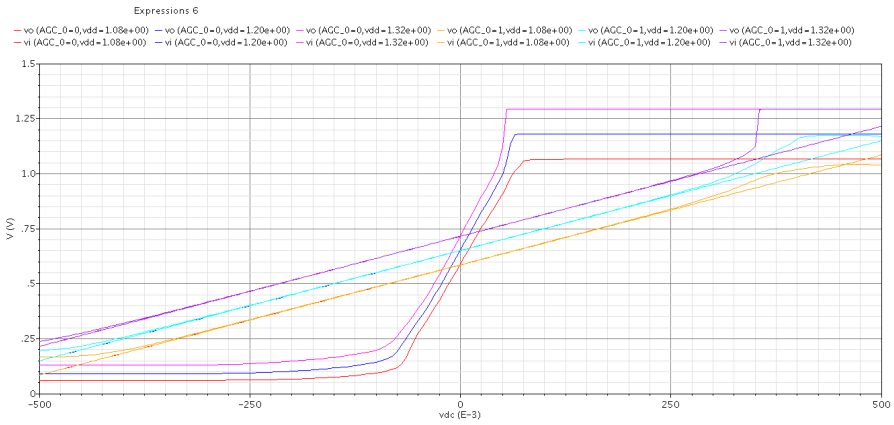
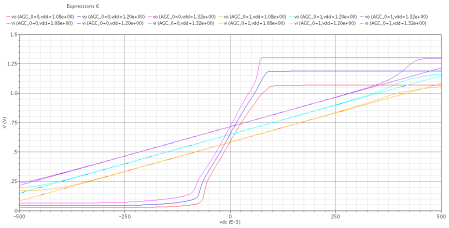


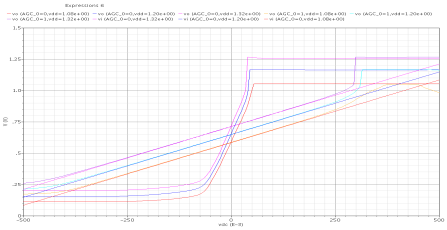
Figure 34: DC response for AGC=[000,110] versus supply voltage.

The loop remains linear from approximately -375mV to +275mV for minimum gain, and ±50mV for maximum gain.

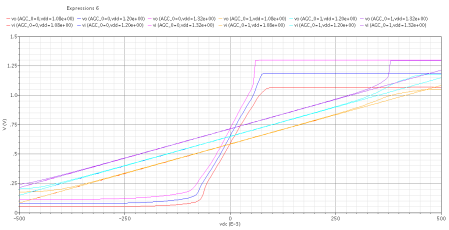
Figure 35a, 35b, 35d and 35c show the DC response of the loop for AGC=[000,110] in corner SS, FF, FNSP and SNFP, respectively.



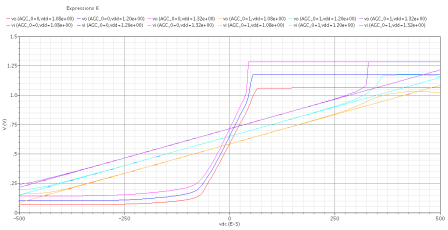
(a) Slow corner



(b) Fast corner



(c) SNFP corner



(d) FNSP corner

Figure 35: Closed loop DC response of filter for $AGC = [000, 110]$.

In corners SS and SNFP, the linearity has improved compared to corner TT because the slow NMOS process reduces g_{m1}. In corner FF and FNSP the opposite effect is observed. The best linearity is observed in corner SS when $V_{DD} = 1.08$, and the worst for corner FF and $V_{DD} = 1.32V$. The worst case linearity ranges from approximately -375mV to +225mV for minimum gain, and

±30mV for maximum gain in the fast corner.

Figure 36, illustrates the NTF at the two integrating nodes. $A_{v_{NTF}}$ reaches a minimum when AGC=[110], while $A_{v_{NTF}}$ reaches a maximum when AGC=[000]. The difference between the two are approximately 3dB.

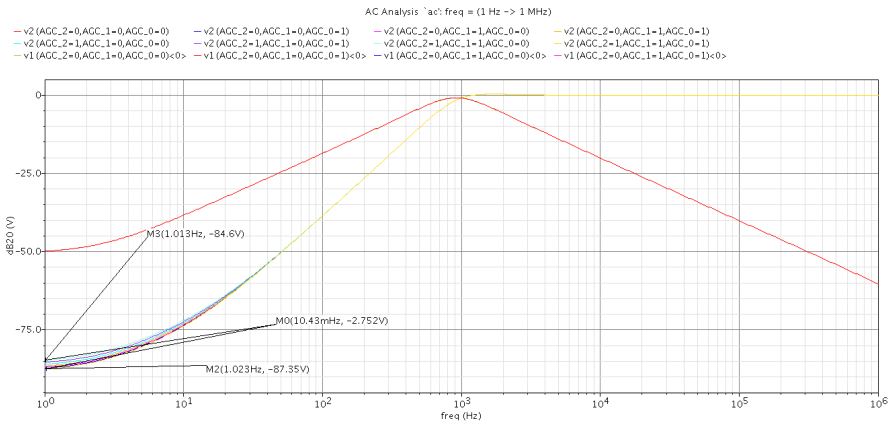


Figure 36: NTF for $AGC = [000 \rightarrow 110]$.

The open loop frequency response for AGC=[000,110] is shown in figure 37. Again, the loss of loop gain is approximately 3dB, and the phase margin changes by 0.4°.

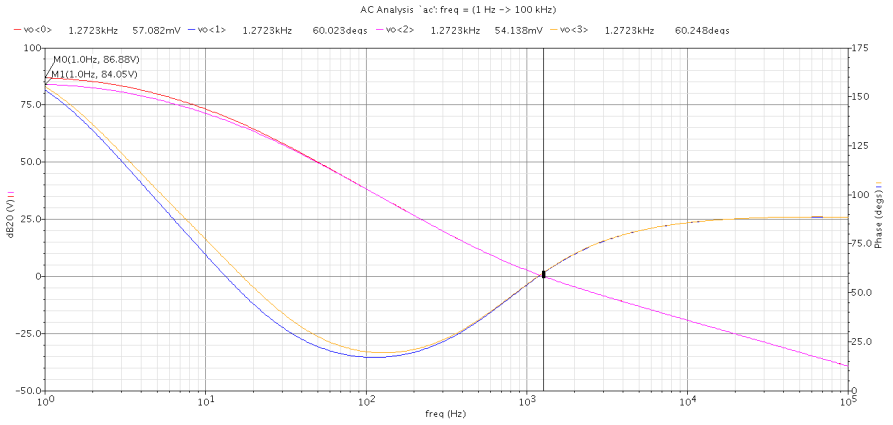


Figure 37: Open loop frequency response in nominal corner.

Figure 38 depicts the STF at the second integrating node while sweeping the supply voltage. The unity gain frequency of the STF is moved out with approximately the same amount as the signal gain of the AGC.

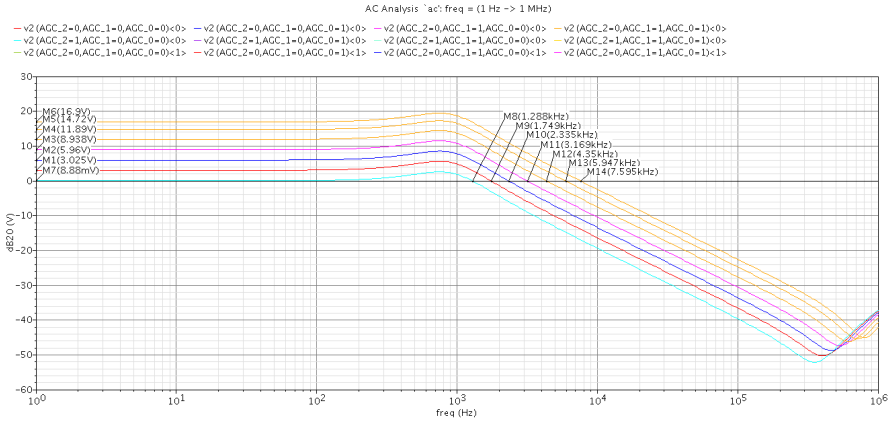


Figure 38: STF for $AGC = [000 \rightarrow 110]$ in nominal corner.

Figure 39, depicts $A_{v_{STF}}$ versus temperature for $V_{DD} = 1.2V$. The variations increase with the signal gain, but are fairly constant, with a maximum $\Delta A_{v_{STF}}$ of 0.22dB between $0°C$ and $50°C$, and a maximum $\Delta A_{v_{STF}}$ of 0.58dB from $-25°C$ to $100°C$.

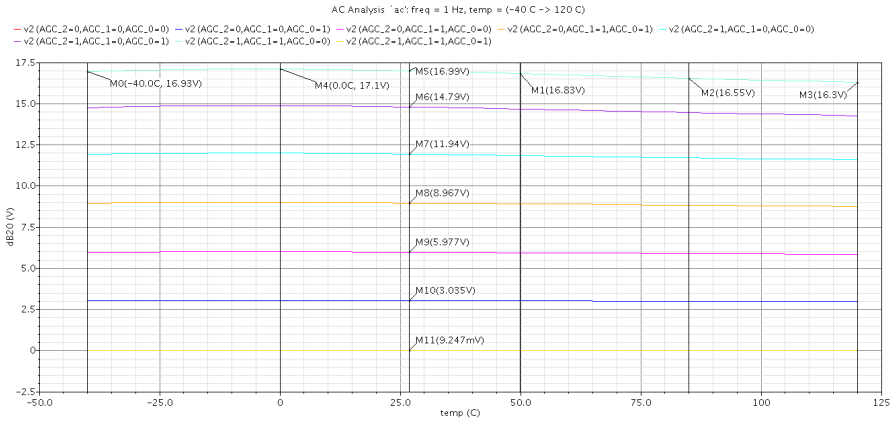


Figure 39: $A_{v_{STF}}$ for $AGC = [000 \rightarrow 110]$ versus temperature, $V_{DD} = 1.2V$.

Figure 40, represents a zoom in of the signal gain variations versus temperature for AGC=[001,110].The variations for AGC=[001] (3dB gain) is much smaller than for AGC=[110], varying by only 60mdB from $-40°C$ to $120°C$, but varying in the same manner as for AGC=[110].

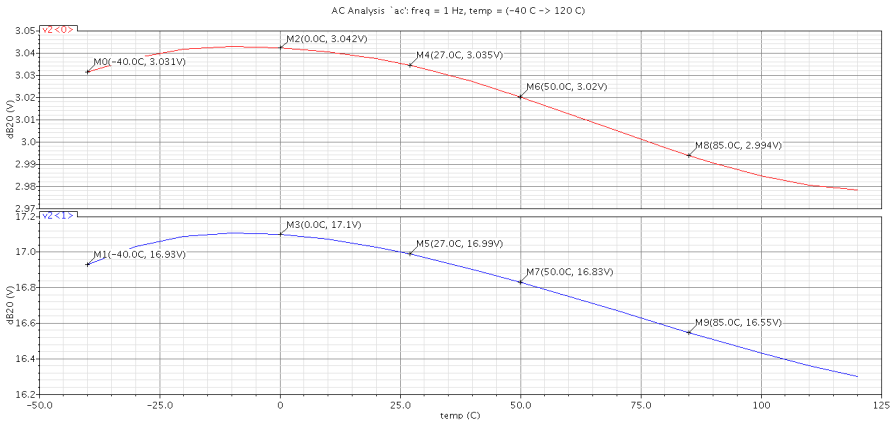


Figure 40: $A_{v_{STF}}$ for $AGC = [001, 110]$ versus temperature, $V_{DD} = 1.2V$.

Figure 41, indicates how the STF varies across temperature for minimum, nominal and maximum corners.

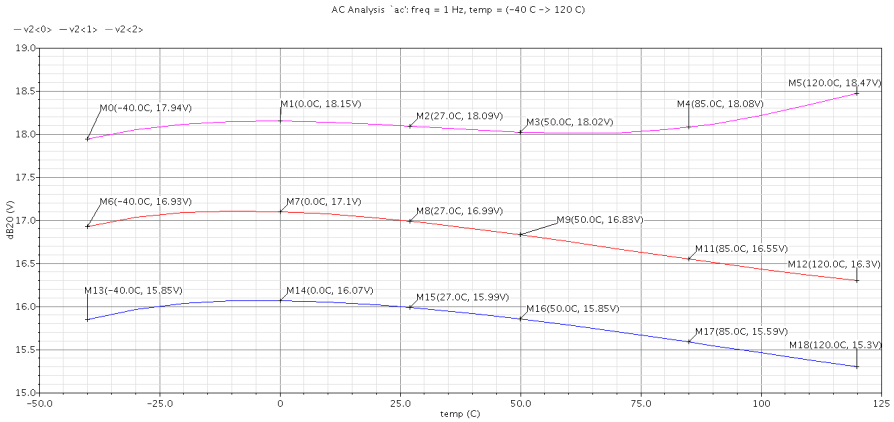


Figure 41: $A_{v_{STF}}$ for $AGC = [110]$ versus temperature, for minimum, nominal and maximum corners.

The gain varies by approximately $\pm 1dB$, which is caused by $\pm 7\%$ g_{m1} due to variation in tail current voltage, and an additional $\pm 10\%$ due to process variations. The tail current in the OTA varies by approximately $\pm 17\%$ against process and supply together. The current consumption is almost constant for temperatures ranging from $0°C$ to $50°C$.

Figure 42, illustrates the variation in $A_{v_{NTF}}$ for $AGC = [000, 110]$ versus temperature. The gain is always greater than 70dB, and remains above 80dB from $-12.5 \circ C$ to $90 \circ C$. The gain decreases by a maximum of 15% from $T = 27°$C.

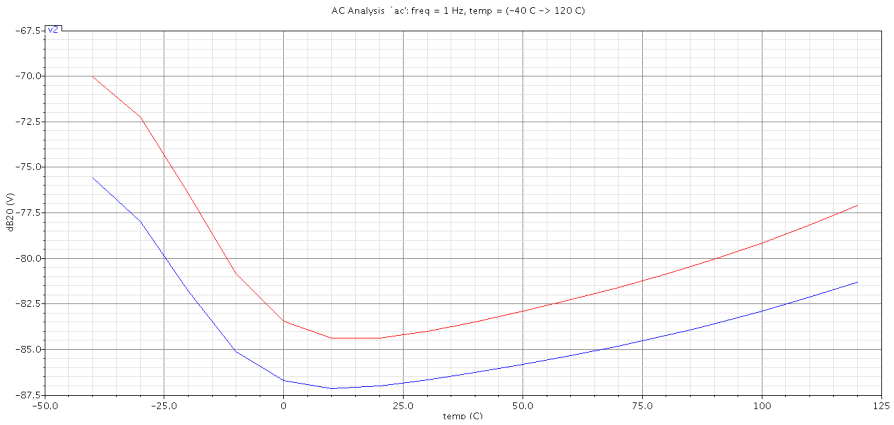


Figure 42: $A_{v_{NTF}}$ for $AGC = [001, 110]$ versus temperature, $V_{DD} = 1.2V$.

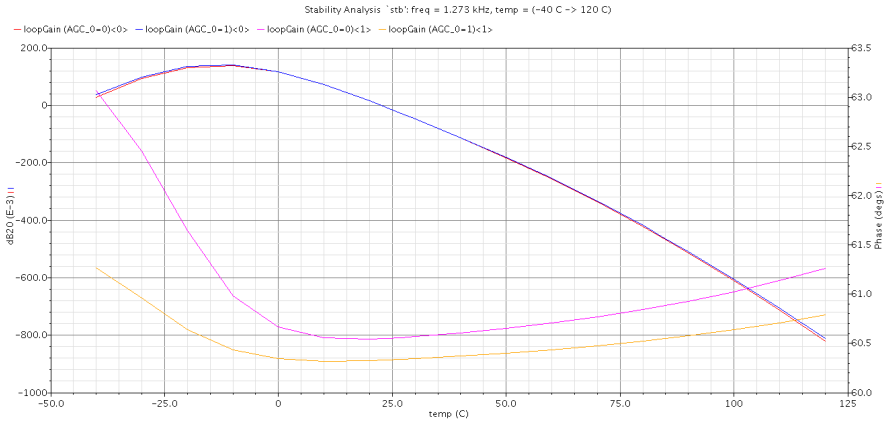


Figure 43: Open loop gain and phase seen at 1273Hz versus temperature for $AGC = [000, 110]$.

Figure 43, reflects the phase and open loop gain at 1273Hz against temperature. The filter response is very stable from $-10°$C to 75°C. It can be found that f_{ug} decrease with temperature as the plot shows that the unity gain frequency have already been passed for temperatures over 25°. This effect is primarily caused by a decrease in g_{m1} as temperature increases. The phase margin is dependant on both g_{m1} and r_{out}. The phase margin shifts with the unity gain frequency in addition to move with the first pole which is dependant on the gain. The phase margin varies similarly to $A_{v,NTF}$ from figure 42.

A complete summary of loop characteristics are listed in table 12 and 13.

Corner	Phase Margin [°]		Unity Gain Frequency [Hz]		$A_{v_{STF}}$ [dB]
[#]	AGC=[110]	AGC=[000]	AGC=[110]	AGC=[000]	AGC=[110]
1	60.970	60.109	1255	1256	16.51
2	60.584	60.279	1272	1274	16.92
3	60.702	60.532	1287	1288	17.27
4	**59.519**	**59.262**	**1228**	**1229**	**15.92**
5	59.717	59.569	1250	1251	16.38
6	59.881	59.707	1267	1267	16.73
7	61.218	60.828	1273	1275	17.13
8	61.373	60.935	1289	1291	17.55
9	**61.604**	**61.135**	**1303**	**1304**	**17.95**
10	61.166	60.795	1269	1270	16.87
11	61.353	60.908	1286	1288	17.27
12	61.582	61.097	1302	1302	17.61
13	59.682	59.299	1238	1239	16.15
14	59.701	59.532	1257	1258	16.59
15	59.902	59.723	1272	1273	16.93
Min	**59.519**	**59.262**	**1228**	**1229**	**15.92**
Max	**61.604**	**61.135**	**1303**	**1304**	**17.95**

Table 12: Phase margin, f_{ug} and $A_{v_{STF}}$ when $AGC = [110]$ vs PVT. Iterations listed as table 11, $\#_1$, describes.

Corner	$I_{DS_{CM}}$ [nA]	$V_{DS_{CM}}$ [mV]	$A_{v_{NTF}}$ [dB]		
[#]	AGC=[000]	AGC=[000]	AGC=[110]	AGC=[000]	$\lvert\Delta A_{v_{NTF}}\rvert$
1	368	109.3	-80.02	-84.49	4.29
2	393	152.7	-84.17	-86.84	2.67
3	415	197.2	-83.04	-85.78	2.74
4	**340**	**90.6**	-85.68	-89.41	3.73
5	366	133.6	**-88.33**	**-90.78**	2.45
6	387	179.4	-86.94	-89.54	2.60
7	402	123.4	-77.05	-81.52	4.47
8	430	164.3	-79.79	-82.85	3.06
9	**459**	**204.4**	**-76.46**	**-80.06**	3.60
10	387	115.2	-78.73	-83.61	**4.88**
11	412	158.7	-84.52	-87.19	2.67
12	435	202.7	-84.97	-87.17	**2.22**
13	351	103.4	-80.95	-84.92	3.97
14	376	146.4	-82.70	-85.73	3.03
15	398	191.2	-78.55	-82.51	3.96
Min	**340**	**90.6**	**-88.33**	**-90.78**	**2.22**
Max	**459**	**204.4**	**-76.46**	**-80.06**	**4.88**

Table 13: OTA tail current ($I_{DS_{CM}}$) when $AGC = [000]$, V_{DS} of OTA tail current mirror when $AGC = [000]$, $A_{v_{NTF}}$ when $AGC = [000, 110]$ and their respective differences. Corner notations are the same as in table 11, $\#_1$.

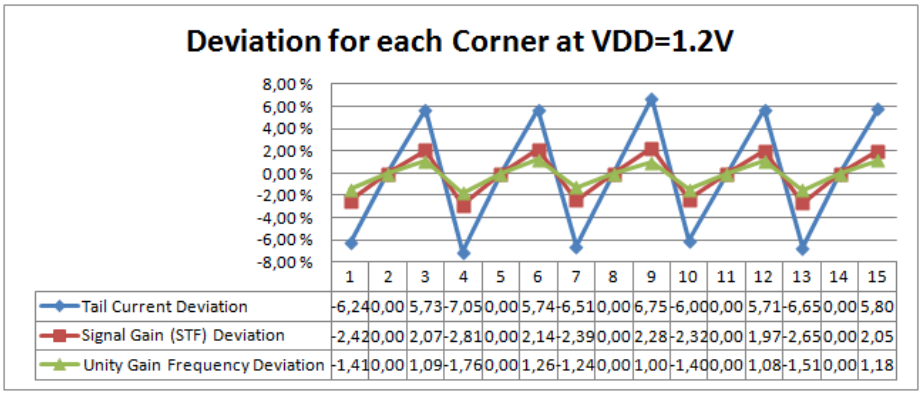
Seen from tables 12 and 13, f_{ug} reaches its minimum for $V_{DD} = 1.08V$ and process SS due to reduced tail current in the OTA. Similarly, f_{ug} reaches its maximum for $V_{DD} = 1.32V$ and process FF. f_{ug} has a range of 75Hz, and the phase margin has a range of 2.342°. $A_{v_{STF}}|_{max}$ varies with 2.03dB, from 15.92dB to 17.95dB (6.25 to 7.9 times gain). From figure 42, it can be concluded that the gain varies by less than 5% from -25°C to -90°C, and decreases by a maximum of 15% from $T = 27$°C at -40°C. The NTF gain is lowest in maximum corner, with a value of 76dB for AGC=[110]. The NTF gain should therefore not get lower than 72dB from -25°C to -90°C, and should never be lower than about 65dB.

Figures 45, 46 and 47 confirm again that the OTA tail current mirror causes a major influence on the loop filter response.

Corner	$I_{DS_{CM}}$		Δf_{ug}		$\Delta A_{v_{STF}}\|_{max}$ [dB]	
[#]	Value [nA]	%	Value [Hz]	%	Value [dB]	%
1	-24.5	-6.24	-18	-1.41	-0.41	-2.42
2	-	-	-	-	-	-
3	22.5	5.73	14	1.09	0.35	2.07
4	-25.8	**-7.05**	**-22**	**-1.76**	**-0.46**	**-2.81**
5	-	-	-	-	-	-
6	21.0	5.74	**16**	**1.26**	0.35	2.14
7	**-28.0**	-6.51	-16	-1.24	-0.42	-2.39
8	-	-	-	-	-	-
9	**29.0**	**6.75**	13	1.00	**0.40**	**2.28**
10	-24.7	-6.00	-18	-1.40	-0.40	-2.32
11	-	-	-	-	-	-
12	23.5	5.71	14	1.08	0.34	1.97
13	-25.0	-6.65	-19	-1.51	-0.44	-2.65
14	-	-	-	-	-	-
15	21.8	5.80	15	1.18	0.34	2.05
Min	**-28.0**	**-7.05**	**-22**	**-1.76**	**-0.46**	**-2.81**
Max	**29.0**	**6.75**	**16**	**1.26**	**0.40**	**2.28**

Table 14: Δ for $V_{DD|_{min}}$ and $V_{DD|_{max}}$ relative to given process at $V_{DD} = 1.2V$. These values are used to see how change in V_{DD} affects a given process. Presented in both actual value and percentage.

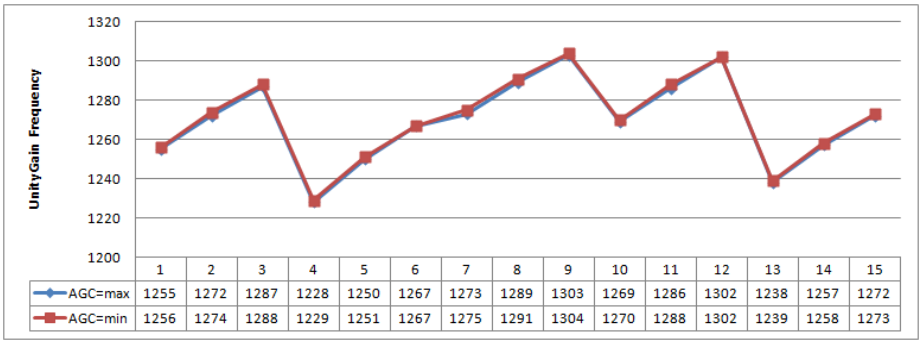
From table 14, it can be seen that tail current varies with approximately $\pm 7\%$ against supply voltage. Figure 44, displays how the tail current increases with V_{DD} as a result of increased $V_{ref(CM)}$ and hence higher $V_{D,\text{tail}}$. It also suggests that $f_{ug} \propto I_{D,\text{tail}}$ and $A_{v,STF} \propto I_{D,\text{tail}}$.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tail Current Deviation	-6,24	0,00	5,73	-7,05	0,00	5,74	-6,51	0,00	6,75	-6,00	0,00	5,71	-6,65	0,00	5,80
Signal Gain (STF) Deviation	-2,42	0,00	2,07	-2,81	0,00	2,14	-2,39	0,00	2,28	-2,32	0,00	1,97	-2,65	0,00	2,05
Unity Gain Frequency Deviation	-1,41	0,00	1,09	-1,76	0,00	1,26	-1,24	0,00	1,00	-1,40	0,00	1,08	-1,51	0,00	1,18

Figure 44: $A_{v_{STF}}|_{AGC=[000]}$, OTA tail current and f_{ug} vs. process and supply. V_{DD} swept for each process and related to typical supply voltage (1.2V) for each process ($\#_1$-notation).

Figure 45, presents a plot of f_{ug} against corners. The observed trend is that corners with fast NMOS (FF and FNSP) have a higher f_{ug}, while corners with slow NMOS have a lower f_{ug}. The same trend can be found in figures 46, 47 and 48.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AGC=max	1255	1272	1287	1228	1250	1267	1273	1289	1303	1269	1286	1302	1238	1257	1272
AGC=min	1256	1274	1288	1229	1251	1267	1275	1291	1304	1270	1288	1302	1239	1258	1273

Figure 45: Unity gain frequency [Hz], f_{ug}, vs. process and supply ($\#_1$-notation).

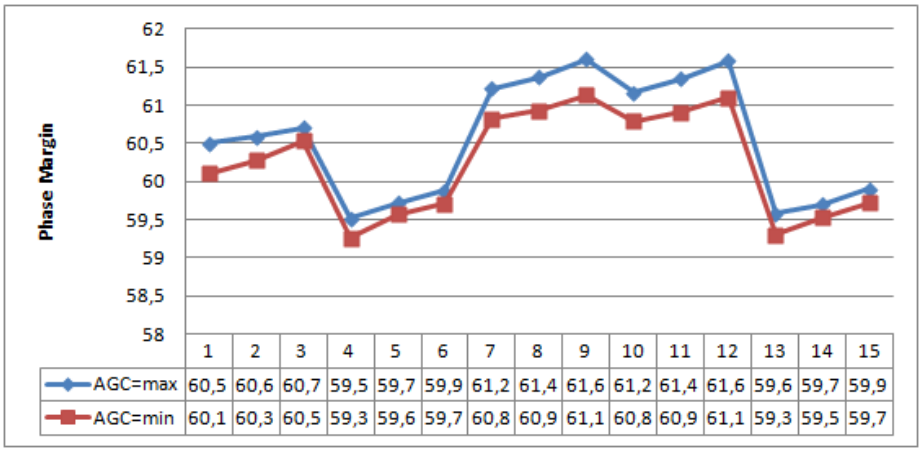


Figure 46: Phase margin [°] vs. process and supply ($\#_1$-notation).

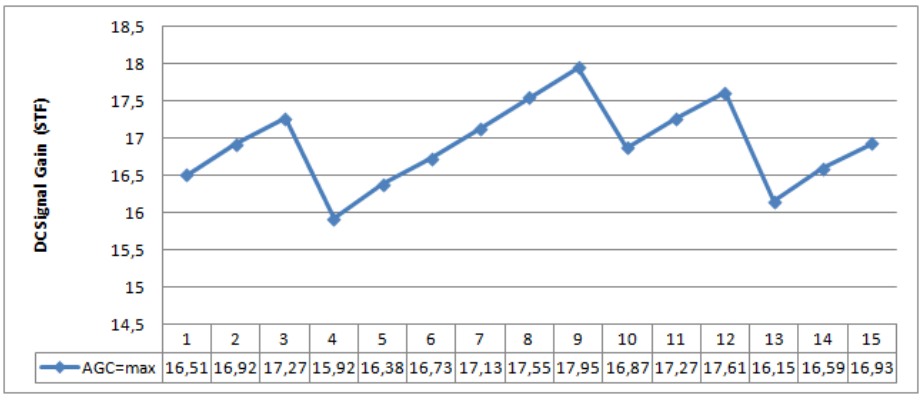
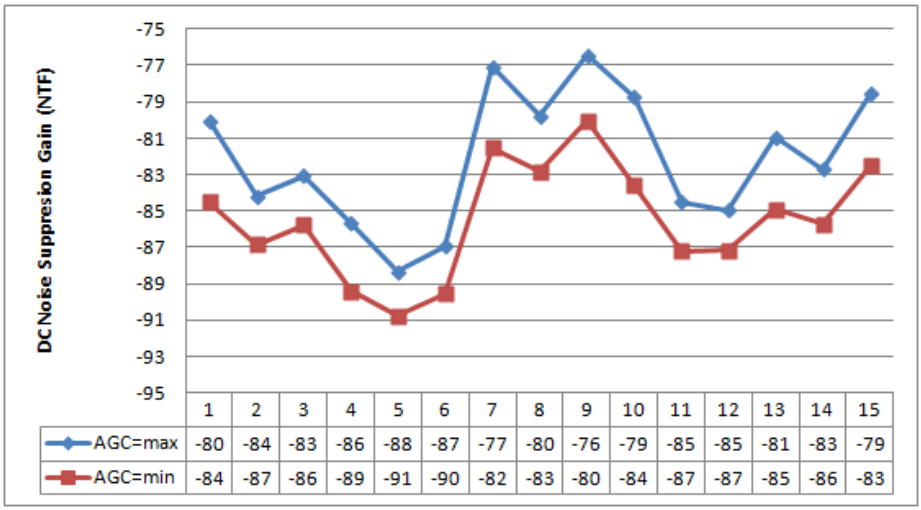


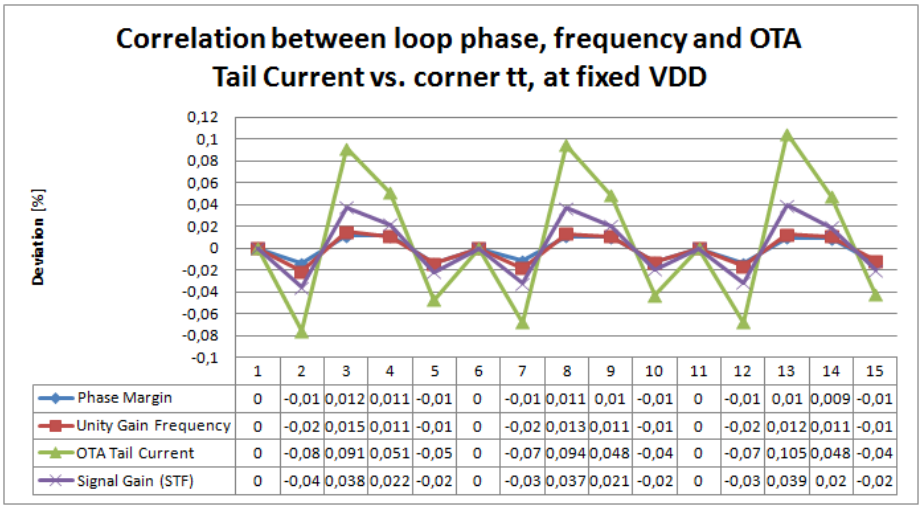
Figure 47: $A_{v_{STF}}$ for $AGC = [000, 110]$ vs. process and supply ($\#_1$-notation).



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AGC=max	-80	-84	-83	-86	-88	-87	-77	-80	-76	-79	-85	-85	-81	-83	-79
AGC=min	-84	-87	-86	-89	-91	-90	-82	-83	-80	-84	-87	-87	-85	-86	-83

Figure 48: $A_{v_{NTF}}$ for $AGC = [000, 110]$ vs. process and supply ($\#_1$-notation).

Figure 48, relates that there is more than enough in-band noise suppression, and that the gain varies little with AGC setting. Also, the peaking of gain for nominal V_{DD} in each corner confirms that the operating point of the NMOS input and cascode have been carefully optimized.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Phase Margin	0	-0,01	0,012	0,011	-0,01	0	-0,01	0,011	0,01	-0,01	0	-0,01	0,01	0,009	-0,01
Unity Gain Frequency	0	-0,02	0,015	0,011	-0,01	0	-0,02	0,013	0,011	-0,01	0	-0,02	0,012	0,011	-0,01
OTA Tail Current	0	-0,08	0,091	0,051	-0,05	0	-0,07	0,094	0,048	-0,04	0	-0,07	0,105	0,048	-0,04
Signal Gain (STF)	0	-0,04	0,038	0,022	-0,02	0	-0,03	0,037	0,021	-0,02	0	-0,03	0,039	0,02	-0,02

Figure 49: Correlation between phase margin, f_{ug}, OTA tail current and $\Delta A_{v_{STF}}$, vs. process and supply ($\#_2$-notation). Process has been swept for a fixed $V_{DD} = [1.08, 1.2, 1.32]V$, and related to process tt in percentages.

The overall trends that can be observed from these results and the results in section 11.1 indicates there is a strong correlation between the condition of the OTA tail current mirror and the response of the loop filter. Furthermore,

the response to temperature variations are fairly constant within the expected region of operation.

5.1.4 Fully differential AGC input - Common-mode rejection

Since a pseudo-differential structure with an AC-grounded negative input only eliminates DC components, a fully differential input to reduce 50Hz power-line interference was tested. Monte Carlo analysis was done against process and mismatch for $AGC = [000]$ and $AGC = [110]$ to find the CMRR[9]. The results are shown in table 15.

AGC	CMRR [dB]		
	Typ	μ	σ
000	66.08	59.36	8.64
110	65.79	54.55	8.84

Table 15: Monte Carlo results for CMRR. N=100, sigma=6.6

5.2 Preamplifier

To verify the behaviour of the preamplifier, Monte Carlo analysis was performed to validate the common-mode variations against process and mismatch. Figure 50, provides the typical DC response of the preamplifier when sweeping V_{in} from -500mV to 500mV. The amount of series stacked triode CMFB transistors were swept to find a good trade-off between good CMFB and gain. Because the current is so low, very low W/L-ratios of the triode CMFB is required in order to increase V_S of the current mirror so that the CMFB can increase $\Delta V_{GS,\text{tail}}$.

[9]Common-Mode Rejection Ratio

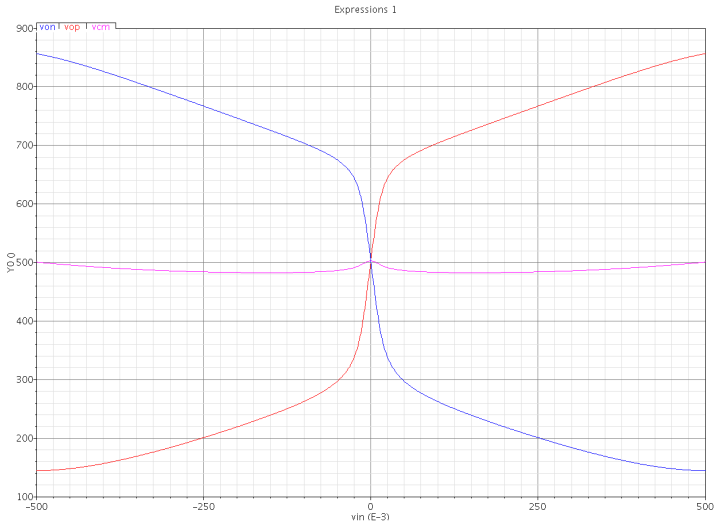
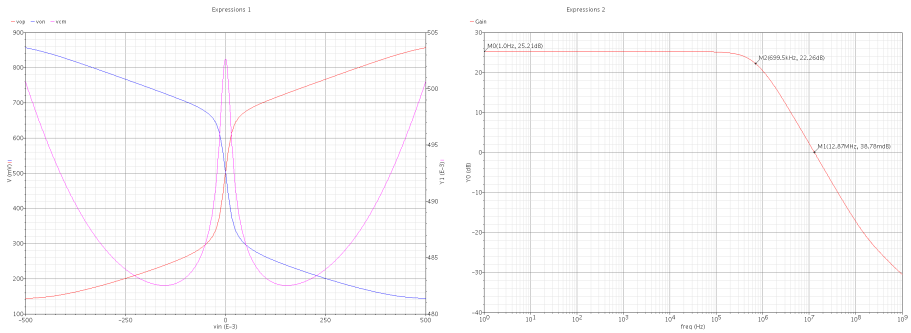


Figure 50: Differential and common-mode outputs between $\pm 500mV$ differential input in typical corner.

The triode CMFB performs more effectively if $V_{S,\text{tail}}$ is increased so that the CMFB can vary the $V_{GS,\text{tail}}$ more. However, due to of gate-to-channel leakage, output common mode and amplifier gain decreases with increased leakage. As a result, longer channels provides better CMFB but lower gain and V_{CM}. The CMFB triode was realized stacking 8 low threshold unit transistors of maximum length and two times minimum width; $W/L = 160nm/1\mu m$. The total W/L-ratio of the triode CMFB therefore becomes 1/50. In appendix 11.2 simulations with N = 1, 4 and 16 have been included.

Figure 51, depicts the small signal frequency response and a zoom in of the DC response of the preamplifier for typical corner.



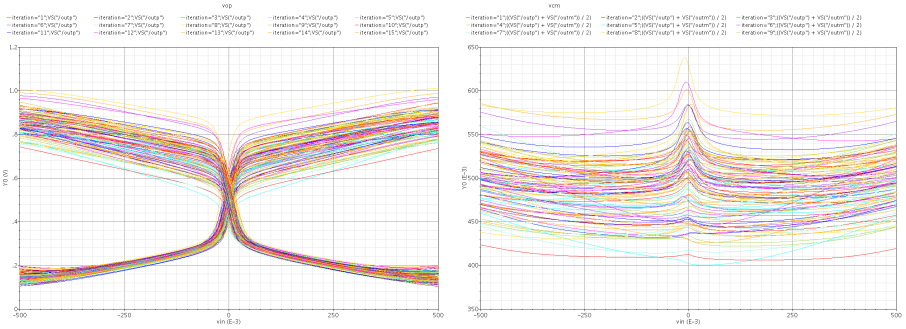
(a) DC response of preamplifier for typical corner, zoomed.

(b) Small-signal response of preamplifier for typical corner.

Figure 51: Small-signal and DC response of preamp in typical corner.

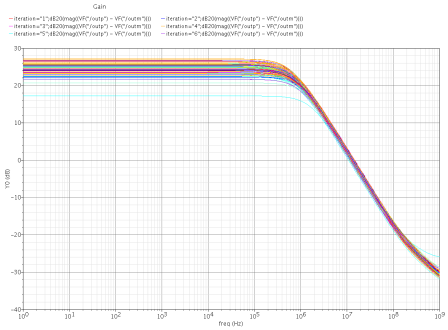
Figure 51a, illustrates that the common mode varies with 20mV from 482.5mV to 502.5mV. In figure 51b, it can be seen that the DC gain is 25.2dB with $f_{-3dB} = 700kHz$ and $f_{ug} = 12.9MHz$.

Monte Carlo analysis with N=100 was simulated for both process and mismatch. The DC response of the two outputs, the common mode voltage and the frequency response are shown in figure 52a, 52b and 52c, respectively.



(a) DC response of preamplifier for typical corner.

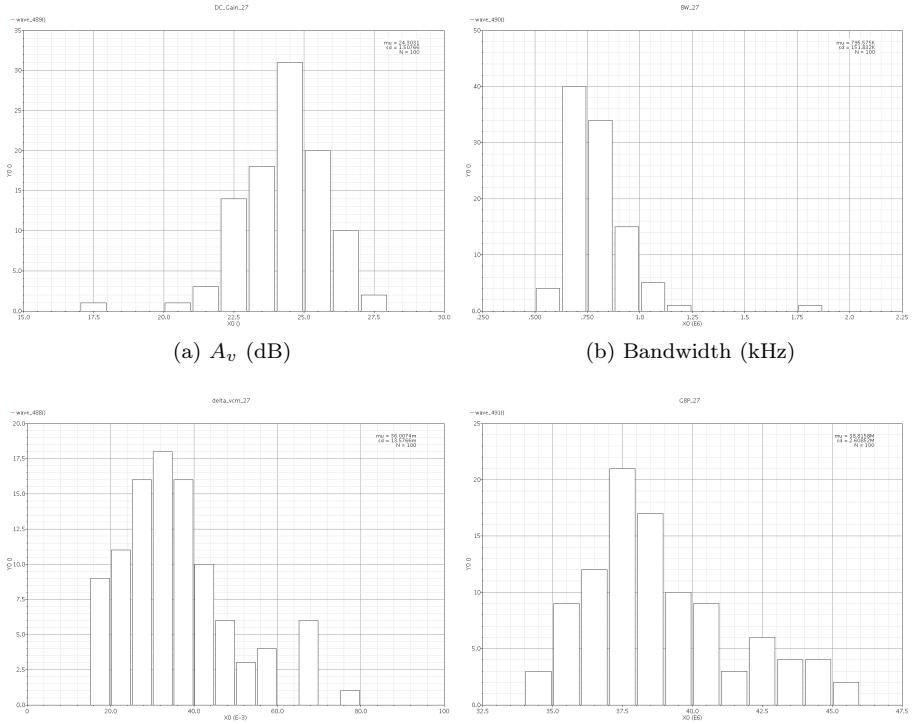
(b) DC response of preamplifier for typical corner, zoomed.



(c) Small-signal response of preamplifier for typical corner.

Figure 52: Small-signal and DC response of preamp from Monte Carlo analysis.

Figure 53, reflects histograms of scalar values for the DC gain, bandwidth, $\Delta V_{CM}|_{\max}$ and the gain bandwidth product.



(a) A_v (dB)

(b) Bandwidth (kHz)

(c) ΔV_{CM} (mV)

(d) Gain bandwidth product

Figure 53: Monte Carlo distribution of key characteristics of preamplifier.

The results have been summarized in table 16. The mean value (μ) and the standard deviation (σ) have been included.

Scalar	μ	σ	min	max
A_v [dB]	24.3	1.5	20.5	27.5
BW [kHz]	795.575	151.832	550	1750
$\Delta V_{CM}\|_{max}$ [mV]	36	13.58	17.5	77.5
GBP	38.82	2.61	34.5	45.5

Table 16: Summary of scalar results from Monte Carlo simulations.

As seen, the triode CMFB is operational for all Monte Carlo runs and the variations in V_{CM} are within an acceptable range.

5.3 Comparator

To avoid metastability, enough clock delay must be given to the latch so that it can latch even input signals of 1LSB ($50\mu V$). Therefore, Monte Carlo analysis for various input voltages were performed to map the delay of the comparator.

From the results, a proper delay was given to the delay element in order to eliminate metastability as much as possible.

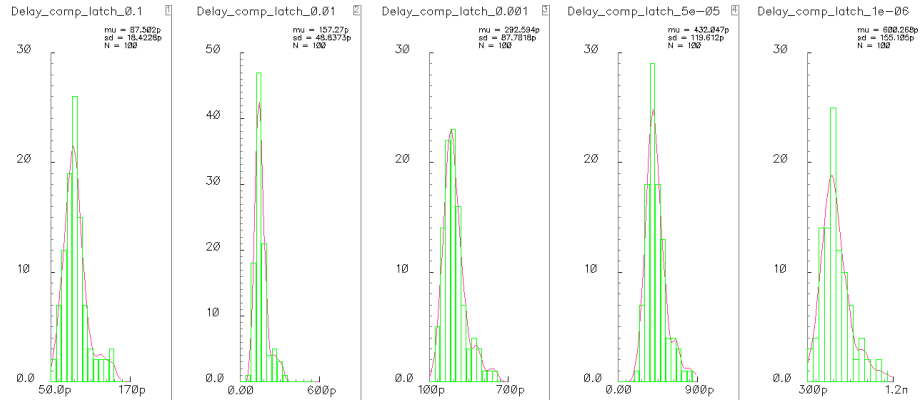


Figure 54: Time delay for the latch output (pre-buffer) to reach 90% of V_{DD}, $V_{in} = [1u, 50u, 1m, 10m, 100m]V$

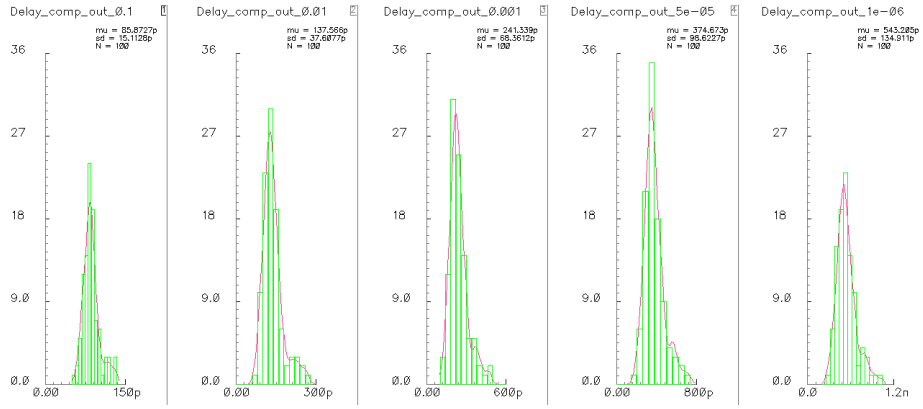
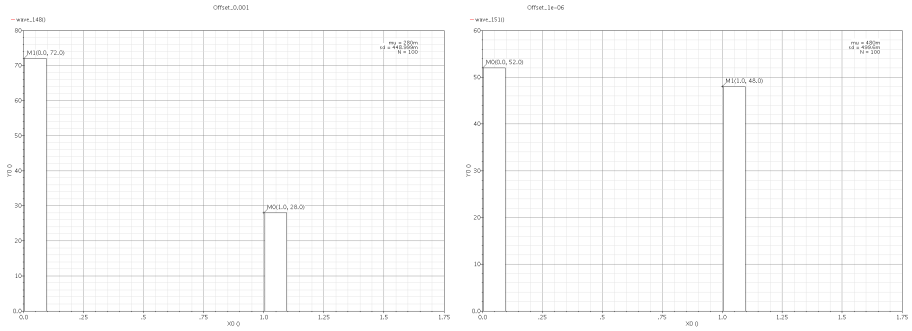


Figure 55: Time delay for the comparator output (post-buffer) to reach 90% of V_{DD}, $V_{in} = [1u, 50u, 1m, 10m, 100m]V$



(a) $V_{in} = 1mV$ (b) $V_{in} = 1\mu V$

Figure 56: Monte Carlo results of offset rate.

5.4 Summary

Monte Carlo analysis was run while V_{in} was swept, and delay, current and offset in the comparator was measured. The offset rate was estimated as how many mistakes the comparator would produce out of 100 tries for different input voltages when varying process and mismatch. The results have been summarized in table 17. The current consumption of the delay element and the SR-latch have also been included in the table.

Measurement	amplitude [V]	Mean value, $\overline{x}$	Standard deviation, δ
Delay latch	100m	87.5ps	18.4ps
	10m	157.3ps	48.9ps
	1m	292.6ps	87.8ps
	50μ	432.0ps	119.6ps
	1μ	600.3ps	155.1ps
Delay output	100m	85.9ps	15.1ps
	10m	137.6ps	37.6ps
	1m	241.3ps	68.4ps
	50μ	374.7ps	98.6ps
	1μ	543.2ps	134.9ps
I_{total}		41.4nA	7.3nA
$I_{\text{comparator}}$		17.7nA	3.2nA
$I_{\text{delay element}}$		9.0nA	2.0nA
$I_{\text{SR-latch}}$		14.7nA	3.1nA
Offset-rate	10m	0%	
	6m	4%	
	5m	5%	
	4m	6%	
	3m	12%	
	2m	22%	
	1m	28%	

Table 17: Summary from Monte Carlo analysis for comparator. Note that as V_{in} becomes smaller, the offset increases along with the latch times.

It can be seen that for comparator input voltages under 10mV, offsets begin to occur. The offset is however constant in $\Delta\Sigma$ and can therefore be easily calibrated. It is expected that signals of $1\mu V$ will not be detected due to intrinsic noise, but because the system is slow enough to afford it, a delay that can avoid metastability for $1\mu V$ signals was added.

With the given sizes, the leakage estimates in figure 57 were found.

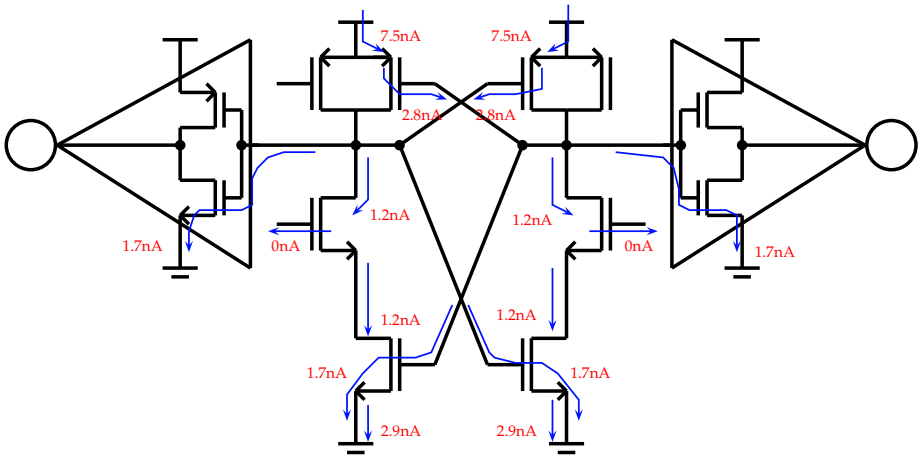


Figure 57: Leakage estimates of comparator in typical corner.

5.5 Delay element

From section 5.3, figure 55, it was found that the maximum delay measured at the output of the comparator for a $1\mu V$ input signal was 1ns. Even though $1\mu V$ is smaller than 1LSB, the system is so slow that it is affordable to add enough delay to avoid metastability even for such low input signals as a safe margin. Therefore, a typical delay of 1ns was given to the delay and a Monte Carlo analysis showed that the variation would be acceptable. The results are shown in figure 58.

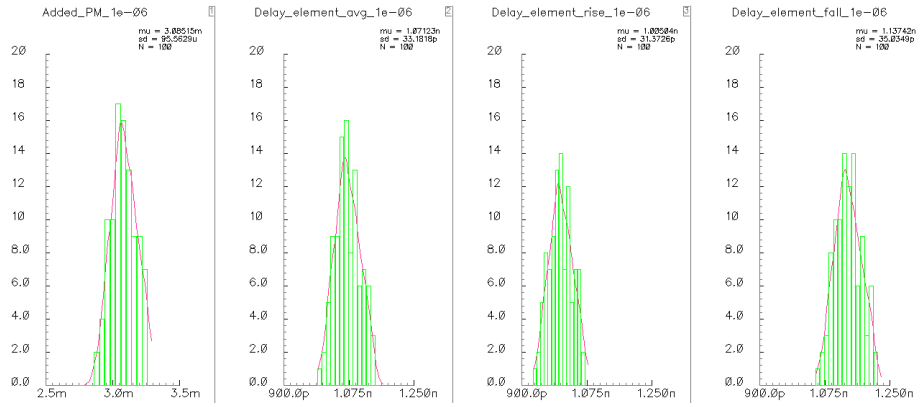


Figure 58: Monte Carlo simulation for delay element.

The histogram to the far left illustrates the distribution of the equivalent extra phase margin that the delay element introduces to the loop. The second to the left describes the average delay when both rising and falling times are combined. Histogram number 3 show how much delay is produced for negative clock edges,

while the histogram to the far right indicates how much delay is produced for positive clock edges. Since the comparator triggers on falling clock edges, it can be seen that the delay is never less than 1ns, and has an average of 1.137ns. In conclusion enough delay has been added to practically guarantee that metastability will not occur. The distribution has a low deviation, caused by low jitter noise, which is a result of having a delaying capacitor rather than an inverter chain. As for excess phase delay, it can be seen that from comparator input to SR-latch output, the added phase has a mean value of $\mu = 3.09m^{\circ}$ where $\sigma = 95.6\mu^{\circ}$. This is a negligible delay and shouldn't affect the response of the $\Delta\Sigma$-modulator.

5.6 Transient response of comparator and delay element

Figure 59 depicts the clock signals, before and after the delay element, along with the comparator's output nodes, before and after the inverting output buffer, as V_{in} changes. It can be seen that even for $V_{in} = 1\mu V$, there is enough time for the comparator latch to define the output of the comparator buffer before the delayed clock switches state. The transition of the delayed clock is slow due to the 300fF capacitor that is placed within the delay element. Though this increases the dynamic power consumption of the inverter, the added power consumption is as mentioned negligible compared to the static power consumption that a long inverter chain would cause due to gate-to-channel leakage . Also, since only two inverters are used in the delay element, the clock signal will be less noisy, which is another benefit.

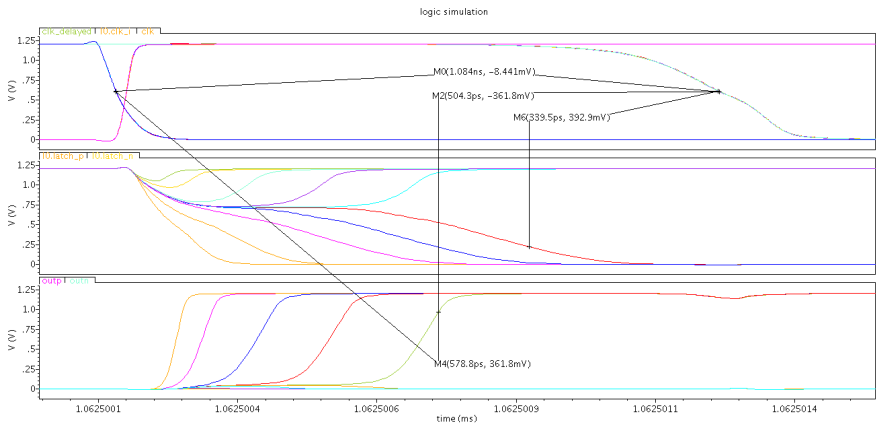


Figure 59: Transient response of the comparator's latch output and the comparator's buffer output for $V_{in} = [1\mu, 50\mu, 1m, 10m, 100m]V$. The upper plot depicts the clock signals, the middle plot shows the output nodes of the latches in the comparator, while the lower plot depicts the outputs of the comparator after the buffers.

From figure 59 it can be seen that the delay element has been given enough delay to prevent metastability as the second latch tries to latch the comparator

output, even for signals in the order of μV.

5.7 DAC

The DAC was stabilized using a Miller compensation of 2.6pF. The closed loop frequency response for minimum, nominal and maximum corner is shown in figure 60

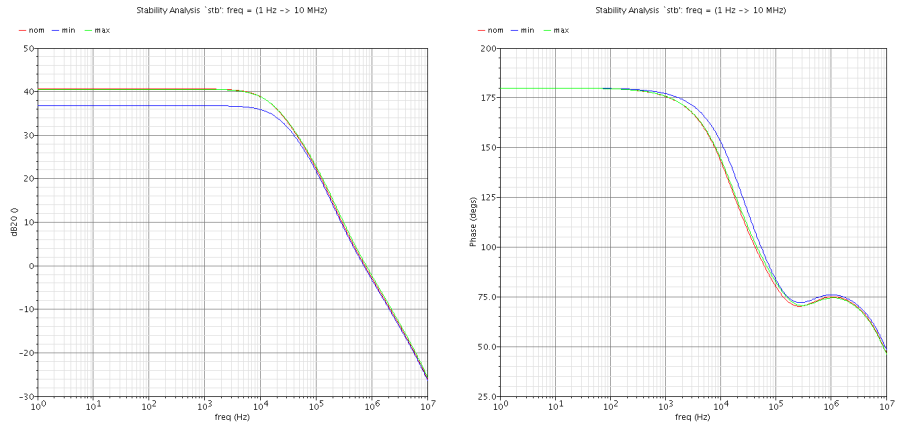


Figure 60: Frequency response of voltage buffer in negative feedback configuration for typical, slow and fast corner.

The gain, $A_{v,LG} = 40dB$, and the phase margin is 74.4° at $f_{ug,CL} = 785kHz$.

The open loop gain seen at the output of the source follower is the product of the buffer's frequency response and the source follower's frequency response. Because the compensating capacitor is so large, the poles and zeros of the source follower becomes dominant.

Figure 61 depicts the frequency response of the two stage amplifier together with the frequency response of the first and second stage separated.

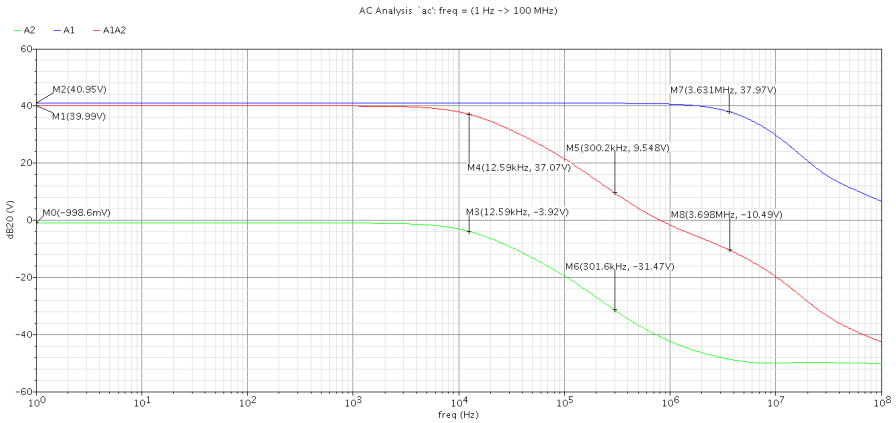


Figure 61: Open loop response of first stage (blue), second stage (source follower) (green) and the two-stage buffer (blue).

As we can see in figure 61, the frequency response of the unity gain buffer behaves as expected.

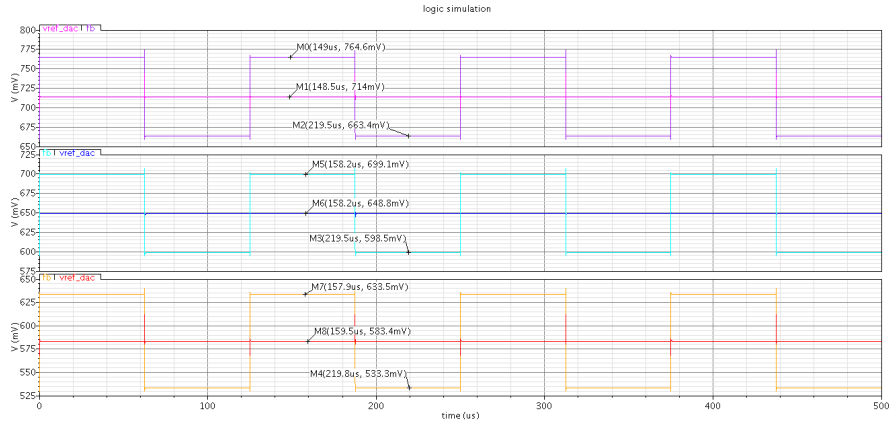


Figure 62: Transient response of DAC for $V_{DD} = [1.08, 1.2, 1.32]V$.

Figure 62 shows how V_{ref} and $V_{fb}^{\pm}$ varies with supply voltage. Due to $\pm 10°$ variation in supply voltage, the voltage read out from the resistor string in the bias circuit will also vary with $\pm 10\%$, suggesting that $\Delta V_{ref} = \pm 10\% V_{ref}|_{V_{DD}=1.2V} = 650mV \times 0.1 = 65mV$. Hence, depending on supply voltage, we expect $V_{ref} = \langle 585mV, 715mV \rangle$, as figure 62 confirms.

The parasitic capacitance seen at the feedback output, $C_{p,fb}$ is approximately equal to the drain capacitances of the two MOS devices in the two transmission gates plus the gate capacitance of the negative input transistor of the feedback OTA. When the DAC changes states, the transmission gate turning off will cause charge injection to charge the parasitic capacitance seen at the input of

that switch. Through the gate turning on, the necessary charge required to charge $C_{p,fb}$ to its correct value will initially be transferred to or from the parasitic capacitance seen at the input of that switch, and some from the parasitic capacitance seen at the V_{ref}-node, $C_{p,vref}$.

$C_{p,vref} \approx 5 \times C_{p,fb}$ as V_{ref} is used at 3 OTA inputs, two buffer inputs and the preamplifier. The parasitic capacitance seen at node V_{ref}^{+} and V_{ref}^{-} is equal to the source (input) capacitance of the transmission gate plus the source capacitance of the source follower in the case of V_{ref}^{+}, or the drain capacitance of the cascode current mirror in the case of V_{ref}^{-}. These parasitics are much smaller than the one seen at the input of the feedback OTA. Therefore, when changing states, the charge on the negative input of the feedback OTA will charge or discharge the parasitics at nodes V_{ref}^{+} and V_{ref}^{-}, causing large, momentarily voltage glitches shown in figure 63.

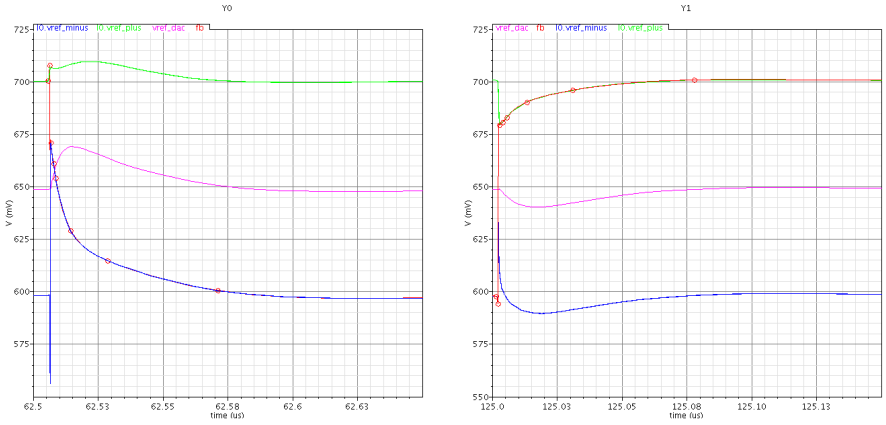


Figure 63: Transition between high and low feedback, seen at nodes $V_{ref}^{+}, V_{ref}, V_{ref}^{-}$ and fb with $C_C = 2pF$ and no C_F to reduce glitches.

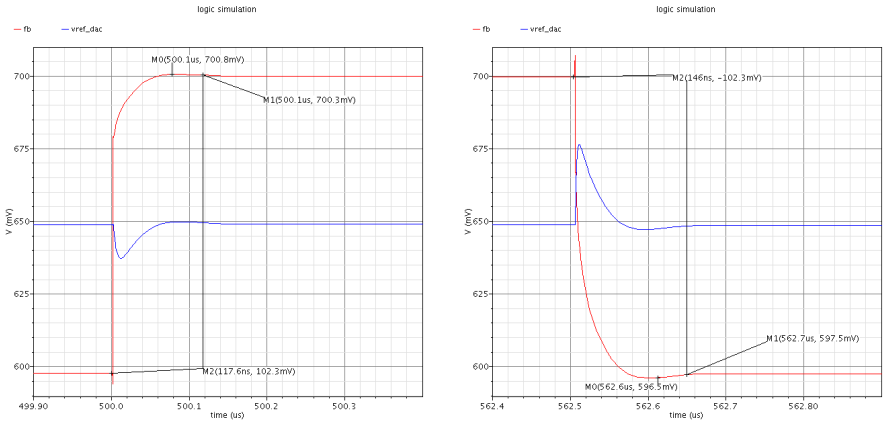


Figure 64: Settling of V_{fb} and V_{ref} with $C_C = 2pF$ and no C_F to reduce glitches.

Though the DAC settles fast (in the order of 100ns, see figure 64), the integrated voltage error and the overshoot causes the resolution of the DAC to decrease some. To overcome this, two capacitors, C_F, of 200fF each were placed at the two nodes in order to reduce ΔV when switching states by buffering the injected charge. C_C was also increased from an initial 2pF to 2.6pF in order to maintain a phase margin of 75°. Though the final settling time increases some, the initial step response becomes much faster due to a decrease in $\Delta V_{ref}^{\pm}$, as seen in figure 65:

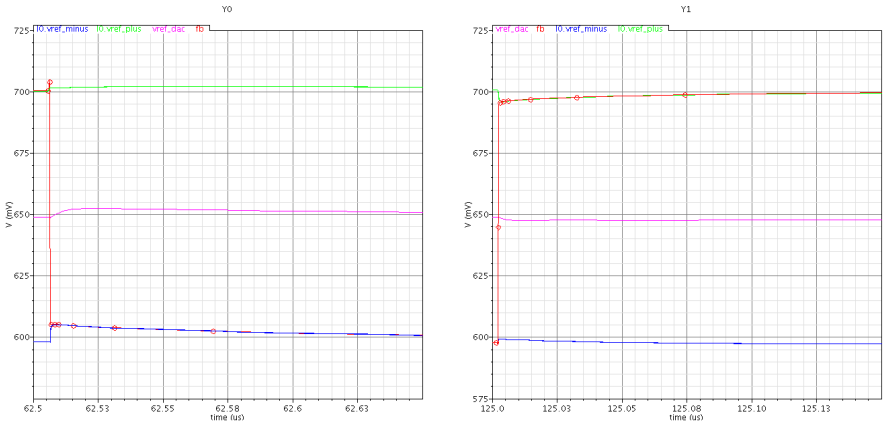


Figure 65: Transient response of nodes $V_{fb}, V_{ref}^{+}, V_{ref}$ and V_{ref}^{-} when switching states.

After adding these load capacitors, the time constants became approximately:

$$\tau_{ref}^{-} \approx (\frac{1}{g_{m1}} + 2 \times 250k\Omega)200fF \approx 140ns \tag{54}$$

$$\tau_{ref}^{+} \approx \frac{1}{g_{m1}} 200fF \approx 40ns \tag{55}$$

For the reference to settle within 1% of its final value, 184ns and 644ns (4.6τ) are required for V_{fb} to rise and fall, respectively. Though $\tau_{ref}^{-} > 3 \times \tau_{ref}^{+}$, the integrated error is negligible. The settling is depicted in figure 65, and the transient response seen at V_{ref}^{+}, V_{ref} and V_{ref}^{-} can be seen in figure 66.

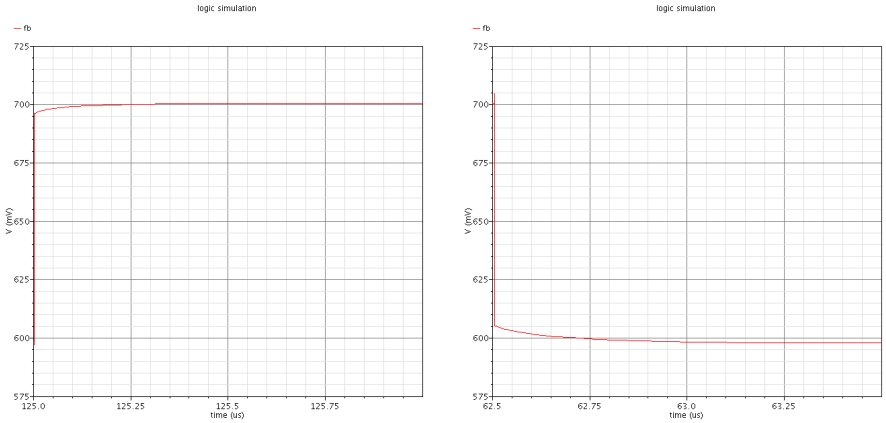


Figure 66: Rising and falling edge of V_{fb}. The settling times are consistent with what we expect.

5.8 PVT

The DAC was simulated against PVT variations and key characteristics were extracted. The results are listed in the table below (18).

Corner	V_{DD}	T [°]	$V_{ref,out}$	V_{ref}^{+}	V_{ref}^{-}	ΔV_{ref}^{+}	ΔV_{ref}^{-}	$\Delta V_{ref}^{\pm}$	I_{tot} [nA]
SS	**1.08**	**27**	**583.4**	**633.7**	**533.4**	**50.27**	**-50.09**	**100.36**	**396**
	1.2	-40	648.0	698.1	598.1	50.13	-49.87	100.00	396
		0	648.5	698.9	598.4	50.34	-50.11	100.45	401
		27	648.8	699.3	598.5	50.54	-50.31	100.85	403
		50	649.0	699.8	598.5	51.54	-51.32	102.86	408
	1.32	27	583.8	634.5	533.3	50.73	-50.46	101.19	406
TT	1.08	27	583.8	634.5	533.3	50.73	-50.46	101.19	406
	1.2	-40	648.0	698.5	597.9	50.48	-50.10	100.58	405
		0	648.6	699.5	598.1	50.91	-50.56	101.47	409
		27	**648.9**	**700.2**	**598.0**	**51.28**	**-50.93**	**102.21**	**412**
		50	649.2	700.9	597.9	51.64	-51.29	102.93	414
		120	650.4	703.7	597.5	53.27	-52.91	106.18	426
FF	1.08	27	583.8	636.1	531.9	52.32	-51.89	104.21	423
	1.2	-40	647.7	699.4	596.5	51.75	-51.19	102.94	421
		0	648.4	701.2	596.1	52.83	-52.28	105.11	430
		27	648.8	702.5	595.7	53.68	-53.13	106.81	437
		50	649.2	703.8	595.2	54.55	-53.98	108.53	444
		120	650.7	710.6	591.5	59.88	-59.23	119.11	491
	1.32	**27**	**713.8**	**769.3**	**659.0**	**55.50**	**-54.80**	**110.30**	**455**

Table 18: DAC reference voltages (in [mV]) and current consumption versus PVT.

In summary, the DAC settles fast and produces fairly accurate references. $\Delta V_{ref}^{+} > \Delta V_{ref}^{-}$ as a result of a small current escaping from the V_{ref} node in form of gate-to-channel leakage through the large input transistors of all the OTAs. The current mirror in the source-follower mirrors a slightly larger current than the buffer mirror because the drain node of the cascode mirror is connected to V_{ref}^{-}. V_{ref}^{-} is high enough that the subthreshold current mirror begins to draw more current.

5.9 $\Delta\Sigma$-ADC

Transient response

The transient response of important nodes in the DSM are shown in figure 67 as V_{in} is swept linearly from V_{ref} up to $V_{ref} + 50mV$ and down to $V_{ref} - 50mV$.

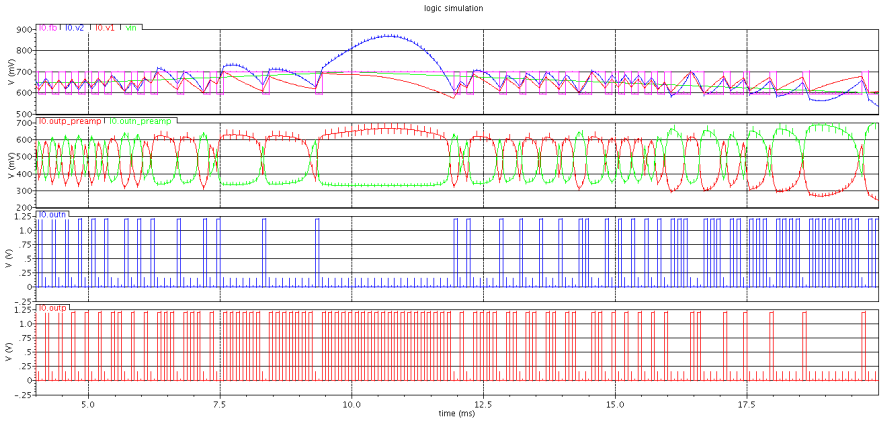


Figure 67: Transient response of nodes V_{in} (green), V_1 (red), V_2 (blue), V_{fb} (pink) above, $V_{out,preamp}^{+}$ (red) and $V_{out,preamp}^{-}$ (green) in the middle, and $V_{out,comparator}^{-}$ (blue) and $V_{out,comparator}^{+}$ (red) in the two bottom plots. V_1 and V_2 are the first and second integrating node of the loop filter, while V_{fb} is the negative feedback voltage provided by the DAC.

Assuming that the input signal can be regarded as a DC signal compared to the high frequency feedback signal, the ramp of the first integrator should be equal to:

$$V_{1,T+\Delta t} \simeq V_{1,T} + \frac{-V_{in}}{\tau_1}\Delta t \tag{56}$$

Where $\frac{1}{\tau_1} = \frac{G_{m,fb}}{C_1}$. Ideally, $G_{m,fb} \simeq \frac{g_{m1}}{R_S} \approx 0.85\mu S$, but the effective $G_{m,fb}$ was found to be 757nS. Therefore, we expect the integrating step to be approximately:

$$\Delta V_1 \approx -V_{in}\frac{\Delta t}{\tau_1} \approx -50mV\frac{G_{m,fb}}{C_1}\Delta t \approx -50mV\frac{757nS}{117pF}125\mu s \approx 40mV \quad (57)$$

Figure 68 confirms the step size of the first integrating node. Looking at the second integrator:

$$V_2(t) = \int_T^{T+\Delta T}\frac{-V_1}{\tau_2}\,\mathrm{d}t = \frac{-V_{fb}}{\tau_1\tau_2}\int_T^{T+\Delta T} t\,\mathrm{d}t = \frac{-V_{fb}}{\tau_1\tau_2}\left[\frac{t^2}{2}\right]_T^{T+\Delta T} \quad (58)$$

Assuming $V_1 = V_2$ at T=0, we find that the voltages will cross again at:

$$\frac{-V_{fb}}{\tau_1}t = \frac{-V_{fb}}{\tau_1\tau_2}\frac{t^2}{2} \Rightarrow t = 2\tau_2 \approx \frac{136.554pF}{757nS} \approx 90.2ns \approx 72.2\%\Delta T$$

The second integrator step is confirmed looking at the 2^{nd} positive and 5^{th} negative slope in figure 68. Analogous with the -6dBFS scaling of the integrators, we see that as V_{in} exceeds -6dBFS, or 25mV, V_1 becomes gradually more nonlinear, and the DSM needs more and more time to pull V_2 back to V_{ref} since $V_{in} - V_{fb} \to 0$. At the point where $V_{in} > V_{fb}$, the DSM becomes disabled as it can never integrate itself back to V_{ref}. These effects can be observed in figures 67 and 69, where V_2 starts to drift towards V_{DD} when $V_{in} \approx +50mV$.

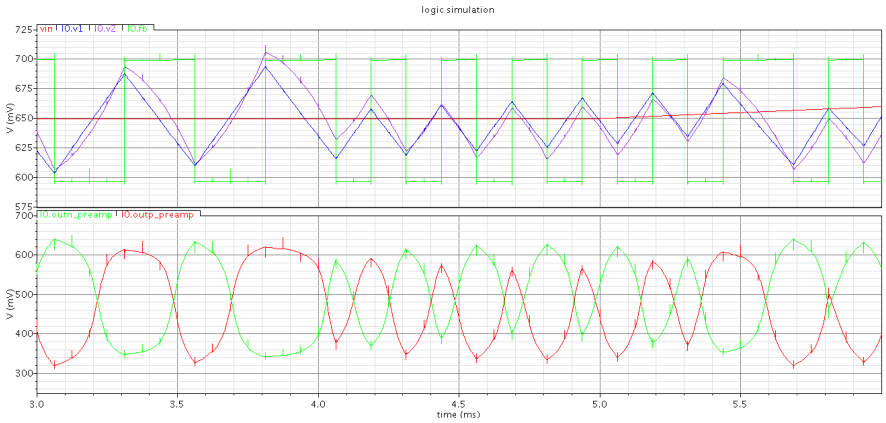


Figure 68: Zoom in of transient response.

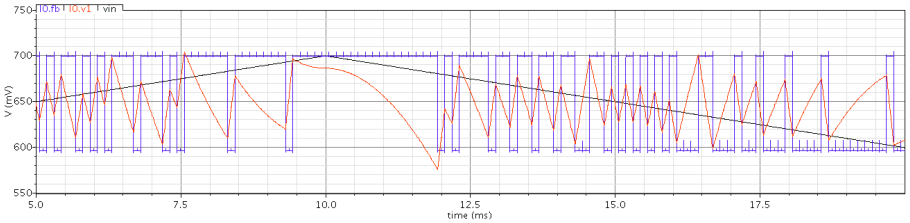


Figure 69: Transient response of V_1 (red), V_{fb} (blue) and V_{in} (black).

A 3-bit MUX was implemented for probing various nodes in the ADC. The readout settings are listed in table 19. To minimize the MUX's interference with the circuit, transmission gates were used as inputs to reduce parasitic capacitance.

Test-MUX setting	Node
000	V_{ref}
001	V_{fb}
010	V_1
011	V_2
100	V_{b1}
101	V_{b2}
110	V_{p-casc}
111	V_{n-casc}

Table 19: Setting for test-MUX

The test-MUX setting were swept from 0 to 7 during runtime and the transient response can be seen in figure 70

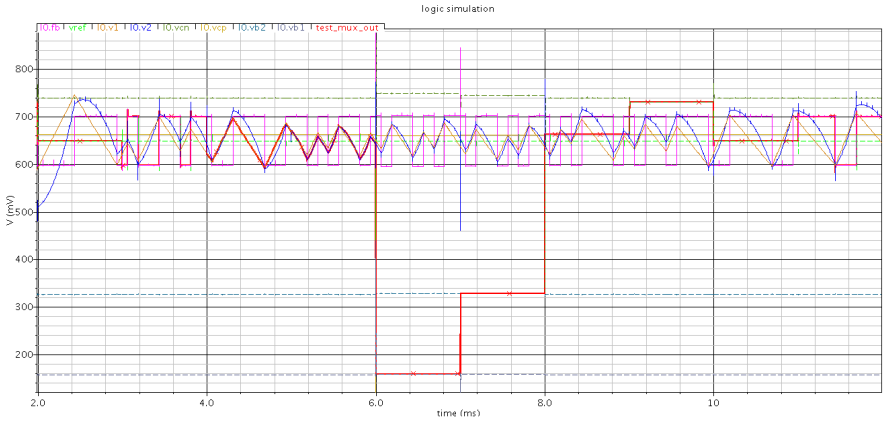


Figure 70: Transient simulation when sweeping test-MUX setting.

A non-post-filtered decimation of the feedback when $V_{in} = 0V$ are depicted in the figure 71. The offset of the decimated signal increases with AGC setting, from approximately 649.5mV to 657mV.

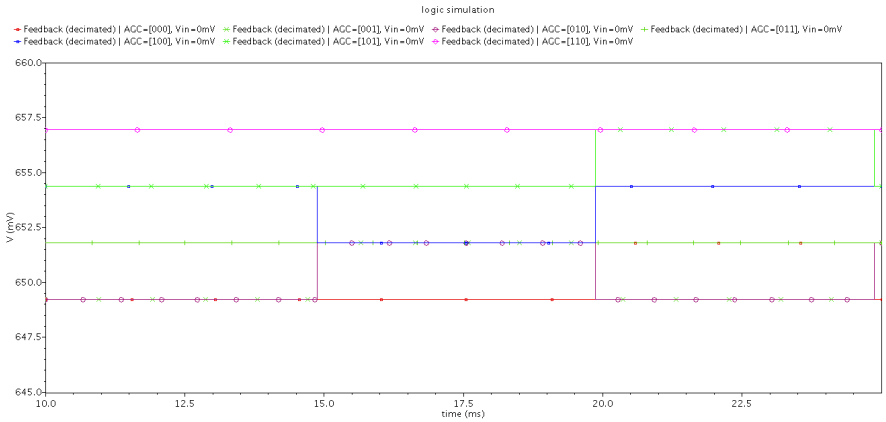


Figure 71: Non-post-filtered decimated offset when $V_{in} = 0V$.

5.10 Power consumption

The focus of the ADC is to minimize power consumption, and extensive testing was therefore done to map the current dissipation. Figure 72 displays the total current consumption of the ADC in addition to the current consumption of various blocks in typical corner. As it can be seen the total current consumption, including biasing network and delay-element (reusable blocks), are $3\mu A$. The reason why the power consumption changes between clock cycles is because the digital blocks consume more current when Q and the clocks are low since the PMOS transistors with larger gate are are forward biased.

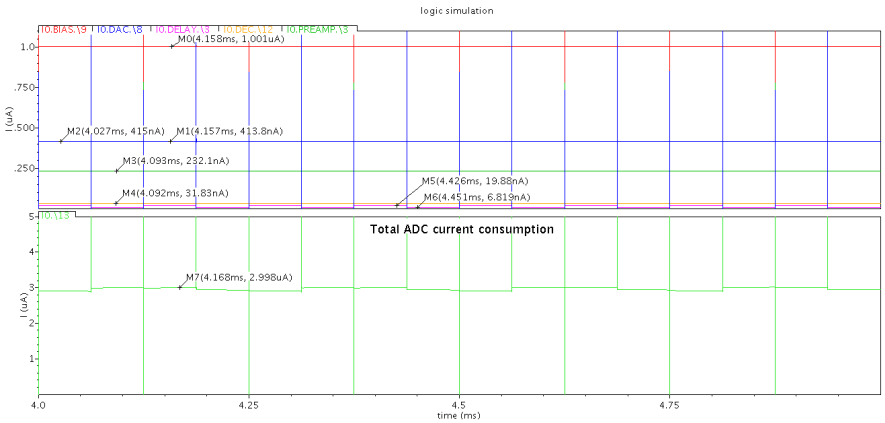


Figure 72: The upper plot displays the current consumption of the following blocks for typical corner: Bias (red), DAC (blue), delay (pink), decoder (yellow), preamplifier (green). The lower plot displays the total current consumption of the whole ADC.

Figure 73 depicts the same plot as above, but includes view of peak currents. The maximum peaking is under $250\mu A$, which in most systems are acceptable peak currents. Also, these measurements are taken without any decoupling capacitor or any voltage regulator connected to V_{DD}. Often both or either of the two are used, especially in low-power circuits, and will reduce peak currents drastically. The major contributor of peak currents are caused by the delay element whose large transition causes the inverters to open fully for a longer time, increasing dynamic current consumption in the form of larger and wider peaks. Figure 74 show how the peak currents are affected by rising and falling edges. The large peak currents occur on negative clock edge, as that is when the SR-latch latches. Furthermore it can be seen that the peaks are larger when Q and $\overline{Q}$ changes state than when Q and $\overline{Q}$ remain unchanged.

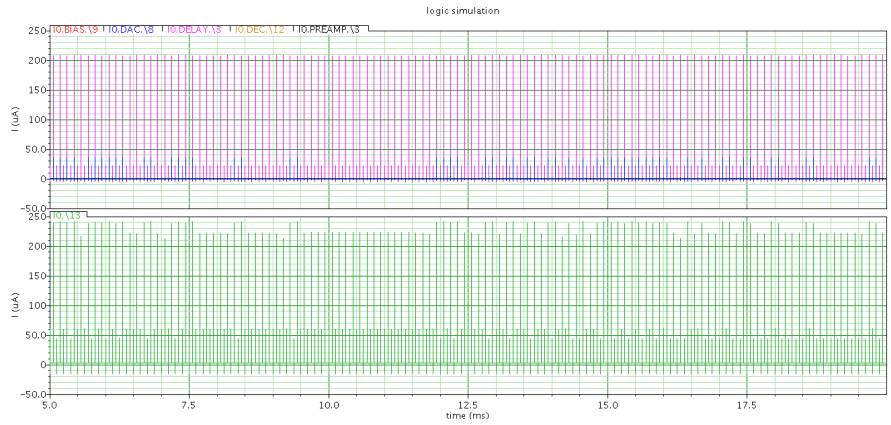


Figure 73: Peak current consumption, same notation as figure above (except for the color of the preamp has been changed from green to black).

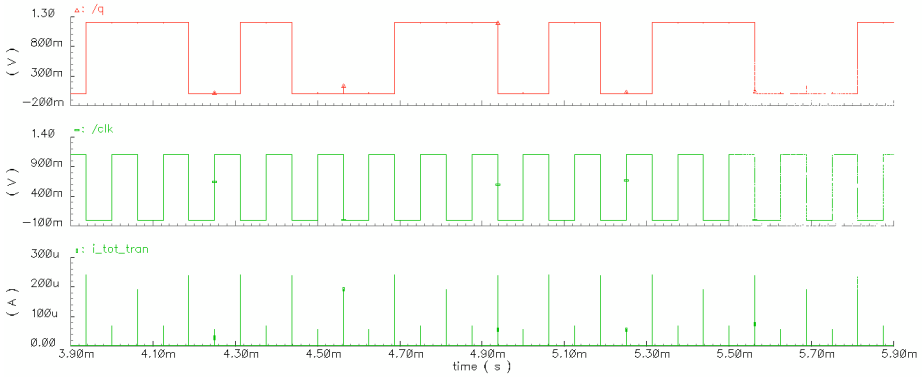


Figure 74: Peak current consumption versus clock- and latched signal signal.

The peak currents versus nominal, slow and fast corner are depicted in figure 75.

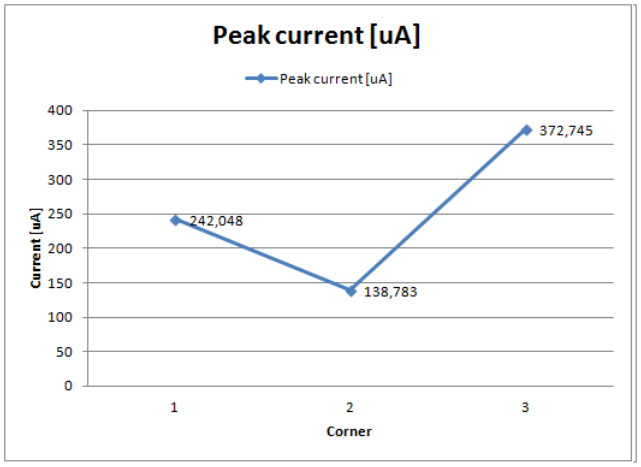


Figure 75: Peak current consumption versus nominal, minimum and maximum corner.

In tables 20 and 21, a complete overview of the current consumption in the ADC is shown against nominal, slow and fast corner. Notice that three additional blocks have been added:

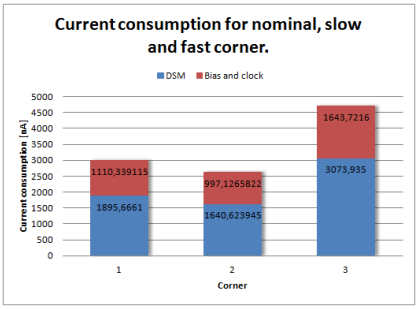
- V_{SS} enabler
- V_{DD} enabler
- Clock enabler

Component	**nom***	**min****	**max*****
AGC	393.300	341.407	458.242
OTA 1	388.191	337.010	452.269
OTA 2	390.572	339.101	460.145
Preamp	230.596	208.963	264.087
Comparator	27.204	6.453	329.844
Latch	15.860	3.708	108.547
DAC	415.637	398.275	463.491
Decoder	34.306	5.707	537.310
Sum per DSM	**1895.666**	**1640.624**	**3073.935**
Bias	1088.980	987.750	1298.800
Delay element	21.342	9.370	264.828
V_{SS}/V_{DD} enabler	0.010	0.004	44.015
Clock enabler	0.008	0.003	36.078
Sum other components	**1110.339**	**997.127**	**1643.722**
Sum total	**3006.005**	**2637.751**	**4717.657**
Peak current [uA]	**242.048**	**138.783**	**372.745**

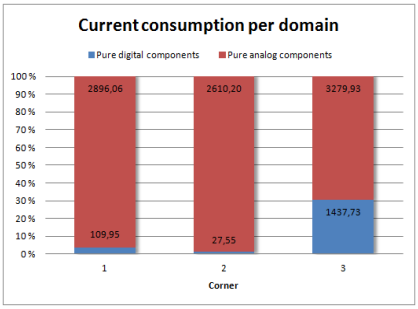
Table 20: Summary of power consumption in ADC in nominal, slow and fast corner.

Component	Subcircuit	nom*	min**	max***
Bias	Resistor string	167.0070	150.1740	184.0020
	Buffer	253.2940	206.4400	373.2210
	Other (bias branches)	668.6790	631.1360	741.5770
DAC	Buffer	200.8190	193.3960	213.8850
	Source Follower	210.1750	203.5640	233.4840
Decoder	Inverter. minimum size	5.6079	1.1521	52.0021
	3-Port NAND-gate	1.2504	0.0428	47.7766
Comparator	Latch	5.9784	1.0688	233.8300
SR-latch	Transmission gate	0.0020	0.0016	6.5517
	2-Port NOR-gate	4.9550	1.1271	40.8090

Table 21: Current consumption of submodules within the main blocks.



(a) Total current consumption per DSM and for a complete 1-channel system (i.e. including bias and clock delay blocks).

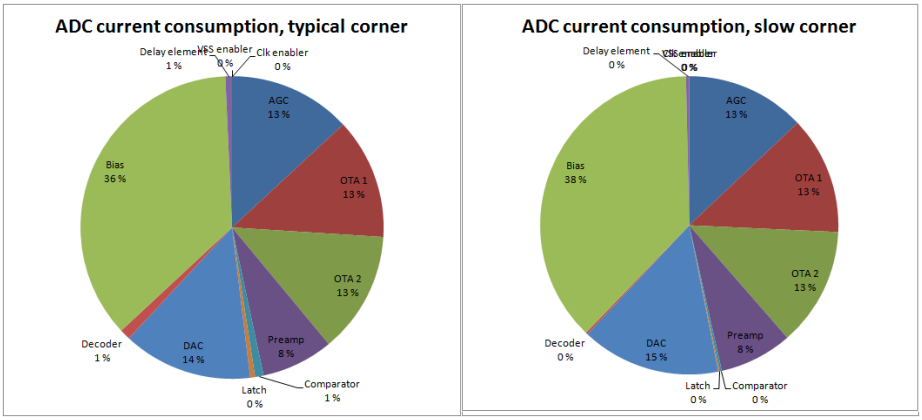


(b) Contribution from digital and analog circuitry on total current consumption.

Figure 76: Total current consumption.

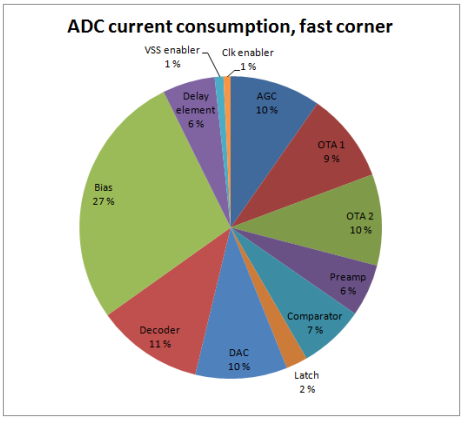
Figure 76a represents the total current consumption of the ADC. The current increases drastically for fast corner. The main reason for this is that the gate-to-channel leakage in digital circuitry increases drastically when $V_{DD} = 1.32$. This is not the case for the analog circuitry because of weaker biasing as explained in section 2.5.1. Figure 76b shows the relation between analog and digital current consumption against corners (including all sub-components, such as inverters).

The analog current consumption varies with $+13.26\%$ and -9.88% from the nominal corner, where the main contribution to the difference is caused by the gate-to-channel leakage in the triode CMFB. For the digital circuitry on the other hand, the current consumption varies with $+1307.62\%$ and -74.96%.



(a) Typical corner

(b) Slow corner



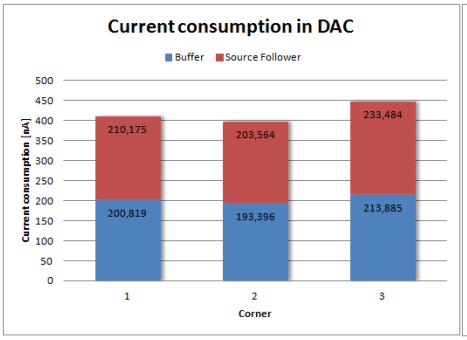
(c) Fast corner

Figure 77: Total current consumption ratio of submodules in minimum, nominal and maximum corners.

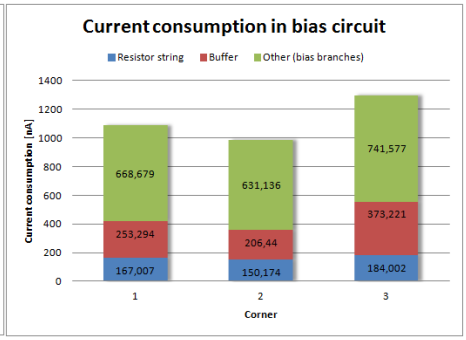
Figure 77 shows how the total current consumption is distributed between the different submodules. For typical and slow corners, almost all power is consumed by the analog circuitry. In the fast corner, contributions from especially the comparator, the delay element and the AGC decoder increase drastically. In the comparator the majority of this contribution comes from gate-to-channel leakage through the PMOS gate of the latch when turned hard on. The same can be found for the delay element. As for the decoder, only minimum size devices are used, but the total amount of logic gates used adds up a significant leakage current, especially in NAND gates, where three PMOS devices are forward biased at the same time.

5.10.1 Submodule current consumption distribution against corners

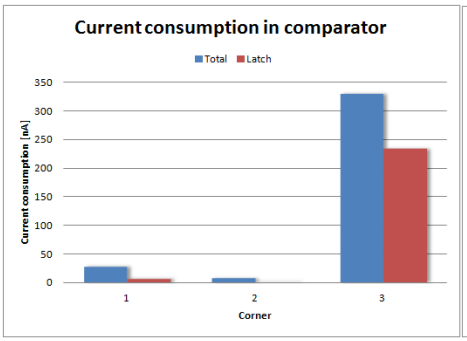
The current consumption of the blocks divided into submodules are shown below.



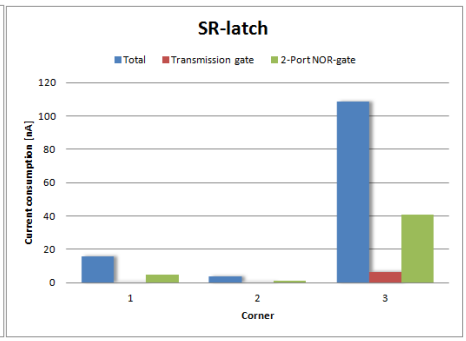
(a) DAC current consumption.



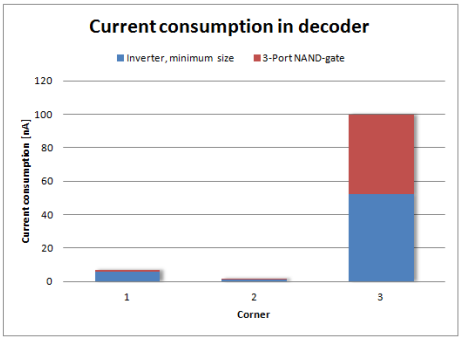
(b) Bias network current consumption.



(c) Comparator current consumption.



(d) SR-latch current consumption. Note that the contribution from the NOR gate only reflects a single gate, and therefore contributes with a total of 80nA. The same accounts for the transmission gates.



(e) Decoder current consumption.

Figure 78: Submodule current consumption in minimum, nominal and maximum corner.

Looking at the bias circuit, it can be seen that the current consumed by the buffer increases drastically. This is due to increased gate leakage in the triode CMFB used in the bias. The gate tunneling current is drawn from the output node of the buffer which has to draw extra current from V_{DD} to compensate. The same accounts for the buffer in the DAC, which has to draw extra current to compensate for increased leakage in the OTAs' input transistors.

The total power consumption is given by:

$$P_{tot} = I_{tot,avg} \times V_{DD} \tag{59}$$

The power consumption of the AFE therefore becomes:

Corner	**Power**
Nominal	$3.607\mu W$
Minimum	$2.849\mu W$
Maximum	$6.227\mu W$

Table 22: Total AFE power consumption

5.11 Area consumption

Large time constants are required to achieve the required loop filter characteristics. With the given bias currents and voltage headroom, the input transistors are forced to operate with a low to weak inversion. There is little room for changing the g_m-values other than reducing the bias current. With a fixed bias current and coefficients, the required area of the ADC is practically predestined. The area estimations have been divided into comparator area, resistor area and MOSFET area.

5.11.1 Capacitor area

The total capacitance in the ADC is as follows:

- $3 \times 100fF$ in the delay element.
- $(26 + 4) \times 100fF$ in the DAC.
- $C_1 = 117.038pF$
- $C_2 = 136.554pF$

The total capacitance is:

$$C_{tot} = 257.6pF \tag{60}$$

The 6-layer MOM capacitor has a capacitance density of $2.3fF/\mu m^2$. The total required area without routing therefore becomes:

$$A_C \approx 0.112mm^2 \tag{61}$$

5.11.2 Resistor area

The resistors used in the ADC are:

- $24 \times 300k\Omega$ in the resistor string.
- $2M\Omega$ in the bias circuit.
- $2 \times 1M\Omega \times 3$ in the three G_m-cells.
- The feed forward resistor $R_Z = 1M\Omega + 300k\Omega + 15525k\Omega$.

The total resistance is:

$$R_{tot} = 16.655M\Omega \tag{62}$$

The resistance area density using minimum width resistors are $0.001mm^2/M\Omega$.

The total required area without routing therefore becomes:

$$A_R \approx 0.01665mm^2 \tag{63}$$

5.11.3 MOSFET area

The area of the MOSFETs are the most flexible in the design. The minimum area is primarily limited by matching and thermal- and flicker noise. Large arrays of transistors in the G_m-cells and the bias circuitry were used to reduce flicker noise, increasing the area substantially. The area of a transistor $A_M = A_D + A_S + A_G$, and can be estimated as $5 \times W \times L$. The area of the sub circuits (excluding resistors and capacitors) becomes:

- $A_{AGC} \approx 2496.546\mu m^2$
- $A_{OTA_1} \approx 2495\mu m^2$
- $A_{OTA_2} \approx 2495\mu m^2$
- $A_{Preamp} \approx 17.56\mu m^2$
- $A_{Comparator} \approx 2.994\mu m^2$
- $A_{\text{Delay element}} \approx 0.66\mu m^2$

- $A_{SR-latch} \approx 1.766\mu m^2$
- $A_{DAC} \approx 1220.464\mu m^2$
- $A_{Bias} \approx 2306.13\mu m^2$
- $A_{extra} \approx 2.344\mu m^2$

The total area required by MOSFET devices therefore becomes:

$$A_M \approx 0.011mm^2 \tag{64}$$

5.11.4 Estimated area consumption including routing

$$A_{tot} \approx A_C + A_R + A_M \approx 0.139688mm^2 \tag{65}$$

Typically 30-50% extra area is used for routing and guardrings. The total area consumption should therefore come between:

$$A_{tot,min} = 0.1816mm^2 \tag{66}$$
$$A_{tot,max} = 0.2095mm^2 \tag{67}$$

5.12 Input referred noise

The AGC gain setting was swept and the input referred noise was measured. Figure 79 shows the equivalent input referred noise within the bandwidth.

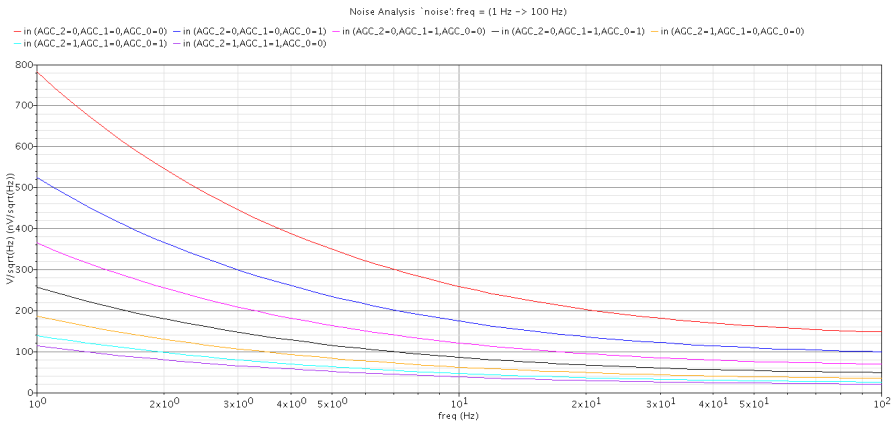


Figure 79: Equivalent input referred noise for $AGC = [000 \rightarrow 110]$ within the bandwidth.

The input referred noise was integrated over the bandwidth and $V_{n(RMS)}$ was found. $V_{n(pp)}$ was then found from $6.6 \times V_{n(RMS)}$. The results are listed in table 23. Derivations of the noise contributions are shown in appendix 9.

AGC	$V_{ni(RMS)}$	$V_{ni(pp)}$		P_{ni}		P_{ni}/Hz
	$[\mu V]$	$[\mu V]$	$[-dBFS]$	$[pW]$	$[-dBFS]$	$[-dBFS]$
000	18.65	111.9	53.00	347.82	65.56	85.56
001	12.54	75.22	56.45	157.25	69.00	89.00
010	8.738	52.43	59.59	76.35	72.14	92.14
011	6.174	37.04	62.61	38.11	75.16	95.16
100	4.456	26.74	65.44	19.86	77.99	97.99
101	3.324	19.94	67.98	11.05	80.54	100.54
110	2.694	16.16	69.81	7.258	82.36	102.36

Table 23: RMS and Peak-to-Peak input referred noise in typical corner, T=27°C.

The input referred noise does not meet the standard for AGC settings 000, 001 and 010, but a $50\mu V$ input signal is detectable employing a higher AGC gain setting. The main noise contributors are M7 and M8 in the AGC. Second comes M1 and M2. The input referred noise decreases with $A_{v,STF}$ as expected. It was also found that the 20 highest noise contributors were all flicker noise. The two last posts in table 23 lists the input referred noise power relative to a full scale input signal and the equivalent flat-band amplitude of the noise power to indicate what level the noise power lies on.

5.13 ADC Conversion performance

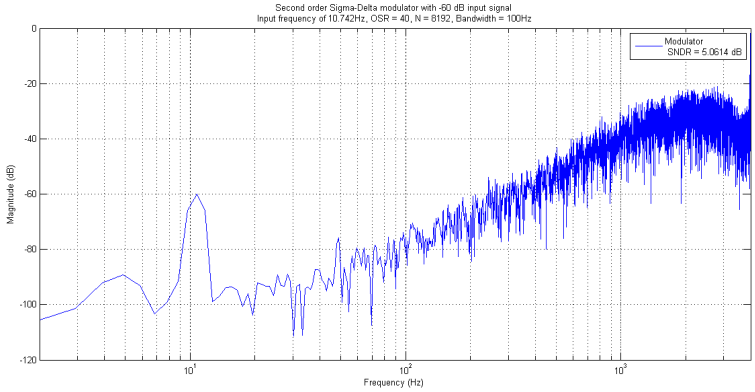
The ECG standard is normally tested with a 10Hz signal. For good FFT-windowing, the following input frequency was used:

$$f_{in} = \text{prime number} \times \frac{10^a}{2^{10}} = \text{prime number} \times \frac{f_s}{2^b} \approx 10Hz \tag{68}$$

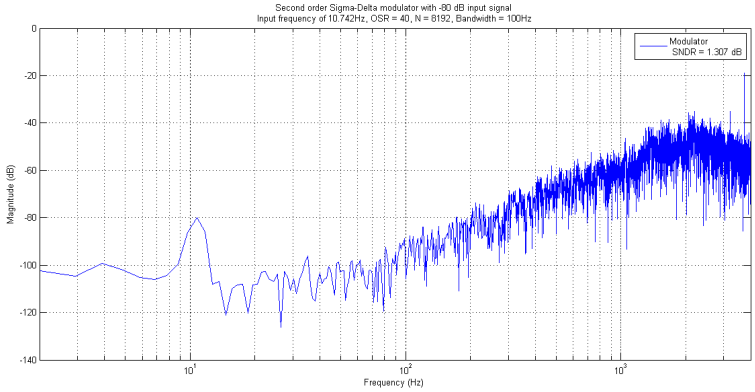
$$\Rightarrow f_{in} = 11\frac{1000}{1024}Hz = 11\frac{8000}{2^13}Hz = 10.7421875Hz \tag{69}$$

The input amplitude and AGC setting was swept. 8192 samples were taken from each sweep and a Hanning-FFT was performed on the recorded data. After removing the input signal from the FFT, the spectrum content up to a 100Hz was integrated and the SNDR was estimated. The FFTs have been referred to the input amplitude instead of the output amplitude. This means that the quantization noise floor also will be suppressed with $A_{v,STF}$ related to $V_{in} = 0dB = 50mV$. In reality, the ADC sees the input signal as $V_{in} \times A_{v,STF}$, and the quantization noise floor is unchanged. In example, an input amplitude of $V_{in} = -12dB$ and a signal gain of $A_{v,STF} = 6dB$ is seen and treated as $V_{in} = -6dB$ and $A_{v,STF} = 0dB$, and they both have the same quantization noise floor

when referred to the output (-6dB). When referred to the input, the noise floor in the case of applied signal gain must be decreased with approximately the same amount as the signal gain.



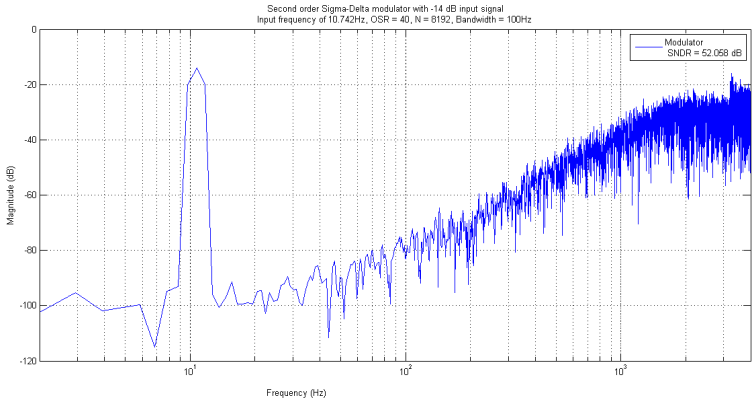
(a) $V_{in} = 50\mu V$, AGC=000



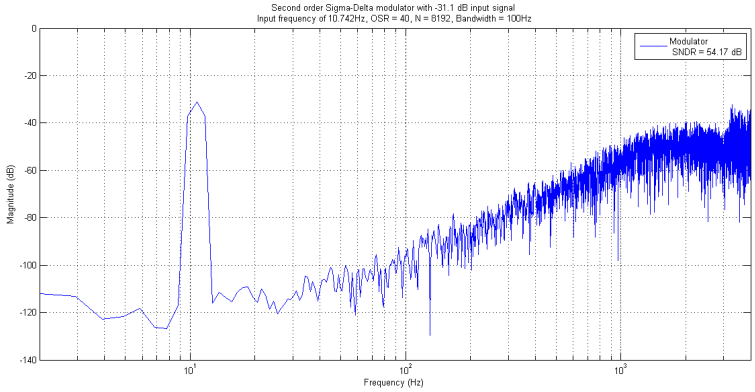
(b) $V_{in} = 5\mu V$, AGC=110

Figure 80: FFT for $AGC = [000, 110]$, with V_{in} close to the dynamic range of each AGC setting.

Figure 80a and 80b show that the ADC is able to convert a $50\mu V$ input signal, with a SNDR of 5.06dB and 1.31dB, respectively. Adding the input referred noise power from section 5.12, the SNDR including input referred noise becomes 2.29dB and -1.21dB respectively. Adding the budgeted 5% extrinsic noise, the final SNDR would become 2.08dB and -1.42dB.



(a) $V_{in} = 10mV$, AGC=000



(b) $V_{in} = 1.4mV$, AGC=110

Figure 81: FFT of $V_{in} = [1.4, 10]mV$ for AGC=[000,110]. The signal gain of AGC=[110] amplifies the 1.4mV signal up to a 10mV level, resulting in the two settings producing the same output signal, with approximately the same SNDR values.

Figures 81a and 81b shows the FFT for equivalent output voltages of 10mV for AGC=[000,110], with their respective SNDR values of 52.07dB and 54.17dB. Including the input referred noise power, the new values for SNDR becomes 48.81dB and 54.01dB respectively. Adding 5% extrinsic noise we get 48.59dB and 53.80dB.

Figure 82 depicts the SNDR plotted against V_{in} for the different AGC settings. As expected the programmable gain of the AGC allows for the SNDR of the ADC to remain high for a broader range of input amplitudes, allowing for signals as low as 0.5mV to be converted with a SNDR of over 43.5dB. For a 5mV input signal, the minimum gain setting (AGC=[000]) converts the signal with a 46.5dB SNDR. The dynamic range (without taking input referred noise into account), is over 80dB, and the peak SNDR that was measured out of the taken samples was found to be 60.8dB. This equals to an ENOB of 9.81. From table 23 it was found that $V_{ni(pp)}|_{\text{AGC=[110]}} = 16.16\mu V \simeq -70dBFS$. The

SNDR measured at -70dBFS for AGC=[110] is 14dB. The SNDR including input referred noise becomes 10.48dB, and adding another 5% extrinsic noise from budget, we get a total SNDR of 9.99dB. The $\Delta\Sigma$-ADC can therefore convert the smallest detectable input signal (-70dBFS), with a SNDR of 9.99dB. Disregarding $V_{ni(pp)}$, the dynamic range becomes approximately 80dB when including input referred noise.

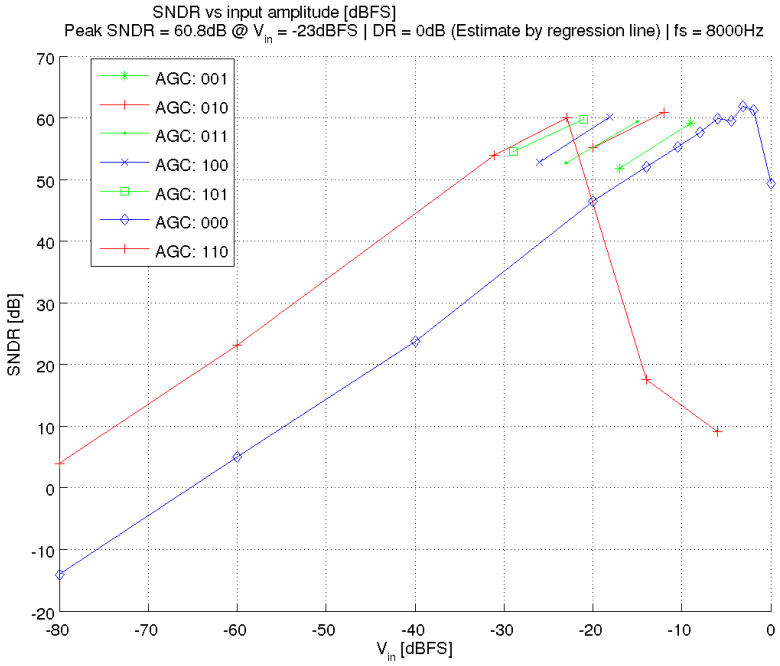


Figure 82: SNDR (input referred noise excluded) for all AGC gain settings and V_{in} swept.

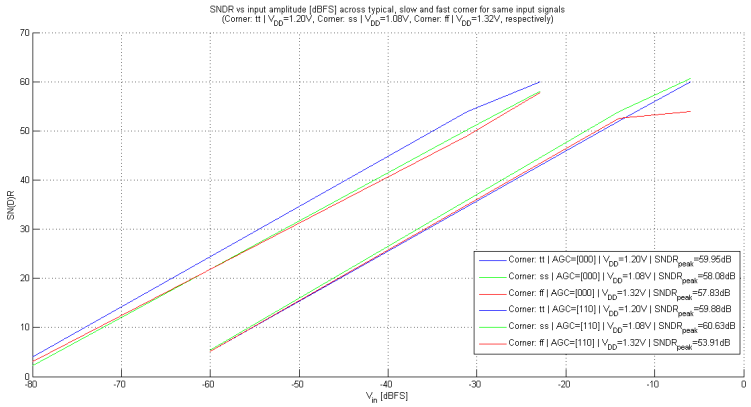


Figure 83: V_{in} sweep for AGC=[000,110] versus nominal, minimum and maximum corner.

Figure 83 depicts some samples for minimum and maximum AGC gain settings versus the nominal, minimum and maximum corner. Looking at the case of AGC=[000], the SNDR is slightly higher in the slow corner as a result of the increased linearity in the OTAs. As for the fast corner, the SNDR peaks earlier because the linearity is poorer. As for the case of AGC=[110], the test performed is not quite accurate as the tests were measured with the same input voltage, and not adjusting V_{in} to the maximum AGC gain for each corner. Effectively, this means that the SNDR in the slow corner should be almost 1dB higher. As for the fast corner, the signal is amplified more, but due to reduced linearity and NTF gain in this corner these results should give a good indication of the performance to expect. Figure 84 shows the FFT for AGC=[000] and $V_{in} = 25mV$ against corners. It shows how the quantization noise suppression is fairly equal, but the peak SNDR being limited by variations in the linearity. Also, the jump in the quantization noise occurring at $F_s/4 = 2000Hz$ is the noise OBG[10] (NTF_{max}), which is related to the phase margin of the filter. The second harmonic component increase by 11.56dB from the minimum corner to the typical corner, and then increases another 10.98dB from typical corner to maximum corner.

[10]Out-of-Band-Gain

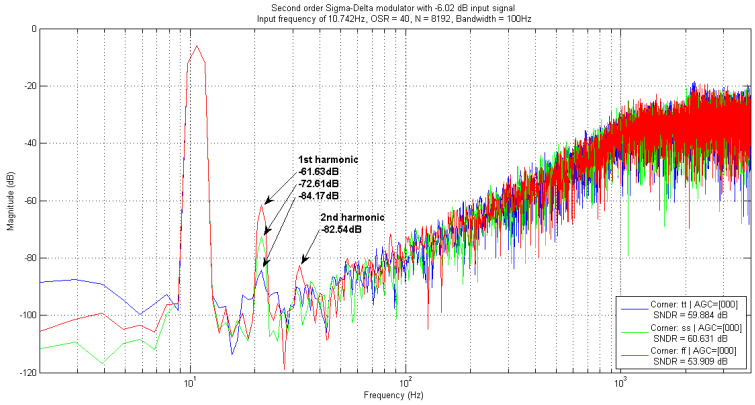


Figure 84: FFT for a 25mV input signal, AGC=[000] against nominal, minimum and maximum corners.

Figure 85 shows the FFT for AGC=[110] and $V_{in} = [5mV, 10mV]$. The input signal of 5mV is still within reference range and near the peak SNDR value. The 10mV input signal is amplified by a factor of approximately 7. The amplified input signal carried on integrator nodes V_1 and V_2 is therefore almost 70mV, larger than the feedback reference, and the DSM becomes overloaded. As a result, the SNDR becomes greatly reduced with large harmonics and a high quantization noise floor.

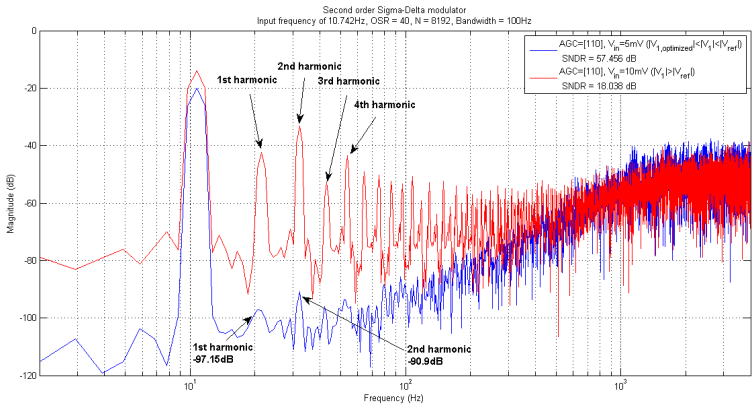
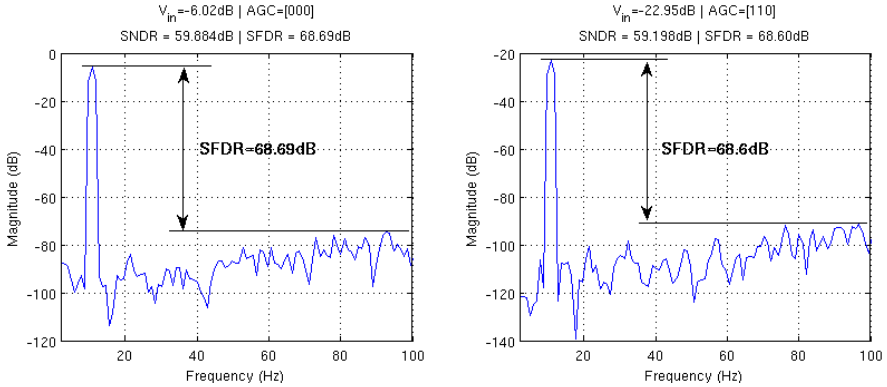


Figure 85

The SFDR was measured for $V_{in} \times A_{v,STF} = -6dB$ since the integrators were optimized for that input level. In figure 86a and 86b the SFDR is depicted within the 100Hz bandwidth on a linear x-axis.



(a) SFDR for a -6dB input signal, AGC=000 (b) SFDR for a -23dB input signal, AGC=110

Figure 86: SFDR within 100Hz bandwidth.

Looking at the figures in 86, it can be seen that the SFDR in the plot is limited by quantization noise close to 100Hz due to reduced in-band noise suppression gain. This implies that a higher input amplitude can be applied without increasing the peak noise. In effect this means that the peak SFDR can reach a few dB higher than what is depicted in this figure.

6 Discussion

From the estimated SNR plot in figure 19 it was found that for an ideal system with $V_{ni(RMS)} = 7.58\mu V$ and including the budgeted extrinsic noise, the dynamic range should be 70dB. If the input referred noise and extrinsic noise is included into figure 82, the dynamic range for AGC=[000] is 62.5dB. The 7.5dB loss is less than budgeted and meets the spec. As for peak SNDR values when including all noise sources, the peak SNDR for AGC=[000] is reduced from 60.8dB to 58.37dB which equals to an ENOB of 9.4 bits. For AGC=[110], the peak SNDR is reduced from 59.95dB to 59.69dB, or an ENOB of 9.62. Section 3 specified that a 6mV input signal should be converted with a SNDR greater than 43.5dB (ENOB $\geq$ 7 bits). For AGC=[110] a 6mV signal will have an output amplitude of 42.52mV and harmonics will have started to degrade the SNDR. However, for AGC=[100], a 6mV input signal translates to a 23.9mV output signal which is in the region of the peak SNDR for that gain setting. For AGC=[000] the SNDR is 47.5dB without extrinsic and intrinsic noise. Including all noise sources the SNDR is degraded to 44.09dB for AGC=[000], which is still greater than specified. Increasing the AGC setting from [000] and up to [100] will keep increasing the SNDR until it peaks at approximately 57.7dB. The SFDR was found to be 68.6dB, but if $V_{ni(pp)}$ is included, the SFDR is reduced for all gain settings except AGC=[110]. For all other the gain settings the peak input referred noise voltage presented in -dBFS is shown in table 23.

In typical ECG circuits, 50Hz power-line interference should be $\leq 5\mu V$. Ways to deal with the common-mode includes ground isolation between AFE and earth ground, using a right leg drive[11], and implementing $\gtrsim 100dB$ CMRR in the AFE. In $\Delta\Sigma$-ADCs, the digital post-filter is one of the architecture components and can be used to achieve good rejection of power-line frequencies. The telescopic OTA has a high intrinsic common mode rejection, and the large arrays of transistors helps improve the rejection and reduce the spread. The DSM only needs enough CMRR to ensure that the 50Hz common-mode won't overload the DSM. For a 1.5V power-line interference, only 30dB CMRR is required to suppress the common signal below full scale range. Hence, the common-mode rejection of the pseudo-differential ADC is sufficient to allow for a fully-differential input signal.

The output bitstream has to pass through digital filtering and decimation after being converted by the ADC, so the signal is still subject to degradation of SNDR. The digital filter should have a bandpass transfer function from 0.67Hz to 100Hz to remove any residue DC components and out-of-band noise, and a notch at 50Hz (or 60Hz if used in the US) to remove any residue common-mode signal, such as power-line interference. A typical implementation for ECG post filtering is to use a five stage filter consisting of two comb filters followed by two cascaded N-th order half-band filters and finally a bandpass filter consisting of an all-pass and a band-stop filter.

[11] Driving the patient with an out-of-phase common-mode signal.

6.1 Input structure

Implementing the OTAs as pseudo-differential signal paths was an attractive alternative for the following reasons: A fully-differential implementation would require extra bias circuitry along with a relatively power-hungry CMFB for each OTA in order to achieve enough CMRR. Using the normally efficient triode CMFB would be unfeasible because the large transistors needed to achieve a good enough CMRR would have so much gate leakage that performance of the OTA would be degraded. A single-ended solution would be impractical for the same reasons as using a triode CMFB for fully-differential OTAs. The $1/g_m$ MOS in triode would require a nominal drain voltage of 100-200mV. For such small currents a $\frac{W}{L} < \frac{1}{250}$ would be required. The huge gate area required for the given bias conditions would cause huge gate leakage and make the amplifier nonoperational. The bias circuitry required would add up to almost the same amount of power consumption as the pseudo-differential solution. Also, the AGC would have to be realized separately and input offset-cancellation circuitry would be required to prevent the loop from saturating as the DC component would also be amplified.

6.2 Area

The required area consumption is directly proportional to the bandwidth and resolution of the system. The area of MOS transitors, $A_{MOS} \propto V_{ni(RMS}$, the capacitor area, $A_C \propto \frac{I_{bias}}{BW}$ and the resistor area, $A_R \propto \frac{1}{I_{bias}}$. The big arrays of relatively large MOS devices reduces mismatch and helps improve both voltage offsets and current mismatch. Recalling section 2.5 the offset from each device is expected to approach a minimum due to the g_m/I_D ratio, while the current mismatch is expected to approach a maximum. However, because lengths of $5 \times 1\mu m$ are used for the input transistors, it is fair to expect some mismatch of V_T due to pocket implants.

About 80% of the area is dedicated to the large capacitors required by the loop filter. Using MOS transistors biased at $V_{GS} > V_{th}$ would make it possible to reduce the area of the capacitor array by approximately 80%, but gate-tunneling would cause all current from the OTA output branches to leak through the gates, and the loop would not be operational. Leaving the MOS drain, source and bulk floating would solve this problem, but would also cause the area to increase by 10 times since the MOS-capacitors cannot be biased where the capacitance is large and linear. Using I/O devices are not an option either since their V_{th} is too high to be properly biased. MOS-capacitors in sub-micron technology can therefore not be used for ECG applications. The MOM-capacitors in the 65nm technology have a high capacitance density and the area consumption is acceptable. The capacitors use all 6 available metal layers and are divided into two unit sizes; one for the loop filter, and one for the DAC. Two unit sizes were chosen in order to improve matching and simplifying layout.

Minimum width resistors were used to reduce area consumption by resistors.

The temperature dependence of the poly-resistors are proportional to $\frac{1}{W_{res}}$. To decrease the dependence the widths should be larger than minimum, but the simulations from 5.1 showed that the variations in the resistances would not affect the performance. The resistors in the AGC and the feed-forward resistor, R_Z, use specific sizes to achieve the desired resistance. Other resistors are made using three different unit sizes with the intentions of simplifying layout and improve matching: $250k\Omega$, $300k\Omega$ and $1M\Omega$.

6.3 Linearity - Telescopic OTA

In appendix 8 it is shown that introducing an NMOS cascode in the OTA is necessary to achieve enough NTF gain for all AGC gain settings. The cascode introduced some more noise, a new bias branch for added power and also decreased the input voltage swing. Trading off swing is inevitable for the telescopic OTA, but it was shown that the linearity is primarily limited for high input voltages as the input transistors enters triode region when $V_{eff} > V_{ds}$. This condition is not an issue for the feedback OTA in the first integrator or the OTA in the second integrator, but may become true if both input transistors of the AGC are exposed to a large positive offsets, as shown in figure 34 and 35. The cascode keeps the drain voltage of M1 almost fixed, while a large input signal will pull the source voltage of M1 up, reducing V_{ds} and eventually force the input transistors into triode. However, it was seen that the OTA is very linear for a large negative swing. The worst case input range is almost 600mV, which is close to the specified requirements. The linearity can therefore be altered by using a lower nominal V_{cm} for the input AGC, i.e 500mV instead of 650mV. Also, it was seen that the loop response is sensitive to V_{DD} because changing $V_{ref(CM)}$ moves the drain voltage of the low-inversion current mirror. Though the loop filter response is acceptable for all corners, digital or analog tuning can be implemented. Placing switches between the segments in the reference resistor string so that the read-out V_{ref} can be calibrated will help keeping the linearity more constant against V_{DD}. Process tuning can be achieved by adding small current mirrors that are connected in parallel to the input current mirror in the bias circuitry. By turning them on or off, the current flowing through the input current mirror can be calibrated.

In summary, the telescopic OTA can be used to meet the system specifications, with the greatest drawback being a limited input signal swing. Alternatively, instead of using a telescopic OTA, a folded cascode could be implemented to improve the input swing at the cost of more power consumption and bias circuitry. Increased degeneration for increased $\Delta A_{v,STF}$ could then also be achieved. Steps to reduce the capacitor area could also be made. Because the G_m of the OTA is directly proportional to the bias current, it would be ideal to be able to reduce the bias current by a magnitude of 10-20, and therefore reduce the capacitor area by 10-20. A solution to this is to use series/parallel current mirrors in the OTA [13]. The output currents of the OTA is mirrored through a $M \times N$-matrix, effectively reducing the output current, and hence the G_m, by $M \times N$ times.

6.4 AGC

In section 2.1 two preamplifier approaches were presented. The first approach uses a high gain preamplifier and is therefore often not feasible for a low-voltage circuit. Because the ADC has a low enough input referred noise, an AGC gain of $\lesssim 20 - 25dB$ is suitable. It was shown that the signal gain of the AGC is proportional to the degenerating resistor, R_S. In order to achieve any higher gain, a larger R_S is required, but signal gain was sacrificed for headroom in the OTA. It was also shown that the offset of the signal increased with the gain, so digital calibration should be used. Digital calibration can also be used on signal gain which varies with ±1dB for process and supply variations. From appendix 9, it was shown that the input referred noise decreases with signal gain by almost cancelling all noise sources but the input transistors when referred to the input.

6.5 Gate leakage

Downscaling of technology has increased the power consumption of digital circuitry per unit area significantly and has approached a limit where further decreasing of oxide thickness will severely impede the performance. The oxide thickness used in the 65nm technolgy is 19.5Å for low threshold devices, and 20Å for high threshold devices. In the model documentation from the foundry it was found that for analog devices biased with $V_{ds} \approx 200mV$ and $V_{gs} \approx 350mV$ the gate-to-channel leakage for a $10\mu m^2$ device is in the order of 10-100pA. For the largest input transistors of the OTAs, the gate leakage is in the order of $\lesssim 2.5nA$. This leakage degrades the performance of the transistor as the gate can no longer be regarded as an ideal electrode. Therefore a trade-off between leakage and flicker noise had to be made. Noise was sacrificed to give a margin for operation as the noise can be further improved by adding a front-end LNA if necessary. Ideally the transistor areas of the PMOS load and the NMOS input should be almost twice their given sizes to make sure that the ADC always meets the input referred noise requirements by [10]. The trade-off made also favors area. As for I_{ds} leakage vs temperature for large devices, the leakage is almost at a constant 100pA for maximum length devices, and decreasing with the width up to about 50°C, from where the leakage starts to increase linearly up to about 1nA. The leakage of I_{ds} and I_{gds} is about twice as large in NMOS as in PMOS. Also it was found that transistors turned hard on and in the absence of a channel leak the most, which explains the large static current consumption by digital circuitry.

6.6 Power

Because minimizing power consumption is the main goal of the system, extensive mapping of current dissipation was done in section 5.10. It was found that each DSM requires approximately $2.27\mu W$ in typical corner. If the AFE is to be used in a multi-channel system, the bias circuit can be reused, resulting in a total power consumption of $1.33\mu W + N \times 2.27\mu W$ for an N-channel system. To avoid the exponential leakage that occurs for maximum V_{DD}, a 1.1V battery can be

used instead. This is likely to cause greater deviations in loop filter response. The biasing conditions remain almost the same except for a lower V_{ref}, which will result in a slight decrease in $V_{ds,n(p)-casc}$ causing a reduction of the OTA's output resistance. This decrease along with reduced bandwidth due to reduced g_{m1} will be the main source of NTF gain degradation. A signal conversion test for a 1V supply has not been documented and it can therefore not be confirmed if the $\Delta\Sigma$-ADC will still be able to meet all the specifications.

6.7 Noise

From appendix 9 it was shown that the the noise contributions from the PMOS loads and the NMOS input pairs are the greatest source of intrinsic noise. Noise from the preamplifier is reduced by the gain of the AGC and the second integrator when referred to the input, and therefore has minimal contribution to the overall noise. The noise from feedback circuitry applied to the first integrator is applied to both inputs of the OTA and with the same sign, and will therefore be fully or partially cancelled out depending on matching.

7 Conclusion

A complete analog front-end for portable ECG systems in 65nm technology was modeled and simulated using Cadence Virtuoso. All the required components for the AFE was incorporated into the continuous-time loop filter of a 10-bit $\Delta\Sigma$-ADC. By varying the effective G_m of the input OTA, preamplification of the input signal was achieved. The required filtering is achieved through the $\Delta\Sigma$-ADCs own loop filter and through digital post-filtering. The $\Delta\Sigma$-ADC meets the IEC60601-2-47 standard [10]. This simple, minimal and digitally-assisted converter show some promising results by dynamically adapting the programmable signal gain of the first integrator to keep the output signal range around 10mV where the SNDR is over 43.5dB. The decimated bit stream can then be divided by the signal gain to restore the input amplitude.

The filter was realized using a pseudo-differential second-order G_m-C filter with a phase margin of 60° and an OSR of 40. The $\Delta\Sigma$-ADC has a 100Hz bandwidth and a sampling frequency, $f_s = 8kHz$. The first order feedback loop was replaced with a zero resistor to save power and area. Extra phase delay and NTF degradation caused by digital circuitry was found to have an negligible impact on the performance of the ADC because of the system's low speed. Monte Carlo analysis showed that comparator offset is less than 10mV, implying that the headroom provided by the 50mV full scale reference is sufficient. Offsets in the two-level quantizer are constant and can therefore easily be digital corrected. The necessity for large gate areas to reduce flicker noise introduced a new major challenge in form of gate tunneling. The magnitude of the leakage is so large that it can no longer be ignored, and had direct impact on many of the design choices taken. Linearity, leakage, input referred noise, area and power all had to be weighed equally to achieve an acceptable performance.

The input referred noise power allows for over 60dB DR for all AGC gain settings, but only gain settings [011 $\rightarrow$ 110] meet the specification of less than $50\mu V_{ni(pp)}$. The maximum dynamic range was found to be $\simeq 80dB$, while the smallest signal amplitude greater than $V_{ni(pp)}$ was found to be -70dBFS. For all AGC settings, ENOB $\geq$ 9.4 bits, and a 6mV input signal can be converted with SNDR $>$ 43.5dB. The SFDR without taking $V_{ni(pp)}$ into account was found to be 68.6dB.

The AFE uses nominally $3.6\mu W$ excluding digital filtering and decimation. It was also found that gate leakage in digital circuitry and other devices driven by hard-on biasing is very sensitive to the supply voltage and consume a substantial amount of power for high supply voltages. The system was estimated to use about $0.2mm^2$ area, which is acceptable for the application.

Due to time constraints and software/licence complications, layout and extraction was not done. The design has been layout driven as much as it can, with as much reuse of devices and components as possible to aid the layout process time and matching. Wiring and coupling capacitance should have minimal effect on the performance, with the exception being the comparator. The comparator latch is very sensitive to parasitic capacitance and any routing and wiring should be guided away.

Alternatively, implementing a folded cascode can increase the input swing and allows for more source degeneration for higher $A_{v,STF}$ range, better linearity and smaller integrating capacitors by the cost of more power, without introducing much more noise. Also, series/parallel current mirrors in the OTAs can be implemented to reduce the effective G_m and hence the integrating capacitors. Additional digital and analog calibration and tuning can be implemented for even more robust performance against PVT variations. For increased performance several front-end components can be used with the proposed ADC: A DC cancelling filter can be added to further improve the linearity of the input OTA. A low-gain LNA front-end can be added for improved noise performance. A chopper can be implemented to further decrease low-frequency errors such as 50Hz interference and flicker noise. The large static leakage in digital circuitry can be greatly reduced by reducing the supply voltage from 1.2V to 1V or 1.1V, though this will make the operational conditions of the G_m-cells even tighter.

A summary of the ΔΣ-ADCs performance is presented in table 24.

Specification			
V_{DD}	[V]		1.2
Technology			65nm
f_s	[Hz]		8000
f_{BW}	[Hz]		100
OSR			40
$\Delta V_{ref}^{\pm}$	[mV]		|50|
Performance		**min**	**max**
AGC setting	[bits]	000	110
ENOB	[bits]	9.81	9.67
SNDR	[dB]	60.81	59.95
DR	[dB]	65.28	85.41
SFDR	[dB]	66.60	66.69
$V_{n(pp)}$	$[\mu V]$	18.65	111.9
$V_{n(RMS)}$	$[\mu V]$	2.694	16.16
$A_{v,STF}\|_{max}$	[dB]	-	16.92
Power	$[\mu W]$	-	3.6
I_{peak}	$[\mu A]$	-	242.048
A_{total}	$[mm^2]$	0.18	0.21

Table 24: Summary for the ΔΣ-ADC

There where no reports found for similar solutions, but table 25 show some other complete channel AFEs considered state-of-the-art that include preamplification and analog-to-digital conversion:

Reference	[14]	[15]	[16]	[17]
Architecture	SAR	SAR	SAR	SAR
Channels	4	3	3	18
Power/channel	$4.8\mu W$	$31.1\mu W$	$40\mu W$	$77.1\mu W$
Number of bits	8	12	12	12
$V_{ni(rms)}$	$2\mu V$	-	$80nV$	-
V_{DD}	1.2V	1.2V	1.2V	1V

Table 25: Sub-14-bit AFEs for EEG/ECG detection. Note that all solutions use SAR architecture.

The gate leakage in 65nm technology introduces great challenges in terms of area, power consumption and performance. However, the ADC shows robustness against PVT variations and proves its strength in simplicity and process scalability. In conclusion, the ADC meets the specification and the performance is comparable to current state-of-the-art as shown in the table above.

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8 The effect of AGC gain variation on NTF gain

Initially a classic differential pair was used to realize the OTA-C filter. However, it was found that changing the gain settings of the AGC (input OTA) would drastically change the loop gain of the filter as the output resistance of the first integrator would change. This change of output resistance affects both noise suppression and phase margin. Reduction in noise suppression is caused by the reduced gain of the feedback OTA whose g_m does not scale with AGC gain. Since the output resistance of the first integrator node becomes dominated by the resistance looking into the drain of the input transistor in the AGC, the gain of the feedback OTA is reduced by as much as approximately 10dB for maximum AGC gain setting.

8.0.1 Analysis of the effect of varying AGC gain in the loop filter of the classical source-degenerated OTA

Because we are operating in subthreshold, it is easier to perform small-signal analysis using g_m/i_d, $g_m r_o$ and v_{ds}/i_d relations than the square model. We make the following assumptions:

- For increased matching we want to operate PMOS load in moderate inversion ($g_m/i_d \simeq 20$).
  - $g_m/i_d = 20$
  - $i_d = 200nA$
  - $g_m = 4\mu S$
  - $g_m r_o \simeq 40 \rightarrow g_{ds} = 100nS$
- Looking into the drain of the input transistor, we want to maximize the g_m of the device, in order to maximize the available AGC gain. This translates to using wide transistors, biasing the transistor in weak inversion where g_m/i_d is at its maximum.
  - $g_m/i_d = 30$
  - $g_m = 6\mu S$
  - $g_m r_o \simeq 100 \rightarrow g_{ds} = 60nS$
- The NMOS input transistor is source degenerated with a $1M\Omega$ resistor.
- The AGC is realized by shorting AC ground between the two branches in the OTA spread across the $1M\Omega$ resistor string.
- Maximum source degeneration is therefore $1M\Omega$, and minimum source degeneration is 0Ω.
- Maximum AGC gain occurs when $G_{m,AGC}$ is at its maximum, i.e. source of input transistors shorted together.
- Minimum AGC gain occurs when $G_{m,AGC}$ is at its minimum, i.e. when AC ground is moved below the $1M\Omega$ source degenerating resistors.

8.0.2 Small-signal analysis of classical source-degenerated OTA

With these assumptions we find that the PMOS load resistance becomes approximately:

$$R_L \simeq \frac{1+\frac{4000}{100}}{100}10^9 = (1+40)10^7 = 410M\Omega \tag{70}$$

As for the resistance looking into the drain of the input transistor, we have:

$$R_D \simeq \frac{1+6}{60}10^9 = \frac{7}{6}10^8 = 117M\Omega \tag{71}$$

The output resistance seen looking into the OTA therefore becomes:

$$R_o = R_L||R_D = 91M\Omega \tag{72}$$

The G_m of the OTA approximately:

$$G_m \approx \frac{g_{m1}}{1+g_{m1}R_s} = \frac{6}{7}\mu S = 850nS \tag{73}$$

Since the integrator at the second integrator node consists of a single OTA, the same small-signal analysis can be applied to this node. The gain of OTA, and therefore also the second integrator, becomes:

$$A_{v_2} = 77 = 37.7dB \tag{74}$$

8.0.3 Small signal analysis of first integrator node using classical source-degenerated OTAs with variable degeneration in AGC

The following abbreviations will be used:

- $R_{o,1}$ = output resistance seen at the first integrator node.
- $R_{o,2}$ = output resistance seen at the second integrator node.
- $R_{o,fb}$ = output resistance seen looking into the feedback OTA.
- $R_{o,in}$ = output resistance seen looking into the input OTA.
- The same notations are used for G_m and A_v.

When AGC setting is set to minimum gain (i.e. 0dB signal loop gain), the small-signal analysis of the OTAs used in the first integrator becomes the same as that of the second and we have that:

$$G_{m,fb} = G_{m,in} = G_{m,2} \approx 850nS \tag{75}$$

$$R_{o,1} = R_{o,fb}||R_{o,in} = \frac{R_{o,2}}{2} \simeq 45M\Omega \tag{76}$$

The DC gain at the first integrator node then becomes:

$$A_{v_1} = 31.7dB = \frac{A_{v_2}}{2} = A_{v_2} - 6dB \tag{77}$$

The total loop gain therefore becomes:

$$A_{v_tot} = A_{v,1} + A_{v,2} = 31.7dB + 37.7dB = 69.4dB \tag{78}$$

When we maximize the signal loop gain by shorting the sources of the input transistors, we get that:

$$R_{D,AGC=max} = \frac{1}{g_{ds1}} = \frac{1}{60nS} = 17M\Omega \tag{79}$$

$$R_{o,OTA|_{AGC_{max}}} = R_L||R_{D,AGC=max} = 410M\Omega||17M\Omega = 16M\Omega \tag{80}$$

Looking at the AGC signal gain, assuming that $g_{m1} = 6\mu$S, the required degeneration resistance can be estimated by equation (84):

$$G_{m_{min}} \approx \frac{g_{m1}}{1 + g_{m1}R_S} \tag{81}$$

$$G_{m_{max}} \approx g_{m1} \tag{82}$$

$$A_{v_{STF}} = \frac{G_{m_{max}}}{G_{m_{min}}} \approx \frac{g_{m1}}{\frac{g_{m1}}{1 + g_{m1}R_S}} = 1 + g_{m1}R_S \tag{83}$$

$$\Rightarrow R_S \simeq \frac{A_{v_{STF}} - 1}{g_{m1}} \tag{84}$$

Using this equation we find that $1.5M\Omega$ source degeneration is required to achieve 20dB gain, and $1.7M\Omega$ source degeneration is required to achieve 21dB gain. Using $R_S = 1M\Omega$, we expect to achieve a maximum signal gain of:

$$A_{v_{STF}} \simeq 1 + g_{m1}R_S = 1 + 6 = 7 = 16.9dB \tag{85}$$

We see that the if we want to achieve a higher STF, we must increase the size of the degenerating resistor to make the relative difference between AGC_{max} and AGC_{min} greater. Obviously, since $G_{m_{AGC}}$ increase with higher AGC settings, we expect the unity gain frequency of the STF to increase with approximately the same amount as $A_{v_{STF}}$.

Now, looking at the NTF (feedback) gain at the first integrator, we have that:

$$R_{o,1|_{AGC_{max}}} = R_{o,fb}||R_{o,in} = 91M\Omega||16M\Omega = 13.6M\Omega \tag{86}$$

$$A_{v,1|_{AGC_{max}}} \simeq G_{m,fb}R_{o,1} = 13.6 \times 0.85 = 11.56 = 21.3dB \tag{87}$$

$$A_{v,tot|_{AGC_{max}}} = A_{v_{1|_{AGC_{max}}}} + A_{v_2} = 21.3dB + 37.7dB = 59dB \tag{88}$$

We see that the noise suppression gain has been reduced by approximately 10dB when we increase the signal gain of the AGC. It was found that across PVT variations, the loss of gain would reduce the total noise suppression so much that the ADC would be unable to achieve an acceptable SNR when operating with high AGC gains. Therefore it becomes necessary to reduce the effects of source degeneration variations on the output resistance. Adding a NMOS cascode in the OTA to increase R_D should help reducing the variations of R_{o_1}.

8.0.4 Measured results of the effect of varying AGC gain in the loop filter of the classical source-degenerated OTA

STF and NTF was measured using the classical OTA.

- $A_{v,STF|_{AGC=min}} = 0dB$
- $A_{v,STF|_{AGC=max}} = 17.82dB$
- $|A_{v,NTF|_{AGC=min}}| = 67.86dB$
- $|A_{v,NTF|_{AGC=max}}| = 58.45dB$
- $\Delta A_{v,NTF} = 9.41dB$

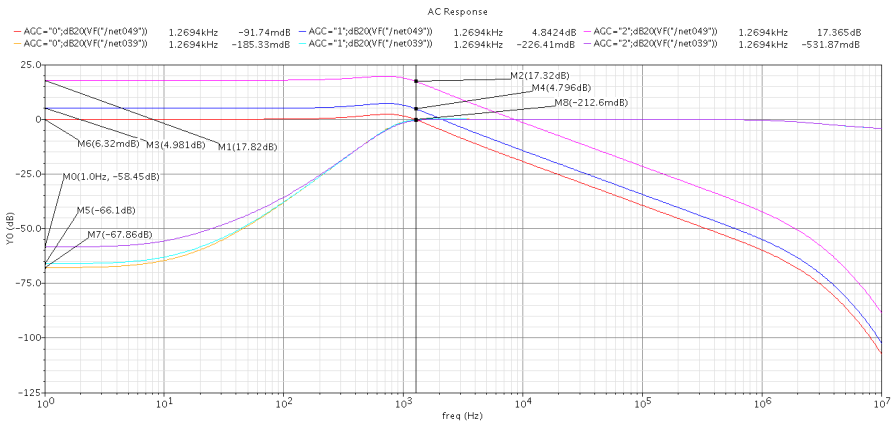

Figure 87: STF and NTF of the three AGC cases.

In figure 87, we see that the STF varies as expected, where the maximum signal gain is 17.82dB, and f_{ug} have increased with approximately the same amount as the gain, from $\sim 1100Hz$ to $\sim 8500Hz$ ($\frac{8500}{1100} \simeq 17.76dB$).

As it can be seen in figure 88, the 9.41dB difference in loop gain is caused by the difference in output resistance at the first integrator node alone, where A_{v_1} varies from 29.99dB when AGC=min to 20.59dB when AGC=max.

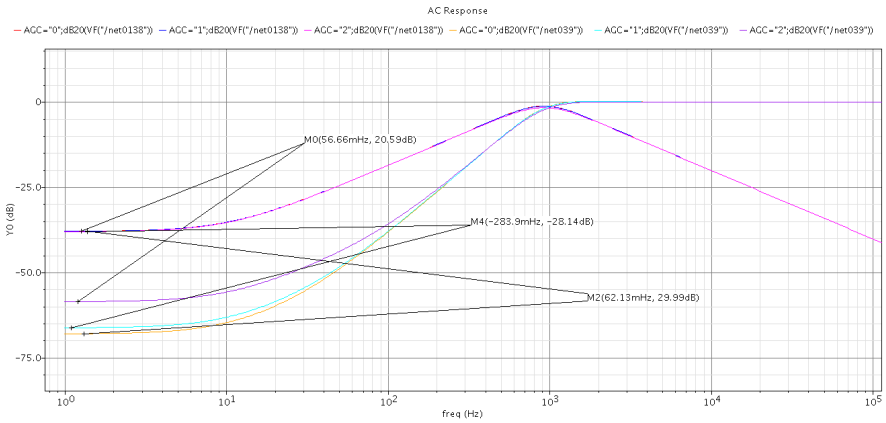

Figure 88: NTF of the three AGC cases.

Figure 89 depicts the open loop gain of for three AGC settings using the classic OTA.

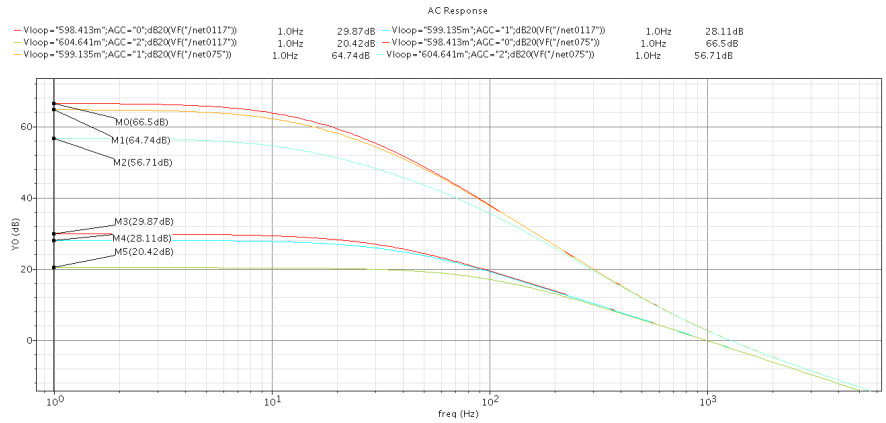

Figure 89: Loop gain of the three AGC cases.

AC and DC response was measured over corners for the classical OTA using minimum AGC gain setting. The worst case corner, FF, is depicted in figure 92.

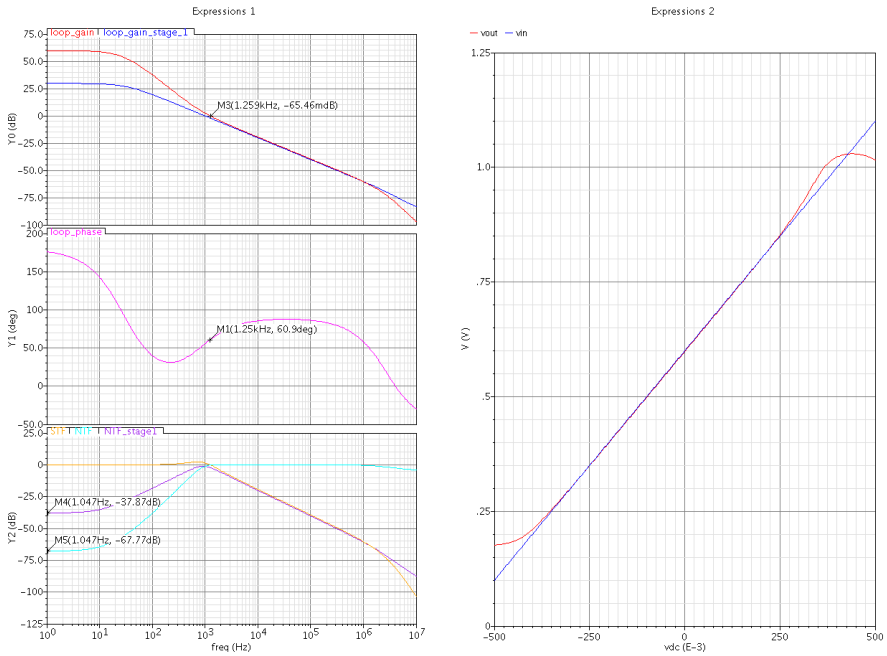

Figure 90: AC and DC loop response using classic OTA. Corner: TT

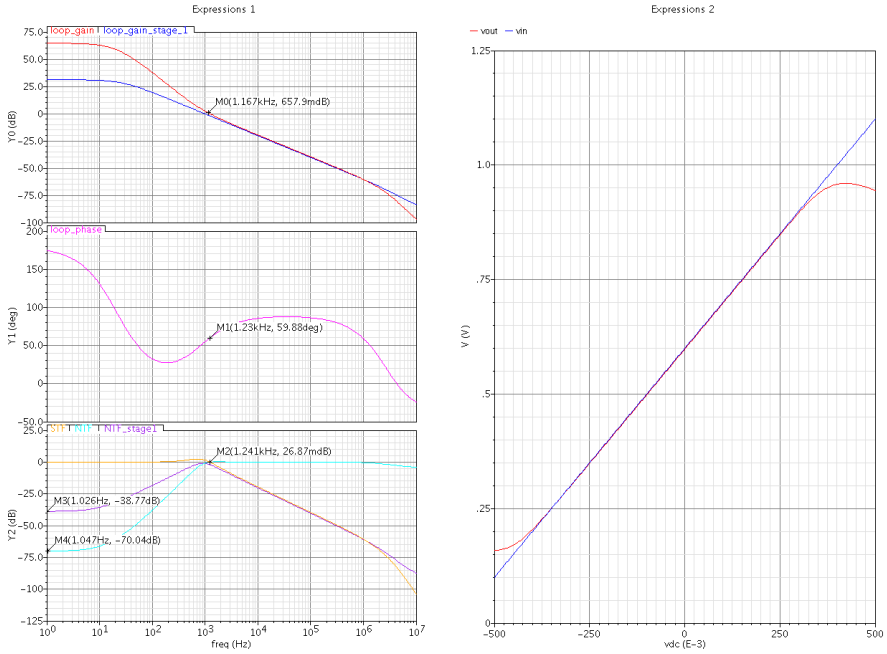

Figure 91: AC and DC loop response using classic OTA. Corner: SS

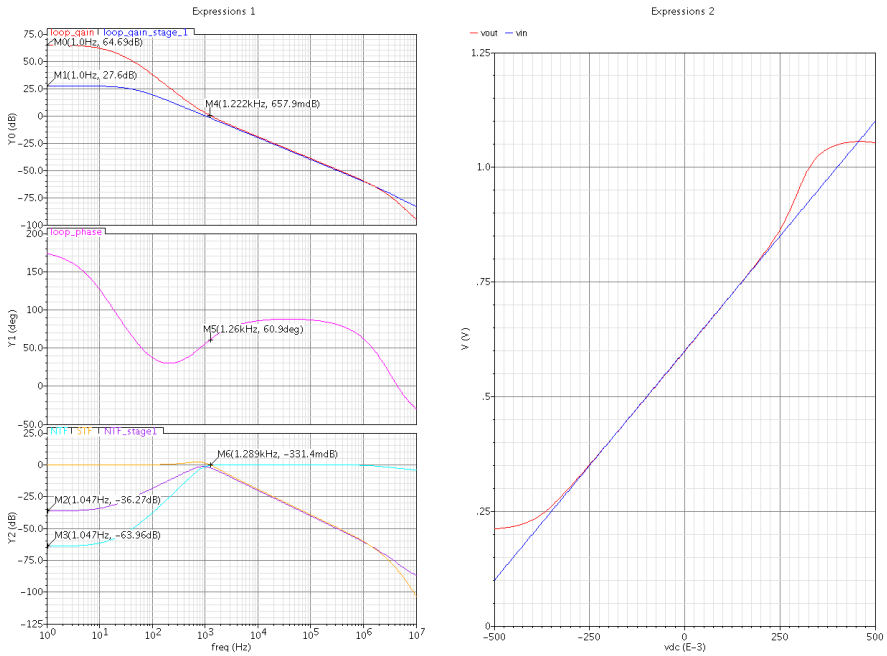

Figure 92: AC and DC loop response using classic OTA. Corner: FF

As seen the DC gain is the lowest with approximately 64dB in corner FF. Because the tail current is higher in this corner, g_{m1}, the relative size of R_S to g_{m1}, $\frac{R_S}{g_{m1}}$ will decrease. This causes $\Delta A_{v,STF}$ to increase, but also $\Delta R_{o,1}$ to increase, meaning that ΔA_{v_1} will peak, and resulting in a minimum $A_{v,tot}$ across corners. This also will result in a minimum source degeneration, which is the cause of the reduced linearity. Also, we notice that the phase margin has a maximum in this corner. This is caused by the first pole moving out because of the reduced loop gain.

8.0.5 Small signal analysis of telescopic OTA

Considering that we need to make room for one more NMOS transistor, the V_{CM} of the loop should be increased, which translates to a lower V_{DS} for the PMOS transistors. Since $r_{ds} \propto v_{ds}$, it is fair to assume that the load resistance will be reduced when increasing V_{CM}. We therefore make the following assumptions (numbers based on v_{ds}/i_d-ratio):

- $g_{ds,p} = 125nS$
- $g_{ds,n|_{cascode}} = 350nS$
- $g_{ds,1} = 150nS$
- $g_{m,p} = 3.7\mu S$

- $g_{m,n} = 6.2\mu S$

The load resistance becomes:

$$R_L = \frac{1}{g_{ds}}(1 + \frac{g_m}{g_{ds}}) \approx 230M\Omega \tag{89}$$

The resistance looking into the NMOS cascode, degenerated with an input transistor and a $1M\Omega$ resistor becomes:

$$R_D \approx 2.4G\Omega \tag{90}$$

The output resistance then becomes:

$$R_o = R_{o_2} = R_{o,AGC_{min}} = R_{o,fb} \approx 210M\Omega \tag{91}$$

And the gain of the OTA, and hence the noise suppression of the second integrator becomes:

$$A_{v_{OTA}} = A_{v_2} \approx 210 \times 0.85 = 178.5 = 45dB \tag{92}$$

When we short the AC ground, $R_{D,AGC_{max}} \approx 120M\Omega$. The output resistance of the input OTA therefore becomes:

$$R_{o,in|_{AGC_{max}}} \approx 120M\Omega||230M\Omega = 79M\Omega \tag{93}$$

We then get that in the case of maximum AGC gain, the DC noise suppression of the first integrator node becomes 33.8dB, while the DC noise suppression of the second integrator is 45dB.

The total DC noise suppression then becomes for minimum AGC gain:

$$A_{v,NTF|_{AGC_{min}}} = A_{v,1|_{AGC_{min}}} + A_{v_2} = (45dB - 6dB) + 45dB = 84dB \tag{94}$$

And in the case of maximum AGC gain, the expression changes to:

$$A_{v,NTF|_{AGC_{max}}} = A_{v,1|_{AGC_{max}}} + A_{v_2} = 33.8 + 45dB = 78.8 \tag{95}$$

We therefore get that the variation in noise suppression gain should be expected to be in the order of:

$$\Delta A_{v,NTF} = A_{v,NTF_{AGC_{min}}} - A_{v,NTF_{AGC_{max}}} = 84 - 78.8 = 5.2dB \tag{96}$$

We therefore see that by introducing a cascode transistor we expect to get both more noise suppression and less noise suppression variation, which should be sufficient to meet the required SNR. A disadvantage that should be taken into consideration of using telescopic OTAs is that the signal swing will be reduced and more power is needed to generate bias voltages for the cascodes.

9 Noise in DSM

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The intrinsic noise of a device, v_n, includes all noise contributions. For MOS that means both thermal/shot-noise and flicker noise.

9.1 Noise contribution from cascodes

By assuming that the load resistance is high, the output referred noise of the cascodes becomes approximately:

$$v_{no,casc} \approx g_{m,casc} r_{ds,casc} \times v_{ni,casc} \tag{97}$$

Where $v_{n,ieq_{casc}}$ is the sum of the flicker and thermal noise referred to the gate of the cascode. The noise contribution from the cascodes in the OTA can be referred to the input of the amplifier as follows:

$$\overline{v_{ni}^2} \approx \overline{v_{ni,1}^2} + \frac{\overline{v_{ni,casc}^2}}{\left(g_{m1} r_{ds_1}\right)^2} \mathrm{d}f \tag{98}$$

This expression assumes that the load resistance is infinite and that the gain of the amplifier is $g_{m1} r_{ds1} g_{m2} r_{ds2}$. Though this is an approximation, this indicates that the noise contribution from the cascodes is reduced by a factor in the order of the intrinsic gain of the input transistors. As this gain is approximately 40dB, the noise power of the cascodes becomes reduced by a factor of approximately 80dB, which can be considered negligible with regards to both flicker- and thermal noise as long as $\frac{W_{in} L_{in}}{W_{casc} L_{casc}} \gg 1$.

9.2 Noise contribution from active load

The noise contribution from the active load can be found with similar approach as that of the cascodes:

$$v_{no,load} \approx g_{m,load} r_{out} \times v_{ni,load} \tag{99}$$

Referring this output noise back to the input of the amplifier, we get that:

$$\overline{v_{ni}^2} = \overline{v_{ni,1}^2} + \overline{v_{ni,load}^2} \times \left(\frac{g_{m3}}{g_{m1}}\right)^2 \mathrm{d}f \tag{100}$$

It is important to notice here that g_{m1} has been source degenerated by a factor of $\frac{1}{1 + g_{m1} R_S}$. Therefore, the actual input referred noise is given by:

$$\overline{v_{ni}^2} = \overline{v_{ni,1}^2} + \overline{v_{ni,load}^2} \times \left(\frac{g_{m3}}{g_{m1}} \left(1 + g_{m1} R_S\right) \right)^2 \mathrm{d}f \tag{101}$$

To see the effect of this, let us assume the following:

- The flicker coefficient of the NMOS is twice that of the PMOS.
- Thermal- and shot-noise can be neglected.
- PMOS and NMOS have been scaled so that the intrinsic g_m of both are $5\mu S$.
- PMOS and NMOS have the same gate area.

$$\begin{aligned} \overline{v_{ni}^2} &= \overline{v_{ni,1}^2} + \left(\frac{\overline{v_{ni,1}^2}}{2} \right) \times \left(\frac{5\mu}{5\mu} (1+5) \right)^2 \mathrm{d}f \\ &= \overline{v_{ni}^2} \left(1 + \frac{6^2}{2} \right) \end{aligned} \tag{102}$$

The example over shows that the noise contribution from the PMOS load completely dominates the total input referred noise. This is the reason for the extremely careful sizing of the load transistors. With regards to the AGC we get that as we reduce the degeneration towards zero, equation 100 becomes valid, and the noise from the input NMOS dominates again.

9.3 Noise contribution from source degenerating resistor, R_S

The noise contribution from a source degenerating resistor, R_S, is approximately:

$$\overline{v_{ni,R_S}} \approx 4 k_B T R_S \mathrm{d}f \tag{103}$$

Notice that for maximum AGC gain, the AC ground is moved above R_S, and noise contribution from the resistor is canceled out similarly to the current mirror noise.

9.4 Noise contribution from differential pair tail current mirror

The noise contribution from the current mirror in a differential pair can be considered zero as the noise current is split in half between the two branches and cancels each other at the output. This is only true for perfect matching.

9.5 Input referred noise of telescopic OTA

The total noise referred to the input of a telescopic OTA can be found to be approximately:

$$\overline{v_{ni}^2} \approx 2 \times \left(\overline{v_{ni,in}^2} + \overline{v_{ni,load}^2} \times \left(\frac{g_{m3}}{g_{m1}} \right)^2 + 4k_b T R_S \right) \mathrm{d}f \tag{104}$$

Equation (104) assumes that the noise contribution from the cascodes and the current mirror can be neglected.

9.6 Input referred noise of loop filter

The noise from the DAC is applied to both inputs of the feedback OTA along with the negative inputs of the OTA in the second integrator and the negative input of the preamplifier. Hence, feedback noise is a function of the common-mode rejection of the OTAs.

The input referred noise of the filter can be expressed as:

$$\begin{aligned} v_{ni} \approx & v_{ni_{\mathrm{AGC}}} + v_{ni_{\mathrm{OTA_{fb}}}} \frac{A_{v\mathrm{OTA_{fb}}}}{A_{v_{\mathrm{AGC}}}} + v_{ni_{\mathrm{OTA_2}}} \frac{1}{A_{v_{\mathrm{AGC}}}} + v_{ni_{\mathrm{preamp}}} \frac{1}{A_{v_{\mathrm{AGC}}} A_{v_{\mathrm{OTA_2}}}} \\ & + \frac{v_{no_{\mathrm{DAC}}}}{A_{v_{\mathrm{AGC}}}} \left(1 + 2A_{CM} A_{v_{\mathrm{OTA_{fb}}}} + \frac{1}{A_{v_{\mathrm{OTA_2}}}} \right) \end{aligned} \tag{105}$$

Where:

$$v_{no_{\mathrm{DAC}}} \approx \quad v_{ni_{\mathrm{Buffer}}} \quad \approx v_{ni_{\mathrm{OTA}}} \tag{106}$$

$$v_{ni_{\mathrm{AGC}}} \approx \quad v_{ni_{\mathrm{OTA_{fb}}}} \quad \approx v_{ni_{\mathrm{OTA_2}}} \tag{107}$$

The flicker noise of the voltage buffer is approximately twice that of the telescopic OTA, but thermal noise is also reduced by more than 2, for simplicity they have been assumed to be the same.

Equation (105) can be rewritten to:

$$v_{ni} \approx v_{ni_{OTA}} \left(1 + \frac{A_{v_{\mathrm{OTA_{fb}}}} + b}{A_{v_{\mathrm{AGC}}}} \right) \tag{108}$$

Where:

$$b = 1 + \frac{v_{ni_{\mathrm{preamp}}}}{A_{v_{\mathrm{OTA_2}}}} + v_{no_{\mathrm{DAC}}} \left(1 + 2A_{CM} A_{v_{\mathrm{OTA_{fb}}}} + \frac{1}{A_{v_{\mathrm{OTA_2}}}} \right) \tag{109}$$

Because the gain of a common source amplifier is given by:

$$A_v = \frac{g_m}{1 + g_m R_S} \frac{1}{g_{ds}} (1 + g_m R_S) = \frac{g_m}{g_{ds}} \tag{110}$$

The gain of the stand-alone AGC should therefore be approximately constant when varying the gain setting. However, when connected to the first integrator, the relative change in the output resistance to $G_{m_{\mathrm{AGC}}}$ decreases. In other words, the voltage gain of the AGC increases. The term in (108) can be approximated and rewritten to:

$$v_{ni} \approx v_{ni_{OTA}} \frac{\underbrace{\left(1 + \frac{G_{m_{\mathrm{OTA_{fb}}}}}{G_{m_{\mathrm{AGC}}}} + \frac{b}{A_{v_{\mathrm{AGC}}}}\right)}}{1 + \frac{1}{A_{v_{\mathrm{STF}}}} + \frac{b}{A_{v_{\mathrm{AGC}}}}} \tag{111}$$

From equation 111 we see that:

$$v_{ni} \propto \frac{1}{A_{v_{\mathrm{STF}}}(1 + \alpha)} \tag{112}$$

Where α describes the further increase in input referred noise due to increased AGC voltage gain. Also recalling equation (100) it is important to notice that the noise of the AGC itself decrease substantially as the AGC gain is increased. From measurements it was found that the total noise decreases by 6.9 times from $AGC = [000 \rightarrow 110]$, which is analogous with our expectations.

10 Design considerations

10.0.1 OTA scaling considerations

The higher the output resistance seen into the drain of the NMOS cascode is, the less variation will be seen when varying the degeneration of M1. Therefore, it is desirable to use at least one high threshold device as its intrinsic $g_m r_o$ is very large. At the same time the g_m is somewhat lower, resulting in maximum linearity when using a $1M\Omega$ source degenerating resistor. Furthermore the increased threshold voltage will allow for higher input voltages before entering triode region, as will be explained shortly. The OTA was therefore realized using high threshold devices for the inputs, and regular threshold devises were used for the cascode since they have a lower V_{dsat} and still have a decent output resistance.

There are especially three trade-offs to consider when scaling the NMOS drivers and cascodes. The two transistors must be scaled so that the cascode can operate in saturation and have a high r_{ds}. More room for the cascode can be given by increasing the W/L-ratio of the input transistor which will reduce the V_{DS}. However, increasing this ratio will result in decreased linearity of the OTA as the condition $V_{eff} \gtrsim V_{DS}$ becomes true for large input voltages, and causes the input transistor to enter triode region. Though this transition is abrupt, and does not degrade linearity too much before occurring, it is important to set the reference voltage and/or W/L-ratio so that the input transistors can stay in saturation across an acceptable swing. It should be noted that it is indeed the input transistor falling into triode, and not the PMOS load falling into triode region, that is the source of degraded linearity for high input voltages. Third, enough room to operate the tail current mirror must be given in order to make the loop filter more robust against PVT variations. Also, because of the restriction to current consumption and to device geometries given in the process, the current mirrors are forced to operate in weak inversion. In weak inversion the current mismatch is at its maximum. Variations in f_{ug} and phase margin of the loop is fairly tolerable, but the change of tail current is directly proportional to the gain of the AGC, whose variation increases more with higher gain settings. There are two ways to give more room for the current mirror to operate. One is, as for the NMOS cascode, to increase the W/L-ratio of the input transistors, which will reduce V_{gs1}. The other is to move V_{CM} up, which will move the source voltage with the same amount. Other ways to deal with $A_{v_{AGC}}$ variations are digital calibration or have passive, analog tuning of the OTA current mirrors.

Another consideration is the area consumption of the transistors and the input referred noise. The ECG standard specifies that the peak input noise voltage, $v_{ni(P-P)}$, should not exceed $50\mu V$. In order to reduce flicker noise, large enough devices must be used, especially for the input and load transistors. The total area consumption of the transistors are small compared to the area consumption of the integrating capacitors in the loop filter, allowing freedom to choose as large devices as the gate-to-channel leakage allows while maintaining proper operation. In summary, three NMOS devices are to be stacked and operated

properly over approximately $\frac{V_{DD}}{2} \simeq 650mV$ and care must be taken to optimize their performance and robustness. If the cascode can be operated properly, sufficient noise suppression can be guaranteed across PVT. The PMOS load and cascode have much more headroom at disposal, and can therefore be scaled with focus on reducing noise contribution while providing high load resistance. Therefore, the remaining issues to address are:

- Linearity.
- Maximum current consumption.
- Signal loop gain variations.
- Input referred noise.

Because of the low bandwidth, flicker noise is expected to dominate. The input transistor's noise directly influences the overall noise. Therefore, using a PMOS transistor in the input with lower flicker coefficient can be beneficial. However, in certain circumstances, using an NMOS transistor in input can reduce the flicker noise, in cases where the noise of the load transistor is larger than that of the input transistor. The reason, in such cases, is that a lower $\left(\frac{g_{m,load}}{g_{m,in}}\right)^2$ is made. Also, the PMOS transistor which has a lower flicker coefficient is put on load, so the noise of the load transistor decreases and causes the total noise to decrease. It can therefore be found that the total flicker noise using a PMOS input is proportional to the bias current used, while the total flicker noise using an NMOS input is much more insensitive to bias current because the noise contribution from the load is decreased. The minimum area required before an NMOS input pair becomes more efficient than a PMOS with regards to flicker noise decreases with bias current. In the following subsections, the noise of the OTAs and the filter is analyzed.

10.1 Derivations for bias circuitry of telescopic OTA's cascodes

The bias networks for V_{n-casc} and V_{n-casc} have been based on a low voltage cascode bias technique for all current levels. The technique is used to reduce headroom consumption of cascodes, which is very important for the OTAs used in this circuit. The technique takes use of the EKV MOS transistor model and following abbreviations are used:

- $\kappa = \frac{1}{n} = \frac{C_{ox}}{C_{ox} + C_{depl}}$
- $U_T = \frac{kT}{q}$
- $I_S = \frac{2\mu C_{ox} U_T^2}{\kappa} \approx 2 \times$ threshold current of square transistor

- I_F - Forward current
- I_R - Reverse current
- $I_F(R) \approx \begin{cases} \frac{W}{L} I_S e^{\kappa(V_G - V_{T0}) - V_{S(D)})/U_T}, & V_G < V_{T0} + \frac{V_{S(D)}}{\kappa} \\ \frac{W}{L} \frac{\mu C_{ox}}{2\kappa} (\kappa(V_G - V_{T0}) - V_{S(D)})^2, & V_G > V_{T0} + \frac{V_{S(D)}}{\kappa} \end{cases}$

I_F depends only on V_G and V_S, while I_R only on V_G and V_S. Hence, if $I_F \gg I_R$, then $I \approx I_F$, and nearly independent of V_D, corresponding to operation in the saturation region. This also explains why it is difficult to have accurate current mirrors in the OTA; because of the limited headroom for the current mirror to operate in, the mirror is forced to operate in weaker inversion, increasing the dependence of V_D, and increasing the variations with supply voltage as $\Delta V_{S,m1} \approx \Delta V_{ref} \approx \pm 10\% V_{ref,\text{nominal corner}}$, assuming that the supply varies with $\pm 10\%$.

As for the cascode biasing, we define the following condition to ensure saturation:

$$\frac{I_F}{I_R} \gtrsim A \gg 1 \tag{113}$$

Using this condition, an expression for V_{DSsat} can be found:

$$A = \frac{I_F}{I_R} = \frac{\log^2(1 + e^{\kappa(V_G - V_{T0}) - V_S)/U_T}}{\log^2(1 + e^{\kappa(V_G - V_{T0}) - V_S - V_{DSsat})/U_T}} \tag{114}$$

$$\Rightarrow V_{DSsat} \approx \begin{cases} U_T \log A, & V_G < V_{T0} + V_S/\kappa \\ (1 - \frac{1}{\sqrt{A}})(\kappa(V_G - V_{T0}) - V_S), & V_G > V_{T0} + V_S/\kappa \end{cases} \tag{115}$$

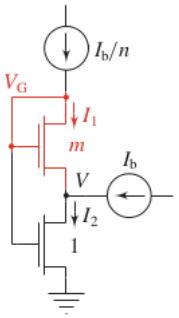


Figure 93

Assuming that *M1* is in saturation ($I_1 \approx I_{F1}$) and that *M2* is either ohmic or in saturation ($I_2 = I_{F2} - I_{R2}$). With m *M2* transistors in parallel, we have that

$I_1 \approx I_{F1}$ and $I_2 = I_{F2} - I_{R2}$. Since node V is source of *M1* and drain of *M2*, we get:

$$I_{F1} = mI_{R2} \Rightarrow I_{R2} = \frac{I_{F1}}{m} \approx \frac{I_1}{m}$$

Solving for I_{F2}/I_{R2} we find:

$$\frac{I_{F2}}{I_{R2}} = 1 + \frac{I_2}{I_{R2}} = 1 + m\frac{I_2}{I_1} = 1 + m(1 + \frac{I_b}{I_1})$$

Then, by setting $I_1 = \frac{I_b}{n}$, we get that:

$$\frac{I_{F2}}{I_{R2}} = 1 + m(1 + n\frac{I_b}{I_b}) = 1 + m(1 + n) \tag{116}$$

Which is independent of I_b. As seen in the figure below, connecting the gate to the drain of M1, M2 will pass the current $I_b(1 + 1/n)$. Setting m and n large enough, we can satisfy (113) and get $V \approx V_{DSsat}$. We can then insert a diode-connected transistor to get V_{n-casc}.

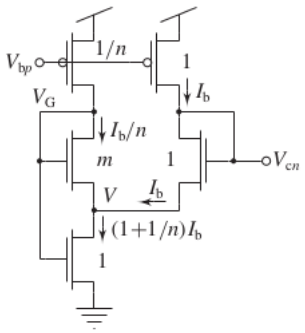


Figure 94: Low-voltage cascode bias.

The ratios m and n are implemented as parallel/series connections of m/n unit transistors. For m even, the drain/source regions of the cascode can be optimally shared. If $n = m+1$ we get that the same amount PMOS strips as NMOS strips for a layout-driven design.

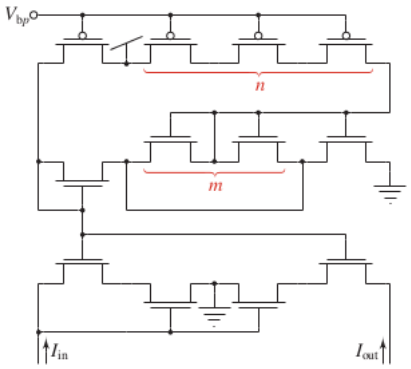
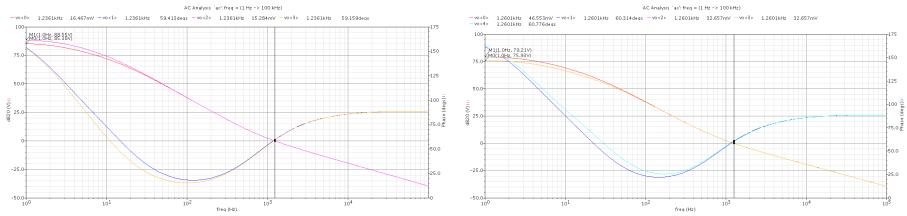


Figure 95: Layout driven design.

11 Additional simulation results

11.1 Loop filter

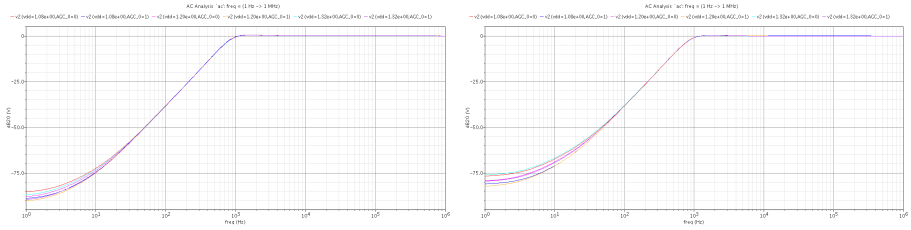
In figures 96a and 96b shows the open loop frequency response for minimum and maximum corner when PGA=[000,110]. The PM and f_{ug} decrease in figure 96a while it increase in figure 96b compared to typical corner. This is because g_{m1} decrease and increase respectively.



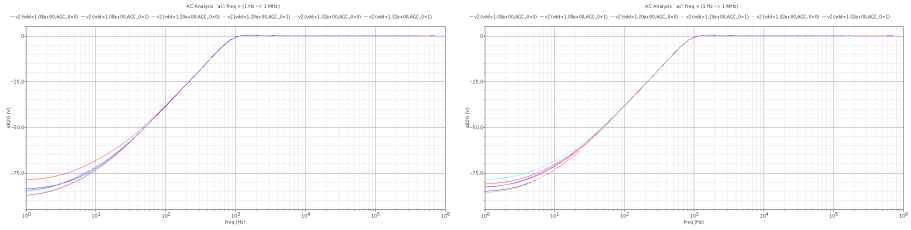
(a) Slow corner, $V_{DD} = 1.08V$ (b) Fast corner, $V_{DD} = 1.32V$

Figure 96: NTF of filter for $PGA = [000, 110]$.

The NTF for corners SS, FF, FNSP and SNFP are shown in figure 97.



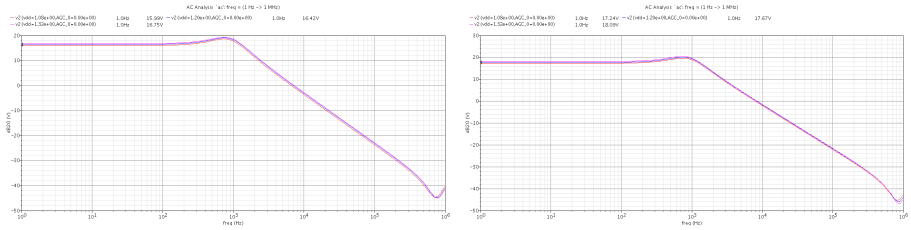
(a) Slow corner (b) Fast corner



(c) SNFP corner (d) FNSP corner

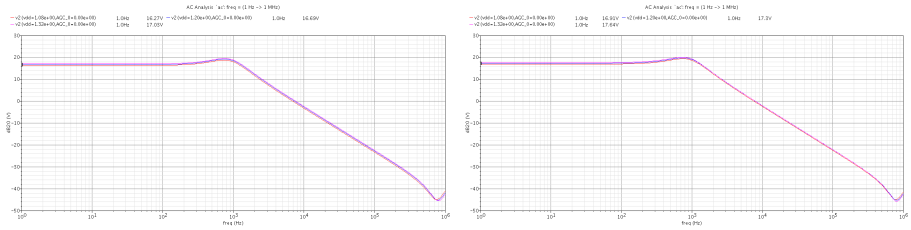
Figure 97: NTF for $PGA = [000 \rightarrow 110]$.

The STF for corners SS, FF, FNSP and SNFP are shown in figure 98.



(a) Slow corner

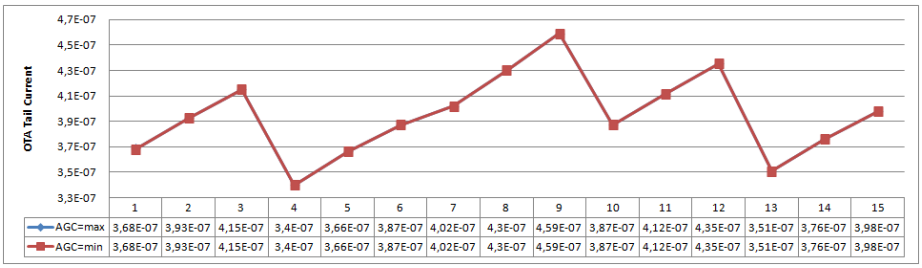
(b) Fast corner



(c) SNFP corner

(d) FNSP corner

Figure 98: STF for $PGA = [110]$.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AGC=max	3,68E-07	3,93E-07	4,15E-07	3,4E-07	3,66E-07	3,87E-07	4,02E-07	4,3E-07	4,59E-07	3,87E-07	4,12E-07	4,35E-07	3,51E-07	3,76E-07	3,98E-07
AGC=min	3,68E-07	3,93E-07	4,15E-07	3,4E-07	3,66E-07	3,87E-07	4,02E-07	4,3E-07	4,59E-07	3,87E-07	4,12E-07	4,35E-07	3,51E-07	3,76E-07	3,98E-07

Figure 99: OTA tail current vs. process and supply ($\#_1$-notation).

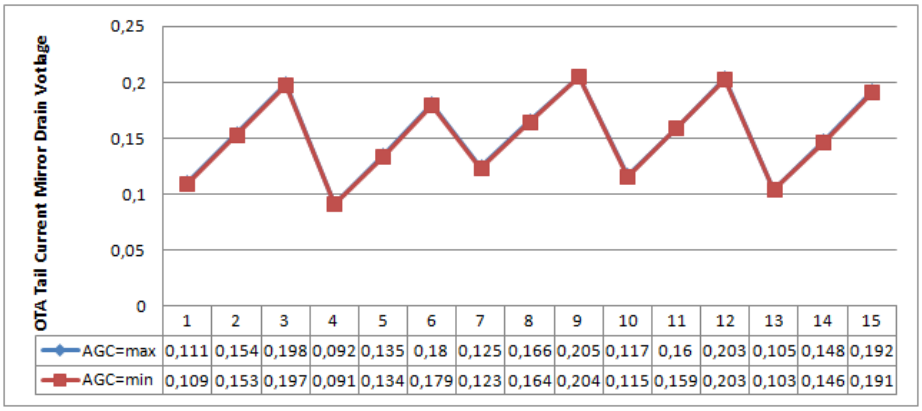


Figure 100: V_{DS} of OTA tail current mirror vs. process and supply ($\#_1$-notation).

Δ from process tt and $V_{DD} = 1.2V$, related to PGA=[000].

Tables 26 and 27 shows how the filter changes across corners relative to corner #2 (typical corner).

		ΔPM[°]		Δf_{ug} [Hz]		$\Delta I_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	PGA=[000]	[A]
tt	1,08	0,218	-0,17	-19	-18	-2,45E-8
	1,2	0,305	0	-2	0	0,00E+0
	1,32	0,423	0,253	13	14	2,25E-8
ss	1,08	-0,76	-1,017	-46	-45	-5,25E-8
	1,2	-0,562	-0,71	-24	-23	-2,67E-8
	1,32	-0,398	-0,572	-7	-7	-5,70E-9
ff	1,08	0,939	0,549	-1	1	9,10E-9
	1,2	1,094	0,656	15	17	3,71E-8
	1,32	1,325	0,856	29	30	6,61E-8
fnsp	1,08	0,887	0,516	-5	-4	-5,70E-9
	1,2	1,074	0,629	12	14	1,90E-8
	1,32	1,303	0,818	28	28	4,25E-8
snfp	1,08	-0,697	-0,98	-36	-35	-4,19E-8
	1,2	-0,578	-0,747	-17	-16	-1,69E-8
	1,32	-0,377	-0,556	-2	-1	4,90E-9
Min		**-0,76**	**-1,017**	**-46**	**-45**	**-5,25E-8**
Max		**1,325**	**0,856**	**29**	**30**	**6,61E-8**

Table 26: Variation in phase margin, unity gain frequency and tail current for all corners relative to corner #2 (typical corner).

		$\Delta A_{v_{NTF}}$ [dB]		$\Delta A_{v_{STF}}$ [dB]	$\Delta V_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	[A]
tt	1,08	6,82	2,35	-0,410	-0,0434
	1,2	2,67	0,00	0,000	0,0000
	1,32	3,8	1,06	0,350	0,0445
ss	1,08	1,16	-2,57	-1,000	-0,0621
	1,2	-1,49	-3,94	-0,540	-0,0191
	1,32	-0,1	-2,70	-0,190	0,0267
ff	1,08	9,79	5,32	0,210	-0,0293
	1,2	7,05	3,99	0,630	0,0116
	1,32	10,38	6,78	1,030	0,0517
fnsp	1,08	8,11	3,23	-0,050	-0,0375
	1,2	2,32	-0,35	0,350	0,0060
	1,32	1,87	-0,33	0,690	0,0500
snfp	1,08	5,89	1,92	-0,770	-0,0493
	1,2	4,14	1,11	-0,330	-0,0063
	1,32	8,29	4,33	0,010	0,0385
Min		-1,49	-3,94	-1,000	-0,0621
Max		10,38	6,78	1,030	0,0517

Table 27: Variation in $A_{v_{NTF}}$, $A_{v_{STF}}$ and V_{DS} of tail current mirror for all corners relative to corner #2 (typical corner).

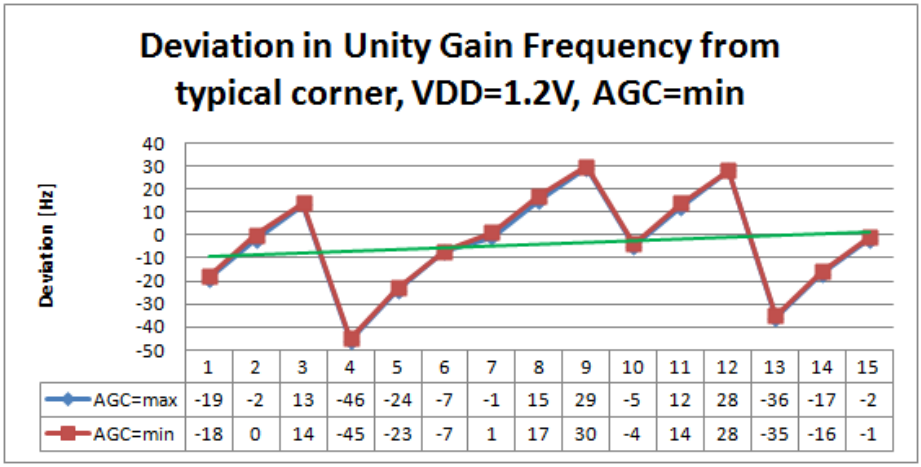


Figure 101: Δf_{ug} [Hz] from typical corner (#2) [Hz], $\#_1$-notation.

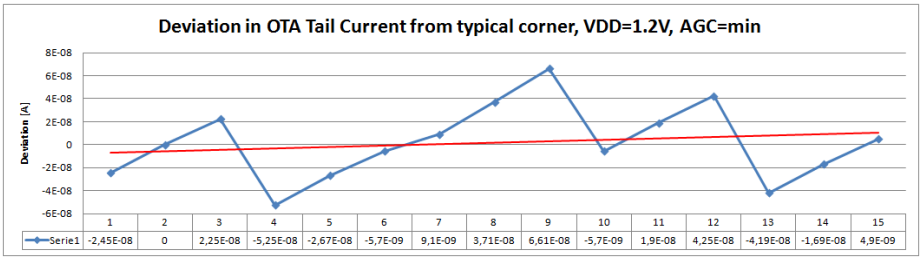


Figure 102: ΔI_{DS} of OTA tail current mirror [A] from typical corner (#2) [A], $\#_1$-notation.

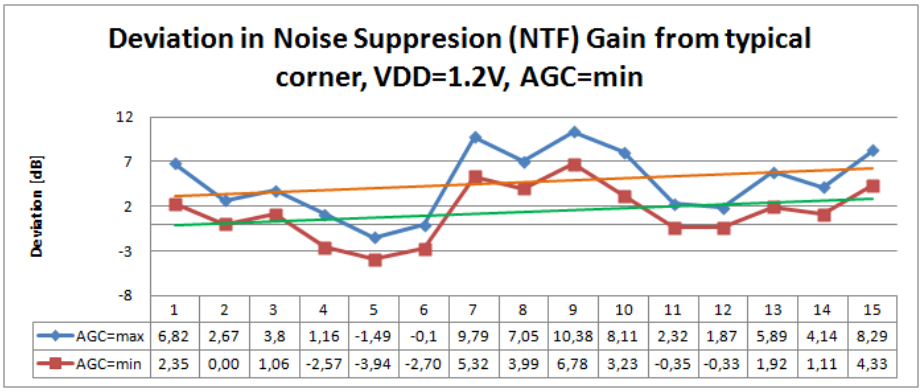


Figure 103: $\Delta A_{v_{NTF}}$ from typical corner (#2) [dB], $\#_1$-notation.

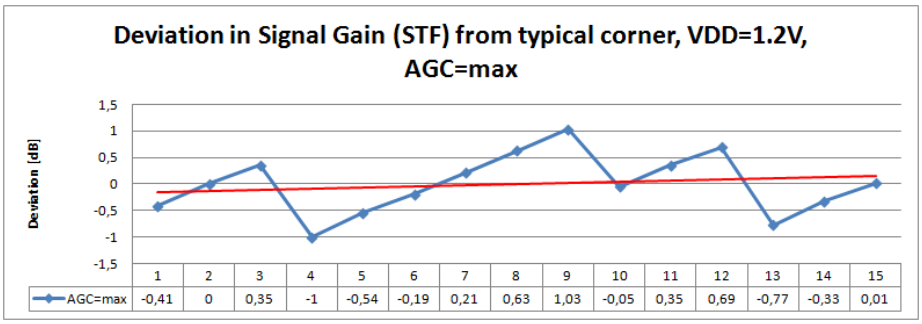


Figure 104: $\Delta A_{v_{STF}}$ from typical corner (#2) [dB], $\#_1$-notation.

Δ from process tt and $V_{DD} = 1.2V$, related to PGA=[000], presented as percentage (%).

Tables 28 and 29 shows how filter changes across corners relative to corner #2 (typical corner), presented as a percentage (%). (Note that the tables are the same as 26 and 27, with the only difference being that the results are presented as percentages).

		ΔPM[°]		Δf_{ug} [Hz]		$\Delta I_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	PGA=[000]	[A]
tt	1,08	0,36%	-0,28%	-1,49%	-1,41%	-6,24%
	1,2	0,51%	0,00%	-0,16%	0,00%	0,00%
	1,32	0,70%	0,42%	1,02%	1,10%	5,73%
ss	1,08	-1,26%	-1,69%	-3,61%	-3,53%	-13,37%
	1,2	-0,93%	-1,18%	-1,88%	-1,81%	-6,80%
	1,32	-0,66%	-0,95%	-0,55%	-0,55%	-1,45%
ff	1,08	1,56%	0,91%	-0,08%	0,08%	2,32%
	1,2	1,81%	1,09%	1,18%	1,33%	9,45%
	1,32	2,20%	1,42%	2,28%	2,35%	16,83%
fnsp	1,08	1,47%	0,86%	-0,39%	-0,31%	-1,45%
	1,2	1,78%	1,04%	0,94%	1,10%	4,84%
	1,32	2,16%	1,36%	2,20%	2,20%	10,82%
snfp	1,08	-1,16%	-1,63%	-2,83%	-2,75%	-10,67%
	1,2	-0,96%	-1,24%	-1,33%	-1,26%	-4,30%
	1,32	-0,63%	-0,92%	-0,16%	-0,08%	1,25%
Min		**-1,26%**	**-1,69%**	**-3,61%**	**-3,53%**	**-13,37%**
Max		**2,20%**	**1,42%**	**2,28%**	**2,35%**	**16,83%**

Table 28: Variation in phase margin, unity gain frequency and tail current for all corners relative to corner #2 (typical corner).

		$\Delta A_{v_{NTF}}$ [dB]		$\Delta A_{v_{STF}}$ [dB]	$\Delta V_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	[A]
tt	1,08	-7,85%	-2,71%	-2,42%	-28,42%
	1,2	-3,07%	0,00%	0,00%	0,00%
	1,32	-4,38%	-1,22%	2,07%	29,14%
ss	1,08	-1,34%	2,96%	-5,91%	-40,65%
	1,2	1,72%	4,54%	-3,19%	-12,51%
	1,32	0,12%	3,11%	-1,12%	17,49%
ff	1,08	-11,27%	-6,13%	1,24%	-19,19%
	1,2	-8,12%	-4,59%	3,72%	7,60%
	1,32	-11,95%	-7,81%	6,09%	33,86%
fnsp	1,08	-9,34%	-3,72%	-0,30%	-24,56%
	1,2	-2,67%	0,40%	2,07%	3,93%
	1,32	-2,15%	0,38%	4,08%	32,74%
snfp	1,08	-6,78%	-2,21%	-4,55%	-32,29%
	1,2	-4,77%	-1,28%	-1,95%	-4,13%
	1,32	-9,55%	-4,99%	0,06%	25,21%
Min		**-11,95%**	**-7,81%**	**-5,91%**	**-40,65%**
Max		**1,72%**	**4,54%**	**6,09%**	**33,86%**

Table 29: Variation in $A_{v_{NTF}}$, $A_{v_{STF}}$ and V_{DS} of tail current mirror for all corners relative to corner #2 (typical corner).

Δ from process tt at fixed V_{DD}, related to PGA=[000].

Tables 30 and 31 shows how the filter varies with process at a fixed supply voltage, V_{DD}, relative to process tt.

		ΔPM[°]		Δf_{ug} [Hz]		$\Delta I_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	PGA=[000]	[A]
tt	1,08	0,39	-	-1,00	-	0,000E+0
ss		-0,59	-0,85	-28,00	-27,00	-2,800E-8
ff		1,11	0,72	17,00	19,00	3,360E-8
fnsp		1,06	0,69	13,00	14,00	1,880E-8
snfp		-0,53	-0,81	-17,00	-17,00	-1,740E-8
tt	1,2	0,31	-	-2,00	-	0,000E+0
ss		-0,56	-0,71	-24,00	-23,00	-2,670E-8
ff		1,09	0,66	15,00	17,00	3,710E-8
fnsp		1,07	0,63	12,00	14,00	1,900E-8
snfp		-0,58	-0,75	-17,00	-16,00	-1,690E-8
tt	1,32	0,17	-	-1,00	-	0,000E+0
ss		-0,65	-0,82	-21,00	-21,00	-2,820E-8
ff		1,07	0,60	15,00	16,00	4,360E-8
fnsp		1,05	0,57	14,00	14,00	4,250E-8
snfp		-0,63	-0,81	-16,00	-15,00	-1,760E-8
	Min	**-0,651**	**-0,85**	**-28**	**-27**	**-2,82E-8**
	Max	**1,109**	**0,72**	**17**	**19**	**4,36E-8**

Table 30: Variation in phase margin, unity gain frequency and OTA tail current versus process at a fixed supply voltage, relative to process tt.

		$\Delta A_{v_{NTF}}$ [dB]		$\Delta A_{v_{STF}}$ [dB]	$\Delta V_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	[A]
tt	1,08	4,47	-	-	-
ss		-1,19	-4,92	-0,59	-0,02
ff		7,44	2,97	0,62	0,01
fnsp		5,76	0,88	0,36	0,01
snfp		3,54	-0,43	-0,36	-0,01
tt	1,2	2,67	-	-	-
ss		-1,49	-3,94	-0,54	-0,02
ff		7,05	3,99	0,63	0,01
fnsp		2,32	-0,35	0,35	0,01
snfp		4,14	1,11	-0,33	-0,01
tt	1,32	2,74	-	-	-
ss		-1,16	-3,76	-0,54	-0,02
ff		9,32	5,72	0,68	0,01
fnsp		0,81	-0,33	0,69	0,01
snfp		7,23	3,27	-0,34	-0,01
	Min	**-1,49**	**-4,92**	**-0,59**	**-0,0191**
	Max	**9,32**	**5,72**	**0,69**	**0,0141**

Table 31: Variation in $A_{v_{NTF}}$, $A_{v_{STF}}$ and V_{DS} of OTA tail current mirror versus process at a fixed supply voltage, relative to process tt.

Δ from process tt at fixed V_{DD}, related to PGA=[000], presented as percentage (%).

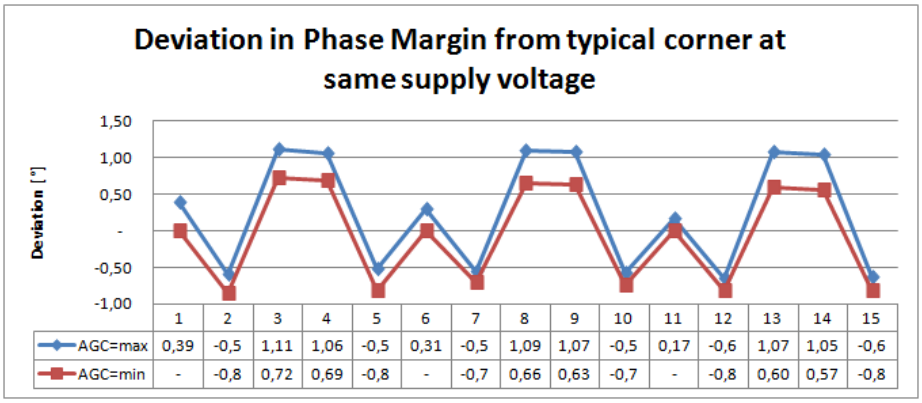
As earlier, tables 32 and 33 shows the same table as 30 and 31, respectively, with the exception being representation in percentage rather than actual value.

		ΔPM[°]		Δf_{ug} [Hz]		$\Delta I_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	PGA=[000]	[A]
tt	1,08	0,65%	0,00%	-0,08%	0,00%	0,00%
ss		-0,98%	-1,41%	-2,23%	-2,15%	-7,60%
ff		1,84%	1,20%	1,35%	1,51%	9,13%
fnsp		1,76%	1,14%	1,04%	1,11%	5,11%
snfp		-0,88%	-1,35%	-1,35%	-1,35%	-4,73%
tt	1,2	0,51%	0,00%	-0,16%	0,00%	0,00%
ss		-0,93%	-1,18%	-1,88%	-1,81%	-6,80%
ff		1,81%	1,09%	1,18%	1,33%	9,45%
fnsp		1,78%	1,04%	0,94%	1,10%	4,84%
snfp		-0,96%	-1,24%	-1,33%	-1,26%	-4,30%
tt	1,32	0,28%	0,00%	-0,08%	0,00%	0,00%
ss		-1,08%	-1,36%	-1,63%	-1,63%	-6,79%
ff		1,77%	1,00%	1,16%	1,24%	10,50%
fnsp		1,73%	0,93%	1,09%	1,09%	10,24%
snfp		-1,04%	-1,34%	-1,24%	-1,16%	-4,24%
	Min	**1,43%**	**-1,54%**	**-2,23%**	**-2,15%**	**-7,60%**
	Max	**5,63%**	**1,59%**	**1,35%**	**2,17%**	**10,50%**

Table 32: Variation in phase margin, unity gain frequency and OTA tail current versus process at a fixed supply voltage, relative to process tt. Presented as a percentage (%).

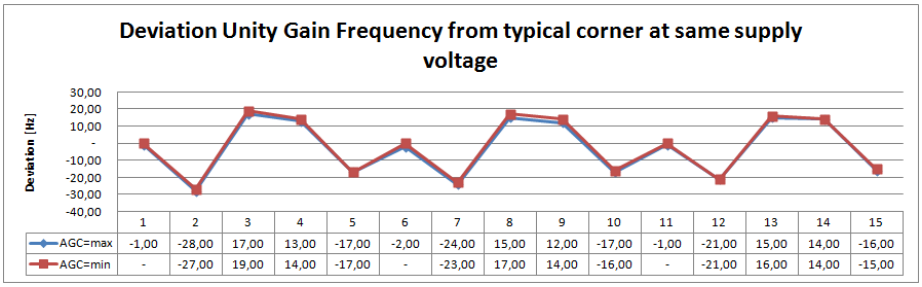
		$\Delta A_{v_{NTF}}$ [dB]		$\Delta A_{v_{STF}}$ [dB]	$\Delta V_{DS_{CM}}$
Process	V_{DD}	PGA=[110]	PGA=[000]	PGA=[110]	[A]
tt	1,08	-5,29%	0,00%	0,00%	0,00%
ss		1,41%	5,82%	7,07%	-17,09%
ff		-8,81%	-3,52%	-3,71%	12,90%
fnsp		-6,82%	-1,04%	-1,61%	5,40%
snfp		-4,19%	0,51%	1,16%	-5,40%
tt	1,2	-3,07%	0,00%	0,00%	0,00%
ss		1,72%	4,54%	4,94%	-12,51%
ff		-8,12%	-4,59%	-5,20%	7,60%
fnsp		-2,67%	0,40%	0,42%	3,93%
snfp		-4,77%	-1,28%	-1,75%	-4,13%
tt	1,32	-3,19%	0,00%	0,00%	0,00%
ss		1,35%	4,38%	4,70%	-9,03%
ff		-10,87%	-6,67%	-7,92%	3,65%
fnsp		-0,94%	0,38%	0,96%	2,79%
snfp		-8,43%	-3,81%	-5,41%	-3,04%
	Min	**-11,41%**	**-1,77%**	**-1,77%**	**-17,09%**
	Max	**-2,71%**	**2,50%**	**2,50%**	**25,35%**

Table 33: Variation in $A_{v_{NTF}}$, $A_{v_{STF}}$ and V_{DS} of OTA tail current mirror versus process at a fixed supply voltage, relative to process tt. Presented as a percentage (%).



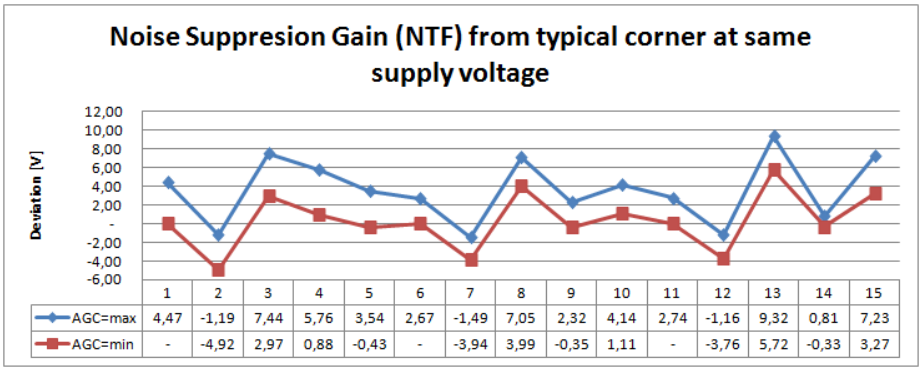
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AGC=max	0,39	-0,5	1,11	1,06	-0,5	0,31	-0,5	1,09	1,07	-0,5	0,17	-0,6	1,07	1,05	-0,6
AGC=min	-	-0,8	0,72	0,69	-0,8	-	-0,7	0,66	0,63	-0,7	-	-0,8	0,60	0,57	-0,8

Figure 105: ΔPM [°] vs. process and supply ($\#_2$-notation). Process has been swept for a fixed $V_{DD} = [1.08, 1.2, 1.32]V$, and related to process tt.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AGC=max	-1,00	-28,00	17,00	13,00	-17,00	-2,00	-24,00	15,00	12,00	-17,00	-1,00	-21,00	15,00	14,00	-16,00
AGC=min	-	-27,00	19,00	14,00	-17,00	-	-23,00	17,00	14,00	-16,00	-	-21,00	16,00	14,00	-15,00

Figure 106: Δf_{ug} [Hz], vs. process and supply ($\#_2$-notation). Process has been swept for a fixed $V_{DD} = [1.08, 1.2, 1.32]V$, and related to process tt.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AGC=max	4,47	-1,19	7,44	5,76	3,54	2,67	-1,49	7,05	2,32	4,14	2,74	-1,16	9,32	0,81	7,23
AGC=min	-	-4,92	2,97	0,88	-0,43	-	-3,94	3,99	-0,35	1,11	-	-3,76	5,72	-0,33	3,27

Figure 107: $\Delta A_{v_{NTF}}$ for $PGA = [000, 110]$, vs. process and supply ($\#_2$-notation). Process has been swept for a fixed $V_{DD} = [1.08, 1.2, 1.32]V$, and related to process tt.

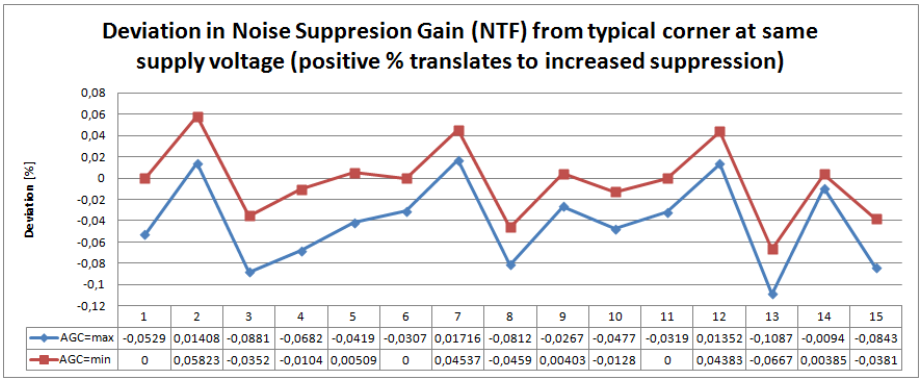


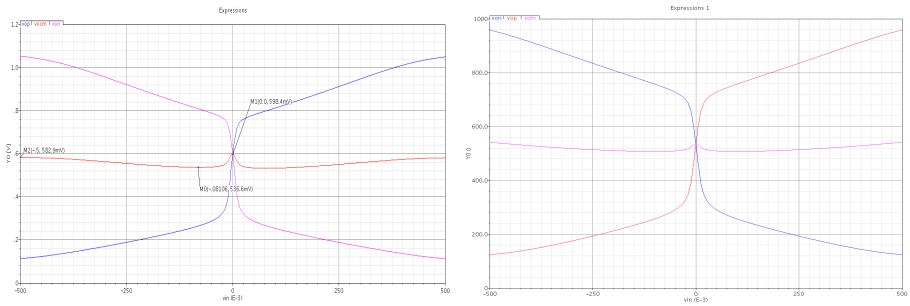
Figure 108: Variation in $\Delta A_{v_{NTF}}$ for $PGA = [000, 110]$ in percentage, vs. process and supply ($\#_2$-notation). Process has been swept for a fixed $V_{DD} = [1.08, 1.2, 1.32]V$, and related to process tt.

11.2 Preamplifier

Unit transistors were stacked in series and four ratios was simulated:

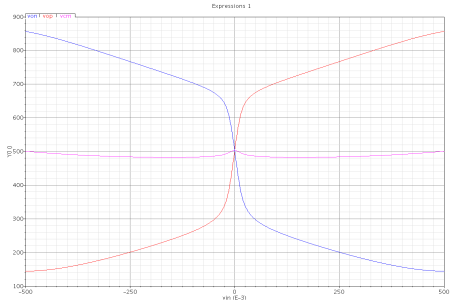
- $\frac{W}{L} = \frac{4}{25}$ (1 unit transistor).
- $\frac{W}{L} = \frac{1}{25}$ (4 unit transistors).
- $\frac{W}{L} = \frac{1}{50}$ (8 unit transistors).
- $\frac{W}{L} = \frac{1}{100}$ (16 unit transistors).

Figure 109 shows that ΔV_{CM} improves with lower W/L-ratio. However, it can also be seen that V_{CM} decreases as well, which is caused by increased gate-to-channel leakage as more devices are stacked and gate area increased. The leakage was found to be almost 50nA in the case of $W/L = 1/100$ ($A = 5.12\mu m^2$). In the same case V_{CM} has decreased from $\simeq 600mV$ to $500mV$ from $W/L = 4/25$ to $W/L = 1/50$. The gate-to-channel leakage also contributes to a reduction in the gain. It was found that the best compromise would be to use $W/L = 1/50$, as it provides sufficient CMFB across process corners and mismatch, while still having an acceptable gain.

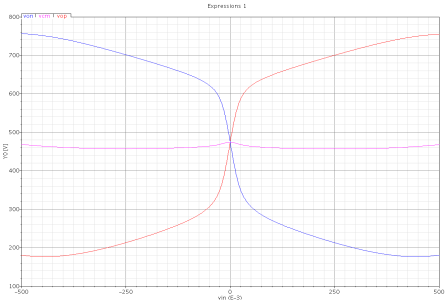


(a) $\frac{W}{L} = \frac{4}{25}$

(b) $\frac{W}{L} = \frac{1}{25}$



(c) $\frac{W}{L} = \frac{1}{50}$



(d) $\frac{W}{L} = \frac{1}{100}$

Figure 109: Differential and common-mode outputs between $\pm 500mV$ differential input, typical corner.

A MOSFET

V_{ch} is a function of the position along the channel length. It describes the disequilibrium of electrons produced by the drain and source voltage V_D and V_S about the Fermi potential, ϕ_F. It can be shown that the channel charge, Q_i can be approximated to:

$$-Q_i \cong C_{ox}(V_G - V_{th}) \tag{117}$$

Where V_{th} is given by:

$$V_{th} \cong V_{th0} + V_{ch} + \gamma(\sqrt{\phi_F + V_{pinch-off}} - \sqrt{2\phi_F}) \tag{118}$$

The slope factor, n, describes the level of inversion, and can be found by differentiating either V_{TB} or V_G with respect to V_{ch}. It is normally under 2, and decreases towards 1 the stronger the inversion. In strong inversion, where $V_{ch} < V_{pinch-off}$, the mobile charge can be described by equation (119).

$$-\frac{Q_i}{C_{ox}} \approx n \times (\frac{V_G - V_{th0}}{n} - V_{ch}) \tag{119}$$

As V_{ch} increases, or consequentially the slope, the mobile charge becomes negligible compared to the charge due to ionized impurities, and the MOSFET gradually behaves more like that of a BJT[12], resulting in the relation in equation (120).

$$-\frac{Q_i}{C_{ox}} \approx e^{\frac{V_G - V_{th0} - nV_{ch}}{nU_T}} \tag{120}$$

Assuming that the charge mobility, μ, is constant, it is possible to derive equations (121) and (122) for strong and weak inversion, respectively.

$$I_D = \mu C_{ox}\frac{W}{L}\int_{V_S}^{V_D} -\frac{Q_i}{C_{ox}}dV \tag{121}$$

$$I_D \sim I_{D_0} e^{\frac{V_G}{nU_T}}(e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}}) \tag{122}$$

Where the approximation of I_{D_0} is shown in equation (123).

$$I_{D_0} \sim \mu C_{ox}\frac{W}{L}e^{-\frac{V_{th0}}{nU_T}} \tag{123}$$

[12]Bipolar junction transistor

As V_{DS} is increased beyond $V_{D_{sat}}$, the drain current saturates to a value $I_{D_{sat}}$. In weak inversion $V_{D_{sat}}$ has a value of a few U_T, which increases the dynamic range for a given supply voltage compared to strong inversion. Moreover; because the MOSFET in weak inversion behaves like a bipolar transistor, its dominant charge transport mechanism is diffusion, unlike in strong inversion where the dominant charge mechanism is surface transportation.

The amount of current that is possible to generate in weak inversion is dependent on the overall size of the transistor since each unit area in the drain and channel layers can generate a certain amount of charge carriers. Therefore, the minimum drain current may be as low as a few pA for minimum-size transistors. For the case of maximum drain current, because of the low $I_{D_{sat}}$, very wide channels are needed in order to operate in weak inversion above a few μA. As for strong inversion, the maximum current is limited by carrier velocity saturation.

The amount of drain current generated can be related to the gate-to-drain transconductance, g_m, which is defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{124}$$

and given by equation (125) and (126) for weak and strong inversion respectively:

$$g_m = \frac{I_D}{nU_T} \tag{125}$$

$$g_m = \frac{\mu C_{ox}}{n}\frac{W}{L}(V_G - V_{th0} - nV_S) = \sqrt{\frac{2\mu C_{ox}}{n}\frac{W}{L}I_D} \tag{126}$$

Because g_m is proportional to I_D in weak inversion, and to $\sqrt{I_D}$ in strong inversion, we see that a transistor operated in weak inversion offers better efficiency.

The lower limit for the source to drain conductance, g_{ds} is given by channel shortening, but is approximately proportional to I_D and inversely proportional to L. Weak inversion therefore offers more gain, as figure 110 suggests.

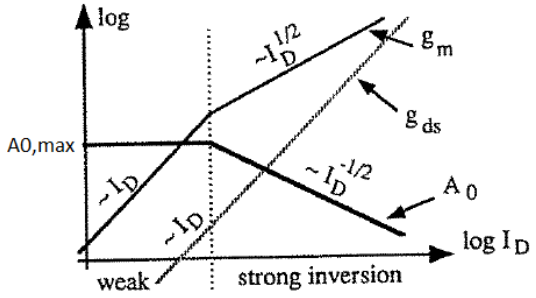


Figure 110: Change of gain, g_m, g_{ds} and inversion with respect to I_D

A.0.1 Noise in MOS transistors

It is important to be able to expect the noise behavior of the MOS transistors in the system, and essential theory will therefore be covered. Normally, the noisy MOSFET is modeled as a noiseless transistor with one noise source at the input and one noise source at the output.

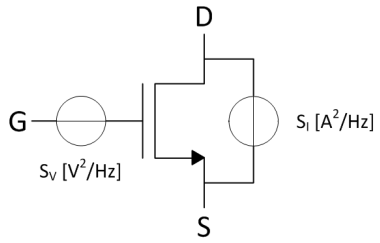


Figure 111: MOSFET noise model

The current noise source, S_I, is white and represents the thermal noise generated by the resistive channel in strong inversion, and is given by equation (127). In weak inversion it represents the shot noise, which is given by equation (128).

$$S_I = \frac{8}{3} nkTg_m \tag{127}$$

$$S_I = 2qI_D \tag{128}$$

The drain current noise for a given I_D is the greatest in weak inversion, and decreases as the inversion gets stronger.

The voltage current noise is flicker noise, which is related to the trapping and release of charge in the silicon-to-silicon-dioxide interface. It can be expressed by the same expression for both strong and weak inversion, which is defined as

$$S_V = \frac{K}{C_{ox} WL \times f} \tag{129}$$

Where the parameter K can be "related" to (130).

$$K = 4kT\rho \tag{130}$$

The parameter ρ is dependent on device characteristics and can vary by a factor of 100 or more from device to device in the same process, though it tends to be larger for n-channel transistors. K is typically in the order of 10^{-24}. Recently, more and more foundries are replacing this simple, K-dependent model with a new, more complex one.

For strong and weak inversion, respectively, we obtain equations (131) and (132) when referring the noise sources to the input gate.

$$V_{in}^2 = \frac{K}{C_{ox}WL \times f} + 4kT\frac{2n}{3g_m} \tag{131}$$

and weak inversion:

$$V_{in}^2 = (\frac{K}{C_{ox}WL \times f} + 4kT\frac{n}{2g_m}) \tag{132}$$

For low frequencies the flicker noise dominates, and the thermal/shot noise at high frequencies. Wide channels helps suppressing both the noise sources, which is an advantageous property in weak inversion. Increasing the length however, only suppresses the flicker noise, and rather increases the white noise as it is inversely proportional to the decreasing g_m.

B Idle-tones in 1^{st}-order $\Delta\Sigma$-modulators

The 1^{st}-order $\Delta\Sigma$-modulator suffers from its fixed pattern noise for DC inputs. The DC level of the signal will be pulse-density modulated and will have a strong tone due to the fixed periodic pattern by which it is represented. Higher-order modulators are free of the fixed pattern noise, and are therefore often preferred.

For the normalized input range of 1, if the input X is a constant 0.25, the output digital bit stream Y from the 1 bit 1^{st}-order modulator will be 0001000100010001...

C The cardiac cycle

Feature	Description	Duration
RR inverval	The interval between an R wave and the next. The normal heart rate is between 60 and 100 bpm[13].	0.6 to 1.2s
P wave	The duration of the P-wave, as seen in figure 2a.	80ms
PR interval	Measured from the beginning of the P wave to the beginning of the QRS complex. This interval is a good estimate of AV node function.	120 to 200ms
PR segment	The time between the end of the P wave and the beginning of the QRS complex. This electrical activity travels down the towards the ventricles, and does not produce any contraction, hence it appears flat on the ECG.	50 to 120ms
QRS complex	The QRS complex is a result of rapid depolarization of the right and left ventricles. Because these muscles have a large mass, the QRS complex has a large amplitude.	80 to 120ms
J-point	The point where the QRS complex finishes and the ST segment begins.	N/A
ST segment	The time between it takes from the QRS complex finishes until the T wave begins.	80 to 120ms
T wave	The T wave represents the recovery of the ventricles.	160ms
ST interval	The ST interval is measured from the J point to the end of the T wave.	320ms
QT interval	Measured from the beginning of the QRS complex to the end of the T wave. A prolonged interval is a risk factor for sudden death.	300 to 430ms
U wave	The U wave follows after the T wave, and have either very low value or are completely absent.	

Table 34: Cardiac waves and intervals

Parameter	Normal value
QRS duration	60 to 100ms
QRS amplitude	$<$ 3.5mV - S amplitude in V1 + R amplitude in V5 $<$ 4.5mV - R+S in a precordial lead $<$ 2.6mV - R in V5 or V6
Ventricular activation time (VAT)	$<$ 50ms in V5 or V6 $<$ 30ms in V1
Q wave	$<$ 40ms in leads other than III and AVR Amplitude less than 1/3 QRS amplitude (R+S) Amplitude less than 1/4 of R wave

Table 35: QRS complex parameters

Electrode label	**Electrode placement**
RA	On the right arm, avoiding thick muscle.
LA	In the same location that RA was placed, but on the left arm.
RL	On the right leg, lateral calf muscle
LL	In the same location that RL was placed, but on the left leg.
V_1	In the fourth intercostal space (between ribs 4 & 5) just to the right of the sternum (breastbone).
V_2	In the fourth intercostal space (between ribs 4 & 5) just to the left of the sternum.
V_3	Between leads V_2 and V_4.
V_4	In the fifth intercostal space (between ribs 5 & 6) in the mid-clavicular line (the imaginary line that extends down from the midpoint of the clavicle (collarbone)).
V_5	Horizontally even with V_4, but in the anterior axillary line. (The anterior axillary line is the imaginary line that runs down from the point midway between the middle of the clavicle and the lateral end of the clavicle; the lateral end of the collarbone is the end closer to the arm.)
V_6	Horizontally even with V_4 and V_5 in the midaxillary line. (The midaxillary line is the imaginary line that extends down from the middle of the patient's armpit.)

Table 36: Placement of electrodes

D MATLAB script for plotting and sizing of transistors

```
clear all;
close all;

%mex loadsig.c;

x = loadsig('eff.sw0');

vds       = getfield(x(2),'data');
Length    = getfield(x(3),'data');
n_id      = getfield(x(4),'data');
n_gm      = getfield(x(5),'data');
n_gm_id   = getfield(x(6),'data');
n_id_w    = getfield(x(7),'data');
n_ro      = getfield(x(8),'data');
n_gmro    = getfield(x(9),'data');
n_ft      = getfield(x(10),'data');
n_vstar   = getfield(x(11),'data');
p_id      = getfield(x(12),'data');
p_gm      = getfield(x(13),'data');
p_gm_id   = getfield(x(14),'data');
p_id_w    = getfield(x(15),'data');
p_ro      = getfield(x(16),'data');
p_gmro    = getfield(x(17),'data');
p_ft      = getfield(x(18),'data');
p_vstar   = getfield(x(19),'data');
driver_id       = getfield(x(20),'data');
driver_gm       = getfield(x(21),'data');
driver_gm_id    = getfield(x(22),'data');
driver_id_w     = getfield(x(23),'data');
driver_ro       = getfield(x(24),'data');
driver_gmro     = getfield(x(25),'data');
driver_ft       = getfield(x(26),'data');
driver_vstar    = getfield(x(27),'data');
cgs_lx20_mn  = getfield(x(32),'data');
cgd_lx19_mn  = getfield(x(33),'data');
cdb_lx22_mn  = getfield(x(34),'data');
cgs_lx20_mp  = getfield(x(47),'data');
cgd_lx19_mp  = getfield(x(48),'data');
cdb_lx22_mp  = getfield(x(49),'data');

%% Length decitions
M1 = 10;
M2 = 10;
M3 = 17;
M4 = 17;

%% Plots:
figure(1);
title('gmro vs gm/id');
ylabel('gmro');
```

```
xlabel('gm/id');
hold on;
plot(n_gm_id(1:236,1:20),n_gmro(1:236,1:20),p_gm_id
    (1:236,1:20),p_gmro(1:236,1:20),'--');
%plot(driver_gm_id(1:236,1),driver_gmro(1:236,1),'r');
%plot(driver_gm_id(1:236,50),driver_gmro(1:236,50),'b');
%plot(driver_gm_id(1:236,499),driver_gmro(1:236,499),'g');
%axis([5 25 10 35]);
%line([12.65;12.65],[10;35]);
line([0;35],[12.65;12.65]);
% line([10.4;10.4],[10;35]);
% plot(n_gm_id(1:236,m1),n_gmro(1:236,m1),'b','linewidth',2);
% plot(n_gm_id(1:236,m2),n_gmro(1:236,m2),'r','linewidth',2);
% plot(p_gm_id(1:236,m3),p_gmro(1:236,m3),'m--','linewidth',2)
    ;
% plot(p_gm_id(1:236,m4),p_gmro(1:236,m4),'g--','linewidth',2)
    ;
legend('N 200n = 1','N 300n = 2','N 400n = 3','N 500n = 4','N
    600n = 5','N 700n = 6','N 800n = 7','N 900n = 8','N 1u = 9
    ','N 1.1u = 10','N 1.2u = 11','N 1.3u = 12','N 1.4u = 13',
    'N 1.5u = 14','N 1.6u = 15','N 1.7u = 16','N 1.8u = 17','N
     1.9u = 18','N 2u = 19','P 200n = 1','P 300n = 2','P 400n
    = 3','P 500n = 4','P 600n = 5','P 700n = 6','P 800n = 7','
    P 900n = 8','P 1u = 9','P 1.1u = 10','P 1.2u = 11','P 1.3u
     = 12','P 1.4u = 13','P 1.5u = 14','P 1.6u = 15','P 1.7u =
     16','P 1.8u = 17','P 1.9u = 18','P 2u = 19');

figure(2);
title('ro vs vds');
ylabel('gmro');
xlabel('vds');
hold on;
plot(vds(1:236,1:20),n_ro(1:236,1:20),vds(1:236,1:20),p_ro
    (1:236,1:20),'--');
% plot(vds(1:236,9),n_gmro(1:236,M1),'b','LineWidth',2);
% plot(vds(1:236,16),p_gmro(1:236,M2),'r--','LineWidth',2);
% plot(vds(1:236,5),n_gmro(1:236,M3),'m','LineWidth',2);
% plot(vds(1:236,11),p_gmro(1:236,M4),'g--','LineWidth',2);
% line([0.1;0.1],[0;35]);
legend('N 200n = 1','N 300n = 2','N 400n = 3','N 500n = 4','N
    600n = 5','N 700n = 6','N 800n = 7','N 900n = 8','N 1u = 9
    ','N 1.1u = 10','N 1.2u = 11','N 1.3u = 12','N 1.4u = 13',
    'N 1.5u = 14','N 1.6u = 15','N 1.7u = 16','N 1.8u = 17','N
     1.9u = 18','N 2u = 19','P 200n = 1','P 300n = 2','P 400n
    = 3','P 500n = 4','P 600n = 5','P 700n = 6','P 800n = 7','
    P 900n = 8','P 1u = 9','P 1.1u = 10','P 1.2u = 11','P 1.3u
     = 12','P 1.4u = 13','P 1.5u = 14','P 1.6u = 15','P 1.7u =
     16','P 1.8u = 17','P 1.9u = 18','P 2u = 19');

figure(3);
title('ft vs gm/id');
ylabel('ft');
xlabel('gm/id');
hold on;
```

```
plot(n_gm_id(1:236,1:20),n_ft(1:236,1:20),p_gm_id(1:236,1:20),
    p_ft(1:236,1:20),'--');
% axis([0 35 0 2e9]);
% line([15;15],[10;35]);
% line([5;25],[29;29]);
% line([10.4;10.4],[10;35]);
% plot(n_gm_id(1:236,9),n_ft(1:236,M1),'b','LineWidth',2);
% plot(p_gm_id(1:236,16),p_ft(1:236,M2),'r--','LineWidth',2);
% plot(n_gm_id(1:236,5),n_ft(1:236,M3),'m','LineWidth',2);
% plot(p_gm_id(1:236,11),p_ft(1:236,M4),'g--','LineWidth',2);
legend('N 200n = 1','N 300n = 2','N 400n = 3','N 500n = 4','N
    600n = 5','N 700n = 6','N 800n = 7','N 900n = 8','N 1u = 9
    ','N 1.1u = 10','N 1.2u = 11','N 1.3u = 12','N 1.4u = 13',
    'N 1.5u = 14','N 1.6u = 15','N 1.7u = 16','N 1.8u = 17','N
     1.9u = 18','N 2u = 19','P 200n = 1','P 300n = 2','P 400n
    = 3','P 500n = 4','P 600n = 5','P 700n = 6','P 800n = 7','
    P 900n = 8','P 1u = 9','P 1.1u = 10','P 1.2u = 11','P 1.3u
     = 12','P 1.4u = 13','P 1.5u = 14','P 1.6u = 15','P 1.7u =
     16','P 1.8u = 17','P 1.9u = 18','P 2u = 19');

figure(4);
title('gm/id vs id/W');
ylabel('gm/id');
xlabel('id/W');
hold on;
plot(n_id_w(1:236,1:20),n_gm_id(1:236,1:20),p_id_w(1:236,1:20)
    ,p_gm_id(1:236,1:20),'--');
legend('N 200n = 1','N 300n = 2','N 400n = 3','N 500n = 4','N
    600n = 5','N 700n = 6','N 800n = 7','N 900n = 8','N 1u = 9
    ','N 1.1u = 10','N 1.2u = 11','N 1.3u = 12','N 1.4u = 13',
    'N 1.5u = 14','N 1.6u = 15','N 1.7u = 16','N 1.8u = 17','N
     1.9u = 18','N 2u = 19','P 200n = 1','P 300n = 2','P 400n
    = 3','P 500n = 4','P 600n = 5','P 700n = 6','P 800n = 7','
    P 900n = 8','P 1u = 9','P 1.1u = 10','P 1.2u = 11','P 1.3u
     = 12','P 1.4u = 13','P 1.5u = 14','P 1.6u = 15','P 1.7u =
     16','P 1.8u = 17','P 1.9u = 18','P 2u = 19');

figure(5);
title('gm/id vs vds');
ylabel('gm/id');
xlabel('vds');
hold on;
plot(vds(1:236,1:20),n_gm_id(1:236,1:20),vds(1:236,1:20),
    p_gm_id(1:236,1:20),'--');
legend('N 200n = 1','N 300n = 2','N 400n = 3','N 500n = 4','N
    600n = 5','N 700n = 6','N 800n = 7','N 900n = 8','N 1u = 9
    ','N 1.1u = 10','N 1.2u = 11','N 1.3u = 12','N 1.4u = 13',
    'N 1.5u = 14','N 1.6u = 15','N 1.7u = 16','N 1.8u = 17','N
     1.9u = 18','N 2u = 19','P 200n = 1','P 300n = 2','P 400n
    = 3','P 500n = 4','P 600n = 5','P 700n = 6','P 800n = 7','
    P 900n = 8','P 1u = 9','P 1.1u = 10','P 1.2u = 11','P 1.3u
     = 12','P 1.4u = 13','P 1.5u = 14','P 1.6u = 15','P 1.7u =
     16','P 1.8u = 17','P 1.9u = 18','P 2u = 19');
```

```
% figure(4);
% ylabel('gmro');
% xlabel('gm/id');
% hold on;
% grid on;
% plot(n_gm_id(1:236,1),n_gmro(1:236,1),n_gm_id(1:236,3),
    n_gmro(1:236,3),'g',n_gm_id(1:236,17),n_gmro(1:236,17),'r
    ')
% plot(p_gm_id(1:236,1),p_gmro(1:236,1),'--',p_gm_id(1:236,3),
    p_gmro(1:236,3),'g--',p_gm_id(1:236,17),p_gmro(1:236,17),'
    r--')
% legend('200n','300n','1u','1u','P200n','P300n','P1u');
% figure(5);
% ylabel('ro');
% xlabel('gmid');
% hold on;
% grid on;
% semilogy(n_gm_id(1:236,1),n_ro(1:236,1),n_gm_id(1:236,3),
    n_ro(1:236,3),'g',n_gm_id(1:236,17),n_ro(1:236,17),'r');
% semilogy(p_gm_id(1:236,1),p_ro(1:236,1),'--',p_gm_id
    (1:236,3),p_ro(1:236,3),'g--',p_gm_id(1:236,17),p_ro
    (1:236,17),'r--');
% legend('200n','300n','1u','1u','P200n','P300n','P1u');
% figure(6);
% ylabel('gm');
% xlabel('gmid');
% hold on;
% grid on;
% semilogy(n_gm_id(1:236,1),n_gm(1:236,1),n_gm_id(1:236,3),
    n_gm(1:236,3),'g',n_gm_id(1:236,17),n_gm(1:236,17),'r');
% semilogy(p_gm_id(1:236,1),p_gm(1:236,1),'--',p_gm_id
    (1:236,3),p_gm(1:236,3),'g--',p_gm_id(1:236,17),p_gm
    (1:236,17),'r--');
% legend('200n','300n','1u','P200n','P300n','P1u');
%% Determine width

W_MIN = 200e-9;

%M5 = 17;
%M6 = 9;



L_M1 = Length(1,M1);
L_M2 = Length(1,M2);
L_M3 = Length(1,M3);
L_M4 = Length(1,M4);
%L_M5 = Length(1,M5);
%L_M6 = Length(1,M6);

gm_id_M1 = 28.9;
gm_id_M2 = 28.9; %instead of 12.75, --> makes it wider -->
    better at leading current from M1
gm_id_M3 = 28.9;
```

```
gm_id_M4 = 28.9;
%gm_id_M5 = 12.75;
%gm_id_M6 = 14;

%gmro = 20;
driver_length = 1;
driver_vds = 1;


ibias1 = 1e-9;
ibias2 = 1e-9;
ibias3 = 1e-9;
ibias4 = 1e-9;

width = 1e-6;

% Because the NMOS transistors operates in weaker inversion,
    they need
% bigger W/L ratios, therefore the smallest transistorwidth
    should be that
% of M4, which therefore sets the required bias current.

%Once ibias has been set, we find the other widths which are
    expected to be
%greater than 200nm.

% M1

%% Finding closest points:
closest1 = 1;
closest2 = 1;
closest3 = 1;
closest4 = 1;
% closest5 = 1;
% closest6 = 1;

%% Closest point given by gmro

% for i = 1:236
%     if abs(n_gmro(i,M1) - gmro) < abs(n_gmro(closest1,M1) -
    gmro)
%         closest1 = i;
%     end
%     if abs(n_gmro(i,M2) - gmro) < abs(n_gm_id(closest2,M2) -
     gmro)
%         closest2 = i;
%     end
% end
% for i = 236:1
%     if abs(p_gmro(i,M3) - gmro) < abs(p_gm_id(closest3,M3) -
     gmro)
%         closest3 = i;
%     end
%     if abs(p_gmro(i,M4) - gmro) < abs(p_gm_id(closest4,M4) -
```

```
    gmro)
%           closest4 = i;
%       end
% end;

%% Closest point given by gm_id
for i = 1:236
    if abs(n_gm_id(i,M1) - gm_id_M1) < abs(n_gm_id(closest1,M1
        ) - gm_id_M1)
        closest1 = i;
    end
    if abs(n_gm_id(i,M2) - gm_id_M2) < abs(n_gm_id(closest2,M2
        ) - gm_id_M2)
        closest2 = i;
    end
    if abs(p_gm_id(i,M3) - gm_id_M3) < abs(p_gm_id(closest3,M3
        ) - gm_id_M3)
        closest3 = i;
    end
    if abs(p_gm_id(i,M4) - gm_id_M4) < abs(p_gm_id(closest4,M4
        ) - gm_id_M4)
        closest4 = i;
    end
%       if abs(n_gm_id(i,M5) - gm_id_M5) < abs(p_gm_id(closest5,
    M5) - gm_id_M5);
%           closest5 = i;
%       end
%       if abs(p_gm_id(i,M6) - gm_id_M6) < abs(p_gm_id(closest6,
    M6) - gm_id_M6);
%           closest6 = i;
%       end;
end;

% Plotting the closest points
figure(1);
plot(n_gm_id(closest1,M1),n_gmro(closest1,M1),'ro');
plot(n_gm_id(closest2,M2),n_gmro(closest2,M2),'ro');
plot(p_gm_id(closest3,M3),p_gmro(closest3,M3),'ro');
plot(p_gm_id(closest4,M4),p_gmro(closest4,M4),'ro');

figure(2);
plot(vds(closest1,M1),n_gmro(closest1,M1),'ro');
plot(vds(closest2,M2),n_gmro(closest2,M2),'ro');
plot(vds(closest3,M3),p_gmro(closest3,M3),'ro');
plot(vds(closest4,M4),p_gmro(closest4,M4),'ro');

figure(3);
plot(n_gm_id(closest1,M1),n_ft(closest1,M1),'ro');
plot(n_gm_id(closest2,M2),n_ft(closest2,M2),'ro');
plot(p_gm_id(closest3,M3),p_ft(closest3,M3),'ro');
plot(p_gm_id(closest4,M4),p_ft(closest4,M4),'ro');

%% Finding the smalles ibias for valid widths
```

```
% While the width is smaller than W_MIN ibias is increased by
    50nA untill a
% valid width is found.

% M1
valid = 0;
while valid == 0
    w = width*ibias1/n_id(closest1,M1);
    if w <= W_MIN;
        ibias1 = ibias1+1e-9;
    else
        valid = 1;
    end
end

% M2
valid = 0;
while valid == 0
    w = width*ibias2/n_id(closest2,M2);
    if w <= W_MIN;
        ibias2 = ibias2+1e-9;
    else
        valid = 1;
    end
end

% M3
valid = 0;
while valid == 0
    w = width*ibias3/p_id(closest3,M3);
    if w <= W_MIN;
        ibias3 = ibias3+1e-9;
    else
        valid = 1;
    end
end

% M4
valid = 0;
while valid == 0
    w = width*ibias4/p_id(closest4,M4);
    if w <= W_MIN;
        ibias4 = ibias4+1e-9;
    else
        valid = 1;
    end
end
% For W/4 > 200nm find length that matches gmro


%% Finding the biggest ibias

% We need to use the biggest ibias since the operation is
    directly
```

```
% dependant of it.
ibias = 0;
if ibias1 >= ibias2 && ibias1 >= ibias3 && ibias1 >= ibias4
    ibias = ibias1;
elseif ibias2 >= ibias1 && ibias2 >= ibias3 && ibias2 >=
    ibias4
    ibias = ibias2;
elseif ibias3 >= ibias1 && ibias3 >= ibias2 && ibias3 >=
    ibias4
    ibias = ibias3;
elseif ibias4 >= ibias1 && ibias4 >= ibias2 && ibias4 >=
    ibias3
    ibias = ibias4;
end;

%% Finding the final ibias and all transistor widths

% From the biggest ibias required, we calculate the
    transistorwidths, if
% any of the widths should get below W_MIN, ibias will again
    be increased
% by 50nA untill all widths are valid.
%ibias = 5e-6;

valid = 0;
while valid == 0;
    W_M1 = width*ibias/n_id(closest1,M1);
    W_M2 = width*ibias/n_id(closest2,M2);
    W_M3 = width*ibias/p_id(closest3,M3);
    W_M4 = width*ibias/p_id(closest4,M4);
    if W_M1 < W_MIN || W_M2 < W_MIN || W_M3 < W_MIN || W_M4 <
        W_MIN
        ibias = ibias+50e-9;
    else
        valid = 1;
    end
end

% W_M5 = width*ibias/n_id(closest5,M5);
% W_M6 = width*ibias/p_id(closest6,M6);

%% Displaying obtained results

disp('ibias1 ibias2 ibias3 ibias 4');
disp(ibias1);
disp(ibias2);
disp(ibias3);
disp(ibias4);

disp('-------------------------------------');

disp('ibias');
disp(ibias);
```

```
disp('W_M1 W_M2 W_M3 W_M4 W_M5');
disp(W_M1);
disp(W_M2);
disp(W_M3);
disp(W_M4);
% disp(W_M5);
% disp(W_M6);

disp('L_M1 L_M2 L_M3 L_M4 L_M5 L_M5');
disp(L_M1);
disp(L_M2);
disp(L_M3);
disp(L_M4);
% disp(L_M5);
% disp(L_M6);

disp('-------------------------------------');

disp('W/L_1 W/L_2 W/L_3 W/L_4 W/L_5');
disp(W_M1/L_M1);
disp(W_M2/L_M2);
disp(W_M3/L_M3);
disp(W_M4/L_M4);
% disp(W_M5/L_M5);

disp('L/W_1 L/W_2 L/W_3 L/W_4 L/W_5');
disp(L_M1/W_M1);
disp(L_M2/W_M2);
disp(L_M3/W_M3);
disp(L_M4/W_M4);
% disp(L_M5/W_M5);

Gm1 = n_gm_id(closest1,M1)*ibias;
Gm2 = n_gm_id(closest2,M2)*ibias;
Gm3 = p_gm_id(closest3,M3)*ibias;
Gm4 = p_gm_id(closest4,M4)*ibias;

disp('-------------------------------------');

disp('Gm (gm1 gm2 gm3 gm4)');
disp(Gm1);
disp(Gm2);
disp(Gm3);
disp(Gm4);

disp('C (nonscaled)');
disp(Gm1/8000);

%% With the given Gm --> find a satisfying M factor which
    gives the required Gm

ibias_req = 10e-9;
M_fac = 1;
for i = 1:250
```

```
    if abs(ibias/i - ibias_req) < abs(ibias/M_fac - ibias_req)
        M_fac = i;
    end
end

disp('-------------------------------------');

disp('M_factor');
disp(M_fac);
disp('ibias');
disp(ibias/M_fac);
disp('Gm1');
disp(Gm1/M_fac);
disp('C_scaled');
disp(Gm1/M_fac/8000);



%% Rounding up ibias to 2uA
%
% disp('-------------------------------------');
% disp('-------------------------------------');
%
% disp('Rounded up to 2uA ibias');
%
% disp('-------------------------------------');
%
% ibias = 2e-6;
% valid = 0;
%
% W_M1 = width*ibias/n_id(closest1);
% W_M2 = width*ibias/n_id(closest2);
% W_M3 = width*ibias/p_id(closest3);
% W_M4 = width*ibias/p_id(closest4);
%
% disp('ibias');
% disp(ibias);
%
% disp('W_M1 W_M2 W_M3 W_M4 W_M5');
% disp(W_M1);
% disp(W_M2);
% disp(W_M3);
% disp(W_M4);
% disp(W_M5);
%
% disp('L_M1 L_M2 L_M3 L_M4 L_M5');
% disp(L_M1);
% disp(L_M2);
% disp(L_M3);
% disp(L_M4);
% disp(L_M5);
%
% disp('-------------------------------------');
%
```

```
% disp('W/L_1 W/L_2 W/L_3 W/L_4');
% disp(W_M1/L_M1);
% disp(W_M2/L_M2);
% disp(W_M3/L_M3);
% disp(W_M4/L_M4);
%
% disp('L/W_1 L/W_2 L/W_3 L/W_4');
% disp(L_M1/W_M1);
% disp(L_M2/W_M2);
% disp(L_M3/W_M3);
% disp(L_M4/W_M4);
%
% Gm1 = n_gm_id(closest1,M1)*ibias;
% Gm2 = n_gm_id(closest2,M2)*ibias;
% Gm3 = p_gm_id(closest3,M3)*ibias;
% Gm4 = p_gm_id(closest4,M4)*ibias;
%
% disp('-------------------------------------');
%
% disp('Gm (gm1 gm2 gm3 gm4)');
% disp(Gm1);
% disp(Gm2);
% disp(Gm3);
% disp(Gm4);
%
%%% With the given Gm --> find a satisfying M factor which
    gives the required Gm
%
%% M_factor: [10nA 20nA 40nA 100nA 200nA]
%
% M_factor = [200 100 50 20 10];
% Gm_scaled = Gm1./M_factor*1e9;
% C_scaled = Gm_scaled/8000*1e3;
%
% disp('-------------------------------------');
%
% disp('ibias: 10nA 20nA 40nA 100nA 200nA');
% disp('M_factor');
% disp(M_factor);
% disp('Gm_scaled [nS]');
% disp(Gm_scaled);
% disp('C_scaled [pF]');
% disp(C_scaled);

%% OLD VALUES:

% M1 = 9;
% M2 = 6;
% M3 = 11;
% M4 = 16;

% gm_id_M1 = 15;
% gm_id_M2 = 19;
% gm_id_M3 = 12.75;
```

```
% gm_id_M4 = 10.4;
% ibias = 1uA, but need 5uA to bias with vds_M1 = 100mV.
```

E Testbench for V_{DS} sweeps for g_m/I_D-methodology

```
.efficiency testbench

*.lib "./L65_SP11_V031.lib" tt

.global vdd vss

.param
+pi = 3.14159265
+length = 600n

.TEMP 25
.OPTION
+     ARTIST=2
+     INGOLD=2
+     MEASOUT=1
+     PARHIER=LOCAL
+     PSF=2
+list
+node
+probe
+post
+dccap=1

*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SP_BJT_V021.lib" TT_BIP
*.INCLUDE "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SP_DIODE_V021.mdl"
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SP_18IO_V032.lib" TT
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SPHVT11_V042.lib" TT
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SPLVT11_V021.lib" TT
.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/L65_SP11_V031.
    lib" TT
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65SP_NCAP11_V011.lib" TYP
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65SP_NCAP18IO_V011.lib" TYP
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SP_RES_V021.lib" res_typ
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SPNVT11_V021.lib" TT
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_18_SPNVT_V021.lib" TT
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65SP_25IO_V011.lib" TT
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65SP_NCAP25_V011.lib" TYP
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_SPNVT25_V011.lib" TT
```

```
*.LIB "/usr/local/PDK/umc65nm/Models/65nm/Hspice/
    L65_momcaps_V011.lib" typ

** Library name: nicole
** Cell name: agm_id
** View name: schematic
mp vss vss vdd vdd p_11_sprvt w=1e-6 l=length sa=160e-9 sb=160
    e-9 nf=1 sd=0 ad=320e-15 as=320e-15 pd=4.32e-6 ps=4.32e-6
mn vdd vdd vss vss n_11_sprvt w=1e-6 l=length sa=160e-9 sb=160
    e-9 nf=1 sd=0 ad=320e-15 as=320e-15 pd=4.32e-6 ps=4.32e-6
mIN vdd vgs vss vss n_11_sprvt w=5e-6 l=length sa=160e-9 sb
    =160e-9 nf=1 sd=0 ad=320e-15 as=320e-15 pd=4.32e-6 ps=4.32
    e-6

vgs vgs 0 dc 550m
vdd vdd 0 1.1
vss vss 0 0

.dc vdd 25m 1.2 0.005 sweep length 200n 50u 100n

.op
.options accurate
.options nomod post

*.print v(vdd) v(vss)
*.print dc lx3(m*) lx4(m*) lx7(m*) lx8(m*)

.probe vds      = par('v(vdd)')
.probe length   = par('L(mn)')

.probe n_id     = par('i(mn)')
.probe n_gm     = par('gmo(mn)')
.probe n_gm_id  = par('gmo(mn)/i(mn)')
.probe n_id_w   = par('i(mn)/W(mn)')
.probe n_ro     = par('1/gdso(mn)')
.probe n_gmro   = par('gmo(mn)/gdso(mn)')
.probe n_ft     = par('abs(gmo(mn)/(2*pi*(cgsbo(mn)+cgdbo(mn)+
    cbdbo(mn))))')
.probe n_vstar  = par('2*i(mn)/gmo(mn)')

.probe p_id     = par('-i(mp)')
.probe p_gm     = par('gmo(mp)')
.probe p_gm_id  = par('-gmo(mp)/i(mp)')
.probe p_id_w   = par('-i(mp)/W(mp)')
.probe p_ro     = par('1/gdso(mp)')
.probe p_gmro   = par('gmo(mp)/gdso(mp)')
.probe p_ft     = par('abs(gmo(mp)/(2*pi*(cgsbo(mp)+cgdbo(mp)+
    cbdbo(mp))))')
.probe p_vstar  = par('-2*i(mp)/gmo(mp)')

.probe driver_id        = par('i(min)')
.probe driver_gm        = par('gmo(min)')
.probe driver_gm_id     = par('gmo(min)/i(min)')
.probe driver_id_w      = par('i(min)/W(min)')
```

```
.probe driver_ro          = par('1/gdso(min)')
.probe driver_gmro        = par('gmo(min)/gdso(min)')
.probe driver_ft          = par('abs(gmo(min)/(2*pi*(cgsbo(min)+
    cgdbo(min)+cbdbo(min))))')
.probe driver_vstar       = par('2*i(min)/gmo(min)')
.end
```