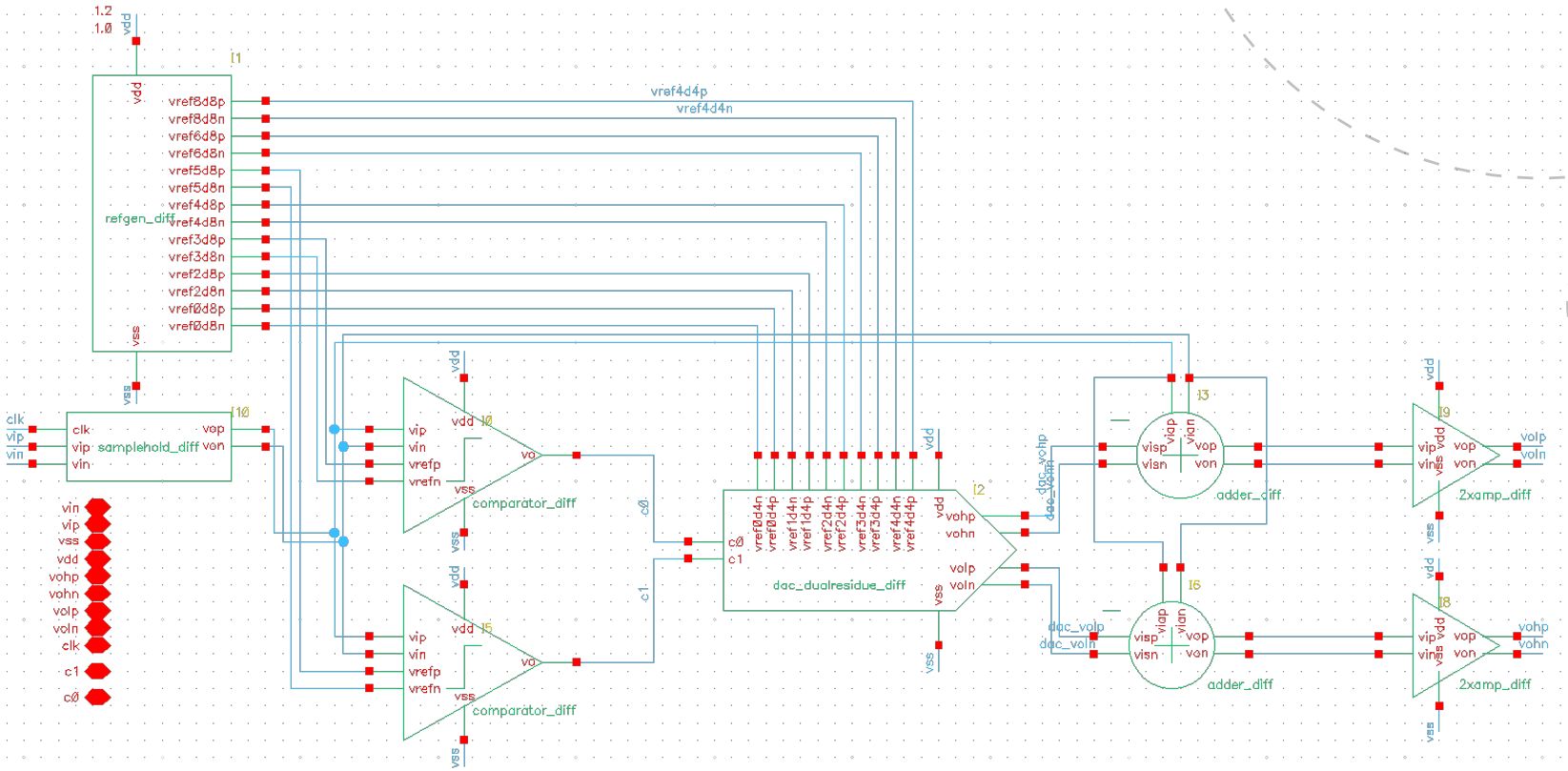
Spec

The objective of this project is to model and design a 50MS/s, 9-bit pipelined ADC in a 3D CMOS technology.
The project consists of the following tasks:

- Perform a literature survey of pipelined ADCs to establish current-state-of-the-art
- Analyze and compare published work
- Develop a behavioral model of the ADC and use the model for deriving specifications of the individual blocks
- Study the characteristics of the 3D CMOS technology
- Design the ADC at transistor level and characterize the performance by simulations
- Perform part of the layout to enable characterization of TSV parasitics and back-annotate to schematics simulations
- $\pm$ 100mV swing

stage1



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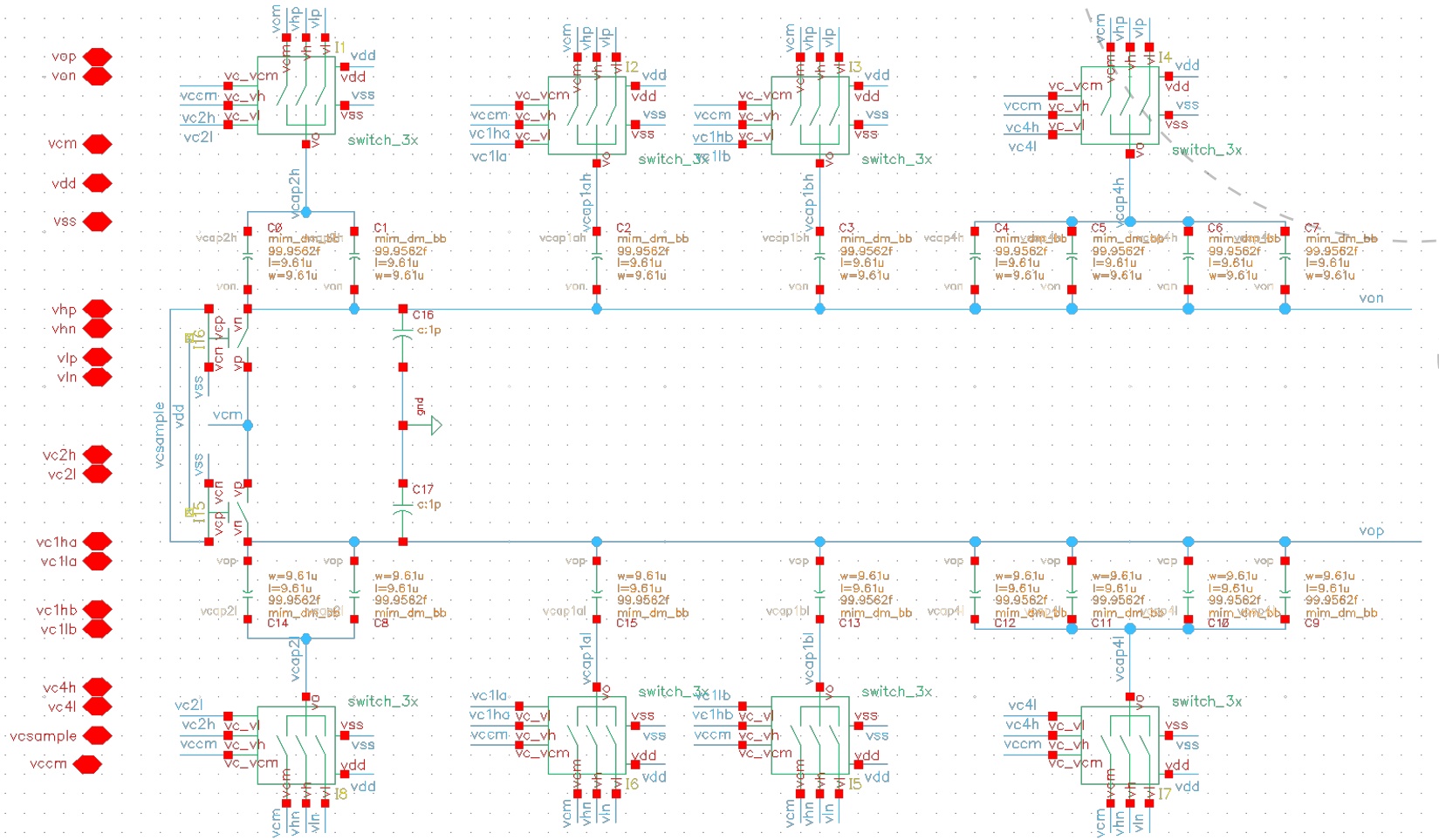
SAR



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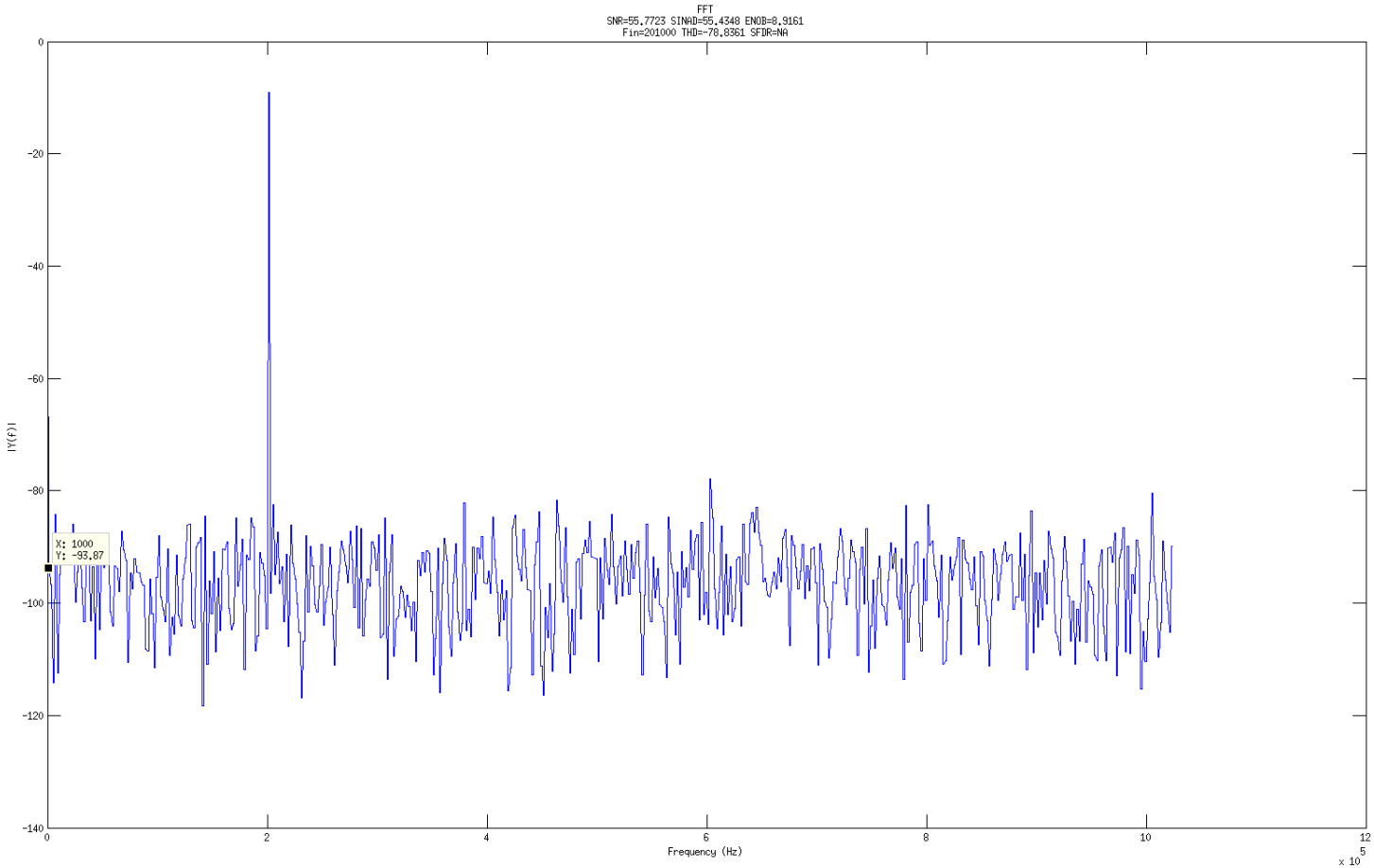
FFT ideal switches



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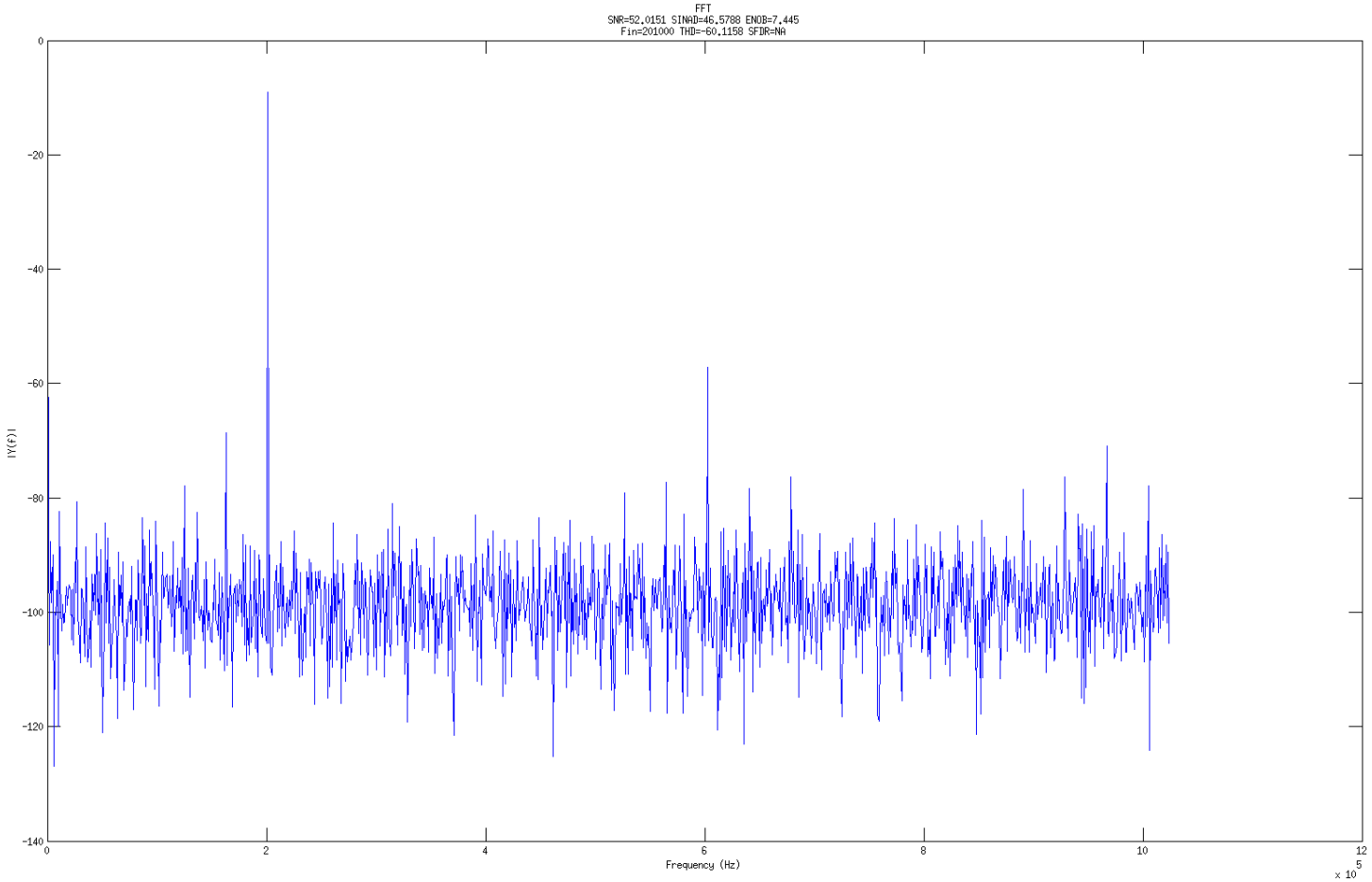
FFT real switches



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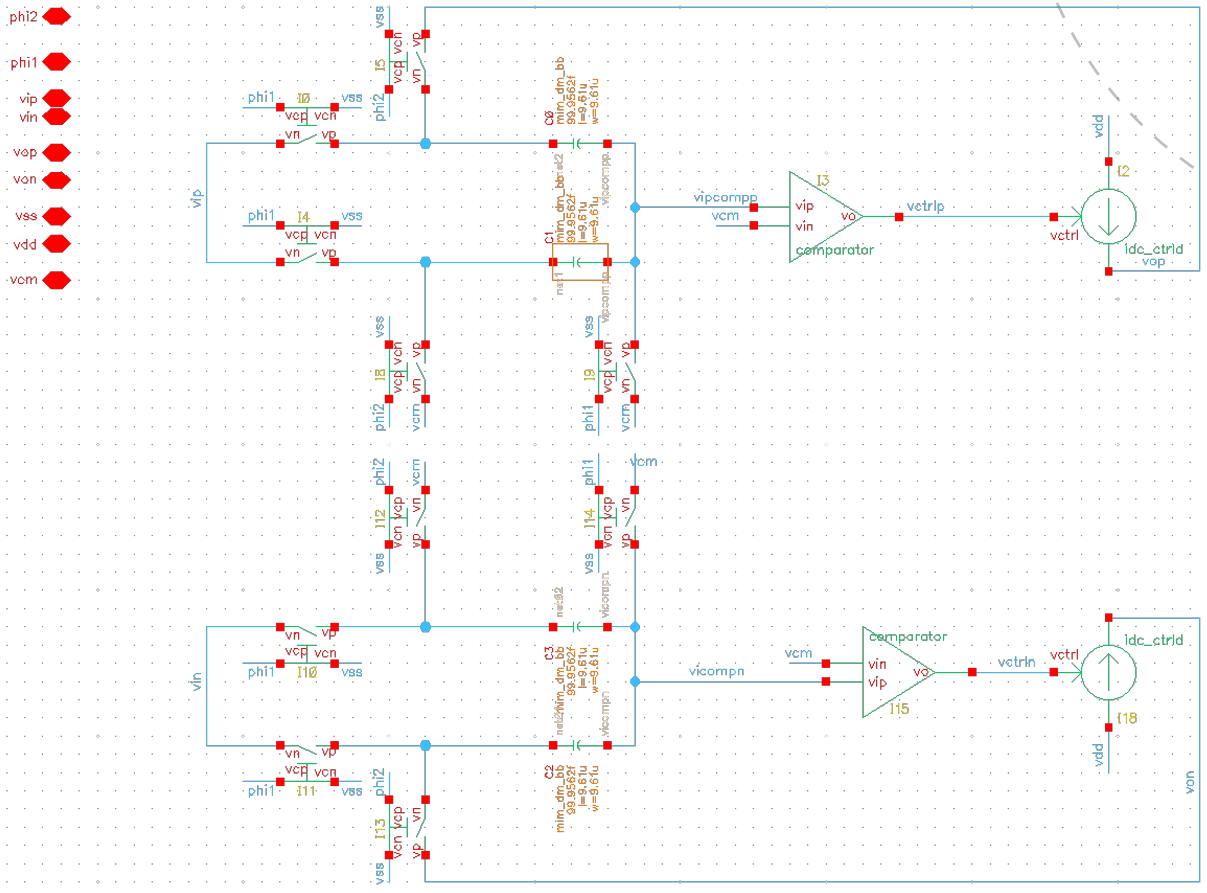

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