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HDMI Transmitter

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Problem Description

The High-Definition Multimedia Interface (HDMI) is a compact audio/video interface for transmitting uncompressed digital data. It is frequently found in multimedia consumer equipment. Traditionally, HDMI transmitters are associated with high cost and high power consumption, limiting their use in embedded equipment.

The student should explore options for low-cost low-power implementations of a HDMI transmitter. The assignment will focus on the implementation of the Transition Minimized Differential Signaling (TMDS) part of the HDMI protocol. The transmitter should be optimized for speed, supporting as many as possible of the defined screen resolutions in the HDMI 1.3 specification across a single digital link, while keeping cost and power to a minimum.

Preface

This report presents the work that has been done in my master thesis, TFE4915, at the Norwegian University of Science and Technology, department of electronics and telecommunications. This is the final part of the education for a master's degree in electrical engineering, where I have specialized in digital circuit design. The study has been conducted during the spring of 2012 at Atmel Norway's headquarters in Trondheim.

HDMI is an important global standard for connecting High Definition (HD) components, and this study involves the planning and design of a low-powered, high performance HDMI-transmitter, with an ultimate goal of implementing it in battery-powered, hand-held multimedia applications.

Some of the sections in the chapters named *HDMI-Theory* and *Hardware Design-Theory* are to a large extent direct copies of sections in my previously published report from my specialization-project on the HDMI-transmitter [1].

My deepest gratitude to Senior Design Engineer Tor Erik Leistad at ATMEL Norway for providing the assignment, and for being my motivator, supervisor and personal help-desk. I would like to thank Professor Einar Johan Aas at NTNUs Department of Electronics and Telecommunications for being my mentor and supervisor, for great advice and contributions. I would also like to thank ATMEL Norway for allowing me to make use of their software, databases and equipment.

Abstract

HDMI is the de facto global standard for connecting HD components and bridging the gap between consumer electronics and personal computer products, making it a priority to develop efficient hand-held, battery-powered units that support the standard.

This is a study into how to design a low-power and high performance system that can transmit HDMI-signals to a valid HDMI-receiver. The main priority is to implement the TMDS part of a HDMI-transmitter, where parallel data is encoded and serialized at high frequencies.

The theory chapters provides an orderly summary of the complex workings of the HDMI-standard, in addition to an introduction to high-performance digital circuit design. This is followed by a system specification chapter, which sets the constraints of the design and discusses the hardware requirements. The subsequent chapter first deals with the design of a straightforward, basic HDMI-transmitter, before moving on to an enhanced design process. The basic design is used as a base for discussions in regard to how effective the suggested enhancement techniques are.

The improvements result in an enhanced design able to operate at 742,5 MHz and support High-Definition video at the impressive resolution of 1080p30. This is achieved by using a 180nm, low-leakage library, and the final design consists of approximately 24.000 unit-sized transistor equivalents, consuming approximately a total of 13,6 mW.

Sammendrag (Norwegian)

HDMI er den ledende globale standarden som skal sørge for at det skal bli både lettere å koble til kilder som leverer høy video-oppløsning. For industrien som leverer forbrukerelektronikk er det en prioritert oppgave å utvikle effektive håndholdte, batteridrevne enheter som støtter HDMI-standarden.

Dette er en studie i hvordan man best kan utvikle et system som kan levere HDMI-video, og som opererer med høy ytelse på lav-effekt. Hovedprioriteten ligger i å implementere TMDS-delen av en HDMI-transmitter, der parallelle data blir kodet om, for så å bli serialisert på svært høye frekvenser.

Teorikapitlene gir et oversiktlig sammendrag av den komplekse standarden som HDMI er, i tillegg til en introduksjon til digital design av systemer med høy ytelse. Videre følger et kapittel som omhandler spesifikasjonen til systemet, der avgrensning av oppgaven og kravene til designet blir diskutert. Det påfølgende kapittelet omhandler først et enkelt, initielt design av en HDMI-transmitter, for så å gå over til prosessen der designet blir forbedret. Det enkle designet blir brukt som en referanse for diskusjoner der man ser på effekten en foreslått forbedring har på designet.

Forbedringene resulterer i en effektivisering av designet i den grad at det er i stand til å operere på 742,4 MHz, og støtte imponerende oppløsninger som 1080p30. Dette blir oppnådd ved å benytte et lavlekkasje 180nm-bibliotek, og det endelige designet består av ca 24.000 transistorekvivalenter med enhetsstørrelse. Designet forbruker ca 13,6 mW.

Glossary

ASIC	Application-Specific Integrated Circuit
BCH	Error-correction code. An acronym made of from the names of the
	creators; Bose and Ray-Chaudhuri.
BIST	Built-In Self-Test
CVT-RB	Coordinated Video Timings - Reduced Blanking
DC	Design Compiler
DVD	Digital Versatile Disc
DVE	Synopsys waveform viewer
DVI	Digital Visual Interface
DVFS	Differential Voltage and Frequency Scaling
ECC	Error Correction Code
FIFO	First In - First Out
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
HD	High-Definition
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
IC	Integrated Circuit
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MSB	Most Significant Bit
PT	PrimeTime
RCA	Electrical connector commonly used to carry audio and video signals.
	Derives from the creators Radio Corporation of America
RTL	Register Transfer Level
SCART	Syndicat des Constructeurs d'Appareils Radiorecepteurs et Televiseurs
STA	Static Timing Analysis
TC	Test Coverage
TERC4	TMDS Error Reduction Code
TMDS	Transition-Minimized Differential Signaling
TPH	Total Pixels Horizontal
TPV	Total Pixels Vertical

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Introduction

Most television sources have previously been transmitting audio and video signals using analog signaling standards. Market-demands, limited network infrastructure and the evolution of multimedia systems have driven the technology towards High-Definition (HD) digital standards. The High-Definition Multimedia Interface (HDMI) has become the leading standard for HD-displays such as televisions, monitors and projectors.

In this master thesis study, parts of a low-power HDMI module will be designed. First as a basic functional system, and further as an enhanced version where the goal of the module is to make it sufficiently efficient in regards of speed and power consumption, so that it may be implemented in a battery-powered system. Achieving this will allow more hand-held products to connect to high-end audio/video-receivers, thereby easily enabling the user to display high-definition movies and pictures.

Initially, the HDMI standard is presented. This is important in order to get to know the key features of the specification, thereby understanding the system requirements and limitations, and how this will ultimately affect the final design. Further relevant low-power and high performance design-techniques are presented, where the focus is on how the different techniques may ensure the functionality and enhance the performance of the design.

Results will to some extent be presented in the context of a particular implementation, but will be wholly presented in a separate chapter. Following the results is a discussion, where the different solutions is compared to the achieved results, and the validity of the results are debated. Finally the conclusion sums up the most important achievements and lists the suggestions for future work.

2

HDMI - Theory

The High-Definition Multimedia Interface (HDMI) is provided for transmitting digital television audio/video-signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and monitor displays [7]. HDMI is the de facto global standard for connecting HD components and bridging the gap between consumer electronics and personal computer products. The HDMI specification combines uncompressed high-definition video and multi-channel audio and data in a single digital interface to provide crystal-clear digital quality over a single cable [8]. A HDMI-system must support high performance and a large bandwitdh due to the uncompressed nature of the signals and the high quality of both audio and video. HDMI is based on Transition-Minimized Differential Signaling technology (TMDS), and is thereby also fully compatible with the Digital Video Interface (DVI) standard [7].

This chapter will focus on theory regarding the parts of the HDMI-system that involves the encoding and transmission of audio and video-signals. This involves a general overview of the operation of an HDMI-transmitter, how video data is encoded using the TMDS encoding algorithm and how audio and auxiliary data-packets are encoded and transmitted. At the end of the chapter, different video formats and bandwidth requirements will be discussed.

2.1 Transmitter Operation

The transmitter is the source of the HDMI-signals. It receives audio/video-data and control-signals from peripheral units. Figure 2.1 shows the TMDS-unit of the transmitter.

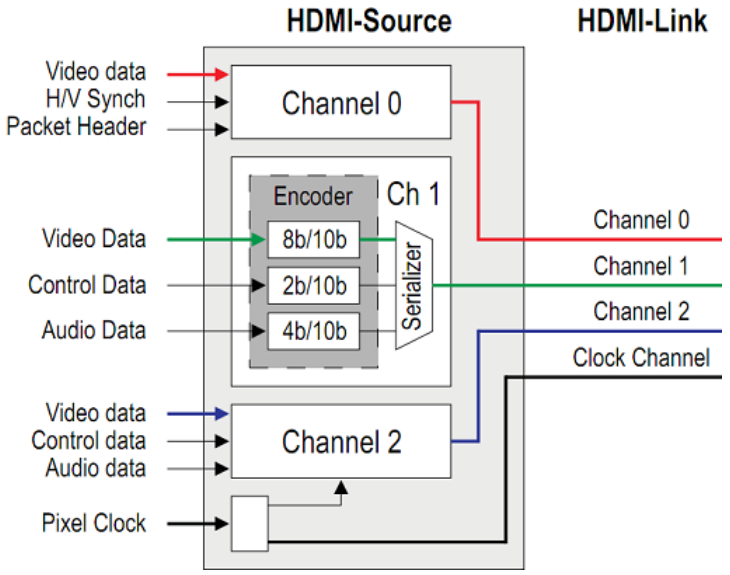


Figure 2.1: TMDS system [19].

2.1.1 TMDS channels

In the transmitter there are three identical encoders, where each is driving one serial TMDS data channel. A HDMI-cable carry four differential pairs that make up the TMDS data and clock channels [7]. The data channels carry auxiliary data in addition to audio and video.

2.1.2 TMDS clock

The TMDS clock frequency is typically related to the video pixel rate, and is used by the receiver to synchronize the data recovery [7]. The transmitter operates on two different clock-frequencies, where the slowest is the TMDS clock frequency. The serialization is done at a frequency which is ten times higher than the TMDS clock frequency. The clock-signal is transmitted on the TMDS clock channel.

2.2 TMDS Operating Modes

HDMI has three different TMDS operating modes:

- *Video Data Period* - Active pixels of an active video line is transmitted.
- *Data Island Period* - A series of packets containing audio and auxiliary data is transmitted.
- *Control period* - Used when no video, audio or auxiliary data needs to be transferred.

The Control Period is also needed between any two periods that are not Control Periods [7]. An example of how the different modes are used in a 720x480 video frame can be seen in figure 2.2. 720x480 refers to the horizontal and vertical number of pixels that builds a complete picture, and they are called the active pixels.

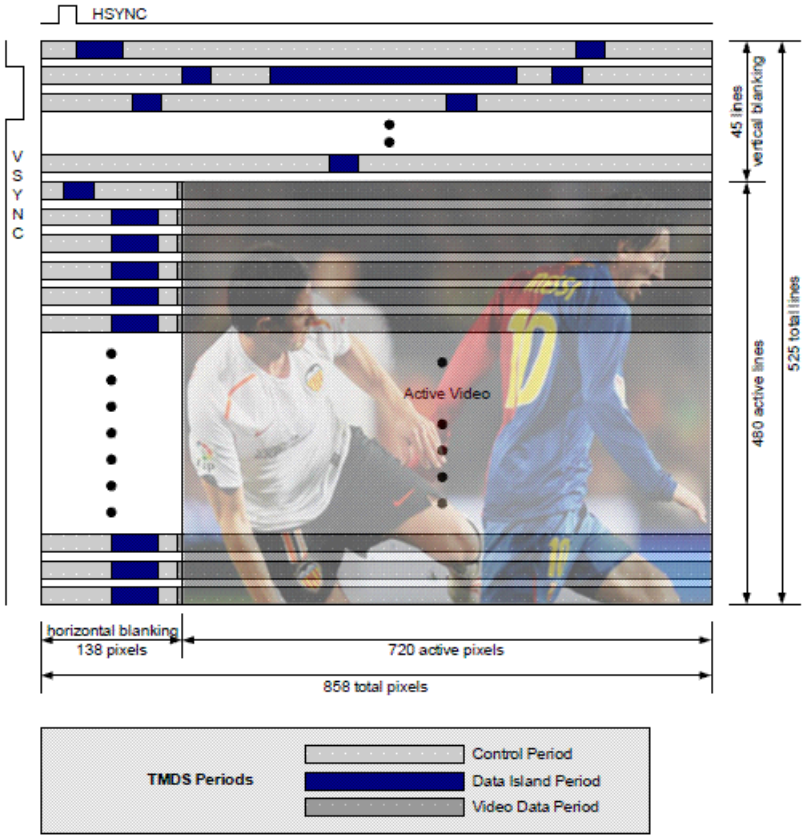


Figure 2.2: TMDS periods in 720x480p video frame [7].

If using 24-bit pixels during Video Data Periods the TMDS encoding converts eight bits per TMDS data channel into a 10-bit DC-balanced, transition-minimized sequence. The sequence is then transmitted serially across the channel pair at a rate of ten bits per TMDS clock period. HDMI uses a packet-structure in order to transmit audio and auxiliary data across the channels during a Data Island Period. This data is protected by BCH error-correction code (ECC). A special TMDS Error-Reduction Code (TERC4) is used to encode a 10-bit word that is transmitted [7]. In the Control Period, a total of six bits (two bit per channel) is encoded into a 10-bit word for each channel, using a transition-minimized encoding. Of the six bits, two of them represent information regarding the horizontal and vertical synchronization (HSYNC/VSYNC) and four bits provides control information (called CTLx-bits). At the end of a Control Period, a preamble is provided using the CTLx-bits, stating if the next period is a Video Data or Data Island Period.

2.3 TMDS Algorithm

Transition-minimized differential signaling is a high speed serial data transmitting technology. An advanced coding algorithm (ref figure 2.4) is incorporated in the transmitter in order to reduce electromagnetic interference over copper cables, and to perform DC-balancing of data transmission over fiber optic cables. It also makes it possible to achieve high skew tolerance due to a more robust clock recovery at the receiver [5]. The algorithm turns a 8-bit word into a 10-bit TMDS encoded word in two stages.

2.3.1 Stage 1: Transition-Minimizing

The first stage produces a 9-bit word, consisting of a new representation of the initial eight bits, and a one bit flag. The representation of the initial eight bits is computed by matching the least significant bit (LSB) of the output with the input. The remaining seven bits of the output is derived from sequential exclusive OR (XOR) or exclusive NOR (XNOR) functions, where each bit of the input is consequently XOR'ed or XNOR'ed with the previous derived bit (and the LSB). The flag indicates which of the two operands (XOR=1/XNOR=0) have been used [5].

An example is shown in figure 2.3 where 01010101 is the input data on the left side. The TMDS encoding algorithm in figure 2.4 will find that there are seven transitions in the input data (transitions are marked as red arrows in figure 2.3). Since the number of transitions in this case is larger than four, the algorithm chooses to transition-minimize the data using XOR. By doing so, the 9-bit output data becomes 100110011, where the MSB states that XOR was used. The remaining eight bits have been converted, and now there are only three data transitions. This makes the data transition-minimized.

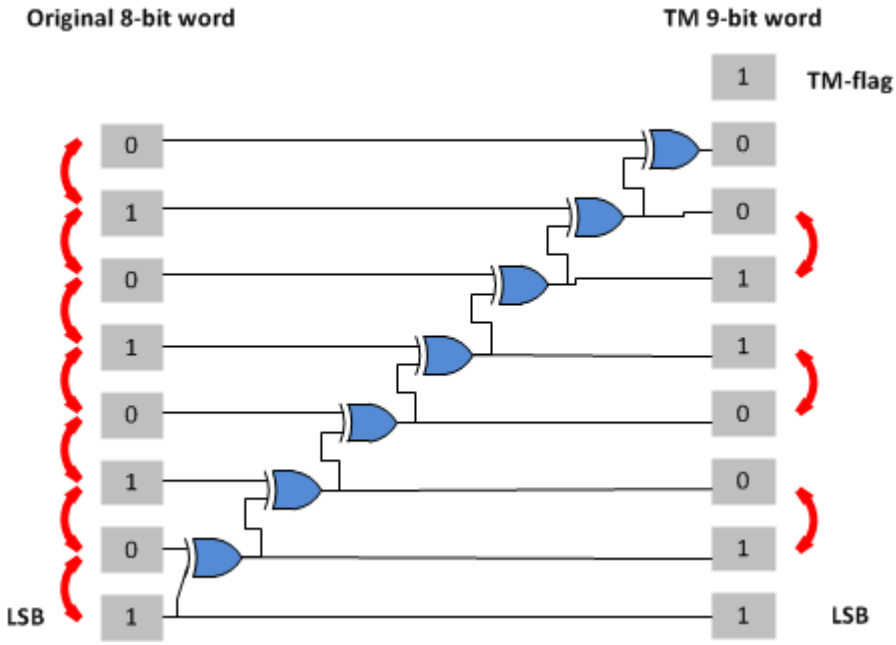


Figure 2.3: Transition-Minimized encoding using XOR.

2.3.2 Stage 2: DC-balancing

The second stage performs an approximate DC-balance on the transmitted stream. A DC-balanced serial data stream means that it has the same number of zeros and ones for a given length of data stream. This is an important feature for certain media-units, as it avoids a build-up of charge in the media [13].

The DC-balancing is done by selectively inverting the 9-bit data representation from the Transition-Minimizing stage. This is based on the running disparity between ones and zeros. If too many zeros have been transmitted and the representation contains more zeros than ones, the code word is inverted. A tenth bit is added and states if the code word has been inverted or not [5].

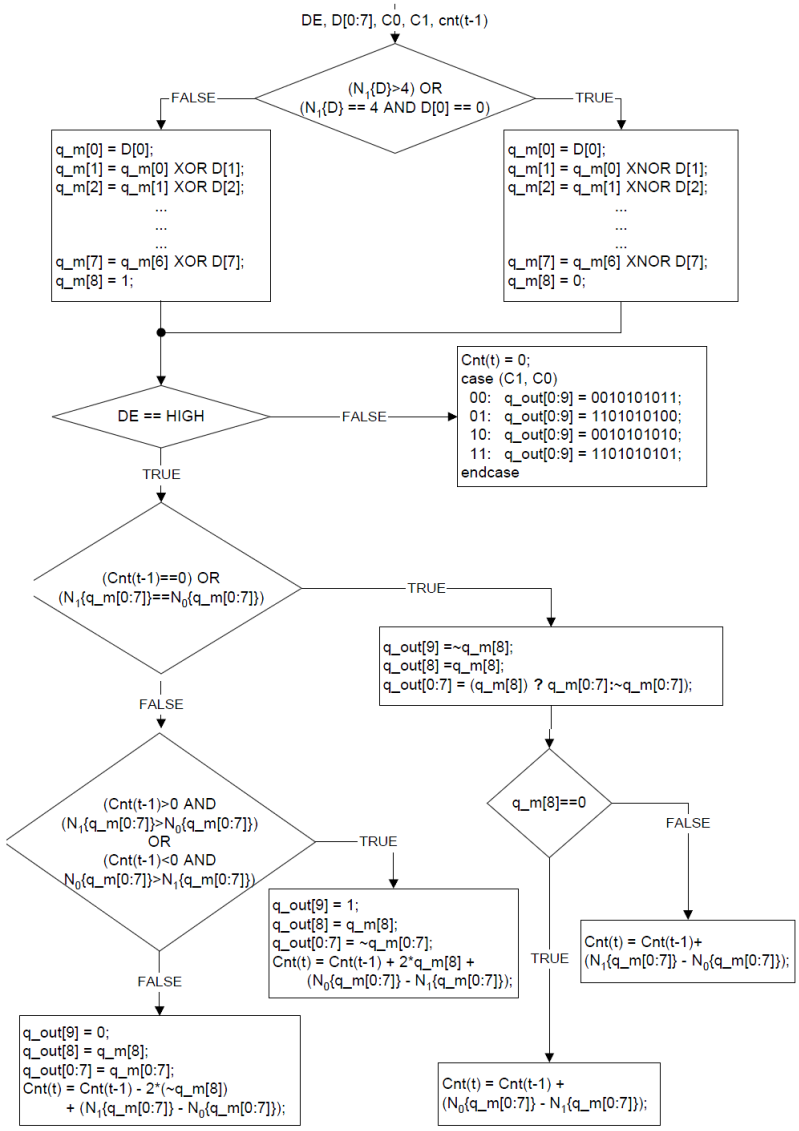


Figure 2.4: TMDS encoding algorithm [5].

2.4 Video Formats

The HDMI-specification supports a number of different video-formats, and a source/ transmitter should ideally support most of them. Some of the formats are optional, while others have to be supported by every transmitter as a minimum required set. In order to make a final specification for the system, it is important to have knowledge of the different factors that form a specific video format, and how this will influence the system performance.

2.4.1 General Video Format Requirements

The latest version of HDMI, version 1.4b, was released October 11, 2011 [18]. This version supports a maximum resolution of 4096x2160 pixels at a frame rate of 24, requiring a channel transfer rate of 3,4 Gbps. The resolution is used in digital movie-theaters. The latest version supports numerous audio/video-coding schemes, different 3D-display variations, 100Mbps ethernet-connection and other features not relevant for this study [18][9]. For a transmitter to be able to supply high definition content to any HDTV, it must support both 1920x1080i and 1280x720p since the HDTV may support only one of the two formats [4]. Some support requirements are in addition to those specified by the Consumer Electronics Association in CEA-861-E. A HDMI source shall e.g. support at least one of the five REQ-mode video formats in table 2.1 [7].

2.4.2 Pixel Encodings and Color Depth

Pixel encodings and color depth combined is often referred to as color space. This is a format in which information is given as to how a pixel is encoded and how colors and intensities are described. HDMI traditionally supports three different kinds of traditional pixel-encodings, the YC_BC_R 4:4:4, YC_BC_R 4:2:2 and RGB [7]. The latest version of the HDMI specification also introduces sYCC601 color, Adobe RGB color and Adobe YCC601 color as three additional new advanced color spaces [10]. HDMI supports four color depths: 24-, 30-, 36- and 48-bit per pixel [7]. If the system is using higher color depths than 24-bit per pixel the TMDS clock rate is increased by the ratio of the pixel size to 24-bit (e.g. 48 bits per pixel doubles the TMDS clock rate) [7]. In the continuation of this study, a 24-bit color depth will be assumed, if not stated otherwise.

2.4.3 Frame Rate

The frame rate is the number of times a complete picture is updated each second. In general, increasing the frame rate will proportionally increase the amount of data needed to be transferred. However, this is not always the case, as for instance with 1080p100 and 1080p120 in table 2.1. Here the number of Total Vertical Pixel stays the same, while Total Horizontal Pixels decrease from 2640 to 2200 when increasing the frame rate from 100 to 120. This reduces the total size of the blanking intervals,

but as the number of blanking intervals increases in accord with the increase in frame rate, the same amount of Data Island Periods will be transferred. The audio and data will thereby not be affected.

2.4.4 Interlaced vs Progressive Scan

When displaying interlaced video, the picture will be made up by displaying the odd and even lines of each frame alternately. This is also called sequential scanning. A picture displayed using Progressive Scan will on the other hand show all the lines of each frame. Progressive Scan is also called non-interlaced scanning. Thus, interlaced video will only use half the bandwidth compared to the progressive video, but the picture will have lower quality and higher distortion [24]. The effect of interlacing is easy to observe on video where an object is moving fast across the screen, as the edge will become blurry.

2.4.5 Bandwidth Calculation

The HDMI specification supports very high transmission-rates. Depending on the pixel resolution of a given video format, a corresponding bandwidth requirement can be calculated. The bandwidth calculations are important, as they determine the system hardware-requirements, in terms of the operational frequency.

Total Bandwidth

The total bandwidth requirement states how much data the transmitter needs to be able to transmit to a receiver each second. For a given resolution, the required total bandwidth is computed using equation 2.1, where TPH and TPV is the total number of horizontal and vertical pixels transferred for a single frame. FR is the frame rate and CDR is the color-depth resolution. The TMDS-encoding requires two extra bits to be transferred on each pixel, and as there are three channels, six bits are added to the color-depth resolution.

$$BWT = TPH \cdot TPV \cdot FR \cdot (CDR + 6) \tag{2.1}$$

Channel Bandwidth

The channel bandwidth requirement states how much data a single TMDS channel needs to be able to transmit each second, and it directly relates the minimum clock rate needed in order to provide the high-speed serial transmission. The required bandwidth for a single channel at a given resolution is computed using equation 2.2. The factors are the same as for equation 2.1, but the difference is that the data is sent in parallel on three channels, and in order to find the single-channel bandwidth, the color-depth resolution is divided by three. The two TMDS-bits for one channel is added.

$$BWC = TPH \cdot TPV \cdot FR \cdot (\frac{CDR}{3} + 2) \tag{2.2}$$

Table 2.1 was made using equations 2.1 and 2.2. The color-depth resolution was set to 24-bit and scan mode is progressive scan for all resolutions in the table. In table 2.1, the *Name* column is the name of the current resolution, and the name is made up by two factors; the number of active, vertical pixels and the frame rate. The $ACTIVE$ column shows the number of horizontal (H) and vertical (V) pixels that are visible. The $TOTAL$ columns is the number of pixels that are transferred for each frame, and is calculated by adding the number of horizontal and vertical blanking pixels to the number of active pixels. The *Hz* column shows the frame rate, and the *MPixel/s* is the total number of pixels transferred each second. The *Gbps* columns show the number of bits transferred each second by the TMDS-channels (*Tot* is for all three channels while *Ch* is for a single channel). The $NOTE$ column is for additional information.

TYPE		ACTIVE		TOTAL		Hz	MPixel/s	Gbps	
NOTE	**Name**	**H**	**V**	**H**	**V**			**Tot**	**Ch**
REQ	**480p59,94**	640	480	800	525	59,94	*25,2*	*0,76*	*0,25*
REQ	**480p60**	640	480	800	525	60	*25,2*	*0,76*	*0,25*
REQ	**480p59,94(2)**	720	480	858	525	59,94	*27,0*	*0,81*	*0,27*
REQ	**480p60(2)**	720	480	858	525	60	*27,0*	*0,81*	*0,27*
REQ	**576p50**	720	576	864	625	50	*27,0*	*0,81*	*0,27*
CEA-861	**720p24**	1280	720	3300	750	24	59,4	*1,78*	*0,59*
CEA-861	**1080p24**	1920	1080	2750	1125	24	74,3	2,23	*0,74*
HDMI 3D	**1080p24 sbs**	3840	1080	5500	1125	24	148,5	4,46	*1,49*
HDMI 3D	**1080p24 fp**	1920	2160	2750	2250	24	148,5	4,46	*1,49*
CEA-861	**720p30**	1280	720	3300	750	30	74,3	2,23	*0,74*
CEA-861	**1080p30**	1920	1080	2200	1125	30	74,3	2,23	*0,74*
HDMI 3D	**1080p30 sbs**	3840	1080	4400	1125	30	148,5	4,46	*1,49*
HDMI 3D	**1080p30 fp**	1920	2160	2750	2250	30	185,6	5,57	*1,86*
CEA-861	**720p50**	1280	720	1980	750	50	74,3	2,23	*0,74*
CEA-861	**1080p50**	1920	1080	2640	1125	50	148,5	4,46	*1,49*
HDMI 3D	**1080p50 sbs**	3840	1080	5280	1125	50	297,0	8,91	*2,97*
HDMI 3D	**1080p50 fp**	1920	2160	2640	2250	50	297,0	8,91	*2,97*
CVT-R	**WQUXGA**	3840	2160	4400	2211	50	486,4	14,59	*4,86*
CEA-861	**720p60**	1280	720	1650	750	60	74,3	2,23	*0,74*
CEA-861	**1080p60**	1920	1080	2200	1125	60	148,5	4,46	*1,49*
HDMI 3D	**1080p60 sbs**	3840	1080	4400	1125	60	297,0	8,91	*2,97*
HDMI 3D	**1080p60 fp**	1920	2160	2200	2250	60	297,0	8,91	*2,97*
CVT-R	**WQHD**	2560	1440	2720	1481	60	241,7	7,25	*2,42*
CVT-R	**WQXGA**	2560	1600	2720	1646	60	268,6	8,06	*2,69*
CVT-R	**WQUXGA**	3840	2160	4000	2222	60	533,3	16	*5,33*
CEA-861	**720p100**	1280	720	1980	750	100	148,5	4,46	*1,49*
CEA-861	**1080p100**	1920	1080	2640	1125	100	297,0	8,91	*2,97*
CVT-R	**WUXGA**	1920	1200	2080	1258	100	261,7	7,85	*2,62*
CVT-R	**WQHD**	2560	1440	2720	1510	100	410,7	12,32	*4,11*
CVT-R	**WQXGA**	2560	1600	2720	1678	100	456,4	13,69	*4,56*
CEA-861	**720p120**	1280	720	1650	750	120	148,5	4,46	*1,49*
CEA-861	**1080p120**	1920	1080	2200	1125	120	297,0	8,91	*2,97*
CVT-R	**WUXGA**	1920	1200	2080	1271	120	317,2	9,52	*3,17*
CVT-R	**WQHD**	2560	1440	2720	1510	120	492,9	14,79	*4,93*
CVT-R	**WQXGA**	2560	1600	2720	1694	120	552,9	16,59	*5,53*

Table 2.1: HDMI: Resolutions and Bandwidths

2.5 Physical Layer

There are many details regarding the physical layers and the electrical specification within the complete DVI- and HDMI specification [5] [7]. However, in the scope of this study, only the most relevant information will be included. The main focus will be on the differential signaling, as this is the physical part of the TMDS technology. The general operating conditions will be listed, along with a short introduction to Low-Voltage Differential Signaling (LVDS), which is important in order to achieve an overall low-power profile for a hand-held, battery-powered HDMI-transmitter.

2.5.1 Operating conditions

The required operating conditions for a HDMI interface is given by table 2.2.

ITEM	VALUE
Termination Supply Voltage, AVcc	3.3 Volts +/- 5%
Termination Resistance, RT	50 ohms +/- 10%

Table 2.2: Required Operating Conditions for HDMI Interface [7].

2.5.2 Differential Signaling

Differential signaling is a method of transmitting information electrically with two complementary signals sent on two paired wires, called a differential pair. External interference tend to affect both wires equally, and a signal is therefore sent as the inverted of the other. The technique improves the resistance to electromagnetic noise compared with the use of single wire and ground as an unpaired reference [22].

2.5.2.1 LVDS

TIA/EIA-644, commonly known as Low-Voltage Differential Signaling (LVDS), is a signaling-method used for low-power, high-speed transmission of binary data over inexpensive copper cables. This signaling technique uses output-voltage levels lower than 5-V differential standards to reduce power consumption, increase switching speed, and allow operation with a 3.3Volt supply rail [20]. It is a physical layer specification only, and the HDMI-standard builds on this specification and adds several layers on top of the physical layer. As the HDMI 1.3 specification utilizes channel bandwidths/data rates ranging from 0,25-2,97 Gbps, the differential signaling comparison in figure 2.5 shows that LVDS is a suitable differential signaling technology for HDMI.

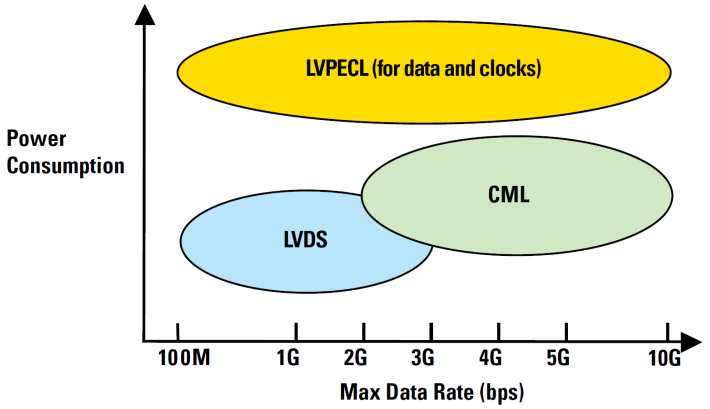


Figure 2.5: Typical Application Targets for Three Common Differential Signaling Technologies [14].

The two other differential signaling technologies are Current-Mode Logic (CML) and Low-Voltage Positive-Emitter-Coupled Logic (LVPECL), which will not be presented here. Additional information can, however, be found in the LVDS owners manual [14]. Differential signaling was chosen for the HDMI-standard due to the excellent noise immunity and the low device-generated switching noise. This is a result of the physical nature of differential signaling, as shown in the conceptual schematic of a TMDS differential pair in figure 2.6.

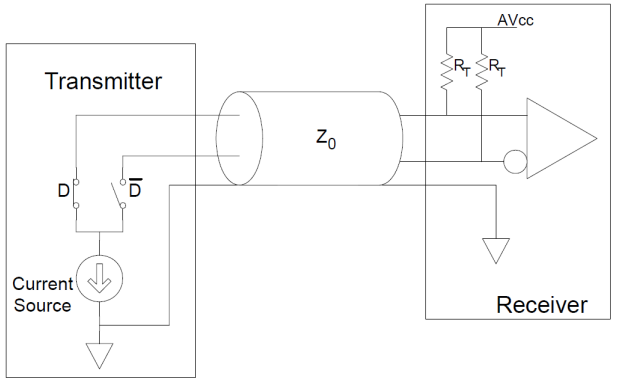


Figure 2.6: Conceptual Schematic for one TMDS differential pair [7].

2.5.3 Connection and cables

A HDMI-connection shall be presented via either a Type- A, B or C connector [7]:

- A - Normal.
- B - Larger connector and carries a second TMDS link (dual link).
- C - Like A, but more compact connector and intended for mobile applications.

A dual link uses an extra set of TMDS pairs, and thereby doubles the bandwidth at a given pixel clock frequency. The dual link is used to support signals greater than 165Mpixels/sec. Otherwise single link shall be used [7].

3

Hardware Design - Theory

Constructing a good low-power design is one of the greatest challenges integrated circuit (IC) designers face today. In order to achieve an overall low power consumption in a system, the process needs to start already at the microchip level. This is also the case when it comes to increasing the performance. Optimizing circuit performance and power consumption at the same time is a major design challenge in modern design [26]. Though the task requires a lot of effort, it is critical in order to extend the battery-life of for instance a portable HDMI-transmitter.

There are several ways to approach the challenge, and there are a lot of trade-offs, both between the different techniques, and in general between power consumption, performance and area costs.

3.1 Power Consumption

The total power consumption is the sum of static, short circuit and dynamic power dissipation, and their relation can be seen in equation 3.1.

$$P_{total} = P_{static} + P_{shortcircuit} + P_{dynamic} \tag{3.1}$$

3.1.1 Static Power Dissipation

Static power is dissipated when a part of logic is disabled or inactive, and the clock is stopped. As there is no activity, the dissipation is due to leakage currents. The extent of the dissipation is dependent on the fabrication technology and the size of the logic area. In general, the supply voltage has been continuously lowered, in accordance with the down-scaling of the fabrication technology, to reduce the dissipation.

A common applicable technique that may reduce the static power dissipation is multi-threshold logic. Changing the threshold voltage of the logic causes a change to the speed and power dissipation of the logic as well. A higher threshold results in less static power dissipation, but on the other hand, it also reduces the speed. Synthesis tools will to a large extent help decide if and where a change in threshold voltage

should be applied, although some manual interaction may be needed. With a multi-threshold library, a designer can choose high- or low-threshold cells in their design. Low-threshold cells are used in the critical path for performance requirement while the high-threshold cells are used in the non-critical path for low-power consideration [17].

Another possibility is to apply power gating, which will turn off the voltage supply to parts of a module when they are not in use. This will eliminate the static power dissipation while it is deactivated [15].

3.1.2 Short Circuit Power Dissipation

Short-circuit power, also known as crowbar- or rush-through power, arises in CMOS technology due to a direct current path between the supply and ground. The path is created because of the finite rise and fall times of the pMOS and nMOS transistors. The short circuit power dissipation component is usually not significant in logic design, but it appears in transistors that are used to drive large capacitances (for instance bus wires and off-chip circuitry) [15].

3.1.3 Dynamic Power Consumption in General

The average dynamic power consumption for a given system is calculated using equation 3.2, where P_{dyn} is the average consumption, f is the clock frequency, C is the switched capacitance, V_{DD} is the supply voltage and α is the switching activity [15].

$$P_{dyn} = \frac{1}{2} \cdot f \cdot C \cdot V_{DD}^2 \cdot \alpha \tag{3.2}$$

Enhancement-techniques that reduce the switching activity optimizes the system in regard to achieving the same system functionality while switching only a minimal number of transistors [15]. This scheme span several design hierarchy levels, including synthesis- and algorithmic levels.

As can be seen from the quadratic term in equation 3.2, it is easily derived that the dynamic power may be significantly reduced by scaling down the supply voltage of the computational elements. Down-scaling the supply voltage has a positive effect on the static power dissipation (as mentioned in section 3.1.1) and may for a fixed threshold also reduce the short circuit power consumption [3]. However, the negative effect of scaling down the supply voltage of a computational element is an increase of the execution delay of that element.

3.2 Clock Gating

Clock gating is an efficient technique in order to reduce dynamic power dissipation in synchronous circuits. Clock gating reduces the dynamic power dissipation by disconnecting the clock from an unused circuit block. The clock signal switches every cycle, and therefore has an activity factor of 1. In a traditional synchronous system, the clock network is connected to the clock pin on every flip-flop in the design, and the entire clock tree is switched on each clock cycle. Power is consumed on each edge by the buffers in the clock tree and the clock pin of flip-flops even if the data input of the flip-flops are steady. [15].

3.2.1 Implementation

Parts of this power-consumption can be reduced by adding additional logic, which allows for pruning of the clock tree. This allows for parts of the circuit to be turned off when it is not in use, leaving only leakage current to contribute to the total power consumption. Clock gating is implemented by identifying groups of flip-flops sharing an enable signal. The clock and enable signal is connected using an AND-operator to generate a gated clock, as shown in figure 3.1 [15].

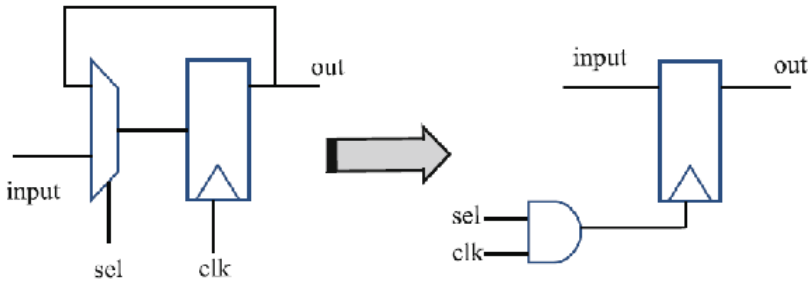


Figure 3.1: Simple gated clock transformation [15].

3.2.2 Considerations

If a design implements clock gating, there are several important considerations. The considerations are in regard of functionality and area cost, but it is especially important for this system to consider how clock gating may influence the performance of the system. Due to the addition of the AND gate for the gated clock, this may result in additional clock skew. For a high-performance design, this clock skew could be significant and should be considered carefully [15]. Due to the extra logic of a clock-gating scheme, the area cost will normally increase. On the other hand, in some cases it is possible to replace a large number of multiplexers with a single shared clock gate, thereby actually decreasing the total area cost [15]. If the clock is gated on the input to a register (as in figure 3.1), this may result in glitches on the gated clock signal.

This does not only cause unnecessary power consumption, but it may also cause the design to malfunction [16]. In order to get a spike-free signal it is common to improve the simple gated clock by adding a latch and an inverter, as can be seen in figure 3.2.

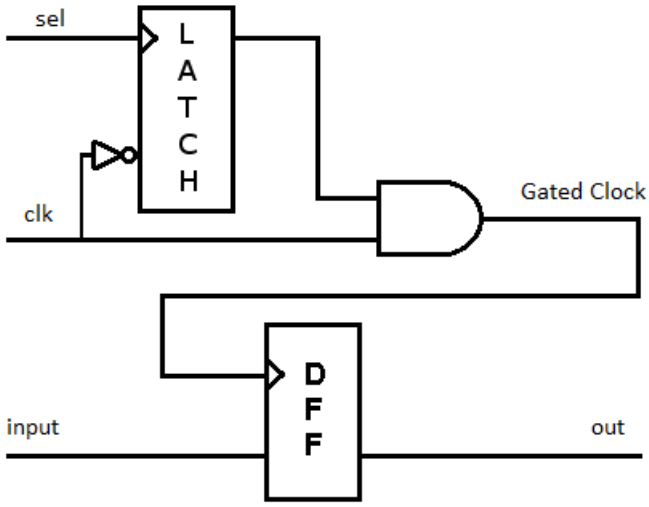


Figure 3.2: Spike-free gated clock.

By adding the latch and the inverter, the sel/clock enable signal gets a setup/hold timing demand that the synthesis tool must relate to. This eliminates the possible spike-related errors.

3.3 Parallelization

There are several ways to optimize the performance of a system. Increasing the clock-frequency will for instance proportionally increase the computational speed, but it will also proportionally increase the dynamic power consumption. Parallelization can be used to increase the computational speed by dividing a task in parts, and increase the throughput by performing computations in parallel.

Another approach is to apply dynamic voltage and frequency scaling (DVFS). From the dynamic power equation (3.2), it is given that the power consumed is proportional to the operation frequency and the square of the supplied voltage. This means, when required timing and performance constraints are satisfied, frequency and voltage can be scaled separately or simultaneously to reduce the power consumption. In cases where maximum performance is not needed, a dynamic voltage and frequency scaling scheme can be applied in order to achieve low power [17]. This can be exploited by parallelization and decreasing the frequency, which results in a reduced supply voltage. Since the dynamic power do, as already stated, depend on the square of the voltage, this will have an impact on the power consumption.

3.4 Pipelining

Pipelining is a hardware design technique utilizing parallelism to increase the computation rate of a system. How efficient pipelining is depends on the executed algorithm and the data that is to be computed. Pipelining of suited computations will result in a significant performance increase. If an algorithm can be divided into a fixed number of steps to be executed in sequence, pipelining can be implemented. This realization consists of two or more hardware stages separated by registers. There is one stage for each step of the algorithm, and the stages must be interconnected in the same order that the steps are executed [12]. Due to the need of additional registers, the area cost will increase. An example of a two-stage pipelined module can be seen in figure 3.3.

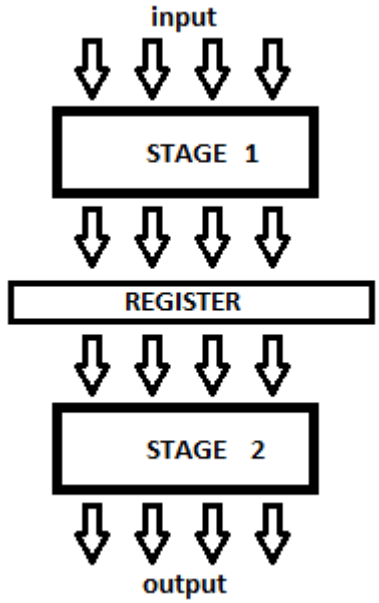


Figure 3.3: Two-stage pipeline module.

Pipelining can only be used effectively when the algorithm is applied repeatedly to a stream of input data [12]. Note that in some cases where the timing initially is acceptable and the execution is satifactory, the addition of a pipeline stage will actually double the delay through the circuit for a single execution, though the throughput will stay the same. When using clock gating and pipelining together, there is the possibility that glitches can propagate down the pipeline and cause extra switching of wires and transistors [11]. A way to avoid this problem is to use the spike-free clock-gating technique shown in figure 3.2

3.5 Technology scaling

In the scope of this study, technology scaling relates to the the size of the geometry. Different sizes have both positive and negative effects. Small technologies are by nature more area effective, but the smaller technology is also more expensive. The increased cost will however normally not outweigh the benefit of reducing the area. The small technologies requires lower supply voltages, and thereby have a lower dynamic power consumption (ref equation 3.2). The computational throughput is higher, but they suffer from larger static power dissipation. The optimal technology is dependent on the objective of the application, and must be chosen based on the design priorities.

3.6 Time Domain Crossing

This section focus on Time Domain Crossing, a subject regarding the problems that may or will arise, when data is to be transferred between two or more domains running on different clock frequencies. The problems arise due to metastability, and a design with such problems needs a synchronizer in order to handle the issue.

As the HDMI-system has two clock domains, where one is ten times faster than the other (ref section 2.1.2), this section will cover the fundamentals of metastability and synchronizers.

3.6.1 Metastability

Sending signals between hardware domains operating at different clock frequencies may lead to bad data integrity if the signals are not properly synchronized. Metastability is a condition where an output of e.g. a register is in a fluctuating, unknown state. In other words, there is an indecision of whether the output should be '0' or '1'. This may occur if signals are clocked into flip-flops without the proper setup-times, and an example of this is presented in figures 3.4 and 3.5.

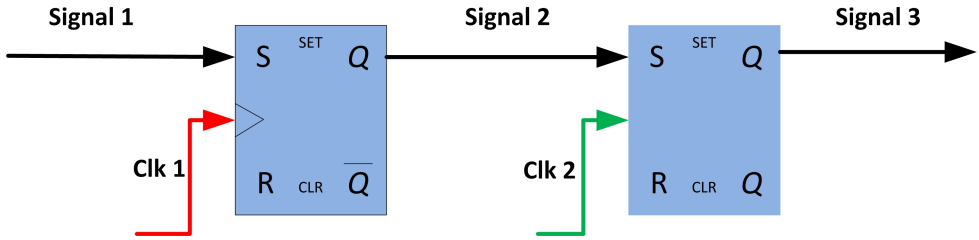


Figure 3.4: Two flip-flops with different clock domains

If the connection between different time domains is as presented in figure 3.4, there is a chance of experiencing metastability if *Signal 2* misses the setup time. This can be seen in figure 3.5, where *Signal 3* is metastable for almost the duration of a *Clk 2* clock cycle.

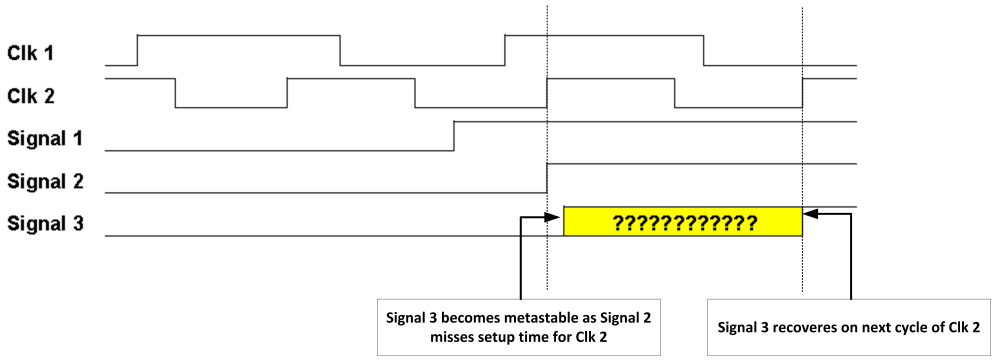


Figure 3.5: Example of metastability.

There are several ways of dealing with metastability. One of them is by simply not allowing signals to cross between the domains. However, if this is unavoidable, synchronizers must be introduced in order to prevent metastability.

3.6.2 Synchronizers

A synchronizer is a device that samples an asynchronous signal and outputs a version of the signal that has transitions synchronized to a local or sample clock [25]. The two-stage synchronizer is very applicable, and is the most common synchronizer. For most applications, the two-stage synchronizer is sufficient to remove all likely metastability. It is however only effective when the signal being passed to another domain is in a high state long enough to be detected. There are numerous other synchronizers, like the edge-, pulse- and level-synchronizers, and they have different advantages and drawbacks [25].

3.7 Design for testing

Design for testing (DFT) is a comprehensive subject, and will not be fully covered in this study. It is, however, important to mention some of the subjects, such as SCAN-logic, as this will be implemented further on. Built-In Self-Tests (BISTs) are also briefly presented, as they will be part of the future work.

3.7.1 SCAN-logic

SCAN-logic is normally implemented by a synthesis tool, and increases the testability of a design. The tool will replace regular registers with SCAN-registers, and thus enabling test-vectors to be loaded into the design. This is done several times in the post-production phase to ensure that the product is fully operational and that there are no manufacturing defects.

A SCAN flip-flop is slower and larger than a regular flip-flop, as an additional multiplexer is incorporated in the flip-flop (see figure 3.6).

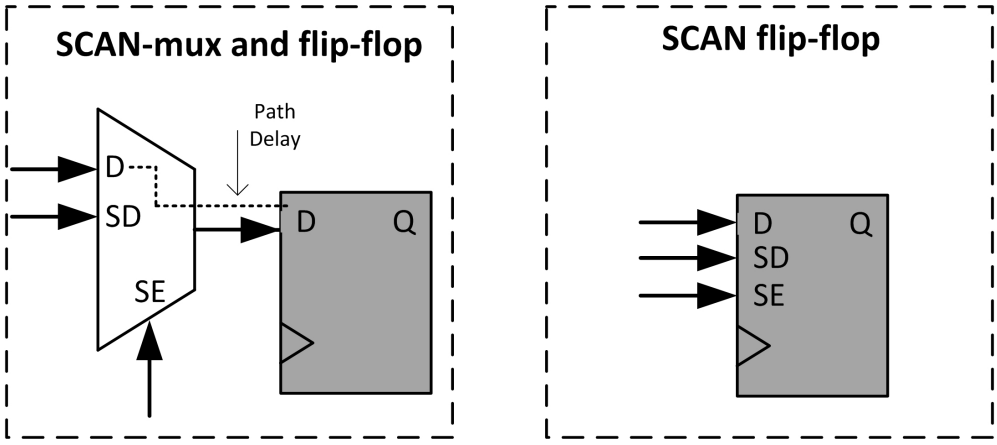


Figure 3.6: SCAN logic and flip-flops.

Test-Coverage (TC) is a value given in percent, which is an estimate of how many of the possible defects can be discovered with the implemented SCAN-logic. A high test-coverage is desirable, but it comes at a cost. The SCAN-logic will slightly increase the power consumption and the area cost, and it will slightly reduce the speed.

3.7.2 BIST

A Built-In Self-Test (BIST) is a mechanism that permits a machine or a circuit to test itself. The BISTs are designed to meet requirements such as high reliability and lower repair cycle times, or constraints such as limited technician accessibility and cost of testing during manufacture. These tests are commonplace in unattended machinery of all types and integrated circuits [2].

4

System Specification

In this chapter, the final system specification will be outlined, based on the discussion in the specialization project report [1] and the problem description.

This specification will establish the hardware requirements and the constraints of the design.

4.1 Constraints

The problem description states that *The assignment will focus on the implementation of the Transition Minimized Differential Signaling (TMDS) part of the HDMI protocol.* Due to this constraint, no effort will be put into creating and designing the control logic and bus-interfaces surrounding the TMDS part of the HDMI-transmitter.

As there are no other available designs to compare against, it will be hard to draw firm conclusions in regard to the efficiency of this HDMI-transmitter. The comparison will have to be based on the comparison of a self-made basic design.

4.2 Hardware requirements

The problem description states that *The transmitter should be optimized for speed, supporting as many as possible of the defined screen resolutions in the HDMI 1.3 specification across a single digital link, while keeping cost and power to a minimum.*

Highest supported screen resolution

The HDMI 1.3 specification supports screen resolutions up to 2560x1600 (WQXGA) at a frame rate of 75 Hz, with 24-bit color resolution. The highest resolutions will demand a maximum system operation frequency of 3,4 GHz, a pixel rate of 336 Mpixel/sec and a single channel bandwidth of 3,4 Gbps, which is very high [23]. As the problem description states that the design should support the screen resolutions across a single

link, and the single link is able to handle 165 Mpixels/sec (ref section 2.5.3), the WQXGA-resolution is simply too high.

The common, highest supported resolution in televisions and computer screens is 1920x1080 progressive scan at varying frame rates. Another argument for limiting the highest screen resolution is that the design is to be implemented in a hand-held, battery-powered unit. The power-consumption, which is dependent on the maximum frequency, must therefore also be considered. As a result of this and the arguments in the specialization report [1], 1080p30 will be the highest supported screen resolution for this design. The design must therefore support a channel bandwidth of 742,5 Mbps (ref table 2.1).

Color Space

The HDMI protocol supports many color spaces. Choosing one over another will, however, have little impact on the efficiency and speed of the transmission. As an ultimate goal, the transmitter should be able to support all the six different color spaces mentioned in chapter 2.4.2. As a minimum it should support RGB, as it is the most common coding used in computer monitors, and as it is a requirement in order to be DVI-compatible. Thus, the design will set RGB as the standard color space in this design.

Color Depth

The design will initially not support higher than 24-bit color depth. 48-bit will double the TMDS clock rate, and thereby approximately double the power consumption (ref 2.4.2). Though a higher color depth will improve the picture quality to some extent, it is not enough to compensate for the increased power consumption.

Time domain crossing mechanisms

As the transmitter operates at two different clock frequencies (ref section 2.1.2) the design will need a synchronizer in order to secure proper transfer of data when performing time domain crossing. A synchronizer module will prevent problems regarding metastability, which may occur due to the different clock frequencies (ref section 3.6). This will further result in the need of a First In - First Out (FIFO) queue, that will handle the temporary storage of encoded data. One clock cycle of the slowest time domain (the domain running on the TMDS-clock) will hereafter also be referred to as a *slow cycle*, while one cycle of the faster domain will be referred to as a *fast cycle*.

4.3 Priorities

The HDMI-protocol is too extensive and complex to explore fully within the given time-frame of this study. The problem description also states that the student is to focus on the Transition-Minimized Differential Signaling part of the protocol. The first stage of the design phase will be to achieve a functional design that meets the basic requirements, meaning a reliable basic transmitter that is able to transmit data using the correct encoding, with no special regard to the transmission speed. The second stage will be to explore solutions that enhances the design.

First priority - Speed

The enhancement process shall focus especially on the throughput speed, by implementing different hardware design techniques presented in the previous chapter. This should be the main priority, as this directly reflects the ability to display the highest screen resolutions, and the minimum screen resolution shall be 1080p30.

Second priority - Power

The second priority will be to make the system as power-efficient as possible by implementing hardware design techniques from chapter 3. This is also a high priority, as the power consumption is crucial for the possibility of implementing this in a mobile, hand-held application. Though speed will be the number one priority, the design will initially be synthesized using a 180nm, low-leakage library, as this will have a significant positive effect on the power consumption.

Third priority - Area cost

There will be put some effort into reducing the area cost, to the extent of trying to avoid unnecessary use of space, which also to some extent reflects the static power dissipation (ref section 3.1.1). If a trade-off between performance, power and area cost arises, the latter will lose unless the gain of the first or the second priority is very small compared to an extensive increase in area cost.

Fourth priority - DFT

Design for testing is very important for every manufacturer of digital circuits, as this may find and eliminate bugs and errors in both prototypes and finished products. However, in the scope of this study, this will not be a high priority. SCAN-logic will be added by the synthesis tool, as it improves the accuracy and quality of the timing and power-reports. The Test Coverage (TC) will be sought to be kept as high as possible, but not on the expense of the above mentioned priorities. BIST will not be implemented in the design at this stage.

4.4 Design Tools

The designs will be divided into separate modules and the RTL code will be written in Verilog. The RTL code will be verified using Synopsys Verilog Compiler (VCS) and Synopsys Discovery Visualization Enviroment (DVE), where suitable, self-made test-benches provide the appropriate inputs. Further, Spyglass will be used to perform lint-checking, which assists in discovering and eliminating suspicious constructs. Design Compiler will be used to perform the synthesis, while Encounter will provide the design layouts. PrimeTime will be used to perform the Static Timing Analysis (STA) as well as the power estimation. Finally, net-list verification will be conducted using VCS and DVE again.

4.5 Specification overview

Hardware requirements	
Highest supported screen resolution	1080p30
Highest TMDS-channel bandwidth	742,5 Mbps
Time domain clock ratio (slow:fast)	1:10
Highest clock-frequency - Fast Domain	742,5 MHz
Highest clock-frequency - Slow Domain	74,25 MHz
Color Space	RGB
Color Depth	24-bit
Design Priorities	
Priority 1	Speed
Priority 2	Power
Priority 3	Area Cost
Priority 4	DFT
Design Tools	
RTL Verification	VCS/DVE
Lint Checking	Spyglass
Synthesis	Design Compiler
Layout	Encounter
Static Timing Analysis	PrimeTime
Netlist Verification	VCS/DVE
Power Estimation	PrimeTime

Table 4.1: Specification overview

5

Design Implementation

This chapter contains the details of the work that has been performed on the design, and covers the general design flow, the basic design stage and the enhanced design stage. The general design flow section contains information on the RTL-code, how the designs are verified, how the synthesis-reports are generated and how to read the results. The basic design stage contains detailed information on how the different modules are interconnected and made, and also the reason why they are designed this way. The enhanced design stage section involves a small discussion related to which enhancement-techniques should be applied in order to improve the basic design, details from the enhancement-process and comments on how the applied techniques affects the design.

5.1 Design Flow

All modules have been written in Verilog and the code of both the basic and the enhanced design are gathered in the *HDMIattachments.zip*-file attached to the report (see Appendix H for the zip-file's table of contents). Note that data and signal names used in the figures and comments of this chapter is preceded by *hdmi_<modulename>* in the actual Verilog-code, but this is left out in some of the following chapters to improve the overview.

The modules were individually tested, using specially constructed test benches for each of them. An initial division of the test benches and modules into smaller units simplified the development, as it was easier to handle one challenge at a time. When all the modules had been individually tested, they were linked together in a top-module to form a complete system.

5.2 Basic Design Stage

The section contains information on the first design stage of the HDMI-transmitter. This stage focus on establishing a straight-forward, basic, reliable and functional design. First the suggested original proposed architecture from the specialization project is presented, covering the general operation of the system. Following this is the current basic design, explaining how and why the design is divided into modules. Further, this will be put together in an abstract summary of how the design works. Each module is then sequentially presented in detail, including its functionality and the dependency to other modules. The TMDS-, FIFO- and Serializer-modules is explored before the synchronizer-module is presented, as the synchronizer acts as the interface between the others.

5.2.1 Original proposed architecture

As already mentioned, the problem description states that the focus will be on the implementation of the TMDS-part of the HDMI protocol, and figure 5.1 shows the original proposal of the system architecture from the specialization project report [1].

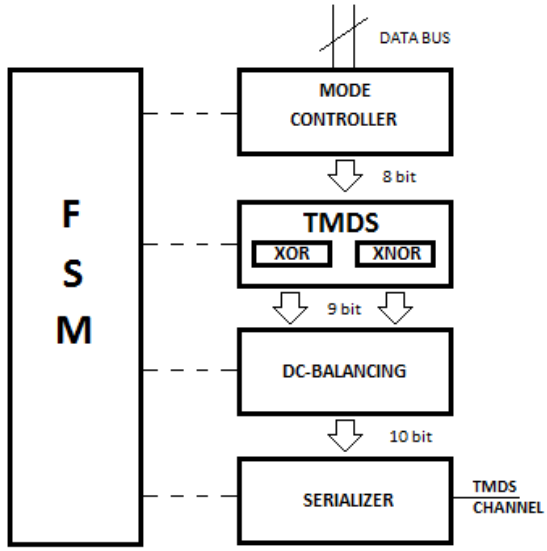


Figure 5.1: Original proposed architecture [1].

There are some issues with the original proposed architecture, and changes have been made to improve the design. The basic design is divided into several modules, in order to gain better perspective, simplify the enhancement process and facilitate the possibility of using different enhancement techniques for different parts of the design. The mode-controller in figure 5.1 will not be implemented at this stage, due to the

scope of the problem description and the constraints listed in section 4.1. The original modules handling the transition-minimizing and the DC-balancing was merged, and incorporated in a single module called TMDS. The serializer will be designed as the independent module proposed in figure 5.1. The proposed Finite State Machine (FSM) is discarded, as it will be more efficient to incorporate individual state-machines in the respective modules (if and where they are needed).

Due to Time Domain Crossing issues (ref chapter 3.6), the design needs synchronization between the slow and the fast clock domain. In order to simplify the try-out of different synchronizers, a independent synchronizer-module is added to the design. A FIFO-module is also introduced due to the delays introduced by the synchronization.

5.2.2 Modules

The modules are dependent on data and signals from either external units and/or the other modules. Figure 5.2 shows how signals and data are interconnected between the modules.

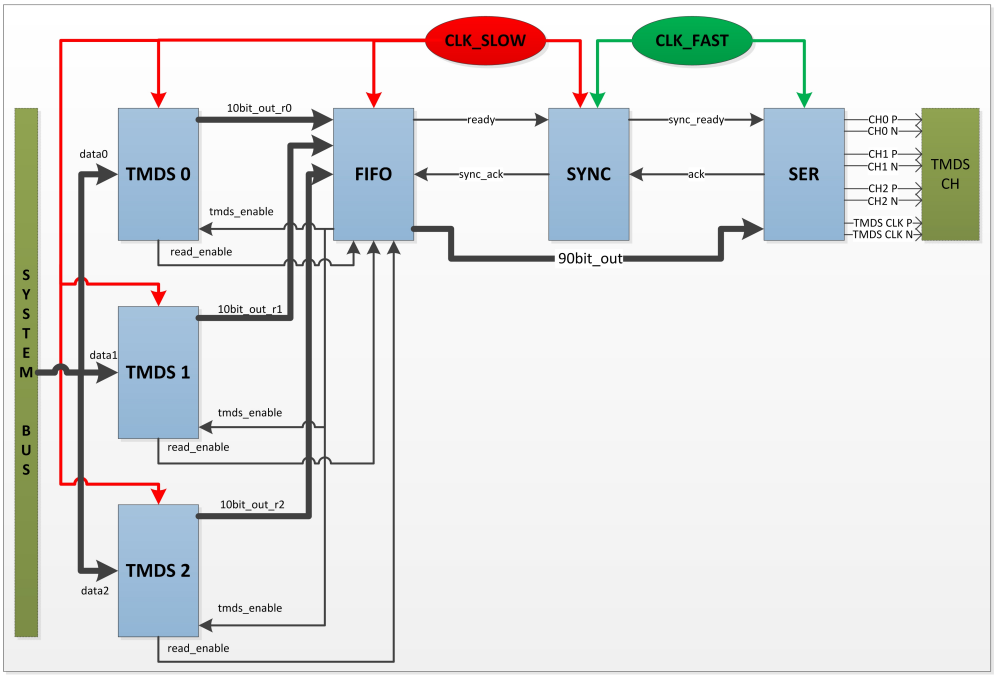


Figure 5.2: Signal and data interconnections.

The design will start loading data and control signals from the system data bus and the mode-controller (they are not part of the design, but are simulated by the test-benches in the top-module). There is one TMDS-module for each of the TMDS-channels, which separately encodes the data using TMDS-encoding. When all the

TMDS-modules have new encoded data on the output, they activate a *read_enable* signal, which enables the FIFO to read and store the data in a FIFO-queue. When the queue is sufficiently filled up, new data is combined in 90-bit packages at the output, and the FIFO signals through the synchronizer to the serializer, that new data is available. When the serializer has read the new data, it signals the FIFO, through the synchronizer, that it is ready for another set of data. In parallel, it continuously converts the data to three serial outputs using a 93-bit shift-register.

5.2.3 TMDS-module

The TMDS-module incorporates the TMDS algorithm described in section 2.3, thereby ensuring that video and audio data is both transition-minimized and dc-balanced. The TMDS-module layout in figure 5.3 shows how the module operates in three pipelined stages/steps, providing a set of 10-bit TMDS-encoded data every slow clock cycle. Section 3.4 states that pipelining can be used effectively when the algorithm is applied repeatedly to a stream of input data. The delay caused by the pipelined stages are in addition irrelevant for this application, and pipelining is therefore applied to the TMDS-module. Also note that the TMDS-module is replicated, and there is one module for each of the three TMDS-channels.

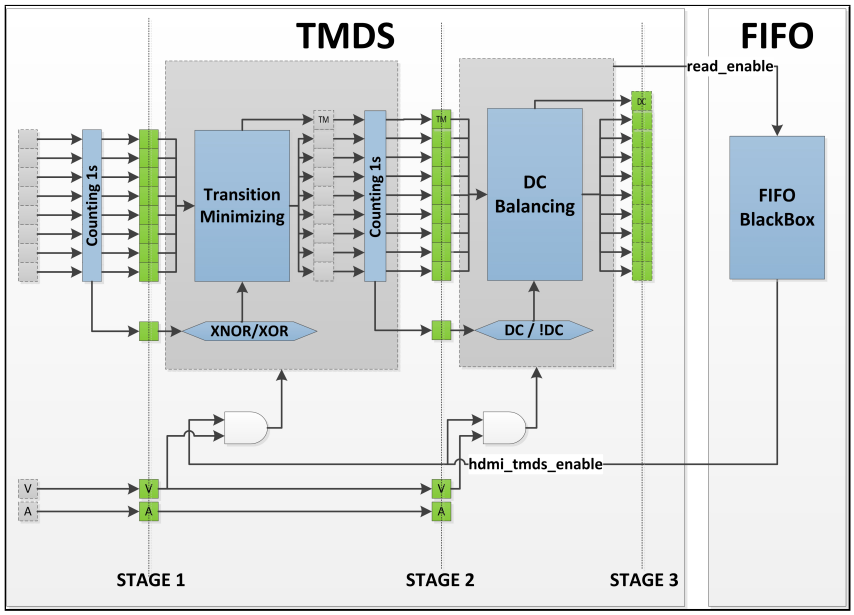


Figure 5.3: TMDS architecture.

Figure 5.3 shows that a combinatorial circuit counts the number of ones in the data input every time the input data from the system bus is changed.

Stage 1

At *Stage 1*, the input data is read along with the number of ones from the counter. Depending on how many ones there are in the 8-bit input data, it chooses to either XOR or XNOR the data in the transition minimizing process. When the transition-minimizing is done, the number of ones in the 9-bit output is counted, so that the result can be used in the next stage.

Stage 2

In *Stage 2* the number of ones is compared to an internal counter, which keeps track of the total number of ones and zeros that have been transmitted thus far. This is done by keeping track of a positive or negative deviation. Depending on the composition of the 9-bit output from the previous stage, the output will be inverted. This is done if the original content of the output will increase the imbalance tracked by the internal counter.

Stage 3

In the third and final step, the finished 10-bit transition-minimized and dc-balanced data is set on the output, together with a read-enable-signal to the FIFO, saying that new data is ready to be sent to the serializer.

5.2.4 FIFO

FIFO is an acronym for First In - First Out, and it is an abstraction related to ways of organizing and manipulate data in regard of time and priority. It is a queue processing technique, where data leaves the queue in the order it arrived. The FIFO operates at a clock frequency that is approximately 10 times slower than the frequency of the serializer. To ensure that the FIFO is always able to provide continuous data to the Serializer, it must run just a little bit faster than a tenth of the serializer-speed (ref section 2.1.2 and 4.2).

The required size of the FIFO-queue is determined by the number of slow clock cycles the synchronizer needs in order to ensure synchronized and secure transfer of data to the fast clock domain (the serializer). For every slow clock cycle the synchronizer is delayed, 3x10 bit data is encoded by the three TMDS-modules, and the 30 bits must be added to the FIFO-queue. If the FIFO-queue is not constructed as a sufficiently large buffer, important data will be lost.

The FIFO disables the preceding TMDS-modules when the FIFO-queue is almost full. This is done so that the TMDS-modules shall not produce encoded data when the FIFO is not ready to receive it. In much the same way the FIFO also re-enables the TMDS-modules when more data has been moved to the serializer (thereby freeing space in the FIFO-queue). The data transfer between the TMDS-modules and the FIFO is coordinated using the *read_enable*-signal, and the disabling and enabling of the TMDS-modules are controlled using the *tmds_enable*-signal.

Figure 5.4 presents an example of how the signals work, and how they relate to the counter that tracks how full the queue is.

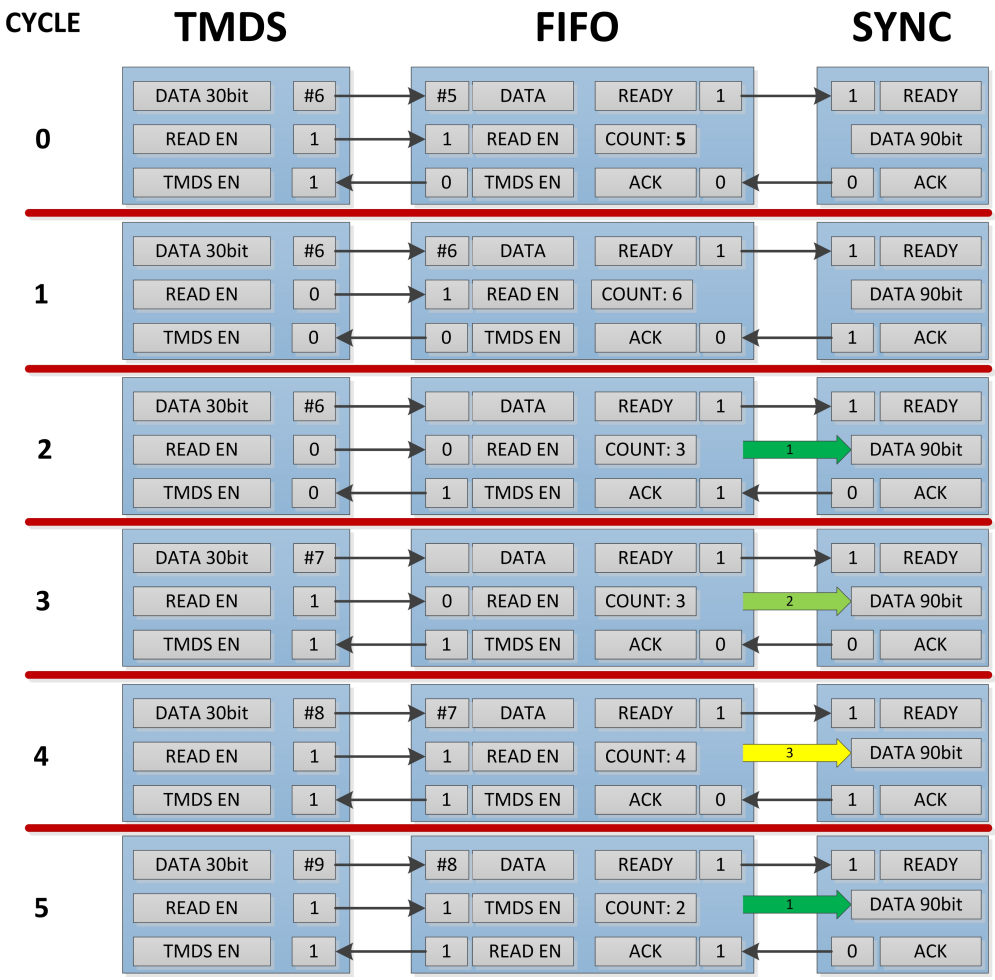


Figure 5.4: Synchronizing the TMDS-modules and the FIFO-module.

Figure 5.4 also shows that the FIFO relates to the synchronizer. When the FIFO detects the *sync_ack*-signal from the synchronizer, this is an indication that the previous transfer of data to the serializer went well, and a new set of data can be set at the output. The *ready*-signal passes through the synchronizer, and informs the serializer that there is data available. The signal will be set high as soon as the FIFO-queue contains sufficient amounts of data to perform a complete transfer to the serializer. It will not be pulled low until HDMI-transfer is complete, or unless the TMDS-modules is not able to provide sufficient data fast enough. This is the main reason why the

slow clock domain must have a clock frequency which is slightly higher than a tenth of the one in the fast clock domain (ref section 4.2). The FIFO-queue will always set the oldest data on the output, ensuring a sequential transfer of data.

5.2.5 Serializer

The serializer-module is located in the fast clock domain, and it performs the high-speed parallel-to-serial conversion. It also handles the differential signaling part of the TMDS-protocol (ref section 2.5.2).

The FIFO transfer data to the serializer, using the *90bit_out* data-bus (see figure 5.2). The size of the parallel data that is moved at each transfer is determined by the number of clock cycles the synchronizer needs to perform a safe transfer (ref section 5.2.4). The synchronizer uses three slow clock cycles for each data-transfer (this will be elaborated in section 5.2.6). The serializer must be able to send 3x10bit for every time the TMDS-modules complete a set of encoded data, in other words it must be able to serialize ten bits per TMDS-channel for every slow clock cycle. The width of the bus connecting the FIFO and the serializer, and the corresponding size of parallel data to be transferred on the bus is thus calculated as stated in equation 5.1.

$$Buswidth = 3\ slow\_clock\_cycle \cdot \frac{3 \cdot 10bit}{slow\_clock\_cycle} = 90bit \tag{5.1}$$

As long as the *ready*-signal from the FIFO is held high, the serializer will continuously load 90 bit of parallel data every 30 fast clock cycles. The serializer-module has a counter that is increased by one every fast clock cycle, and it controls the loading of the data. As illustrated in figure 5.5, at start-up and every time the counter reaches 29, the serializer will start the loading-procedure.

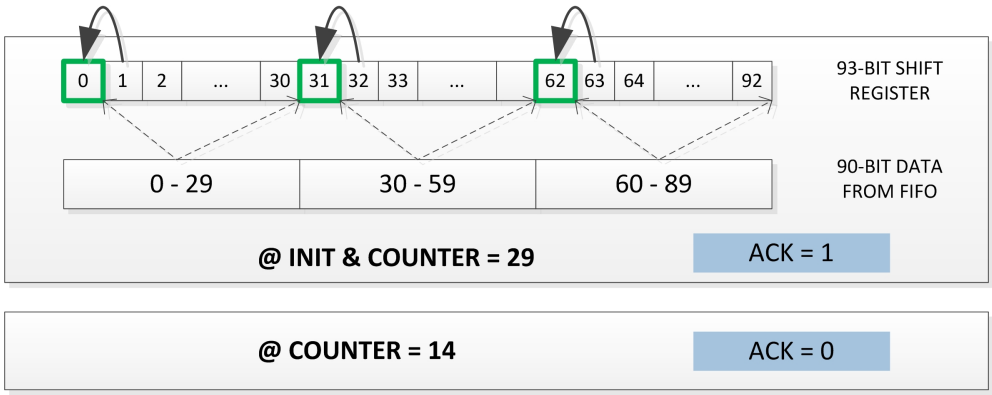


Figure 5.5: Serializer shift-counter and synchronization.

First, the remaining three bits that has not yet been shifted out is instead copied to their respective channel-buffers. A channel-buffer is a one-bit part of the shift-register, where the bit-value is set on a TMDS-channel (see figure 5.6).

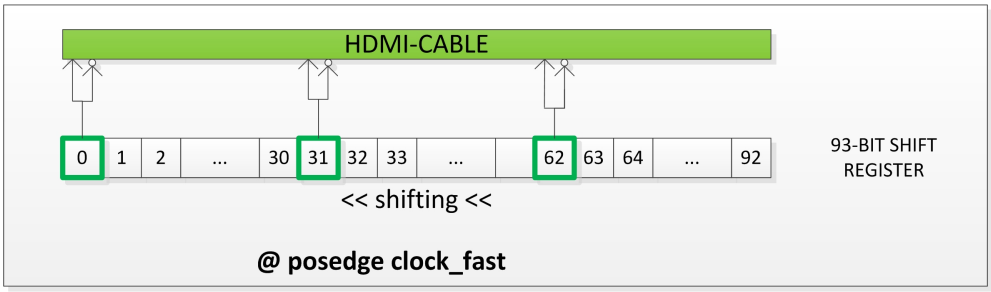


Figure 5.6: Serializer shift-register.

Second, the *90bit_out* parallel data is divided in three parts, and added to the shift-register in between the channel-buffers. Next the counter is reset, and the shift-register will continue to shift 3 bits to the channel-buffers every fast clock cycle. The *acknowledge*-signal from the serializer is set high each time new data has been loaded from the FIFO. The synchronizer-module uses this signal to generate a slow clock-cycle pulse on the receiving end (the FIFO). Figure 5.7 is part of a waveform showing how the *acknowledge*-signal is set high when data is loaded, and pulled low when the counter is half-way between two loading sessions.

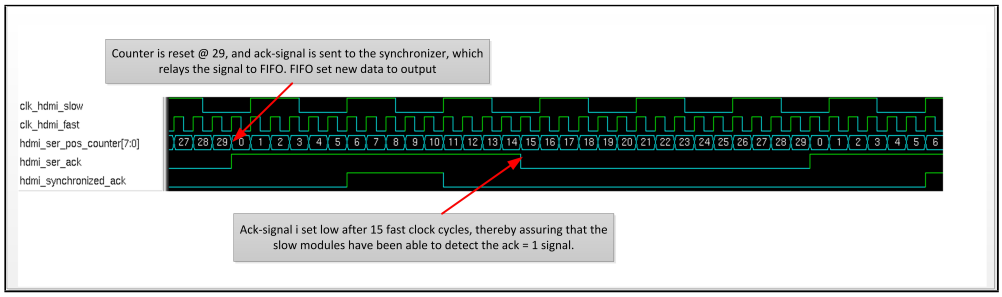


Figure 5.7: Waveform: Acknowledge and serializer-counter relation.

The counter is also used to control the TMDS-clock signal (ref section 2.1.2). For every five fast clock cycles, the TMDS-clock channel outputs are inverted, thus producing the TMDS-clock signal used by a HDMI-receiver to synchronize the transfers.

5.2.6 Synchronizer

A synchronizer-module is needed to handle the time domain crossing between the fast clock domain of the serializer-module and the slower clock domain of the TMDS- and FIFO-modules (ref section 3.6).

To improve the overview, and to simplify the testing of several different kinds of synchronizers, the mechanism is placed within an independent module. Several synchronizers are considered and evaluated. Two factors are key when choosing the best suited synchronizer; It needs to be fast, and it must be designed in such a way, that it keeps the FIFO-queue as small as possible while still maintaining synchronicity.

The implemented synchronizer is a custom made pulse synchronizer and works as detailed in figure 5.8.

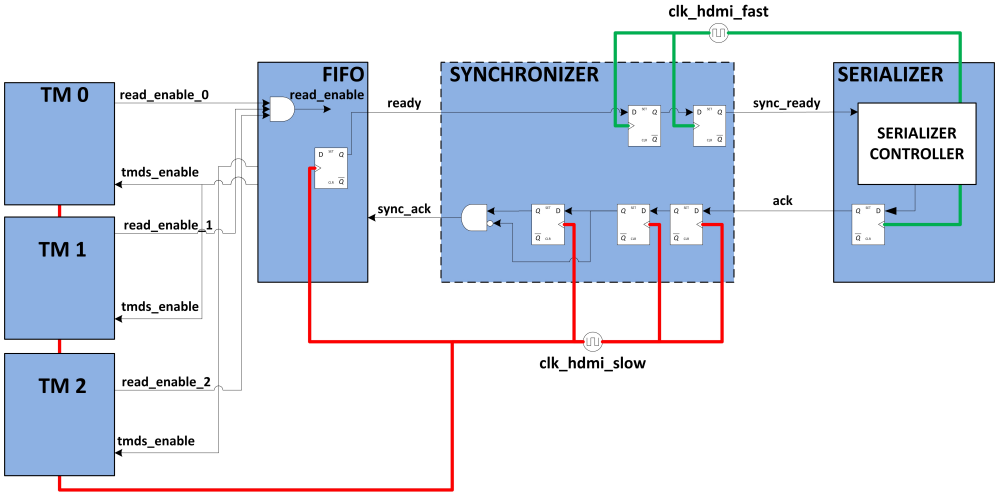


Figure 5.8: Synchronizer architecture.

The serializer must alternate the value of the *acknowledge*-signal in order for the flip-flops of the synchronizer to generate a pulse (the *sync_ack*-signal in figure 5.8), which tells the FIFO that the serializer has read the previous data successfully.

The flip-flops in the synchronizer causes the *acknowledge*-signal from the serializer to be delayed at most three slow clock cycles. The delay through the two flip-flops running on the fast clock, which is handling the *sync_ready*-signal synchronization, is significantly smaller. Three slow clock cycles is therefore the longest delay caused by the synchronizer, and this is directly influencing the size of the FIFO-queue (ref section 5.2.4).

5.2.7 Preliminary Results

Table 6.1 in section 6.1 shows the results from the basic design stage. The preliminary results states that the Basic Design is able to support low HD-resolutions like e.g. 480p60 and 576p50. The highest channel bit-rate supported by the design, is approximately 330 Mbps. This is less than half of the goal of 742,5 Mbps, which is needed to support the 1080p30-resolution (ref section 4.1).

The timing reports show that the timing issues are located in the fast clock-domain, where the serializer-logic is too slow. Because of this, the focus of the enhanced design-stage is to improve the speed of the serializer, as this is the system bottleneck in regard of speed and performance.

5.3 Enhanced Design Stage

The main problem of the basic design, is that the synthesis reports show that it does not meet timing when synthesizing for 1080p30 (742,5 MHz). Different improvement hypothesis will be discussed, and the procedures regarding the implementation of the best solutions will be presented.

5.3.1 Improvement hypothesis discussion

Different solutions for enhancing the design are evaluated, implemented and analyzed in order to find the best way to enhance the design sufficiently, so that it meets the specification listed in section 4.5. This is a discussion regarding how to best proceed in order to reach the goal. The discussion includes determining the focus area, the effects of technology scaling and attribute tweaking, and the options regarding changing the counters of the serializer-module. There is also an own segment on the possibilities of optimizing the counters in the serializer, as the synthesis reports state that this is the first bottleneck of the basic design.

5.3.1.1 Focus Areas

Enhancement of the modules in the slow clock domain will not be explored initially. The timing-reports show that they are nowhere close to experience timing violations at the maximum frequency of the basic design, which is approximately 30MHz for the modules of the slow clock domain. If the serializer is improved sufficiently in order to meet the timing-demands at 752,5 MHz, while on the other hand the slow time domain modules suffer from timing violations, options for enhancing the slow clock domain will be explored.

5.3.1.2 Technology

Scaling the technology (ref section 3.5), in other words changing the synthesis library, would be a simple way of increasing the speed. Optimizing for speed is the main priority, however, the 180nm low-leakage library is very power efficient, and replacing it with a faster high-leakage library will cause a significantly higher static power consumption. This is not a beneficial trade, and the library will not be changed until it is absolutely necessary.

5.3.1.3 Attribute tweaking

The Design Compiler operates based on a variation of attributes that has impact on how the actual synthesis is performed. The attributes state to which extent a certain technique or factor should be weighed in, and how priorities should be settled in case of a trade-off during the optimization process. They can be changed in the synthesis-scripts, and examples of different attributes can be found in the *constraints.tcl*-file in Appendix I.

5.3.1.4 Counter optimization

The timing-report provided by the synthesis-tool, stated that the worst bottleneck in regards of performance, was the counters in the serializer within the fast clock domain. They needed to be modified in order to increase the clock-frequency sufficiently to support the 1080p30 mode. As the counter was too slow, different options were explored in order to find the best course of optimization. The options included clock gated-, pipelined-, ripple- and ring counters (see references [21] and [6] for more information). As the different counters have different benefits and disadvantages, a large effort was put into comparing them.

5.3.2 Enhanced Design Process

The process of enhancing the basic design is a complex task, and it involves a lot of planning, drafting, testing and rewriting of RTL code and scripts. In this case, where the goal is to make a faster design, the synthesis-tool provides helpful timing-reports. Timing-reports show the critical timing path, which is the slowest path in the current design (an example of a timing-report can be viewed in Appendix J). The report shows a detailed representation of how much time each of the gates in the path consumes. This information indicates where the worst timing-issues (often called bottlenecks) are located in the design, and these areas must be changed in order to improve the design further.

As a problem or bottleneck is improved, a new critical timing path will arise, as there will always be a path that is slower than the others. The process must be repeated until the design meets the required timing. The detailed effects of the different enhancements techniques will be presented in the Results-chapter. The first challenge of the basic design involves the counters of the serializer-module.

5.3.2.1 Counter enhancement

The basic design incorporates a straightforward 8-bit counter (called *hdmi_ser_pos_counter* in the Verilog-code), and the counter is used to keep track of when to load new data, and when to pull the *acknowledge*-signal to the synchronizer high and low. The timing-reports state that the counter in the serializer-module is too slow, as it is in the basic design. The highlighted lines in figure 5.9 shows that at 300 MHz, the *hdmi_ser_pos_counter*-register uses 0,63 ns of the total cycle of 3,33 ns.

Point	Fanout	Trans	Incr	Path
clock clk_hdmi_fast (rise edge)			0.00	0.00
clock network delay (ideal)			0.00	0.00
U_HDMI_SER/hdmi_ser_pos_counter_reg_6_/cp (sdcrq1rol7)		0.00	0.00	0.00 r
U_HDMI_SER/hdmi_ser_pos_counter_reg_6_/q (sdcrq1rol7)		0.17	0.63	0.63 f
U_HDMI_SER/hdmi_ser_pos_counter[6] (net)	3		0.00	0.63 f
U_HDMI_SER/U69/z (or03d1l7)		0.24	0.48 *	1.11 f
U_HDMI_SER/n85 (net)	3		0.00	1.11 f
U_HDMI_SER/U127/zn (nr02d0l7)		0.22	0.18 *	1.30 r
U_HDMI_SER/n1 (net)	1		0.00	1.30 r
U_HDMI_SER/U255/z (bufbd1l7)		0.37	0.35 *	1.65 r
U_HDMI_SER/n2 (net)	5		0.00	1.65 r

Figure 5.9: Segment of timing report from basic design at 300MHz.

As mentioned in section 5.3.1.4, there are several other ways of implementing a counter. Based on exploration and analysis, the ring counter was chosen, as it is the most effective for the enhanced design. A ring counter is in fact a shift-register, where the value that is shifted out is also shifted back in again in the other end of the register. The size (number of bits) of the register decides how far it counts. Note that one of the bit-values in the register must contain the opposite value of the others in order for the ring counter to work (e.g. 1000 or 0111 for a 4-bit ring counter). This is a very fast counter, as the only operation within a clock cycle is to shift the bits in parallel from one register to another [21].

As the single shift-operation is the only operation needed within a clock cycle, the counter is extremely fast. The ring counters are implemented in the design as two shift-registers, controlling the *acknowledge*-signal and the TMDS-clock, and they are respectively fifteen and five bits large. At startup and reset, the shift-registers are initiated with one as the value in the MSB, and zeros are distributed among the remaining space of the registers. Figure 5.10 is an excerpt of the code for the enhanced serializer, and shows how the bits of the shift-registers are continuously shifted around in a ring.

```
hdmi_ser_pos_counter[14:0] <=
          {hdmi_ser_pos_counter[0], hdmi_ser_pos_counter[14:1]};
hdmi_ser_tmds_counter[4:0] <=
          {hdmi_ser_tmds_counter[0], hdmi_ser_tmds_counter[4:1]};
```

Figure 5.10: Ring counter shifting.

The ring counters improves the enhanced design significantly, and new timing-reports state that the next challenge must be to change the RTL-structure and reduce the decision tree depth of the serializer.

5.3.2.2 Reducing the depth of the decision tree

The timing reports showed that after implementing the ring counter, the next task would have to be an pruning of the decision tree depth in the serializer. The decision tree depth is an abstract definition of the maximum number of sequential *if*-statements which are executed within a single clock cycle. As the design needs to be very fast, there is a very limited number of operations that can take place within a clock cycle, and the multiple sequential *if*-statements from the code structure of the basic design lead to a timing violation. The problem is solved by applying pipelining (ref section 3.4), and spreading the *if*-statements over several clock cycles. This requires more registers in order to save the temporary results between each clock cycle. This adds to the area cost, but it increases the operation speed. Figure 5.11 shows a random example of how it is possible to achieve the same result by changing three sequential *if*-statements within a clock cycle, to three consecutive statements spread over three clock cycles.

No pipelining - High tree depth

```
if A :
    if AB:
        if ABC:
            <DO SOMETHING COMPLEX>
```

Pipelined - Low tree depth

```
if A:    <DO SOMETHING SIMPLE>
         B = TRUE
else:    B = FALSE

if B:    <DO SOMETHING SIMPLE>
         C = TRUE
else:    C = FALSE

if C:    <DO SOMETHING COMPLEX>
else:    <DO NOTHING>
```

Figure 5.11: Pipelining the decicion tree.

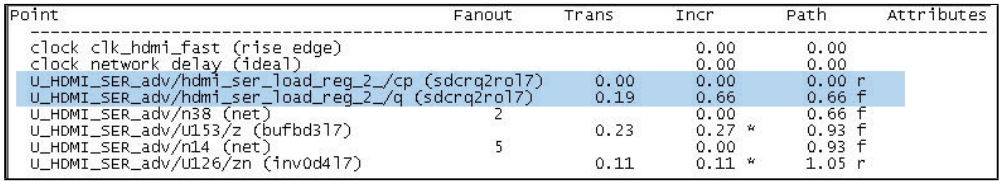
By reducing the depth of the decision three in the serializer, this adds to the reduction of the critical timing path. The ring counters combined with a pipelined decision three greatly improves the design, but there are still some challenges to solve. The next challenge is to explore the way the synthesis tool performs register replication.

5.3.2.3 Attribute tweaking

The counter and structure of the serializer from the basic design is changed in order to improved the performance of the transmitter. Though a significant improvement, the ring counter still does not improve the enhanced design enough, and it is necessary to start the process of tweaking the attributes of Design Compiler (the synthesis tool).

The tweaking is done by repeatedly changing attributes in the synthesis tool, before performing synthesis and analysis of the timing-reports. Examples of the attributes that may be tweaked, is found in Appendix I.

Figure 5.12 is an excerpt of a timing-report after the counters have been changed, and the highlighted area states that there is a problem with the delays through the *hdmi_ser_load*-registers.



Point	Fanout	Trans	Incr	Path	Attributes
clock clk_hdmi_fast (rise edge)			0.00	0.00	
clock network delay (ideal)			0.00	0.00	
U_HDMI_SER_adv/hdmi_ser_load_reg_2_/cp (sdcrq2rol7)		0.00	0.00	0.00 r	
U_HDMI_SER_adv/hdmi_ser_load_reg_2_/q (sdcrq2rol7)		0.19	0.66	0.66 f	
U_HDMI_SER_adv/n38 (net)	2		0.00	0.66 f	
U_HDMI_SER_adv/U153/z (bufbd3l7)		0.23	0.27 *	0.93 f	
U_HDMI_SER_adv/n14 (net)	5		0.00	0.93 f	
U_HDMI_SER_adv/U126/zn (inv0d4l7)		0.11	0.11 *	1.05 r	

Figure 5.12: Excerpt of timing-report.

The problem with the registers are related to the way the synthesis tool handles the fanout while optimizing the design. The fanout of a logic gate is the number of gate inputs to which it is connected, and the technology used in this design allows for a certain number of gate inputs to be wired directly together without additional circuitry like buffers. The maximum fanout of an output is directly related to the load-driving capability. The positive effect of a large fanout, is that it is area cost effective. On the other hand, each additional gate input will increase the capacitance, resulting in longer transition times and an increased power consumption. It is however difficult to predict the impact the fanout has on the timing, as the synthesis tool is to some extent unpredictable in itself in regard to the fanout optimization. The synthesis tool may insert a buffer in order to reduce the maximum capacitance if the maximum capacitance is too high and the timing is satisfactory. The added buffer may improve or aggravate the timing, depending on where the synthesis tool choose to insert the buffer.

The design suffered timing violations, as the synthesis tool had problems finding an effective optimization of the large 93-bit shift-register (see figure 5.6). In order to facilitate the conditions for the synthesis tool, the 93-bit shift-register was split into three 31-bit shift-registers, and a large effort was put into rewriting the entire serializer-module. Splitting up the shift-register reduced the maximum capacitance in the critical timing path, and enabled the synthesis tool to better optimize the design. This had a beneficial effect on the enhancement. In addition to splitting up the shift-register, the design was slightly enhanced by restricting the fanout as well. Figure 5.13 shows the script command that restricts the fanout of registers that has a name that starts with *hdmi_ser_load*, as these were the registers causing the highest delay.

```
set_register_replication -max_fanout 5 -num_copies 10   ->
        ->      [get_cells -h * -f {@name =~ *hdmi_ser_load*}]
```

Figure 5.13: Tweaking the register replication attribute.

The command makes sure that the fanout is not larger than five and that there will be no more than ten copies. Further it states that the rule shall only be applied to registers with *hdmi_ser_load* as part of the name. Though the fanout optimizations turns out to be beneficial for the design, it still needs some small changes before it is able to deliver according to the specification. The next step and final enhancement step involves removing the SCAN-logic from the serializer.

5.3.2.4 Removing SCAN-logic from serializer

After applying all the above changes to the serializer, the timing reports showed that the final bottleneck is caused by the SCAN-logic registers that is automatically inserted by Design Compiler in order to increase the Test Coverage. However, though replacing normal registers with SCAN-registers improves the Test Coverage, it also increases the the critical timing path and the area cost of the design (ref section 3.7.1).

In the case of the enhanced design, where speed is the absolute top priority, the last resort before changing the technology is to remove the SCAN-logic from the serializer. This is done by changing the *set_scan_element*-attribute of the Design Compiler. The lines in figure 5.14 was added to the synthesis script.

```
################ DISABLING SCAN IN SERIALIZER ################
set_scan_element false U_HDMI_SER_adv/hdmi_ser_ch0_data_reg[*]
set_scan_element false U_HDMI_SER_adv/hdmi_ser_ch1_data_reg[*]
set_scan_element false U_HDMI_SER_adv/hdmi_ser_ch2_data_reg[*]
set_scan_element false U_HDMI_SER_adv/hdmi_ser*
##############################################################
```

Figure 5.14: Commands to remove SCAN-logic from the serializer.

Initially, only the SCAN-logic of the three 31-bit shift-registers on the output was removed. Though this had a beneficial effect, ultimately the SCAN-logic of all the registers in the serializer had to be removed before the timing finally was met.

6

Results

This chapter presents the results from the synthesis-reports of both the basic design and the enhanced design. The synthesis reports are produced by a tool called Design Compiler. The different clock-frequencies used for synthesis are based on screen resolutions that are relevant for a hand-held application, and they are found in table 2.1. In addition to the comparison of the results from both the basic and the enhanced design, there are results that details the effect the SCAN-logic removal and the fanout-restrictions have on the design. There are also results related to alternative clock-ratios between the slow and the fast clock domain.

6.1 Basic Results

The results of the basic design synthesis are based on the synthesis-reports found in Appendix B, and the results are listed in table 6.1. The columns are read as following; *Mbps* is the required channel bit-rate for the current resolution. *CC (ns)* is the corresponding clock cycle in nano-seconds. The *TIMING* column states if the current design meets the timing requirements or not, while *Verified* states if simulation of the test-bench on the net-list is satisfactory. The *AREA* and *PWR* columns are respectively the area cost given as the number of NAND2-gate-equivalents (consisting of four unit-sized transistors) and the power consumption is given in mW. *TC (%)* is the test coverage of the current design. Blocks containing a star, has no valid data availiable, typically when the design does not meet the timing requirement.

Resolution	Mbps	CC (ns)	TIMING	Verified	AREA	PWR	TC (%)
480p60	252	3,968	OK	Yes	7882,5	5,94	99,63
576p50	270	3,704	OK	Yes	7923,5	6,20	99,63
720p24	590	1,69	NO	*	*	*	*
720p50	742,5	1,347	NO	*	*	*	*
1080p24	742,5	1,347	NO	*	*	*	*
1080p30	742,5	1,347	NO	*	*	*	*
1080p50	1485	0,67	NO	*	*	*	*

Table 6.1: Performance results from basic-design

The results of table 6.1 are from the basic design, which has SCAN-logic incorporated in all modules, and no fanout restrictions are applied to the synthesis.

6.2 Enhanced Design Results

The best achieved results of the enhanced design synthesis, for all the relevant resolutions, are based on the synthesis-reports found in Appendix C. The results are listed in table 6.2. The columns are read as described in section 6.1.

Resolution	Mbps	CC (ns)	TIMING	Verified	Area	PWR	TC (%)
480p60	252	3,968	Y	Y	5964,5	3,47	84,41
576p50	270	3,704	Y	Y	5939,0	3,49	84,41
720p24	590	1,695	Y	Y	5961,5	6,96	84,41
720p50	742,5	1,347	Y	Y	6078,0	13,6	84,41
1080p24	742,5	1,347	Y	Y	6078,0	13,6	84,41
1080p30	742,5	1,347	Y	Y	6078,0	13,6	84,41
1080p50	1485	0,673	N	*	*	*	*

Table 6.2: Enhanced Design Results

The results in table 6.2 are from the enhanced design, where several changes have been made compared to the basic design. The counters of the serializer are changed, the decision tree depth is reduced, the 93-bit shift-register of the output is divided into three smaller ones, the SCAN-logic of the serializer is removed, and restrictions have been applied to the fanout-attribute of the synthesis tool.

6.3 Basic and Enhanced Design Comparison

Table 6.3 compares the results from the basic and enhanced design. The columns are read as described in section 6.1, but with the added *R*-column that states the improvement ratio.

			B	E	R	B	E	R
Resolution	**Mbps**	**CC (ns)**	**Area actual**			**Power Actual**		
480p60	252	3,968	7882,0	5934,5	0,753	5,94	3,47	0,58
576p50	270	3,704	7923,5	5939,0	0,750	6,20	3,49	0,56
720p24	590	1,695	*	5961,5	*	*	6,96	*
720p50	742,5	1,347	*	6078,0	*	*	13,6	*
1080p24	742,5	1,347	*	6078,0	*	*	13,6	*
1080p30	742,5	1,347	*	6078,0	*	*	13,6	*
1080p50	1485	0,673	*	*	*	*	*	*

Table 6.3: Basic and Enhanced design comparison

6.4 Exploratory Results

This section contains results detailing the effect of removing SCAN-logic, how much impact restrictions on the fanout and register replication has on the synthesis, and the effects of changing the ratio between the slow and the fast clock domain.

6.4.1 Comparison of SCAN-logic and Register replication

Table 6.4 shows how SCAN-logic and restrictions on fanout affects the size and speed of the design, as discussed in section 5.13 and 5.3.2.4. The results are based on synthesis reports generated from the enhanced design, at the stage where the counters are changed, the decision three depth is reduced and the 93-bits shift-register is divided into three smaller ones.

RESTR. FANOUT	SCAN-logic	AREA	SLACK (ns)	TIMING INCREASE
Y	N	6078,00	0	0
Y	Y	6164,75	-0,25	18,6%
N	N	6019,25	-0,27	20,7%
N	Y	6092,75	-0,42	31,2%

Table 6.4: SCAN-logic and fan-out comparison

The results of the comparison in table 6.4 are achieved by alternating the SCAN-logic and fanout-attribute on the last and most effective version of the enhanced design.

6.4.2 Changing clock domain ratios

Some experimenting was done, where the speed relation between the fast- and the slow clock domain was changed. Table 6.5 shows how the area cost and power consumption changes if the slow clock domain clock is increased from being a tenth of the maximum fast clock domain frequency, to an eight and a quarter of the fastest frequency.

Table 6.5: Other fast/slow clock domain ratios

	1:10	**1:8**	**1:4**
SLACK - Slow Domain (ns)	4,91	2,26	0
AREA COST	6078	6071,5	6352
POWER (mW)	13,6	13,6	13,7

All the results are based on 742,5 MHz being the fast clock domain frequency, and the synthesis has been run on the enhanced design. The *SLACK*-row states how much time there is to spare on the critical timing paths.

6.5 Verification

The functionality of the design was verified using a test bench for the top-module, and simulated using VCS. While running the test-benches on the net-lists, DVE-waveforms were used to check the verification.

The waveform produced when running the test bench on the complete system (*hdmi_top_module.v*) can be viewed in figure 8.1 in Appendix E. Figure 8.2 in Appendix F displays the same content as figure 8.1, but the detail-level is higher, showing the fast clock edges.

7

Discussion

This chapter contains a discussion of the results and the techniques that have been applied during the implementation process. The achievements and reliability of the designs are discussed first, followed by suggestions on what needs to be explored in the future work.

7.1 Results

The basic design was made in order to create a foundation, of which the enhanced design could be compared against. This section will focus on the overall improvement of the enhanced design compared to the basic design, and how well the enhanced design performs compared to the requirements of the specification.

7.1.1 Basic vs Enhanced design

There is a problem when comparing the results of a given screen resolution in the basic and the enhanced design. The problem is that only the frequencies of 480p60 and 576p50 met the timing in the basic design. Developing a design that is able to handle 1080p30 was the main goal of the system specification in section 4.3. This is achieved by the enhanced design, but as there are no valid data from the corresponding resolution in the basic design, it is hard to make an accurate comparison. However, the comparison of 480p60 and 576p50 for both the basic and the enhanced design shows that in the enhanced design the power consumption is reduced by more than 40% and the area cost by almost 25% for both resolutions. The other resolutions supported by the enhanced design shows a relatively consistent area cost. The power consumtion increases as the operation frequency is increased, and this is to be expected with an increased activity factor (ref equation 3.2). Though there is no data to support the comparison of the highest resolution, it is assumed that the reduction of the power consumption and the area cost that is seen for 480p60 and 576p50 is also applicable to the higher resolutions. In other words, it is assumed that the enhancement techniques in the enhanced design have had just as significant impact on all the screen resolutions.

7.1.2 Achievements vs Problem Description

The enhanced design performs in accordance with the specification overview in section 4.5. The design fulfills the requirements of the HDMI-standard, and is able to transfer data over a single link at a rate compatible with the the 1080p30 resolution (742,5 MHz). Though the design does not support all the possible defined screen resolutions of version 1.3 of the HDMI-specification, it does support the most relevant resolutions (ref section 4.2).

7.1.3 Speed and Power consumption

Achieving a functional design, that is able to deliver 1080p30 using a 180nm, low-leakage library, is very satisfactory. As a result of not changing the library, and thereby avoiding using transistors with a significant higher power consumption, the design is made in accordance with not only the main priority (speed), but the second priority as well (power consumption). The power consumption of the system is 13,6 mW, and the enhanced design compared to the basic design has an average reduction of the power consumption of approximately 40 %. The significant improvement must be largely credited to the changes made to the counters (ref section 5.3.2.1). In addition, the splitting of the large shift-register (ref section 5.13) and the general re-structuring of the RTL-code for the enhanced design made it easier for the synthesis tool to enforce its optimization.

7.1.4 Area Cost

The enhanced design area cost of 6087,25 NAND2 equivalents corresponds to approximately 24.000 unit-sized transistors. This accounts for a reduction of approximately 25% compared to the basic design. As there are no other known sources of comparison, and since the area cost is listed as the third priority in section 4.5, the result must be deemed to be satisfactory. Most of the reduction is a direct result of the changes made to the counters and the rewriting of the RTL code. This we can derive from table 6.4, where we can see that removing the SCAN-logic and restricting the fanout has little effect on the area cost.

7.1.5 Design for testing

The Design For Test is listed as the fourth priority in the specification, and it is a little disappointing that the SCAN-logic had to be removed in order to increase the speed of the enhanced design sufficiently to achieve the 1080p30 resolution (ref section 5.3.2.4). This reduced the Test Coverage from 99,63% to 84,41%, as there is no SCAN-logic in the serializer-module. However, a functional test on the output of the serializer will show whether or not the module is working properly. A functional test would exploit the simple nature of the serializer, as the parallel input data shall be exactly the same as the output data, with the exception that the output data is serialized. As the the removal of the SCAN-logic in the serializer benefits the design, and simple functional

tests can be constructed in order to counteract the reduced Test Coverage, the reduced Test Coverage is seen as an accceptable tradeoff.

7.1.6 Reliability

It is important to discuss the reliability of the results, and to what extent they can be trusted. As the transmitter is designed for ASIC, we rely on the synthesis reports to provide the needed results.

7.1.6.1 Basic vs Enhanced design

It is easy to assume that the basic design was made unnecessary simple, so as to produce better results for the enhanced design. This is however not the case, and a lot of time and effort was put into making the original design reliable and efficient. Many of the performance enhancing techniques that are presented in the hardware design chapter is implemented in the basic design, such as pipelining and parallelization of the TMDS-modules.

7.1.6.2 Corner Cases

Corner cases are simulated variations of temperature and voltages, and they are applied to the synthesis tools as they affect the transition times of the transistors in the library. In the case of the synthesis done on these design, they have all been performed using the worst-case corners. As no chip is available for testing, we will have to assume that the synthesis reports provide us with reliable estimations in regard to timing, area cost and power consumption. The estimations are based on reliable tools and the libraries used for the synthesis are very good.

7.1.6.3 Synthesis report variations

Two synthesis reports, based on the exact same RTL-code and constraints, yield slightly different results. There is a theory that this is caused by random heuristics in the synthesis process, but there are no official sources supporting the theory, as this concerns the inner workings of the Synopsys Design Compiler. The variations are however very small, and the ones that have been observed have been less than 1%.

7.1.6.4 Library

The 180 nm low-leakage library that is used for the synthesis is developed by Atmel, and have been used for several applications that have been put into production. The data within the library is highly reliable and have been verified on several occasions. This adds to the reliability of the estimations of the design.

7.2 Future work

Though the enhanced design is working in accordance with the problem description, there are still several area that can be explored in order to improve the design. New ideas on how to improve the design has surfaced as the work on the thesis has progressed. There is a lot to be done in order to explore how much the modules of the slow clock domain can be enhanced, and changing the ratio between the slow and the fast clock domain should be explored to see its effect on the performance. The exploration is time-consuming, ant there is not enough time to complete the task at this stage. This will have to be included in the future work.

7.2.1 Enhancing the slow domain

The main effort has been put into achieving the desired resolution of 1080p30. The focus of the design enhancement has therefore been on meeting the timing-requirements, by improving the serializer in the fast clock domain. This has resulted in a relative power-efficient, high-speed system. However, further improvement of the modules in the slow clock domain should be explored, as this will reduce the total power consumption.

7.2.2 Standalone HDMI-transmitter

The focus of this study has been on the TMDS-part of a HDMI-transmitter, and the specification chapter states that constraints shall exclude the surrounding control logic and the data-buses needed to complete a standalone HDMI-transmitter (ref section 4.1). The design should, however, be expanded in order to become a fully operational, standalone HDMI-transmitter. This possibility should be explored after the design is optimized.

7.2.3 FPGA-implementation

The possibility of testing the enhanced design on an FPGA was considered, as at-speed testing in hardware is desirable. The high frequency of this design is, however, a problem. 742,5 MHz is a very high frequency for FPGA-operation. If a FPGA was found capable of handling this high frequency, the RTL-code would still have to be rewritten in order to exploit the typical built-in functionality of the FPGA. Ultimately, the FPGA-implementation was discarded, as there was not enough time to perform this task. In addition, large amounts of time spent on implementing it would most likely yield little relevant information at this stage in the design process. It is however recommended that an FPGA-implementation is explored after the surrounding control-logic and data-buses have been implemented.

7.2.4 Changing the synchronizer

As already mentioned, the synchronizer and FIFO accounts for a large portion of the area cost and the power consumption of the design. The final enhanced design was also synthesized using other ratios between the fast and the slow clock domain than the standard 1:10 ratio, and the results tell us that there is practically no significant difference between 1:10, 1:8 and 1:4. The reason the different ratios was explored was that there is a possibility that these results can be used to build a different synchronizing mechanism. One theory is that based on a fixed operation frequency and a clock divider, there is a possibility that the synchronization can be simplified and the size of the FIFO can be significantly reduced.

8

Conclusion

The design is completed in accordance with the prerequisites of the problem description. It meets the specifications listed in section 4.5. The TMDS-part of the HDMI-transmitter is able to provide a serial data-flow of 742,5 Mbps per channel, which is sufficient for providing the HD-resolution of 1080p30. The power consumption of the enhanced design was reduced by approximately 40% compared to the basic design, and the enhanced design consumes approximately 13,6 mW. The area cost of the final enhanced design was reduced by 25%, and sums up to approximately 24.000 unit-size transistor equvialents.

The design demonstrates that it is possible to efficiently use a battery-powered, hand-held application as a source of High-Definition video and audio signals.

Future Work

In the continuation of this project, there are several tasks to complete:

- Enhance the slow clock domain.
- Expand the design to a standalone HDMI-transmitter.
- Explore a possible FPGA-implementation.
- Explore the possibility of changing the synchronizer.

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APPENDIX A

Spyglass Results Summary

```
-------------------------------------------------------------------------------------------
Results Summary:
-------------------------------------------------------------------------------------------
   Template/Goal Run  :      lint/sign_off
   Command-line read  :      0 error,      0 warning,      1 information message
   Design Read        :      0 error,      0 warning,      3 information messages
      Found 1 top module:
         hdmi_top_module   (file: ../../module/verilog/hdmi_top_module.v)

   Blackbox Resolution:      0 error,      0 warning,      0 information message
   SGDC Checks        :      0 error,      0 warning,      0 information message
   Policy latch       :      0 error,      0 warning,      1 information message
   Policy lint        :      0 error,      1 warning,      1 information message
   Policy morelint    :      0 error,      1 warning,      0 information message
   Policy erc         :      0 error,      0 warning,      0 information message
   ------------------------------------------------------------------------------------
   Total              :      0 error,      2 warnings,     6 information messages

  Total Number of Generated Messages     :        18 (0 error, 12 warnings, 6 Infos)
  Number of Waived Messages              :        10 (0 error, 10 warnings, 0 Info)
  Number of Reported Messages            :         8 (0 error, 2 warnings, 6 Infos)

-------------------------------------------------------------------------------------------
```

APPENDIX B

Basic Results for 480p60 (3,968ns)

```
  ---------------------------------------------------------------------------------------------
  data required time                                                                      3.51
  data arrival time                                                                      -3.48
  ---------------------------------------------------------------------------------------------
  slack (MET)                                                                             0.03

  ---------------------------------------------------------------------------------------------
  data required time                                                                     39.21
  data arrival time                                                                     -36.36
  ---------------------------------------------------------------------------------------------
  slack (MET)                                                                             2.85

Combinational area:       1884.500000
Noncombinational area:    5997.500000

Total cell area:          7882.000000
Total area:                 undefined

                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network           3.373e-03 1.307e-03 5.676e-10 4.680e-03 (78.75%)  i
register                7.112e-04 1.824e-04 4.096e-09 8.936e-04 (15.04%)
combinational           2.106e-04 1.586e-04 1.984e-09 3.692e-04 ( 6.21%)
sequential                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.648e-03   (27.73%)
  Cell Internal Power  = 4.295e-03   (72.27%)
  Cell Leakage Power   = 6.648e-09   ( 0.00%)
                         ---------
Total Power            = 5.943e-03  (100.00%)

X Transition Power     = 1.564e-06
Glitching Power        = 1.272e-06

Peak Power             = 6.481e-03
Peak Time              =      1000
```

Basic Results for 576p50 (3,703ns)

```
  ----------------------------------------------------------------------------------------
  data required time                                                              3.25
  data arrival time                                                              -3.11
  ----------------------------------------------------------------------------------------
  slack (MET)                                                                     0.14

  ----------------------------------------------------------------------------------------
  data required time                                                             36.56
  data arrival time                                                             -33.99
  ----------------------------------------------------------------------------------------
  slack (MET)                                                                     2.57

Combinational area:       1926.000000
Noncombinational area:    5997.500000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          7923.500000
Total area:                 undefined


                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network           3.471e-03 1.441e-03 5.917e-10 4.912e-03 (79.14%)  i
register                6.992e-04 1.882e-04 4.097e-09 8.874e-04 (14.30%)
combinational           2.432e-04 1.639e-04 2.036e-09 4.071e-04 ( 6.56%)
sequential                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.794e-03   (28.90%)
  Cell Internal Power  = 4.413e-03   (71.10%)
  Cell Leakage Power   = 6.724e-09   ( 0.00%)
                         ---------
Total Power            = 6.206e-03  (100.00%)

X Transition Power     = 5.330e-06
Glitching Power        = 1.437e-06

Peak Power             = 6.764e-03
Peak Time              =      1000
```

APPENDIX C

Enhanced Results for 480p60 (3,968ns)

```
  ----------------------------------------------------------------------------------------------
  data required time                                                                      1.98
  data arrival time                                                                      -0.60
  ----------------------------------------------------------------------------------------------
  slack (MET)                                                                             1.38

  ----------------------------------------------------------------------------------------------
  data required time                                                                     39.19
  data arrival time                                                                      -8.59
  ----------------------------------------------------------------------------------------------
  slack (MET)                                                                            30.60

Combinational area:       1700.000000
Noncombinational area:    4234.500000
Net Interconnect area:      undefined  (Wire load has zero net area)
Total cell area:          5934.500000
Total area:                 undefined

                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network           2.014e-03 6.422e-04 4.268e-10 2.656e-03 (76.46%)  i
register                4.669e-04 8.983e-05 2.978e-09 5.568e-04 (16.03%)
combinational           1.349e-04 1.136e-04 1.823e-09 2.485e-04 ( 7.16%)
sequential              1.173e-05 6.930e-07 1.157e-11 1.242e-05 ( 0.36%)

  Net Switching Power  = 8.464e-04   (24.37%)
  Cell Internal Power  = 2.627e-03   (75.63%)
  Cell Leakage Power   = 5.240e-09   ( 0.00%)
                         ---------
Total Power            = 3.474e-03  (100.00%)

X Transition Power     = 2.177e-06
Glitching Power        = 1.613e-06

Peak Power             = 3.613e-03
Peak Time              =      1000
```

Enhanced Results for 576p50 (3,703ns)

```
  ------------------------------------------------------------------------------------------
  data required time                                                                  1.85
  data arrival time                                                                  -0.60
  ------------------------------------------------------------------------------------------
  slack (MET)                                                                         1.25


  ------------------------------------------------------------------------------------------
  data required time                                                                 36.55
  data arrival time                                                                  -8.44
  ------------------------------------------------------------------------------------------
  slack (MET)                                                                        28.11

Combinational area:       1704.500000
Noncombinational area:    4234.500000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          5939.000000
Total area:                 undefined

                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network           2.024e-03 6.320e-04 4.117e-10 2.656e-03 (76.05%)  i
register                4.727e-04 8.986e-05 2.978e-09 5.625e-04 (16.11%)
combinational           1.397e-04 1.216e-04 1.836e-09 2.613e-04 ( 7.48%)
sequential              1.175e-05 5.941e-07 1.157e-11 1.234e-05 ( 0.35%)

  Net Switching Power  = 8.441e-04   (24.17%)
  Cell Internal Power  = 2.648e-03   (75.83%)
  Cell Leakage Power   = 5.237e-09   ( 0.00%)
                         ---------
Total Power            = 3.492e-03  (100.00%)

X Transition Power     =    0.0000
Glitching Power        = 2.241e-06

Peak Power             = 3.639e-03
Peak Time              =      1000
```

Enhanced Results for 720p24 (1,695ns)

```
  ----------------------------------------------------------------------------------------
  data required time                                                              1.45
  data arrival time                                                              -1.45
  ----------------------------------------------------------------------------------------
  slack (MET)                                                                     0.00


  ----------------------------------------------------------------------------------------
  data required time                                                             16.45
  data arrival time                                                              -8.53
  ----------------------------------------------------------------------------------------
  slack (MET)                                                                     7.92

Combinational area:       1690.000000
Noncombinational area:    4271.500000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          5961.500000
Total area:                 undefined

                         Internal  Switching  Leakage    Total
Power Group              Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                      0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network            3.935e-03 1.367e-03 4.151e-10 5.303e-03 (76.24%)  i
register                 9.503e-04 2.033e-04 2.980e-09 1.154e-03 (16.59%)
combinational            2.536e-04 2.211e-04 1.992e-09 4.746e-04 ( 6.82%)
sequential               2.348e-05 1.237e-06 1.157e-11 2.472e-05 ( 0.36%)

  Net Switching Power  = 1.793e-03   (25.78%)
  Cell Internal Power  = 5.163e-03   (74.22%)
  Cell Leakage Power   = 5.398e-09   ( 0.00%)
                         ---------
Total Power            = 6.956e-03  (100.00%)

X Transition Power     = 1.836e-06
Glitching Power        = 6.596e-06

Peak Power             = 7.044e-03
Peak Time              =      1000
```

Enhanced Results for 720p50 & 1080p24 & 1080p30 (1,347ns)

```
  ----------------------------------------------------------------------------
  data required time                                                      1.13
  data arrival time                                                      -1.13
  ----------------------------------------------------------------------------
  slack (MET)                                                                 0.00


  ----------------------------------------------------------------------------
  data required time                                                     12.99
  data arrival time                                                      -8.32
  ----------------------------------------------------------------------------
  slack (MET)                                                             4.67

Combinational area:       1886.000000
Noncombinational area:    4275.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          6078.000000
Total area:                 undefined


                     Internal  Switching  Leakage    Total
Power Group          Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box              0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network       7.803e-03 2.456e-03 4.412e-10    0.0103 (75.68%)  i
register            2.052e-03 3.734e-04 3.014e-09 2.425e-03 (17.89%)
combinational       5.071e-04 3.148e-04 1.939e-09 8.219e-04 ( 6.06%)
sequential          4.689e-05 2.819e-06 1.157e-11 4.971e-05 ( 0.37%)

  Net Switching Power  = 3.147e-03   (23.22%)
  Cell Internal Power  =    0.0104   (76.78%)
  Cell Leakage Power   = 5.405e-09   ( 0.00%)
                         ---------
Total Power            =    0.0136  (100.00%)

X Transition Power     = 5.080e-07
Glitching Power        = 5.794e-07

Peak Power             =    0.0133
Peak Time              =         0
```

APPENDIX D

Basic Test Coverage

fault class	code	#faults
Detected	DT	16334
Possibly detected	PT	0
Undetectable	UD	62
ATPG untestable	AU	60
Not detected	ND	0
total faults		16456
test coverage		99.63%

Enhanced Test Coverage

fault class	code	#faults
Detected	DT	11372
Possibly detected	PT	0
Undetectable	UD	27
ATPG untestable	AU	2101
Not detected	ND	0
total faults		13500
test coverage		84.41%

APPENDIX E

The waveform shows the data flow through the system, from parallel input at the TMDS-modules, to the serial-channel outputs from the serializer.

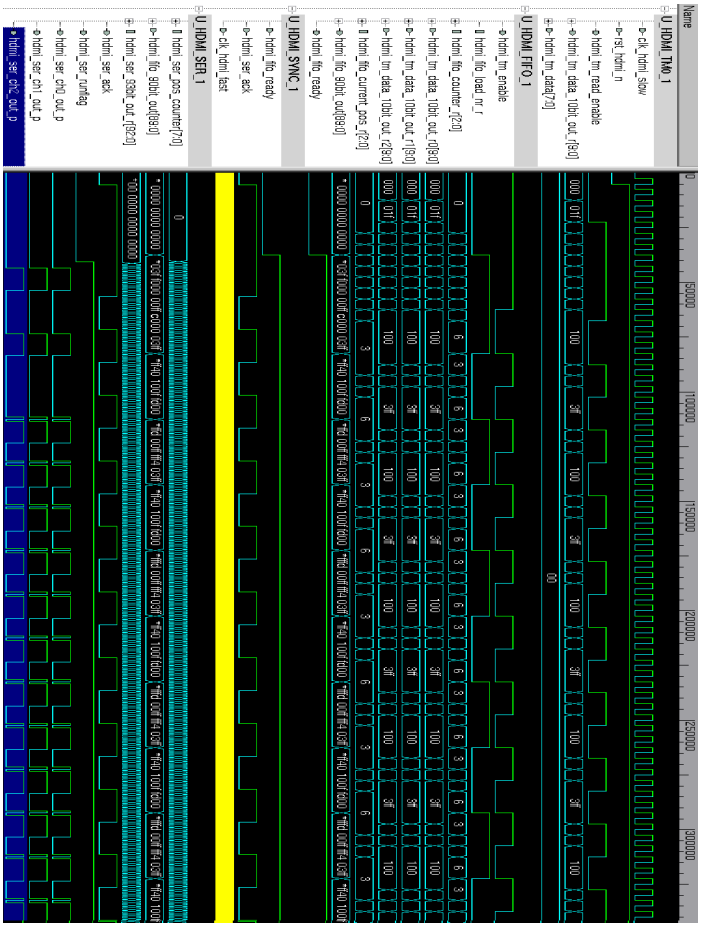

Figure 8.1: System functionality waveform.

APPENDIX F

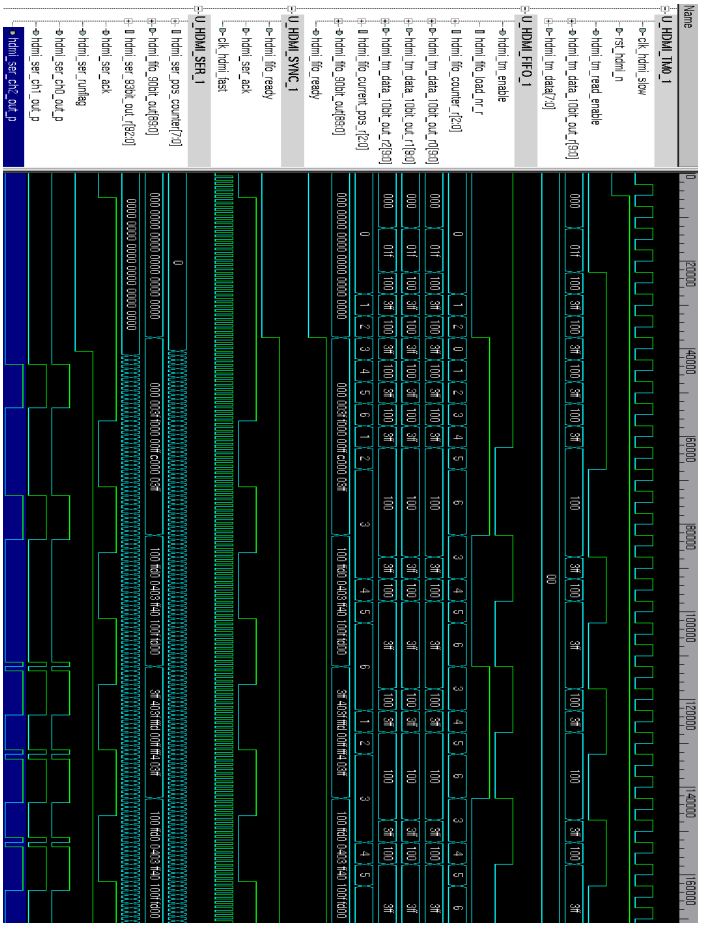

Figure 8.2: System functionality waveform (detailed).

APPENDIX G

Atmel Technology Confidentiality

The library-files used for the synthesis of the design are regulated by Atmel Technology Confidentiality agreements, and is not attached to this design. In addition, the scripting files are not attached.

APPENDIX H

Contents of *HDMIattachments.zip*

- Basic design
  - hdmi_fifo.v
  - hdmi_serializer.v
  - hdmi_sync.v
  - hdmi_tm.v
  - hdmi_top_module.v
- Enhanced design
  - hdmi_fifo.v
  - hdmi_serializer_adv.v
  - hdmi_sync.v
  - hdmi_tm.v
  - hdmi_top_module.v
- Testbench
  - tb.sv

APPENDIX I

constraints.tcl - Design Compiler scipt-file

```
#HDMI_TOP_MODULE clk period

#AHB clk period
set ahb_clk_hdmi_fast_period 1.3468
set ahb_clk_hdmi_slow_period 13.468

create_clock clk_hdmi_fast -period $ahb_clk_hdmi_fast_period
create_clock clk_hdmi_slow -period $ahb_clk_hdmi_slow_period

#Set driving cell for the clocks, this helps CTS build a reasonable tree
set_driving_cell -lib_cell ctprebuffl7 [get_ports {clk*}]

set_false_path -from clk_hdmi_fast -to clk_hdmi_slow
set_false_path -from clk_hdmi_slow -to clk_hdmi_fast


# Enable identification of shift registers to save area

#set compile_seqmap_identify_shift_registers true

set_register_replication -max_fanout 5 -num_copies 10 (cont. ->)
                (cont. ->) [get_cells -h * -f {@name =~ *hdmi_ser_load*}]

################ DISABLING SCAN IN SERIALIZER ################
set_scan_element false U_HDMI_SER_adv/hdmi_ser_ch0_data_reg[*]
set_scan_element false U_HDMI_SER_adv/hdmi_ser_ch1_data_reg[*]
set_scan_element false U_HDMI_SER_adv/hdmi_ser_ch2_data_reg[*]
set_scan_element false U_HDMI_SER_adv/hdmi_ser*
##############################################################

# Enable identification of shift registers to save area
# set compile_seqmap_identify_shift_registers true

#set compile_enable_register_merging false
#set_dont_touch loadsig

#should be put after first compile_ultra
#optimize_registers
#-clock cld_comain1 -edge rise -justification_effort high -delay_threshold ???
```

APPENDIX J

Timing report 300 MHz Basic Design)

```
Point                                          Fanout     Trans      Incr       Path      Attributes
-------------------------------------------------------------------------------------------------------
clock clk_hdmi_fast (rise edge)                                      0.00       0.00
clock network delay (ideal)                                          0.00       0.00
U_HDMI_SER/hdmi_ser_pos_counter_reg_6_/cp (sdcrq1rol7)  0.00         0.00       0.00 r
U_HDMI_SER/hdmi_ser_pos_counter_reg_6_/q (sdcrq1rol7)   0.17         0.63       0.63 f
U_HDMI_SER/hdmi_ser_pos_counter[6] (net)      3                      0.00       0.63 f
U_HDMI_SER/U69/z (or03d1l7)                             0.24         0.48 *     1.11 f
U_HDMI_SER/n85 (net)                          3                      0.00       1.11 f
U_HDMI_SER/U127/zn (nr02d0l7)                           0.22         0.18 *     1.30 r
U_HDMI_SER/n1 (net)                           1                      0.00       1.30 r
U_HDMI_SER/U255/z (bufbd1l7)                            0.37         0.35 *     1.65 r
U_HDMI_SER/n2 (net)                           5                      0.00       1.65 r
U_HDMI_SER/U251/z (buffd3l7)                            1.01         0.72 *     2.37 r
U_HDMI_SER/n5 (net)                          22                      0.00       2.37 r
U_HDMI_SER/U176/z (mx02d1l7)                            0.12         0.49 *     2.86 f
U_HDMI_SER/N75 (net)                          1                      0.00       2.86 f
U_HDMI_SER/hdmi_ser_93bit_out_r_reg_47_/d (sdcrq1rol7)  0.12         0.00 *     2.86 f
data arrival time                                                               2.86

clock clk_hdmi_fast (rise edge)                                      3.33       3.33
clock network delay (ideal)                                          0.00       3.33
U_HDMI_SER/hdmi_ser_93bit_out_r_reg_47_/cp (sdcrq1rol7)              0.00       3.33 r
library setup time                                                  -0.45       2.88
data required time                                                              2.88
-------------------------------------------------------------------------------------------------------
data required time                                                              2.88
data arrival time                                                              -2.86
-------------------------------------------------------------------------------------------------------
slack (MET)                                                                     0.02
```