NTNU

Det skapende universitet

NUTS Backplane

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Revision History

Revision	Comment
PA00	Initial Pre-Release Version
PA01	Fixed errors from initial review
A00	First Release Version

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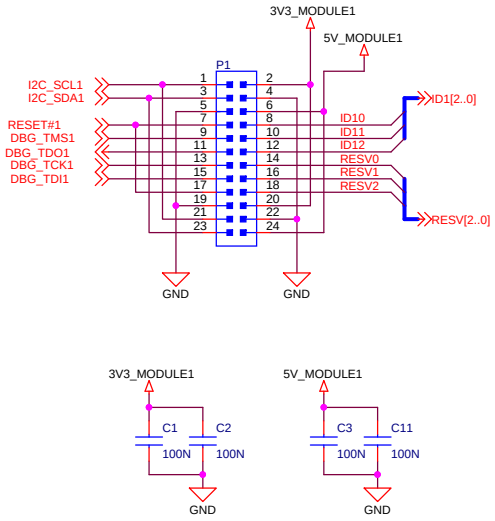
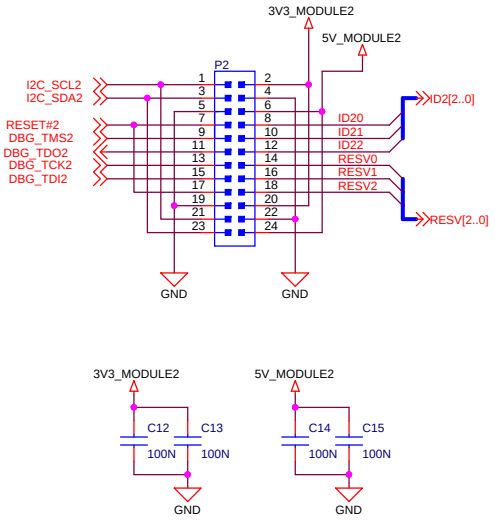
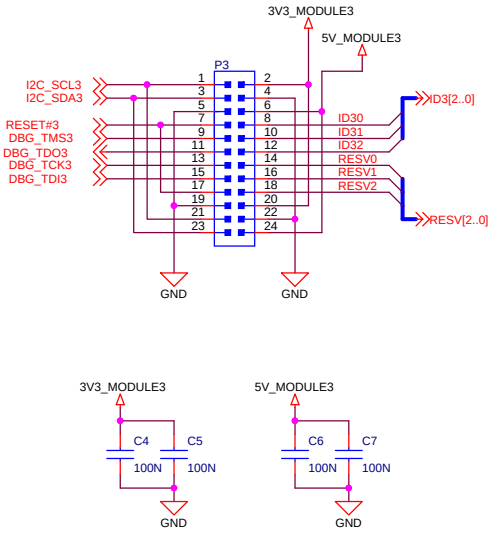
Module Connector 1



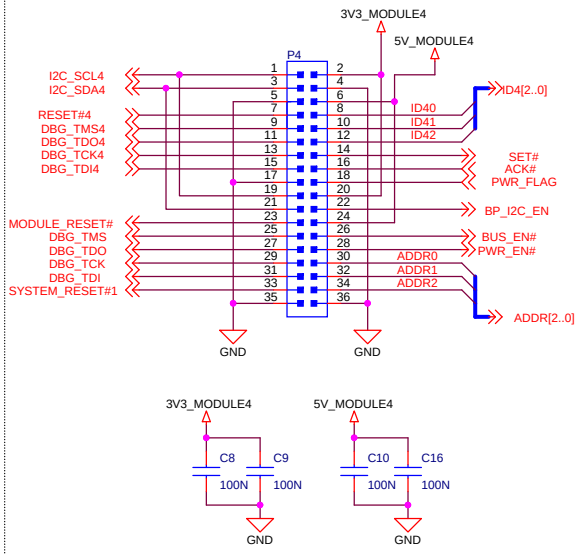
Module Connector 2



Module Connector 3

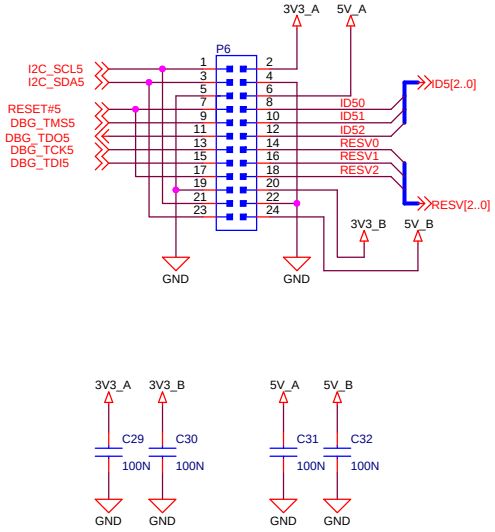


Module Connector 4
On Board Data Handling



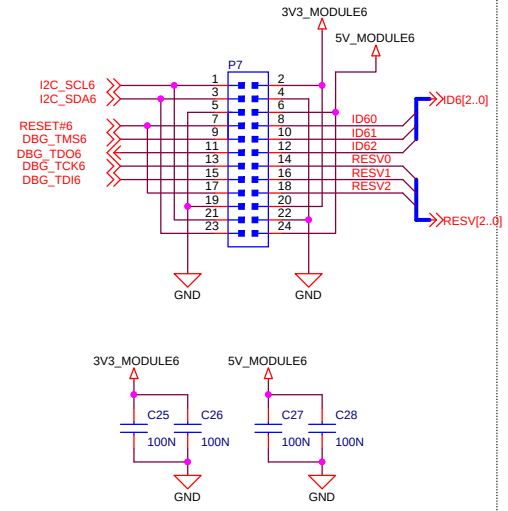
Module Connector 5

Electrical Power System

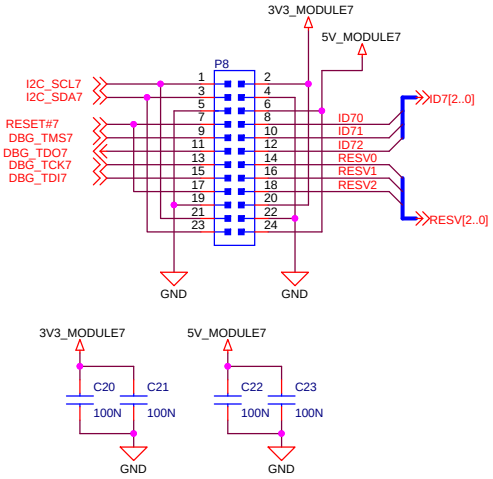


The EPS supplies the 3V3_A, 3V3_B, 5V_A and 5V_B rails. The module 5 power distribution circuit is used to provide protection to the backplane. Module 5 power cannot be turned off.

Module Connector 6



Module Connector 7



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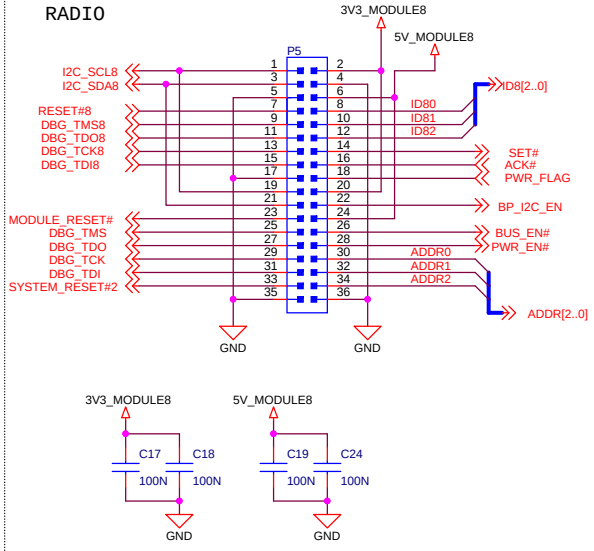
TOP

Module Connector 8

RADIO



	Schematic Title: **NUTS Backplane**	
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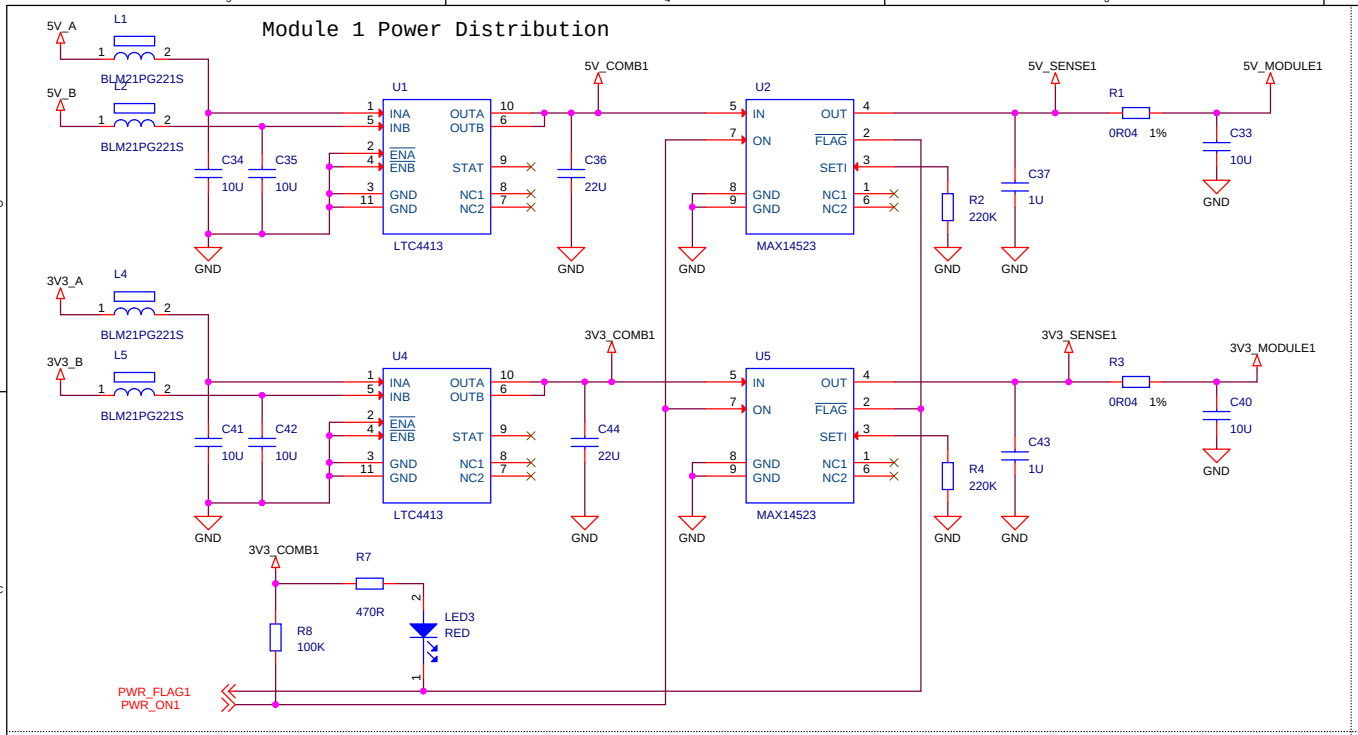

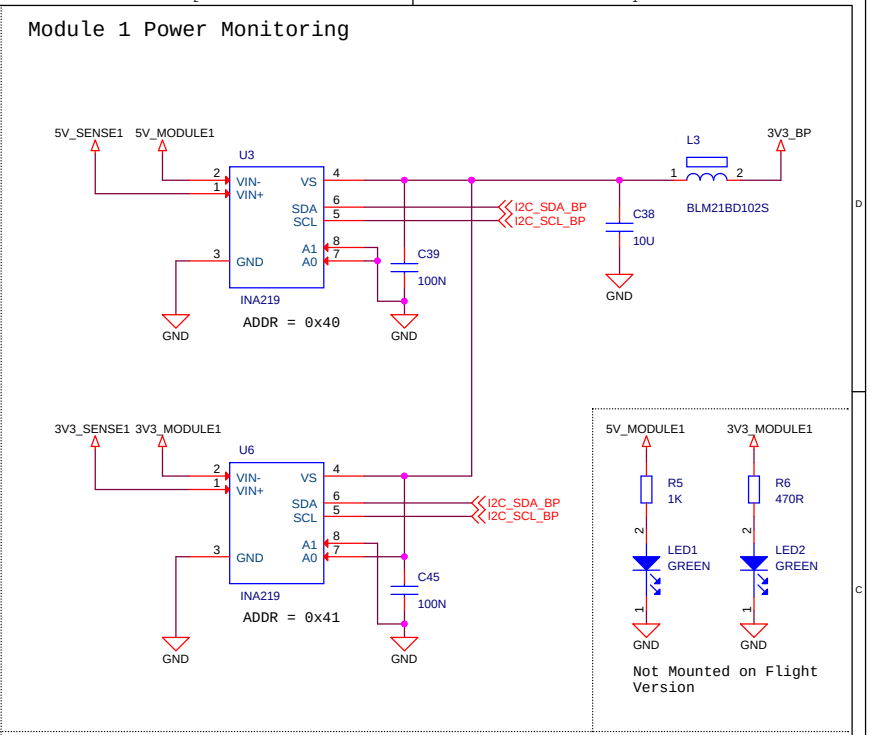

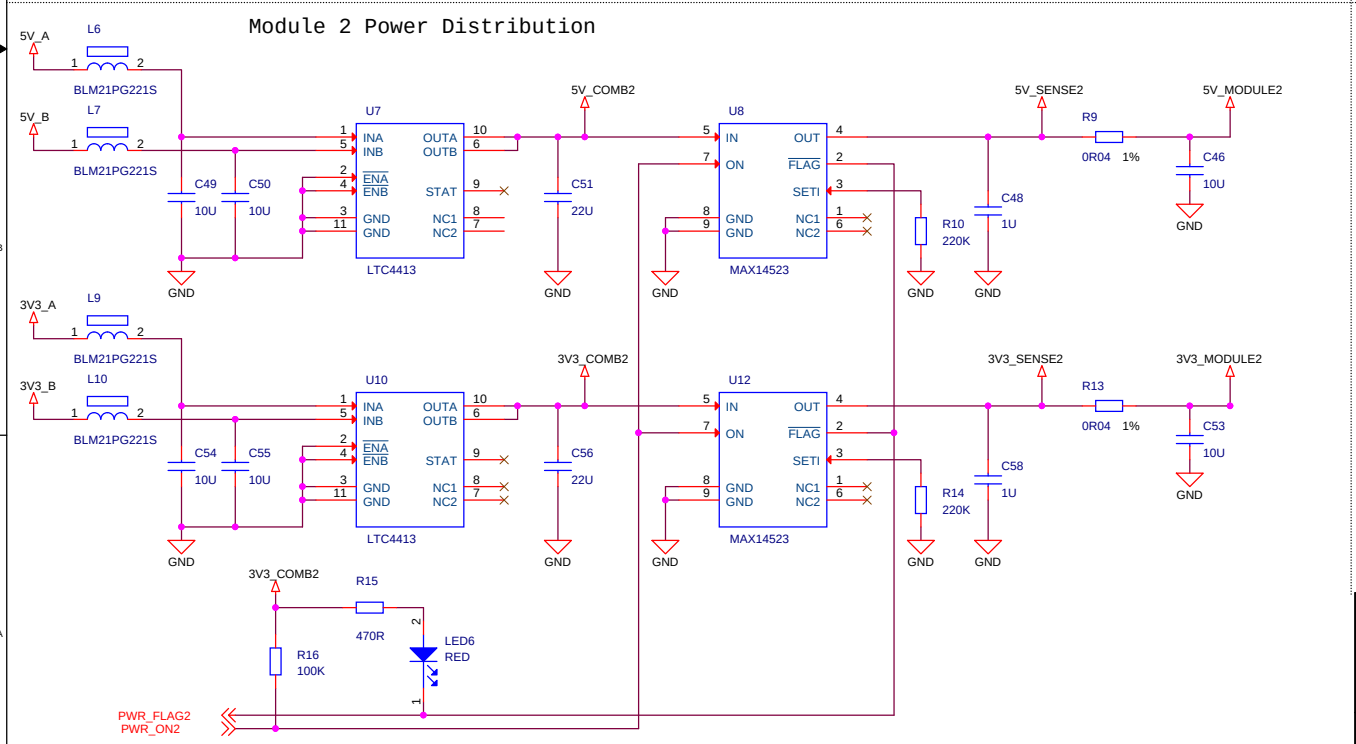

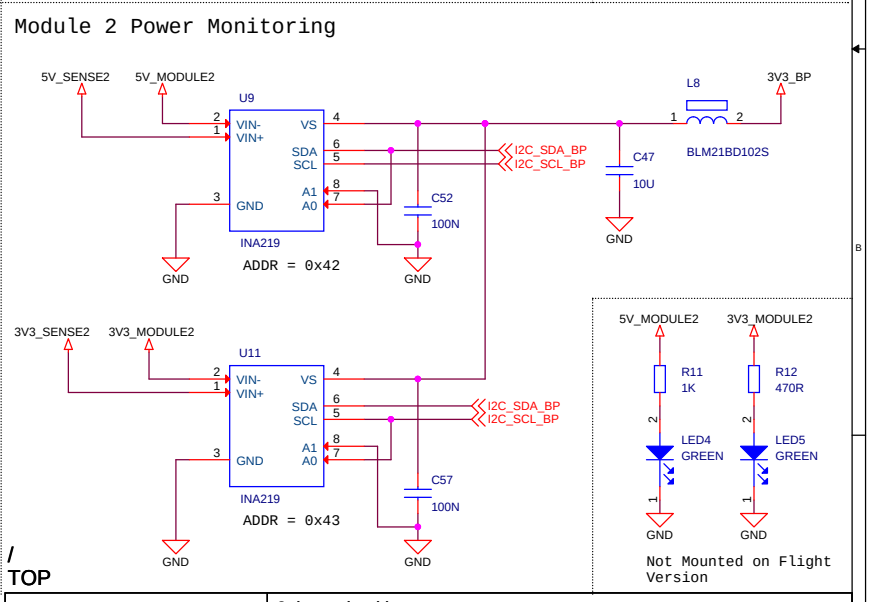

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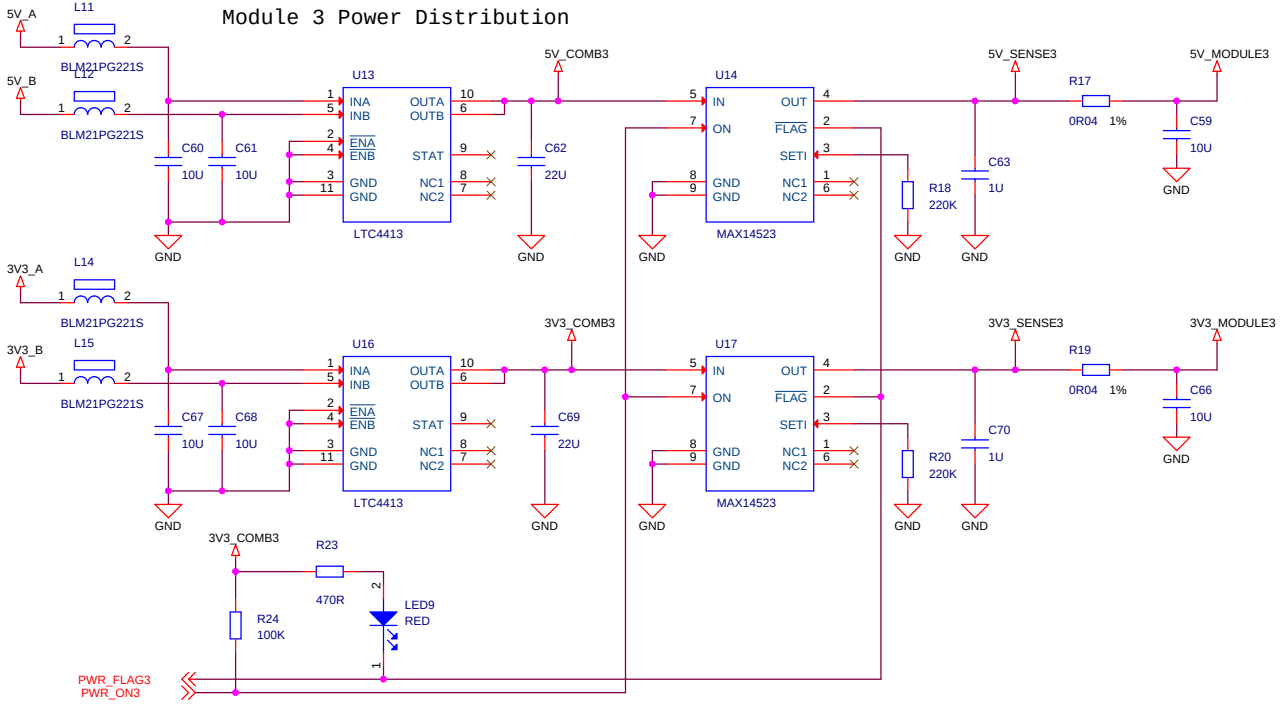
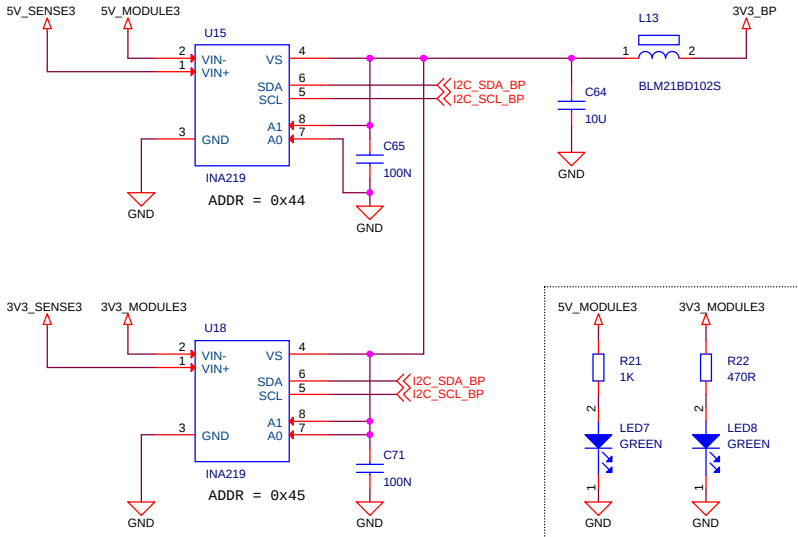
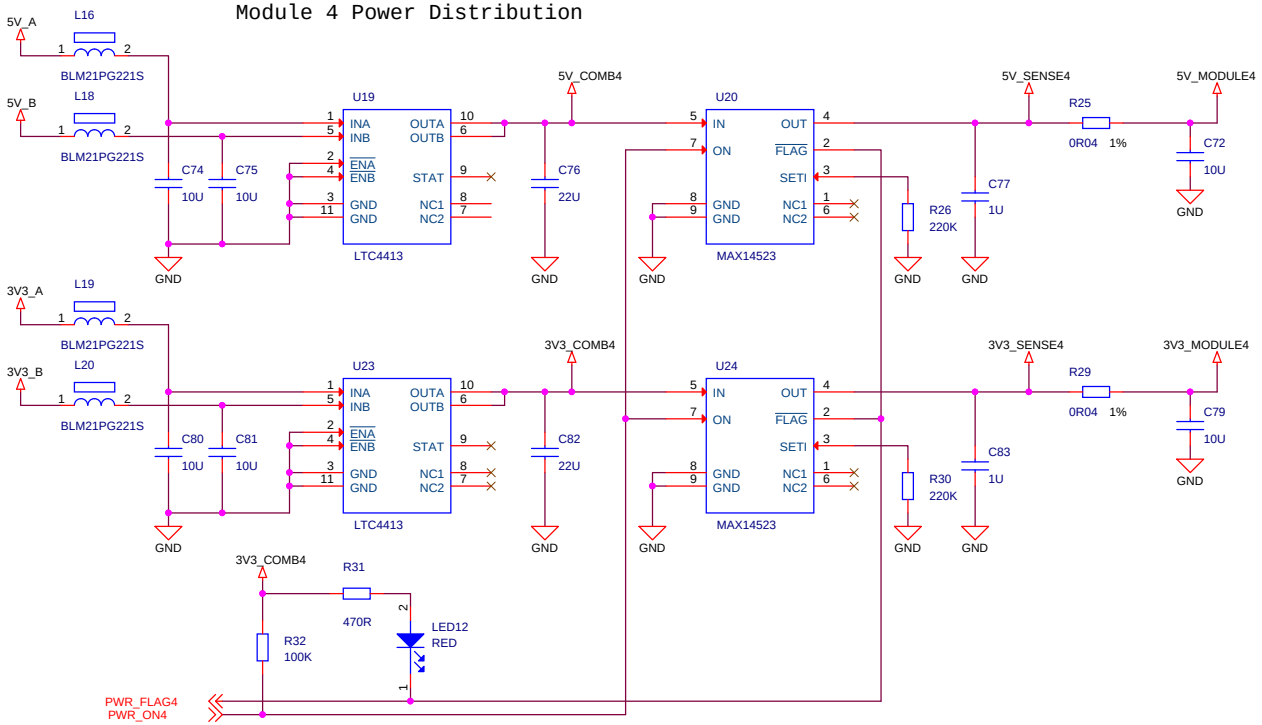
Module 3 Power Distribution



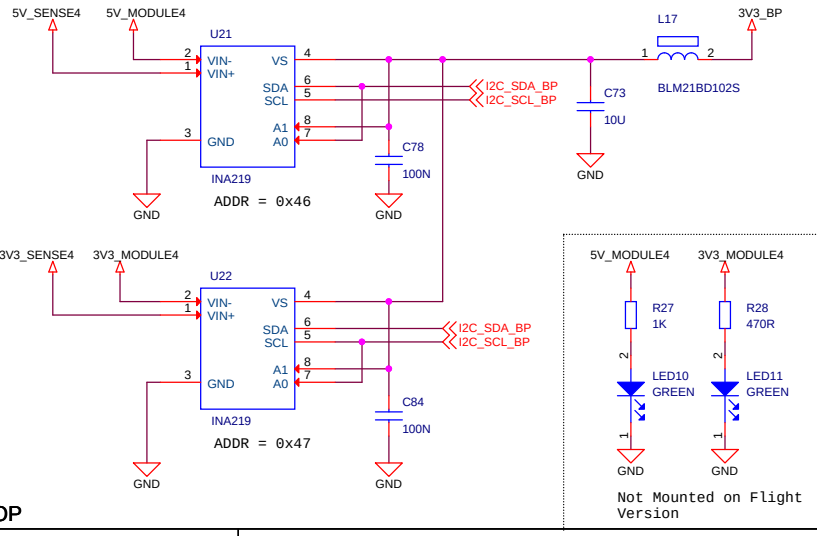
Module 3 Power Monitoring



Module 4 Power Distribution



Module 4 Power Monitoring



/
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Schematic Title	**NUTS Backplane**
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Designed: <OrgAddr1> / Approved: <OrgAddr2>	
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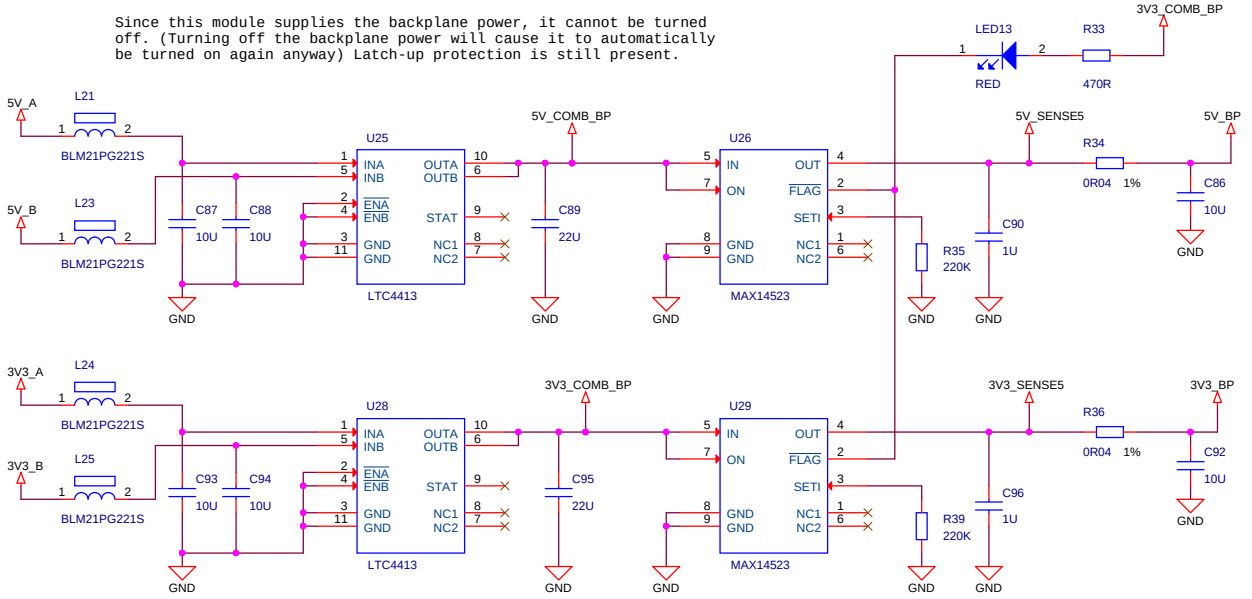
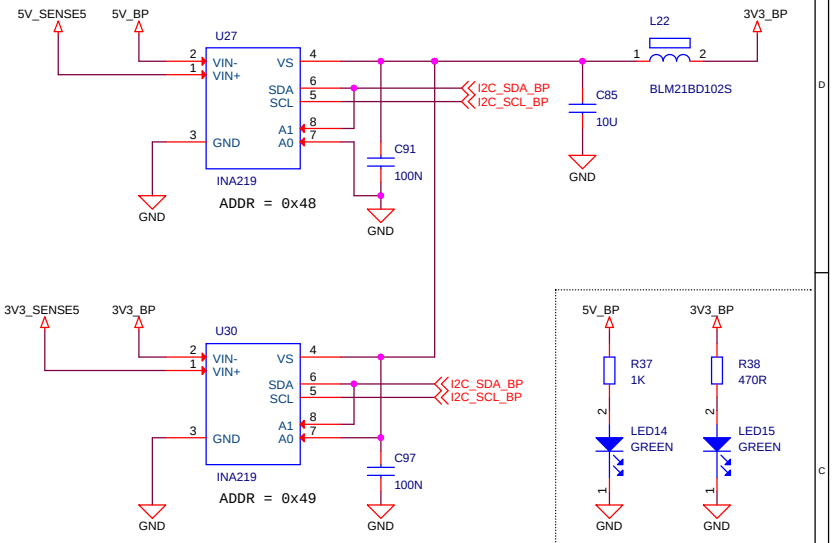
Backplane Power Distribution

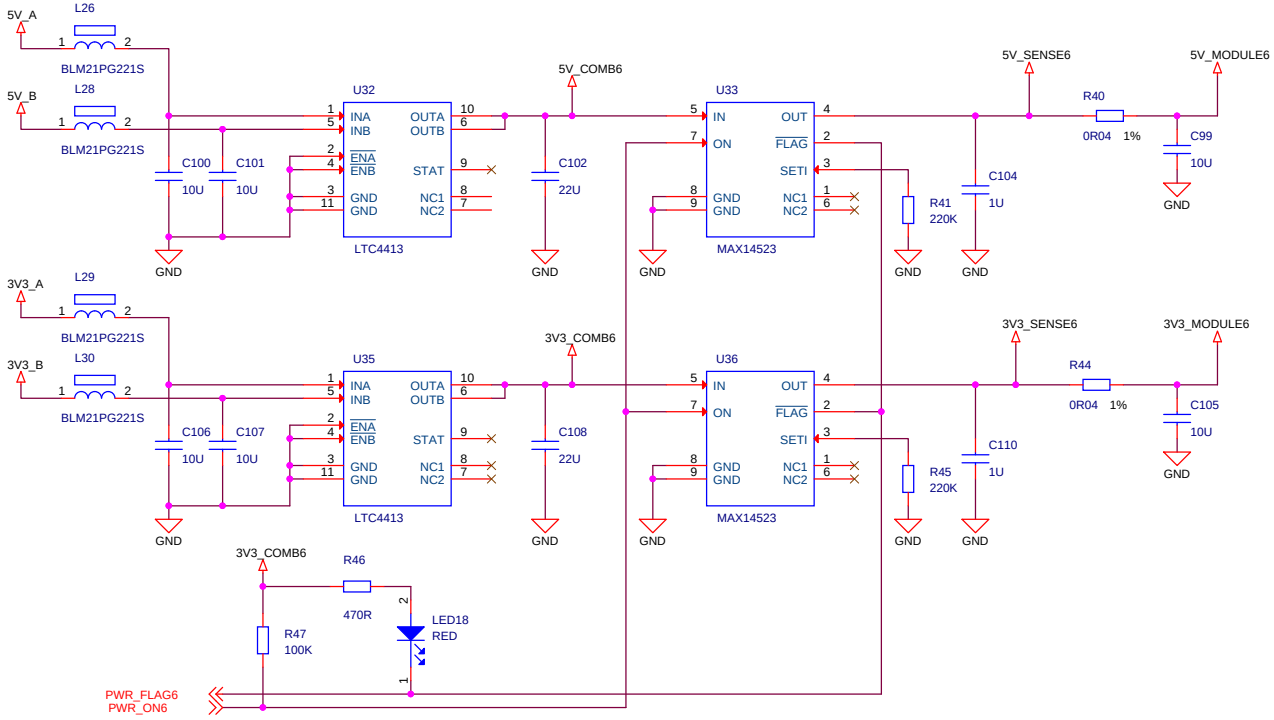
Since this module supplies the backplane power, it cannot be turned off. (Turning off the backplane power will cause it to automatically be turned on again anyway) Latch-up protection is still present.



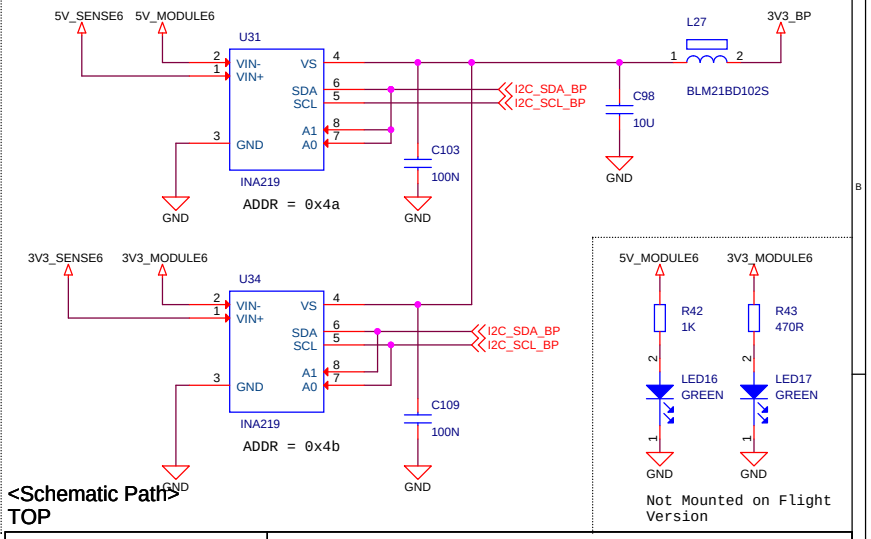
Backplane Power Monitoring



Module 6 Power Distribution



Module 6 Power Monitoring



<Schematic Path>
TOP

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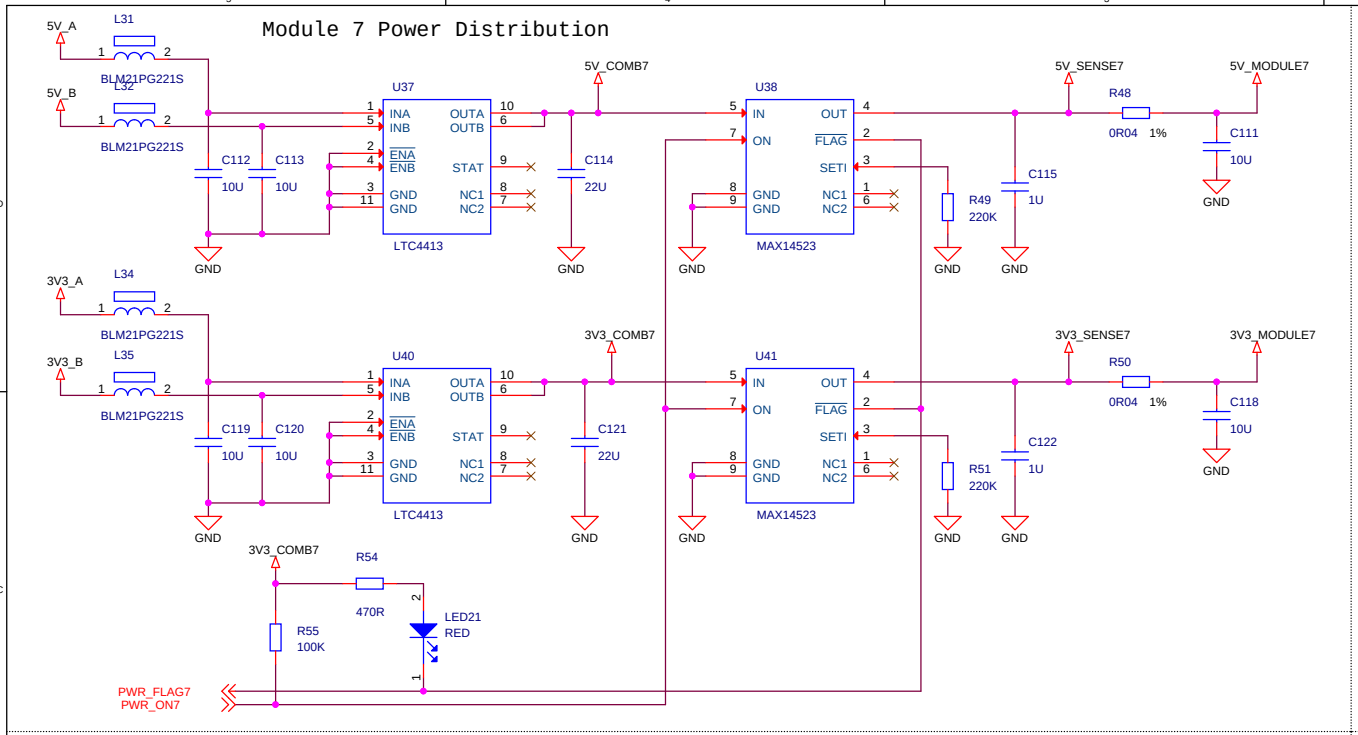

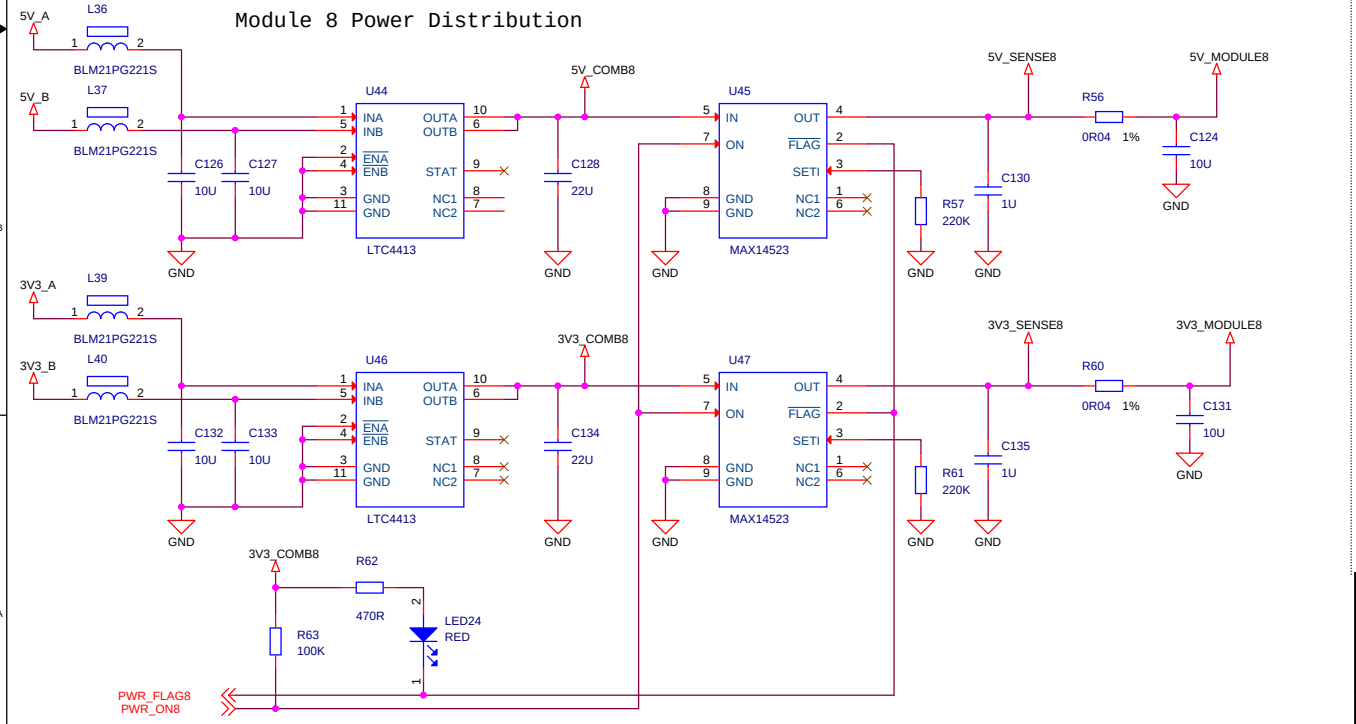

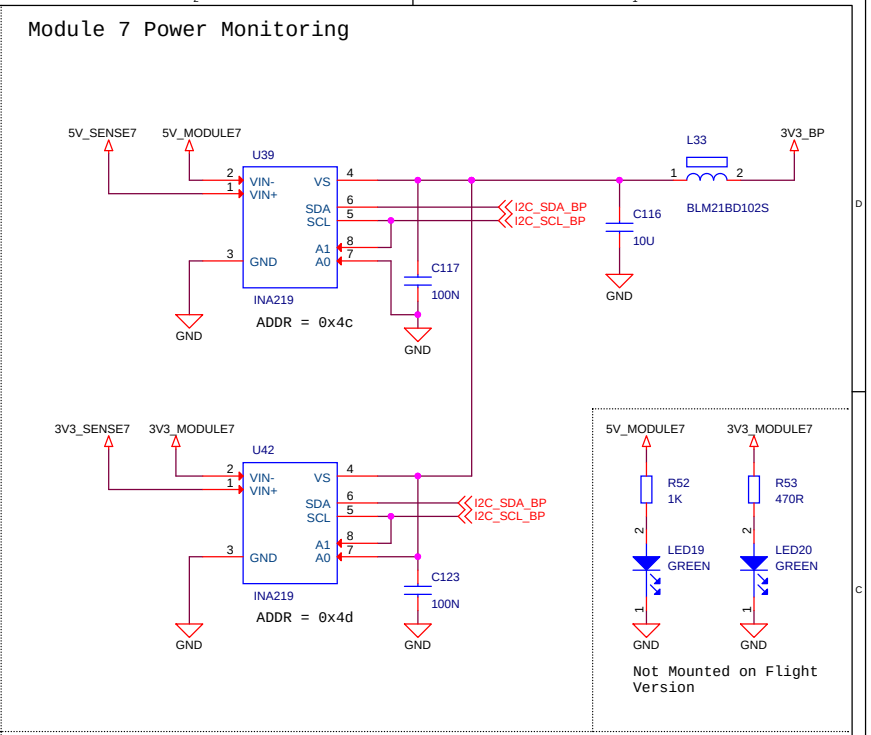

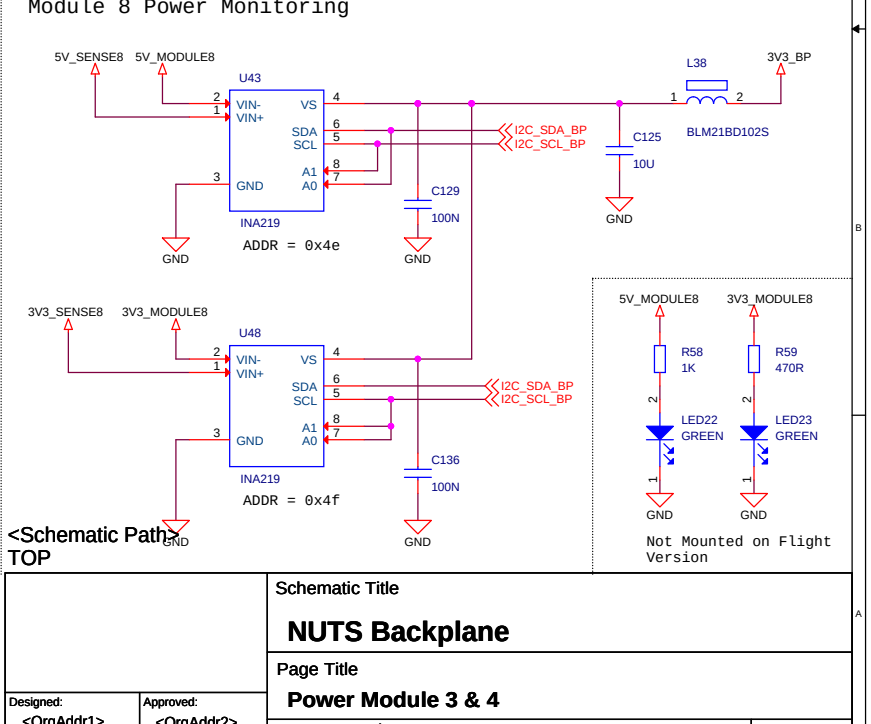

	Schematic Title: **NUTS Backplane**	
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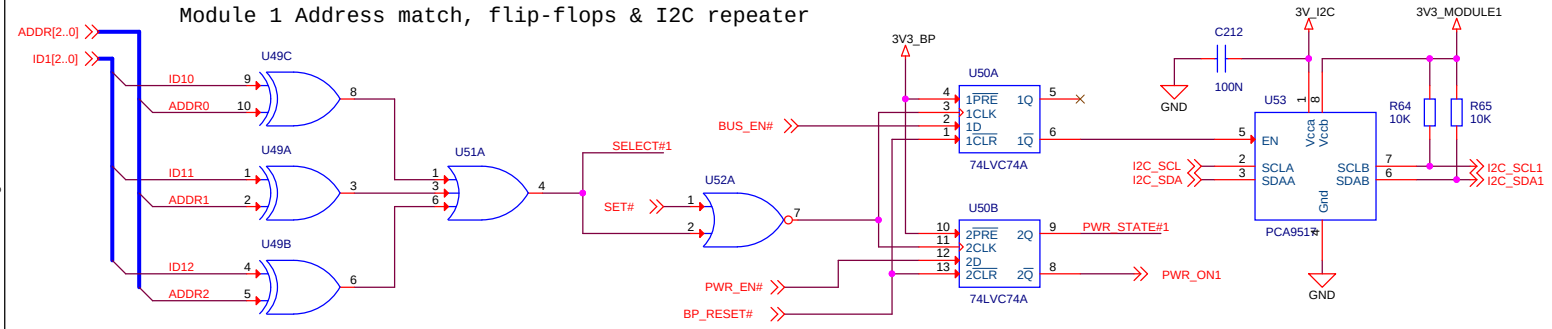
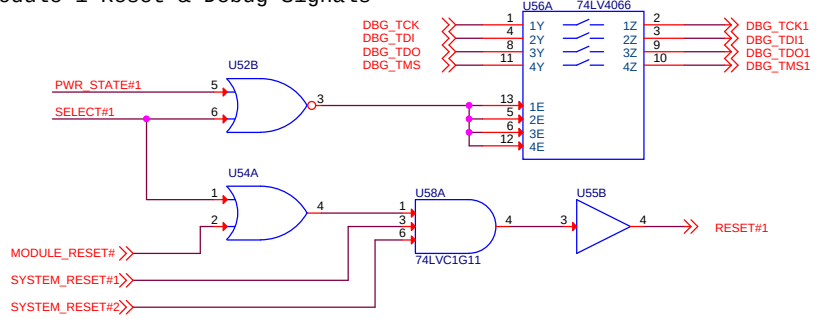
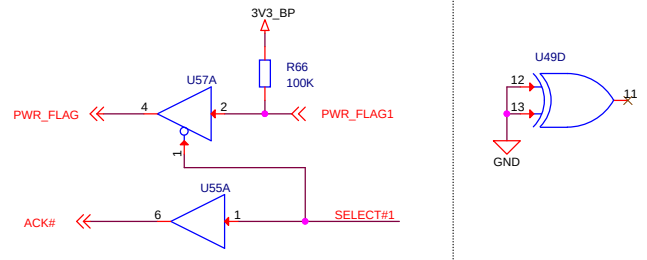
Module 1 Address match, flip-flops & I2C repeater



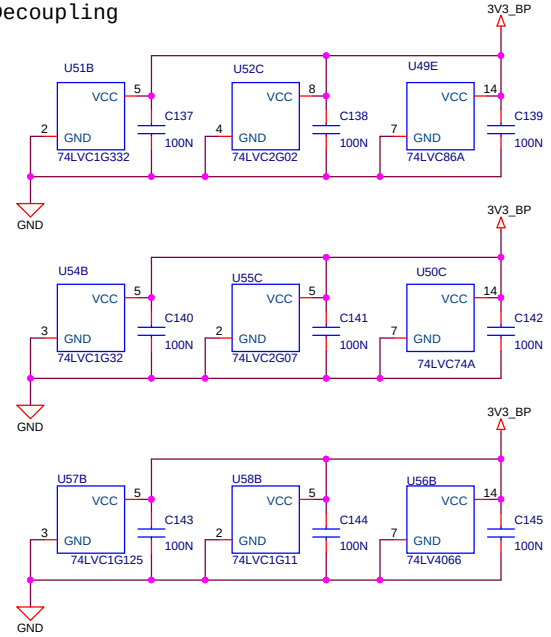
Module 1 Reset & Debug Signals



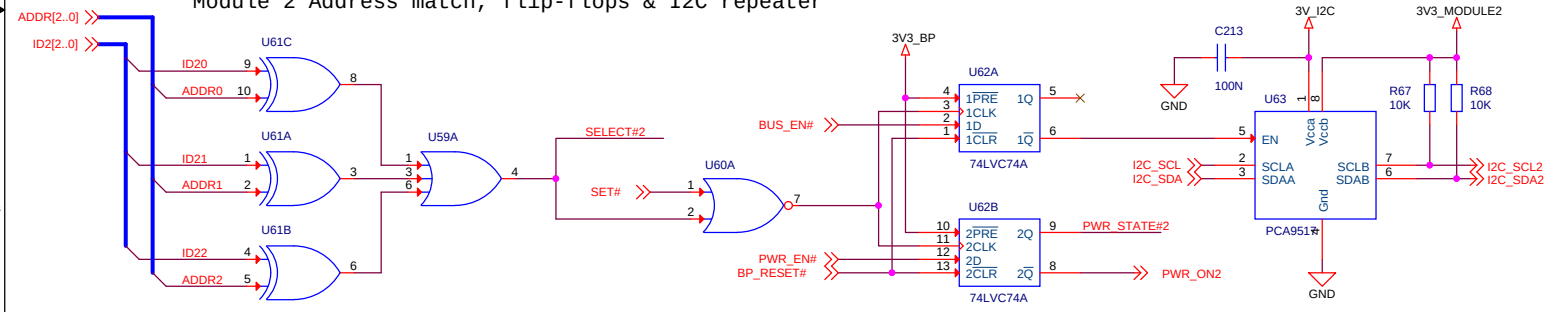
Module 1 Acknowledge & Power flag



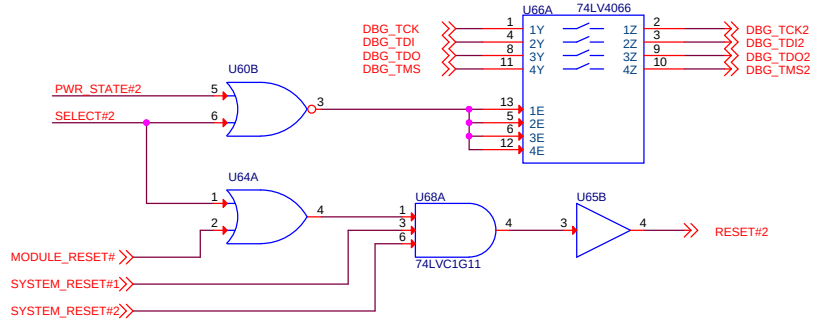
Decoupling



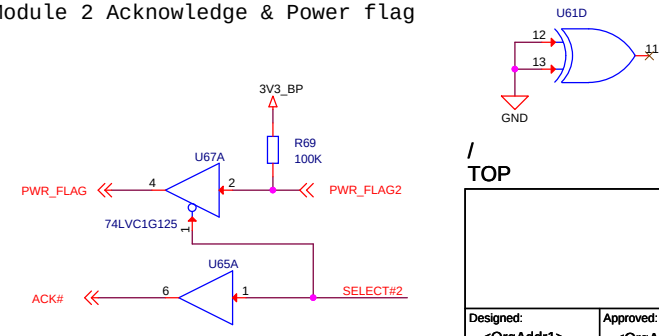
Module 2 Address match, flip-flops & I2C repeater



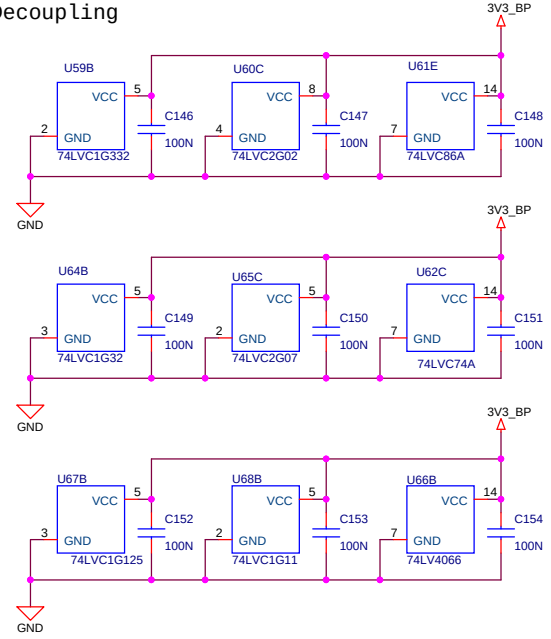
Module 2 Reset & Debug Signals



Module 2 Acknowledge & Power flag



Decoupling



/
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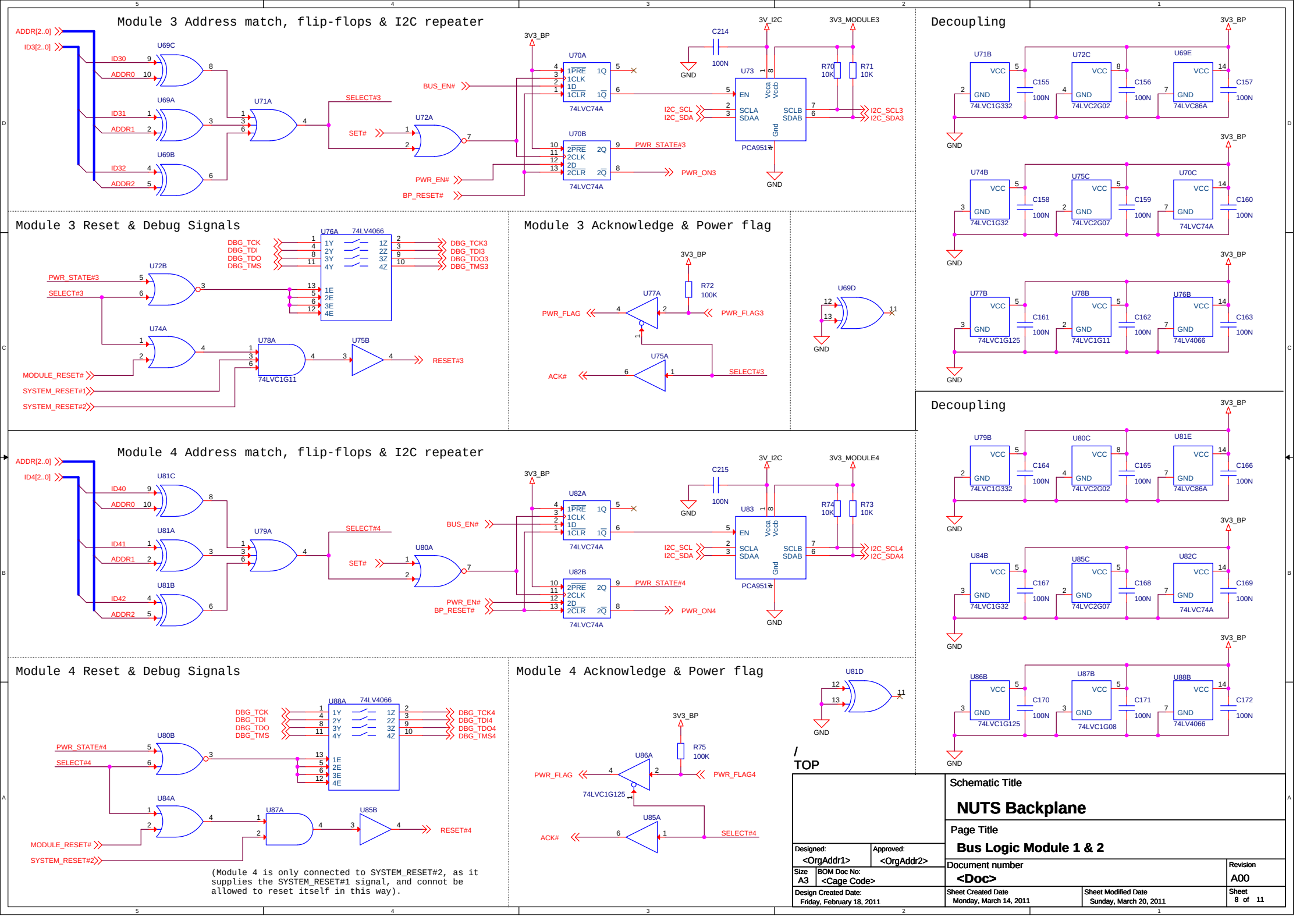
Module 3 Address match, flip-flops & I2C repeater
Module 3 Reset & Debug Signals
Module 3 Acknowledge & Power flag
Module 4 Address match, flip-flops & I2C repeater
Module 4 Reset & Debug Signals
Module 4 Acknowledge & Power flag
Decoupling
Decoupling
(Module 4 is only connected to SYSTEM_RESET#2, as it supplies the SYSTEM_RESET#1 signal, and connot be allowed to reset itself in this way).
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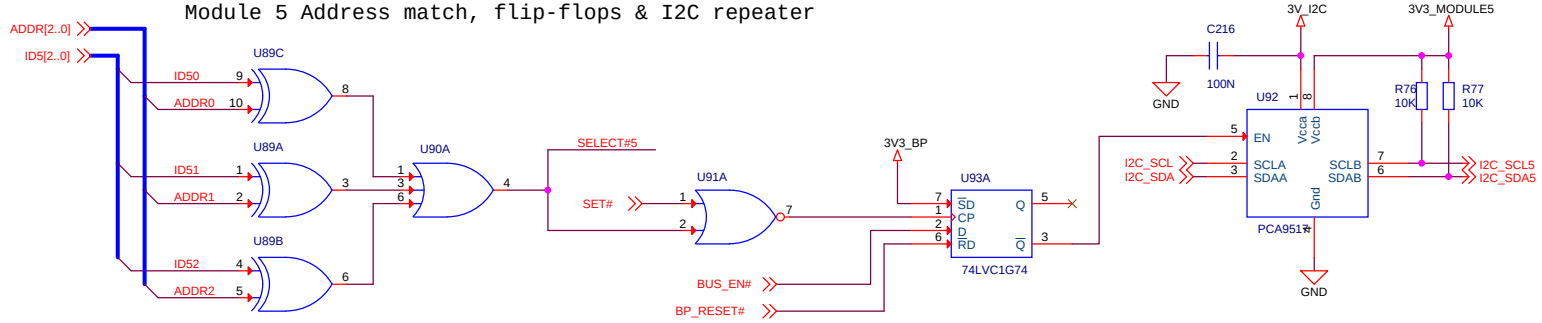
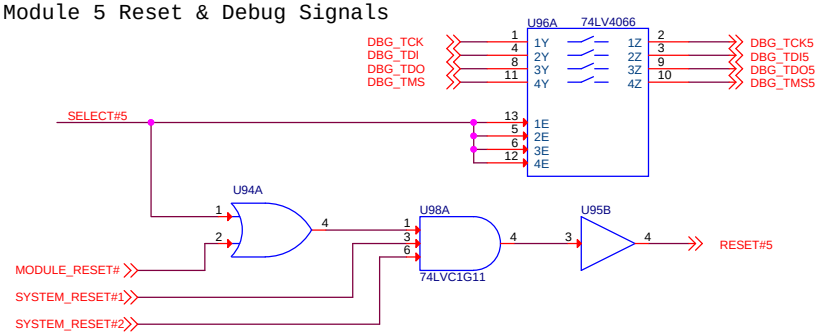
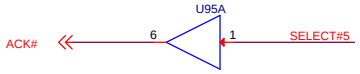
Module 5 Address match, flip-flops & I2C repeater



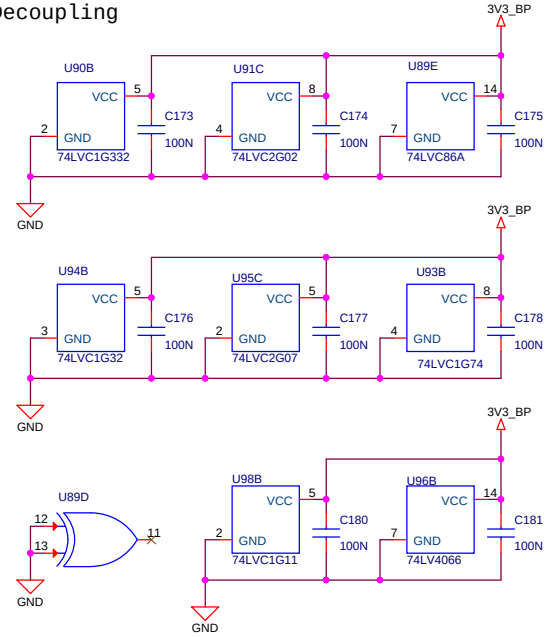
Module 5 Reset & Debug Signals



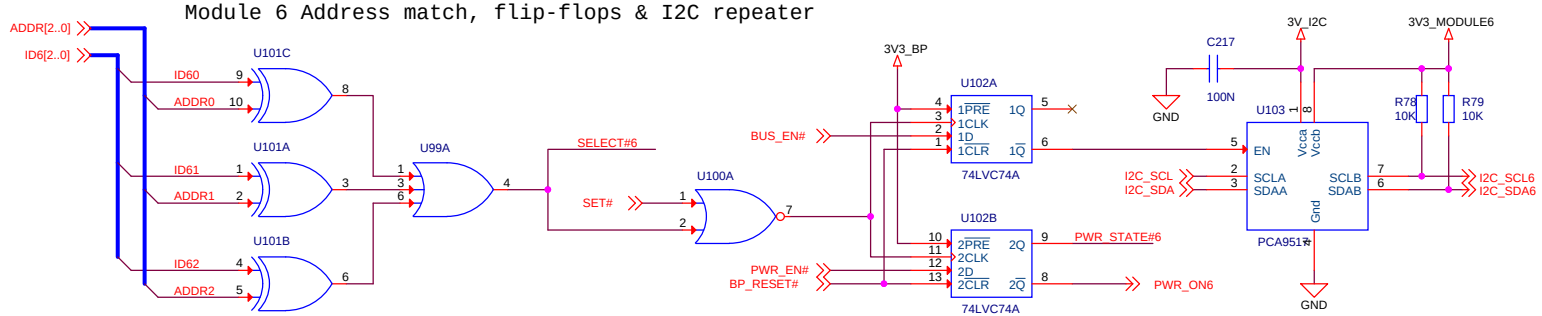
Module 5 Acknowledge



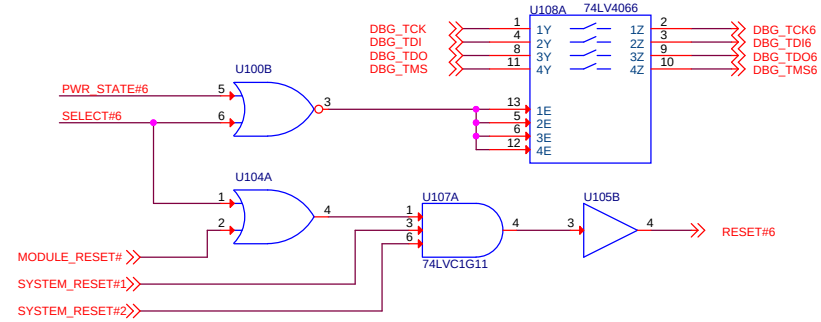
Decoupling



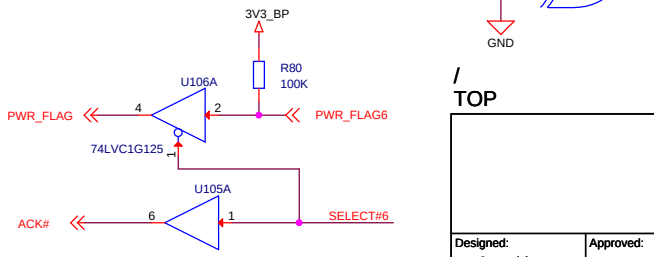
Module 6 Address match, flip-flops & I2C repeater



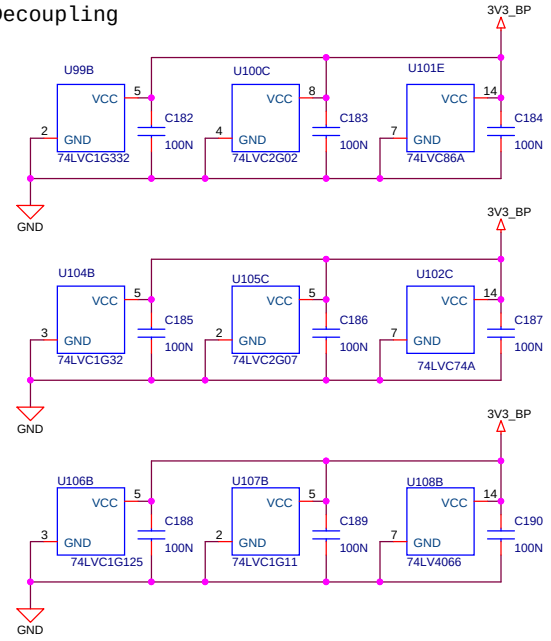
Module 6 Reset & Debug Signals



Module 6 Acknowledge & Power flag



Decoupling



/
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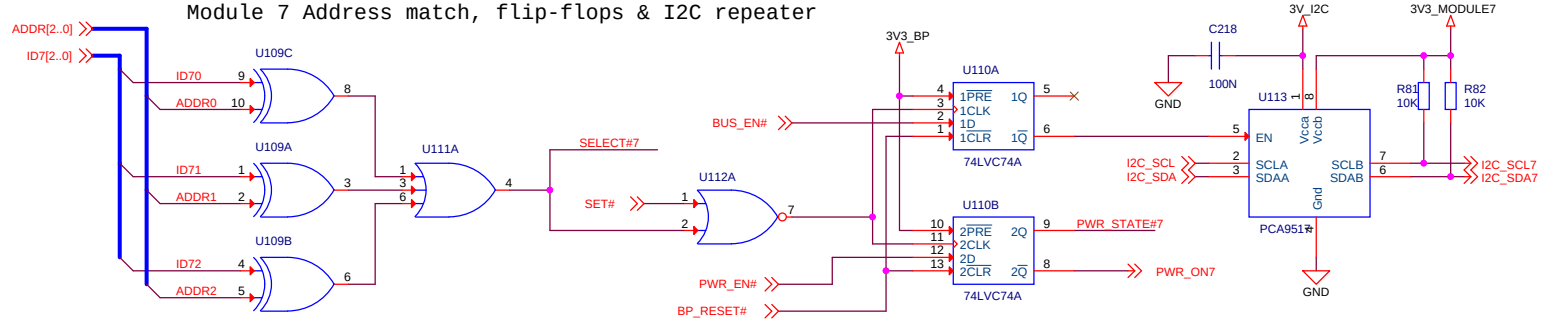
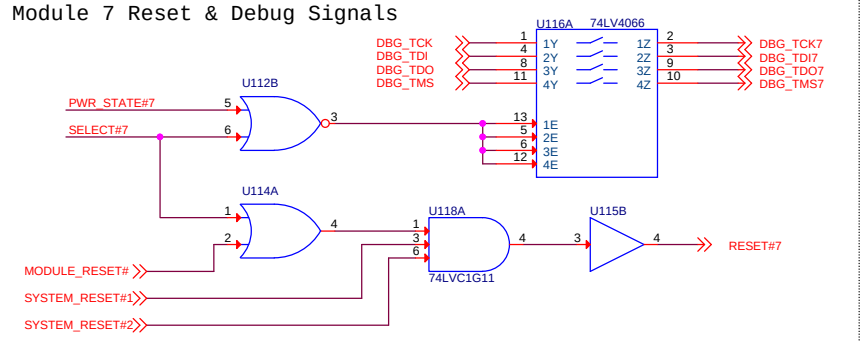
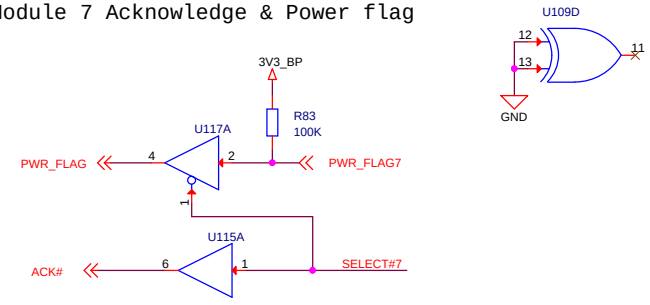
Module 7 Address match, flip-flops & I2C repeater



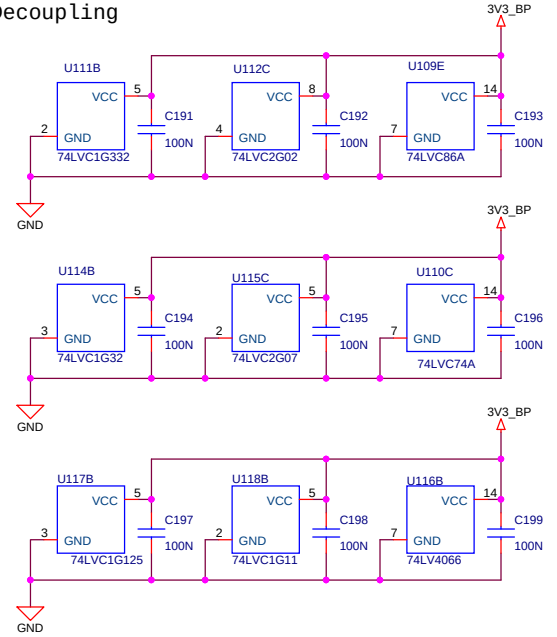
Module 7 Reset & Debug Signals



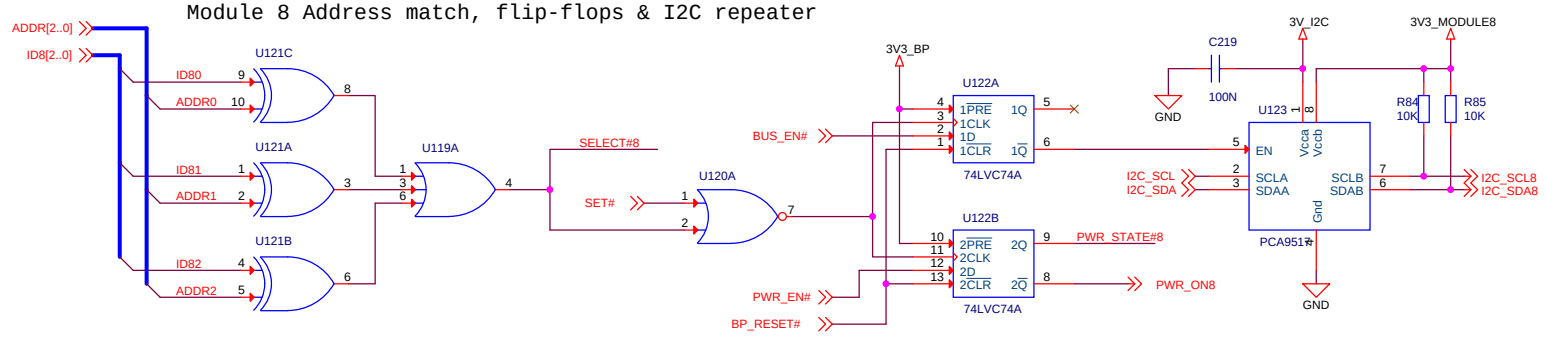
Module 7 Acknowledge & Power flag



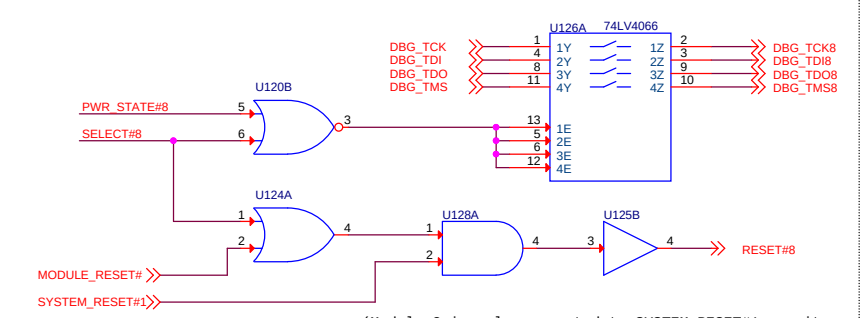
Decoupling



Module 8 Address match, flip-flops & I2C repeater

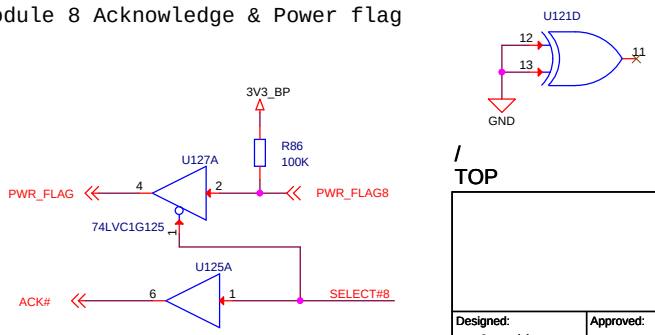


Module 8 Reset & Debug Signals

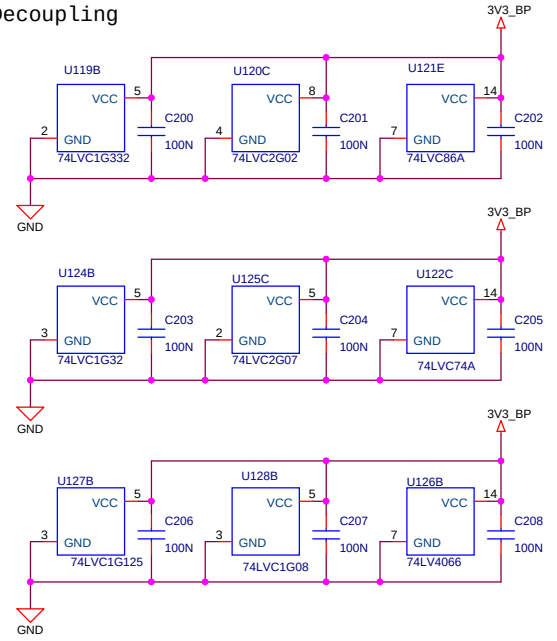


(Module 8 is only connected to SYSTEM_RESET#1, as it supplies the SYSTEM_RESET#2 signal, and connot be allowed to reset itself in this way).

Module 8 Acknowledge & Power flag



Decoupling



/
TOP

Schematic Title	**NUTS Backplane**
Page Title	**Bus Logic Module 1 & 2**
Designed: <OrgAddr1> / Approved: <OrgAddr2>	Document number **<Doc>** / Revision **A00**
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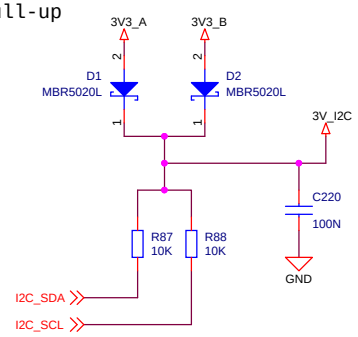
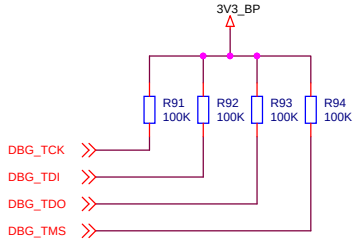
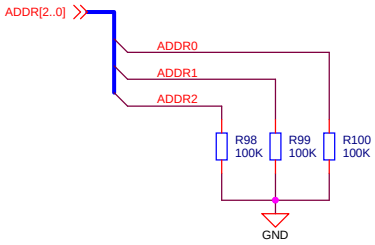
I2C Bus Pull-up



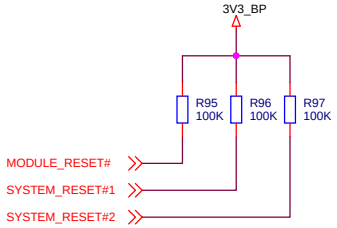
DEBUG Pull-up



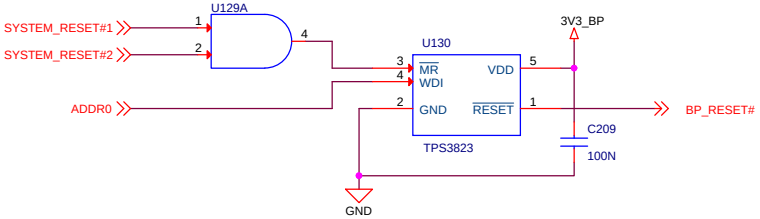
ADDR Pull-down

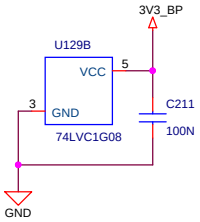


RESET Pull-up

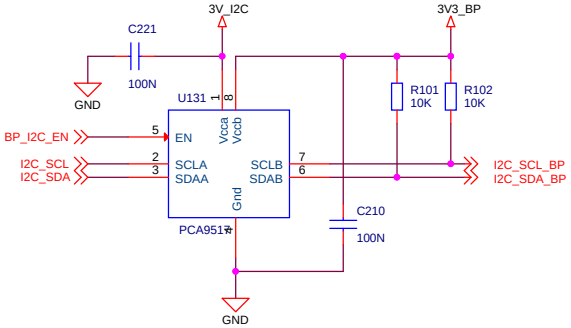


Backplane Reset Monitor

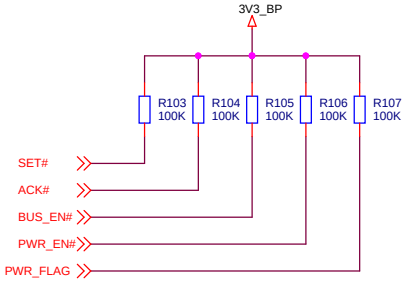


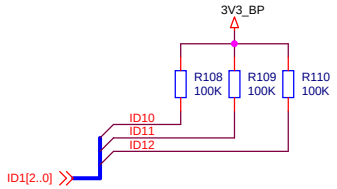


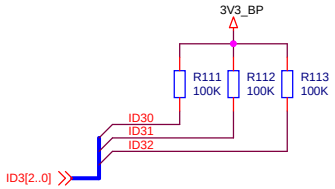
Backplane I2C Isolation

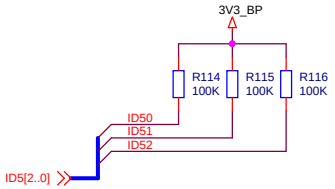


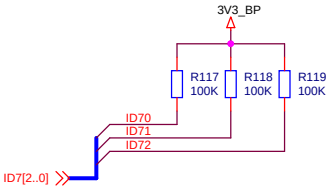
Control signals Pull-up

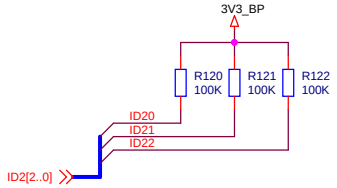


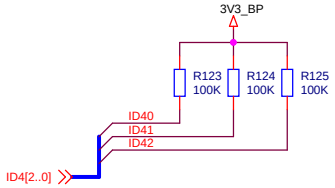


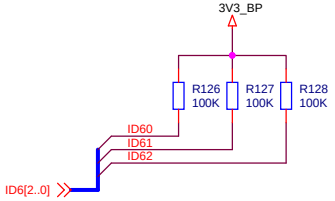


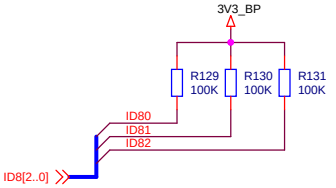












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Pull-ups on all ID lines

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