NTNU

Norwegian University of
Science and Technology

A 33 µW Sub-3 dB Noise Figure Low Noise Amplifier for Medical Ultrasound Applications

Hans Herman Hansen

Master of Science in Electronics
Submission date: July 2011
Supervisor: Trond Ytterdal, IET

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Problem Description

The main goal of this project is to design a low nose amplifier for medical ultrasound imaging using a 180 nm design kit from Austria Microsystems. The low noise amplifier is intended to be used with a piezoelectric transducer with a center frequency of 7 MHz and a 100 % relative bandwidth, i.e. from 3.5 MHz to 10.5 MHz.

The main focus should be on the design of the low noise amplifier, having a very low power budget and small area. The maximum power per channel is 130 µW for both transmit and receive. Therefore, the available power for the analog–front end is limited to half of this. As a result the maximum power consumption for the low noise amplifier is 40 µW, which only allows for a bias current of 22.2 µA for a 1.8 V supply. The noise factor should ideally be less than 3 dB, but due to the extremely low power budget a noise factor as high as 5 dB is acceptable. It would also be of great advantage if the amplifier could perform a single–ended to differential conversion.

The given transducer element can be modeled at resonance as a capacitor of 450 fF in parallel with a 32 kΩ resistor. Due to the high impedance of this small element, the input capacitance should be as small as possible in order to cause minimum attenuation of the input signal of the amplifier, i.e. less than 100 fF. The input resistance should be much higher than 32 kΩ in order to achieve a good voltage division when using voltage sampling.

The type of output could be both current and voltage. In case of a voltage amplifier, the voltage gain should be more than 20 dB.

The main topic of this thesis is to design a low noise amplifier for ultrasound applications. Thus, the task will consist of

1. Be familiar with low noise amplifier fundamentals
2. Be familiar with ultrasound front–end electronics, including variable gain
3. Designing a low noise amplifier within the specifications
4. Verifying the design through relevant test benches

A major specification of any ultrasound front–end is the ability to handle the large dynamic range of the ultrasound signal. If time, the project could also include investigations of different methods of implementing variable gain. Finally, designing the layout and doing post layout simulations could also be done as a part of the thesis.

Assignment given: 31. August 2010. Supervisor: Trond Ytterdal, IET.

Abstract

The low noise amplifier is a critical part of most high performance ultrasound receivers, and is important for achieving high sensitivity and a wide dynamic range. By having a large gain in the low noise amplifier, the total noise of the receiver system will be dominated by that of the amplifier. For most low noise amplifier, there is a fundamental trade–off between accuracy and power consumption, which makes it difficult to design micro power front–end amplifiers with excellent noise performance. In some cases, however, lower accuracy can be tolerated if the source itself is noisy. This is the case for small, high impedance sources, where the noise level is in the region of $18\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

This thesis presents the design and simulations of a low noise amplifier in standard 180 nm CMOS suitable for use with high impedance sources. In fact, high impedance sources pose challenges on the biasing of voltage amplifiers, where maintaining high input impedance is necessary. In addition, for differential amplifiers, implementing common–mode feedback will typically result in a significant increase in power consumption and area overhead. To alleviate this problem, a switched common–mode feedback scheme is implemented, that also provide high input impedance biasing of the input transistors.

In order to cope with the large dynamic range requirement inherent in many ultrasound modalities, variable gain is often used to compress the dynamic range for the analog front–end. Methods for adding variable gain without resulting in a large increase in area and power consumption is therefore of huge interest in many ultrasound applications. Several methods of adding variable gain is investigated in this thesis, and a capacitive attenuator is proposed, which causes minimum increase in noise factor, while increasing the gain range by at least 20 dB.

Large scale integration of several thousands analog front–ends in a single ultrasound probe handle requires low power consumption and minimum area overhead for all parts of the analog front–end, including the low noise amplifier. By using a figure–of–merit based optimization technique, the designed amplifier topology achieves an low power consumption of 17.3 µA, while maintaining a noise factor of less than 3 dB at resonance. In addition to performing a single–ended to differential conversion, this amplifier realizes a maximum voltage gain of 23.4 dB, with a 3 dB bandwidth of 21.5 MHz.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of master of science (MSc) at the Department of Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU). The work was carried out in the period August 2010 to July 2011 as a 50 % part time study, under the supervision of Professor Trond Ytterdal, who is with the Department of Electronics and Telecommunications at NTNU

Acknowledgment

First and foremost I would like to thank my adviser Trond Ytterdal, both for introducing me, and giving me the opportunity to work with the topic of analog circuit design. His vast, and seemingly never–ending insight within the topic, combined with his enthusiasm, have been a great source for both motivation and inspiration during this work.

I would like to thank my fellow students for valuable input during the course of writing this thesis. I would especially like to thank my friend and fellow student Dragan Mitrevski for many motivating and fruitful conversations, and for introducing me to many of the advanced typesetting techniques used throughout this thesis. I'm also grateful to the rest of my friends I've made over the years at NTNU for six unforgettable year. Especially thanks to Einar Berge Mogstad, Henning Bjørgo, Johannes Haukelidsæter, Even Heum Hennie, Anders Ellingsen Stephansen, Eirik Skogestad Næs, Rune Bergh Nilssen and Markus Løland for making all these years fly by.

Trondheim, Norway, July 2011,
Hans Herman Hansen

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Ultrasound imaging for medical and nondestructive testing purposes has made significant progress since its introduction over half a century ago [1]. In fact, much of the increase in the use of diagnostic ultrasonic imaging can be traced to improvements in image quality. In addition, digital imaging systems coming into use hold the promise of further enhancing image quality [2]. The flexibility inherent in digital imaging systems enables the possibility of using a wide range of algorithms to reconstruct, enhance, and analyze ultrasonic images. However, the usefulness of these algorithms is limited by the quality of the original data. Critical to any digital ultrasound imaging system is the analog front–end; the transducer and associated electronics which link the digital system to the medium under examination. Although imaging capabilities can be improved by digital signal processing techniques, the analog front–end normally sets the performance limits of the complete system. In particular, the signal–to–noise ratio (SNR), bandwidth, and dynamic range of the sampled data all have a strong impact on the utility of certain image processing approaches.

Typically, one of the bottlenecks in analog front–ends is the low noise amplifier, which must introduce as little noise and distortion as possible in order to maximize the sensitivity and dynamic range. On the other hand, the noise requirements can be relaxed if the source itself, i.e. the transducer, is less accurate. For transducers with a body resistance of several kilo ohms, the noise requirements for a 3 dB noise factor can be achieved with a relatively low power consumption. However, as the ultrasound wave propagating in tissue experiences an attenuation of 1 dB/cm/MHz the dynamic range requirements can in some applications be as high as 160 dB [3]. In order to cope with the large dynamic range associated with ultrasound imaging, variable gain is usually required in the receive amplifier.

In the pursuit of even more flexible ultrasound systems, there is an ongoing trend of integrating as much of the electronics into the transducer probe, including a low noise amplifier and analog to digital converter (ADC). Especially for 3–D ultrasound imaging this can reduce the amount of channels by employing micro beamforming in the probe handle, but also relax the amount of high quality micro–coaxial cables by also integrating the ADC in the transducer. In fact, the system cable consisting of several hundred micro–coaxial cables can be one of the most expensive part of the ultrasound system. By integrating the ADC in the probe

handle, digital beamforming can be partially done in the front–end as well as in the main unit, which usually results in a better increase in signal–to–noise ratio compared to analog beamforming. Although very desirable, the area and power consumption of such an analog front–end would be extremely limited.

A front–end amplifier topology that can satisfy the requirement of high input impedance and sufficient linearity is based on the source coupled differential pair with resistive source degeneration. This amplifier topology can achieve high linearity, without sacrificing power consumption and noise performance, by boosting the transconductance, g_{m}, of the input transistors using a composite device [4]. This linearized transconductor cell has received some attention in the literature [5], [6], [7], [8], [9]. For most of the applications, however, the noise performance is incompatible with medical ultrasound [5], [6], [7]. Even though [8] shows excellent linearity and variable gain, the power consumption and integrated noise is too high for this ultrasound application. Also, the low noise and distortion achieved in [9] comes at the expense of a current consumption of 40 mA, which is a few decades above the requirement in the design specifications.

This thesis presents the design of a ultra low power, low noise amplifier using a figure–of–merit based approach [10]. By applying the figure–of–merit based technique proposed in [10], an optimized trade–off between noise and power consumption can be achieved. The designed amplifier performs a single–ended to differential conversion to match the single–ended transducer to a differential front–end. By exploiting the fact that most ultrasound systems transmit and receive pulses in time intervals, a switched common–mode feedback is proposed and implemented, that minimizes the power and area overhead typically involved with common–mode feedback circuitry, while also providing biasing of the input transistors. In contrast to many ultrasound systems, where variable gain can be implemented in a separate amplifier, the analog front–end integrated in the probe handle does not have the luxury of too much analog signal processing. However, the dynamic range must be compressed before the ADC, as dynamic range is very expensive in terms of power consumption. Therefore, a digitally controlled variable gain method is proposed that is based on a capacitive attenuator. By using a capacitive divider in front of the low noise amplifier, the input dynamic range of the micro power, front–end amplifier can be limited to avoid clipping, without sacrificing the receiver noise factor.

1 Thesis Outline

This thesis is organized as follows; Chapter 2 provides a theoretical background for low noise amplifiers, with focus on noise and linearity.

In Chapter 3, ultrasound systems are described in general in order to understand the most important trade–offs in the design of front–end electronics for ultrasound. Some previous knowledge on the topic is assumed.

Chapter 4 motivates the need for in–probe electronics, and sketches the requirements for the analog front–end amplifier to be used in such a system. Some of the specifications of the amplifier have been derived using the piezoelectric transducer source, such as input referred noise level and required input resistance.

The proposed amplifier topology is described in Chapter 5, and a small–signal analysis of the circuit is provided in order to derive design equations and investigate noise performance.

Chapter 6 describes different ways of implementing variable gain for the proposed front–end, where a capacitive attenuator, that can limit the dynamic range requirement for the front-end amplifier, is proposed and described.

In Chapter 7 the figure–of–merit based approach is described and applied in the design of the front–end amplifier. In addition, the design of the variable gain attenuator and common–mode feedback circuitry is covered in this chapter. A coarse variable gain attenuator is described and simulated using a simple array, consisting of only a few capacitors and switches.

In Chapter 8 the most relevant simulation results are presented and discussed. A comparison with state of the art micro power, low noise amplifiers for biomedical applications is also shown.

Finally, the thesis is concluded in Chapter 9. The conclusion also contains suggestions for future work and a summary of the main contributions of this thesis.

Appendix A shows that the figure–of–merit (fom) used in this thesis is proportional with the more known noise efficiency factor (nef) and argues why they are essentially equivalent formulations.

Appendix B contains the test bench used in the design of the transistor dimensions.

In Appendix C the schematic of the amplifier is shown with a 1:1 corresponding netlist.

Finally, Appendix D shows the different test benches used to verify the amplifier performance.

Chapter 2

Theoretical Background

This chapter briefly describes relevant, fundamental background theory for this thesis, with special focus on noise and linearity. Understanding these two parameters of the analog front–end is important in achieving a high dynamic range, one of the most essential specifications of any ultrasound front–end.

1 Low Noise Amplifiers

The low noise amplifier (LNA) is one of the key building blocks in most high performance analog front–ends, and is essential for achieving high sensitivity and a wide dynamic range. The low noise amplifier buffers the input signal such that the noise generated by the following blocks has little impact on the total signal–to–noise ratio (SNR). In a typical analog front–end, the low noise amplifier is one of the most important components, as it tends to dominate the sensitivity. In general, the amplifier design involves many trade–offs between noise figure (NF), gain, linearity and power dissipation. Given a large gain in the front–end amplifier, the total noise of the receiver system will be dominated by that of the amplifier. For this reason, it is essential that the amplifier can maintain a good signal–to–noise ratio, even at extremely low input signals, but also to be able to have a high dynamic range. This requires that all the receiver blocks, including the low noise amplifier, maintain a good SNR for both small signals and large signals. In fact, the linearity of a circuit is often one of the limiting factors to its dynamic range, and it is typically one of the major specifications for any front–end amplifier.

2 Linearity

Linearity is an important parameter that is determined by a circuit's ability to handle relatively large signal swings. Large signals can cause desensitization and harmonic distortion in a non–linear circuit, and in order to improve performance, linearization techniques are often used in CMOS circuits. For CMOS amplifiers with linear load at the output, the linearity is mainly determined by the input transistors. The transconductance, g_{m}, of a MOSFET in saturation is given by [11]

$$g_{\mathrm{m}} = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} V_{\mathrm{eff}} \frac{1 + (\alpha/2) V_{\mathrm{eff}}}{(1 + \alpha V_{\mathrm{eff}})^2}, \tag{2.1}$$

where V_{eff} is the overdrive voltage, and α is defined as

$$\alpha = \theta + \frac{\mu_0}{2 v_{\mathrm{sat}} L}. \tag{2.2}$$

Here, μ_0 is the mobility when the overdrive voltage is zero and θ is a process constant.

In addition, the body effect causes the threshold voltage to change with the input voltage, described by the following equation

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma_{\mathrm{th}} \left(\sqrt{V_{\mathrm{sb}} + 2\phi_{\mathrm{f}}} - \sqrt{2\phi_{\mathrm{f}}} \right), \tag{2.3}$$

where V_{th0} is the threshold voltage when the source-to-substrate voltage, V_{sb}, is zero. The factor γ_{th} is the well known body-effect constant and ϕ_{f} is the Fermi potential at the channel. This effect usually introduces additional distortion into a CMOS amplifier. Connecting source and substrate together can reduce the distortion, but increases the parasitic capacitance at the source.

In recent years, voltage–to–current converters or transconductance amplifiers has shown signs of dramatic change and find many applications in traditional analog applications. The simplest and most widely used transconductance amplifier is the differential pair. While offering excellent high frequency performance and low noise, its large signal characteristics are inherently non–linear.

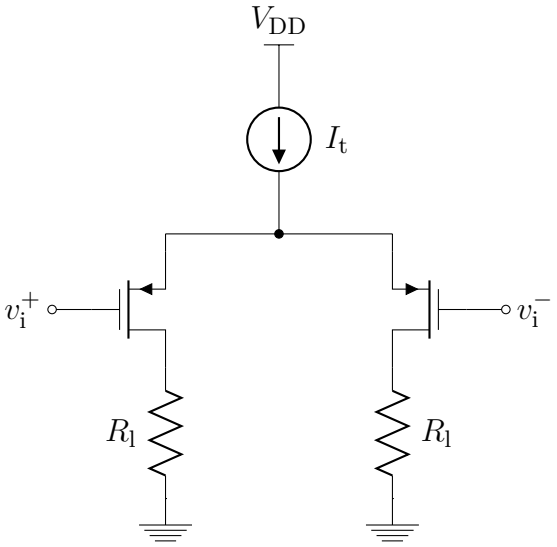

Figure 2.1: P–channel input differential pair.

Assuming perfectly quadratic $i - v$ characteristics for the MOS transistor in the saturation region and neglecting short channel effects such as channel length modulation, the drain current can be written as

$$I_{\mathrm{d}} = \frac{\beta}{2} (V_{\mathrm{gs}} - V_{\mathrm{t}})^2, \tag{2.4}$$

where, β is the transconductance parameter and V_t is the threshold voltage of the transistor. Using this expression for the circuit in Figure 2.1 the output current is given by

$$i_\mathrm{o} = \sqrt{2\beta I_\mathrm{o}}v_\mathrm{i}\sqrt{1-\frac{\beta v_\mathrm{i}^2}{8I_\mathrm{o}}} = \sqrt{2\beta I_\mathrm{o}}v_\mathrm{i}\sqrt{1-\frac{v_\mathrm{i}^2}{4\left(V_\mathrm{gs}-V_\mathrm{t}\right)^2}} \tag{2.5}$$

In general, increasing the overdrive voltage, $V_\mathrm{gs}-V_\mathrm{t}$, and using a longer channel device can improve linearity. Using longer devices, results in a smaller α, but on the other hand, it also increases the power consumption and reduces the cut–off frequency, ω_t.

For low–voltage applications requiring a high overdrive voltage usually constitutes a major drawback. In fact, using a very high overdrive voltage usually results in a poor current efficiency, $g_\mathrm{m}/I_\mathrm{d}$, which may be unacceptable in power constrained designs.

3 Linearization Techniques

The principle idea behind linearization is to reduce the dependence of the gain upon the input signal level. Normally, this translates into making the gain less dependent of the transistor bias current. One of the simplest topologies to linearize the transfer characteristic of the MOS transconductor is by means of source degeneration using a linear resistor as depicted in Figure 2.2.

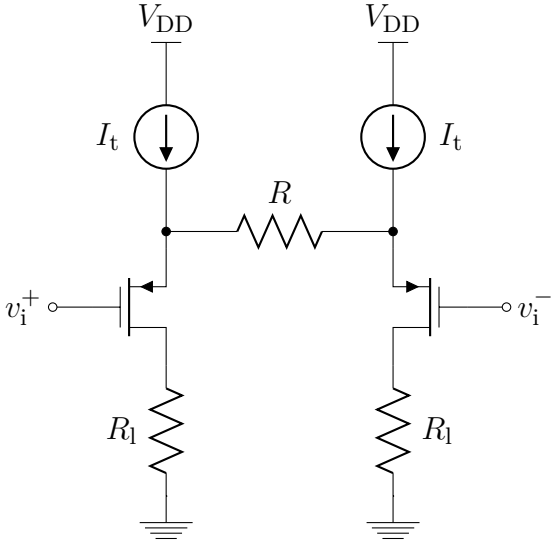

Figure 2.2: Differential pair using resistive degeneration.

The degeneration resistor reduces the signal swing applied between the gate and the source of the transistor by means of an internal feedback path, thus making the transfer function more linear. Neglecting the body effect, the overall transconductance of the stage can be written as

$$G_{\mathrm{m}} = \frac{g_{\mathrm{m}}}{1 + g_{\mathrm{m}} R}, \tag{2.6}$$

which for large $g_{\mathrm{m}}R$ is given by $G_{\mathrm{m}} \approx 1/R$, an input independent parameter. It is worth mentioning that the amount of linearization is dependent on $g_{\mathrm{m}}R$ rather than the degeneration resistor alone. Using this technique the G_{m} is relatively independent of the input and the amplifier is thus linearized.

The disadvantage of this configuration is the large resistor value needed to achieve a wide linear input range as it requires $g_{\mathrm{m}}R \gg 1$. Since in this case $G_{\mathrm{m}} \approx 1/R$, the obtained transconductance may be restricted to small values. Alternatively, using a $g_{\mathrm{m}} \gg 1/R$ is typically not a viable option in power constrained designs.

4 Noise in Solid–State Circuits

In general, there are several noise contributors in solid–state circuits. For transistors, they include thermal noise generated in the resistive channel, usually caused by the random collisions of carriers with the lattice, flicker noise generated by the surface traps between the silicon and the gate oxide and shot noise related to the junction diodes, caused by the random emission of electrons or photons, or the random passage of carriers across potential barriers [12].

Both the channel thermal noise and the junction shot noise have a white noise spectrum, in contrast to the flicker noise, which has a $1/f^{\alpha}$ spectrum, where $\alpha \approx 1$. For field–effect transistors in saturation, the channel thermal noise is generally much more significant than the shot noise.

5 Thermal noise

The limiting noise mechanism in field-effect transistors is in many applications thermal noise from the conducting channel. Thermal noise arises from the random thermal motion of the carriers in addition to its drift in the field. A MOSFET has an inverse resistive channel between the drain and the source, where the gate voltage forms with minority carriers in the channel. In the case when the drain source voltage $V_{\mathrm{ds}} = 0$ V, the noise corresponds to thermal noise of the drain conductance, i.e. the channel can be treated as a homogeneous resistor with associated thermal noise. The noise in the channel is then

$$i_{\mathrm{n}}^2(f) = 4kTg_0, \tag{2.7}$$

Here, g_0 is the channel conductance at zero drain–source voltage. This expression is also valid when the transistor is operating in the linear area with resistive characteristics, by replacing g_0 with the actual drain–source conductance, g_{ds}. The temperature T is given in Kelvin and k is Boltzmann's constant.

For typical biasing conditions, V_{ds} is not close to zero, which results in noise characteristics different from that of a homogeneous resistor. Taking the body effect into account, the thermal noise current can be found as

$$i_{\mathrm{n}}^2(f) = 4\gamma kT g_{\mathrm{m}}, \tag{2.8}$$

where g_{m} is the transconductance of the transistor. The factor γ is a complex function of transistor parameters and biasing conditions. Without taking short channel effects, such as channel length modulation and mobility degradation into account it typically has a value of between 2/3 and 1 [12], [13]. It is worth mentioning that (2.8) has limited validity and cannot be used when the transistor is operating in the triode region, which is a limitation in applications such as MOSFET–C and G_{m}–C filters [14], [15].

On the other hand, using (2.7) and multiplying with γ results in a model that works well for long channel devices. However, it is not very accurate for short channel devices, especially in saturation, which is the usual region of operation for MOSFETs in analog integrated circuits.

A more accurate noise model is therefore required for robust simulations of high performance analog circuits. It has been shown that the noise due to thermal fluctuation in the transistor channel can be expressed as [16]

$$i_{\mathrm{n}}^2(f) = 4\gamma kT \frac{\mu_{\mathrm{eff}}}{L_{\mathrm{eff}}^2} Q_{\mathrm{N}}. \tag{2.9}$$

Here, Q_{N} is the total channel inversion charge and μ_{eff} is included to take mobility degradation into account, while L_{eff} is the effective electrical channel length of the device given by $L_{\mathrm{eff}} = L - \Delta L$. L is the channel length between the drain and the source, channel length minus drain and source lateral diffusions, and ΔL is the reduction in the electrical channel length due to the extension of the drain depletion region into the channel when $V_{\mathrm{ds}} > V_{\mathrm{dsat}}$.

Hence, it is clear from (2.9) that channel length modulation will result in an increase in the thermal noise as the effective electrical length becomes smaller and bias–dependent. Again, this can also be modeled in (2.8) by using a larger value for γ.

6 Shot Noise

When the transistor is operating in the subthreshold region, shot noise usually dominates over thermal noise. Shot noise was first studied using vacuum–tube diodes [17], but also occurs in pn junctions. This noise is present because the dc bias current is not continuous and smooth, but instead is a result of pulses of current caused by the individual flow of carriers (electrons and holes). As such, shot noise is dependent on the dc bias current. The shot noise drain current can be found as [18]

$$i_{\mathrm{n}}^2(f) = 2qI_{\mathrm{ds}} \tag{2.10}$$

where q is the electron charge and I_{ds} is the net drain current. In the subthreshold region, the drain current is dominated by diffusion mechanism, thus the shot noise in (2.10) can be rewritten as [19]

$$i_{\mathrm{n}}^2(f) = 2kT\nu g_{\mathrm{m}}, \tag{2.11}$$

where $\nu = (g_\mathrm{m} + g_\mathrm{mb})/g_\mathrm{m} \approx 1.5$. Therefore, the shot noise in a subthreshold MOS transistor can be comparable to the thermal noise in a standard superthreshold design, when both transistors have identical g_m values.

7 Flicker Noise

Low frequency noise is normally dominated by flicker noise in MOSFETs, and can in result in reduced sensitivity in many low frequency applications. It is now widely believed that $1/f$ noise in a MOSFET is due to traps in the gate oxide [20], [21].

As flicker noise is inversely proportional to the frequency, it becomes a dominating noise source at low frequencies. The flicker noise is usually described by its corner frequency, which is defined as the frequency where the flicker noise equals the channel thermal noise. For many analog circuits it is desirable to use large–sized transistors so that their corner frequencies are lower than the signal band.

The $1/f$ gate–referred noise voltage can be found as

$$v_\mathrm{n}^2(f) = \frac{K_\mathrm{f}}{WLC_\mathrm{ox}^2 f^\alpha}, \tag{2.12}$$

where K_f is a process and bias dependent parameter and α is a correction factor. The correction factor α is included to adjust for deviations from a $1/f$ line.
Depending on technology node and transistor area, flicker noise can contribute significantly to the total noise, even in the frequency band of interest for piezoelectric transducers, which stretches from 3.5 MHz to about 10 MHz.

A p-channel transistor model is shown in Figure 2.3, where channel thermal noise and flicker noise is included.

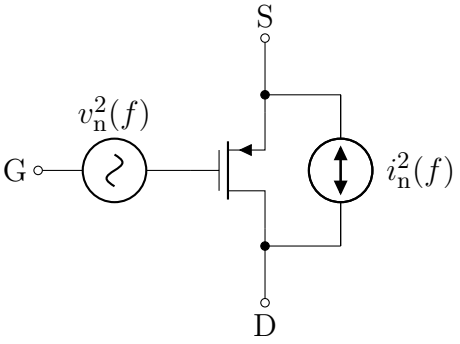

Figure 2.3: A p–channel transistor with noise sources.

If the transistor is operating above subthreshold, the white noise generator $i_\mathrm{n}^2(f)$ is modeling the thermal noise in the transistor. On the other hand, if the transistor is operating in subthreshold, $i_\mathrm{n}^2(f)$ represents the shot noise, which is the resulting dominating white noise source.

Chapter 3

Ultrasound Front–End Electronics

This chapter presents an overview of front–end electronics for medical ultrasound imaging, with emphasis on the low noise amplifier and implementation of variable gain, typically referred to as time gain compensation (TGC). Furthermore, this chapter will try to show the trade–offs for ultrasound front–end circuits by starting from a high–level system overview, followed by a more detailed description of how ultrasound systems work. Clearly, some system level understanding is necessary to fully appreciate the desired front–end integrated circuit (IC) function and performance.

1 Systems Overview

In ultrasound front–ends, as in many other high quality receivers, the analog signal processing components are key in determining the overall performance of the system; once noise and distortion have been introduced to the input signal it is essentially impossible to compensate for the effect of them.

Figure 3.1 shows a simplified diagram of an ultrasound system. In most systems the transducer element is connected to the end of a relatively long cable of about 2 m. In traditional ultrasound, this cable has from a minimum of 48 and up to 256 micro–coaxial cables, and is usually one of the most expensive parts of the system. For 3–D ultrasound, the number of channels increases dramatically, and the number of cables can typically not be correspondingly large. In traditional systems the transducer elements directly drive the cable, which can result in significant signal loss due to the loading of the cable capacitance on the transducer elements. Unfortunately, this in turn demands that the receiver noise figure (NF) is lower by the amount of the cable loss. The loss is typically on the order of 1–3 dB depending on transducer and operating frequency. In most systems multiple probe heads can be connected to the system, this allows the operator to select the appropriate transducer for optimal imaging. The heads are selected via high voltage relays; these relays introduce a large parasitic capacitance in addition to the cable.

A high voltage mux/demux is used in some arrays to reduce the complexity of transmit and receive hardware at the expense of flexibility. The most flexible systems are phased array digital beamforming systems where all transducer elements can be individually phase and amplitude controlled. These also tend to be the most

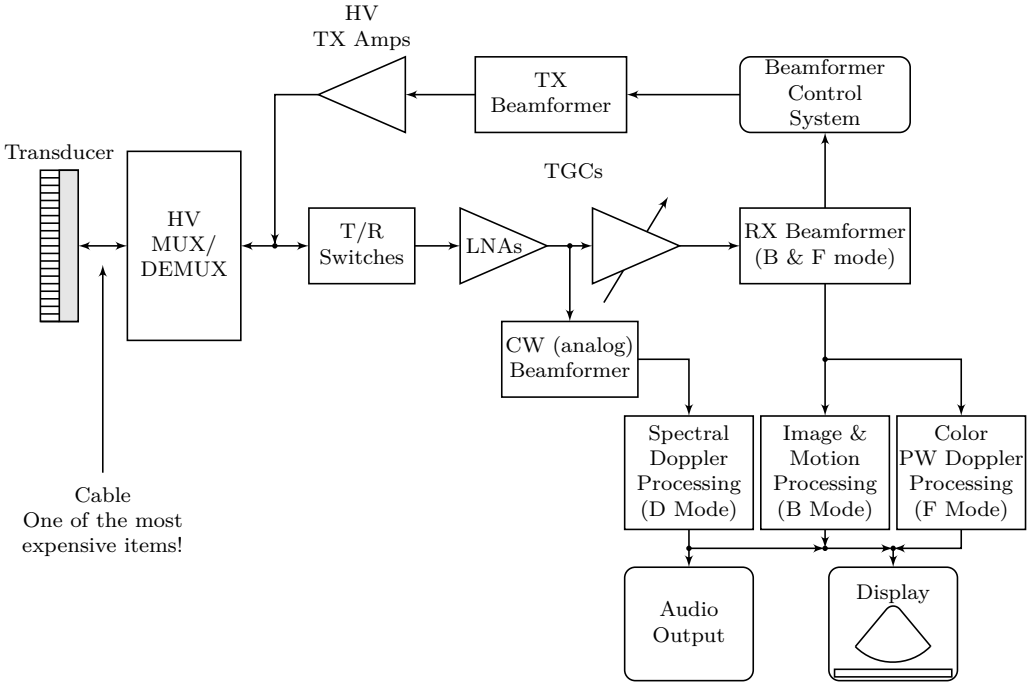

Figure 3.1: Receiver system for ultrasound diagnostics.

expensive systems due to the need for full electronic control of all channels.

On the transmit side the Tx beamformer determines the delay pattern and pulse train that set the desired transmit focal point. The outputs of the beamformer are then amplified by high voltage transmit amplifiers that drive the transducers. These amplifiers might be controlled by DACs to shape the transmit pulses for better energy delivery to the transducer elements. Typically multiple transmit focal regions (zones) are used, i.e. the field to be imaged is divided up by focusing the transmit energy at progressively deeper points in the body. The main reason for doing this is to increase the transmit energy for points that are deeper in the body because the signal is heavily attenuated as it travels into the body.

On the receive side there is a transmit/receive switch, generally a diode bridge, which blocks the high transmit voltage pulses, followed by a low noise amplifier and variable gain amplifiers which implement the time gain compensation and sometimes also apodization functions; spatial windowing to reduce sidelobes in beam. TGC is under operator control and used to maintain image uniformity. After amplification, beamforming is performed which can be implemented in analog (ABF) or digital (DBF) form. Digital beamforming is usually preferred in modern systems except for continuous wave (CW) Doppler processing whose dynamic range is mostly too large to be processed through the same channel as the image. Finally, the Rx beams are processed to show either a gray scale image, color flow overlay on the 2–D image, and/or a Doppler output.

2 Practical Front–End Circuit Considerations

In order to achieve an optimal transducer interface it is necessary to discuss the type of transducers first. Most relevant for this application is the 2–D array transducer. On the other hand, the designed amplifier is versatile enough to be with most transducer array types.

Linear Array: The shape of the transducer is determining the image shape. For example, if the array is convex, then the image generated will be a sector just like in a phased array.

Phased Array: The main advantages of phased arrays are full electronic steering of the beam and small size. This makes it the predominant transducer in cardiac imaging since a small transducer probe is required to image in between the ribs. The sector format is the optimal solution in cardiac imaging since the heart is far away from the surface and the beams all bundle near the skin, which makes them fit easily between the ribs. However, as pointed out earlier, the linear and phased array technology can be mixed and used to generate compound linear scans.

2–D Array: Theoretically the most versatile transducer since no mechanical motion of the transducer is required to scan a volume if a phased array approach is used. The biggest drawback of the 2–D array is that the complexity is proportional to N^2 compared to a linear array with N elements. Some systems use mechanical motion to generate a volumetric image or use 1.25–D or 1.5–D arrays; these sub–2D electronic arrays reduce complexity by restricting beam steering to only the lateral plane. Another major challenge is also the need for much larger cables to access the additional elements. The cable is one of the most expensive items in an ultrasound system, and they become very stiff and unwieldy for 256 and more micro–coax cables. Because of this, high voltage multiplexers could be used in the transducer handle to reduce the number of cables.

Annular Array: This type of array allows for 2–D focusing, but no beam steering. With this type of array it is possible to focus both in the lateral and elevation plane and produce a circular symmetrical beam. The focal point is determined, just like in the phased or linear array, by the delay pattern to the circular elements. As already mentioned above under 2–D arrays, a 1.25–D or 1.5–D array can be built which allows 2–D focusing but only 1–D beam steering. Full explanation of this technology is, however, beyond the scope of this thesis.

Figure 3.2 [22] shows a simplified equivalent circuit of an ultrasound front–end at series resonance of the transducer element. Figure 3.2 represents the electrical equivalent of the transmitter. A high voltage pulse is generated on the left side by a source with 50 Ω source impedance. This pulse is typically transmitted to the transducer element via a few meter micro–coaxial cable. A capacitor and resistor represent the electrical equivalent for the transducer. The resistor, R_{m}, is the electrical equivalent of the transducer plus body resistance. This resistor is real

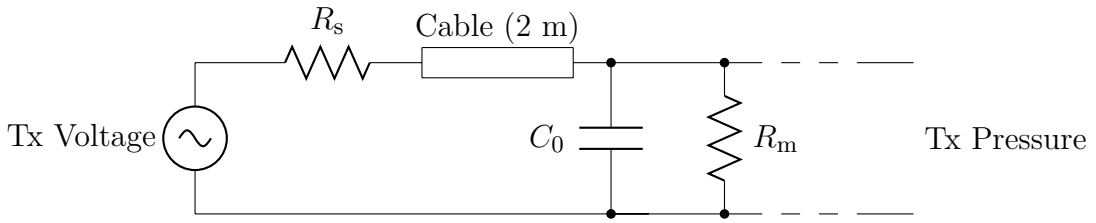

Figure 3.2: Simplified equivalent circuit of ultrasound transmitter.

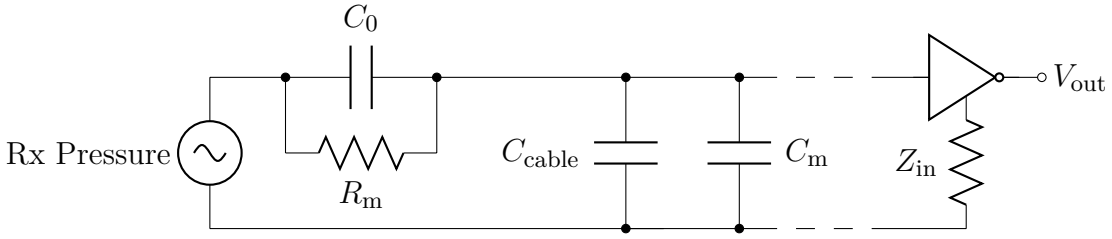

Figure 3.3: Simplified equivalent circuit of ultrasound receiver.

and therefore noisy; ideally this resistor should limit the noise performance in an ultrasound system. During transmit, the transducer element converts the electrical energy into acoustic pressure. Figure 3.3 represents the electrical equivalent of the receiver. Acoustic pressure is converted into electrical signals by the transducer. C_{cable} loads the transducer which normally is tuned out with an inductor, but since this is a narrow band solution and the ultrasound signals are broadband bandpass signals, a resistor is needed to de–Q the tuning resonator formed by C_{cable} and the inductor. This can done with a resistive input preamplifier to minimize the degradation in receiver noise figure (NF), as using a shunt termination at the input of the low noise amplifier will result in suboptimal noise performance. However, if the cable capacitance does not need to be tuned out then it is best to not set the input resistance of the low noise amplifier as this tends to degrade the noise performance.

3 Transducer Elements

Transducer impedances can vary from less than 50 Ω to 32 kΩ for single element and 2–D transducers respectively. Single element transducers has more latitude in designing the transducer, this allows for customized impedances. In array transducers spacing between the elements is important to minimize grating lobes, therefore the spacing needs to be less than $\lambda/2$, i.e. 250 µm at 3 MHz [2]. In addition, ultrasound is a coherent imaging modality; therefore optical artifacts like grating lobes due to diffraction are present. Grating lobes are a problem as they generate gain away from the main beam; if a strong undesired signal is coming along the direction of the grating lobe it could mask a weak signal along the main lobe. The main effects are ghost images and reduced SNR in the main image. The lateral size restriction makes it more difficult to design low impedance transducers; this problem gets compounded in 2–D arrays due to the size restriction in the elevation

plane in addition to the lateral plane. Lastly, as the transducer frequency increases, the wavelength and consequently the area decrease, which results in an increase in element impedance (reduction in capacitance; increase in resistance).

Increased transducer element impedances have the strong disadvantage that it becomes ever more difficult to drive the cable directly. I.e., a typical 2 m cable might have a capacitance of 200 pF, while a transducer element could have capacitance on the order of 5 pF. This makes for a large capacitive attenuator; there are only a few possible solutions: (1) try to reduce the element impedance; (2) integrate parts of the front–end in the transducer handle; (3) use a more sensitive LNA in the system. Solution (1) is difficult to achieve for 2–D transducer arrays. The usefulness of (3) is also limited as the noise factor of any LNA is always larger than 0 dB. Solution (2) would be ideal, but it brings with it many problems like: how to protect the front–end amplifiers from the high voltage transmit pulses. Due to health regulations, the temperature of the transducer probe is strictly limited, which makes for a very limited power consumption, especially for 2–D arrays where the channel count can be very high. Also, the small transducer dimensions may result in difficult area constraints.

4 Variable Gain

Automatic gain control (AGC) circuits are most often used in audio and video mixed–signal ICs in order to maximize the dynamic range of the overall system. The specifications for the linearity of the analog variable–gain amplifier (VGA) forming the core of these circuits are generally very high, to prevent limiting of the overall harmonic distortion by the AGC itself. In ultrasound applications, variable gain is typically used to compensate for the increased loss as the wave propagates through tissue. Received signals arising from increasing depth, or increasing time, suffer more attenuation, and as a result the signal amplitude rapidly diminishes. This can partially be compensated for by increasing the gain with time. This technique, also known as swept gain or time–gain compensation (TGC), can result in dramatic improvements in the image quality [23].

The time gain compensation amplifier is a crucial link in the ultrasound signal path. It must have the ability to amplify signals ranging from a few microvolts to several millivolts up to one or two volts for the ADC. This gain will be exponentially increased along each transmit/receive sweep line. At the near end of the wedge, the gain will be very low. It will have to process the return signal right after the high voltage ceramic excitation pulse. As time after the excitation pulse passes, the gain will be swept into very high levels. This must be done while maintaining very low noise to avoid masking low level signal coming from deep within the body.

5 Dynamic Range

In the front–end circuitry, the noise floor of the LNA determines how weak a signal can be received. But at the same time—especially during CW Doppler signal processing—the LNA must also be able to handle very large signals. So it is crucial

to maximize the dynamic range of the LNA. In general, it is extremely difficult to implement any filtering before the LNA due to noise constraints.

CW Doppler has the largest dynamic range of all signals in an ultrasound system– during CW, a sine wave is transmitted continuously with half of the transducer array, while the other half is receiving. There is a strong tendency for the Tx signal to leak into the Rx side; and there are also strong reflections coming from stationary body parts that are close to the surface. This tends to interfere with examination of, for example, blood flow in a vein deep in the body with concomitant very weak Doppler signals.

At the current state of the art, CW Doppler signals cannot be processed through the main imaging (B-mode) and PW Doppler (F–mode) path in a digital beamforming (DBF) system. As the ABF has larger dynamic range, it has to be used for continuous wave Doppler processing. Naturally, the goal in digital beamforming ultrasound is for all modes to be processed through the digital beamforming chain at realistic cost, and there is a great deal of ongoing research as to how to get there.

6 Power Consumption

Since ultrasound systems require many channels, power consumption of all the front–end components—from T/R switch, through LNA, VGA, and ADC, to the digital circuitry of the beamformer—is a very critical specification. As has been pointed out above, there will always be a push to increase the front-end dynamic range in order to arrive at eventual integration of all ultrasound modes into one beamformer—a tendency that will lead towards increasing the power in the system. However, there is a corresponding need to make the ultrasound systems forever smaller—with a tendency towards reducing power. Power in digital circuits usually decreases with supply voltage; but this is not necessarily true for analog and mixed signal circuitry. Furthermore, taking into account the fact that reduced analog «headroom» tends to reduce dynamic range, there will be a limit to how low the supply voltage can go and still achieve a desired dynamic range.

Chapter 4

In–Probe Analog Front–End

This chapter motivates the need of integrating parts of the front–end in the probe handle, especially in terms of placing the analog to digital converter as close to the transducer as possible. Unfortunately, the large dynamic range requirement inherent in most ultrasound modalities, especially continuous wave doppler processing, makes for a very power hungry ADC specification. By compressing the dynamic range using a variable gain amplifier, the requirement for the ADC can be relaxed. In addition, the front–end amplifier can match the single–ended transducer to a differential ADC by employing a single–ended to fully balanced amplifier topology. Due to the high switching activity in the transducer probe, with a corresponding level of switching noise, the need for a fully balanced ADC architecture is present even for 7/8 bits of accuracy.

1 Analog versus Digital Power Consumption

For 3–D ultrasound systems with several thousand channels and a total power budget in the milliwatt region, the available power per channel can be as little as a few tens of micro watt. Hence, for in–probe electronics, low power consumption is the first constraint, for which speed and dynamic range have to be sacrificed for. Although integrating the analog front–end in the probe handle can lead to improved image quality and flexibility, it is still necessary to maintain a certain performance in terms of bandwidth and dynamic range, but with stringent requirements on low power. It is therefore relevant to investigate the fundamental lower limits and how they can be reached.

In analog circuits, the absolute limit comes from the need to maintain the energy of the signal much larger than the thermal energy, to achieve the required signal to noise ratio S/N. This condition can be expressed as a minimum power per functional pole [24]

$$P_{\min} = 8kT(S/N)f, \tag{4.1}$$

where f is the signal frequency and S/N is the signal–to–noise ratio. Clearly, this fundamental limit does not depend on technology. It can be reached in a simple, passive RC filter, while the best existing active filters are still a few orders of

magnitude above. Also, it applies to amplifier stages with an additional margin proportional to their voltage gain. Obviously, this limit is steep since it corresponds to a 10–fold increase of power consumption for each 10 dB increase in signal–to–noise–ratio.

In digital systems, each elementary operation requires a certain number m of binary–gate transition cycles, each of which dissipates an amount of energy E_{tr}. The number m of transitions is only proportional to some power of the number of bits N_{bit}, and therefore power consumption is only weakly dependent on signal–to–noise ratio. In fact, the power consumption is essentially logarithmically dependent on signal–to–noise ratio for digital circuits, as can be seen in Figure 4.1 [25].

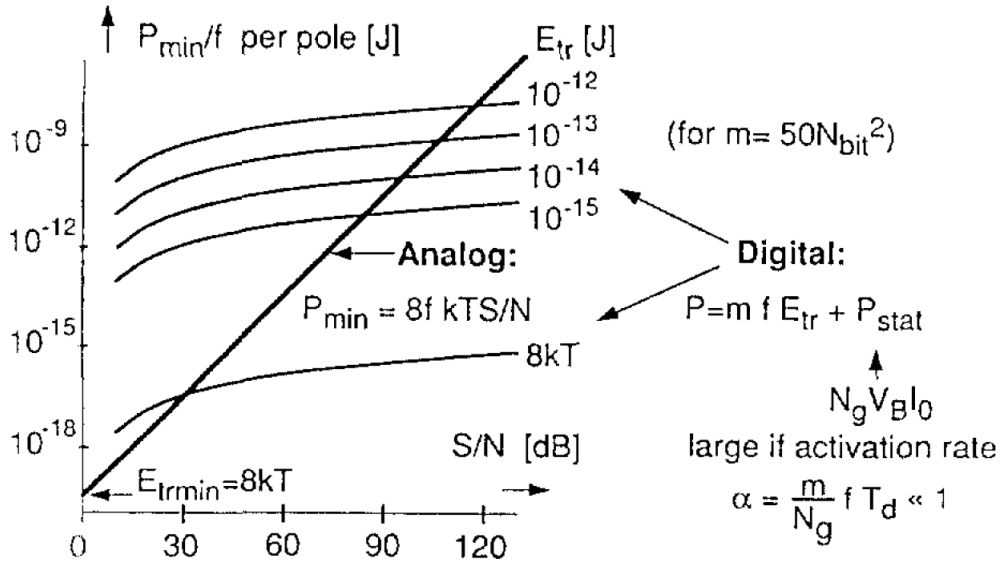

Figure 4.1: Analog and digital power consumption versus signal–to–noise ratio.

Comparison with analog power consumption is obtained by estimating the number of gate transitions required to compute each period of the signal, for example $m = 50N_{\mathrm{bit}}^2$. Immunity to thermal noise imposes an absolute minimum energy per transition E_{tnn} estimated at $8kT$, which provides the absolute minimum power limit.

From Figure 4.1 it is clear that for 10 to 12 bit accuracy after beamforming, digital signal processing can be done at a substantially lower power consumption, especially for digital circuits that approaches the fundamental lower limits. Also, increasing the number of bits after summation in the beamforming can be done quite easily in the digital domain.

2 Digital Beamforming ASICs

In the pursuit of even more flexible ultrasound systems, there is an ongoing need for integrating as much of the electronics, from the low noise amplifier to the ADC into the transducer probe. Digital beamforming can then be partially done in the front–end as well as in the main unit, which holds the promise of increasing sensitivity,

as the increase in signal–to–noise ratio in digital beamforming systems tends to be better than in corresponding analog beamforming systems. Figure 4.2 shows a

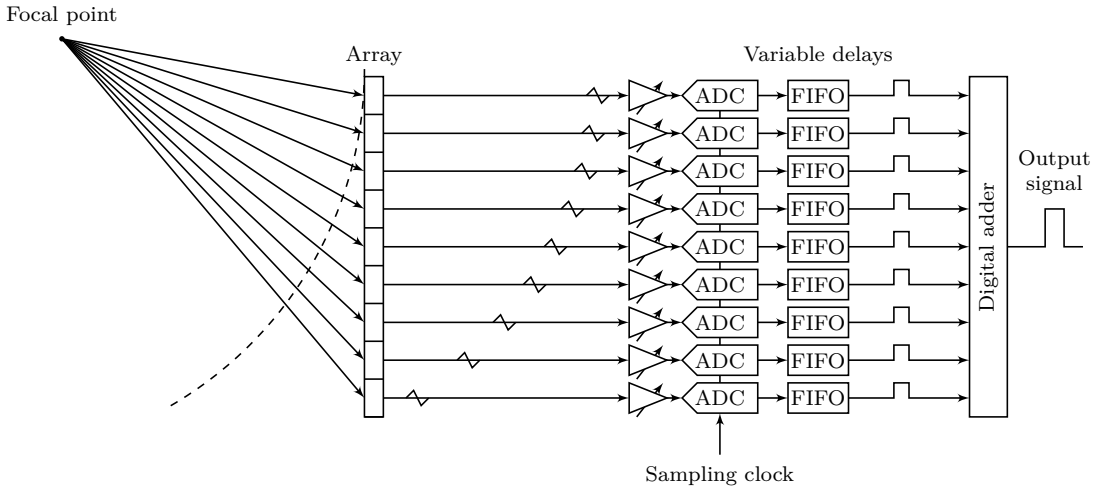

Figure 4.2: Digital Beamforming System.

basic block diagram of a digital beamforming system [26]. Note that a variable gain amplifier is typically needed in most implementations to reduce the dynamic range required for the ADC. In fact, doing some analog signal processing to compress the dynamic range before the A/D converter can relax the requirement significantly for the ADC, with a corresponding reduction in power consumption. For instance, increasing the resolution for a thermal noise limited ADC by 1 bit of resolution would require at least quadruple the power consumption. Clearly, for analog to digital converters and other analog building blocks, dynamic range is very expensive in terms of power consumption.

The main difference between an analog and digital beamforming system are the way the beamforming is done, both require perfect channel–to–channel matching. In analog beamforming, an analog delay line and summation is used, while in digital beamforming the signal is sampled as close to the transducer elements as possible and then the signals are delayed and summed digitally. In analog and digital beamforming ultrasound systems, the received pulses from a particular focal point are stored for each channel and then lined up and coherently summed; this provides spatial processing gain because the noise of the channels are uncorrelated. Note that in an analog beamforming imaging system, only one very high resolution and high speed ADC is needed, while in a digital beamforming system many high speed and high resolution analog to digital converters are needed. Sometimes a logarithmic amplifier is used in the analog beamforming systems to compress the dynamic range before the analog to digital converter.

Digital beamforming has the principle advantage that once data is acquired, digital storage and summing is ideal, i.e. in the digital domain the channel–to–channel matching is perfect, while analog delay lines tend to be poorly matched. This reduces the spatial processing gain, as the signal is not ideally, coherently added. The number of delay taps in analog delay tends to be limited, which determines the resolution. Therefore, fine adjustment circuitry normally needs to be used. In

contrast, digital memory is cheap, therefore the FIFOs can be very deep and allow for fine delay resolution. Unfortunately, the sampling rate of the analog to digital converter directly influences axial resolution and accuracy of phase delay adjustment channel–to–channel. Ideally, analog to digital converters with above 200 MS/s would be used to get fine delay resolution [27]. However, because it is difficult to get analog to digital converters with low enough power and high enough resolution for those speeds, most systems use digital interpolation in the beamforming ASICs instead.

Digital beamforming also holds the possibility of increasing flexibility, for instance by forming multiple beams by summing data from different locations in the FIFOs. As the digital IC performance continues to improve, even more flexible ultrasound systems can be implemented. Ideally, systems can be differentiated through software only.

3 Front–End Architecture

As indicated in Figure 4.2, a low noise amplifier is needed in front of the A/D converter. In addition, variable gain is required, either in the low noise amplifier or in a separate stage before the ADC. Also, a single–ended to differential converter is necessary, which usually adds the requirement for some common–mode feedback circuitry in the amplifier. All this should be implemented with as little power and area overhead as possible due to the high number of channels in a relatively small and power constrained probe handle. For this reason, the analog front–end should be as simple as possible, while incorporating all the required functionality.

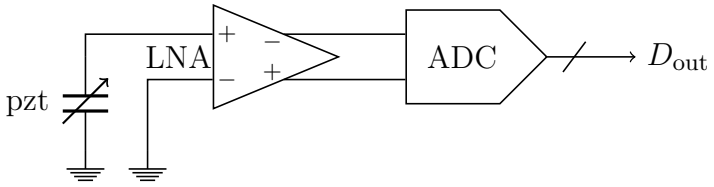

Figure 4.3: Proposed analog front–end including LNA and ADC.

A proposed front–end architecture is shown in Figure 4.3. Here, the low noise amplifier acts as a single–ended to differential converter and interfaces the ADC. Unfortunately, implementing a variable gain amplifier compensating for the large attenuation as the ultrasound wave propagates trough tissue would require a gain range of several tens of decibel. This might be difficult to achieve in a micro power front–end such as this. On the other hand, by employing the vast computational power of digital signal processing, time gain compensation can be done at lower cost after the analog to digital converter, or in the main unit where power consumption is not critical.[1] In fact, by means of digital filtering, more advanced time gain compensation can be implemented to improve image quality. Traditionally, time gain compensation is done by increasing gain with

[1] Of course, with the introduction of hand held ultrasound systems, this might not be the case.

depth in a frequency independent manner. However, it is well–known that higher frequency components are attenuated more than lower ones, a difference which is progressively increasing with depth. Frequency dependent attenuation implies that echoes from large depths contain essentially the lower frequencies of the transmitted pulse [28], [29]. Clearly, the loss of higher frequency components at higher depths will deteriorate the resolution, as resolution is intimately related to the frequency content of the signal. In fact, by performing time varying and frequency dependent, digital filtering of the received signal, an improvement in image quality can be achieved [30]. However, the improvement in resolution using frequency dependent compensation is most considerable when the signal-to–noise ratio in the received signal is high. Nevertheless, the low noise amplifier still has to limit the dynamic range of the signal before it is sampled by the analog to digital converter.

4 Piezoelectric Transducers

In order to derive accurate front–end specifications it is essential to have some knowledge about the electrical properties of the piezoelectric transducer. Figure 4.4 shows the electrical equivalent of the piezoelectric transducer on receive linearized around it operating point [31].

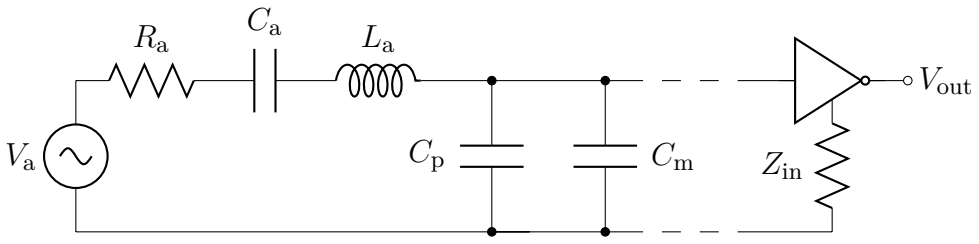

Figure 4.4: Small–signal equivalent of the piezoelectric transducer.

The left part of the equivalent circuit represents the acoustical part of the piezoelectric transducer with body resistance, while the capacitor C_p represents the electrical port of the transducer. At the resonance frequency $f_0 = 7\,\text{MHz}$, the equivalent circuit reduces to R_a in parallel with C_p.

Unfortunately, only these two parameters are known for the piezoelectric transducer at hand. On the other side, knowing the impedance at resonance can be used to derive the noise figure for the front–end amplifier. In addition, the required input impedance of the front–end can be found by using the impedance level of the transducer at resonance. 2–D transducer are typically limited in size, which makes for a large impedance source, i.e. large body resistance and small capacitance. In fact, the body resistance is as high as $32\,\text{k}\Omega$ and the intrinsic capacitance is in the region of $450\,\text{fF}$. The principle advantage of having such a large body resistance is the corresponding high noise levels, which lead to relaxed noise requirements for the analog front–end.

5 Voltage Sampling

For this low noise amplifier a voltage gain of 20 dBis required in order to raise the weak signal from the piezoelectric transducer above the noise floor of the A/D converter. On the other hand, the output voltage of the front–end amplifier should be limited in order to avoid saturation in the ADC.

For optimal power transfer from the source to the amplifier, the source impedance should be matched to the input impedance of the low noise amplifier. However, the received pulses from the transducer elements are voltage signals, and for efficient voltage sampling a very high input impedance results in a favorable voltage division

$$V_{\text{in}} = V_{\text{s}} \cdot \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{s}}}, \tag{4.2}$$

where V_{s} is the source signal, sensed by the receiver as V_{in}. Moreover, R_{in} is the input resistance of the receiver and R_{s} is the source resistance.

This voltage division can be calculated using the given electrical and body resistance of the transducer elements of 32 kΩ. Clearly, for optimal sensitivity for voltage sampling, the input resistance of the amplifier should be much larger than the source resistance. In addition, the input capacitance of the low noise amplifier should be kept much smaller than the source capacitance, in order to minimize any addition attenuation of the voltage signal at the input of the low noise amplifier.

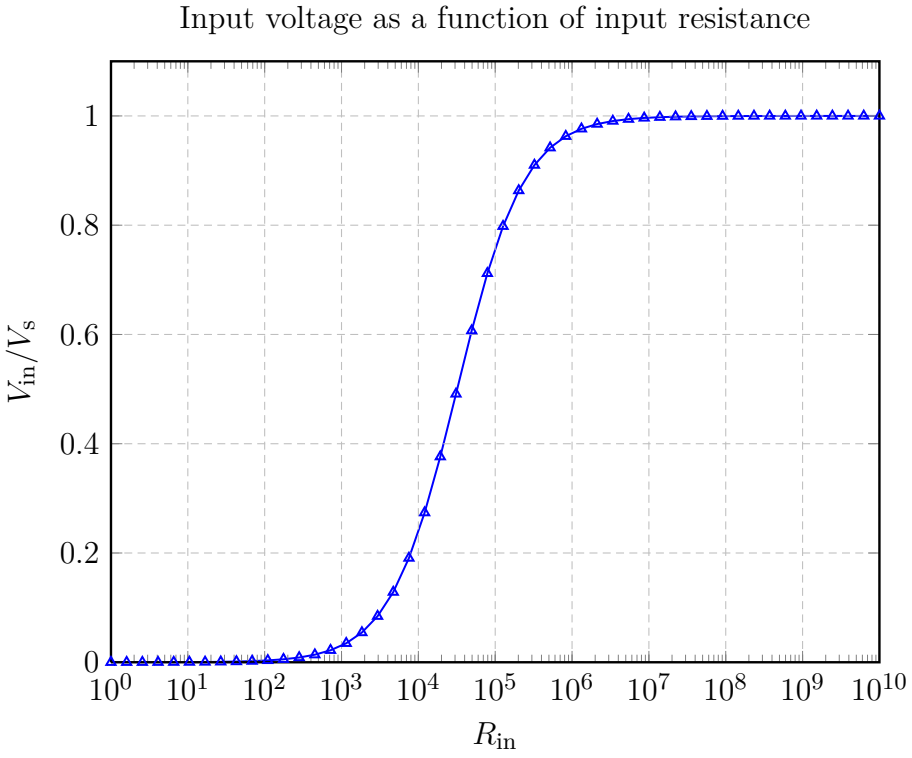

Figure 4.5: Effect of input resistance, i.e. the real part of Z_{in}, on the circuit performance.

From Figure 4.5 it is clear that when using voltage sensing, the input resistance of the amplifier must be in the range of several mega ohms in order to be sufficiently

high to cause minimum attenuation of the pzt voltage signal at the input of the amplifier. For higher values of the input resistance, the overall transfer function has minimal sensitivity to the input resistance variations. Such a high input resistance is usually obtained by connecting the source to the gate of a mos transistor.

6 Single–Ended to Differential Conversion

The single–ended to fully differential converter is an important building block in many applications, mostly caused by the need to match single–ended sources to processing blocks that features a fully balanced architecture. These fully balanced architectures have many benefits as compared to their single–ended counterparts in terms of lower sensitivity to substrate noise and saturated output levels. The last point is especially important for scaled down technology nodes where the supply voltages are reduced to 1 V and below. The single–ended to differential converter usually has to provide symmetric outputs, high tolerance to input dc–level variations and a wide bandwidth.

Symmetrical single–ended to differential converters are typically based on the differential pair, and in the simplest case only consists of a simple differential pair driven by a single input, where the second input is ac–grounded [32], [33], [34].

By using this configuration, also known as a single input differential pair, half of the input signal is seen as a common–mode input component. As a result, this topology provides 6 dB lower gain and lower common–mode rejection ratio when compared to the fully differential input case.

Other arrangements exists that can improve the efficiency of the circuit [35], [36], but this comes at the cost of increased complexity and possible stability problems caused by the use of a positive feedback path. In addition, the positive feedback provides a very low common–mode rejection ratio. Similarly, negative feedback can be used to generate the second input [37], thus alleviating some of the potential instability problem.

Chapter 5

Circuit Topology

Having reviewed the fundamental properties of ultrasound imaging and the transducer source itself, this chapter focus on the chosen amplifier topology. The proposed front–end architecture imposes challenges on the low noise amplifier, such as maintaining high input resistance as well as implementing a single–ended to differential conversion at a low power consumption and input referred noise voltage. In addition, the dynamic range requirement is also high, especially for maintaining good linearity even at large input levels. The chosen amplifier is therefore based on the differential pair with additional circuitry to maintain good linearity without investing too much power.

1 Linearized Transconductor

As mentioned in Chapter 2, a simple way of linearizing a differential pair is by means of resistive degeneration. By using a degeneration resistance at the source of the differential pair, the bias current can be made relatively independent on the input signal.

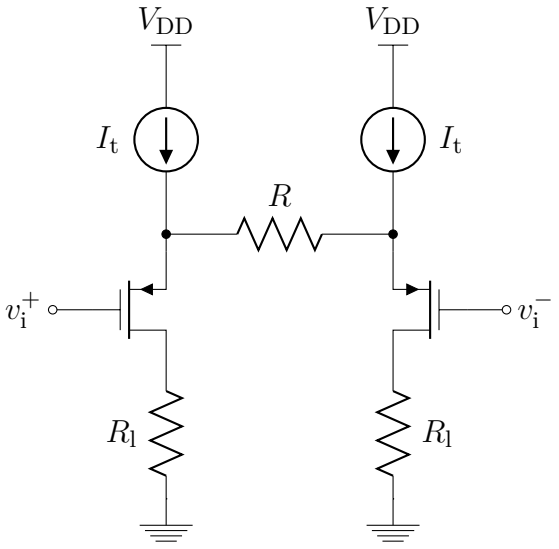

Figure 5.1: Differential pair using resistive degeneration.

If the transconductance of the input transistor is g_m, the transconductance by using resistive source degeneration will be given by

$$G_\mathrm{m} = \frac{g_\mathrm{m}}{1 + g_\mathrm{m} R}, \tag{5.1}$$

where the degeneration resistor has a value of R. Clearly, the source degeneration resistance results in an internal, negative feedback loop that linearizes the transconductance of the amplifier. If the feedback factor, $g_\mathrm{m} R$, is much larger than unity, the overall transconductance is given by the $1/R$, an input independent factor. By having $g_\mathrm{m} R \gg 1$, only a small portion of the input voltage lies across the active devices, implying reduced signal swing and distortion. The requirement $g_\mathrm{m} \gg 1/R$ can usually be satisfied with large transistors widths and/or bias currents. In many practical application however, this may be very undesirable in terms of area and current consumption.

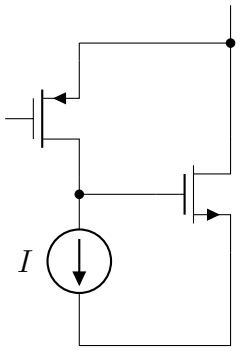

Figure 5.2: P–channel input transistor with composite device.

An alternative way is to boost the g_m of the p–channel device by using a compound device as shown in Figure 5.2 [4]. This compound configuration is often used in the design of many bipolar output stages instead of a single p–n–p transistor with poor performance. In this case, M_1 acts like a floating voltage source. Its g_m is no longer an important factor in the distortion performance of the amplifier. However, any threshold voltage shift due to the body effect becomes part of the input signal. For this reason, p–channel input transistors were chosen for the n–well process, in which the body effect can be minimized by connecting the source of each input transistor to its own well. Also, p–channel devices tend to be less noisy than n-channel devices, especially when flicker noise is concerned. To complement the design, n–channel current mirrors can be used that have better frequency response than p–channel current mirrors, which would have been used with n–channel input devices.

A basic transconductor with the compound devices and biasing is shown in Figure 5.3. The p–channel transistors serve as voltage followers buffering the input voltage across the resistor while the four constant current sources force any change in the resistor current to be directly reflected to the drain currents of $M_{2\mathrm{a}}$ and $M_{2\mathrm{b}}$, which is mirrored to the output by M_3 and M_3'. The local feedback loop of M_1 and M_2, therefore creates an input device with a high effective g_m. Therefore, the effective G_m of the input transconductor circuit is set by the resistor, R, which provides degeneration between the two input devices and by the mirroring ratio,

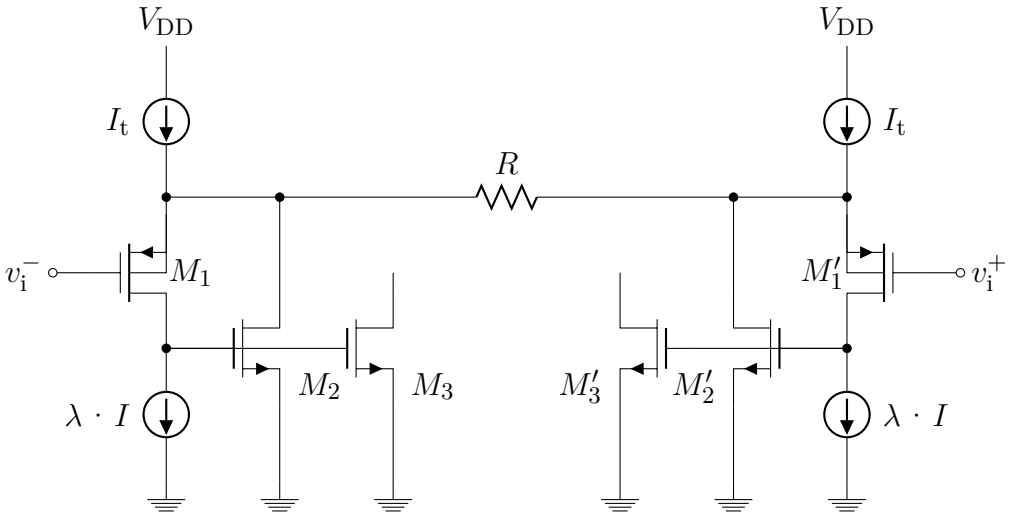

Figure 5.3: Basic transconductor cell.

B, between M_2 and M_3. This not only provides a fixed transconductance that is largely insensitive to process variation, but it also linearizes the transconductance of the circuit.

2 Simplified Amplifier Topology

The usefulness of analytical analysis of the amplifier is limited by the complexity of the resulting equations. In addition, using simple circuit topologies increases the possibility of finding useful analytical expressions. In order to simplify complexity and design effort, only the core of the transconductor is designed. The output stage consisting of the current mirror of M_3 can be designed as a separate second stage. In fact, having a large gain in the first stage, will result in a neglectable noise contribution from the output stage. For the first stage, the output voltage can be found at the gate of M_2. The simplified amplifier topology is shown in Figure 5.4. The loading of M_3 on M_2 is modeled by a load capacitance of 25 fF.

Optimizing the core of the amplifier also constitutes the major design effort. As long as M_2 has been designed, the output transistor determines out current by a current mirror of B. The geometry of M_3 is therefore given, and the current mirror gain is realized using an appropriate M factor. Depending on the type of output that is desired, the output stage can simply consist of M_3 if a current output is required, or by adding a resistive load if a voltage output is necessary.

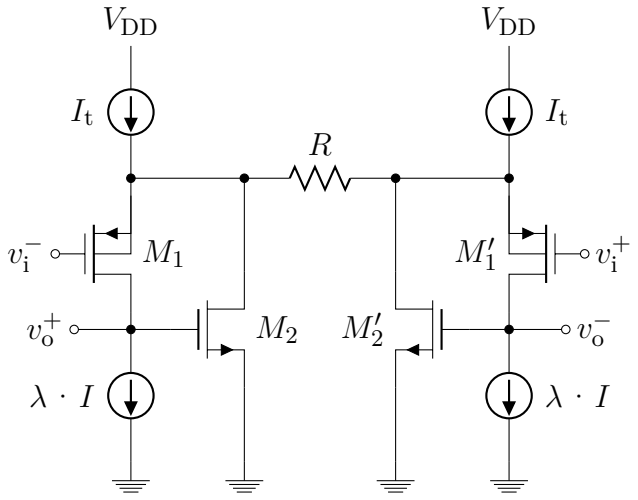

Figure 5.4: Simplified Low Noise Amplifier Topology

3 Small–Signal Analysis

In order to fully appreciate the functionality of the amplifier topology, consider the small–signal equivalent circuit of the amplifier shown in Figure 5.3. To simplify the analysis, only the half–circuit equivalent is used for the calculations. Also, the transistors are modeled as ideal transconductors.

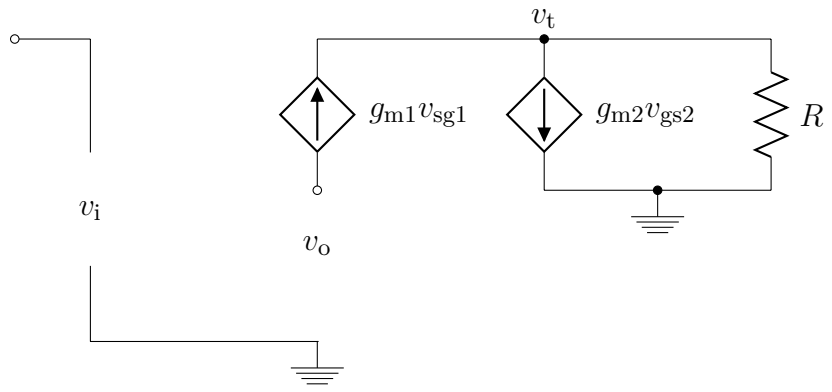

Figure 5.5: Low frequency small–signal equivalent circuit.

The ideal current source, forces any current change in the resistor to be reflected to the drain of the feedback transistor M_2. Summing all the currents at v_t yields

$$g_m(v_t - v_i) + g_{m2} \cdot v_o + 2G \cdot v_t = 0 \tag{5.2}$$

Since the small–signal current through M_1 is forced to be zero, the input voltage is buffered over the degeneration resistor, and $v_i = v_t$, where v_t is the node voltage indicated in Figure 5.5. The current through R is forced through M_2, so

$$g_{m2} \cdot v_o + 2G \cdot v_i = 0 \tag{5.3}$$

where, $G = 1/R$. Solving (5.3) yields the voltage gain A

$$A \triangleq \frac{v_\mathrm{o}}{v_\mathrm{i}} = -\frac{2G}{g_\mathrm{m2}}. \tag{5.4}$$

Unfortunately, the gain in (5.4) is not well–defined across process corners and temperature variations; however, this is also the case for a range of other analog circuits, such as active RC–filters and integrators used in continuous–time $\Delta\Sigma$–modulators. Also, for the complete amplifier, the voltage gain will be given by the ratio of two resistors, which can be matched quite well in CMOS.

4 Source–Follower

In the previous analysis using ideal current sources, the input transistors will behave as ideal source-followers. However, when including non–ideal current sources and resistive loading through the degeneration resistor, the gain in the voltage buffer will decrease from the desired value of one. For the source follower M_1 with output resistance r_ds1, transconductance g_m1 and a resistive load of $R/2$, the voltage gain is given by

$$A_1 \triangleq \frac{v_\mathrm{t}}{v_\mathrm{i}} = \frac{g_\mathrm{m1} \cdot r_\mathrm{ds1}}{1 + (g_\mathrm{m1} + g_\mathrm{mb1}) \cdot r_\mathrm{ds1} + 2 \cdot r_\mathrm{ds1}/R}, \tag{5.5}$$

when taking the body effect into account. This reduces to the well–known expression when the load and output resistance approaches infinity

$$\lim_{R,\, r_\mathrm{ds1} \to \infty} A_1 = \frac{g_\mathrm{m1}}{g_\mathrm{m1} + g_\mathrm{mb1}}, \tag{5.6}$$

which is always less than unity. As previously mentioned, the body effect can be minimized by using p–channel input transistors, where the source can be connected to its own well. Not only will this lead to improved linearity, but also reduced attenuation in the voltage buffer. As can be seen from (5.6), the voltage buffer has a gain less than unity, regardless of output resistance and loading conditions as long as the body effect must be taken into account. On the other hand, this drawback is suppressed when minimizing the body effect. If the body effect is sufficiently small, equation (5.5) can be rewritten as

$$A_1' = \frac{g_\mathrm{m1} \cdot r_\mathrm{ds1}}{1 + g_\mathrm{m1} \cdot r_\mathrm{ds1} + 2 \cdot r_\mathrm{ds1}/R}, \tag{5.7}$$

where typically $r_\mathrm{ds1}/R \gg 1$. Hence, (5.7) can be simplified to

$$\hat{A}_1 = \frac{g_\mathrm{m1} R}{1 + g_\mathrm{m1} R}, \tag{5.8}$$

which implies that $g_\mathrm{m1}R$ should be larger than one by a at least a few times. Although, any loss in the signal path adds directly to the noise figure, some loss in the voltage buffer is acceptable. From (5.8) it is clear that the requirement $g_\mathrm{m1}R \gg 1$ is not completely removed when using g_m boosting.

In addition to the direct loss in the signal path, the overall voltage gain suffers additional loss due to the attenuation in the source follower. This can be seen

from (5.2) when $v_\mathrm{i} \neq v_\mathrm{t}$, but instead $v_\mathrm{t} = \hat{A}_1 v_\mathrm{i}$. The overall voltage gain can then be written as

$$\hat{A} = -\frac{2G}{g_\mathrm{m2}}\hat{A}_1 + \frac{g_\mathrm{m1}}{g_\mathrm{m2}}(1-\hat{A}_1). \tag{5.9}$$

Note the negative contribution from the second term as $\hat{A}_1$ is less than one. Clearly, the voltage gain in (5.9) suffers additional loss when $g_\mathrm{m1} > g_\mathrm{m2}$, which is typically the case for low noise applications. In fact, for optimal noise performance g_m1 should be larger than g_m2 by a few times, leading to a compromise between voltage gain and low noise. On the other hand, any loss from the input signal to the degeneration resistor results in reduced small–signal currents in M_2, which typically leads to relaxed linearity requirements.

5 Noise analysis

One of the key factors in designing power efficient analog circuits is understanding noise. For most low noise amplifies, noise factor is one of the most significant performance parameters, making a thorough noise analysis is vitally important for a successful design. It is therefore of interest to identify the most important noise contributors of this amplifier topology, and be able extract design equations for low noise.

6 Previously Published Noise Analysis

Even though this transconductor cell has received some attention in the literature, only a simplified noise analysis is included in [5], where the noise contribution from the input transistors are neglected. This is a good approximation if $g_\mathrm{m1} \gg 1/R$, a constraint that is not necessarily satisfied when using g_m boosting. Nevertheless, the input referred noise voltage is found as [5]

$$v_\mathrm{n}^2 = 8kT\gamma(g_\mathrm{mbp} + g_\mathrm{mbn} + g_\mathrm{m2})R^2 + 4kTR, \tag{5.10}$$

when assuming perfect matching for the two half–circuits. Here, g_mbp represents the transistor realizing the current source supplying I_t, while g_mbn corresponds to the transistor acting as the current source draining $\lambda \cdot I$. Also, as a simplification γ is assumed to have the same value for all the transistors.

Clues for minimizing the noise can be found in (5.10). Clearly, R has a significant impact on the noise performance and should therefore be as small as possible. On the other hand, R also determines the small–signal current in M_2 which cannot be larger than its bias current. Therefore, having a small value for R results in requiring a large bias current for M_2, reducing the obtained efficiency by boosting the g_m of the input transistors. In addition, having a larger g_m in the bias transistors and M_2 effectively decreases the noise performance. This however, has less impact on the total amplifier noise than reducing R, as the degeneration resistor has a significant, second order effect on the noise performance, which clearly can be seen in (5.10).

Obviously, g_{m} can be reduced with a fixed bias current by decreasing W/L for the relevant transistors.

7 Simplified Noise Analysis

Even though (5.10) provides some insight in how to improve the noise properties of this amplifier, it still suffers from the assumption that g_{m1} should be much larger than $1/R$. For low power applications, the value of g_{m} cannot be made arbitrarily large, while R is restricted both by the requirement for low noise and setting the voltage gain. Therefore, a noise analysis is required where the noise from M_1 is taken into account. At the same time, it is also clear from (5.10) that noise from the bias transistors acting as current sources can be made small by minimizing their g_{m} values. Clearly, the most important noise sources to be taken into consideration is M_1, M_2 and R.

First, consider the simplified small signal half–circuit equivalent shown in Figure 5.6. For the noise analysis, the noise contribution is modeled as a current source in parallel with the drain source of each transistor. First, the noise contribution from each transistor is found individually, before summing all contributions using the superposition principle. The input is set to zero, meaning that the gate voltage of the input transistor is at ground, unless any noise current forces it to have different value. The noise source I_{n} represents the noise from M_2 and all the other noise contributors in parallel with M_2, such as R and the bias transistors acting as current sources.

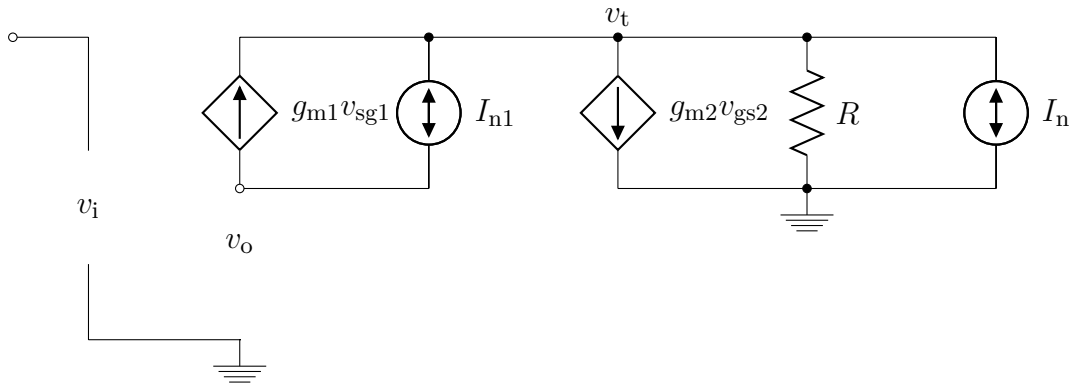

Figure 5.6: Low frequency small–signal equivalent circuit including noise source.

Clearly, due to the lack of any return path, the noise current from the input transistor can only circulate through the voltage–controlled current source of M_1 by forcing the node voltage at v_{t} to have the value v_{n}, given by

$$I_{\mathrm{n1}} = g_{\mathrm{m1}} \cdot v_{\mathrm{n1}}. \tag{5.11}$$

Similarly, the current through R is forced through M_2 as all the other noise sources are set to zero

$$g_{\mathrm{m2}} \cdot v_{\mathrm{o}} + G \cdot v_{\mathrm{n1}} = 0. \tag{5.12}$$

By using this expression, the output referred noise voltage can be found as

$$v_{\mathrm{o}}^2 = \left(\frac{I_{\mathrm{n1}}}{g_{\mathrm{m1}}}\right)^2 \left(\frac{G}{g_{\mathrm{m2}}}\right)^2. \tag{5.13}$$

The noise from M_2 can be found by summing all currents through v_{t}

$$g_{\mathrm{m1}} \cdot v_{\mathrm{t}} + g_{\mathrm{m2}} \cdot v_{\mathrm{o}} + G \cdot v_{\mathrm{t}} + I_{\mathrm{n2}} = 0 \tag{5.14}$$

Again, the small signal current trough M_1 is zero, which means that v_{t} is also zero. Essentially, the noise current of M_2 is therefore forced through its own voltage–controlled current source, which yields

$$v_{\mathrm{o}}^2 = \left(\frac{I_{\mathrm{n2}}}{g_{\mathrm{m2}}}\right)^2. \tag{5.15}$$

Similarly, the noise from R, I_{n3} can be found, as this noise source is in parallel with the noise source from M_2. This results in

$$v_{\mathrm{o}}^2 = \left(\frac{I_{\mathrm{n3}}}{g_{\mathrm{m2}}}\right)^2. \tag{5.16}$$

The total output referred noise voltage is found by superimposing all the contributions above

$$v_{\mathrm{o}}^2 = \left(\frac{I_{\mathrm{n1}}}{g_{\mathrm{m1}}}\right)^2 \left(\frac{G}{g_{\mathrm{m2}}}\right)^2 + \left(\frac{I_{\mathrm{n2}}}{g_{\mathrm{m2}}}\right)^2 + \left(\frac{I_{\mathrm{n3}}}{g_{\mathrm{m2}}}\right)^2. \tag{5.17}$$

Referring all the noise sources to the input

$$v_{\mathrm{n}}^2 = \left(\frac{I_{\mathrm{n1}}}{g_{\mathrm{m1}}}\right)^2 + \left(\frac{1}{G}\right)^2 \left[(I_{\mathrm{n2}})^2 + (I_{\mathrm{n3}})^2\right]. \tag{5.18}$$

Now, inserting for the noise sources given by (2.8), yields

$$v_{\mathrm{n}}^2 = 4kT\gamma \frac{1}{g_{\mathrm{m1}}} + 4kT\gamma g_{\mathrm{m2}} R^2 + 2kTR, \tag{5.19}$$

which is in agreement with the previously mentioned noise analysis when noting that the neglected noise sources is essentially in parallel with M_2

$$v_{\mathrm{n}}^2 = 4kT\gamma \left(\frac{1}{g_{\mathrm{m1}} R^2} + g_{\mathrm{m2}}\right) R^2 + 2kTR. \tag{5.20}$$

This can be more easily seen by adding the noise contributions from the two half–circuits, assuming uncorrelated noise

$$v_{\mathrm{n}}^2 = 8kT\gamma \left(\frac{1}{g_{\mathrm{m1}} R^2} + g_{\mathrm{m2}}\right) R^2 + 4kTR. \tag{5.21}$$

By ignoring M_1 and realizing that the remaining noise sources essentially are in parallel with M_2, this expression collapses to the noise calculation found in (5.10).

Chapter 6

Methods for Adding Variable Gain

As previously mentioned, a major specification of the analog front–end is the ability to implement variable gain. This section describes different techniques for reducing the dynamic range of the ultrasound signal.

1 Capacitive Divider

A simple method of varying the high input signal level can be the use of a voltage division circuit. Due to the requirement of keeping a very high input resistance and low input referred noise, capacitors are better suited than resistors in realizing this voltage divider. A capacitive voltage division circuit is shown in Figure 6.1.

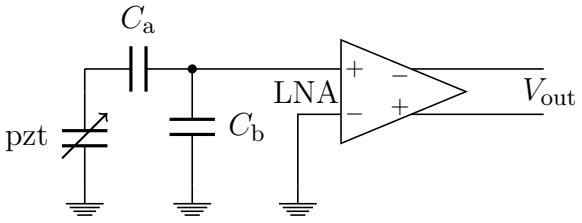

Figure 6.1: Capacitive attenuator at the input of the front–end amplifier.

Using Laplace analysis the voltage gain of the capacitive divider can be found as

$$\frac{V_i}{V_{in}} = \frac{Z_b}{Z_a + Z_b} = \frac{1/sC_b}{1/sC_a + 1/sC_b} = \frac{C_a}{C_a + C_b}, \tag{6.1}$$

where the capacitor C_b is a parallel capacitor C_p in addition to the input capacitance of the amplifier C_{in}. Hence, it is given by $C_b = C_p + C_{in}$. Ideally, this method is a frequency independent way of varying the input signal. One of the benefits of this approach is that the gain is given by the ratio of capacitors, which can be matched quite accurately in CMOS processes. Thus, the gain is well defined and can be matched from channel to channel. On the other hand, the gain range is limited by the capacitor ratio, which cannot be made arbitrarily small or large. First, the value of C_b is always larger than the input capacitance of the amplifier. In order to achieve minimum attenuation, the value of the series capacitor C_a must be much

larger than C_b. This method is therefore dependent on the amplifier to be able to have a very small input capacitance. For large attenuation, the value of C_a should be much smaller than C_b. This is typically limited by the minimum capacitor size achievable.

For weak signals, the capacitive divider should cause minimum attenuation of the input signal. In order to have an attenuation less than 10 % of the input signal, the value of C_a must be

$$C_\mathrm{a} \geq 0.9(C_\mathrm{a} + C_\mathrm{b}) \tag{6.2}$$

which can be conveniently rewritten as

$$C_\mathrm{a} \geq 9C_\mathrm{b}. \tag{6.3}$$

This means that the series capacitor C_a must be at least nine times as large as the input capacitance of the amplifier. If the input capacitance of the amplifier is large, this would make for a very large capacitor array, especially in terms of area, which is quite limited for in–probe electronics. On the other hand, maximum attenuation requires C_b to be much larger than C_a. For an attenuation of 20 dB, the value of C_b is given by

$$C_\mathrm{a} \leq 0.1(C_\mathrm{a} + C_\mathrm{b}), \tag{6.4}$$

$$C_\mathrm{b} \geq 9C_\mathrm{a}. \tag{6.5}$$

In this case, the value of C_a must be at least nine times smaller than C_b. If C_a can be made small, the value of C_b is not restricted to very large values. Clearly, if both C_a and C_b can be varied from small to large values, this attenuator can change the gain from 0 to −20 dB with simple control logic. For instance, this can be done by using a capacitor array controlled by switches as illustrated in Figure 6.2 Obviously, this approach suffers from much of the same limitations as many switched capacitor circuits, such as charge injection from switches turning off and thermal noise associated with the on–resistances of the switches. The added noise penalty from switch on–resistance can be problematic for low noise application. In addition, the switches near ground will add a parasitic capacitance at the input. This method can be used for large signals, when the charge injection is small compared to the signal level. Using complementary switches is also an option.

Of course, well–known techniques can be used to reduce the effects of charge injection, as well as reducing the on–resistance and increasing the off–resistance of the switches. Charge injection can be reduced by means of a dummy switch to absorb the charge from the main switch. This approach is effective if the dummy switch can acquire exactly the amount of charge that the main switch has stored in its channel. Therefore, good matching between the control signals is necessary. If necessary, bulk switching can be used to improve the on– and off–resistance properties of the switches.

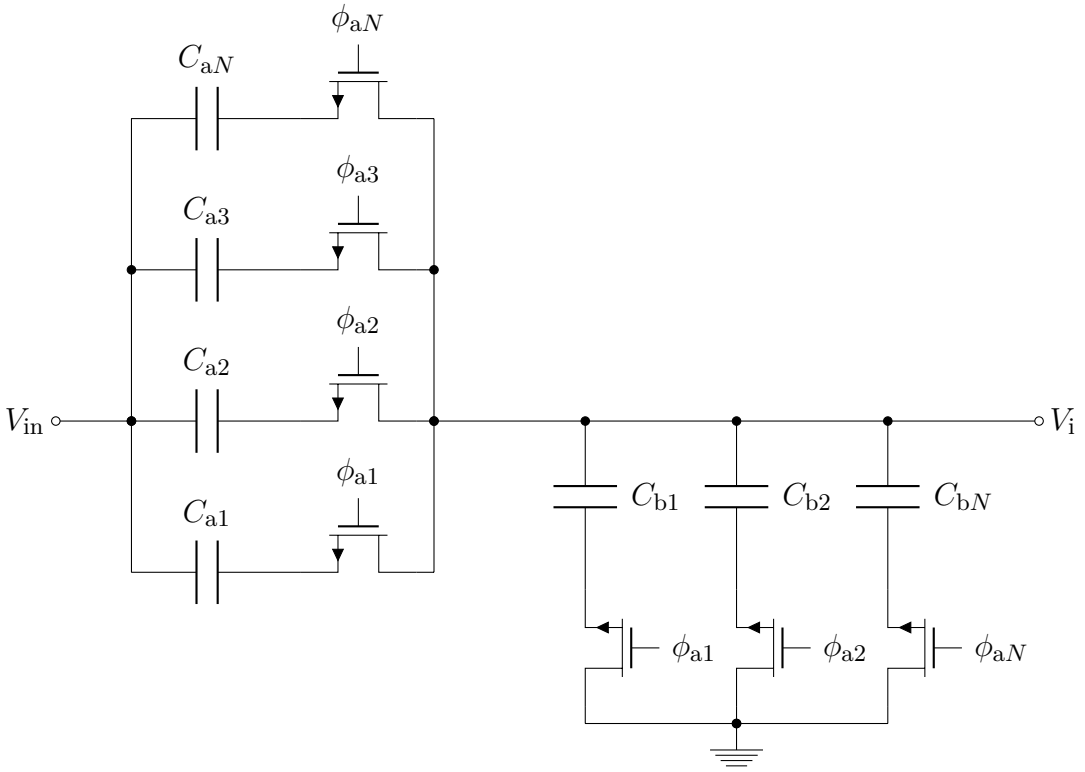

Figure 6.2: Capacitive attenuator at the input of the front–end amplifier.

2 Variable Resistor

The original transconductor cell supports several ways of implementing variable gain, for instance by changing the current mirror ratio M or by tuning the degeneration or load resistor value. The simplified amplifier topology also supports methods of varying the gain. From the small–signal analysis in Chapter 5, the voltage gain was found to be given by

$$A \triangleq \frac{v_o}{v_i} = -\frac{2G}{g_{m2}}. \tag{6.6}$$

Hence, (6.6) reveals that it is possible to vary the gain by changing the degeneration resistor. In general, this method is compatible with variable gain, as the largest gain settings yields the best noise performance. However, if the degeneration resistor is increased to lower the gain for large signals, the noise figure will increase rapidly, as can be seen from (5.20). If the degeneration resistor is increased to very large values, the signal–to–noise ratio may degraded, even for relatively large signal swings.

The principle disadvantage of using the degeneration resistor to implement variable gain, is therefore the strong dependence of the noise performance on the value of the degeneration resistor. If the degeneration resistor is made larger to reduce the gain, the reduction in gain is not as large as predicted by (6.6). As the value of $g_{m1}R$ increases, the gain of the input transistors buffering the input voltage across the degeneration resistor also improves, as can be seen from (5.8). Therefore, the value of the degeneration resistor required to reduce the gain by factor of two

could be more than a factor of five, depending on the value of $g_{m1}R$.

3 Coarse Gain Steps

For micro power low noise amplifiers, the gain range is typically limited, and it is therefore difficult to increase the gain exponentially as the signal propagates through tissue. Changing the gain in fine steps increases the complexity power consumption. However, the dynamic range still has to be reduced, which can be done by sweeping the gain i coarse gain steps. The gain range can be increased by 20 dB changing the attenuation in five steps from −20 dB to 0 dB. Such coarse gain steps are illustrated in Figure 6.3

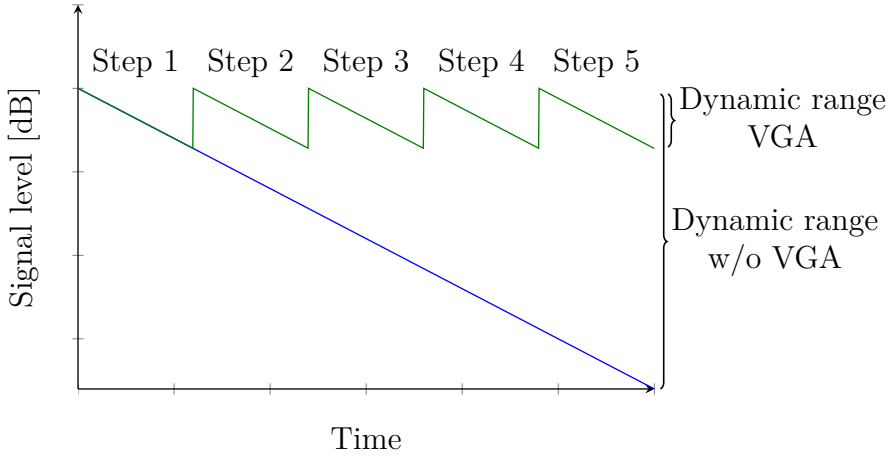

Figure 6.3: Coarse VGA implementation.

Obviously, using coarse gain steps can increase the dynamic range by a large amount. In order to maintain image uniformity, a more fine tuned time gain compensation can be implemented in the digital domain at lower power consumption.

Chapter 7

Design Methodology

This Chapter focus on the design of a low noise amplifier, having a very tight power and area budget. For this reason, it is necessary to investigate the fundamental lower limits in terms of power consumption for a given dynamic range and bandwidth. For a low noise, voltage amplifier, noise performance and power consumption is usually traded–off each other, meaning that for ultra low power designs, a relatively high noise floor is to be expected. However, this can be acceptable in terms of noise figure if the source itself is noisy. Nevertheless, a good trade–off between accuracy and power consumption is important for an energy efficient amplifier.

1 Figure–of–Merit for Analog Modules

As previously mentioned, sufficient dynamic range is a very important parameter in medical ultrasound imaging systems. The echoed signal returning from human tissue during imaging suffer from heavy attenuation when propagating toward the receive electronics. Far–field signals are extremely weak and detection should be limited by the noise of the receiver. Noise in the front–end amplifier must then be as low as possible, as this noise will deteriorate receive sensitivity. At the same time, echoes from the near–field are very strong. It is important that the amplifier and subsequent modules can handle these strong signals at while keeping a high signal–to–noise ratio. Clipping is undesirable but often unavoidable. Moreover, rail–to–rail performance is highly desirable, as high dynamic range is expensive in terms of power consumption.

2 Definition of Figure–of–Merit

Figure–of–merit (fom) optimal designs have received increased attention over the last decades, especially for area and power constrained circuits. In addition, the fundamental lower limits of power consumption in analog circuits have been extensively studied [38], [39], [40]. In [41] a figure–of–merit is proposed where dynamic range, bandwidth and power consumption are combined in one equation

$$\psi_{\text{fom}} = \frac{\sigma_{\text{r}} \cdot f}{P}, \tag{7.1}$$

where σ_r is the dynamic range, f is the bandwidth and the dissipated power is P. In order to have low numbers for power efficient circuits, (7.1) is inverted. Also, the dynamic range is squared, as to relate power quantities in the figure–of–merit

$$\psi_{\text{fom}} = \frac{P}{\sigma_r^2 \cdot f}. \tag{7.2}$$

3 Dynamic Range and Power Consumption

Although random offsets resulting from mismatch errors dominate over noise in many analog CMOS circuits [42], dynamic range is at the lower end usually limited by the noise–flor. Maximum signal in the same circuit is typically limited by the power supply[1]. The dynamic range can then be written as

$$\sigma_r \triangleq \frac{v_s}{v_n}, \tag{7.3}$$

where root–mean–square (rms) values are used for the signal voltage, v_n, and the noise voltage, v_s, respectively. Dynamic range, the ratio between these to extremes, is in other words squeezed between the supply level and the noise level. What complicates the situation further is that more advanced technologies requires lower supply levels due to lower breakdown voltages. These technologies often also dictate lower power consumption per area. To achieve this, current levels must be reduced. Decreased current levels lead to higher noise. This makes design of low power, high dynamic range circuits challenging. There is a fundamental trade–off between dynamic range, power consumption and bandwidth. These quantities are strongly related to each other, see Figure 7.1.

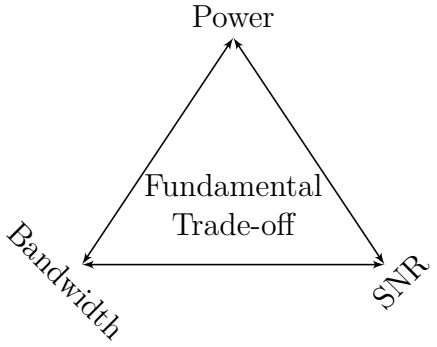

Figure 7.1: Fundamental trade–offs in analog design.

[1]For low impedance, current mode circuits this is not always the case.

4 Minimum Power Consumption

In order to identify the minimum energy per pole, consider the model in Figure 7.2.

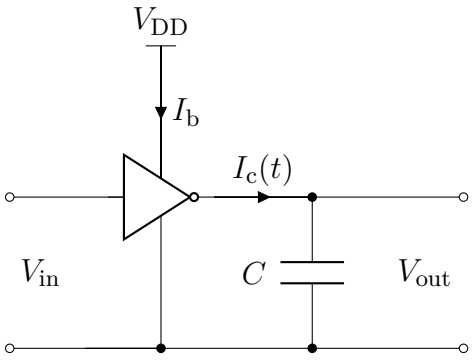

Figure 7.2: Scheme to find minimum energy per pole.

Here the load capacitor, C, is driven by a class–A output–stage. A constant current source, I_{b}, is connected to the positive power supply, V_{dd}. During operation, I_{b} is either steered into the load or down to ground through the voltage controlled current source controlled by v_{i}. For class–A biasing, quiescent current in the output stage must be as large as the maximum current to be delivered to the load. Because of this, the efficiency of such stages can never be higher then 25 %.

Theoretical maximum amplitude is equal to half the supply voltage, $V_{\mathrm{dd}}/2$. In reality it is somewhat lower due to non–zero saturation voltage in the current source. This effect is taken into account by the voltage efficiency, η_{v}.

It can be shown that the minimum energy per pole is given by [43], [44]

$$P = V_{\mathrm{dd}} \cdot \langle I_{\mathrm{b}} \rangle = \frac{v_{\mathrm{p}}}{\eta_{\mathrm{v}}} \cdot \frac{\pi \cdot f \cdot C \cdot v_{\mathrm{p}}}{\eta_{\mathrm{i}}}. \tag{7.4}$$

Here, v_{p} is the peak–to–peak voltage and η_{i} is the current efficiency. An ideal amplifier handling a typical ultrasound signal with $v_{\mathrm{p}} = 1.8\,\mathrm{V}$, $f = 7\,\mathrm{MHz}$ and a load capacitance of 70 fF would consume at least 5 µW. Here, η_{v} and η_{i} are assumed to be one, not necessarily a good assumption. For a differential amplifier this number is usually doubled. The need for common–mode feedback circuitry could lead to another doubling in the power consumption, dictated by the need of achieving enough gain in the common–mode feedback loop. Evidently, this leads to a minimum power consumption of 20 µW, which is still low enough for in–probe electronics. However, in order to achieve such a low power consumption, effective trade–offs must be done in order to maximize the energy efficiency of this amplifier. This can for instance be done by defining and obtaining an optimal figure–of–merit.

5 Figure–of–Merit Optimized Design

High quality, analog circuit engineering requires effective decision making, and a good solution to a given design problem typically involves choices among a multiple

of suitable topologies and a variety of circuit implementations. Moreover, a figure–of–merit (fom) is a number that quantifies the quality of a given design, and is one of the most concise and yet one of the most useful tools for analog design. In fact, defining a meaningful figure–of–merit can in some cases be very difficult; however, doing so may prove to be extremely valuable to the design process as it forces the analog designer to think critically about the parameters that are the most important for a successful design.

When summarizing the complete performance of an analog circuit, there is usually no perfect figure–of–merit for the given design. However, there exist many bad figures–of–merit for any circuit. Therefore, when deciding a specific figure–of–merit, it should be based on real trade–offs in the circuit design. For example, it usually doesn't make sense to have a figure–of–merit on the form $A_{\mathrm{v}}[\mathrm{dB}]/I[\mathrm{mA}]$, simply because the voltage gain in decibel is not proportional to the current consumption in milliampere.

In order to define a meaningful figure–of–merit, the well–known figure–of–merit defined in (7.2) serves as a useful starting point. In order to investigate this figure–of–merit in more detail, it is possible to insert for the dynamic range term from (7.3). This results in the following expression for the figure–of–merit

$$\psi_{\mathrm{fom}} = \frac{v_{\mathrm{n}}^2 \cdot P}{v_{\mathrm{s}}^2 \cdot f}. \tag{7.5}$$

For a given power supply voltage, the average current drained determines the power consumption

$$P = V_{\mathrm{dd}} \cdot \langle I_{\mathrm{b}} \rangle, \tag{7.6}$$

where $\langle I_{\mathrm{b}} \rangle$ is the mean current drained by the circuit from the power supply. For a design of an amplifier limited by noise and current consumption with a relatively small input swing and bandwidth, a natural figure–of–merit is therefore given by [10]

$$\psi'_{\mathrm{fom}} = v_{\mathrm{n}}^2 \cdot I_{\mathrm{b}}. \tag{7.7}$$

In this case, v_{n}^2 is the input referred noise voltage spectral density given in V^2/Hz and I_{b} is the total current drained from the supply. This figure–of–merit makes sense for many analog circuits, especially for low noise application where linearity and bandwidth do not constitute the major bottlenecks in the system. Hence, this figure–of–merit is suitable in the design of a low noise amplifier for ultrasound imaging systems. Imaging systems based on piezoelectric transducers (pzt) typically have a limited bandwidth, and signal swing in the region of some tens of millivolts. On the other hand, in order to maximize image quality and flexibility, the ultrasound front–end amplifier should have as low as possible noise figure and dissipate as little power as possible. Due to the influence of post filtering, typically performed in ultrasound imaging systems, it is more relevant to compare power spectral densities instead of integrated noise in the figure–of–merit. Also, it can be shown, that the figure–of–merit proposed in [10] is proportional to the square of the more acknowledged and complex noise efficiency factor proposed in [45] when only white noise sources are considered.

First, the input referred noise voltage spectral density of the low noise amplifier can be found by conveniently rewriting (5.20)

$$v_{\mathrm{n}}^2 = 4kT\gamma\left[\frac{1}{g_{\mathrm{m1}}} + \frac{1}{g_{\mathrm{m2}}} \cdot \frac{1}{A^2}\left(1+\frac{A}{\gamma}\right)\right], \tag{7.8}$$

where A is the voltage gain of the amplifier. Based on the noise expression (7.8) and the previously defined figure–of–merit in (7.7), it is now possible to derive the figure–of–merit for the given amplifier topology. First, the half–circuit current consumption, I_{t}, is defined as $I_{\mathrm{t}} = I_1 + I_2 = (\lambda+1)I$. Thus, the current in M_1 is implicitly defined to be λ times the current in M_2. For simplicity, we specify the operating point of the devices in terms of the $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio. Specifically, we let $g_{\mathrm{m1}}/I_1 = \alpha_1$ and $g_{\mathrm{m2}}/I_2 = \alpha_2$.

By using these definitions, the figure–of–merit for the low noise amplifier can be expressed as

$$\psi'_{\mathrm{fom}} = 4kT\gamma(\lambda+1)\left[\frac{1}{\lambda\alpha_1} + \frac{1}{\alpha_2} \cdot \frac{1}{A^2}\left(1+\frac{A}{\gamma}\right)\right]. \tag{7.9}$$

With a fixed total current consumption, it is possible to trade–off for instance noise performance with linearity, by decreasing the factor λ which will lead to a relatively increased bias current in M_2 improving linearity. This comes at the expense of bias current in M_1 which will lead to a decreased g_{m1} and therefore an increase in the input referred noise voltage spectral density. On the other hand, the original transconductor cell is designed to exhibit good large signal–linearity, leading to relaxed linearity requirements. Also, observe that there is an optimal value of the figure–of–merit with respect to λ. This should be evident, as the figure–of–merit is on the form $\lambda + 1/\lambda$, which is convex on $\mathbb{R}^+$. Thus, there is a value of $\lambda = \lambda_{\mathrm{o}}$ that minimizes the figure–of–merit.

This optimum can be found by differentiating (7.9) with respect to λ. Setting the resulting equation equal to zero yields

$$\lambda_{\mathrm{o}} = \sqrt{\frac{\alpha_2}{\alpha_1}} \cdot \frac{A}{\sqrt{1+A/\gamma}}. \tag{7.10}$$

This optimum value λ_{o} is a function of the voltage gain A as well as the $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio of M_1 and M_2. This means that requiring a larger gain will result in an increase in power consumption, which also can be true for a common–source amplifier with a gain of $g_{\mathrm{m}}r_{\mathrm{o}}$. Nevertheless, the current consumption, $I_{\mathrm{t}} = (\lambda+1)I$ can be decreased by having a larger $g_{\mathrm{m}}/I_{\mathrm{D}}$ in M_1 than for M_2. A ratio of 2 or even more is possible, resulting in a lower optimal value for λ.

The figure–of–merit in (7.9) is calculated in Figure 7.3 versus $\lambda \in [0.25, 8]$ for several different values for the voltage gain, $A = \{14.0, 15.6, 18.1, 20.0\}$ dB. In addition, the value of $\alpha_2/\alpha_1 = 1/2$ and $\gamma = 2/3$. The top line corresponds to $A = 14.0$ dB, while the lines below are for increasing values of A. Clearly, choosing a value near the optimum will result in a relatively good figure–of–merit. In fact, this confirms the robustness of the proposed optimization scheme as several values near the optimal one will also give reasonably good results, especially for large values of

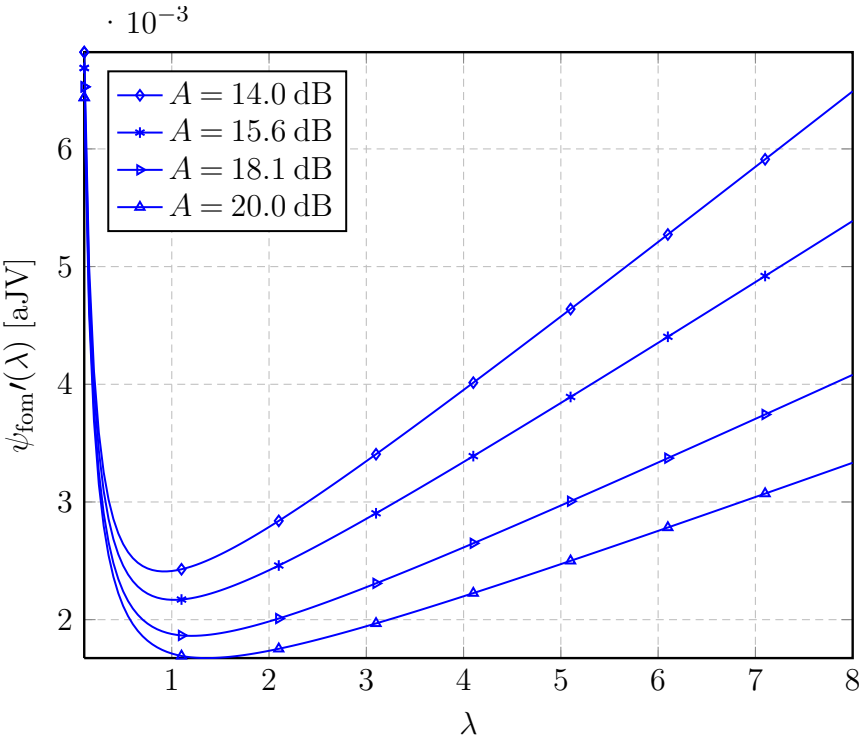

Figure 7.3: Calculated figure–of–merit for different gain settings.

A. However, it is also obvious that using values for λ much larger or smaller than the optimum will lead to a much worse figure–of–merit. A value of 1/3 was used in [7], which will result in a relatively high figure–of–merit when only noise and power is concerned. However, this offers improved linearity, one of the bottlenecks in that particular system.

Clearly, having a larger gain setting results in a lower figure–of–merit, normally at the cost of a higher current consumption $(\lambda+1)I$. However, the higher optimal value of λ can be compensated for by minimizing the value of α_2/α_1. The value of $g_\mathrm{m}/I_\mathrm{d}$ determines the operating point of the transistor, and can easily be varied from less than 5 to around 20. The maximum value of $g_\mathrm{m}/I_\mathrm{d}$ is obtained in weak inversion operation and is given by [46]

$$g_\mathrm{m}/I_\mathrm{d}\Big|_\mathrm{max} = \frac{1}{nU_T} = 25, \tag{7.11}$$

where $U_T = kT/q = 26\,\mathrm{mV}$ is the thermal voltage at 300 K and $n = 1.5$ is the weak inversion slope factor.

The choice of $g_\mathrm{m}/I_\mathrm{d}$ as a fundamental design tool is highly relevant due to a number of reasons. Firstly, it is strongly related to the performance of most analog circuits. It gives an indication of the device operating region, while it provides a tool for calculating the transistors dimensions. The $g_\mathrm{m}/I_\mathrm{d}$ ratio is a measure of the efficiency to translate bias current into transconductance; the greater $g_\mathrm{m}/I_\mathrm{d}$ value the more transconductance is achieved for a given bias current. Therefore, the $g_\mathrm{m}/I_\mathrm{d}$ ratio is sometimes referred to as a measure of transconductance generation efficiency [47].

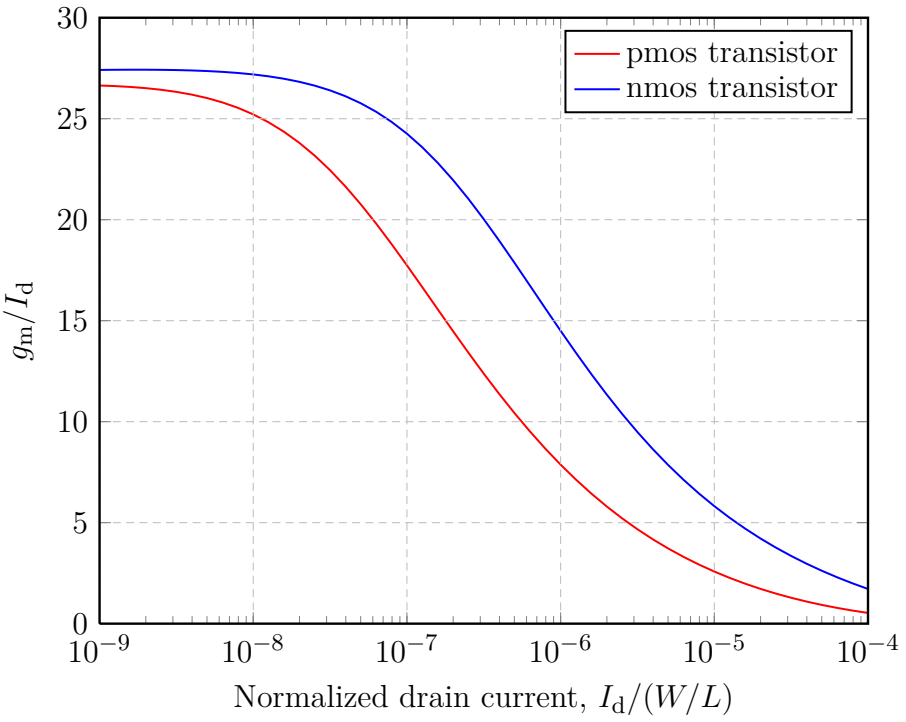

Figure 7.4: Plot showing g_m/I_d versus normalized drain current $I_d/(W/L)$.

Figure 7.4 shows g_m/I_d for different values of normalized drain current $I_w = I_d/(W/L)$. The relation of the g_m/I_d with the transistor operating point can be seen from the fact that this ratio is equal to the derivative of the logarithm of I_d with respect to V_g [48]

$$g_m/I_d = \frac{1}{I_d}\frac{\partial I_d}{\partial V_g} = \frac{\partial \ln I_d}{\partial V_g} = \frac{\partial \ln I_d/(W/L)}{\partial V_g} \tag{7.12}$$

This derivative is maximum in the weak inversion region where the I_d dependence versus V_g is exponential while it is quadratic in strong inversion, becoming almost linear deeply in strong inversion because of the velocity saturation. The g_m/I_d ratio decreases as the operating point moves toward strong inversion when I_d or V_g, are increased as shown in Figure 7.4.

The normalized drain current I_w is independent of the transistor size, and according to (7.12) the g_m/I_d ratio is also size independent. Hence, the relationship between g_m/I_d and the normalized current is a unique characteristics for all transistors of the same type (p–channel or n–channel) in a given batch. Of course, this is not exactly true when dealing with short channel transistors. The versatility of the g_m/I_d versus I_w curve can be extensively exploited during the design phase, when the transistor aspect ratios W/L are unknown. Once a pair of values among g_m/I_d, g_m and I_d has been derived, the W/L of the transistors can be determined.

The actual g_m/I_d versus I_w can typically be obtained in two ways, analytically using a transistor model that provides a continuous representation of the transistor current and small–signal parameters in all regions of operation, or from simulations using accurate device models. Figure 7.4 shows plots of g_m/I_d for n– and p–

channel transistors using an design kit for 180 nm CMOS from Austria Microsystems (AMS) with typical device parameters. The different evolution of n– and p–channel transistor curves with I_w is related to the mobility difference. However, both nmos and pmos transistors provides a maximum g_m/I_d value of above $25\,V^{-1}$. On the other side, minimum g_m/I_d for a given drain current is also of interest in order to minimize input referred noise contribution from biasing transistors and M_2. From Figure 7.4 it is clear that a value as small $5\,V^{-1}$ can be achieved, even for drain currents in the micro ampere region.

6 Systematic Design Approach

From Figure 7.3 it is evident that higher gain values results in a lower minimum figure–of–merit. This is in general compatible with time gain compensation, as the highest gain levels usually demands the best noise performance. As gain is small for the first strong signals, noise performance can be quite relaxed while maintaining a signal–to–noise ratio above a certain limit. For the absolute weakest signals, the performance should be limited by the noise of the receiver. The piezoelectric transducer is a noisy source, which means that input referred noise voltage of the amplifier can be in the region of $25\,nV/\sqrt{Hz}$ while maintaining a noise figure less than 5 dB.

As mentioned in Chapter 6, the gain can be varied by changing the resistance value of R and or the value of g_{m2}. Interestingly, the optimal value of λ decreases for lower gain settings, which means that a larger part of the current can be directed to M_2 when processing strong signals. By also changing the width of M_2 as the current increases, a great deal of change can be put into g_{m2} yielding relaxed requirement for the range of R values. A voltage gain of 20 dB is sufficient, and could be for instance be implemented with a designed gain of 26 dB, as half of the input signal is a common–mode component. On the other hand, some loss in the capacitive voltage gain caused by g_mR not being much larger than 1. Therefore, a quite high gain value can be used without obtaining a too large overall gain. This lead to a very low obtainable figure–of–merit and adds some margin for the required voltage gain. Of course, as half of the input signal is a common–mode component, the designed gain must be 6 dB higher than the desired gain value. Therefore, a gain value of 40 dB serves as a useful starting point.
Figure 7.5 shows the figure–of–merit for very high gain settings. The highest gain settings are intended to be used for very weak signals, while at the same time keeping a certain signal–to–noise ratio. For a gain of 40 dB the optimal value of $\lambda_o = 4.5$ results in a figure–of–merit of $8.35 \cdot 10^{-22}$ JV. For this gain setting, $\alpha_1 = 20$ and $\alpha_2 = 6$. From the noise requirement, (7.9) can be used to calculate the half–circuit current consumption,

$$I_t = \psi_{fom}/v_n^2 \approx 8.5\,\mu A. \tag{7.13}$$

This yields a total power consumption for the complete amplifier, $I_a = 17\,\mu A$. Using the optimum current ratio $\lambda_o = 4.5$, the drain currents of M_1 and M_2 are determined to be $7\,\mu A$ and $1.5\,\mu A$ respectively. Now that g_m/I_d and I_d have been

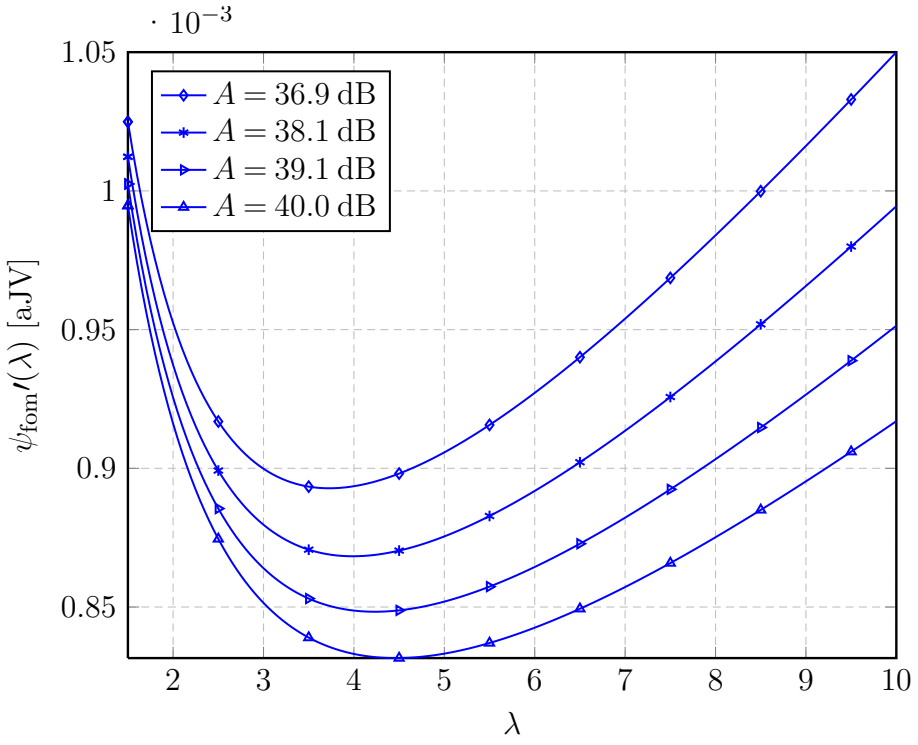

Figure 7.5: Calculated figure–of–merit for higher gain settings.

determined, W/L of M_1 and M_2 can be found. In addition, the W/L of the bias transistors can be found by minimizing their g_m values, while keeping the drain–source saturation voltage below 400 mV. The transistor lengths are determined by a trade–off between area and bandwidth on one side and flicker noise on the other side. For the bias transistors acting as current mirrors, keeping a high output resistance is also considered when choosing gate lengths. Table 7.1 shows the chosen transistor dimensions and corresponding parameter values. Additional information regarding the sizing of the transistors are shown in Appendix B.

Table 7.1: Important transistor parameters for the designed amplifier.

Transistor	W [µm]	L [µm]	$g_\mathrm{m}/I_\mathrm{d}$ [V^{-1}]	V_dss [mV]	C_gg [fF]
Input transistors, M_1	24	0.22	21.0	− 121	7.85
Composite devices, M_2	0.5	2.5	6.0	282	2.63
Bias transistors, M_bp	3.0	1.5	4.2	− 350	6.00
Bias transistors, M_bn	0.8	5.0	4.5	372	4.00

7 Common–Mode Feedback Circuitry

As for most differential amplifiers, the output common–mode should be well defined. A typical approach is to use additional circuitry to determine the output common–mode voltage and control it to be equal to some specified voltage, for instance the

input common–mode level. This circuitry, commonly referred to as the common–mode feedback circuitry (CMFB), may even be the most difficult part of the amplifier to design.

The common–mode feedback circuit should ideally suppress common–mode signal components on the whole band of differential operation. For this amplifier topology, however, this will not be the possible due to the single input operation. In general, the goal of the common–mode feedback circuit is to fix the common–mode voltage at different high impedance nodes that are not stabilized by the negative differential feedback.

Typically, the output common–mode level is sensed using an additional common–mode detector circuit, then compared with a reference voltage, and an error–correcting signal is injected to the biasing circuitry of the amplifier. The common–mode feedback loop has to be designed carefully to avoid stability problems. This often increases the complexity of the design, the power consumption, and the silicon area used. The frequency response of the differential path is also degraded due to the added parasitic components involved in conventional common–mode feedback schemes, i.e. the loading of the output to sense the common–mode level.

8 Feedback Biasing

A simple way of introducing low frequency (essentially dc) common–mode feedback for this amplifier topology, can be achieved by using feedback biasing. This will also bias the input transistors. Traditional biasing of the gate using resistors have the benefit of setting the operating point based on voltage division, and thus ratios of resistors, which can be matched quite closely in CMOS processes. In our circuit, however, these component values typically modify the input impedance to unacceptable levels, as well as increasing the already crucial noise level at the input of the amplifier.

The use of self biasing [49], as illustrated in Figure 7.6, also implies a modification of the input impedance to $1/g_{\mathrm{m1}}$ if the value of R_{f} is much less than r_{ds}. The noise level is also increased by the introduction of the internal feedback path. On the other hand, by having a very large value of R_{f}, the feedback action will be neglectable and the input impedance level will be unaffected. This requires a resistor in the range of $10\,\mathrm{M}\Omega$, especially when noting that the equivalent resistance seen at the gate will be different than that of R_{f} due to the Miller effect. Such large resistance values are difficult to realize in CMOS processes using poly resistors.
Still, this high resistance value can be achieved by using a diode connected p–channel transistor in sub threshold region. The application of using sub threshold MOSFETs as high–value resistors have been reported for low frequency applications [50], but recently also for common–source amplifiers interfacing 30 MHz and 100 dB ultrasound transducers [51], [52]. This technique typically limits the available voltage swing at the drain, in order to avoid driving the sub–threshold transistor in the linear region. However, in this micro power design the available input swing is limited, and is relatively small compared to the supply voltage. The contribution to the input capacitance is also neglectable, since small transistors can be used.

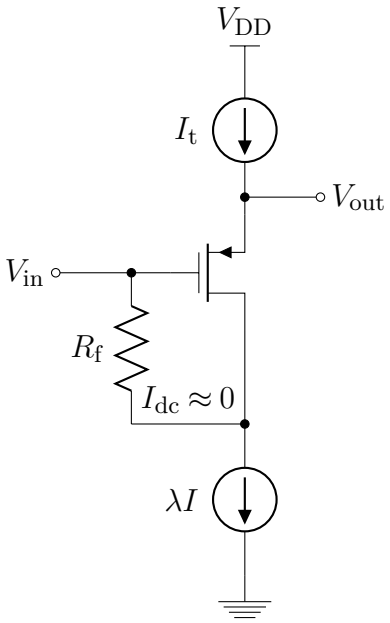

Figure 7.6: Feedback biasing. The voltage at drain and gate are equal, and the behaviour for dc–signals is the same as for a diode connected transistor.

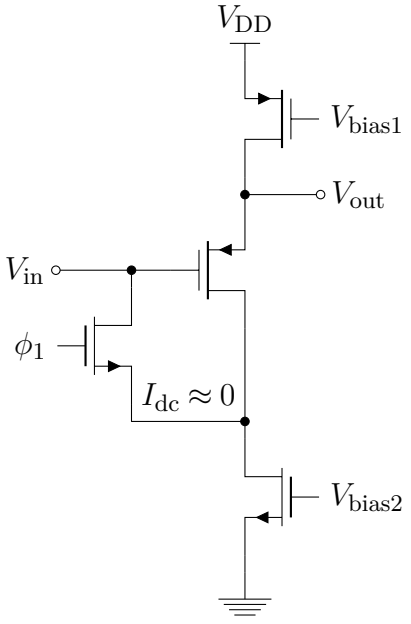

Figure 7.7: Feedback biasing realized using sub–threshold n–channel MOSFET

For ultrasound applications the receive and transmit electronics are switched on and off in periods. First a pulse is transmitted, followed by a certain receive period. During this period, the receive electronics processes the signal before a new pulse is transmitted. By exploiting the time interleaving properties of ultrasound imaging, the feedback biasing scheme can be further improved. By replacing the diode connected transistor with a switch, the output and input common–mode can be set to the same value during the short period of transmit. During the receive

period, the inputs are biased by the off–resistance of the common–mode feedback switches. This will provide a stable output common–mode level during the 120 us receive period.

The feedback biasing can be implemented as illustrated in Figure 7.7. For simplicity, only one of the inputs is shown. Here, ϕ_1 is a control voltage that is determined by the transmit/receive electronics. Typical disadvantages associated with transistor switches are also taken into account. First, the channel charge injected to the circuit when turning the transistor switch off is not likely to be a problem, as the current source forcing a current through M_1 can sink most of this charge. In addition, the added noise penalty associated with the on–resistance of the switches will not pose a limitation, as the switches are turned off during receive. Maintaining a high input impedance will also be achieved by using small transistors with a very large off–resistance.

9 Implementing Variable Gain

Both the proposed methods of implementing variable gain will introduce more noise at the input of the amplifier. For simplicity, only one of the two proposed methods will be investigated further. The capacitive attenuator is chosen as it is not among the methods of implementing variable gain that has been extensively used for this particular amplifier topology. Changing the degeneration resistance and current mirror ratio have been shown to offer variable gain in relatively small steps [8]. Unfortunately, the available gain range achieved in [8] is only 14 dB at a power consumption of 5 mV from a 5 V supply. The capacitive attenuator can therefore be a very good alternative to implement variable gain. The gain factor of the capacitive attenuator is based on ratios of capacitors, which can be matched closely, at least compared to changing the degeneration resistor alone. Especially when noting the large increase in R required to reduce the gain.

Extracting the input capacitance of the amplifier determines the smallest value of C_b, which is about 10 fF. For this value, the series capacitor value can be determined by the required minimum attenuation of 0.9 or -1 dB.

$$C_\mathrm{a} \geq 9C_\mathrm{b} = 90\,\mathrm{fF}. \tag{7.14}$$

Similarly, maximum attenuation is achieved when the parallel capacitor is much larger than the series capacitor C_a. For an attenuation of 20 dB and a minimum capacitor size of $C_\mathrm{a} = 10\,\mathrm{fF}$ yields the required value of C_b

$$C_\mathrm{b} \geq 9C_\mathrm{a} = 90\,\mathrm{fF}. \tag{7.15}$$

Hence, with a small input capacitance of 10 fF and using a unit capacitor of 10 fF results in a total array capacitance of about 200 fF. This means that this variable gain method can be implemented without a large increase in area overhead. Also, using a unit capacitor of 10 fF is achievable in 180 nm cmos [53].

Chapter 8

Simulation Results and Discussion

This Chapter presents key results from the amplifier design, such as noise performance, bandwidth and gain. Essentially all interesting design parameters are investigated and verified through simulations. In addition, important simulation results are discussed and compared with specification and relevant theory. Finally, limitations and possible error sources impacting simulation results are discussed.

1 Simulation Setup

For most analog circuits several different simulations are required. The first done is usually a dc analysis to check that all transistors operate as expected and that they have the designed value of g_{m}, I_{d} and V_{dss} (V_{eff}). When the transistors are operating according to the design, it is normal to proceed to an ac analysis to check the frequency response. The frequency response can be used to find and verify small–signal gain and noise performance, as well as bandwidth and stability. In addition, transient analysis can be used to find large signal gain and linearity. In order to have more robust results, the test setup should also include mismatch simulations, process corner simulations, supply voltage sweeps and the like. Note that large temperature sweeps are not directly relevant, as ultrasound probes have quite stringent surface temperature requirements. However, a slight increase in temperature is included, to model self heating during normal operation. The specifications are investigated using the following verification plan shown in linearization 8.1. The different test benches are found in Appendix D.

The piezoelectric transducers can typically not be integrated on the same chip as the analog front–end. Therefore a bonding inductance of 1 nH and bonding capacitance of 200 fF is included to take additional attenuation into account. The transistor models used are from a 180 nm design kit from Austria Microsystems (AMS) using a nominal supply voltage of 1.8 V.

2 Transistor Level Implementation

Figure 8.1 shows the complete amplifier topology implemented on transistor level. The current mirrors implemented did not result in exactly the designed bias currents.

Table 8.1: Depicted simulations in the verification of the amplifier.

Specification	Analysis	Test bench
Biasing	dc analysis	tb_vgalna_dc.cir
Input capacitance	dc analysis	tb_vgalna_dc.cir
Current consumption	dc analysis	tb_vgalna_dc.cir
Small signal voltage gain	ac analysis	tb_vgalna_ac.cir
3 dB Bandwidth	ac analysis	tb_vgalna_ac.cir
Noise factor at f_0	ac analysis	tb_vgalna_ac.cir
Large signal voltage gain	transient analysis	tb_vgalna_tr.cir
Capacitive divider	transient analysis	tb_vgalna_tr.cir
Linearity	transient analysis	tb_vgalna_tr.cir
Common–mode feedback	transient analysis	tb_vgalna_tr.cir

This is partially caused by the mismatch in drain source voltage observed in the current mirror transistors. Finite output resistance in the current mirrors can also contributes to reduced output current, but the output conductance of the current mirrors were designed to be very low. In fact, extracted output resistance of the current mirrors turns out to be very high.

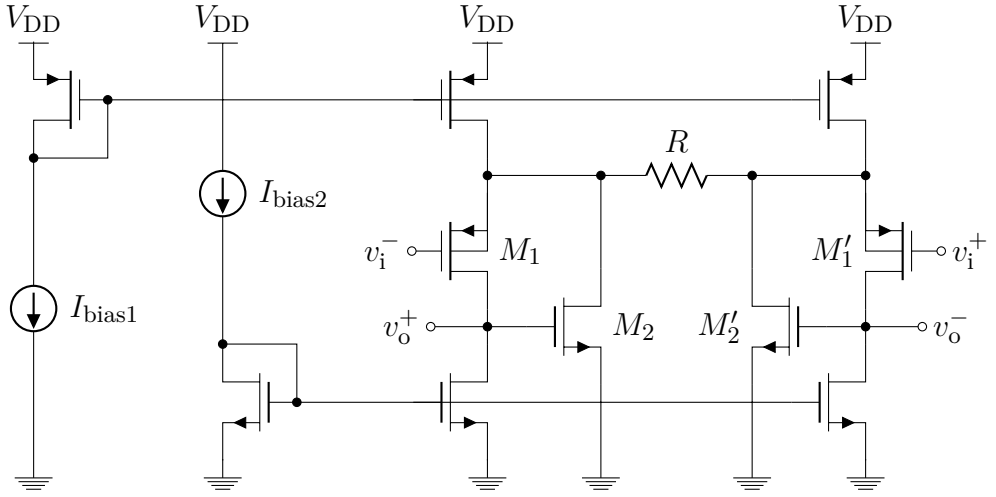

Figure 8.1: Simplified voltage amplifier topology including biasing.

Due to these non ideal effects, the current mirror gain differ slightly from the ideal case, where it is given by

$$I_o/I_i = \left(\frac{W}{L}\right)_2 \Big/ \left(\frac{W}{L}\right)_1. \tag{8.1}$$

The device dimensions in the current mirror are therefore matched given by (8.1) and the two current sources tuned to better match the desired bias currents. linearization 8.2 shows relevant parameters for the current mirror transistors extracted using dc simulation. Extracting the operation point of the different

transistors reveals that the input transistors operate in subthreshold, while all other transistors are well in saturation.

Table 8.2: Transistor parameters for the complete amplifier.

Transistor	W [µm]	L [µm]	V_{dss} [mV]	r_{ds} [MΩ]	I_{d} [µA]
Input transistors, M_1	24	0.22	− 121	0.223	6.90
Composite devices, M_2	0.5	2.5	317.0	11.42	1.75
Input Current Mirror, M_{p}	3.0	1.5	− 357	5.556	4.00
Bias transistors, M_{bp}	3.0	1.5	− 355	1.934	8.65
Input Current Mirror, M_{n}	0.8	5.0	557.0	7.463	4.00
Bias transistors, M_{bn}	0.8	5.0	546.0	2.092	6.90

Hence, the systematic mismatch in the current mirrors can be tuned out by changing the two bias currents independently. This increase in complexity is a disadvantage if the circuit is intended for mass production. However, for prototyping this increase of controllability by being able to individually tuning the bias currents is essential for a simple and accurate biasing of the transistors. Clearly, this mismatch in the current mirrors will get worse when including random variations in the threshold voltage and β parameter for the transistors. Fortunately, the figure–of–merit is relatively robust with respect to the optimal current distribution λ_{o}, especially for large gain settings, as can be seen from Figure 7.5. Also, any input offset due to mismatch in the input transistors is not of particular interest, due to fact that the signal from the ultrasound is bandpass. The low frequency offset is therefore not a part of the output signal. Obviously, it is possible to reduce stochastic mismatch in the current mirrors and input transistors by scaling up the transistor dimensions.

3 Noise Performance

The noise performance is one of the major specifications of this circuit. The requirement of 5 dB noise factor is defined according to a piezoelectric transducer source. From the equivalent circuit of the ultrasound transducer, the input referred noise voltage spectral density should be less than $25\,\text{nV}/\sqrt{\text{Hz}}$. Figure 8.2 shows the input referred noise voltage spectral density.

Clearly, the input referred noise is well below the requirement for typical transistor parameters and an operating temperature of 27 °C. From Figure 8.2 flicker noise can clearly be observed for low frequencies. The thermal noise level is $16.3\,\text{nV}/\sqrt{\text{Hz}}$ and the $1/f$ noise corner occurs at 500 kHz. In fact, in the frequency band of interest from 3.5 MHz to 10.5 MHz, the flicker noise is below the thermal noise floor, which is a bit surprising considering the relatively small transistors. The input transistors are made wide to minimize the input referred noise, and the composite devices are relatively long for the same reason. From (2.12) it is clear that the flicker noise corner is inversely proportional to the total capacitance of the transistor WLC_{ox}. Having a total capacitance of less than 10 fF in the input transistors, the flicker noise corner is not expected to be well below the lower

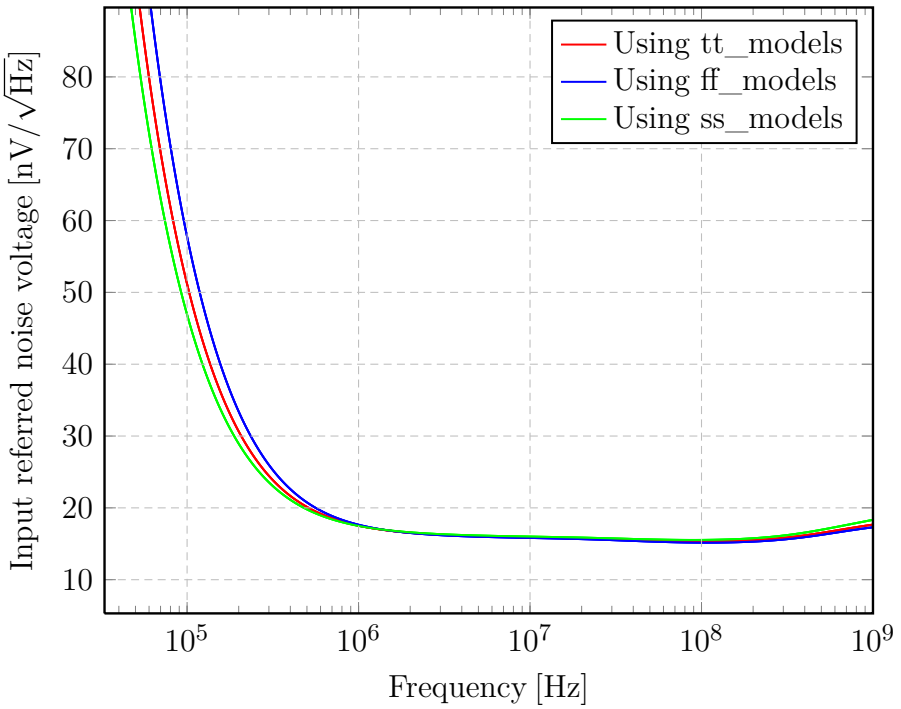

Figure 8.2: Input referred noise voltage spectral density for three process corners.

transducer passband frequency of 3.5 MHz. This could be caused by optimistic flicker noise models in the design kit, but this is difficult to verify. On the other hand, the most important flicker noise contributors are the input transistors, which are relatively large, even though the input capacitance is quite small. Also, recall that the effect of flicker noise is minimized when using p–channel transistors as input devices and by using devices with large gate areas. Flicker noise in pmos transistors is typically one to two order of magnitude lower than flicker noise in nmos transistors as long as the $|V_{gs}|$ is not much larger than the threshold voltage [13], [21]. As the input transistors are operating in subthreshold, this condition is clearly satisfied. Therefore, the low flicker noise corner is due partially to the use of p–channel input devices, but also to the relatively high thermal noise level of $16.3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Also notice the relatively small variations for the different process corners.
Figure 8.3 shows the noise figure given the piezoelectric transducer source. The noise figure definition is the well–known expression given by [54]

$$NF \triangleq 10\log_{10}\left(\frac{V_\mathrm{n}^2}{V_\mathrm{s}^2}\right) = 20\log_{10}\left(\frac{V_\mathrm{n}}{V_\mathrm{s}}\right), \tag{8.2}$$

where V_n is the total noise, amplifier noise plus source noise, and V_s is the noise from the source. Referring the noise of the transducer source to the input of the amplifier yields a noise voltage of $18.2\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This voltage noise is attenuated by the electrical capacitance of transducer in addition to any input capacitance of the amplifier. Having an input capacitance much less than the capacitance of the piezoelectric transducer minimizes the capacitive loading of the source, resulting in best possible noise figure for the given source. It is worth mentioning that the piezoelectric transducer noise model with a $32\,\mathrm{k}\Omega$ resistor in parallel with a 450 fF

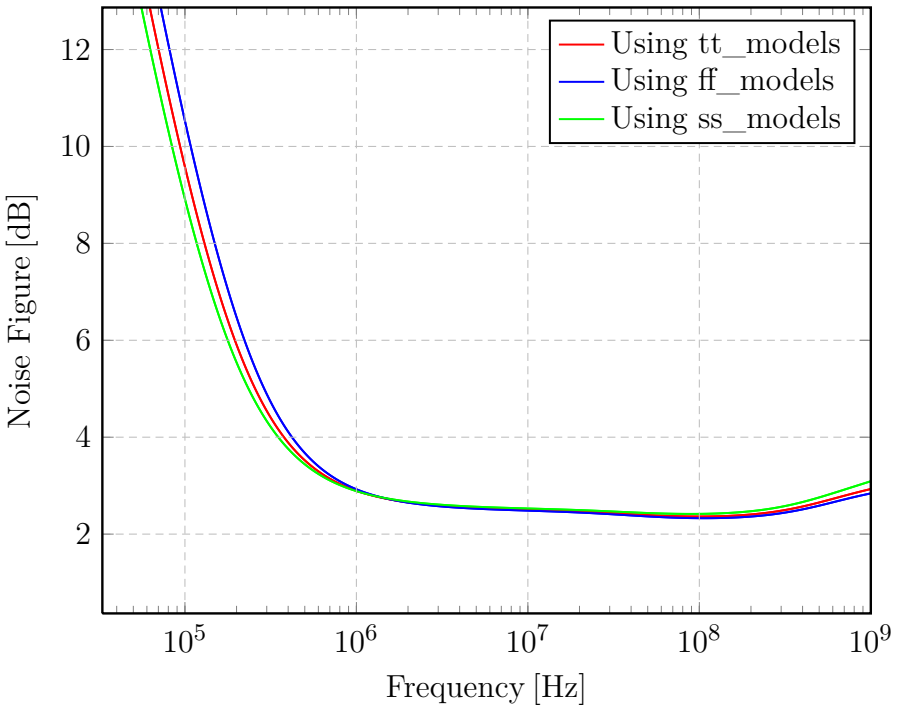

Figure 8.3: Noise figure for three process corners.

capacitor is only valid at resonance. On the other hand, the noise figure requirement is only defined for the center frequency of 7 MHz, which should be less than 5 dB. Figure 8.3 shows a noise figure of 2.6 dB at 3.5 MHz, which is well below the requirement. Figure 8.3 also shows only small differences due to process variations.

For the amplifier design, one of the most important trade–offs is to minimize noise within a strict power budget. The figure–of–merit defined in [10] quantifies this trade–off between power and noise. This figure–of–merit is also proportional to the square of the noise efficiency factor (nef) introduced in [45]

$$\epsilon \triangleq V_{\text{ni, rms}} \cdot \sqrt{\frac{2I_{\text{tot}}}{(\pi \times U_T \times 4kT \times f)}}, \tag{8.3}$$

where $V_{\text{ni, rms}}$ is the input referred rms noise voltage, I_{tot} is the total amplifier current drained from the supply and f is the amplifier bandwidth in Hertz. An amplifier using a single bipolar transistor (with no $1/f$ noise) has an noise efficiency factor of one; all practical circuits have higher values. Substituting the expression for the amplifier thermal noise integrated across the bandwidth into the noise efficiency factor, assuming the input transistors dominate the noise floor, yields

$$\epsilon = \sqrt{\frac{4I_{\text{tot}}}{3 \times U_T \times g_{\text{m1}}}} = \sqrt{\frac{4(22/9)I_{\text{d1}}}{3 \times U_T \times g_{\text{m1}}}}, \tag{8.4}$$

where I_{d1} is the drain current through M_1, which is 9/22 of the total amplifier supply current. From this expression it is clear confirms that in order to minimize the noise efficiency factor, the $g_{\text{m}}/I_{\text{d}}$ of the input devices should be maximized. As previously mentioned, $g_{\text{m}}/I_{\text{d}}$ reaches it maximum value in weak inversion operation.

The transistor dimension W/L is therefore large to approach subthreshold operation with microampere current levels. Inserting a more accurate noise expression valid in weak inversion yields [13]

$$\epsilon^2 = \frac{22n}{9 \times U_T} \left(\frac{I_{\mathrm{d1}}}{g_{\mathrm{m1}}} \right). \tag{8.5}$$

The maximum $g_{\mathrm{m}}/I_{\mathrm{d}}$ in weak inversion yields the minimum noise efficiency factor

$$\epsilon_{\mathrm{min}} = \sqrt{(22/9) \times n^2} \approx 2.35. \tag{8.6}$$

Inserting for the input referred noise voltage of 42.6 μV_{rms} and power consumption of 17.3 µA and bandwidth of 7 MHz for the designed amplifier into (8.3) results in a noise efficiency factor of $\epsilon \approx 2.57$ a value very close to the theoretical lower limit. In derivation of the minimum noise efficiency factor, only noise from the input transistors are included. The higher value achieved in this work is partially caused by other transistors contributing to the total noise, as well as using a value of $g_{\mathrm{m}}/I_{\mathrm{d}}$ lower than the theoretical maximum value. In order to achieve the maximum value of $g_{\mathrm{m}}/I_{\mathrm{d}}$ even larger transistor dimensions are required. This would lead to a larger input capacitance and lower bandwidth of the complete amplifier. Thus, using the method proposed in [10] to optimize the trade–off between noise and power consumption, also results in a noise efficiency close to the theoretical lower limit. In fact, the simulated noise efficiency factor is 10 % above the theoretical lower limit. In comparison, the noise efficiency factor achieved in [50] is 37 % above the theoretical lower limit with a noise efficiency factor of 4.0. linearization 8.3 shows a performance summary of the designed amplifier compared to state of the art micro power, low noise amplifiers reported in the literature.

Table 8.3: Performance summary for the designed low noise amplifier.

	This work	[50]	[55]	[56]	[57]	[58]	[59]	[60]
NEF [−]	2.57	4.0	3.1	3.26	3.3	4.3	4.6	9.2
v_{n} [nV/$\sqrt{\mathrm{Hz}}$]	16.3	21.0	85.1	117	60.0	55.0	98.0	57.0
I_{t} [µA]	17.3	0.18	0.87	0.34	1.8	2.3	1.1	11.1
V_{dd} [V]	1.8	± 2.5	2.8	1.0	1.0	3.0	1.8	3.0
L_{min} [µm]	0.18	1.5	0.6	0.35	0.065	0.5	0.8	0.5

where v_{n} is the input referred noise voltage spectral density, I_{t} is the current consumption, V_{dd} is the supply voltage and L_{min} is the minimum gate length, i.e. the technology node.

4 Frequency Response

In order to verify small signal gain and bandwidth, the frequency response is found by means of an ac analysis. First, the small signal gain for the input transistors is found in Figure 8.4. Then, the small signal gain from the input devices to the gate of M_2 is shown in Figure 8.6. For these two plots, the variable gain attenuator is not used, as it would complicate the calculations.

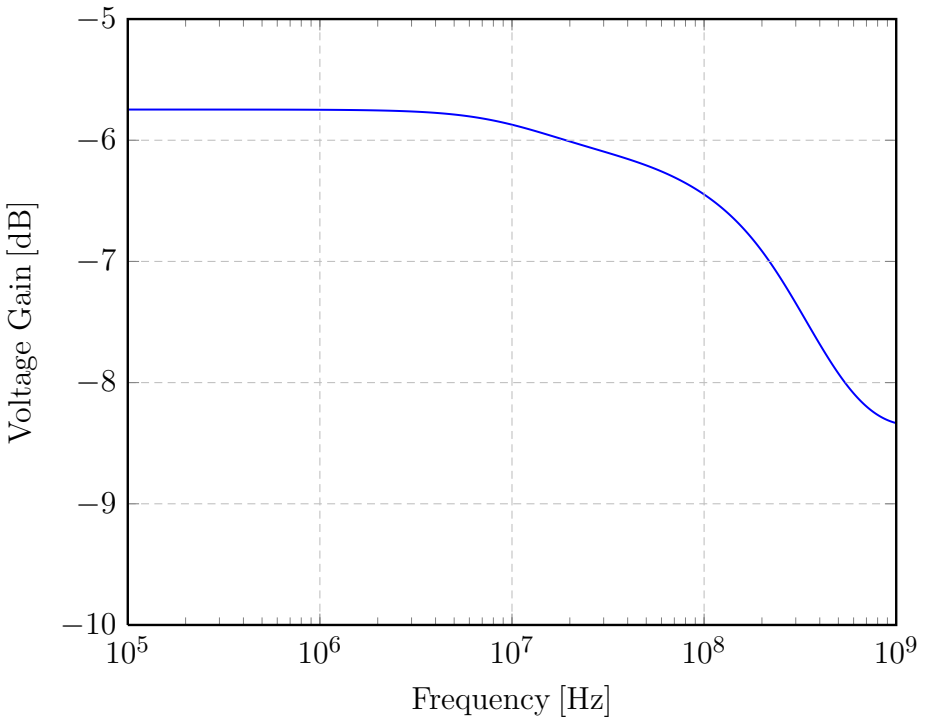

Figure 8.4: Magnitude plot of the source followers buffering the input voltage across the degeneration resistor.

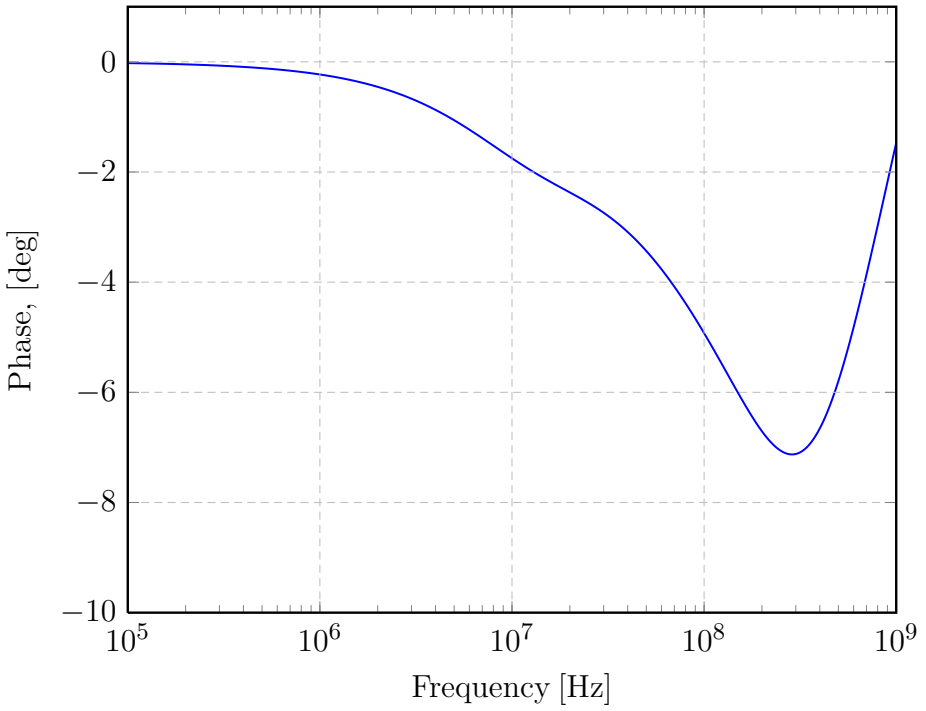

Figure 8.5: Phase plot of the source followers buffering the input voltage across the degeneration resistor.

From Figure 8.6 it is clear that the simulated small signal gain is lower than

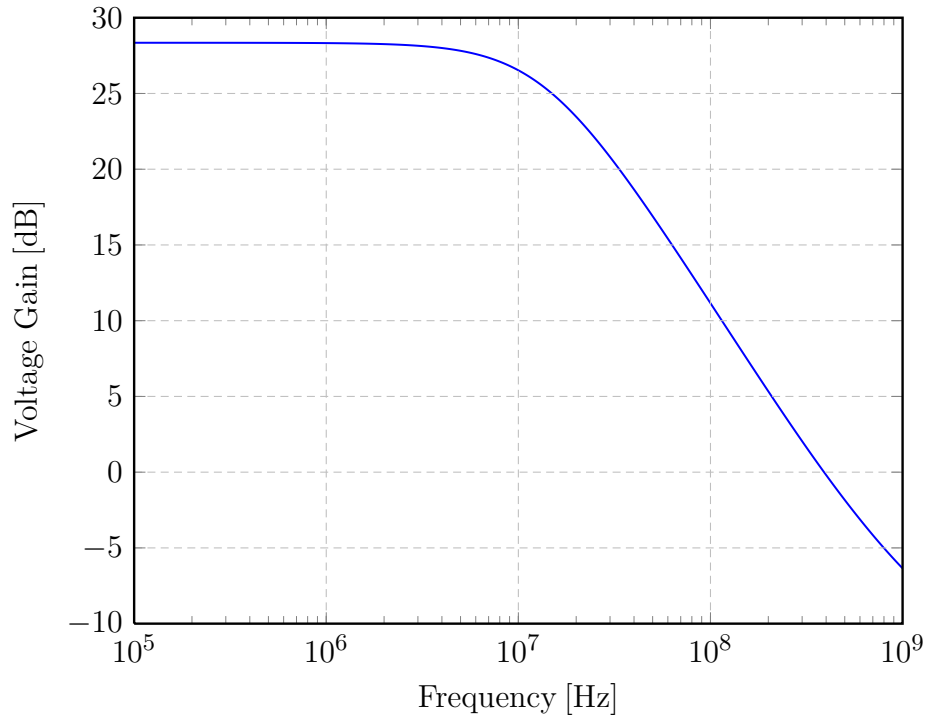

Figure 8.6: Magnitude plot of the source followers buffering the input voltage across the degeneration resistor.

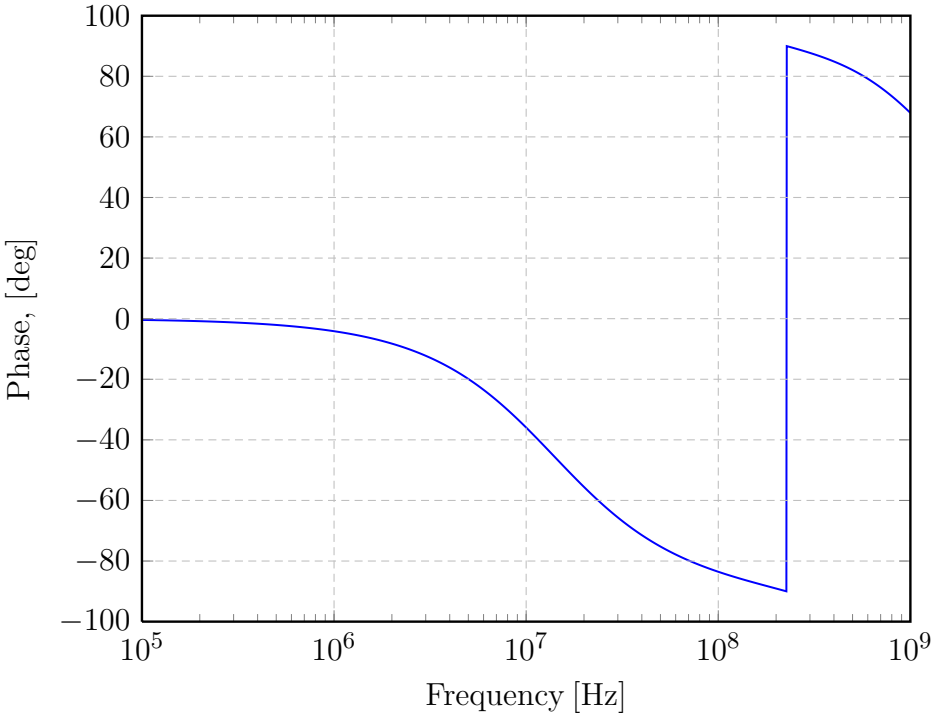

Figure 8.7: Phase plot of the source followers buffering the input voltage across the degeneration resistor.

expected from the simplest gain expression $2G/g_{m2}$. The designed gain of 40 dB obviously drops by 6 dB to 34 dB due to the single input operation. In addition, any attenuation in the input devices buffering the input voltage across the degeneration resistor will result in additional gain loss, as can be seen from (5.9), rewritten here for convenience

$$\hat{A} = -\frac{2G}{g_{m2}}\hat{A}_1 + \frac{g_{m1}}{g_{m2}}(1 - \hat{A}_1). \tag{8.7}$$

Given a voltage gain of $\hat{A}_1$ −5.75 dB in the input transistors and a g_{m1}/g_{m2} of 18, the voltage gain should be around 30.9 dB. This is in better agreement with the simulation result in Figure 8.6, which shows a gain of 28.34 dB.

Figure 8.8 shows the bandwidth of the complete circuit including the variable gain attenuator at minimum attenuation. The bandwidth of the amplifier is 21.5 MHz when driving a 25 fF load. Due to the additional attenuation of capacitive voltage divider, even at minimum attenuation, the overall voltage gain is about 23.3 dB. Obviously employing the weak inversion region of the input transistors to achieve a good noise and power trade–off yields a relatively low bandwidth. On the other hand, the bandwidth for the piezoelectric transducer is in the region of 3.5 MHz to 10.5 MHz, which makes this amplifier fast enough. For lower load capacitances the bandwidth obviously increases, but there is of course no point in making the load capacitance smaller than the parasitic capacitance of the transistors in the amplifier. Also note that the transfer function of the front–end amplifier and capacitive attenuator now is bandpass. This is due to the fact that the capacitive voltage divider itself forms a bandpass filter. The lower 3 dB frequency is well below the lower frequency content of the transducer.

5 Small Signal Performance Summary

linearization 8.4 shows a summary of key small–signal parameters for the front–end amplifier using worst case transistor parameters, which turned out to be slow–slow process corner, and a temperature of 27 °C. Note that the noise requirement is met while keeping decent power consumption.

Table 8.4: Important simulation results.

Parameter	Specification	Simulated	Unit
Voltage gain	20.0	23.3	[dB]
3 dB Bandwidth	10.5	21.5	[MHz]
Input capacitance	< 100	10.5	[fF]
Noise factor at f_0	< 5.0	3.1	[dB]
Current consumption	< 22.0	17.3	[µA]

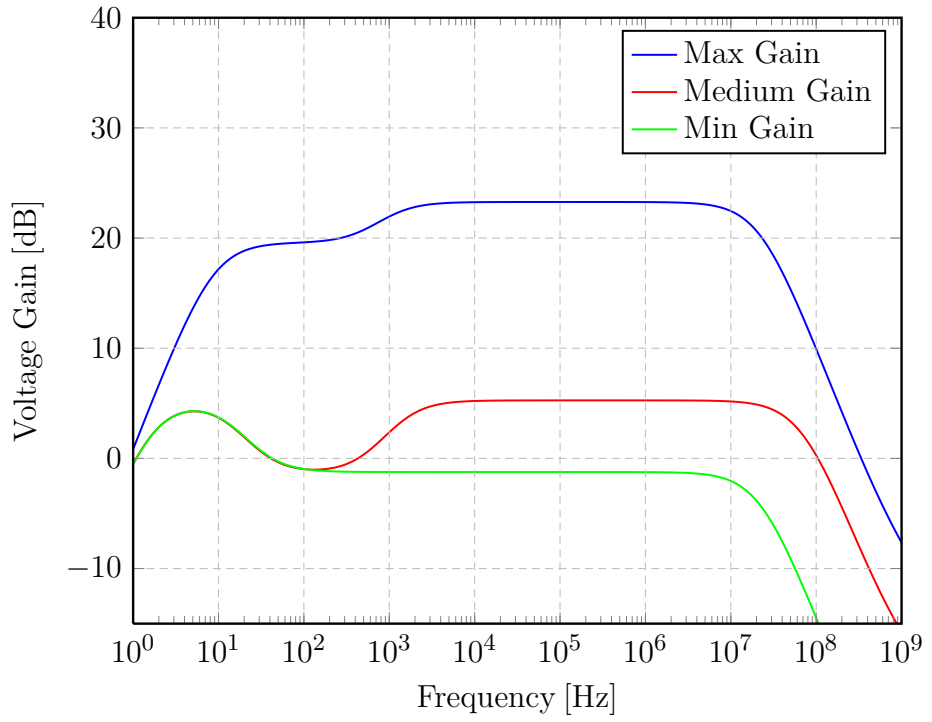

Figure 8.8: Magnitude plot of the complete front–end amplifier.

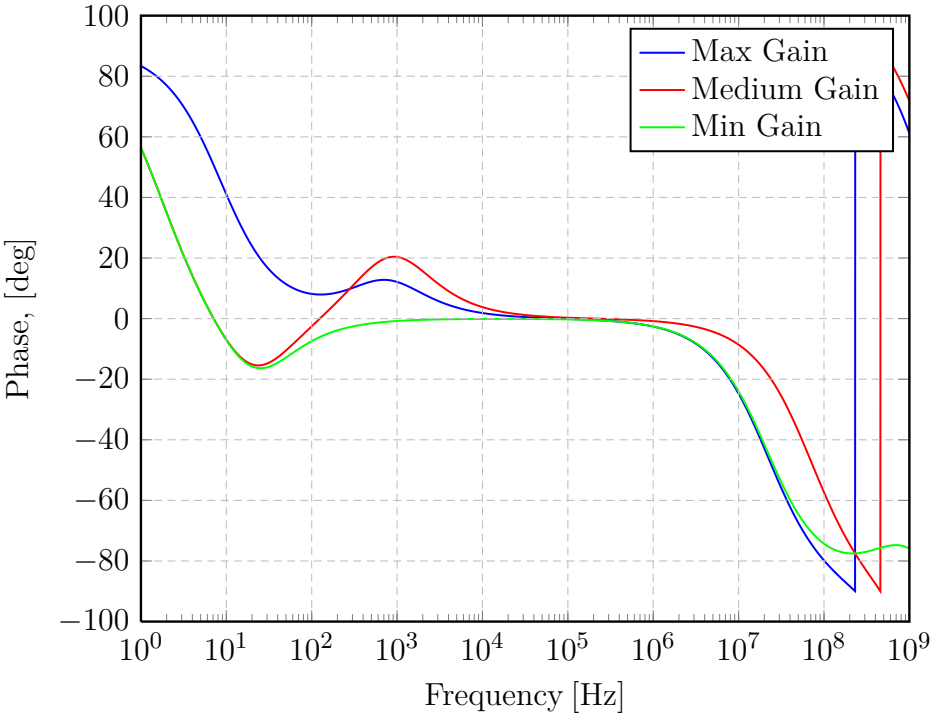

Figure 8.9: Phase plot of the complete front–end amplifier.

6 Large Signal Performance

Large signal performance such as linearity and large signal gain is verified through a transient analysis. First using single tone input signal at 7 MHz, but a Gaussian pulse with 7 MHz center frequency and 100 % relative bandwidth is also employed for more realistic simulation results. This Gaussian pulse generated from a realistic transducer model has a finite energy, and is therefore not well suited for simulating transients much longer than the pulse length.

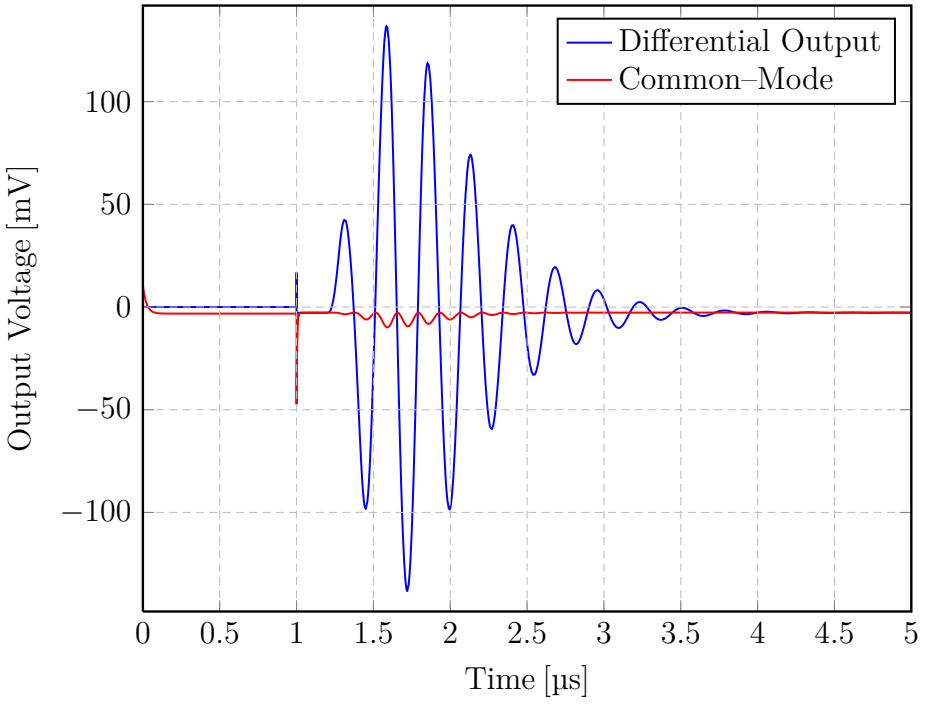

Figure 8.10: Differential output voltage and common–mode level variations.

Figure 8.10 shows the maximum input signal using the minimum gain setting. Clearly, the common–mode voltage does not drift very far during this relatively short transient. Similar results also holds for a single tone transient of 120 µs with a 7 MHz input signal. Even when using ideal common–mode feedback, half of the input signal is a common–mode component. Figure 8.11 shows how the common–mode variations compare with half of the input signal.

From Figure 8.11 it is clear that the variations in common–mode is of the same size as half the input voltage. The switched common–mode feedback is therefore working as expected, and is sufficient to ensure a well-defined output common–mode level during the 120 µs receive period.

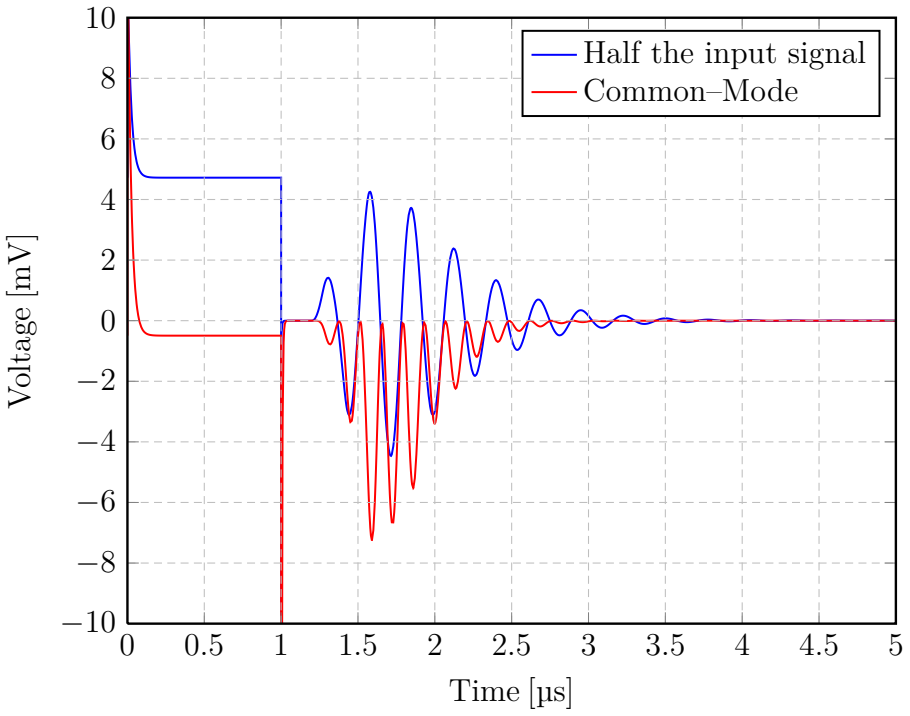

Figure 8.11: Half the input signal versus common–mode variations.

7 Extracting Input Resistance

When using the proposed common–mode feedback circuit to set the output common–mode, the input transistors are effectively diode connected. Usually this translates into a input resistance of $1/g_{\mathrm{m1}}$. For this amplifier topology, this is not the case, as the two current sources forcing a constant bias current through the input transistor constitute high impedance nodes. Using a test source, it is possible to extract the input resistance of the amplifier.

In the dc test bench in Appendix D a test dc voltage is applied. The input resistance is found by extracting the current through the test source

$$R_{\mathrm{in}} = \frac{V_{\mathrm{x}}}{I_{\mathrm{x}}} \tag{8.8}$$

Spice simulations show that the amplifier can maintain an input resistance of more than 1 MΩ, even when the common–mode feedback control signal ϕ_1 is high.

Table 8.5: Input resistance simulation results.

Control signal level	R_{in}	Specification	Unit
ϕ_1 high	1.211	–	[MΩ]
ϕ_1 low	5160	maximize	[GΩ]

Clearly, the proposed common–mode feedback does not reduce the input resistance to unallowable low levels. This is partly due to the high off–resistance of the nmos

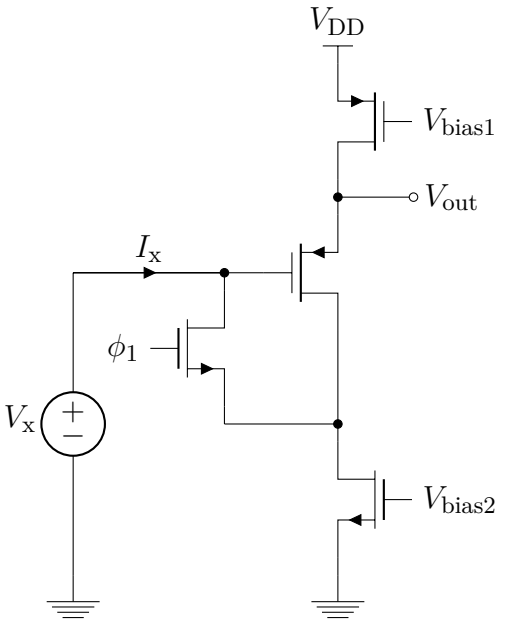

Figure 8.12: Test source to extract input resistance.

switch, but also due to the amplifier topology itself which can maintain a high resistance even when the input transistors are diode connected.

8 Discussion

Using the figure–of–merit optimization technique in order to scale the currents in M_1 and M_2 have been shown to result in a very energy efficient design. On the other hand, random mismatch variations in the current mirrors have not been taken into account during the simulations, which will likely result in variations in the current distribution. The analytical calculations show that the figure–of–merit is not very sensitive to variations in the optimal current distribution. Statistical Monte Carlo simulations can be basis for further investigations.

The noise performance of $16.3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ is well below the requirement for 5 dB noise figure. This matches the calculated value of $14.1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ very well. The additional noise is partly due to the noise sources not taken into account in the noise analysis, i.e. the current mirrors, and the added noise penalty introduced by the variable gain attenuator.

The proposed common–mode feedback switches are working as expected. On the other hand, no simulations using an ideal common–mode feedback circuit have been conducted. Therefore, providing such a circuit as a test bench for the proposed solution, would increase the confidence that the common–mode feedback circuit is working properly.

Another possible error source impacting the simulation result is the use of ideal spice capacitors. Obviously, using capacitors from the design kit with layout parasitics will yield a more realistic result. However, no layout has been made, and is subject for future work. Type of capacitor metal–insulator–metal (MIM),

metal–oxide–metal (MOM) or the like will also determine the amount of parasitic capacitance, and its impact on simulation results.

For the degeneration resistor a high resistive poly resistor model have been used. Clearly, this will give more realistic simulation results that using spice resistors. In addition, using this model yields a layout estimate given by the length and width of the resistor of 320 nm $\times$ 1.2 µm. Hence, if no parasitic capacitance is modeled for this device, it is not likely to be very large, due to the small resistor dimensions.

The designed amplifier achieves the required voltage gain of 20 dB as well as implementing variable gain i coarse steps. The simulated gain steps are 23.4 dB, 5.27 dB and -1.4 dB. This means that the gain range of the designed amplifier as approximately 25 dB, which increases the dynamic range of the designed amplifier by the same amount. On the other hand, the simulated gain settings did not match calculated values. Therefore larger capacitor sizes were required to reduce the attenuation in the capacitive divider. Of course, the simulated transfer function of the capacitive attenuator were much closer to the calculated values when tested by itself. In contrast, when connecting the capacitive divider to the amplifier, the attenuation in the passband was too large. This could be caused by the input resistance of the amplifier moving the poles of the capacitive attenuator. However, the input resistance is several giga ohms, which should lead a low frequency pole well below the passband for the piezoelectric transducer. Using the extracted input resistance and input capacitance of the amplifier yields a pole at

$$f = \frac{1}{2\pi}\frac{1}{\tau} = \frac{1}{2\pi}\frac{1}{10\,\mathrm{fF}\,\cdot\,5160\,\mathrm{G\Omega}} = 3\,\mathrm{Hz}, \tag{8.9}$$

which is well below passband of the piezoelectric transducer. Still from Figure 8.8 it is obvious ripples between 100 Hz and 1 kHz.

Also, accurate simulations rely on correct use of the simulator and meaningful test benches. The accuracy of simulation results are dependent of correct settings in the test bench and accurate simulation models. The transistor models used in this thesis are from a 180 nm AMS design kit. In fact, the simulated noise performance seem to agree very well with the analytical calculations, implying that the noise models are quite accurate.

Chapter 9

Conclusion

This thesis have shown the design of a low noise amplifier for medical ultrasound imaging that achieves a noise factor of less than 3 dB while draining only 17.3 µA from the 1.8 V supply. The excellent trade–off between power and accuracy have been achieved by applying a figure–of–merit optimization technique. Specifically, taking advantage of the high $g_{\mathrm{m}}/I_{\mathrm{d}}$ ratio of devices operating in subthreshold, have resulted in an optimal compromise between power consumption and noise performance for the designed front–end amplifier. This excellent trade–off between current consumption and input referred noise is also reflected in the low noise efficiency factor of 2.57, comparable with the current state of the art.

In order to reduce the dynamic range requirement for the low noise amplifier a variable gain attenuator have been proposed and simulated, and have been shown to be able to implement digitally controlled variable gain with a small increase in receiver noise factor and power consumption. By using a resistive degenerated differential pair at the input stage, a single–ended to differential conversion is achieved, at a stage where the signal swing is relatively limited, even at full scale output. The benefits of fully differential signaling in terms of noise and distortion suppression is then passed on to the next stage of the analog front–end. The versatile amplifier topology can be driven from a single–ended or a differential input signal source and can produce both gain and attenuation. Simulations show that the noise factor is well below the required value of 5 dB, even for single–input operation. In fact the inband noise level of 42.6 μV_{rms} is lower than the calculated noise from the transducer source, resulting in an analog front–end limited by both its noisy source and front–end amplifier rather than by the front–end amplifier alone. The simulation results show good agreement with the analytical calculations, implying a very energy efficient and robust design.

The designed low noise amplifier, combined with digital beamforming, can reduce the overall cost, size and power consumption of typical ultrasound front–end electronics, and allow for the integration of the analog front–end into the probe handle. In addition to increased integrability, the proposed solution may lead to an increase in the reliability and flexibility of phased array front–end signal–processing most often used in ultrasound applications.

1 Future Work

This thesis have presented the design and schematic level simulations of a low noise amplifier. Left out for future work is creating the layout and doing post layout simulation of the designed amplifier, and hopefully also conducting measurements on a fabricated chip. Post layout simulations will most likely result in a slower amplifier, as it also includes routing capacitances not modeled in the schematic simulations. Additional parasitic capacitances, such as layout parasitic capacitances of the degeneration resistor not already modeled might also further reduce the bandwidth of the amplifier. On the other hand, running corner simulations is typically underestimating the performance of the amplifier. In fact, the amplifier specifications are met at all process corners, which makes for a robust amplifier design.

In this thesis, the core of the transconductor have been optimized and designed. Future work could focus on the design of the output stage, consisting of the current mirror and appropriate load. If a voltage output is desired, a resistive load can be connected to the current mirror transistor M_3. In this case, the overall voltage gain is given by

$$A = \frac{R_{\mathrm{L}}}{R} B, \tag{9.1}$$

where R_{L} is the resistive load, R is the degeneration resistor, and B is the current mirror gain. This two stage amplifier can be implemented with a small increase in power consumption and input referred noise, depending on the current mirror ratio and the voltage gain of the first stage. In fact, for a current mirror ratio of 1, the total current consumption would only increase to 20.5 µA. Clearly, the increase in power consumption and input noise will result in a slightly higher noise efficiency factor, but it would likely still be comparable with current state of the art. In addition, the output stage resistive load will offer additional methods of adding variable gain, for instance by changing the current mirror ratio or more likely by varying the load resistor. On system level, the implementation of variable gain can be optimized using several of the methods sketched throughout this thesis, for instance by change the gain settings partly in a attenuator at the input, and simultaneously changing the degeneration resistor and load resistor. By doing so, smaller capacitor and resistor ratios can be employed, reducing the area overhead caused by the implementation of variable gain.

The variable gain attenuator is only considered for coarse gain steps. Of course, the gain steps can be changed in finer steps to better match the attenuation as the ultrasound wave propagates through tissue, by employing a more complex capacitor array with digital control logic. The area and power consumption overhead should not increase dramatically, as digital power consumption is not very high in 180 nm CMOS. The capacitive attenuator is only sketched in this thesis. Also left out for future work is a more thorough analysis with respect to well–known non ideal effects.

The gain range available for the attenuator is dependent on ratios and capacitor and is therefore a function of the input capacitance of the amplifier total area available. For a given input capacitance of the amplifier, the total gain range of the capacitive attenuator can be traded off with area consumption. Hence, this

holds the possibility of optimizing the capacitive attenuator with respect to the increase in dynamic range and area overhead.

2 Main Contributions

The designed amplifier in this thesis have accomplished an optimal trade–off between noise and power consumption by applying the method proposed in [10]. By exploring the design space available in this technique, a state of the art noise efficiency factor has been achieved. The main contribution of this thesis is the application of the figure–of–merit optimization technique, resulting in the design of a low noise amplifier only consuming 17.3 µA while maintaining a noise figure of less than 3 dB. In particular, the good noise and power trade–off can be traced back to using the high $g_{\mathrm{m}}/I_{\mathrm{d}}$ ratio of input transistors operating in subthreshold. Also, by exploring the figure–of–merit as a function of voltage gain have resulted in an extremely low optimal figure–of–merit, as very high gain values results in lower attainable figure–of–merit values. As this high gain setting is not suitable for large input signal, a capacitive attenuator have been proposed, that can be put in front of the amplifier to increase the dynamic range performance of the front–end. This attenuator ensures that the amplifier can maintain this high gain setting for all the input range, implying a very energy efficient design.

In order for in–probe analog front–end to be viable option, power consumption must be kept to a minimum, especially for 2–D ultrasound arrays where the number of channels are in the order of 1500 to 2000. For differential micro power amplifiers, power consumption in the common–mode feedback circuitry is a major specification. A major contribution of this thesis is the proposed switched common–mode feedback circuitry, which causes the output common–mode to be well controlled during the transmit period. The proposed common–mode feedback does not contribute to an increase in static power consumption, and only marginally increases the area consumption. The diode connection modifies the input impedance to the switch off–resistance, which usually is lower than the finite input resistance caused by gate leakage. However, off–resistance can be made large by using long transistors and other well–known techniques, such as bulk switching.

Additional contribution in this work is the derivation of small–signal design equations describing the amplifier, especially in terms of understanding how loss in the input transistors affect the overall voltage gain. The gain predicted when assuming that the input transistors are acting like ideal source–followers buffering the input voltage across the degeneration resistor deviates significantly from the actual gain achieved when the condition $g_{\mathrm{m1}} \gg 1/R$ is not satisfied. The transfer function derived in this thesis are matching the simulations results very well, also when the input buffers are quite lossy. This thesis have also shown that g_{m1} should not be chosen much smaller than $1/R$ in order to avoid unnecessary loss in the input transistors.

Bibliography

[1] J. Wild, "The Discovery of Ultrasonic Soft Tissue Reflection," *Proc. Int. Ultrason.*, vol. 1, pp. 229–234, 1981.

[2] M. Schafer and P. Lewin, "The Influence of Front–End Hardware on Digital Ultrasonic Imaging," *IEEE Transactions on Sonics and Ultrasonics*, vol. 31, pp. 295–306, 1984.

[3] P. Wells, *Biomedical Ultrasonics*. New York: Academic, 1 ed., 1977.

[4] T. Kwan and K. Martin, "An Adaptive Analog Continuous–Time CMOS Biquadratic Filter," *IEEE Journal of Solid–State Circuits*, vol. 26, pp. 859–867, 1991.

[5] C. Yang and A. Mason, "Process/Temperature Variation Tolerant Precision Signal Strength Indicator," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 55, pp. 722–729, 2008.

[6] O. Vermesan, L.-C. Blystad, R. Bahr, M. Hjelstuen, L. Beneteau, and B. Froelich, "A Mixed–Signal BiCMOS Front–End Signal Processor for High–Temperature Applications," *IEEE Journal of Solid–State Circuits*, vol. 41, pp. 1638–1647, 2006.

[7] D. A. Sobel and R. W. Brodersen, "A 1 Gb/s Mixed–Signal Baseband Analog Front–End for a 60 GHz Wireless Receiver," *IEEE Journal of Solid–State Circuits*, vol. 44, pp. 1281–1289, 2009.

[8] J. Rijns, "CMOS Low–Distortion High–Frequency Variable–Gain Amplifier," *IEEE Journal of Solid–State Circuits*, vol. 31, pp. 1029–1031, 1996.

[9] Y. Tang and R. L. Geiger, "A Highly Linear CMOS Amplifier for Variable Gain Amplifier Applications," *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS–2002.*, vol. 1, pp. 1029–1031, 2002.

[10] H. H. Hansen and T. Ytterdal, "Figure–of–merit Optimization of a Low Noise Amplifier in 180 nm CMOS," *Circuit Theory and Design, 2011. ECCTD 2011. European Conference on*, vol. 1, 2011. To Appear.

[11] Y. Ding and R. Harjani, *High–Linearity CMOS RF Front–End Circuits*. Springer, 1 ed., 2004.

[12] A. van der Ziel, "Noise in Solid–State Devices and Lasers," *Proceedings of the IEEE*, vol. 58, pp. 1178–1206, 1970.

[13] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: Wiley, 1 ed., 1987.

[14] Y. Tsividis, M. Banu, and J. Khoury, "Continuous–time MOSFET–C filters in VLSI," *IEEE Journal of Solid–State Circuits*, vol. 21, pp. 1015–1030, 1986.

[15] R. Castello, F. Montecchi, R. Alini, and A. Baschirotto, "A Very Linear BiCMOS Transconductor for High–Frequency Filter Applications," *IEEE Journal of Solid–State Circuits*, vol. 2, pp. 1364–1367, 1990.

[16] B. Wang, J. Hellums, and C. Sodini, "MOSFET Thermal Noise Modeling for Analog Integrated Circuits," *IEEE Journal of Solid–State Circuits*, vol. 29, pp. 833–835, 1994.

[17] W. Schottky, "Über Spontane Stromschwankungen in verschiedenen Elektrizitätsleitern," *Ann. Phys.*, vol. 57, pp. 541–567, 1918.

[18] H. Teng, S. Jang, and M. Juang, "A Unified Model High–Frequency Current Noise of MOSFETS," *Solid–State Electron.*, vol. 47, pp. 2043–2048, 2003.

[19] H. Lee and S. Mohammadi, "A Subthreshold Low Phase Noise CMOS LC VCO for Ultra Low Power Applications," *IEEE Microwave and Wireless Components Letters*, vol. 17, pp. 796–798, 2007.

[20] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A Unified Model for the Flicker Noise in Metal–Oxide–Semiconductor Field–Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 37, pp. 654–665, 1990.

[21] C. Jakobson, I. Bloom, and Y. Nemirovsky, "1/f Noise in CMOS Transistors for Analog Applications From Subthreshod to Saturation," *Solid–State Electronics*, vol. 42, pp. 1807–1817, 1998.

[22] R. L. Goldberg and S. W. Smith, "Multilayer Piezoelectric Ceramics for Two–Dimensional Transducers," *IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 41, pp. 761–771, 1994.

[23] J. M. Reid and J. Wild, "Ultrasonic Ranging for Cancer Diagnosis," *Electronics*, vol. 25, pp. 136–138, 1952.

[24] E. Vittoz, "Future of Analog in the VLSI Environment," *Proc. IEEE ISCAS'90*, vol. 1, pp. 1372–1375, 1990.

[25] E. Vittoz, "Low–Power Design: Ways to Approach the Limits," *Proc. IEEE Int. Solid–State Circuit Conference*, vol. 1, pp. 14–18, 1994.

[26] M. Karaman, E. Kolagasioglu, and A. Atalar, "A VLSI Receive Beamformer for Digital Ultrasound Imaging," *Proc. ICASSP 1992*, vol. 1, pp. 657–660, 1992.

[27] M. O'Donnell, W. Engeler, J. Pedicone, A. Itani, S. Noujaim, R. Dunki-Jacobs, W. Leue, C. Chalek, L. Smith, J. Piel, R. Harris, K. Welles, and W. Hinrichs, "Real–Time Phased Array Imaging Using Digital Beam Forming and Autonomous Channel Control," *Proceedings of the 1990 IEEE Ultrasonics Symposium*, vol. 1, pp. 1499–1502, 1990.

[28] R. Kuc and M. Schwartz, "Estimating the Acoustic Attenuation Coefficient Slope for Liver from Reflected Ultrasound Signals," *IEEE Transactions on Sonics and Ultrasonics*, vol. 26, pp. 333–362, 1979.

[29] R. Kuc, "Digital Filter–Models for Linear Media with Frequency Loss Characteristics," *Journal of the Acoustical Society of America*, vol. 1, pp. 35–40, 1981.

[30] I. Claesson and G. Salomonsson, "Frequency– and Depth–Dependent Compensation of Ultrasonic Signals," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 35, pp. 582–592, 1988.

[31] K. S. van Dyke, "The Piezo–Electric Resonator and its Equivalent Circuit," *Proc. IRE*, vol. 16, pp. 1178–1206, 1928.

[32] K. Hagimoto, Y. Miyagawa, Y. Miyamoto, M. Ohhata, T. Suzuki, and H. Kikuchi, "Over 10 Gb/s Regenerators Using Monolithic ICs for Lightwave Communication Systems," *IEEE Journal on Selected Areas in Communications*, vol. 9, no. 5, pp. 673–682, 1991.

[33] A. Wyszynski, "High-frequency Linear Tunable Single-Ended Voltage to Differential Current Converter," in *Circuits and Systems, Proceedings., Proceedings of the 38th Midwest Symposium on*, vol. 2, pp. 897–900, 1995.

[34] J. Lin, C. Zelley, O. Boric-Lubecke, P. Gould, and R. Yan, "A Silicon MMIC Active Balun/Buffer Amplifier With High Linearity and Low Residual Phase Noise," in *Microwave Symposium Digest. IEEE MTT-S International*, vol. 3, (Boston, MA), pp. 1289–1292, 2000.

[35] V. Ramakrishnan, J. N. Albers, R. N. Nottenburg, and W. J. Hillery, "Broadband Single-ended to Differential Signal Converter Embedded in Silicon Decision Circuit," *Electronics Letters*, vol. 31, no. 17, pp. 1400–1401, 1995.

[36] H. Ma, S. J. Fang, F. Lin, and H. Nakamura, "Novel Active Differential Phase Splitters in RFIC for Wireless Applications," in *Radio Frequency Integrated Circuits (RFIC) Symposium IEEE*, (Baltimore, MD), pp. 51–54, 1998.

[37] N. Larciprete, F. Loriga, P. Marietti, and A. Trifiletti, "A High CMRR GaAs Single-Input to Differential Convertor," *In GAAS 96 Proceedings of European Galium Arsenide Application Symposium*, vol. 1, pp. 1400–1401, 1996.

[38] E. Vittoz, "Micropower Techniques," *Design of VLSI Circuits for Telecommunications and Signal Processing*, vol. 1, 1993.

[39] E. Sánchez-Sinencio and A. G. Andreou, *Low–Voltage Mixed–Signal Circuits*. Wiley, 1 ed., 1999.

[40] R. van der Plassche, W. Sansen, and J. H. Huijsing, *Analog Circuit Design*. Kluwer Academic Publishers, 1 ed., 2002.

[41] R. H. Walden, "Analog to Digital Converter Survey and Analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, pp. 539–550, 1999.

[42] P. R. Kinget, "Device Mismatch and Tradeoffs in the Design of Analog Circuits," *IEEE Journal of Solid–State Circuits*, vol. 40, pp. 1212–1224, 2005.

[43] E. Vittoz, *Analog Circuit Design — Low–Power Low–Voltage Integrated Filters and Smart Power*. Kluwer Academic Publishers, 1 ed., 2002.

[44] T. Ytterdal and C. Wulff, "On the Energy Efficiency of Analog Circuits in Nanoscale CMOS Technologies," *Proc. of the* 20^{th} *International Conference on Microelectronics 2008 (ICM 2008)*, pp. 215–218, 2008.

[45] K. Najafi and K. D. Wise, "An Implantable Multielectrode Array with On–Chip Signal Processing," *IEEE Journal of Solid–State Circuits*, vol. 21, pp. 1035–1044, 1986.

[46] F. Forti and M. E. Wright, "Measurement of MOS Current Mismatch in the Weak Inversion Region," *IEEE Journal of Solid–State Circuits*, vol. 29, pp. 138–141, 1994.

[47] K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw–Hill, 1 ed., 1994.

[48] F. Silveira, D. Flandre, and P. G. A. Jespers, "A $g_{\mathrm{m}}/I_{\mathrm{D}}$ Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon–on–Insulator Micropower OTA," *IEEE Journal of Solid–State Circuits*, vol. 31, pp. 1314–1319, 1996.

[49] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford University Press, 5 ed., 2003.

[50] R. R. Harrison and C. Charles, "A Low-power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE Journal of Solid–State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.

[51] T. Singh, T. Sæther, and T. Ytterdal, "Feedback Biasing in Nanoscale CMOS Technologies," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 5, pp. 349–353, 2009.

[52] T. Singh, T. Sæther, and T. Ytterdal, "Common Source Amplifier with Feedback Biasing in 90 nm CMOS," in *Research in Microelectronics and Electronics 2006*, (Otranto), pp. 161–164, 2006.

[53] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, and C.-M. Huang, "A 1 V 11 fJ/Conversion–Step 10 bit 10 MS/s Asynchronous SAR ADC in 0.18 µm CMOS," *Symposium on VLSI Circuits Digest of Technical Papers*, vol. 1, pp. 241–242, 2010.

[54] T. H. Lee, *The Design of CMOS Radio–Frequency Integrated Circuits*. Cambridge University Press, 1 ed., 1998.

[55] C. Qian, J. Parramon, and E. Sánchez-Sinencio, "A Micropower Low–Noise Neural Recording Front–End Circuit for Epileptic Seizure Detection," *IEEE Journal of Solid–State Circuits*, vol. 46, pp. 1392–1405, 2011.

[56] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1 V 450 nW Fully Integrated Programmable Biomedical Sensor Interface Chip," *IEEE Journal of Solid–State Circuits*, vol. 44, pp. 1067–1077, 2009.

[57] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 µW 60 nV/$\sqrt{\text{Hz}}$ Capacitively–Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes," *IEEE Journal of Solid–State Circuits*, vol. 46, pp. 1534–1543, 2011.

[58] R. F. Yazicioglu, P. Merken, R. Puers, and C. V. Hoof, "A 200 µW Eight–Channel Acquisition ASIC for Ambulatory EEG System," *IEEE Journal of Solid–State Circuits*, vol. 43, pp. 3025–3038, 2008.

[59] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley, and A. Kelly, "A 2 µW 100 nV/$\sqrt{\text{Hz}}$ Chopper–Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," *IEEE Journal of Solid–State Circuits*, vol. 42, pp. 2934–2945, 2007.

[60] R. F. Yazicioglu, P. Merken, R. Puers, and C. V. Hoof, "A 60 µW 60 nV/$\sqrt{\text{Hz}}$ Readout Front–End for Portable Biopotential Acquisition Systems," *IEEE Journal of Solid–State Circuits*, vol. 42, pp. 1100–1110, 2007.

Appendix A

Figure–of–Merit and Noise Efficiency Factor

This chapter proves that the figure–of–merit proposed in [10] is proportional to the square of the more acknowledged noise efficiency factor proposed in [45] for white noise. For applications where flicker noise dominates, this no longer accurate. However, flicker noise can in most cases be reduced by proper design techniques.

First, the square of the noise efficiency is given by

$$\epsilon^2 = V_{\text{ni, rms}}^2 \cdot \frac{2I_{\text{tot}}}{\pi \cdot U_T \cdot 4kT \cdot \Delta f}, \tag{A.1}$$

where $V_{\text{ni, rms}}$ is the input referred rms noise voltage, I_{tot} is the total amplifier current drained from the supply and f is the amplifier bandwidth in Hertz. The input referred rms noise voltage can be found as

$$V_{\text{ni, rms}}^2 = \int_{\Delta f} v_{\text{n}}^2 \, \mathrm{d}f \,. \tag{A.2}$$

If the noise voltage is only given by white noise source, such as thermal noise or shot noise, this can be rewritten as

$$V_{\text{ni, rms}}^2 = \int_{\Delta f} v_{\text{n}}^2 \, \mathrm{d}f = v_{\text{n}}^2 \cdot \Delta f \,. \tag{A.3}$$

Inserting (A.3) into (A.1) yieds the desired equation,

$$\epsilon^2 = v_{\text{n}}^2 \cdot \frac{2I_{\text{tot}}}{\pi \cdot U_T \cdot 4kT} \propto v_{\text{n}}^2 \cdot I_{\text{t}} = \psi'_{\text{fom}} \,, \tag{A.4}$$

which proves that the figure–of–merit considering input referred noise voltage and current consumption is proportional to the square of the noise efficiency factor. Therefore, the figure–of–merit proposed in [10] can be regarded as useful tool when considering the trade–off between noise and power. The expressions are quite similar, especially when noting that the factor $4kT$ is used to simplify (A.4) as it normally is a part of v_{n}^2. U_T is also a scaling factor in order to get a dimensionless unit. Therefore, these two figure–of–merits are essentially equivalent formulations. However, the fact that the figure–of–merit in [10] can be analytically optimized makes for a much more useful tool in achieving a good noise and power trade–off.

Appendix B

Transistor Sizing

The design kit used for designing this amplifier is a 180 nm CMOS process from Austria Microsystems for Cadence 5. Typical design flow is as follow; First, the circuit schematic is drawn in Virtuoso Schematic Editor. Then, Virtuoso Analog Environment is used to extract netlists. Eldo is the preferred simulator, but as Eldo is not supported by the design kit, Spectre is chosen as simulator when extracting netlists. The spectre netlist is then converted to Eldo syntax using a Perl script. In the test benches, hSpice model files are used with in Eldo compatibility mode. Finally, Eldo is run as simulator for the relevant test benches.

1 Sizing NMOS Transistors

The test bench *tb_nmos.cir* was used to size the nmos transistors to have the appropriate $g_\mathrm{m}/I_\mathrm{d}$ values. For M_2 the value for W/L was found by looking at $g_\mathrm{m}/I_\mathrm{d}$ versus the normalized drain current $I_\mathrm{d}/(W/L)$ as shown in Figure 7.4. Then, the gate length was found by a trade–off between flicker noise and output resistance on one side and area and bandwidth on the other side.

```
*The comment line
*The CMOS0180 device library for typical corner
.compat
.lib tt_models.inc
.endcompat

* Schematic netlist
.inc ~/amskit/cds_setup/Sim/nmosgmid/spectre/schematic/netlist/netlist

.opt eps=1e-8
.opt aex
.opt numdgt=14
.opt nomod
.opt noerrmlog
.opt nomod
.opt notrc
.opt noascii
.opt noasciiplot
.opt extract_eval_final
.opt acm
```

```
*The transistor length
.param lp=2.5u
*The transistor width
.param wp=0.5u

*Transistor current
.param id = 10u

*Drain current
id vdd g dc id
vss s 0 dc 0

*Biasing
vdd vdd 0 1.8

.op

.extract dc opmode(xtn0.m0)

.extract dc label=gain gm(xtn0.m0)/gds(xtn0.m0)
.extract dc label=gm_over_id gm(xtn0.m0)/id(xtn0.m0)
.extract dc label=cgg cgg(xtn0.m0)
.extract dc label=vt vth(xtn0.m0)

*Transistor transconductance, the transistors in 90nm are subcircuits
.plot dc gm(xtn0.m0)

*Drain source saturation voltage, this is roughly equal to our VEFF
.plot dc vdss(xtn0.m0)'

*Calculate & plot eta1
.defwave eta1 = vdss(xtn0.m0) *gm(xtn0.m0)/(2*i(xtn0.m0.d))
.plot dc w(eta1)

*Calculate & plot gm over id
.defwave gm_id = abs(gm(xtn0.m0)/id(xtn0.m0))
.plot dc w(gm_id)

*Calculate & plot intrinsic frequency
.defwave f_t = abs(gm(xtn0.m0)/(2*pi*(cgs(xtn0.m0)+cdb(xtn0.m0))))
.plot dc w(f_t)
.defwave i_d2 = id(xtn0.m0)

*Calculate & plot intrinsic gain
.defwave i_g = abs(gm(xtn0.m0)/gds(xtn0.m0))
.plot dc w(i_g)

*Calculate & plot output conductance gain.
*Important for current mirrors
.defwave gds = gds(xtn0.m0)
.plot dc w(gds)

*Calculate & plot FOM = f_t*gm/id
.defwave fom = f_t*gm_id*i_g
```

```
.plot dc w(fom)

*Run a dc analysis and sweep the normalized drain current
.dc param id dec 10 1n 100u

.end
```

2 Sizing PMOS Transistors

```
*The comment line
*The CMOS0180 device library for typical corner
.compat
.lib tt_models.inc
.endcompat

* Schematic netlist
.inc ~/amskit/cds_setup/Sim/pmosgmid/spectre/schematic/netlist/netlist

.opt eps=1e-8
.opt aex
.opt numdgt=14
.opt nomod
.opt noerrmlog
.opt nomod
.opt notrc
.opt noascii
.opt noasciiplot
.opt extract_eval_final
.opt acm

*The transistor length
.param ln=0.22u
*The transistor width
.param wn=100*ln

*Transistor current
.param id = 10u

*Drain current
id g 0 dc id

*Biasing
vdd vdd 0 1.8

.op

.extract dc opmode(xtp0.m0)
.extract dc label=vt vth(xtp0.m0)

.extract dc label=gain gm(xtp0.m0)/gds(xtp0.m0)
.extract dc label=gm_over_id gm(xtp0.m0)/id(xtp0.m0)
.extract dc label=cgg cgg(xtp0.m0)
```

```
*Transistor transconductance, the transistors in 90nm are subcircuits
.plot dc gm(xtp0.m0)

*Drain source saturation voltage, this is roughly equal to our VEFF
.plot dc vdss(xtp0.m0)

*Calculate & plot eta1
.defwave eta1 = vdss(xtp0.m0) *gm(xtp0.m0)/(2*i(xtp0.m0.d))
.plot dc w(eta1)

*Calculate & plot gm over id
.defwave gm_id = abs(gm(xtp0.m0)/id(xtp0.m0))
.plot dc w(gm_id)

*Calculate & plot intrinsic frequency
.defwave f_t = abs(gm(xtp0.m0)/(2*pi*(cgs(xtp0.m0)+cdb(xtp0.m0))))
.plot dc w(f_t)

*Calculate & plot intrinsic gain
.defwave i_g = abs(gm(xtp0.m0)/gds(xtp0.m0))
.plot dc w(i_g)

*Calculate & plot output conductance gain.
*Important for current mirrors
.defwave gds = gds(xtp0.m0)
.plot dc w(gds)

*Calculate & plot FOM = f_t*gm/id
.defwave fom = f_t*gm_id*i_g
.plot dc w(fom)

*Run a dc analysis and sweep the normalized drain current
.dc param id dec 10 100n 100u

.end
```

Appendix C

Amplifier Schematic and Netlist

Figure C.1 shows the schematic for the amplifier including node definitions. This circuit schematic is used in the various test benches. The different values for transistor dimensions W/L found in the design process is specified in the test benches.

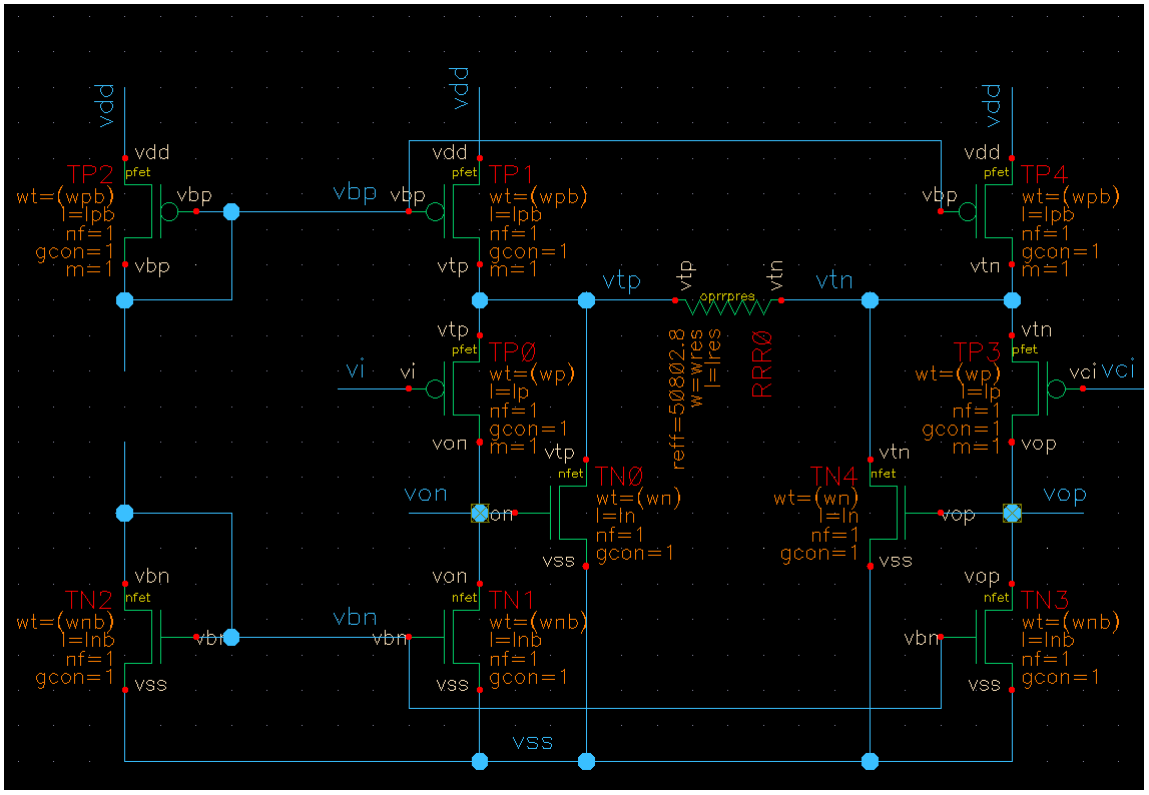

Figure C.1: Amplifier Schematic.

```
* Converted netlist on 6/7/2011 14:51:37
* // Library name: prosjekthans
* // Cell name: pzt_lna
* // View name: schematic

.subckt pztlna vi vci vtp vtn vbp vbn vdd vss vop von
```

```
xrrr0 (vtp vtn vss) oprrpres r=50802.8 w=wres l=lres m=1 par=1 pbar=1
s=1 dtemp=0 sh=1 rsx=50 bp=3

xtn3 (vop vbn vss vss) nfet l=lnb w=wnb2 nf=1 m=1 par=1
ad=((wnb2-6e-08)*4.3e-07) as=((wnb2-6e-08)*4.3e-07)
pd=(2*(wnb2-6e-08)+2*4.3e-07) ps=(2*(wnb2-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wnb2-6e-08) nrs=2.6e-07/(wnb2-6e-08)
gcon=1 lstis=2 rsx=50 dtemp=0

xtn4 (vtn vop vss vss) nfet l=ln w=wn nf=1 m=1 par=1
ad=((wn-6e-08)*4.3e-07) as=((wn-6e-08)*4.3e-07)
pd=(2*(wn-6e-08)+2*4.3e-07) ps=(2*(wn-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wn-6e-08) nrs=2.6e-07/(wn-6e-08)
gcon=1 lstis=2 rsx=50 dtemp=0

xtn2 (vbn vbn vss vss) nfet l=lnb w=wnb1 nf=1 m=1 par=1
ad=((wnb1-6e-08)*4.3e-07) as=((wnb1-6e-08)*4.3e-07)
pd=(2*(wnb1-6e-08)+2*4.3e-07) ps=(2*(wnb1-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wnb1-6e-08) nrs=2.6e-07/(wnb1-6e-08)
gcon=1 lstis=2 rsx=50 dtemp=0

xtn1 (von vbn vss vss) nfet l=lnb w=wnb2 nf=1 m=1 par=1
ad=((wnb2-6e-08)*4.3e-07) as=((wnb2-6e-08)*4.3e-07)
pd=(2*(wnb2-6e-08)+2*4.3e-07) ps=(2*(wnb2-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wnb2-6e-08) nrs=2.6e-07/(wnb2-6e-08)
gcon=1 lstis=2 rsx=50 dtemp=0

xtn0 (vtp von vss vss) nfet l=ln w=wn nf=1 m=1 par=1
ad=((wn-6e-08)*4.3e-07) as=((wn-6e-08)*4.3e-07)
pd=(2*(wn-6e-08)+2*4.3e-07) ps=(2*(wn-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wn-6e-08) nrs=2.6e-07/(wn-6e-08)
gcon=1 lstis=2 rsx=50 dtemp=0

xtp3 (vop vci vtn vtn) pfet l=lp w=wp nf=nf m=1 par=1
ad=((wp-6e-08)*4.3e-07) as=((wp-6e-08)*4.3e-07)
pd=(2*(wp-6e-08)+2*4.3e-07) ps=(2*(wp-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wp-6e-08) nrs=2.6e-07/(wp-6e-08)
gcon=1 rsx=50 dtemp=0

xtp4 (vtn vbp vdd vdd) pfet l=lpb w=wpb2 nf=1 m=1 par=1
ad=((wpb2-6e-08)*4.3e-07) as=((wpb2-6e-08)*4.3e-07)
pd=(2*(wpb2-6e-08)+2*4.3e-07) ps=(2*(wpb2-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wpb2-6e-08) nrs=2.6e-07/(wpb2-6e-08)
gcon=1 rsx=50 dtemp=0

xtp2 (vbp vbp vdd vdd) pfet l=lpb w=wpb1 nf=1 m=1 par=1
ad=((wpb1-6e-08)*4.3e-07) as=((wpb1-6e-08)*4.3e-07)
pd=(2*(wpb1-6e-08)+2*4.3e-07) ps=(2*(wpb1-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wpb1-6e-08) nrs=2.6e-07/(wpb1-6e-08)
gcon=1 rsx=50 dtemp=0

xtp1 (vtp vbp vdd vdd) pfet l=lpb w=wpb2 nf=1 m=1 par=1
ad=((wpb2-6e-08)*4.3e-07) as=((wpb2-6e-08)*4.3e-07)
pd=(2*(wpb2-6e-08)+2*4.3e-07) ps=(2*(wpb2-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wpb2-6e-08) nrs=2.6e-07/(wpb2-6e-08)
```

```
gcon=1 rsx=50 dtemp=0

xtp0 (von vi vtp vtp) pfet l=lp w=wp nf=nf m=1 par=1
ad=((wp-6e-08)*4.3e-07) as=((wp-6e-08)*4.3e-07)
pd=(2*(wp-6e-08)+2*4.3e-07) ps=(2*(wp-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wp-6e-08) nrs=2.6e-07/(wp-6e-08)
gcon=1 rsx=50 dtemp=0

.ends
```

Appendix D

Verifying Design Through Simulations

In this chapter, the test benches used to verify the amplifier performance is included. The different test benches are designed to test the different specifications.

1 DC Test Bench

```
*The comment line
*The CMOS0180 device library for typical corner
*Change manually, as .alter is not compatible with .compat
*tt_models.int, ss_models.inc and ff_models.inc
.compat
.lib tt_models.inc
.endcompat

* Schematic netlist and PZT Model
.inc ~/amskit/cds_setup/Sim/pzt_lna/spectre/schematic/netlist/netlist

.opt eps=1e-8
.opt aex
.opt numdgt=14
.opt nomod
.opt noerrmlog
.opt notrc
.opt noascii
.opt noasciiplot
.opt extract_eval_final
.opt acm
.opt nowarn=276

*Current distribution
.param p=4.5

*Number of fingers in M1 and M1'
.param nf=8

*The transistor lengths
.param lp=220n
```

```
.param lpb2=1.5u
.param ln=3u
.param lnb2=5u
.param lnb='lnb2'
.param lpb='lpb2'
*The transistor widths
.param wp='24u/nf'
.param wn=0.5u
.param wpb2=3u
.param wnb2=0.8u
.param wnb1=0.8u
.param wpb1=3u

*Degeneration resisor generation
.param lres=320n
.param wres=1.2u
*Transistor switch dimensions
.param lsw=320n
.param wsw=1.2u

*Transistor current
.param ibias1 = 8.5u
.param ibias2 = 7.1u

*Supply voltage, can be varied plus minus 10 %
.param vdd = 1.8
.param vx = 0.7

*Load capacitance
cla von 0 25f
clb vop 0 25f

*Drain current and biasing
ibias1 vbp 0 dc ibias1
ibias2 vdd vbn dc ibias2
vss vss 0 dc 0
vdd vdd 0 dc vdd
vci vcic 0 dc 0.8
cbc vcic vci 1G

*Amplifier subcircuit
xamp vi vci vtp vtn vbp vbn vdd vss vop von pztlna !noise=0

*Ultrasund Pulse Repitition Frequency
vclkb clkb 0 pulse(0 0 0 10ps 10ps 1us 240us)

*Transistor nmos switch
.subckt tswitch vi vc vo
xtn5 (vi vc vo vo) nfet l=lsw w=wsw nf=1 m=1 par=1 ad=((wsw-6e-08)*4.3e-07)
as=((wsw-6e-08)*4.3e-07) pd=(2*(wsw-6e-08)+2*4.3e-07) ps=(2*(wsw-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wsw-6e-08) nrs=2.6e-07/(wsw-6e-08) gcon=1 lstis=2 rsx=50 dtemp=0
.ends

*Switch Model voltage controlled resistor
.subckt mswitch a c z
```

```
rr a z value={eval(v(c)>0.5?100:1g)}
.ends

*Switched feedback
x1a von vdd vi tswitch !noise=0
x1b vop vdd vci tswitch !noise=0

*Input resistance simulation
*vi vi 0 dc vx
*.extract dc label=rx vx/i(vi)
*RX = 5.15961798556138E+12 r=roff
*RX = 1.21126762534778E+06 r=on


.op
.extract dc opmode(xamp.xtp0.m0)
.extract dc opmode(xamp.xtp3.m0)
.extract dc opmode(xamp.xtn0.m0)
.extract dc opmode(xamp.xtn4.m0)
.extract dc opmode(xamp.xtp1.m0)
.extract dc opmode(xamp.xtp4.m0)
.extract dc opmode(xamp.xtn1.m0)
.extract dc opmode(xamp.xtn3.m0)
.extract dc opmode(xamp.xtp2.m0)
.extract dc opmode(xamp.xtn2.m0)

*Extract important small-signal parameters like gm/id,
*intrinsic gain and input capacitance
.extract dc label=gain_m1a gm(xamp.xtp0.m0)/gds(xamp.xtp0.m0)
.extract dc label=gm_over_id_m1a gm(xamp.xtp0.m0)/id(xamp.xtp0.m0)
.extract dc label=cgg_m1a cgg(xamp.xtp0.m0)

.extract dc label=gain_m1b gm(xamp.xtp3.m0)/gds(xamp.xtp3.m0)
.extract dc label=gm_over_id_m1b gm(xamp.xtp3.m0)/id(xamp.xtp3.m0)
.extract dc label=cgg_m1b cgg(xamp.xtp3.m0)

.extract dc label=gain_m2a gm(xamp.xtn0.m0)/gds(xamp.xtn0.m0)
.extract dc label=gm_over_id_m2a gm(xamp.xtn0.m0)/id(xamp.xtn0.m0)
.extract dc label=cgg_m2a cgg(xamp.xtn0.m0)

.extract dc label=gain_m2b gm(xamp.xtn4.m0)/gds(xamp.xtn4.m0)
.extract dc label=gm_over_id_m2b gm(xamp.xtn4.m0)/id(xamp.xtn4.m0)
.extract dc label=cgg_m2b cgg(xamp.xtn4.m0)


*Extract bias currents
.extract dc label=id_m1a id(xamp.xtp0.m0)
.extract dc label=id_m1b id(xamp.xtp3.m0)
.extract dc label=id_m2a id(xamp.xtn0.m0)
.extract dc label=id_m2b id(xamp.xtn4.m0)
.extract dc label=id_mbp1 id(xamp.xtp2.m0)
.extract dc label=id_mbp1 id(xamp.xtp2.m0)
.extract dc label=id_mbp2a id(xamp.xtp1.m0)
.extract dc label=id_mbp2b id(xamp.xtp4.m0)
.extract dc label=id_mbn1 id(xamp.xtn2.m0)
```

```
.extract dc label=id_mbn2a id(xamp.xtn1.m0)
.extract dc label=id_mbn2b id(xamp.xtn3.m0)

.extract dc label=gds_m1 gds(xamp.xtp0.m0)
.extract dc label=gds_m1b gds(xamp.xtp3.m0)
.extract dc label=gds_m2 gds(xamp.xtn0.m0)
.extract dc label=gds_m2b gds(xamp.xtn4.m0)
.extract dc label=gds_mbp1 gds(xamp.xtp2.m0)
.extract dc label=gds_mbp2 gds(xamp.xtp1.m0)
.extract dc label=gds_mbn1 gds(xamp.xtn2.m0)
.extract dc label=gds_mbn2 gds(xamp.xtn1.m0)
.extract dc label=gds_mbn2 gds(xamp.xtn3.m0)
.extract dc label=gds_mbp2 gds(xamp.xtp4.m0)

*Transistor transconductance, the transistors in 180nm are subcircuits
.plot dc gm(xamp.xtn0.m0)
.plot dc gm(xamp.xtp0.m0)
.plot dc gm(xamp.xtn1.m0)
.plot dc gm(xamp.xtp1.m0)

*Transistor output conductance, the transistors in 180nm are subcircuits
.plot dc gds(xamp.xtn0.m0)
.plot dc gds(xamp.xtp0.m0)
.plot dc gds(xamp.xtn1.m0)
.plot dc gds(xamp.xtp1.m0)

*Drain source saturation voltage, this is roughly equal to our VEFF
.plot dc vdss(xamp.xtn0.m0)
.plot dc vdss(xamp.xtp0.m0)
.plot dc vdss(xamp.xtn1.m0)
.plot dc vdss(xamp.xtp1.m0)
.plot dc vdss(xamp.xtp2.m0)
.plot dc vdss(xamp.xtn2.m0)
.plot dc vdss(xamp.xtp3.m0)
.plot dc vdss(xamp.xtn3.m0)
.plot dc vdss(xamp.xtp4.m0)
.plot dc vdss(xamp.xtn3.m0)

*Calculate & plot gm over id
.defwave gm_id_m2 = abs(gm(xamp.xtn0.m0)/id(xamp.xtn0.m0))
.plot dc w(gm_id_m2)
.defwave gm_id_m1 = abs(gm(xamp.xtp0.m0)/id(xamp.xtp0.m0))
.plot dc w(gm_id_m1)
.defwave gm_id_mbn = abs(gm(xamp.xtn1.m0)/id(xamp.xtn1.m0))
.plot dc w(gm_id_mbn)
.defwave gm_id_mbp = abs(gm(xamp.xtp1.m0)/id(xamp.xtp1.m0))
.plot dc w(gm_id_mbp)

.dc
.extract dc
.probe v

.end
```

2 AC Test Bench

```
*The comment line
*The CMOS0180 device library for typical corner
*Change manually, as .alter is not compatible with .compat
*tt_models.int, ss_models.inc and ff_models.inc
.compat
.lib key=mos tt_models.inc
.endcompat


* Schematic netlist and PZT Model
.inc ~/amskit/cds_setup/Sim/pzt_lna/spectre/schematic/netlist/netlist

.opt eps=1e-8
.opt aex
.opt numdgt=14
.opt nomod
.opt noerrmlog
.opt notrc
.opt noascii
.opt noasciiplot
.opt extract_eval_final
.opt acm
.opt nowarn=276

*Current distribution
.param p=4.5

*Number of fingers in M1 and M1'
.param nf=8

*The transistor lengths
.param lp=220n
.param lpb2=1.5u
.param ln=2.5u
.param lnb2=5u
.param lnb='1*lnb2'
.param lpb='1*lpb2'
*The transistor widths
.param wp='24u/nf'
.param wn=0.5u
.param wpb2=3u
.param wnb2=0.8u
.param wnb1=0.8u
.param wpb1=3u

*Degeneration resisor generation
.param lres=320n
.param wres=1.2u

*Transistor switch dimensions
.param lsw=320n
.param wsw=1.2u
```

```
*Transistor current and supply voltage
.param ibias1 = 8.5u
.param ibias2 = 7.1u

*Supply voltage, can be varied from 1.6 to 2.0
.param vdd = 1.8

*Load capacitance
cla von 0 25f
clb vop 0 25f

*Drain current and biasing
ibias1 vbp 0 dc ibias1
ibias2 vdd vbn dc ibias2
vss vss 0 dc 0
vdd vdd 0 dc vdd
vci vcic 0 dc 0.8
cbc vcic vci 200f

*Signal Source including bonding parasitics
vin vin 0 dc 0 ac 1
lbond vin vi 1n
cbond vi 0 100f

*Amplifier subcircuit
xamp vi vci vtp vtn vbp vbn vdd vss vop von pztlna !noise=0

*Ultrasund Pulse Repitition Frequency
vclkb clkb 0 pulse(0 0 0 10ps 10ps 1us 240us)

*Transistor nmos switch
.subckt tswitch vi vc vo
xtn5 (vi vc vo vo) nfet l=lsw w=wsw nf=1 m=1 par=1 ad=((wsw-6e-08)*4.3e-07)
as=((wsw-6e-08)*4.3e-07) pd=(2*(wsw-6e-08)+2*4.3e-07) ps=(2*(wsw-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wsw-6e-08) nrs=2.6e-07/(wsw-6e-08) gcon=1 lstis=2 rsx=50 dtemp=0
.ends

*Switch Model voltage controlled resistor
.subckt mswitch a c z
rr a z value={eval(v(c)>0.5?100:1g)}
.ends

*Capacitive divider - vga
.subckt capdiv vi vo vc1 vc2 vss
xsw1a vinp vc1 vo tswitch
c1a vi vo 10f
c1b vi vinp 180f
xsw2a vcc vc2 vss tswitch
c1c vcc vo 180f
.ends

xcapdiv vin vi vss vdd vss capdiv

*Switched feedback
x1a von 0 vi tswitch !noise=0
```

```
x1b vop 0 vci tswitch !noise=0

.op
.extract dc opmode(xamp.xtp0.m0)
.extract dc opmode(xamp.xtp3.m0)
.extract dc opmode(xamp.xtn0.m0)
.extract dc opmode(xamp.xtn4.m0)
.extract dc opmode(xamp.xtp1.m0)
.extract dc opmode(xamp.xtp4.m0)
.extract dc opmode(xamp.xtn1.m0)
.extract dc opmode(xamp.xtn3.m0)
.extract dc opmode(xamp.xtp2.m0)
.extract dc opmode(xamp.xtn2.m0)

*Extract important small-signal parameters like gm/id,
*intrinsic gain and input capacitance
.extract dc label=gain_m1a gm(xamp.xtp0.m0)/gds(xamp.xtp0.m0)
.extract dc label=gm_over_id_m1a gm(xamp.xtp0.m0)/id(xamp.xtp0.m0)
.extract dc label=cgg_m1a cgg(xamp.xtp0.m0)

.extract dc label=gain_m1b gm(xamp.xtp3.m0)/gds(xamp.xtp3.m0)
.extract dc label=gm_over_id_m1b gm(xamp.xtp3.m0)/id(xamp.xtp3.m0)
.extract dc label=cgg_m1b cgg(xamp.xtp3.m0)

.extract dc label=gain_m2a gm(xamp.xtn0.m0)/gds(xamp.xtn0.m0)
.extract dc label=gm_over_id_m2a gm(xamp.xtn0.m0)/id(xamp.xtn0.m0)
.extract dc label=cgg_m2a cgg(xamp.xtn0.m0)

.extract dc label=gain_m2b gm(xamp.xtn4.m0)/gds(xamp.xtn4.m0)
.extract dc label=gm_over_id_m2b gm(xamp.xtn4.m0)/id(xamp.xtn4.m0)
.extract dc label=cgg_m2b cgg(xamp.xtn4.m0)


*Extract bias currents
.extract dc label=id_m1a id(xamp.xtp0.m0)
.extract dc label=id_m1b id(xamp.xtp3.m0)
.extract dc label=id_m2a id(xamp.xtn0.m0)
.extract dc label=id_m2b id(xamp.xtn4.m0)
.extract dc label=id_mbp1 id(xamp.xtp2.m0)
.extract dc label=id_mbp1 id(xamp.xtp2.m0)
.extract dc label=id_mbp2a id(xamp.xtp1.m0)
.extract dc label=id_mbp2b id(xamp.xtp4.m0)
.extract dc label=id_mbn1 id(xamp.xtn2.m0)
.extract dc label=id_mbn2a id(xamp.xtn1.m0)
.extract dc label=id_mbn2b id(xamp.xtn3.m0)

.extract dc label=gds_m1 gds(xamp.xtp0.m0)
.extract dc label=gds_m1b gds(xamp.xtp3.m0)
.extract dc label=gds_m2 gds(xamp.xtn0.m0)
.extract dc label=gds_m2b gds(xamp.xtn4.m0)
.extract dc label=gds_mbp1 gds(xamp.xtp2.m0)
.extract dc label=gds_mbp2 gds(xamp.xtp1.m0)
.extract dc label=gds_mbn1 gds(xamp.xtn2.m0)
.extract dc label=gds_mbn2 gds(xamp.xtn1.m0)
.extract dc label=gds_mbn2 gds(xamp.xtn3.m0)
```

```
.extract dc label=gds_mbp2 gds(xamp.xtp4.m0)

*Transistor transconductance, the transistors in 180nm are subcircuits
.plot dc gm(xamp.xtn0.m0)
.plot dc gm(xamp.xtp0.m0)
.plot dc gm(xamp.xtn1.m0)
.plot dc gm(xamp.xtp1.m0)

*Transistor output conductance, the transistors in 180nm are subcircuits
.plot dc gds(xamp.xtn0.m0)
.plot dc gds(xamp.xtp0.m0)
.plot dc gds(xamp.xtn1.m0)
.plot dc gds(xamp.xtp1.m0)

*Drain source saturation voltage, this is roughly equal to our VEFF
.plot dc vdss(xamp.xtn0.m0)
.plot dc vdss(xamp.xtp0.m0)
.plot dc vdss(xamp.xtn1.m0)
.plot dc vdss(xamp.xtp1.m0)
.plot dc vdss(xamp.xtp2.m0)
.plot dc vdss(xamp.xtn2.m0)
.plot dc vdss(xamp.xtp3.m0)
.plot dc vdss(xamp.xtn3.m0)
.plot dc vdss(xamp.xtp4.m0)
.plot dc vdss(xamp.xtn3.m0)

*Calculate & plot gm over id
.defwave gm_id_m2 = abs(gm(xamp.xtn0.m0)/id(xamp.xtn0.m0))
.plot dc w(gm_id_m2)
.defwave gm_id_m1 = abs(gm(xamp.xtp0.m0)/id(xamp.xtp0.m0))
.plot dc w(gm_id_m1)
.defwave gm_id_mbn = abs(gm(xamp.xtn1.m0)/id(xamp.xtn1.m0))
.plot dc w(gm_id_mbn)
.defwave gm_id_mbp = abs(gm(xamp.xtp1.m0)/id(xamp.xtp1.m0))
.plot dc w(gm_id_mbp)

*Calculate output voltage
.defwave voutdm = '(v(vop)-v(von))'
.plot ac w(voutdm)
.defwave voutcm = '(v(vop)+v(von))/2'
.plot ac w(voutcm)

.dc
.op

*Ac analysis
.AC      dec      500   1 1g
.noise   v(vop,von) vdd   2
.noise   v(von) vdd       2
.noise   v(vop) vdd       2
.plot noise inoise onoise

.probe v

*Sweep temperatures
```

```
.temp 27 50
.end
```

3 Transient Analysis Test Bench

```
*The comment line
*The CMOS0180 device library for typical corner
*tt_models.int, ss_models.inc and ff_models.inc
.compat
.lib tt_models.inc
.endcompat

* Schematic netlist and PZT Model
.inc ~/amskit/cds_setup/Sim/pzt_lna/spectre/schematic/netlist/netlist
.inc ~/amskit/cds_setup/ICE_Trondheim_Spice.cir

.OPTION VOLTAGE_LOOP_SEVERITY = WARNING
.option iem

.opt eps=1e-8
.opt aex
.opt numdgt=14
.opt nomod
.opt noerrmlog
.opt notrc
.opt noascii
.opt noasciiplot
.opt extract_eval_final
.opt acm
.opt nowarn=276
.opt nowarn=459

*Current distribution
.param p=4.5

*Number of fingers in M1 and M1'
.param nf=8
.param r=15k

*The transistor lengths
.param lp=220n
.param lpb2=1.5u
.param ln=2.5u
.param lnb2=5u
.param lnb='1*lnb2'
.param lpb='1*lpb2'
*The transistor widths
.param wp='24u/nf'
.param wn=0.5u
.param wpb2=3u
.param wnb2=0.85u
.param wnb1=0.85u
.param wpb1=3u

*Degeneration resisor generation
```

```
.param lres=320n
.param wres=1.2u

*Transistor switch dimensions
.param lsw=320n
.param wsw=1.2u

*Transistor current
.param ibias1 = 8.5u
.param ibias2 = 7.1u

*Supply voltage, can vary plus minus 10 %
.param vdd = 1.8

*Pulse train
.param vpp='0.8*70.0k'
.param vpn='-0.8*70.0k'

*Load capacitance
cla von 0 25f
clb vop 0 25f

*Drain current and biasing
ibias1 vbp 0 dc ibias1
ibias2 vdd vbn dc ibias2
vss vss 0 dc 0
vdd vdd 0 dc vdd
vci vcic 0 dc 0.8
cbc vcic vci 200f

*Signal Source and bonding parasitics
vin vinn 0 dc 0 ac 1 sin(0 12.5m 7.025146484meg)
lbond vinn vin 1n
cbond vin 0 100f
xcapdiv vin vi vdd vss vss capdiv

*Capacitive divider - vga
.subckt capdiv vi vo vc1 vc2 vss
xsw1a vinp vc1 vo tswitch
c1a vi vo 20f
c1b vi vinp 180f
xsw2a vcc vc2 vss tswitch
c1c vcc vo 190f
.ends

*Sampling Clock signal
vclk clk 0 pulse(0 1.8 0 10ps 10ps 10ns 20ns)

*Transmit 1.5 periode of pulsetrain (square wave)
vtx vtx 0 pwl (1140n 0 1141.45n vpp 1281.45n vpp 1284.35n vpn 1424.35n
vpn 1425.8n 0 1428.7n vpp 1568.7n vpp 1570.15n 0)

*PZT Source
*xpzt_tx itx vtx base xdcr
*fsource irx 0 xpzt_tx.vzr 1
```

```
*esource irx 0 itx 0 1
*xpzt_rx irx vinn base xdcr
*lbond vinn vin 1n
*cbond vin 0 100f

*Amplifier subcircuit
xamp vi vci vtp vtn vbp vbn vdd vss vop von pztlna !noise=0

*Ultrasund Pulse Repitition Frequency
vclkb clkb 0 pulse(0 vdd 0 10ps 10ps 1us 240us)
vc1 vc1 0 pulse(0 vdd 2.85us 10ps 10ps 120us 240us)
vc2 vc2 0 pulse(0 vdd 0 10ps 10ps 2.85us 240us)

*Switch Model voltage controlled resistor
.subckt mswitch a c z
rr a z value={eval(v(c)>0.5?100:1g)}
.ends

*Transistor nmos switch
.subckt tswitch vi vc vo
xtn5 (vi vc vo vo) nfet l=lsw w=wsw nf=1 m=1 par=1 ad=((wsw-6e-08)*4.3e-07)
as=((wsw-6e-08)*4.3e-07) pd=(2*(wsw-6e-08)+2*4.3e-07) ps=(2*(wsw-6e-08)+2*4.3e-07)
nrd=2.6e-07/(wsw-6e-08) nrs=2.6e-07/(wsw-6e-08) gcon=1 lstis=2 rsx=50 dtemp=0
.ends

*Switched feedback
*x1a von clkb vi mswitch !noise=0
*x1b vop clkb vci mswitch !noise=0
x1a von clkb vi tswitch !noise=0
x1b vop clkb vci tswitch !noise=0

.op
.extract dc opmode(xamp.xtp0.m0)
.extract dc opmode(xamp.xtp3.m0)
.extract dc opmode(xamp.xtn0.m0)
.extract dc opmode(xamp.xtn4.m0)
.extract dc opmode(xamp.xtp1.m0)
.extract dc opmode(xamp.xtp4.m0)
.extract dc opmode(xamp.xtn1.m0)
.extract dc opmode(xamp.xtn3.m0)
.extract dc opmode(xamp.xtp2.m0)
.extract dc opmode(xamp.xtn2.m0)

*Extract important small-signal parameters like gm/id,
*intrinsic gain and input capacitance
.extract dc label=gain_m1a gm(xamp.xtp0.m0)/gds(xamp.xtp0.m0)
.extract dc label=gm_over_id_m1a gm(xamp.xtp0.m0)/id(xamp.xtp0.m0)
.extract dc label=cgg_m1a cgg(xamp.xtp0.m0)

.extract dc label=gain_m1b gm(xamp.xtp3.m0)/gds(xamp.xtp3.m0)
.extract dc label=gm_over_id_m1b gm(xamp.xtp3.m0)/id(xamp.xtp3.m0)
.extract dc label=cgg_m1b cgg(xamp.xtp3.m0)

.extract dc label=gain_m2a gm(xamp.xtn0.m0)/gds(xamp.xtn0.m0)
.extract dc label=gm_over_id_m2a gm(xamp.xtn0.m0)/id(xamp.xtn0.m0)
```

```
.extract dc label=cgg_m2a cgg(xamp.xtn0.m0)

.extract dc label=gain_m2b gm(xamp.xtn4.m0)/gds(xamp.xtn4.m0)
.extract dc label=gm_over_id_m2b gm(xamp.xtn4.m0)/id(xamp.xtn4.m0)
.extract dc label=cgg_m2b cgg(xamp.xtn4.m0)


*Extract bias currents
.extract dc label=id_m1a id(xamp.xtp0.m0)
.extract dc label=id_m1b id(xamp.xtp3.m0)
.extract dc label=id_m2a id(xamp.xtn0.m0)
.extract dc label=id_m2b id(xamp.xtn4.m0)
.extract dc label=id_mbp1 id(xamp.xtp2.m0)
.extract dc label=id_mbp1 id(xamp.xtp2.m0)
.extract dc label=id_mbp2a id(xamp.xtp1.m0)
.extract dc label=id_mbp2b id(xamp.xtp4.m0)
.extract dc label=id_mbn1 id(xamp.xtn2.m0)
.extract dc label=id_mbn2a id(xamp.xtn1.m0)
.extract dc label=id_mbn2b id(xamp.xtn3.m0)

.extract dc label=gds_m1 gds(xamp.xtp0.m0)
.extract dc label=gds_m1b gds(xamp.xtp3.m0)
.extract dc label=gds_m2 gds(xamp.xtn0.m0)
.extract dc label=gds_m2b gds(xamp.xtn4.m0)
.extract dc label=gds_mbp1 gds(xamp.xtp2.m0)
.extract dc label=gds_mbp2 gds(xamp.xtp1.m0)
.extract dc label=gds_mbn1 gds(xamp.xtn2.m0)
.extract dc label=gds_mbn2 gds(xamp.xtn1.m0)
.extract dc label=gds_mbn2 gds(xamp.xtn3.m0)
.extract dc label=gds_mbp2 gds(xamp.xtp4.m0)

*Transistor transconductance, the transistors in 180nm are subcircuits
.plot dc gm(xamp.xtn0.m0)
.plot dc gm(xamp.xtp0.m0)
.plot dc gm(xamp.xtn1.m0)
.plot dc gm(xamp.xtp1.m0)

*Transistor output conductance, the transistors in 180nm are subcircuits
.plot dc gds(xamp.xtn0.m0)
.plot dc gds(xamp.xtp0.m0)
.plot dc gds(xamp.xtn1.m0)
.plot dc gds(xamp.xtp1.m0)

*Drain source saturation voltage, this is roughly equal to our VEFF
.plot dc vdss(xamp.xtn0.m0)
.plot dc vdss(xamp.xtp0.m0)
.plot dc vdss(xamp.xtn1.m0)
.plot dc vdss(xamp.xtp1.m0)
.plot dc vdss(xamp.xtp2.m0)
.plot dc vdss(xamp.xtn2.m0)
.plot dc vdss(xamp.xtp3.m0)
.plot dc vdss(xamp.xtn3.m0)
.plot dc vdss(xamp.xtp4.m0)
.plot dc vdss(xamp.xtn3.m0)
```

```
*Calculate & plot gm over id
.defwave gm_id_m2 = abs(gm(xamp.xtn0.m0)/id(xamp.xtn0.m0))
.plot dc w(gm_id_m2)
.defwave gm_id_m1 = abs(gm(xamp.xtp0.m0)/id(xamp.xtp0.m0))
.plot dc w(gm_id_m1)
.defwave gm_id_mbn = abs(gm(xamp.xtn1.m0)/id(xamp.xtn1.m0))
.plot dc w(gm_id_mbn)
.defwave gm_id_mbp = abs(gm(xamp.xtp1.m0)/id(xamp.xtp1.m0))
.plot dc w(gm_id_mbp)

*Calculate output voltage
.defwave vut = 'v(vop) - v(von)'
.plot tran w(vut)
.defwave vcm = '1/2*(v(vop) + v(von))'
.plot tran w(vcm)
.defwave vin = v(vi)
.plot tran w(vi)
.defwave avd= 'vut/vin'
.plot tran w(avd)

*.dc parameter ibias2 6.3u 7.7u .1u
.op

*get the data, and store it in txt file
.extract label=finaloutput file=vga_fft.txt VECT
yval(w(vut),xdown(v(clk),1.7999,1))

*Do a transient analysis
*.tran 1n 5u
.tran 1n 168.84u

.dc
.extract dc
.probe v

.end
```