Norwegian University of
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Fabrication and Characterization of Single Doped GaAs Nanowire Devices

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Problem Description

The student will in this project learn the complete process for development of nanowire devices, from fabrication to the final optoelectric characterization. In collaboration with PostDoc Dong Chul Kim, he/she will produce nanowire components by the use of electron beam lithography and other cleanroom methods in the NTNU NanoLab. For characterization, up to date measurement setups in the nanophotonics lab at the Institute for Electronics and Telecommunications (IET) will be used to study the physical properties of the NW components, from room temperature all the way down to liquid helium temperature (4 K).

In this project, primarily doped GaAs nanowires will be studied. The understanding of doping of individual nanowires is still at an early stage, but is vital for future applications.

Assignment given: 17th of February, 2011

Supervisor: Prof. Helge Weman, IET

Abstract

In the work with this master thesis, electron beam lithography (EBL) and other clean room methods was used to develop a reproducible process for making ohmic contacts to nanowires (NWs), with the aim of investigating different dopants' influence on their physical properties. After optimizing the EBL process, good alignment of the contact patterns to the NWs was achieved by doing a thorough alignment procedure. A detailed write field alignment close to the sample position prior to the 3-point alignment, along with consistent use of alignment positions, was found the be especially important to reduce misalignment.

For surface treatment it is shown how a diluted HCl solution is used to remove native oxide on the NW surface, and how a solution of citric acid and hydrogen peroxide can be used to effectively etch the AlGaAs shell of core-shell nanowires, though selective etching of AlGaAs on GaAs is difficult. Further, an ammonium sulphide solution is used to passivate the surface prior to metal deposition.

Metalization was done using an electron beam evaporator, however optimal thin films could not be achieved due to the presence of strain. This is believed to originate in the evaporation of electron beam resist (ER) during metal deposition due to high local heating of the samples. While this was remedied by, among other, depositing thinner films at high deposition rates, it could not be fully avoided. Nevertheless, satisfactory lift-off was still achieved in most cases.

IV characterization of the different samples was done using a probing station. The samples generally display asymmetric and non-linear characteristics, indicating that ohmic contacts have not been achieved. Annealing tests was also done on a number of samples, and while this generally resulted in more linear IV curves, the current was also reduced in most cases.

Preface

The aim of the nanowire group at the Department of Electronics and Telecommunications here at the Norwegian University of Science and Technology (NTNU), is to make core/shell nanowire junctions for use as photovoltaic elements in next generation solar cells. It is as part of this group, lead by Professor Helge Weman, that I have done my master thesis, Fabrication and Characterization of Single Doped GaAs Nanowire Devices, during the spring of 2011.

The nanowire group is a collection of people with incredible experience and knowledge within their fields, and it has been a privilege to work and learn alongside them all. Through the course of the work with this thesis I have obtained valuable insight into scientific research on, and characterization of, nw components, as well as extensive training in clean room methods and equipment. This would not have been possible without the help and support of many, but I would like to thank a few specifically.

First I would like to thank my supervisor, Dr. Dong Chul Kim for his guidance, all the long discussions, his valuable feedback during the writing of this thesis, as well as the countless hours he has devoted to helping me in the lab. After which he has spent countless more to finish off his own work. His work ethics are truly beyond anything else I have ever encountered, and is an example for all of us to follow.

I would also like to thank my head supervisor Professor Helge Weman for allowing me to be part of this project, and for all his assistance, and help with revising this thesis.

Last but not least, I would like to thank Espen Rogstad and the rest of the NTNU NanoLab staff for all the work they have put down to help out on numerous occasions.

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List of Abbreviations

SC	Semiconductor
NW	Nano wire
EBL	Electron Beam Lithography
SEM	Scanning Electron Microscopy
IPA	Isopropyl alcohol
VLS	Vapor-Liquid-Solid (growth mechanism)
VS	Vapor-Solid (growth mechanism)
ML	Monolayer
DI	De-ionized
RHEED	Reflection High Energy Electron Diffraction
UHV	Ultra-high vacuum
PMMA	Polymethyl methacrylate
EL	Ethyl lactate

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Chapter 1

Introduction

In a society driven by the urge to go smaller and faster, and with device sizes approaching the limit of traditional lithography techniques, semiconducting nanowires (SC NWs) have emerged as promising building blocks for nanoscale device applications. NW based devices such as light emitting diodes (LEDs) [1, 2], transistors [3, 4], biological sensors [5, 6], photo detectors [7, 8] and solar cells [9, 10, 11] have been demonstrated, in which understanding of, and ability to control the properties of the NWs are crucial.

For photovoltaic applications III-V semiconductors are preferred over traditional semiconductors such as silicon, due to their direct bandgap nature. In photovoltaic devices conversion of sunlight into electrical current happens by excitation of an electron from the valence band to the conduction band by absorption of a photon (given that the photon energy is higher than the bandgap of the sc). This process is more efficient in the case of direct bandgap materials since it does not include change in the electron momentum, thereby avoiding loss of energy to phonons in the material. In addition, the III-V materials show high mobility of carriers, making them useful for high-speed electronic devices.

The small size of the NWs allows for growth of heterostructures with materials of large lattice mismatch, due to the possibility of relaxing in the radial direction without forming misfit dislocations. Heterostructures can be grown in the axial direction, radial direction or both, opening up for a myriad of new devices. NW growth as a buttom-up approach to device fabrication is most commonly done by catalyst driven Vapor-Liquid-Solid growth (VLS), producing one-dimensional crystalline structures with diameters in the range of a few 10s of nanometers and lengths up to a few micrometers.

An important way of changing the NW properties is doping. This can be done either during VLS growth, which is the case for the samples used on this work, or after growth using diffusion or ion implantation. In this work, both core and core-shell GaAs NWs (shell of AlGaAs) with different dopants will be investigated, and a method for contacting and characterizing single NWs will be established by the use

of an electron beam lithography (EBL) process. Methods for passivation of the NW surface, as well as etching of the AlGaAs shell to provide good contact between the NWs and the deposited metal contacts will be investigated. Finally, the IV characteristics of the contacted NWs will be measured, both before and after annealing, with the aim of verifying that ohmic contacts to the wires have been achieved. This will enable us to effectively measure the effect of dopants, which is important for future use of GaAs NWs as photovoltaic components.

Chapter 2

Theory

2.1 Nanowire synthesis

2.1.1 Vapor-Liquid-Solid growth mechanism (VLS)

Fabrication of NWs by the bottom-up approach was first demonstrated by Wagner and Ellis in 1964, and the process was named VLS growth [12]. This technique uses a metal particle as a catalyst, which forms a liquid-alloy particle on reacting with source material supplied in vapor form, at substrate temperatures above the Au eutectic temperature. On supplying the source material continuously to this liquid-alloy, it will become supersaturated, and NWs will grow by precipitation at the bottom interface of the droplet.

Both the diameter and the position of the NWs are governed by the metal catalyst (typically gold (Au)), which can be deposited either as a thin film or as nanoparticles. In the first case particles are formed upon heating the substrate. For both cases these particles are randomly distributed, resulting in random positioning of the NWs. However, recent research has demonstrated the possibility of making arrays of Au droplets, and hence NWs, by techniques such as e-beam lithography [14], nanoimprint lithography [15] and laser-interference lithography [16]. It has been shown that the diameter of the NWs are given by the size of the catalyst particle through a linear relation close to 1:1 [13].

The VLS method is now commonly used for growing III-V SC NWs, and the different stages involved in growing GaAs NWs by MBE, which is the case for the NWs used in this work, are shown in figure 2.1.

Here, the Au particles/thin film is first deposited on the GaAs(111)B substrate and heated to react with the Ga from the substrate surface, thereby forming a liquid Au-Ga alloy. On supplying Ga continuously the Ga adatoms can either hit the Au droplet directly, or first hit the substrate surface followed by diffusion along the NW sidewall to the Au droplet. Once the Au droplet is supersaturated, the excess Ga precipitates at the Au-NW interface and forms the GaAs NW by reacting with As, also

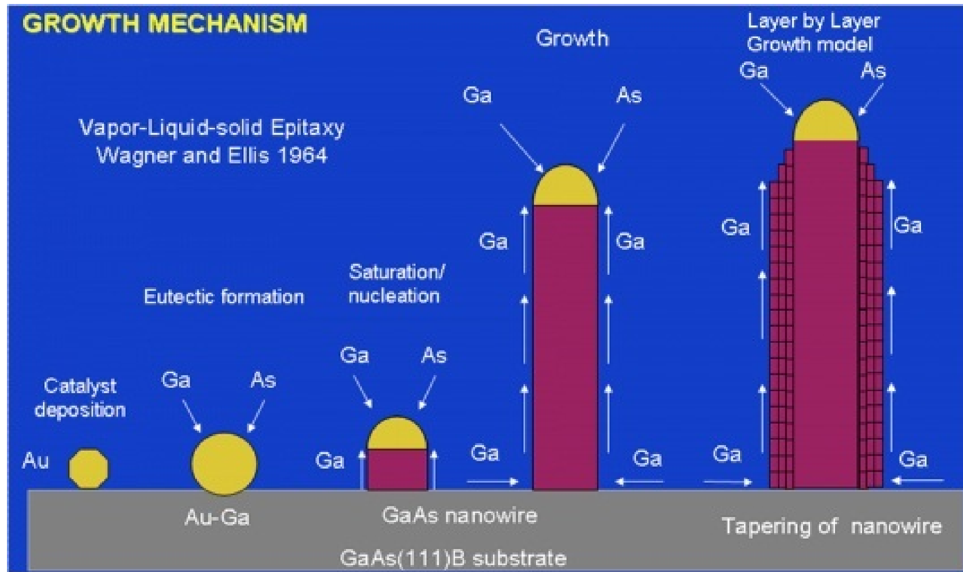

Figure 2.1: Figure showing the different stages of VLS growth of a GaAs NW.

supplied in the chamber. As it is energetically preferable for the Ga and As adatoms to diffuse to the existing Au-NW interface over forming secondary nucleations, this leads to axial NW growth.

As the NW continues to grow, tapering is often observed. This is attributed to two effects. The first one is based on diameter reduction of the seed particle. When the length of the NW exceed the diffusion length of Ga, adatom influx to the seed particle is reduced. This results in a change in the composition of the seed particle, leading to a slight reduction in droplet diameter and hence also NW diameter. The second one is based on the initiation of radial growth. Eventually the Ga adatoms will not be able to diffuse all the way to the seed particle, thus leading to radial growth of the NW by a Vapor-Solid growth mechanism.

2.1.2 Vapor-Solid growth mechanism (VS)

The VS growth mechanism differentiates itself from VLS growth by that there is no liquid element present in the process as catalyst for nucleation. In VS growth atoms nucleate at the substrate surface, or along the sidewalls of previously grown NWs, as discussed in the previous section. VS growth is well studied as part of thin film growth of SC materials.

2.2 Molecular Beam Epitaxy (MBE)

MBE is one of the most versatile and commonly used techniques for growing thin epitaxial films. The deposition of material on the substrate is done by evaporation of materials in a chamber maintained under ultrahigh vacuum (UHV, 10^{-10}-10^{-11} Torr,

obtained by cooling the cryopanels with liquid nitrogen). For example, in the growth of AlGaAs layers on GaAs substrates, the Al, Ga and As components, along with dopans, are heated in separate cylindrical cells, called effusion cells (figure 2.2). Due to the high vacuum in the chamber, the mean free path of the evaporated elements will be very high, which leads to no collisions until they reach the sample surface. The deposition rates of these materials can be very closely controlled, down to as low as 0.1 monolayer (ML) per second, by changing the temperature of the effusion cells, and controlling a shutter in front of each cell. This results in very high quality crystals, and allows for growth of heterostructures with abrupt interfaces.

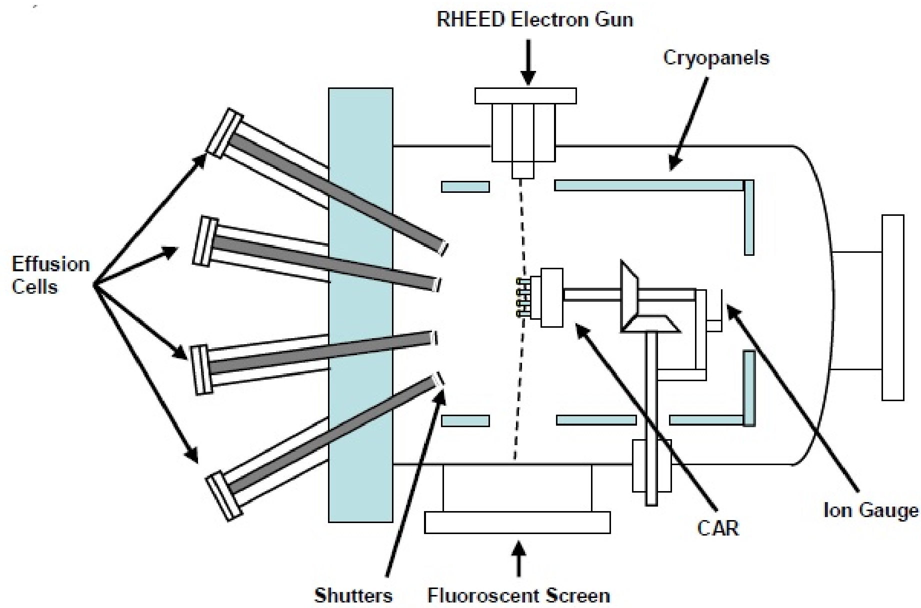

Figure 2.2: Schematic of the MBE chamber.

Another benefit of the UHV is that it allows for use of in-situ characterization techniques (characterization done during growth) such as reflection high energy electron diffraction (RHEED). As seen in figure 2.2, the RHEED system requires an electron source (gun), a photoluminescent detector screen and a clean surface. The electron gun generates a beam of electrons which strikes the sample at a very small angle relative to the sample surface. Incident electrons diffract from atoms at the surface of the sample, and a small fraction of the diffracted electrons interfere constructively at specific angles and form regular patterns on the detector. The electrons interfere according to the position of atoms on the sample surface, so the diffraction pattern at the detector is a function of the sample surface. Figure 2.3 illustrates typical REED oscillation, where each top corresponds to the completeon of a single ML.

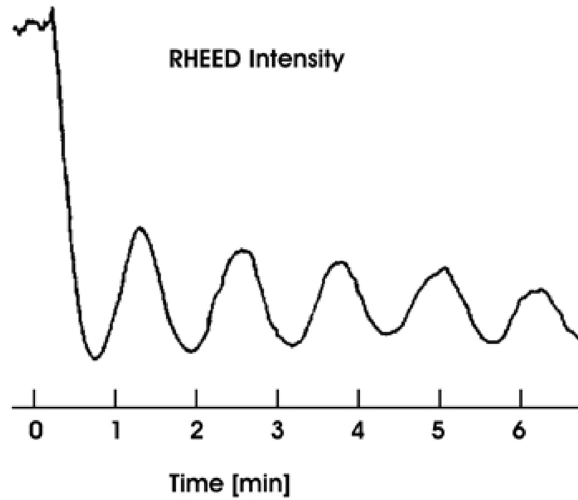

Figure 2.3: RHEED oscillation diagram.

2.3 Scanning Eleectron Microscope

The SEM is a sophisticated microscope that functions by creating a highly focused beam of electrons that scans an object while detectors measure the resulting scattered electrons. It is a non-destructive and non-contact metrology tool. The SEM has an electron gun, focusing elements for shaping the electrons into a beam, and a final electrostatic-magnetic focusing system that makes the electrons strike the sample within a small, 2 to 6 nm spot (see figure 2.4). Since electrons have a very short wavelength, atomic-scale objects can be viewed with SEM imaging.

The electron gun produces a beam of electrons in a vacuum chamber of about 10^{-6} torr. It is desirable to have a high current of stable electrons with narrow energy spread. Near the wafer the electrons are focused into a narrow beam with a cylindrical magnetic objective lens often combined with electrostatic focusing elements to create a high-energy beam. The beam undergoes x-y deflection with an electrostatic deflector to raster-scan the wafer.

When the incident beam strikes the surface, secondary and backscattered electrons, along with X-rays and photons, are emitted or transmitted due to interaction between the beam and the sample surface. A detector is then used to collect the secondary electrons and create an electronic image that represents the sample surface. Backscattered electrons are also collected and offer superior compositional contrast between different materials.

The energy of the electron beam is directly related to the image needed. Low acceleration voltages are used to image structures on or close to the surface of the samples, while high acceleration voltages (typically 100 - 200 keV) is used to image underlying or deep structures. The limitations of the SEM are that it requires a high

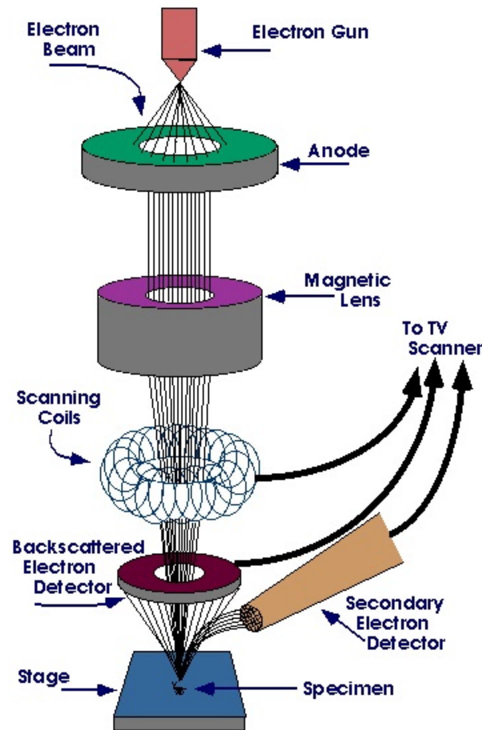

Figure 2.4: Schematic of SEM.

vacuum, and that it is necessary to coat insulating samples with a conductive film (typically Au) prior to imaging.

In this work an acceleration voltage of 5 keV was used when determining the nw positions on the sample. Beam interaction was thus limited to regions very close to the sample, giving highly detailed surface images ideal for inspection of the fine structures of the nws.

2.4 Electron Beam Lithography

Electron Beam Lithography (EBL) is a lithographic method to achieve sub 100 nm resolution. In this method electrons are formed to a beam and accelerated to a determined position on the wafer surface, where the resist is exposed to form a pattern. An EBL system consists of the electron source or electron gun, the electron-optical system (the electron column), a mechanical wafer stage, a SEM and a controller system [19, p. 235]

The time needed for exposure of the sample depends on the pattern, but because it is a serial method, it is time-consuming and not suitable for industrial mass production. Nevertheless, because of the high resolution, and not being dependent on masks, it is a valuable tool for research and development.

In the EBL two different coordinate systems are used to obtain proper pattern alignment [20, p. 147]. The first one is fixed, and is defined by the directions of the stage movement, and is labeled (x,y,z). The second one, labeled (u,v,w), is related to the sample and have to be defined every time (see figure 2.5).

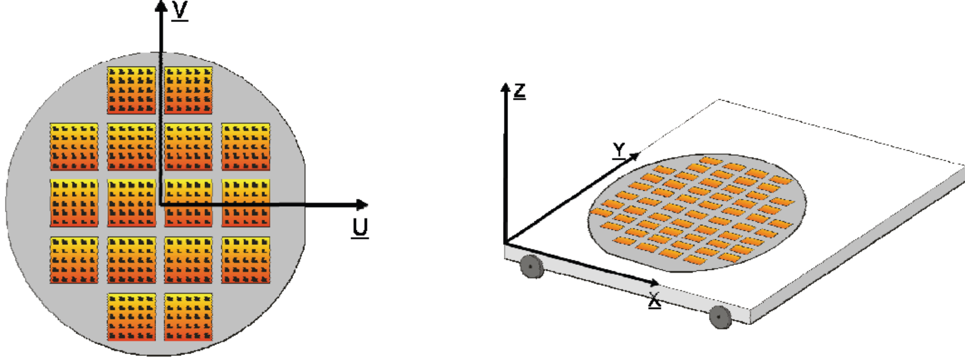

Figure 2.5: Definition of coordinate systems in the EBL

These two coordinate systems are generally not identical, as they may have different origin causing an offset vector, be rotated in relation to each other or have different scales. To be able to drive to a specific location on the sample a coordinate transformation therefore needs to be calculated. This is done by a procedure called *3-point alignment*.

Another important step of the alignment procedure is *Write Field Alignment*. This procedure adjusts the electron beam deflection system according to the sample specific (u,v,w) system in three ways: by scaling the beam's major axis to the u- and v axis achieving proper dimensions; by adjusting the offset of the beam center with respect to a point in u,v, enabling overlay exposure; and by adjusting the rotation of the beam major axis, enabling correct movement of the beam relative to the sample coordinate system.

2.5 Fabrication of Ohmic Contacts

When contacting the NWs it is important that ohmic contacts are achieved, meaning that the contacts have a linear IV characteristic in both biasing directions, minimal resistance and no tendency to rectify signals. Ideal metal-semiconductor contacts are ohmic when the charge induced in the SC in aligning the Fermi levels is provided by majority carriers. For example, in the p-type case where $\Phi_m > \Phi_s$, the Fermi levels are aligned at equilibrium by transferring holes from the SC to the metal. This lowers the electrostatic contact potential, and the barrier for hole flow between the metal and the SC is small and easily overcome by a small voltage.

A number of effects can complicate the forming of ohmic contacts. A metal-semiconductor junction includes a termination of the SC crystal, and the SC surface contains *surface states* due to incomplete covalent bonds and other effects, which can lead to charges in the metal-semiconductor interface. Surface states can be visualized as a material with the same band diagram as the bulk, but with several additional states inside the band gap, as shown in figure 2.6 (b) [26]. These surface states cause the Fermi energy to be pinned. Electrons from the valence band fall into the surface states until the Fermi energy coincides with the level of which the surface states are filled, hence deteriorating the the optical properties of the NWs.

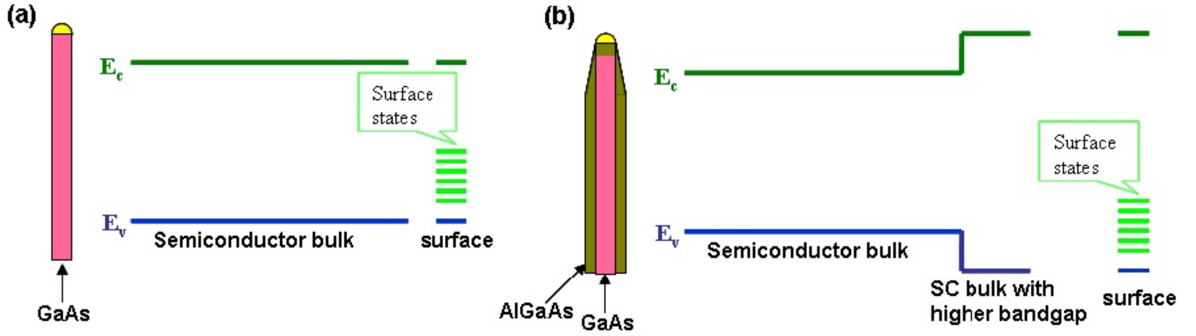

Figure 2.6: Illustration of surface states in a GaAs NW, without (a), and with (b) an AlGaAs shell.

Furthermore, the contact is seldom an atomically sharp discontinuity between the SC crystal and the metal. There is typically a thin interfacial layer which is neither semiconductor nor metal. For example, GaAs is covered by an oxide layer under atmospheric conditions, which leads to the forming of such an interfacial layer upon depositing metal. Although electrons can tunnel through this thin layer, it does affect the current transport through the junction.

Because of surface states, interfacial layer and other effects, it is difficult to fabricate junctions with barriers near the ideal values predicted from the workfunctions of the isolated materials. In compound SCs the interfacial layer introduces states in the SC band gap that pin the Fermi level at a fixed location, regardless of the metal used, causing the barrier height to be determined by this pinning effect rather than the workfunction of the metal [25, p. 231-234]. To counter these effects, surface treatment of the NWs to remove native oxide and passivation becomes important.

2.6 Surface treatment and passivation

During processing the samples are constantly being exposed to different impurities, both from organic vapors in the air as well as contaminants from the different pro-

cessing steps, such as resists and developers. The most common method for removing contaminants such as these is rinsing with acetone, methanol, isopropylalcohol (IPA), or a combination of these. Another method is oxygen plasma ashing, where the sample is exposed to an oxygen plasma, which combines with the organic materials to form ash, and is removed by a vacuum pump. In this process the energy of the plasma is low, as to not damage the SC.

2.6.1 Removal of the native oxide

When GaAs comes in contact with air a layer of oxide is produced. This native layer is typically on the order of 1-2 nm after prolonged exposure to air and severely decreases the contact conductance if it is not removed prior to metalization. Diluted acidic solutions such as HCl (1) : H_2O (1) can be used to remove this layer, with minimal etching of the NWs.

2.6.2 Passivation

Ammonium polysulfide, NH_4S_x, solutions have been found to remove native oxides and contaminants from III-V semiconductor surfaces, and to provide passivation with covalently bonded sulfur atoms. The passivation provides good short-term surface stability without considerable reoxidation in air and aqueous solutions [17, 18]. It also provides both chemical and electrical passivation of a surface. Surface passivation becomes increasingly important as the surface-to-volume ratio of the structure increases. The key difference in chalcogenide passivation technology for nanostructures, compared to bulk materials, is the importance of etching rates. In bulk, a certain amount of surface material can be sacrificed without the loss of device functionality. However, nanowires are extremely sensitive to removal of surface material due to their large surface-to-volume ratio.

While chalcogenide passivation has been shown to increase the quality of metal contacts, perhaps the most effective way of suppressing the surface states in SCs is an in-situ process. As discussed in chapter 2.1 radial growth can be achieved in the EBL. By depositing a shell with higher bandgap that provides type I band alignment with the core material (typically AlGaAs for GaAs NWs), an energy barrier is created, ensuring that both electrons and holes are confined in the core, see figure 2.6 b).

2.6.3 Ethching of the AlGaAs shell

In the case of AlGaAs shells being used as passivation layers, as well as for more complex core-shell structures, it is necessary to remove the high bandgap AlGaAs shell at the NW-metal interface to give good contact characteristics. However, etching $Al_xGa_{1-x}As$ on top of GaAs with x<0.4 with a high selectivity is difficult. Methods do exist, but these require a much higher Al content (>70%).

An alternative for etching of the shell is a solution of citric acid ($C_6H_8O_7$) and hydrogen peroxide (H_2O_2), which gives smooth surfaces in addition to being gentle on the resist.

2.7 Electron Beam Physical Vapor Deposition

EBPVD is a form of physical vapor deposition where the process of evaporation consists of placing the material to be deposited in a crucible and heating it inside a vacuum chamber until it vaporizes. In this system, as illustrated in figure 2.7, an electron beam is magnetically deflected 270° and is centered on the target material. In this way a melt of the source material is produced on a block of the same material, which can be held in a water-cooled cold crucible in order to avoid contamination of the melt. By maintaining a high vacuum in the process chamber, the mean free path of the vapor atoms is increased, and the vapor travels in a straight line in the chamber until it strikes a surface and condenses to form a film [21, p. 313].

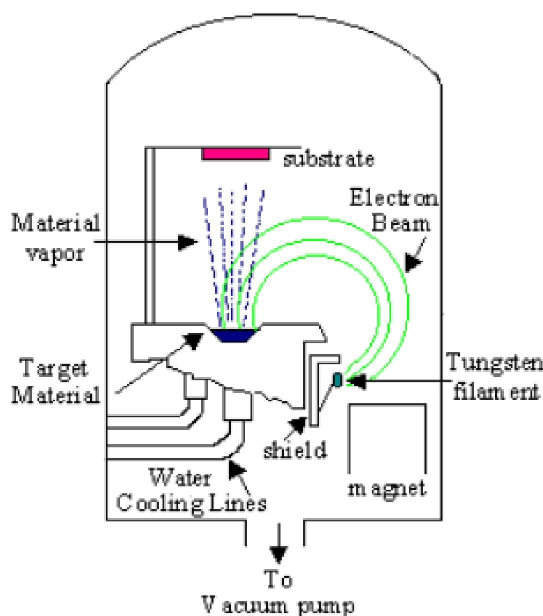

Figure 2.7: Schematic of the e-beam evaporator

The advantage of EBPVD is that it can be used to deposit both thick and thin films of a wide variety of metals, with good control of deposition rates. Its greatest drawback though is the inability to produce uniform step coverage. This can to some extent be improved by heating and rotation of the wafers, but it is still not capable of filling higher aspect ratio holes.

Chapter 3

Experimental

3.1 Sample preparation

The nanowires used during the course of this master assignment were supplied by Dr. Derashj Dasa, and were grown at the Department of Electronics and Telecommunication (IET) at NTNU. A number of different types were used, as summarized in table 3.1 below. All of these nanowires were grown with relatively few stacking faults using MBE, with lengths ranging from 1 to 8 μm and expected doping concentration $\approx 10^{18}$.

Table 3.1: Nanowire summary

Sample number	Structure
As 518-2	Be doped (p-type) GaAs core
As 518-3	Si doped (*) GaAs core
As 518-4	Te doped (n-type) GaAs core
As 539-8	Be doped (p-type) GaAs core, intrinsic AlGaAs shell
As 539-6	Si doped (*) GaAs core, intrinsic AlGaAs shell
As 580-2	Si doped (*) GaAs core, Si doped (n-type) AlGaAs shell
As 580-3	Te doped (n-type) GaAs core, Te doped (n-type) AlGaAs shell
As 562-3	Te doped (n-type) GaAs core, intrinsic AlGaAs passivation layer, Be doped (p-type) AlGaAs shell

* the exact doping type is currently unknown, as Si doping in GaAs is amphoteric and can hence be both (see chapter 4.5).

These substrates containing as-grown nanowires were then immersed in isopropyl alcohol (IPA) and sonicated for approximately 30 s, to break the NWs off of the substrate. The NWs could then be transfered to prefabricated sample holders (the process of making these are covered in detail in appendix A), by placing a droplet of the solution on the holders and leaving it to dry off. Once all the IPA was evaporated, the samples were cleaned using IPA and de-ionized water (DI water) and blown dry using a nitrogen gun. The samples were then inspected with an optical microscope

to verify that a sufficient number of promising NWs were present. And if not enough NWs were present, the process was repeated. To produce trustworthy results, consisted IV characteristics for at least 4 wires is necessary, so in most cases 7-10 wires were aimed for.

Once a sufficient number of wires were obtained, the samples were introduced into the MBE, where its scanning electron microscope (SEM) was used to take high resolution pictures of the most suited positions. For this, an acceleration voltage of 5 kV was used to minimize the impact on the nanowires caused by the electron beam. Depending on how many usable wires each position had, one or two were chosen for patterning.

3.2 The EBL process

3.2.1 Contact design

Once the high resolution pictures had been taken, the exact position of the nanowires could be determined. This was done using a program called *Engauge Digitizer*. By importing the pictures into the program, a 3-point coordinate system could be defined using easily distinguishable features at each position.

For the 50 μm wf positions the corners of the rough metal contacts were used, but the exact positions could vary from sample to sample depending on the position of the nanowires that was to be contacted. The reason for this was that these 3 points would be exposed to the electron beam during the alignment stage of the EBL process (as will be discussed in detail in chapter 4.2), and they were hence chosen as far away from the nanowires as possible to avoid any unwanted exposure. For the 100 μm wf positions, defining the coordinate system was straight forward, as alignment marks had been included in the design. These were located outside the actual wf ensuring that the same 3 points could be used every time (see figure A.4 in appendix A). Once the coordinate system was correctly defined, the most suitable nanowires (i.e. single, and with little to no particles attached to them) could be defined using the *Curve Point* tool, and all points listed with the *Measure Geometry Info* tool. Figure 3.1 shows how this would typically look for the two different write fields.

Once the position of the different nanowires had been defined, they could be inputted into *CleWin 4.0*, the program used to design the actual contacts. This was done by using the *Insert Wire* tool, and inputting each separate wire coordinate, into a pre-designed stencil, resembling the ends of the rough contacts of any given position (shown in black in figure 3.2). The contacts to each wire could then be designed using the *Insert Polygons* tool, resulting in circuits typically resembling figure 3.2 below.

The big parts of these contacts could be designed arbitrarily as one saw fit, but the

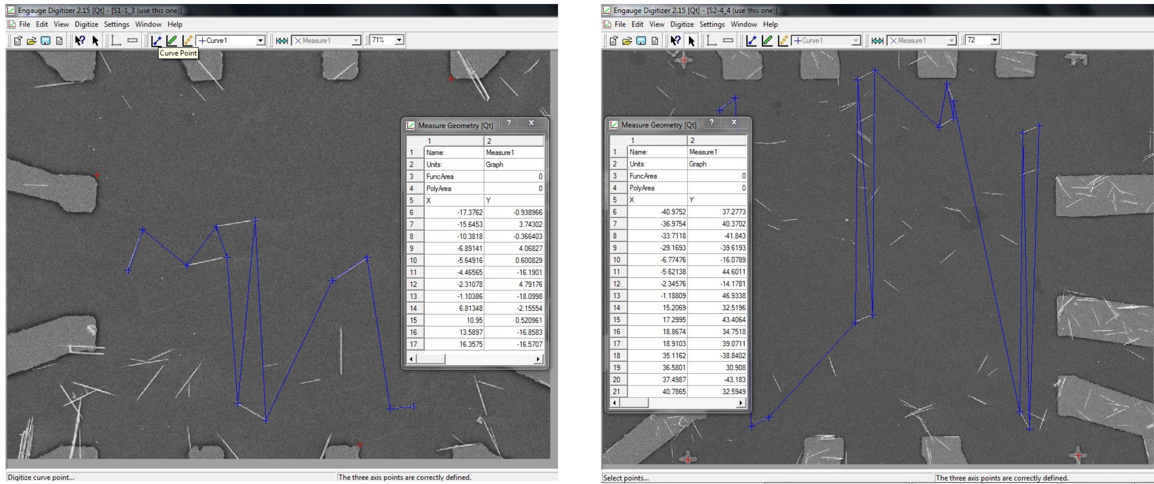

Figure 3.1: Defining the NW coordinates at a 50 μm (left) and a 100 μm (right) wf position.

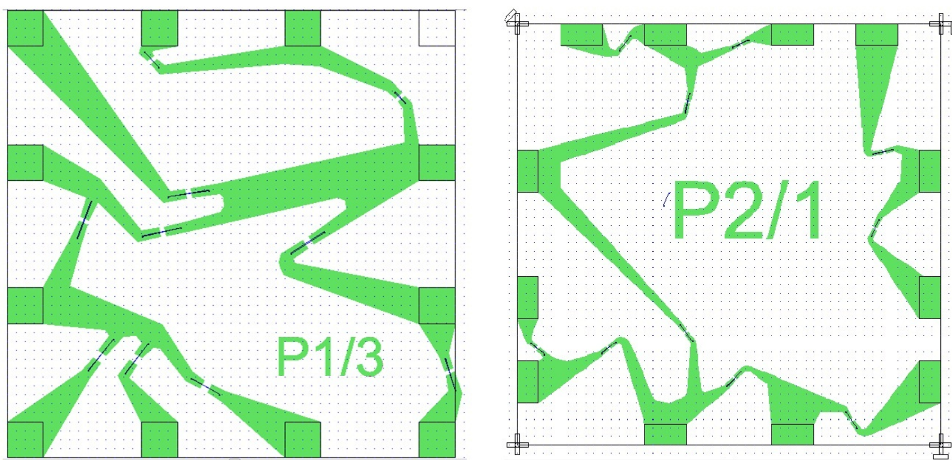

Figure 3.2: Contact design using CleWin, 50 and 100 μm wf

point where the contacts overlapped the nanowires were subject to somewhat more stringent requirements. For these, a minimum width of 1 μm was used to account for slight misalignment during the EBL process, and a minimum gap length of 400 nm to avoid shorting the contacts due to possible overexposure (see figure 3.3). For the longer wires this gap could be increased, however, a big overlap of the wires was usually preferred to minimize contact resistivity; especially for the core/shell wires, to ensure good contact to the core after etching, as one can never know exactly where the core ends (as discussed in chapter 4.3). Finally, the designs were saved in *.gds* format, for use in the EBL software.

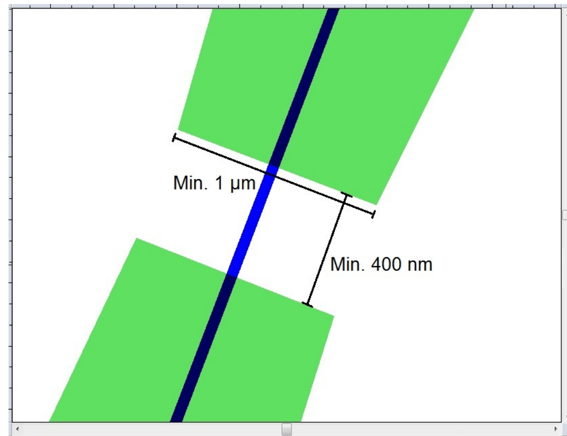

Figure 3.3: Contact requirements

3.2.2 Spin coating

Before the actual exposure could be done, the samples were coated with photoresist. Different types and mixtures of polymethyl methacrylate (PMMA) and Ethyl Lactate (EL) were used, depending on what thickness of the film was needed. Both of these resists are positive and well suited for deep UV EBL, however PMMA 6.5 was most commonly used in this thesis, yelding a thickness of about 400 nm as indicated by the spinspeed curves shown in figure 3.4. Here the number 6.5 denotes a mixture of two stock PMMAs made by Don Chul Kim, tailored to this specific process. After spincoating, the samples were baked on a hotplate to remove any remnant water on the surface. See table 3.2 for details on the on the spincoating process.

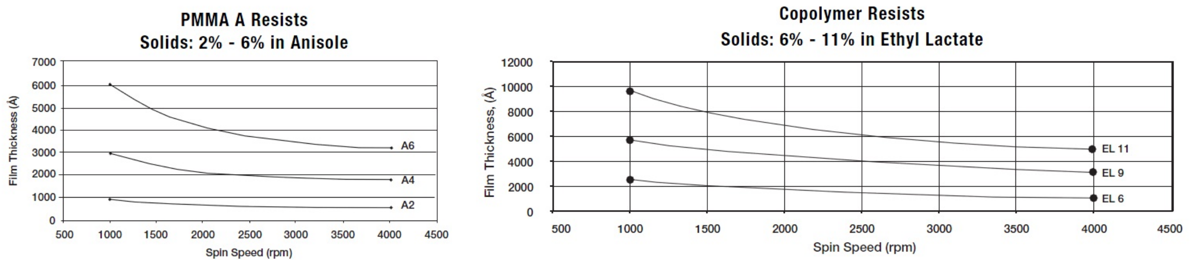

Figure 3.4: Spinspeed versus thickness of the ER

Table 3.2: Resist parameters

Resist	PMMA 6.5	PMMA 7.6	EL 11 + PMMA 6.5
Thickness	400	≈ 700	≈ 900
Spin speed (rpm)	4000		
Acceleration (rpm/s)	1000		
Time (s)	120		
Bake temp. (°C)	180		
Bake time (s)	120		

3.2.3 EBL procedure

EBL was done at the NTNU NanoLab, using a *Hitachi S-4300SE* SEM machine. The whole EBL procedure is quite complex and only an overview will be presented here, for more detailed descriptions please refer to [22] and [23].

The EBL process consists of a number of steps:

1. Focus and beam alignment
2. Current measurement
3. Rough angle correction at the sample corners
4. Fine angle correction
5. Writefield alignment
6. 3-point alignment
7. Redo writefield alignment
8. Parameter input and exposure

Once the samples were introduced into the EBL, the first step of the process was to secure a proper SEM image, and in that way ensuring a confined beam spot necessary for accurate exposure; as the beam alignment changes with changing acceleration voltage, it is important to do this at the acceleration voltage that is to be used for exposure, 20 kV. Focus and beam alignment can be done at an arbitrary position of the sample holder. In this case some fine features at the edge of the Faraday cup was used, due to the good contrast that could be achieved there, which in turn made focusing much easier. Once good focus at 80 k magnification had been achieved, aperture alignment and astigmatism correction could be done to secure a proper image.

Next, the current was measured, as this was needed in the last step of the process to calculate the dosage needed for exposure. This was done by moving the stage to the center of the Faraday cup and using maximum magnification to ensure that all the beam current was focused into the cup. A high sensitivity ampere meter from

EM System Support was then used to measure the current, with typical values in the range of 30-45 pA.

The stage was then moved to the sample, where the corners were used to do a rough angle correction, followed by a fine angle correction using the bottom corners of the two outermost contact pads (shown as black in figure A.2).

The next step was then to move the stage to the position index (seen in figure A.3 as a cross with two numbers indicating x and y direction), to verify that one was at the right position. A ruler tool in the EBL software was then used to measure the distance to the sample position in the design file, so that the stage could be moved to the correct position with the electron beam blocked, thereby reducing the risk of exposing sensitive areas of the sample. For the 50 μm wf positions this point was also used for write field alignment. For the 100 μm wf positions, one of the three points used for defining the coordinate system was chosen.

Once write field alignment had been done to a satisfactory degree, the stage was moved to the sample position and 3-point alignment was done, using the same 3 points that was used for defining the coordinate system when the contact patterns were designed.

Depending on how much the alignment was corrected during the fine 3-point alignment, the write field alignment would be changed to some degree as well. In most cases this would be negligible, but, to be on the safe side, a final write field alignment was done before doing the exposure.

The final step of the EBL process is to input the exposure parameters. Many parameters are calculated automatically by the software, but the measured current and the dose needs to be input manually. Here, the dose is calculated by using equation 3.1 below, where t is the desired development time, I is the current and A the area.

$$Dose = \frac{t * I}{A} \tag{3.1}$$

Exposure would usually take from 40 seconds to a couple of minutes, with the parameters summarized in table 3.3 below.

Table 3.3: Exposure parameters

Acceleration voltage	20 kV
Beam current	30-45 pA
Magnification	1000 (50 μm wf), 500 (100 μm wf)
Dose	125-600 μAs/cm^2

3.2.4 Pattern development

By using a positive PR the exposed parts of the film was now soluble, and the contact patters could be developed using a mixture of IPA and DI water (IPA (9): H_2O (1)). After 20 seconds the development was stopped by holding the samples under running water for approximately 30 seconds, and the pattern was inspected with an optical microscope to check the state of the pattern. The process was then repeated until proper development had been achieved, which typically took a total of approximately 35 seconds. As a last step of the development process, the samples were subjected to oxygen plasma ashing (12 s at 50% power and 30 % oxygen flow), to remove any remnant organic contaminants on the surface.

3.3 Etching and Passivation

To ensure a good contact between the wires and the metal, the samples were transfered to a fume hood, where surface treatment and, in the case of some of the core-shell samples, etching was done. As described below, this was a multi step process, with many different chemicals, hence the samples were cleaned thoroughly with DI water in between each step to stop any reactions, and to avoid contaminating the solutions.

1. HCl (1) : H_2O (1) for 8 s $\rightarrow$ DI water for 30 s
2. $C_6H_8O_7$ (50) : H_2O_2 (1) for 15-17 s $\rightarrow$ DI water for 30 s (only for core-shell NWs)
3. NH_4S_2 (1) : H_2O (9) for $\approx$ 2 min $\rightarrow$ DI water for 1 min $\rightarrow$ blow dry with N_2

The purpose of the first step was to remove any native oxide, formed at the surface of the wires due to exposure to air. For this solution, 37 % HCl was diluted with water to avoid too high etching rates of the wires and to minimize resist damage.

For shell etching, a freshly made (important as described in chapter 4.3), highly concentrated solution of citric acid and hydrogen peroxide was used, for selective etching of GaAs and AlGaAs.

The last step of the surface treatment was to create a passivation layer at the surface to reduce native oxide growth before metalization could be done. For this, an ammonium sulphide solution was used, but as the solution can also etch the wires, it was highly diluted to prevent overetching.

3.4 Thin film deposition

Metalization was done using a *Pfeiffer Classic 500* electron beam evaporator. By running it in manual mode (see figure 3.5 below), the position, size and shape of the beam spot as well as the current, could be changed to give accurate control of the deposition rates for the different metals, and deposition tests were regularly carried out to ensure consistent metalization of all samples. In addition, the stage was rotated to give a more uniform deposition across the whole sample.

Figure 3.5: E-beam run in manual mode

When running the e-beam in manual mode it is important to increase the current slowly to reduce the strain on the filament. For the same reason every increase of 30 mA is followed by a 1 minute pause to allow it to stabilize. Finally, once the target current is reached and metal is evaporating from the target, a 2 minute pause (denoted a pre deposition hold in automatic mode) is included before opening the shutter to secure a stable deposition rate. For more details on the e-beam procedure see [24].

Many different metalization schemes were tested, depending on the doping of the wires that was to be contacted, as summarized in table 3.4 below.

In addition, 3 samples (As 518-2) were finalized up to the surface treatment step so that metalization could be done at IBM in Zürich, Switzerland, to be used as reference and for comparison with the metalization done at NTNU NanoLab.

Table 3.4: Metalization schemes

p-type	n-type
Pd/Au	Ti/Au
Pd/Ti/Au	Pd/Ge/Au
Ti/Pd/Ti/Au	
Pd/Zn/Pd	
Ni/Au	
Pt/Ti/Pt/Au	

After metalization, lift-off was done by splashing the samples with acetone, followed by rinsing with IPA and DI water, and then blown dry using a nitrogen gun. In some cases however, acetone would not be enough to give proper lift-off. If so, the samples were immersed in PG remover and placed on a hotplate at 80 °Cfor approximately 10 minutes, which was very effective. Inspection was then carried out using an optical microscope to make sure that satisfactory lift-off had been achieved, followed by a detailed inspection of each contact using SEM.

3.5 IV measurements

The final step of the fabrication process was to measure the IV characteristics of the different NWs. For this a probing station from *Cascade Microtech* was used along with a parameter analyzer, *Ke,ithley 4200 Semiconductor Characterization System*, available at the department of Electronics and Telecommunication at NTNU. For measurements, one side of the NWs were grounded, while the other was subjected to a voltage sweep from -3 to 3 V. The resulting current was then plotted by the software.

3.6 Annealing tests

Following the IV measurements a few of the most promising samples were taken back into the lab where annealing tests were performed to check for any changes in the IV characteristics. Theoretically, annealing should change the characteristics as the different layers forms alloys at the interfaces, resulting in more ohmic behavior. This was done using a *JetFirst 200* rapid thermal annealer from *Jipelec*, available in the chemical area of the NTNU NanoLab. The recipe for the process had to be input into the software and included multiple steps of which the most important ones are summarized below.

1. Evacuate the chamber → 5 min
2. Fill with N_2 → 5 min

3. Ramp up to 400 °C→ 10 s
4. Anneal → 30s
5. Ramp down to room temp. → 10s

After opening the N_2 valve in step two, the nitrogen flow was kept constant through the remainder of the process to ensure a clean environment. When the process was complete the software plotted the temperature curves of set values and actual temperature, shown in figure 3.6 (where the set value is shown in white, actual temperature in red and lamp power in yellow). After annealing IV measurements were done once again so that the results could be compared.

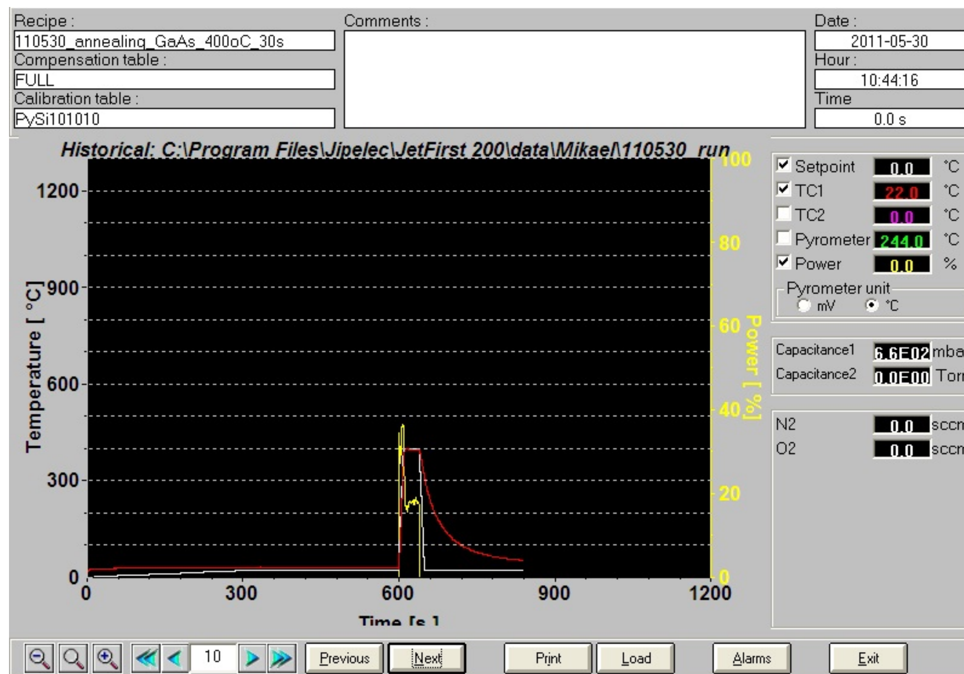

Figure 3.6: Time versus temp. graph of the annealing process

Chapter 4

Results and Discussion

4.1 Substrate fabrication

Fabricating our own substrates (as described in appendix A) eased the processing step in several ways. By including an index for each sample (see figure A.2) they could easily be distinguished from each other and orientation was trivial, as opposed to the old substrates where marks had to be made manually by breaking off parts of the sample edge.

Increasing the number of positions across the substrate surface gave a higher chance of dispersing the NWs at a sample position, thereby reducing the number of applications needed to achieve a sufficient number of NWs. Also, by increasing the number of contact pads from 8 til 12 (see figure C.5 and C.19), better yield from each position was achieved, to a point where designing contact patterns for a single position was enough to produce sufficient results. This proved to be much less time consuming than the case of having to make contacts for two different positions, which was usually the case for the old substrates.

4.2 The EBL process

Slight misalignment of the contact patterns is usually not a problem since they were designed to allow for some error (broad contacts and a large overlap of the wires). However, in the early stages of the project, alignment was very arbitrary and many of the samples had patterns that had missed the nanowires entirely, resulting in them having to be redone. Hence, a part of the work was devoted to optimizing the EBL procedure such that proper alignment of the contact patterns could be done consistently.

Initially the current was changed during the EBL process, using a low current for the alignment and then switching to a higher current for the exposure itself, with the purpose of minimizing the exposure of the e-beam resist. However, it quickly

became evident that this had a huge impact on both beam and WF alignment resulting in misalignment of the patterns. This was avoided by using the exposure current throughout the process, however, misalignment still occurred on many occasions.

Proper alignment was finally achieved by optimizing the write field alignment and 3-point alignment. To minimize any error introduced by moving the stage, the WF alignment was done as close to the sample position as possible without risking exposure of any sensitive parts of the sample (the position index for the 50 WF positions, and the coordinate system origins for the 100 WF positions, as described in chapter 3.2.3). The SEM was used at high magnification to place the stage at some easily recognizable feature, and the WF alignment procedure was done repeatedly with decreasing scan size until close to unity accuracy had been achieved.

By doing this the shift values (difference between the stage X/Y coordinate system, and the user defined U/V coordinate system) of the WF was drastically reduced, giving a smaller error in position. This meant that the target point used for 3-point alignment was within close proximity after moving the stage according to the design, such that the 3-point alignment could be done easily and with minimum effect on the WF alignment. This also meant that the scan size of the 3-point alignment could be reduced, exposing a smaller area of the sample and thereby minimizing the risk of exposing any critical regions. Mistakes could still happen, as is the case in figure 4.1 below where two of the contacts are shorted, however that is one of the few exceptions. As seen in the same figure, by following the procedure described above, close to perfect alignment was achieved for all samples.

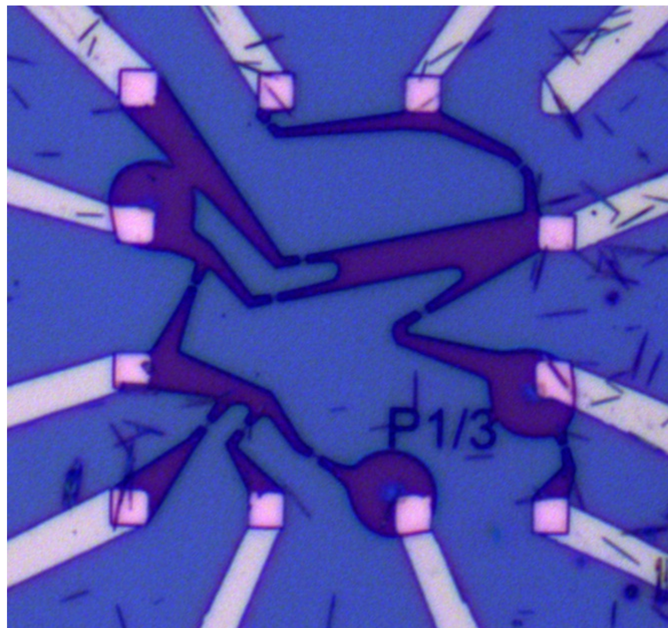

Figure 4.1: Example of proper alignment of the contact patterns

4.3 Etching and Passivation

For etching of the AlGaAs shell of the core-shell NWs it was discovered that a relatively freshly mixed solution should be used, as citric acid tends to loose its etching properties over time. The solution proved quite effective though, as illustrated in figure 4.2 below, and figure C.3 and C.7 in the appendix (similar results should have been observed for As 580-3 sample 4 (C.19), but they seem to not be etched at all).

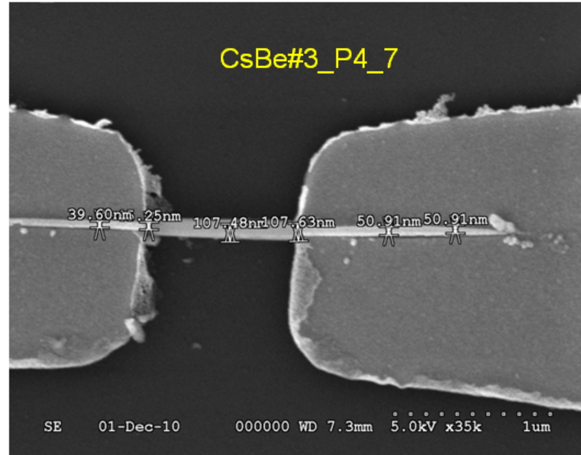

Figure 4.2: Etch profile of a CS Be doped NW

However, as discussed in the theory section (chapter 2.6.3) etching AlGaAs on top of GaAs with a high selectivity is difficult, resulting in many NWs being etched more on one side than the other. Since the exact endpoint of the core of the wires is unknown, one can not be certain that the shell has been fully removed on the top side of the NWs, and might be, at least part of, the cause of why diode-like IV characteristics are measured (will be discussed further in section 4.5).

When doing post lift-off examination of the samples sent to IBM, it was found that many of the wires seemed to have been etched severely (see figure 4.3). This had also been seen on a few occasions earlier, but was at the time attributed to the problems with the e-beam metalization as will be discussed later in this chapter.

Now, seeing that there is obviously nothing wrong with the metalization done at IBM (see figure 4.6), and knowing that no shell etching had been performed (samples in question are Be doped single core NWs), it seems that the problem is located in the passivation step of the surface treatment procedure. As discussed earlier, the NH_4S_2 solution can etch the sample if the concentration is too high, and further testing is needed to optimize the process to achieve a continuous passivation layer with minimum etching. In addition, as figure 4.4 shows, many of the wires seem to be etched more at the parts where they should be protected by the ER than at the contacts themselves. This effect is currently not fully understood and needs to be investigated

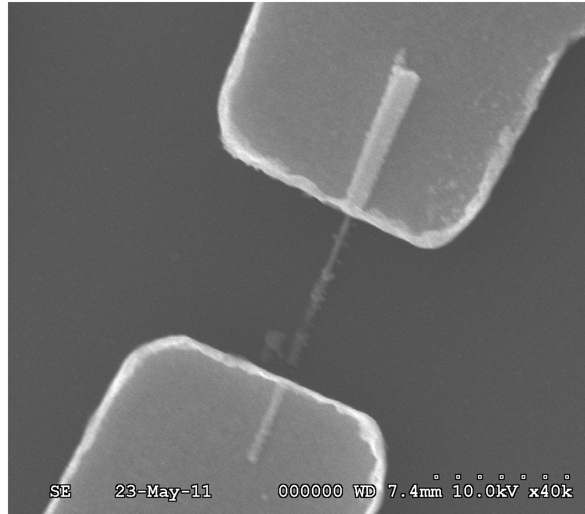

Figure 4.3: Loss of NW due to etching during passivation

further.

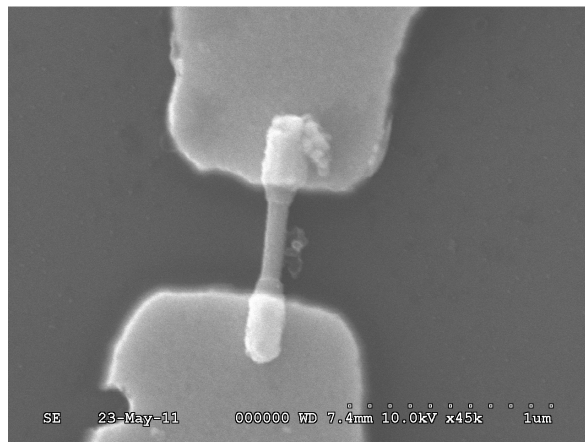

Figure 4.4: Etcing of the ER protected parts of the NWs

4.4 Thin film deposition

A major part of the work was dedicated to improving the metalization, as depositing homogeneous films was a problem throughout the entire work. When depositing metal with the e-beam evaporator, massive strain would occur in the thin films. As shown in figure 4.5, this could be seen as wrinkles and cracks, and often also bubbles that would burst, revealing the bare ER beneath. In some cases the strain even distorted the contact patterns to such a degree that parts of it broke off during lift-off. Hence, a significant amount of work was done, not just by Dong Chul Kim and myself, but also by Espen Rogstad, the nanolab engineer in charge of the e-beam

evaporator, to reduce the occurrence of strain so that proper lift-off could be achieved.

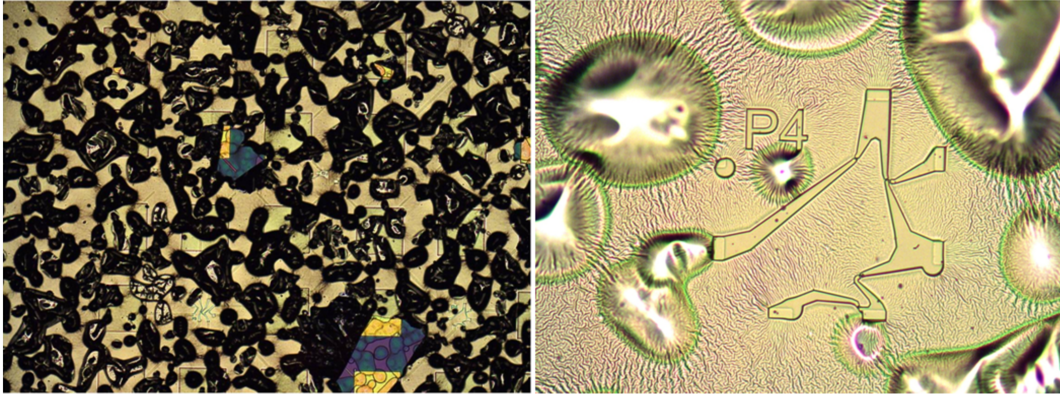

Figure 4.5: Presence of strain the the thin film after metal deposition using an e-beam evaporator.

For comparison, figure 4.6 shows one of the samples where metalization was done at IBM.

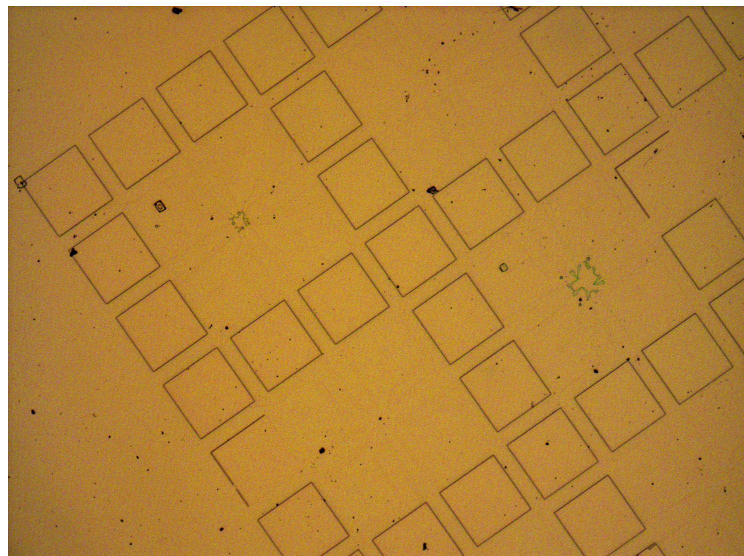

Figure 4.6: Optimal metalization as done at IBM

4.4.1 Optimizing the metalization process

The origin of this strain is thought to be evaporation of the ER due to high local heating. There are two different sources of heat in the system. One is thermal radiation from the target since the distance between the target crucible and the sample stage is quite small within the chamber (32,2 cm); the other is due to the flux of evaporated

metal. Several measures were taken to reduce this heating effect, as discussed below.

First of all the deposition procedure itself was revised. As mentioned earlier, the evaporator was run in manual mode to give proper control of the deposition rates. It was found that the strain could be reduced, at least to some degree, by increasing the deposition rate, thereby reducing the time the samples were exposed in the chamber. This was further improved by depositing thinner layers of metal. However, neither the deposition rate nor the metal thickness could be chosen completely freely as higher deposition rates results in reduced contact quality, in addition to a certain metal thickness being required to sufficiently cover the wires to give a good contact. It was found that deposition rates between 3 and 5 Å/s was optimal, with metal thicknesses approximately equal to the diameter of the NWs.

As discussed in appendix B, metalization using a sputterer with a thermal evaporation mode was also tested, with the hopes of avoiding the problems with the e-beam entirely, however, after a number of tests this possibility had to be discarded due to problems with lift-off and poor contact quality.

Further, tests were done where the distance from the target to the sample (working distance) was increased. This was done by opening the chamber and attaching the sample to the heater, located at what would usually be the backside of the sample holder. This could obviously not be used for a regular process, as opening the chamber with the following evacuation took at least two hours, but it was interesting to see if the increased distance would give better results. In this way the distance could be increased by 5 cm, giving a working distance of approximately 37 cm, however, the results showed close to no improvement. Good metalization using working distances between 40 and 54 cm has been reported, indicating that the current setup of the e-beam evaporator is not optimal.

The last measure taken to increase heat dissipation in the system was to fabricate two new sample holders, one made of aluminum and one of copper, both with a thickness of about 7 mm to act as a heat sink during deposition. Of these, the Al plate seemed to give some improvement, with one of the samples (As580-2 sample 2, see figure 4.7) showing a large area free of strain. Whether or not this is purely coincidental is unknown, nevertheless, it is the first sample where proper metalization have been observed over such a large area.

4.4.2 Metalization summary

Table 4.1 provides an overview of metalization schemes as well as the etching parameters of the samples of which IV characterization was done successfully.

As can be seen, different metal combinations were tested, but for the most part Pd was chosen for the interface to the p-doped NWs (in some cases after a thin layer

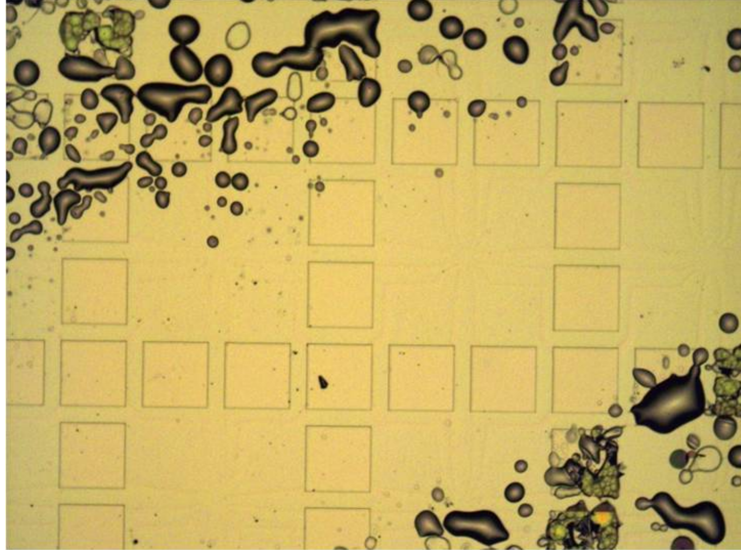

Figure 4.7: Improvement of the metalization, seen in OM

Table 4.1: Metalization summary

Sample	Date	Etch/passivation	Metalization [nm]
As 518-2, #3	06.10.2010	10s/2min	Ti(5)/Pd(40)/Au(35)
As 518-3, #3	17.11.2010	10s/2min	Pd(15)/Au(65)
As 539-8, #2	19.11.2010	10s/20s/2min	Pd(10)/Au(25)
As 539-6, #1	30.11.2010	10s/17s/2min	Pd(10)/Au(35)
As 580-2, #1	16.05.2011	8s/2min	Ti(14)/Au(76)
As 580-3, #3	16.05.2011	8s/2min	Ti(14)/Au(76)
As 562-3, #1	18.05.2011	8s/2min	Pd(10)/Zn(10)/Pd(70)
As 562-3, #2	18.05.2011	8s/2min	Pd(40)/Ti(10)/Au(40)
As 580-2, #2	24.05.2011	8s/1min	Pd(10)/Ge(50)/Au(30)
As 580-3, #4	24.05.2011	8s/15s/2min	Ti(14)/Au(76)

of Ti acting as an adhesive) due to its high work function (5.12 eV) and good vetting to the wires. Similarly, Ti was chosen for the n-doped wires due to its smaller work function (4.33 eV).

Despite of all these tweaks to the metalization process, strain is still present in most of the thin films, and it seems there is currently nothing further that can be done with the equipment available at the NanoLab. Regardless, satisfactory lift-off can still be achieved in many cases, as can be seen from the post lift-off SEM inspection pictures in appendix C.

4.5 IV characterization

As can be seen in appendix E, all samples, save possibly the core Si doped ones(As518-3, sample 3), show diode-like features, indicating that ohmic contacts have not been achieved. Ohmic contacts exhibit linear characteristics, as opposed to the the rectifying nature observed here, indicating Schottky contacts. Several different mechanisms can explain this behavior, as discussed below.

One possible reason is insufficient surface treatment and/or passivation of the NW surface, either by the etchant not being able to remove all of the native oxide layer, or that passivation was not effective enough, leading to growth of new oxide before entering the samples into the e-beam evaporator. Should this be the case, as discussed in chapter 2.7, the oxide will introduce additional surface states within the bandgap, which can pin the Fermi level in the bandgap. Thereby effectively trapping charge carriers resulting in an energy barrier, giving similar IV characteristics regardless of the deposited metal.

As discussed in chapter 4.3, another reason might be remnant shell after etching. Since it is difficult to selectively etch the shell with citric acid, and since overetching should be kept to a minimum due to the strong increase of NW resistance with decreasing diameter (Belived to be due to the radial confinement becoming strong enough to deplete the wire of carriers [18]), one can not be sure that all of the shell has been removed. Should this be the case, contacting the intrinsic shell instead of the doped core would obviously give rectifying behavior.

For the Si doped samples, the low currents can also be explained by the fact that Si, when used as a dopant in GaAs, is *amphoteric*. This means that the Si atoms can act both as donors and acceptors depending on whether they reside on the column III or column V sub lattice of the crystal [25, p. 84]. In GaAs it is common for Si impurities to occupy Ga sites, hence serving as a donor. However, an excess of As vacancies arising during growth or processing of the NWs can cause Si impurities to occupy As sites, where they act as acceptors. Hence, choice of contact metal is not straight forward, and might give different results than expected.

Another interesting observation is that most of the currents measured (except for the p doped core Be sample (As518-2) and the p-i-n samples (As562-3)) is on the same order as currents in intrinsic NWs (observed to tens of nA). This indicates that most dopants are either not electrically active, or maybe not even present in the NWs at all. Exactly how dopants are incorporated into the NWs under VLS growth is currently not know, so it is uncertain how these dopants affect the IV characteristics. This will most likely improve as better insight into VLS growth and doping is obtained.

Should it turn out that the doping concentration is in fact much lower than expected, while the doping concentration of the shell is relatively certain as it is grown using VS growth mode (also known as thin film growth mode which is well studied),

another effect can explain the low currents observed for two Te doped core/shell samples (As 580-3). If the core is close to intrinsic, modulation doping effects can occur, effectively trapping the majority carriers (in this case electrons) in the core/shell interface, resulting in non-ohmic behavior. To investigate this, the first sample was contacted directly to the shell, whereas the second was etched to contact the core, however, as mentioned in chapter 4.3, proper etching was not achieved, which is probably the reason why the two samples show very similar IV characteristics.

As for annealing, it seems to generally give somewhat more linear characteristics, but contrary to what was expected the current was in most cases reduced.

Chapter 5

Preliminary Conclusions and Future Work

Over the course of this work, devices of single, doped GaAs nanowires have been fabricated. By making new substrates, the yield from each sample was increased, providing the proper statistics needed to draw valid conclusions, while at the same time reducing processing time.

The EBL procedure was optimized to reliably produce close to perfect alignment of the contact patterns. This was achieved by being very thorough during the alignment process. In particular, doing a detailed write field alignment close to the sample position prior to 3-point alignment was crucial. In this way the difference between the global and the user defined coordinate system was reduced, resulting in better alignment, as well as making the 3-point alignment easier to carry out, thereby reducing the overall time needed for the alignment procedure.

A solution of citric acid and hydrogen peroxide proved effective for etching of the AlGaAs shell where applied, however, a different composition of the shell is needed for a more selective etch, either by increasing the Al content drastically or using a different shell material entirely. Alternately, to ensure that the shell is completely removed, the diameter of the NWs could be increased to allow for more overetching. One must take care not to etch the wires too much though, as their conduction properties are very sensitive to decrease in diameter. As indicated by the samples sent for metalization at IMB, it seems that the passivation process in some cases etches the wires. This can occur if the concentration is too high, and further testing is needed to optimize the process so that a continuous passivation layer with minimum etching can be achieved. The same samples also show NWs that has been etched more at the areas that should be protected by the ER than at the contacted ends. This effect is currently not understood and needs to be investigated further.

A lot of effort has been put into optimizing the metalization process, specifically reducing the strain (in the form of wrinkles, cracks and bubbles) in the deposited metal. This strain seems to be the result of the ER evaporating during metal de-

position. This happens because of high local heating due to thermal radiation from the target and the flux of evaporated metal. This was improved to some degree by depositing thinner metal layers, at relatively high deposition rates (optimal rates seemed to be 3-5 Å/s), to reduce the time the samples were exposed in the chamber, as well as using a thick Al sample carrier to increase heat dissipation. However, despite all the measures taken to improve the metalization process, strain is still present in most films deposited by the e-beam evaporator in NTNU NanoLab, and seems to be a limitation of the machine itself. Despite this, satisfactory lift-off was achieved in most cases.

The IV characteristics of the samples are generally non-linear, which indicates that ohmic contacts have not been achieved. This can, among other, be due to both remnant shell after etching inhibiting carrier transport, as well as insufficient surface treatment introducing surface state defects. Additionally, most of the samples show currents in the same range as intrinsic NWs, indicating that the dopants are not electrically active, or even present in the NWs. Annealing the samples showed a tendency to give slightly more linear characteristics, however, the current was in most cases reduced.

Looking adead, as already mentioned, more tests should be done to optimize the passivation procedure to avoid etching of the NWs. Also, the NTNU NanoLab is currently in the process of purchasing a new e-beam evaporator, where one of the criteria is longer work distance. Hopefully this will give better results when depositing thin films on ER. Should this indeed be the case, a large number of samples can be processed in a relatively short time frame, enabling effective characterization of new samples, possibly leading to exact determination of the WZ bad gap. In the future this work can be taken a step further, by contacting arrays of NWs on substrates as grown, so that actual devices can be produced, closing in on the goal of making high efficiency solar cells from nanowires.

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Appendix A

Pattern layout and dimensions

A.1 Substrate design

It was quickly evident during the work with my project that the design of the samplesholders would need to be improved to ease the processing step and improve the yield per sample. This was to a large degree achieved by the a design made by PostDoc Dong Chul Kim, shown in figure A.1 below, made to fit on a 2 inch Si wafer.

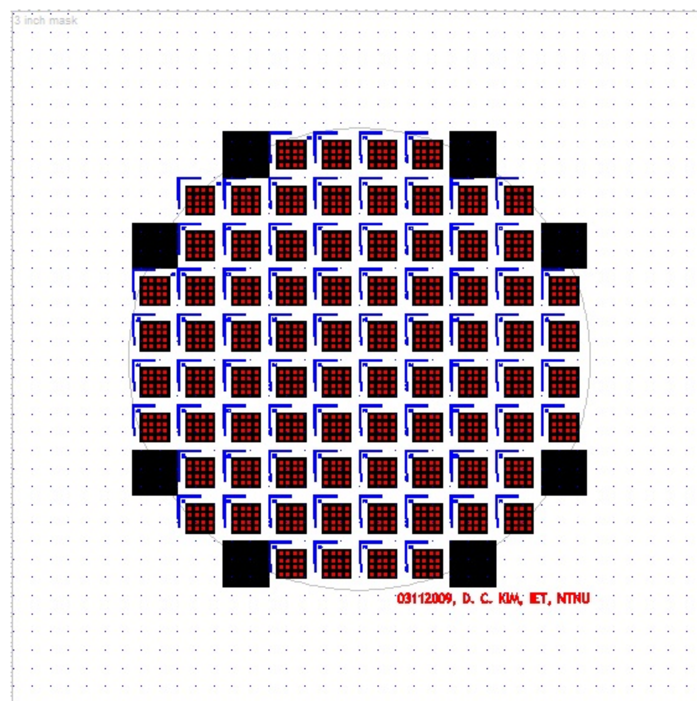

Figure A.1: Overview of the complete substrate design.

As can be seen in figure A.2, each sample has 16 different positions, where column 1 and 3 have a write field (WF) of 50 by 50 μm, and column 2 and 4 have a WF of 100 by 100 μm (as is evident in figure A.3 below).

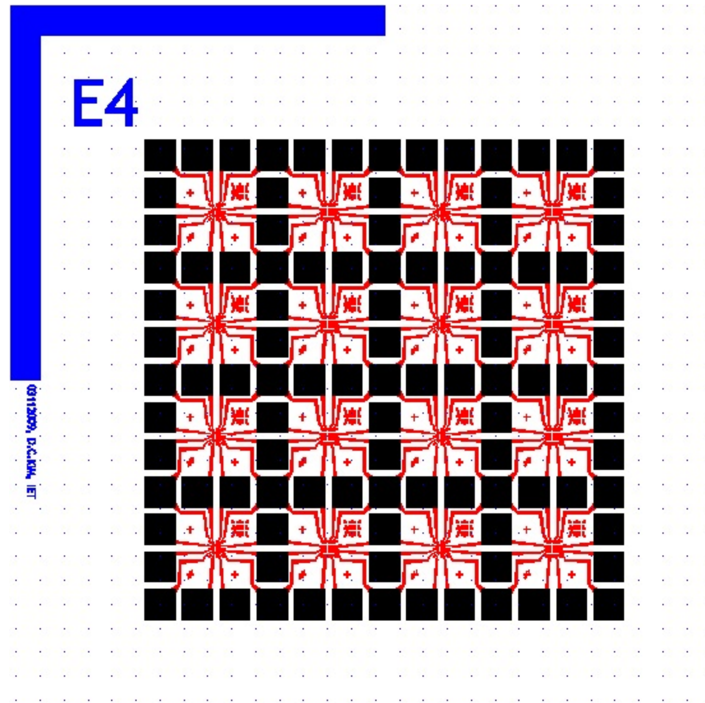

Figure A.2: Overview of a single sample design.

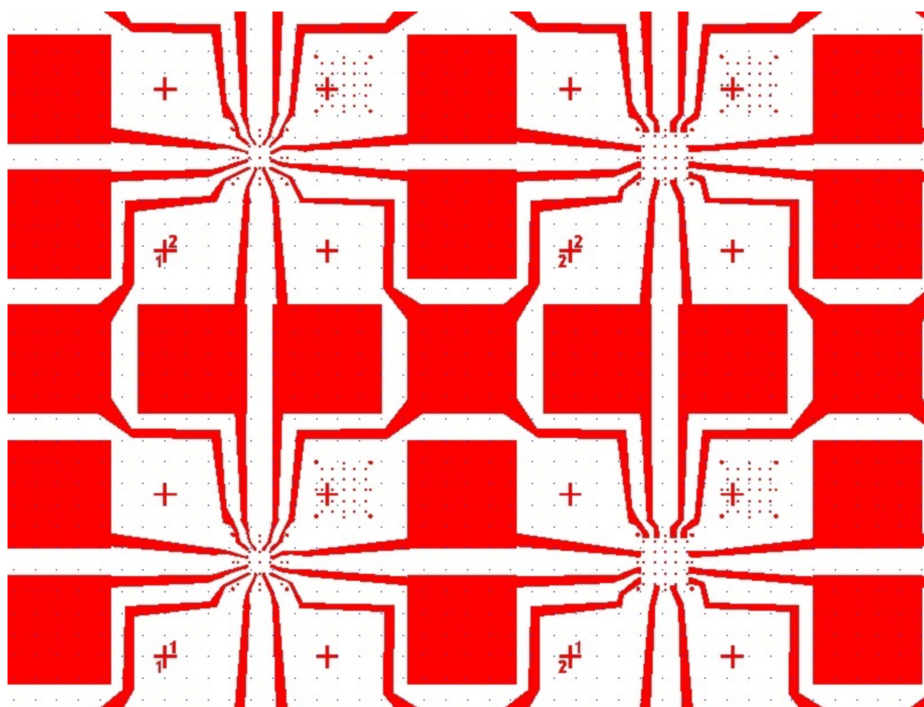

Figure A.3: Closeup of positions.

Design details of the two different write fields (figure A.4). Origo is defined at the center of the designs.

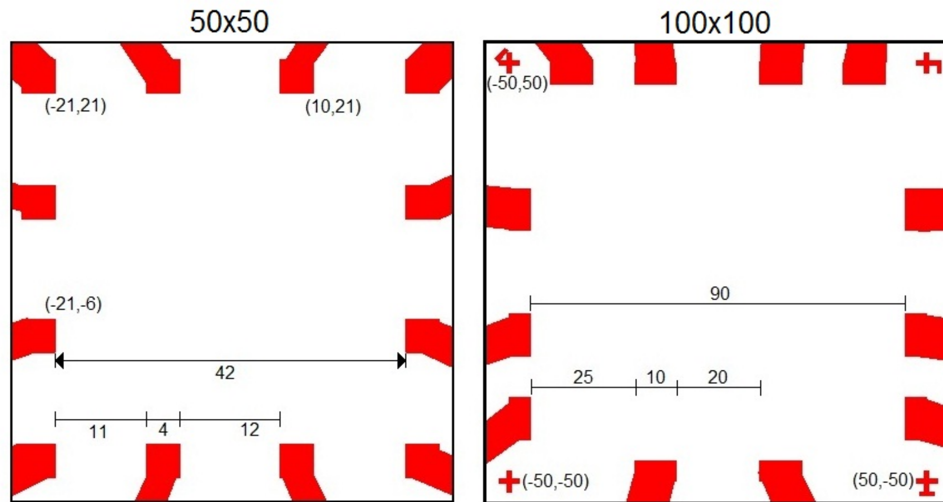

Figure A.4: Contact pad design using a wf of 50 μm (left) and 100 μm (right)

A.2 Substrate fabrication

The fabrication itself was a two step process. First, the fine details of the pattern (displayed in red in figure A.2) were deposited as a thin layer of metal, and secondly, the big contact pads (seen as black squares in A.2) were deposited as a much thicker metal layer to make them suitable for wire bonding. For the photolithography step, two different specially ordered masks were used in a MA56 mask aligner, and lift off was done by acetone splashing followed by cleaning with IPA and DI water. See table A.1 for details on the fabrication process.

After finalizing the metalization (see figure A.5 and A.6), the wafer was spincoated with a thick layer of photoresist to act as a protective layer during dicing. This was done by one of the NTNU NanoLab engineers, Espen Rogstad, using an automated scriber, yielding quite clean cuts as shown in figure A.7 below.

Table A.1: Substrate fabrication parameters

Spin coating (*)	' same for both layers
Speed	4000 RPM
Time	120 s
Thickness	≈ 1 μm
Layer 1	
Lamp power	6,1 mW/cm^2
Exposure	30 s
Develop	4 min
Plasma ashing	12 s, 50% power, 30% oxygen flow
Metalization	Ti (10 nm)/Au (40 nm)
Layer 2	
Lamp power	6,4 mW/cm^2
Exposure	30 s
Develop	4 min
Plasma ashing	12 s, 50% power, 30% oxygen flow
Metalization	Ti (10 nm)/Au (250 nm)

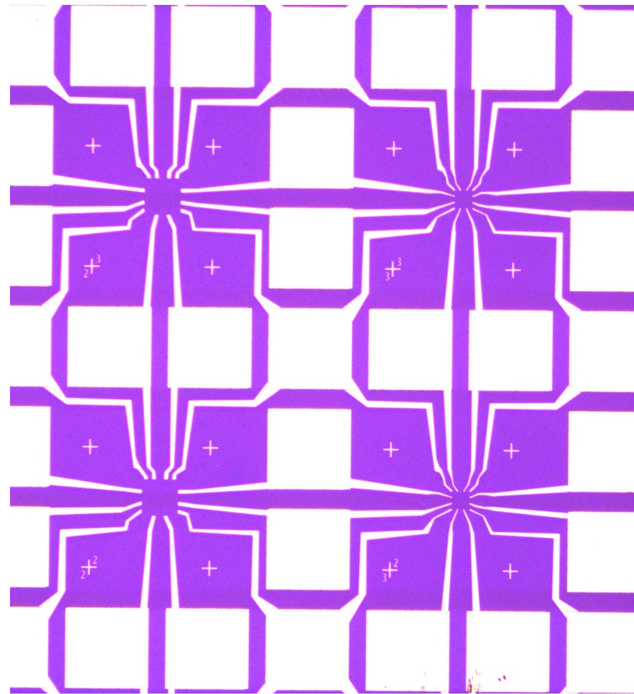

Figure A.5: Sample overview post lift off.

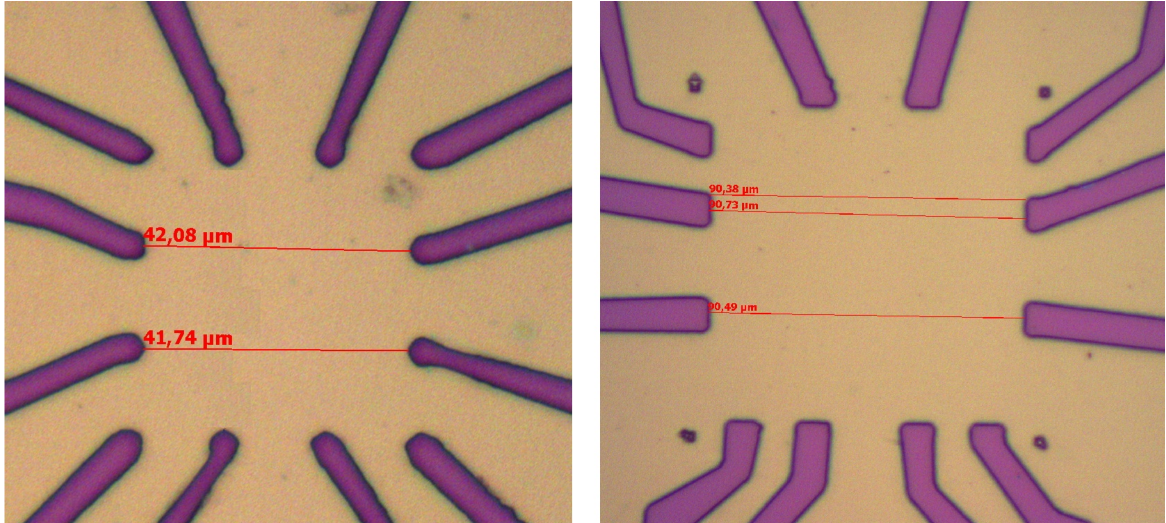

Figure A.6: 50 and 100 μm wf post lift off

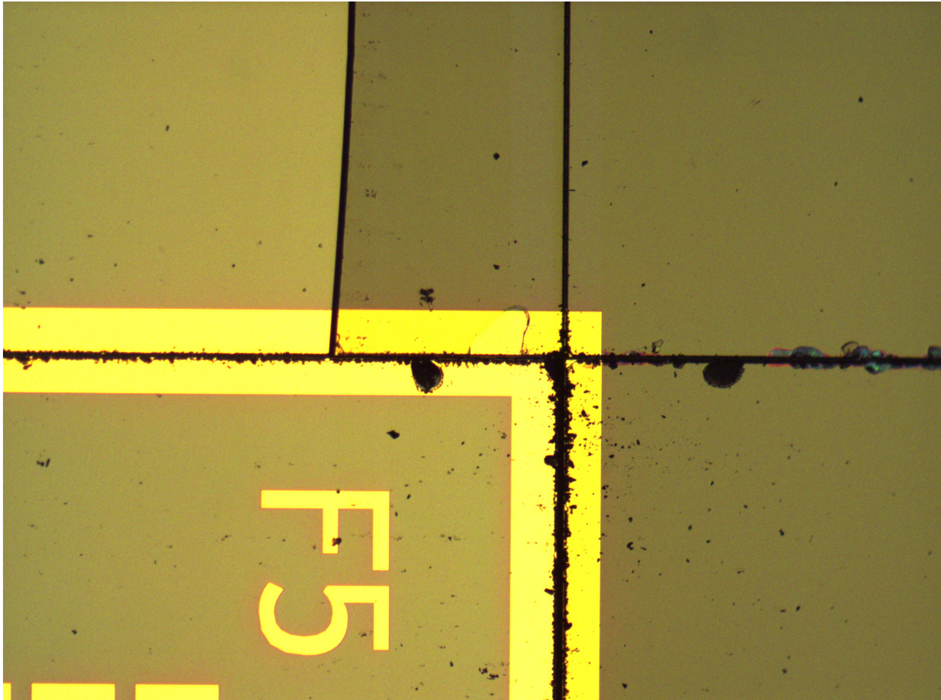

Figure A.7: Wafer diced with scriber.

Appendix B

Thermal evaporator tests

NTNU NanoLab recently installed a *Cressington 308R* sputtering system, with an additional mode for thermal evaporation of metals. With the current issues experienced with the e-beam, this was quickly investigated as a possible substitute for the e-beam for metal deposition. A number of deposition tests were carried out and the initial results were very positive. As can be seen in figure B.1 below, the deformation of the film seems much less severe, with no big cracks or bubbles.

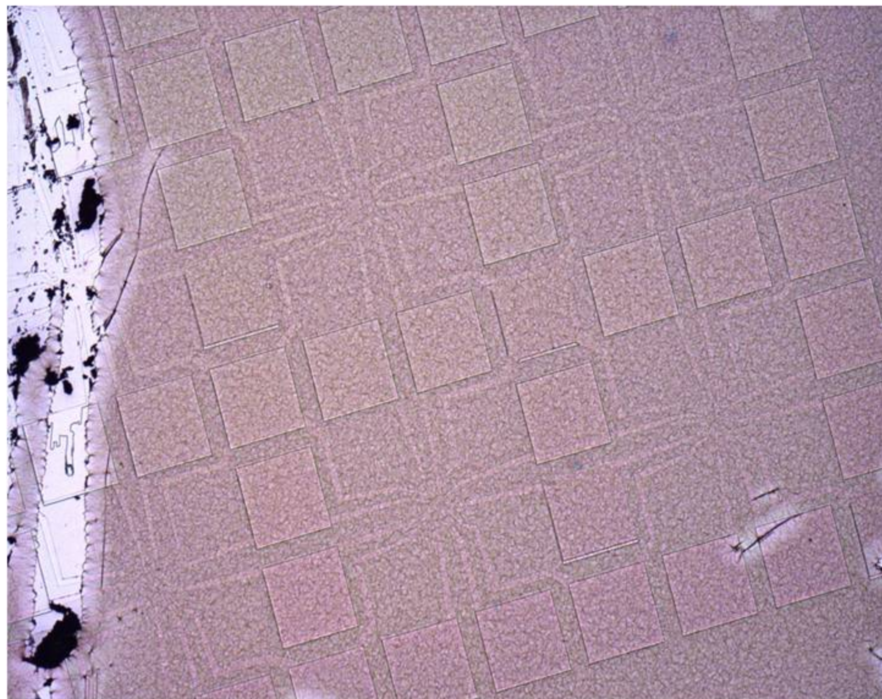

Figure B.1: Deposition test using thermal evaporation.

However, after doing tests on actual samples, it was obvious that proper lift-off could not be achieved (see figure B.2), in addition to contact quality being very poor (figure B.3).

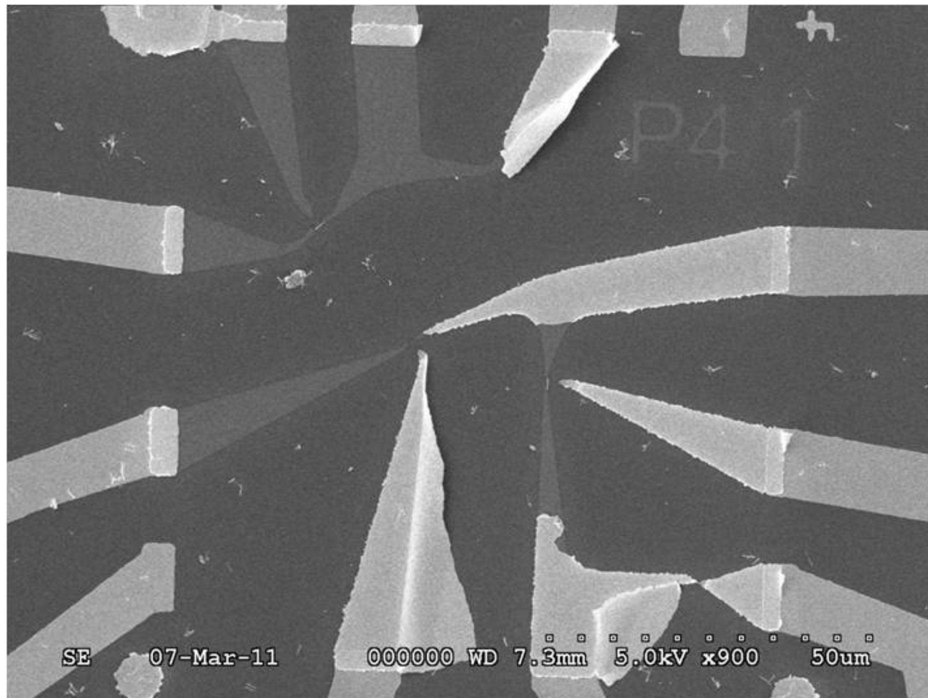

Figure B.2: Problems with lift-off after thermal metalization.

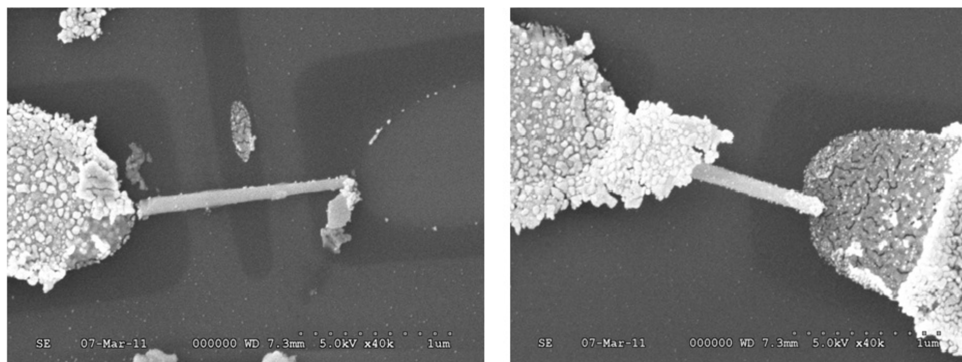

Figure B.3: Poor quality of the thermally deposited contacts as seen in SEM

These issues eventually resulted in the sputterer being discarded as a possibility for metalization.

Appendix C

NW contacts and IV measurements

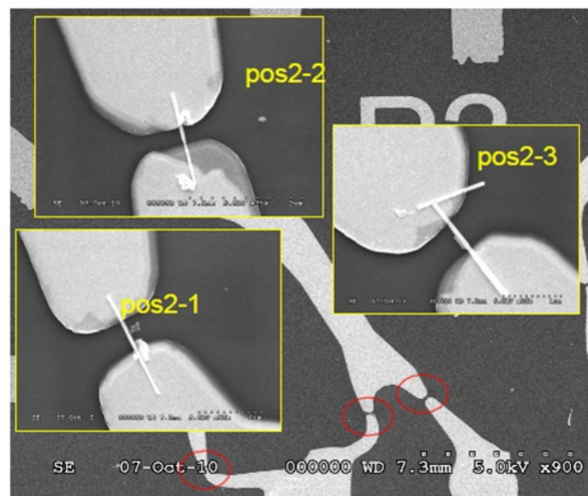

Figure C.1: As518-2, sample 3: Contacts as seen in SEM.

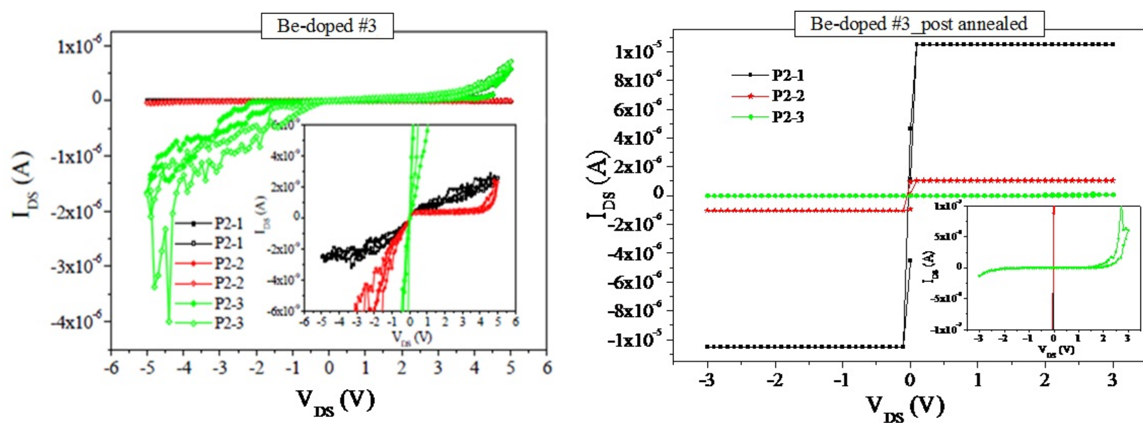

Figure C.2: As518-2, sample 3: IV characteristics before and after annealing.

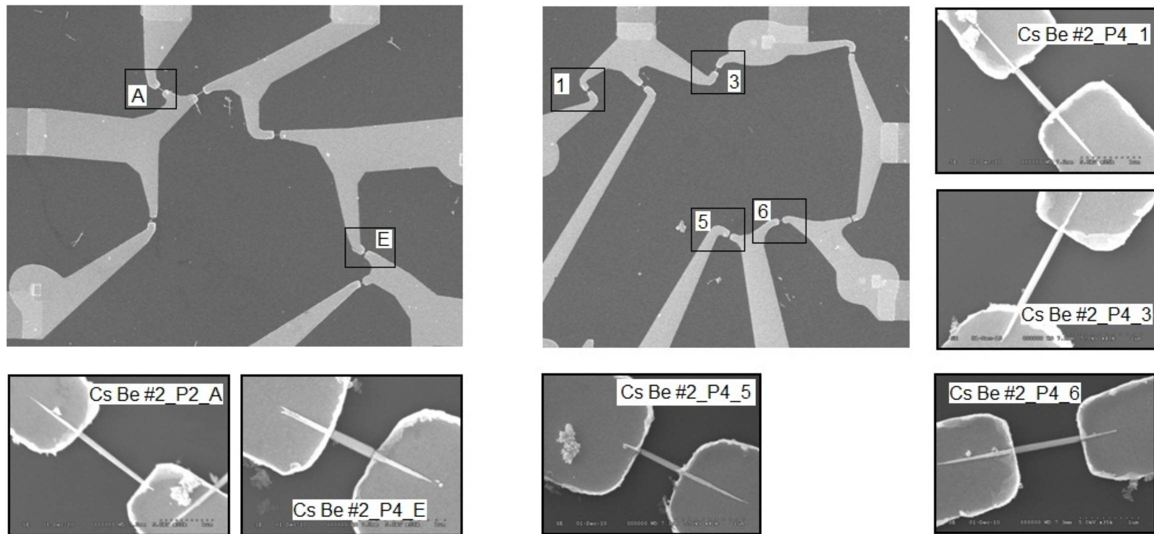

Figure C.3: As539-8, sample 2: Contacts as seen in SEM.

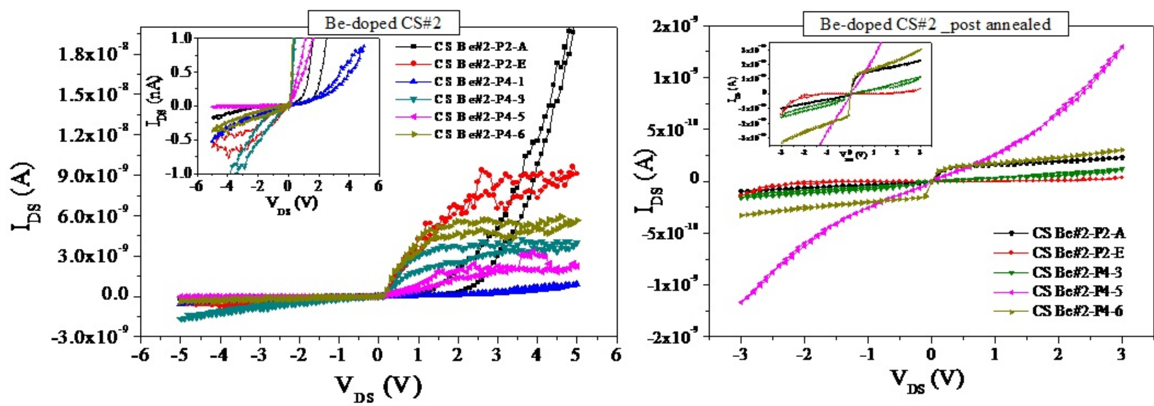

Figure C.4: As539-8, sample 2: IV characteristics before and after annealing.

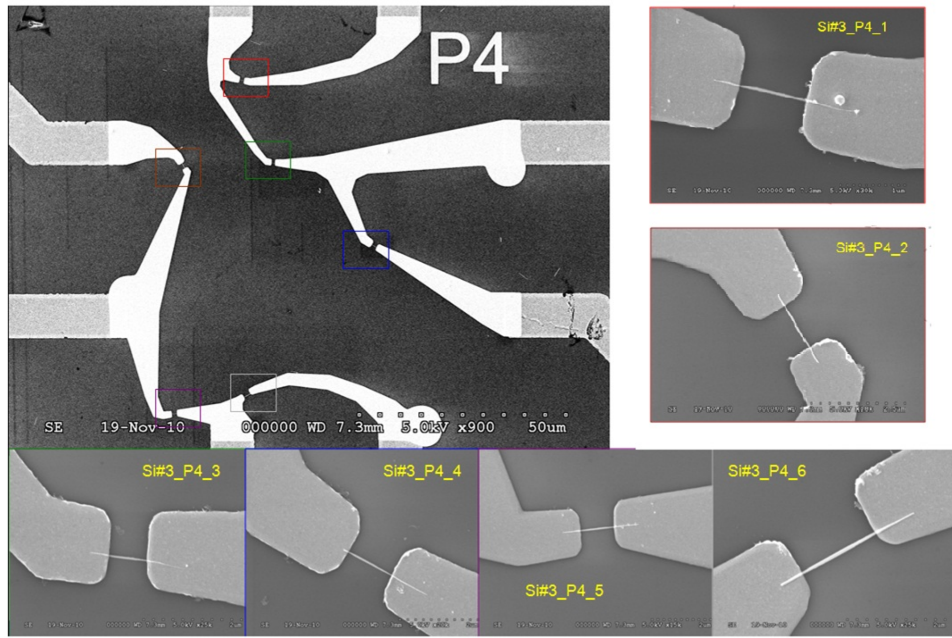

Figure C.5: As518-3, sample 3: Contacts as seen in SEM.

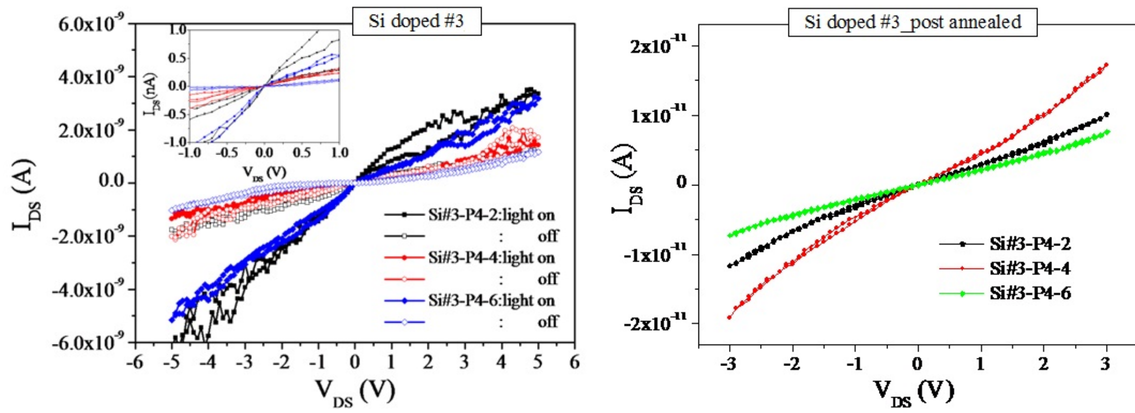

Figure C.6: As518-3, sample 3: IV characteristics before and after annealing.

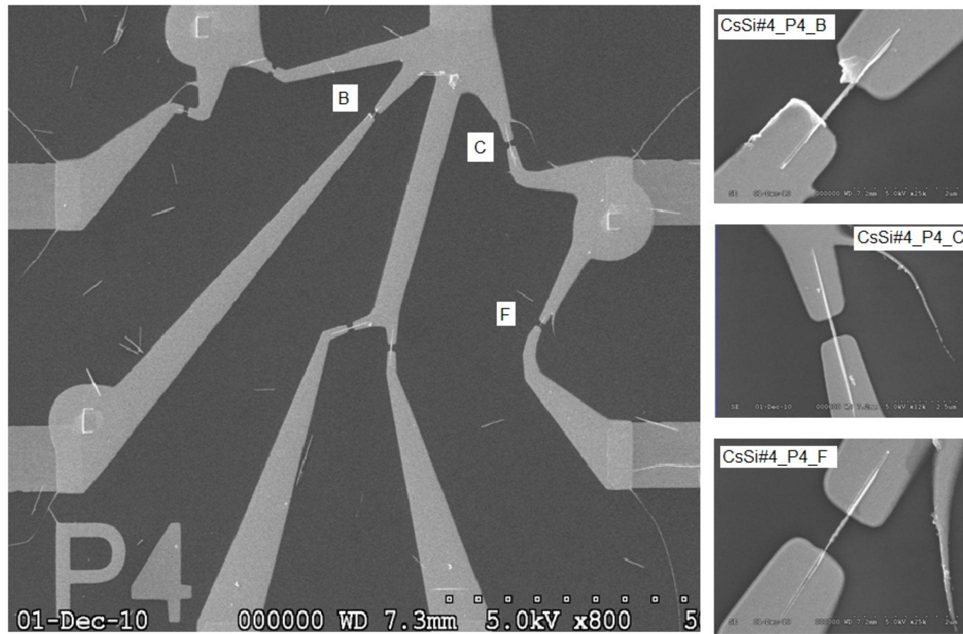

Figure C.7: As539-6, sample 1: Contacts as seen in SEM.

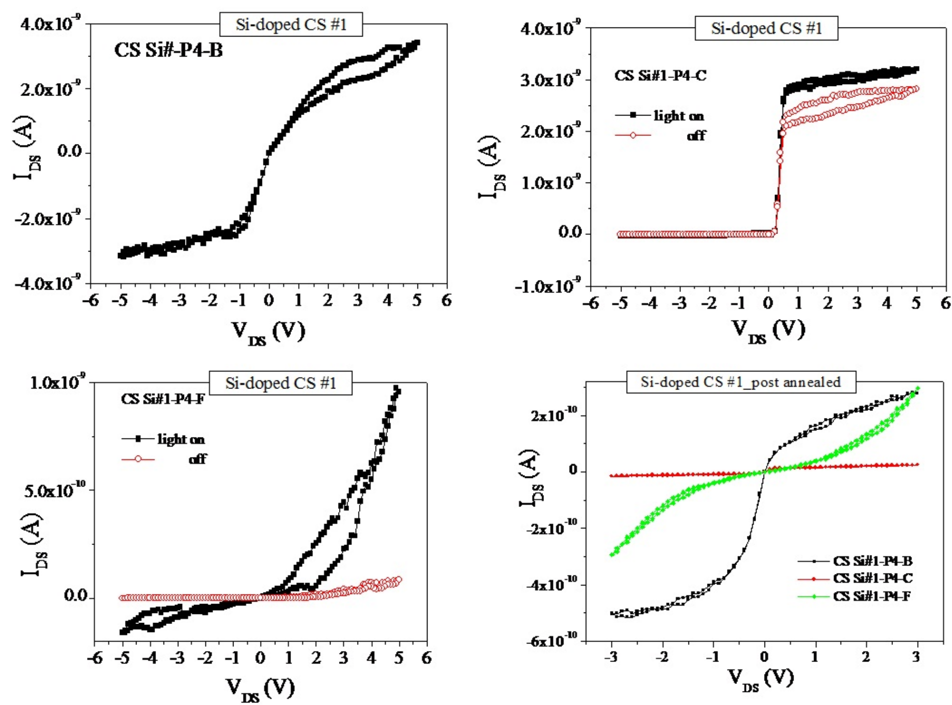

Figure C.8: As539-6, sample 1: IV characteristics before and after annealing.

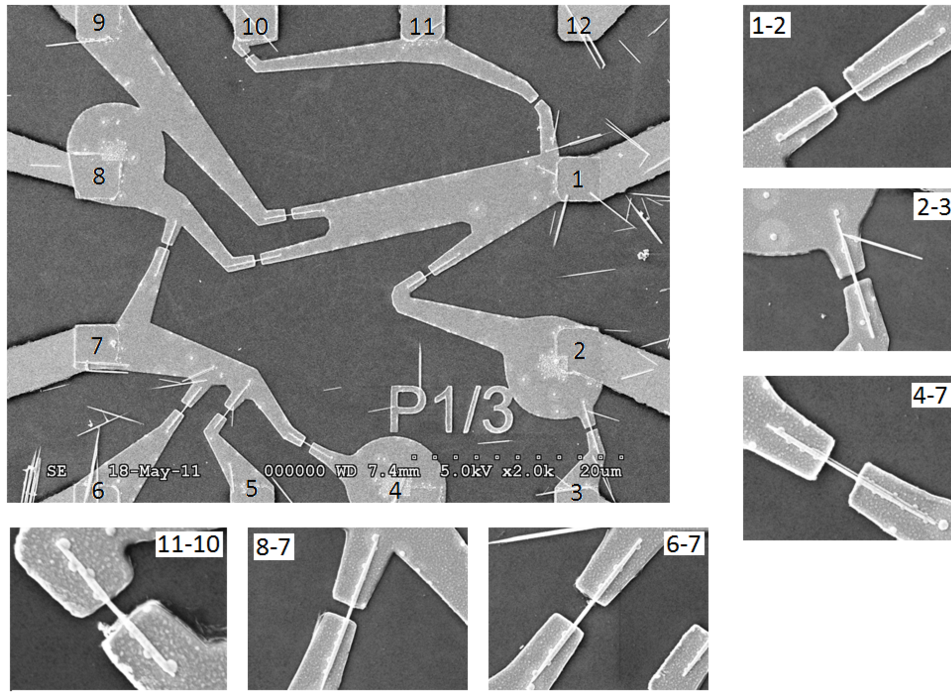

Figure C.9: As562-3, sample 1: Contacts as seen in SEM.

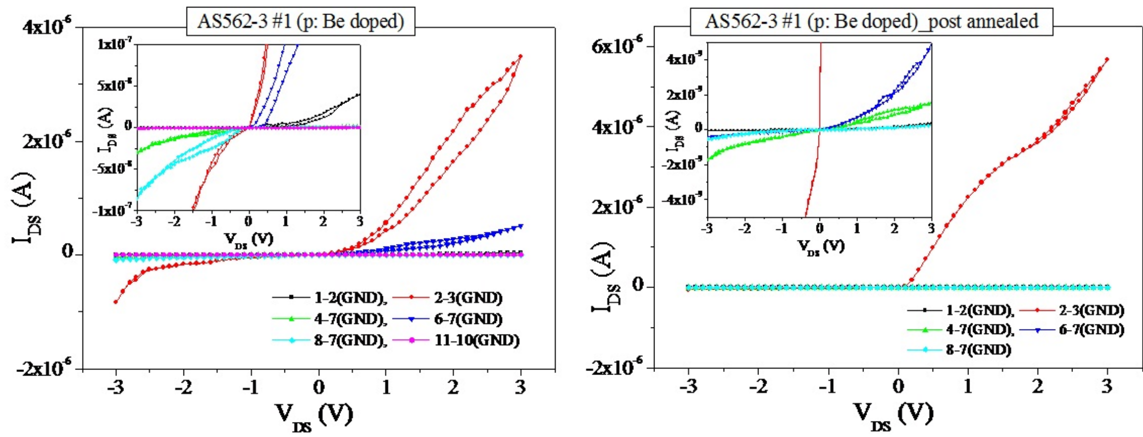

Figure C.10: As562-3, sample 1: IV characteristics before and after annealing.

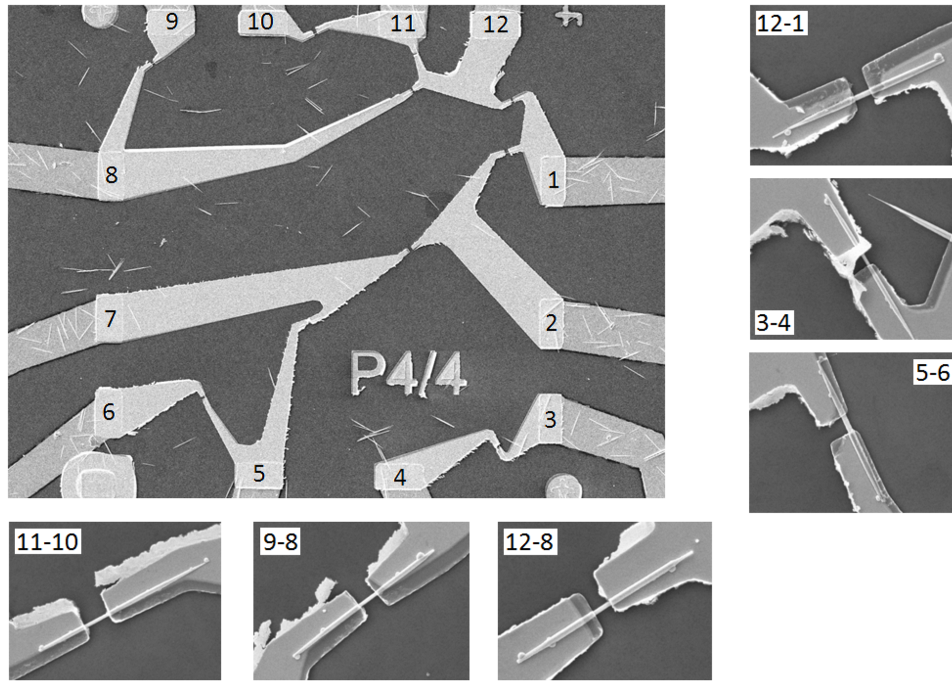

Figure C.11: As562-3, sample 2: Contacts as seen in SEM.

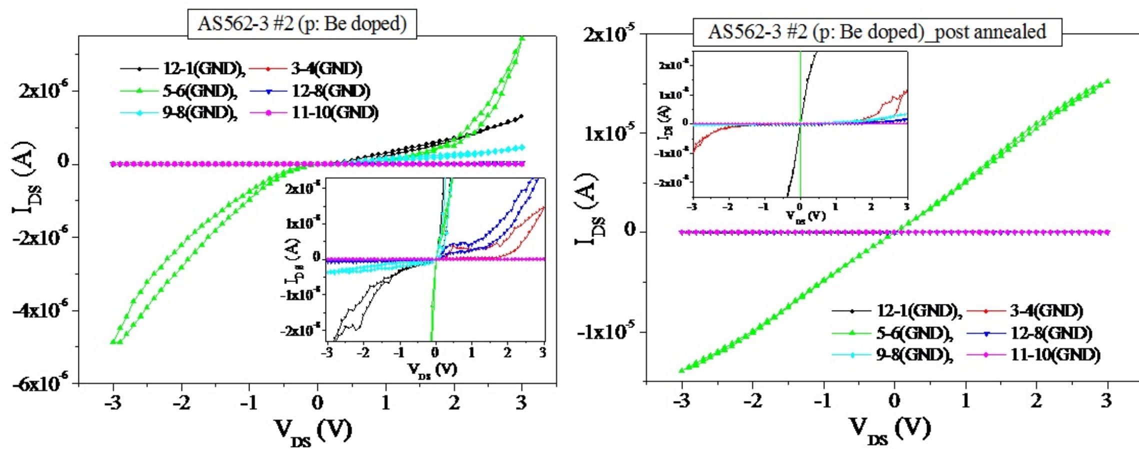

Figure C.12: As562-3, sample 2: IV characteristics before and after annealing.

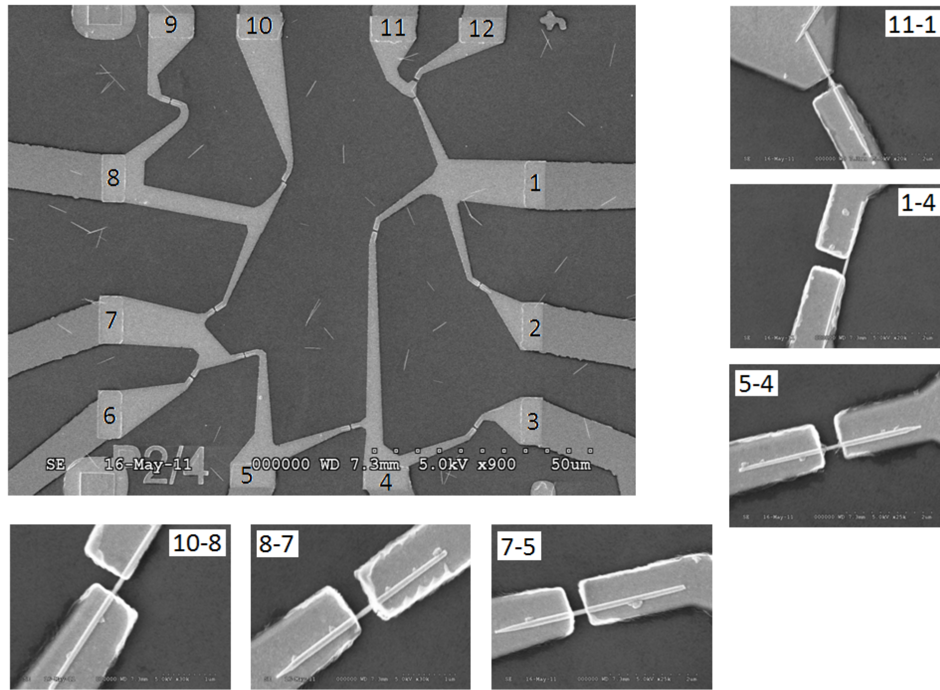

Figure C.13: As580-2, sample 1: Contacts as seen in SEM.

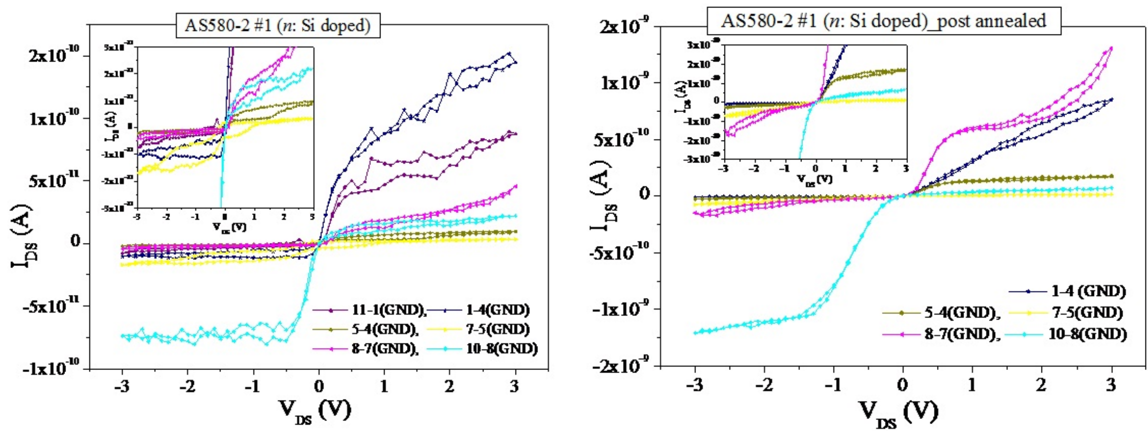

Figure C.14: As580-2, sample 1: IV characteristics before and after annealing.

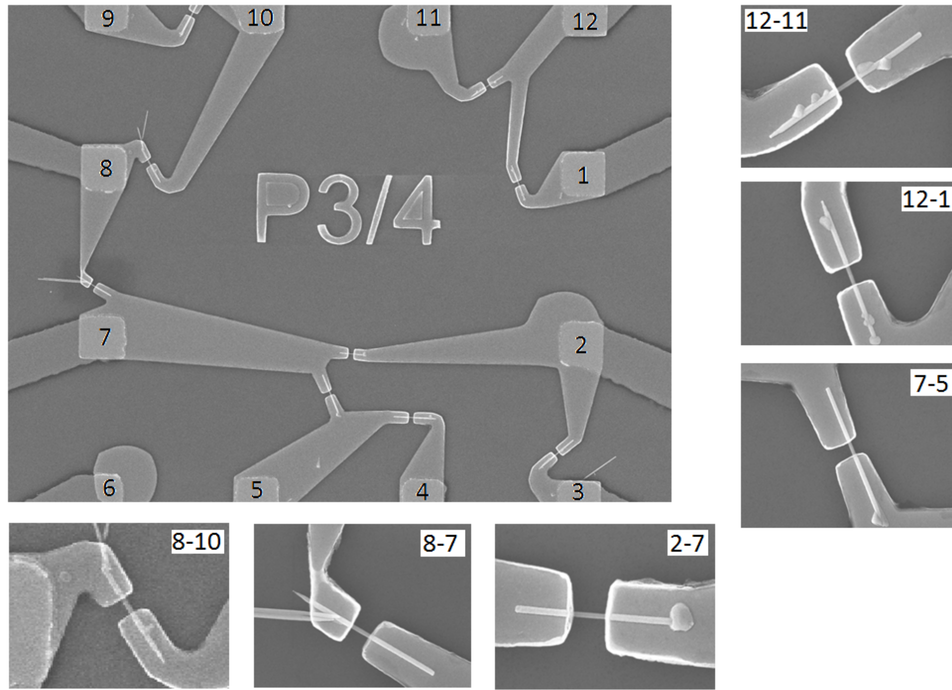

Figure C.15: As580-2, sample 2: Contacts as seen in SEM.

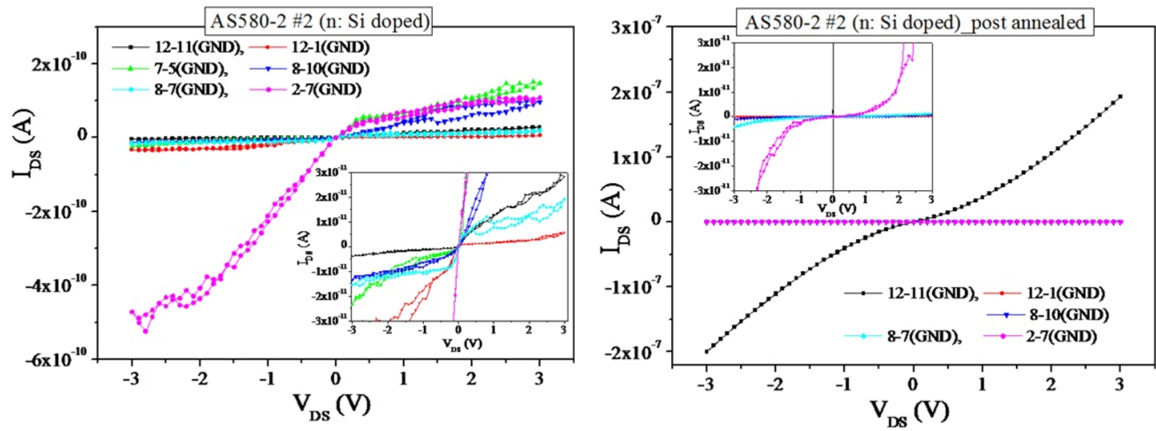

Figure C.16: As580-2, sample 2: IV characteristics before and after annealing.

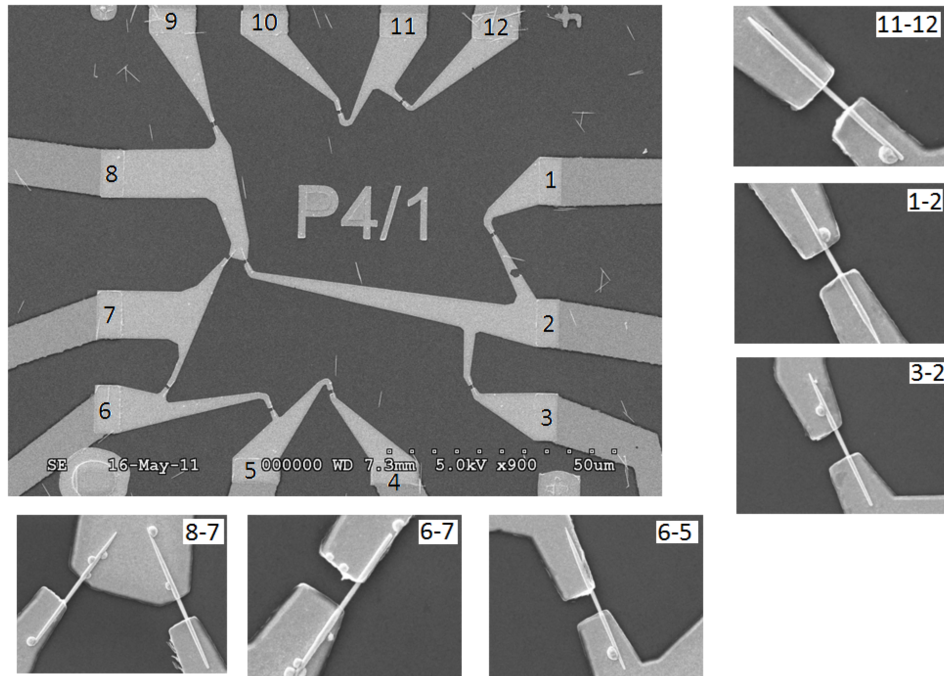

Figure C.17: As580-3, sample 3: Contacts as seen in SEM.

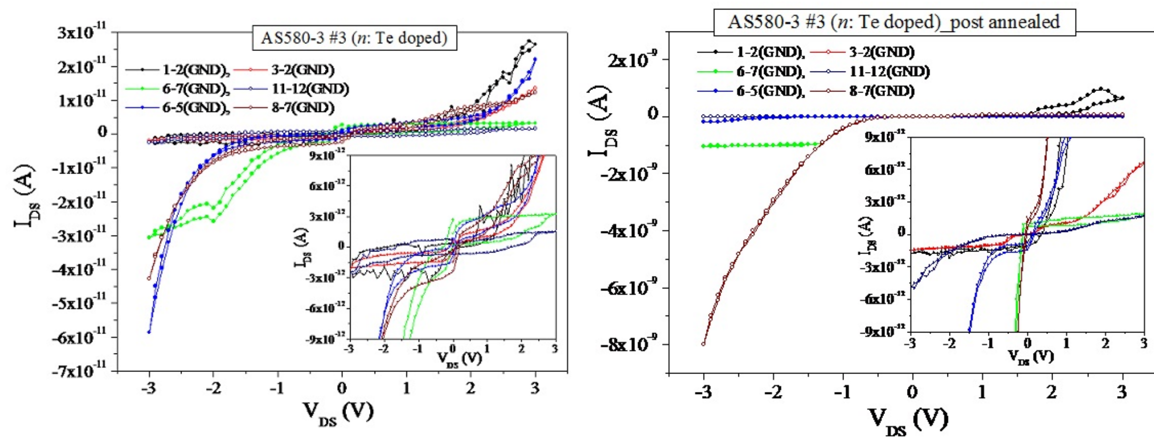

Figure C.18: As580-3, sample 3: IV characteristics before and after annealing.

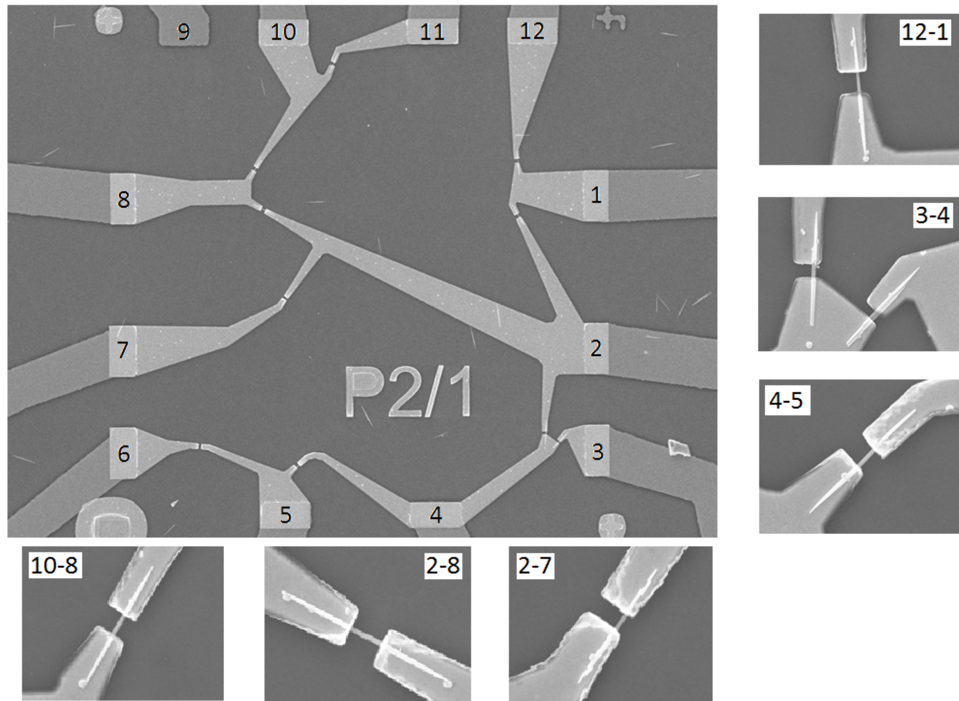

Figure C.19: As580-3, sample 4: Contacts as seen in SEM.

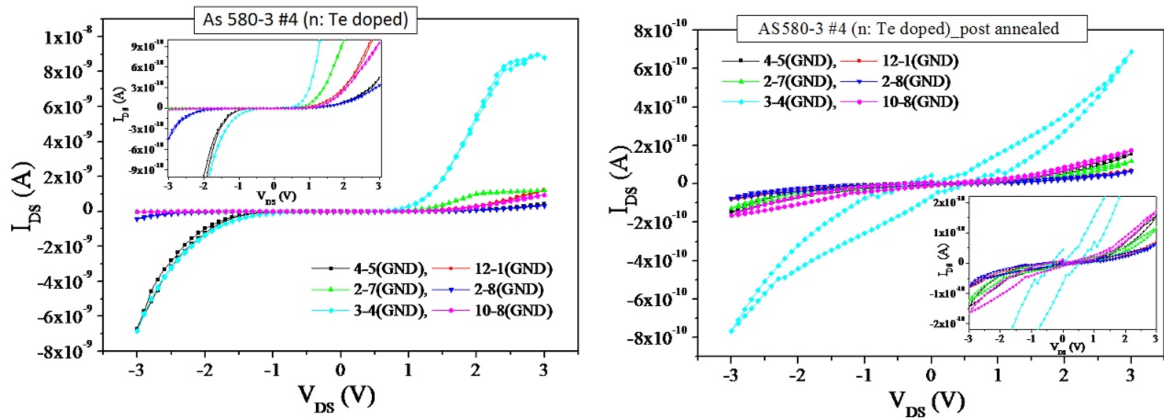

Figure C.20: As580-3, sample 4: IV characteristics before and after annealing.