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Design and Modelling of a High Resolution, Continuous-Time Delta-Sigma ADC

In-depth noise considerations and optimization

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Problem description

The main objectives of this work is to model and analyze different topologies for a Continuous-Time $\Delta\Sigma$ A/D converter and make an informed decision on the optimal architecture, with respect to efficiency, for a given set of system requirements.

The performance requirements are listed below

- 2.5 MHz input signal bandwidth, equivalent to 5 MS/s
- 74 dB SNDR, equivalent to 12 bits resolution
- 84 dB SFDR
- Application: Communication

The basis of this work rest on the development and results achieved in a project by the author documented the fall of 2010[1].

Assignment given: February 1, 2011
Supervisors: Ivar Løkken, Hittite Microwave Corporation and Trond Ytterdal, NTNU

Abstract

This work documents the important design considerations and high–level development of an efficient Continuous-Time $\Delta\Sigma$ A/D converter for given system requirements. Projecting characteristics is especially essential in the design of the option-versatile $\Delta\Sigma$ converter and involves both advanced control and signaling theory, in addition to circuit and system design. Thus, extensive simulations was carried out through synthesis and behavioral modelling.

Synthesis was performed using R. Schreiers $\Delta\Sigma$ toolbox while modelling was done using the framework of CADENCE with VIRTUOSO and SPECTRE. Behavioral modelling was based on the mixed-signaling language VERILOGA. A list of candidates, meeting the performance requirements set, was formed from synthesis and two modulator architectures stood out; a multi-bit 3^{rd} order and a single-bit 5^{th} order, both with an oversampling ratio of 32. Both feedback and feedforward loop filter structures were analyzed.

A useful and powerful analysis was carried out to characterize and quantify the impact of location on nonidealities in $\Delta\Sigma$ modulators. The model was prepared for verification, helping to analyze, characterize and specify crucial parts of each structure. Decisive nonidealities, such as excess loop delay, finite DC gain, limited GBW, circuit noise and their influence on the overall modulator were included and examined. From this, a specification for the integrators as well as a preliminary noise and power budget was established.

The final result ends in a realistic environment capable of analyzing different types of CT$\Delta\Sigma$ structures and making an informed decision on the most optimal and suitable configuration. Results from synthesis and behavioral modelling showed a great correspondance between the results obtained in each part. After an iterative process of evaluating performance among other metrics with nonideal effects, the best architecture was found to be the 3^{rd} order multi-bit feedback modulator, which achieved all of the requirements while consuming 3724 μW.

Acknowledgements

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I would like to thank Hittite Microwave Corporation for letting me stay at their arctic design center and especially supervisor Ivar Løkken for offering great support and guidance throughout the work with this thesis. From troubleshooting to sharing his experience, I'm deeply grateful for his genuine dedication and useful input.

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Trondheim, June 27, 2011
Lars Rypestøl

Abbreviations

AAF Anti-Aliasing Filter
ADC Analog-to-Digital Converter
CI Chain of Integrators(Cascade is also used instead of chain)
CT Continuous-Time
DAC Digital-to-Analog Converter
DEM Dynamic Element Matching
DT Discrete-Time
DWA Data Weighted Averaging
ELD Excess Loop Delay
FB Feedback
FF Feedforward
ISSCC International Solid-State Circuits Conference
NG Noise gain
NRZ Non-Return-to-Zero
NTF Noise Transfer Function
OSR OverSampling Ratio
PSD Power Spectral Densities
RMS Root-Mean-Square
S/H Sample-and-Hold
SoC System on Chip
STF Signal Transfer Function

Symbols

$\Delta\Sigma$ Delta-Sigma

Metrics

A_0 DC amplifier gain
f_B Input signal bandwidth
f_{in} Input signal frequency
f_S Sampling frequency
GBW Gain Bandwidth
PM Phase Margin
SFDR Spurious-Free Dynamic Range
SMNR Signal-to-Mismatch-and-Noise
SNDR Signal-to-Noise-and-Distortion Ratio
SNR Signal-to-Noise Ratio
SQNR Signal-to-Quantization-Noise Ratio

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1 Introduction

In the rapidly increasing market for portable and low-powered devices for communication and consumer electronics, the shift of functionality to the digital domain and the resulting relocation of the analog-to-digital interface to the front-end, has led to increased interest in development of the indispensable analog-to-digital converter(ADC). The growing trend of placing data conversion closer to the system front-ends and let clever and technology-scaling digital circuitry dominate, reduces the overall power dissipation, however at the cost of increased design challenges as the stringent demands of the ADC get higher. High-resolution, wide bandwidth and low-power are some of the most desirable converter properties in todays electronic industry. The contradicting desire/request of converters operating at an even higher data throughput whilst consuming even less power is of major interest. Significant effort has been made to create power efficient converter interfaces meeting the demands of the next generation of wireless communication. Anticipated requirements for bandwidth in the next generation of receivers, are in the tens of MHz range with a dynamic range of at least 10 bits[4].

Low-power Continuous-Time(CT) Delta-Sigma($\Delta\Sigma$) ADCs have been given increased attention recently, resulting in rapid performance increase in both published literature and the market. Oversampled and noise-shaping converters provide highly desirable benefits with respect to their traditional ADC counterparts[1]. Compared to the commonly used Nyquist pipeline conversion employed at analog receiver front-ends, oversampling $\Delta\Sigma$ converters trade signal processing complexity with relaxed requirements for analog components[3]. In comparison to their well proven and established Discrete-Time(DT) counterparts, mainly two, often claimed, unique benefits apply to the CT$\Delta\Sigma$ converter. First, the well known property of possessing an inherent anti-aliasing filter(AAF) potentially enables the possibility of eliminating or at least significantly reduce the AAF that is typically preceding other ADCs. Secondly, in contrast to the clock rate being limited by settling-time constraints, thus limit the sampling frequency resulting in a narrow bandwidth from oversampling, the clock rate in CT$\Delta\Sigma$ is theoretical only limited by the speed of the internal quantizer and feedback digital-to-analog converters(DACs). In practice, CT$\Delta\Sigma$ can convert and digitize signals in the tens of MHz range while DT still lacks this ability[5]. The overall result; reduced system complexity and power while simultaneously relaxing the requirements on filters and accurate sample-and-hold(S/H) circuitry.

However, although these benefits combined typically yield an exceptionally effective ADC, CT$\Delta\Sigma$'s also suffer from unique nonidealities such as the unavoidable excess loop delay and fundamental circuit limitations such as noise, all of which need to be accounted for. The foundation of this work come from the investigating study performed in [1] by the author, suggesting a CT$\Delta\Sigma$ ADC

to be the most effective architecture for the performance requirements provided. Although published literature describes several different implementations of the $\Delta\Sigma$ modulator, to limit the range of candidates, only traditional, modulator structures are investigated.

1.1 Outline of thesis

The rest of section 1 contains motivation and specific CT$\Delta\Sigma$ problems encountered, as well as some literature background. Section 2 contains a brief theoretical overview of the fundamental mechanisms and aspects in $\Delta\Sigma$ converters. Section 3 include noise considerations and analysis specific for CT$\Delta\Sigma$ converters, used to develop a realistic model. Next, sections 4 and 5 describe and summerize the methods and results obtained from the synthesis and the behavioral modelling. Finally, section 6 discuss the findings before concluding in section 7. Final considerations and remarks are given in section 8.

1.2 Motivation

A common issue in communication applications is the strong spectral components close to the carrier frequency. This problem necessitates[1] a high–performance AAF in order to minimize their impact when folding back into the signal band during sampling. By having features such as inherent anti-aliasing and high bandwidth capabilities, in addition to the common $\Delta\Sigma$ characteristics of noise-shaping and oversampling, CT$\Delta\Sigma$ converters are geared towards and have become the choice for many wired and wireless communication applications.

However, although the benefits of CT$\Delta\Sigma$ converters are desirable for communication systems, the design procedure typically involves more effort in modelling and analysis then normal Nyquist converters. Advanced control theory and signal processing is a large part of the design process and needs to be extensively examined to ensure proper operation and help determine block requirements of the final design. Compared to the DT$\Delta\Sigma$ architecture, effects such as high sensitivity to clock jitter, feedback loop delay and large component variations give the designer additional challenges.

Normal design procedure of CT$\Delta\Sigma$ modulators makes use of the equivalence between a CT modulator and a filter followed by a DT modulator. By constructing a DT prototype, one can transform it to CT by making sure the noise transfer functions(NTFs) are equivalent. In order to achieve this goal, the DT's impulse response must match the CT's sampled response which leads to the two systems implementing the same noise transfer functions. This is commonly done using

[1] Recall that the Nyquist theorem demands the sampling of any signal to performed at least at twice the signal bandwidth to avoid loss

the impulse-invariant transformation[2, 6]. This is also where one of the major challenges of CT design appear. In order to achieve equivalent responses, the internal quantizer and DAC must operate and deliver its feedback instantaneously. Any deviation from this ideal, non-delaying case will, if not compensated, severly degrade the performance of the system. One of the major concerns of CT modulators is therefore the importance of accounting for the inevitable excess loop delay(ELD) and accurately compensate for it by allocating enough time for this operation. Adjusting the loop filter coefficients and adding an additional feedback DAC, is a common and often required modification/alteration to acquire the desired DT-CT equivalence. By developing a high-level environment closely related to the final circuit-level implementation, the transition from specification to implementation can be made more automated and transparent. Designing a $\Delta\Sigma$ modulator is an iterative and time-consuming process, making the need for closely linked design stages all the more important. An accurate high–level representation of the system will help to evaluate and predict the actual behavior of each block comprising the modulator, and minimize any unforeseen effects influencing the performance of the final system. By also considering the occuring location of the nonideal effects and quantify their impact on the overall system, a comprehensive specification of individual parts can be obtained. As an effect, tailoring and optimization of each component in detail can be achieved.

The efforts made will create a solid platform for observation and give useful insight about the nature of $\Delta\Sigma$ converters. This project will involve getting experience in high-level modelling and system analysis. Current, highly popular technologies utilizing $\Delta\Sigma$ modulators include among others; GSM, Bluetooth, UMTS, DVB, WLAN, EDGE and CDMA, with WLAN and UMTS needing the highest bandwidth in tens of MHz.

1.3 Background literature and state-of-the-art

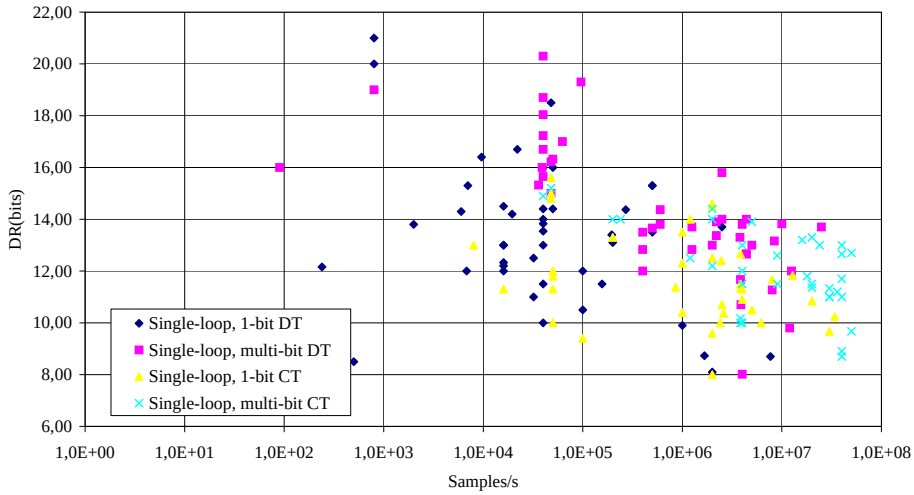
The theoretical background for this work are based on a couple of main sources. The majority of books used are devoted especially to $\Delta\Sigma$ modulators and include G. Temes and R. Schreier's *Understanding Delta-Sigma Data Converters*[3], *Continuous-Time Sigma-Delta A/D Conversion*[2] by M. Ortmanns and F. Gerfers, and J. A. Cherry and W. M. Snelgrove's *Continuous-time Delta-Sigma Modulators for High-speed A/D Conversion*[6]. Temes and Schreier's extensive work covers the most important subjects and are geared toward design and implementation, although quite limited on the CT part. It also includes real examples and challenges faced with the many architectural dilemmas in $\Delta\Sigma$ design. Ortmanns and Gerfers novel book tries to summerize the most important aspects in CT$\Delta\Sigma$ design and create an overview of issues arising when using CT filters. This book is heavily based on results from existing literature, with a comprehensive and

exceptional reference list(extremely useful), and it tries to present the essence of what the published literature have presented up to 2006. A more thorough and elaborate book is Cherry and Snelgrove's, comprising of extensive CT$\Delta\Sigma$ synthesis as well as detailed theory and background. It features detailed design procedures and solutions for crucial elements, and is therefore a highly cited book by researchers.

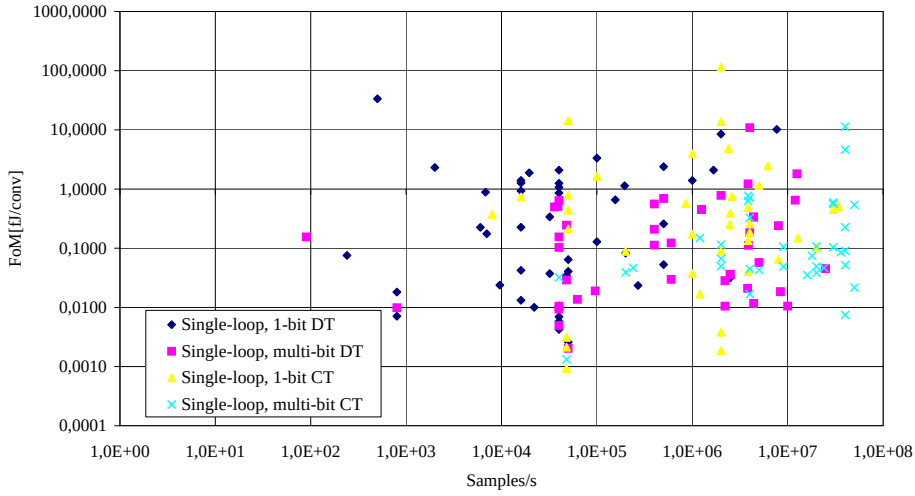
Other important sources include the International Solid-State Circuits Conference(ISSCC) proceedings representing the state of the art research made in data conversion technology. It depicts the future trends of the market and the interests in focus. Recently the converter efficiency has become a focus of innovation, with emphasis on lower power, cost and integration on systems-on-chip(SoC)[7, 8]. Also, from the conference in 2009, oversampling converters showed a distinct trend towards continuous-time implementations[9], and a recent survey of state-of-the-art $\Delta\Sigma$ modulators conclude with that especially applications targeting wideband and/or low power, use more and more continuous-time circuits[10]. The survey also found that most $\Delta\Sigma$ converters employed multi-bit quantization and signals with a $10-40$ MHz bandwidth was handled by 11-13 bits resolution. CMOS $0.18\mu m$ 1.8 V process is the most common technology employed.

Resolution in bits(DR) and energy per conversion step(FoM) versus samples/s(i.e. Nyquist rate $\equiv 2f_B$) for discrete and continuous-time, both single and multi-bit single-loop $\Delta\Sigma$ converters, are depicted in figure 1. The DR plot shows clearly that multi-bit CT$\Delta\Sigma$ dominates the high bandwidth(>10MS/s) range while DT$\Delta\Sigma$ occupy most of the high resolution(>14 bits), suggesting that for a wideband application using $10-14$ bits, a multi-bit continuous-time implementation is most suitable. The thermal figure of merit[2] is used as an efficiency metric to compare different ADCs and where lower value is better. CT implementations are by far superior in terms of efficiency at high bandwidths as demonstrated in the FoM plot.

[2] $FoM = \frac{P}{2^{2 \cdot ENOB} \cdot 2f_B} \left[\frac{J}{conv}\right]$



(a) Dynamic range in bits versus samples/s



(b) Thermal figure-of-merit in fJ/conv versus samples/s

Figure 1: State-of-the-art $\Delta\Sigma$ performance(2011)[10]

2 ΔΣ ADC fundamentals

Despite its introduction in 1962 by Inose, Yasuda and Marakami[11], ΔΣ modulation was not truly acknowledged until the 1980s when implementation techniques for integrated circuits and filters was developed, and enabled the transition from theory to integrated circuit implementation. From implementation methodology by Candy[12] and a proper stability analysis by Lee et. al. [13], ΔΣ modulation increasingly became a popular method for data conversion. The main block in ΔΣ converters is the modulator that exploits oversampling incorporated with noise-shaping filters to achieve a very high resolution. The typical ΔΣ ADC buildup is shown in figure 2 and consists of four main blocks; an AAF, a S/H circuit, a ΔΣ modulator and a decimator part.

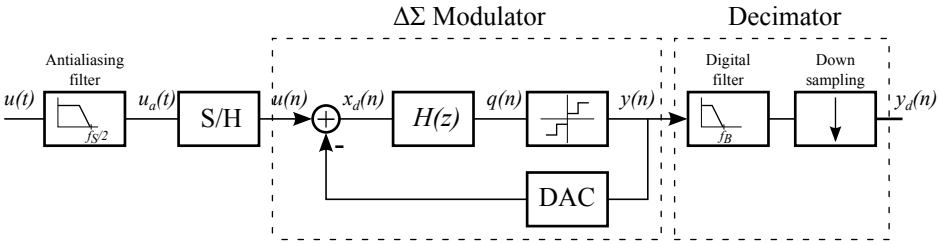


Figure 2: Traditional DT ΔΣ ADC block diagram[2]

The operation of the AAF is to remove spectral components over $\frac{f_S}{2}$ from the input signal, thus band-limiting the signal and avoiding that the S/H operation folds higher frequency components into the band of interest[1]. The actual A/D conversion is done by the ΔΣ modulator consisting of a filter, here $H(z)$, followed by an internal quantizer and feedback DAC. Quantization is normally done with a low resolution quantizer, up to 6 bits reported[14], and introduces quantization errors that subsequently get shaped out of band by the loop filter. The modulator puts out a digital pulse train $y(n)$ representing the analog input $u(t)$, in other words it modulates the input signal. Under ideal circumstances, the average of this pulse train represents the average of the input[3, Ch. 2.2]. The last part, the decimator, low-pass filters and performs down-sampling, eliminating out of band noise above the bandwidth f_B, and providing a Nyquist output rate with bit width corresponding to the ADC's resolution.

2.1 Oversampling

There are two main types of converter categories; namely Nyquist converters and oversampled converters. The design difference between the two categories can be

thought of as using an input occupying a large portion of the available bandwidth, Nyquist, or using an input occupying a small part, oversampled.

This difference leads to oversampled converters achievable of a large anti-aliasing transition region Δf_R and the total quantization noise only taking up a small part of the signal band. In other words, by oversampling the quantization noise is spread out over a wider frequency range and relaxes anti-aliasing filter requirements[15].

Using this property of oversampled converters, digital circuitry, the filter in figure 2, can be used to remove a large part of the quantization noise that is outside the band of interest. Ideally, the quantization noise can be reduced by a factor equal to $\frac{f_S}{2f_B}$, called the oversampling ratio(OSR), where f_S is the sampling frequency and f_B is the input signal bandwidth. For each doubling in OSR, the Signal-to-Quantization-Noise(SQNR) is improved by approximately 3dB/.5bit. The difference in performance considering only quantization noise becomes apparent in the two maximum achievable SQNRs for an ideal B_Q-bits quantizer, (1) and (2);

$$SQNR_{Nyquist} = 6.02B_Q + 1.76 \quad (1)$$

$$SQNR_{Oversampled} = 6.02B_Q + 10log_{10}(OSR) + 1.76. \quad (2)$$

In [16, Sec. 2.2] it is argued and shown that a minimum OSR of ≈ 4 is needed to maintain the profit of the noise-shaping ΔΣ architectures in comparison to unshaped oversampling converters.

2.2 Noise shaping

The ΔΣ modulator consists of a loop filter along with an internal quantizer and DAC as briefly already discussed. Due to the quantizer and the memory of the loop filter, it is both a nonlinear and dynamic system and hence, a difficult system to analyze mathematically. To ease the mathematical analysis and gain a fundamental understanding of the system, a linearized model is preferable. By replacing the quantizer with its linear model, i.e. with gain k_q and quantization noise $e(n)$[2, Sec. 2.1.1], and assuming an ideal feedback DAC, the model in figure 3 is obtained.

With the introduction of the feedback path, different transfer functions can be designed for the signal and the destructive quantization noise, ideally making them spectrally distinct. The signal and noise transfer function are abbreviated to STF and NTF, optimally conserving the signal and attenuating the noise inband. Using the linear model in 3, the following relation can be set

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \quad (3)$$

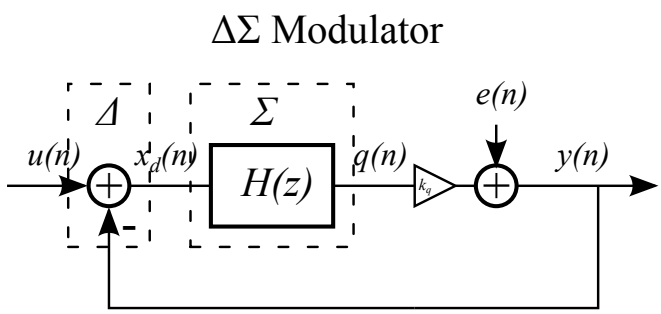


Figure 3: Linear $\Delta\Sigma$ model with the quantizer represented by quantization noise $e(n)$ and gain k_q

where

$$STF(z) = \frac{1}{\frac{1}{k_q H(z)} + 1}, \; NTF(z) = \frac{1}{1 + k_q H(z)}. \tag{4}$$

Here $U(z)$, $Y(z)$ and $E(z)$ of the input, output and quantization noise is represented using the DT $\mathcal{Z}$-domain. Clearly, to accomplish noise-shaping characteristics, the loop filter $H(z)$ needs to have a large gain inband, while outside it may decrease. By making the filter a simple 1^{st} order integrator,

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}, \tag{5}$$

the 1^{st} order $\Delta\Sigma$ modulator is created. Evaluating 4 and 5 with respect to low frequencies yield

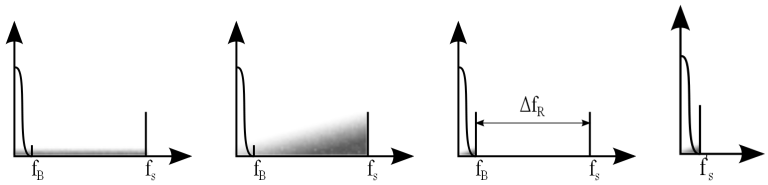
$$STF_1(z) = z^{-1}, \; NTF_1(z) \approx \frac{1 - z^{-1}}{k_q}, \tag{6}$$

realizing the NTF as a high-pass filter and demonstrates how an integrating filter and a feedback path generates the unique noise-shaping nature of $\Delta\Sigma$ modulators. The output spectrums from the oversampling, noise-shaping and decimator block are shown in figure 4 for clarity.

By designing a higher order loop filter, the portion of inband noise can be further reduced as will be discussed in the next section.

2.2.1 Higher order modulation

One of the main techniques for improved performance is to increase the order of the modulator. The NTF of an ideal N^{th} order $\Delta\Sigma$ modulator, ignoring k_q, is simply



(a) Oversampled **(b)** Noise shaped **(c)** Digital cutoff **(d)** Output

Figure 4: Spectrums as the signal goes through the ΔΣ ADC depicted in figure 2. **(4a)** shows how the oversampling disperse the noise, **(4b)** the noise-shaping pushing noise out of the band, **(4c)** the cut off filter removing spectral components above f_B and **(4d)** the output finally limited to $f_S^{'}$

$$NTF_{N,ideal}(z) = (NTF_1(z))^N = (1 - z^{-1})^N. \tag{7}$$

In figure 5, the NTFs for the 1^{st} to 5^{th} order ideal modulator and their frequency response have been plotted. The slope at low frequencies are 20 dB/decade/order showing the power of higher order noise-shaping.

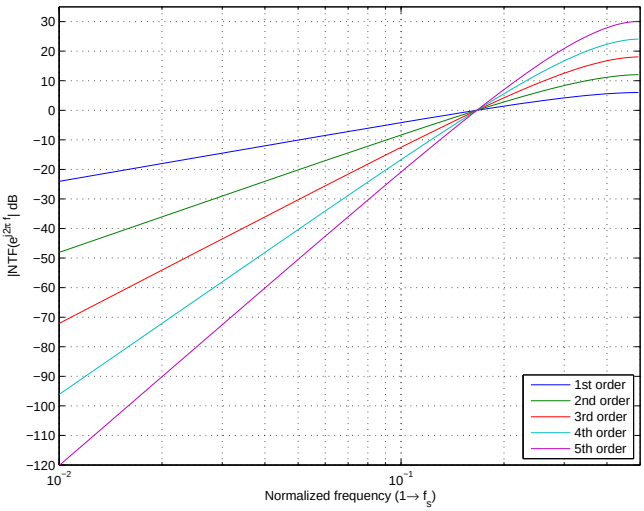


Figure 5: NTFs$((1 - z^{-1})^N)$ for a generic 1^{st} to 5^{th} order ΔΣ modulator, no resonator poles for lower inband noise. Notice that while higher order attenuates inband quantization noise substantially as the order increase, they also amplify the out of band noise.

However, one should notice the gain at $\frac{f_S}{2}$, the out-of-band gain(OBG). The higher order NTF magnitudes are increasing 6 dB/order at $f_S/2$ and need to be limited to ensure stability. High OBG may cause overloading of the quantizer and consequently make an unusable modulator. The basic principle to increase stability is to reduce the loop gain, commonly done by proper internal stage scaling. Stability is guaranteed if the internal modulator states or equivalently the integrator outputs are bounded over time.

To ensure stabile operation the input level needs to be less or equal to the fullscale of the first feedback DAC. In higher-order single-bit $\Delta\Sigma$ modulators this input range is a few dB below the DACs fullscale[3, Ch. 4.2]. This stable range is mainly determined by the NTF and the number of quantizer bits. A stability condition for single-bit modulators widely in use is the Lee's Criterion[13]

$$|NTF_{MAX}| \leq 1.5, \tag{8}$$

where $|NTF_{MAX}|$ is the maximum magnitude over all frequencies. A NTF with the OBG set at 1.5 suffers significantly in terms of inband noise suppression compared to the ideal NTF. Limited, single-bit NTFs for the 1^{st} to 5^{th} order $\Delta\Sigma$ modulator can be seen in figure 6. Also as order increase, the performance starts to saturate and the desired performance boost due to higher order filters, loses its leverage. However as will be stated in section 2.2.3, the introduction of multi-bit quantization enable higher order systems to be stable even with a large OBG.

2.2.2 Zero optimization for increased resolution

The NTF functions plotted in figure 5, $(1-z^{-1})^N$, with zeros at $z=1$ and poles at $z=0$ could gain substantial improvement by performing zero optimization. By minimizing the noise power with respect to all the zeros, optimal values can be found. Spreading the zeros results in decreased inband noise[3, Ch. 4.3]. Architectural changes for altering these fixed zero locations involve the introduction of resonators into the loop filter.

A brief overview of achievable SQNR improvement by minimizing the inband noise is listed in table 1. The optimized zero locations have been derived with the assumption of white quantization noise and the influence of the NTF poles to be minimal. An increase in SQNR of 18 dB of a 5^{th} order system is quite significant and results in the use of zero optimization a necessity for maximum resolution.

However, the resonator feedback coefficients quickly decrease with OSR^{-2}, resulting in placing them accurately within the smaller signal band of higher OSR architectures difficult. Although with this limitation, most recent designs commonly implement resonators just for the pure potential enhancement[2, Sec. 2.7.3].

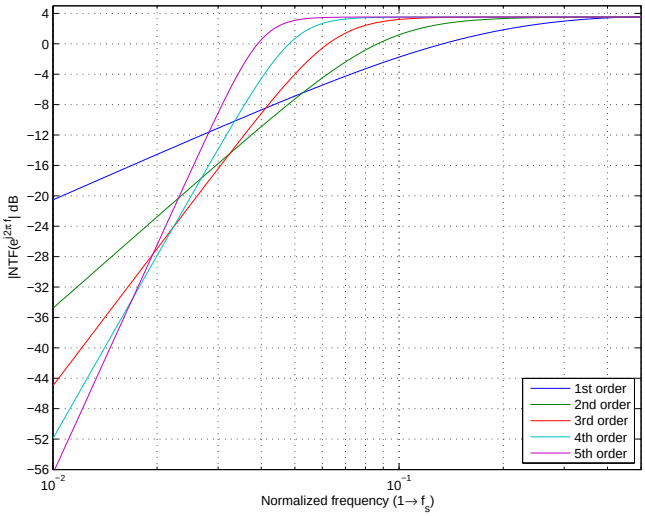


Figure 6: Stable NTFs with an OBG of 1.5(3.52 dB) for a 1^{st} to 5^{th} order modulator. Notice the lower inband suppression of the limited NTFs compared to the ideal NTFs

Order	*Normalized zero locations*	*SQNR improvement*
3	$0, \pm\sqrt{\frac{3}{5}}$	8 dB
4	$\pm\sqrt{\frac{3}{7} \pm \sqrt{(\frac{3}{7})^2 - \frac{3}{35}}}$	13 dB
5	$0, \pm\sqrt{\frac{5}{9} \pm \sqrt{(\frac{5}{9})^2 - \frac{5}{21}}}$	18 dB

Table 1: Zero optimization improvements and their locations [3, Table 4.1]

2.2.3 Single and multi-bit internal quantization

Each additional bit added to a quantizer gives ideally 6 dB increase in SQNR as a consequence of the lower quantization noise. Further, introducing multi-bit quantization also has an influence of making higher order modulators more stable[2, Sec. 2.6.2], and consequently capable of handling more aggressive noise-shaping functions and higher input swings[16]. However, the cost of multi-bit implementations is that the internal DACs linearity, it is inherently linear in single-bit implementations, needs to be at least as good as the overall modulator[17]. The reason for this is that errors induced by variations in the feedback levels are without suppression, illustrated in the ΔΣ ADC block diagram, added to the

input as distortion. This high linearity requirement may require making use of complex, area and power consuming correction techniques. Different published techniques involve analog or digital calibration, dual-quantization or dynamic element matching(DEM). While background calibration require complex circuitry and dual-quantization lack the full improvement of multi-bit structures, DEM techniques utilizing methods such as the noise-shaping data weighted averaging(DWA), fully exploit the enhancement of multi-bit along with reduced linearity requirements and hardware complexity[Sec. 2.7][16]

2.3 Continuous-time ΔΣ modulation and its advantages

In the CT based ΔΣ ADC, illustrated in figure 7, a couple of important differences appear. Most noticeable is the location of the sampling operation which is now located inside the loop, shown as a quantizer clocked at f_S. As sampling is executed inside the loop, the AAF is slightly shaded, illustrating that it can be significantly reduced or even removed. The last major difference is the loop filter now consisting of CT filters $H(s)$ instead of DT filters $H(z)$.

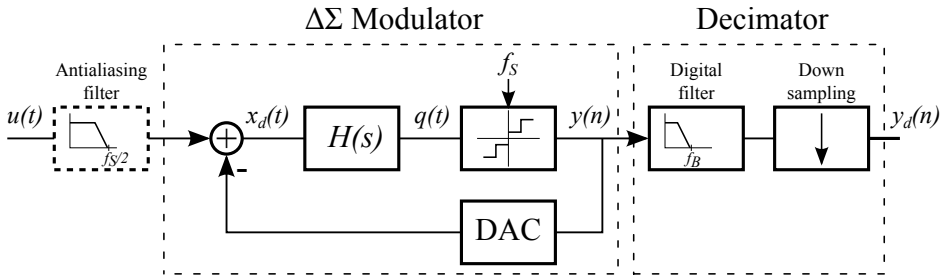


Figure 7: CT ΔΣ ADC block diagram[2]

The most commonly claimed advantage of CT based ΔΣ modulators is the postponement of the sampling operation. Instead of errors introduced by this operation directly adding to the signal as in the DT case, these errors are subject to the same amount of noise-shaping as the quantization noise. In high-bandwidth applications, the DT S/H block needs to operate fast and accurate making DTΔΣ design difficult. The implicit anti-aliasing filtering caused by $H(s)$ preceding sampling, gives the signal transfer function a sinc-like characteristic, is also one of most decisive property of CT implementations, especially in high-speed or low OSR architectures.

By employing the same analogy as mentioned in the introduction, CT being equivalent to a DT with a preceding CT filter, the NTF of both CT and DT will remain the same. To evaluated the desirable anti-aliasing effect of CTΔΣ

modulators seen in the spectral response of the STF, the STF can be considered a combination of CT and DT transfer functions[18]. This is due to the fact that the input signal is continuous while the output is discrete. The amount of alias attenuation of higher order CT modulators is at minimum as good as the attenuation of quantization noise since sampling and quantization now occurs at the same location[3, Ch. 6.6.1]. A list of advantages the continuous and discrete filters possess is listed in table 2. Many of the CT benefits are obviously

CT filter	*DT filter*
Implicit AAF	Insensitive to clock jitter
Noise shaped S/H error	Insensitive to ELD
High sampling frequencies	Insensitive to DAC waveform
Reduced Opamp speed requirements	Accurate transfer functions
Reduced impact from supply and ground noise	SC integrator highly linear
Less glitch and switching noise	Only capacitive loads
Low circuit-level simulation time	Low high-level simulation time

Table 2: Advantages obtained in favor of using DT and CT filters[2, Table 3.1]

appealing power saving characteristics, but proper design is needed to counter its weaknesses later discussed in section 2.5.

2.3.1 Loop filter structures and characteristics

The general model of the ΔΣ converter is illustrated in figure 8

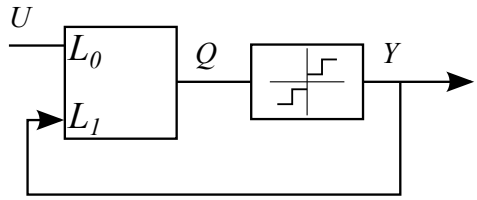


Figure 8: General ΔΣ model, L_0 and L_1 defined as the signal filter and feedback filter respectively

By doing a quick analysis and applying the linear model of the quantizer(k_q set to unity), results in

$$Q = L_0U + L_1Y \tag{9}$$

$$Y = Q + E \tag{10}$$

$$\Rightarrow Y = \frac{L_0}{1-L_1}U + \frac{1}{1-L_1}E. \tag{11}$$

Comparing this result with the previously defined NTF and STF in equation 3 gives the relationship between the loop filter and the signal- and noise transfer function

$$NTF = \frac{1}{1 - L_1},\ STF = \frac{L_0}{1 - L_1} \tag{12}$$

$$\Rightarrow L_1 = 1 - \frac{1}{NTF},\ L_0 = \frac{STF}{NTF}. \tag{13}$$

Hence, in order to achieve the same characteristics for the NTF and the STF as before, it becomes evident that L_1 must be large in the range $[0, f_B]$ to decrease the NTF and that L_0 must be equally large in the same range to obtain STF unity. Also notice that denominator of the two functions is the same, suggesting that L_1 and L_0 have the same poles (equiv. to NTF zeros). However, in general L_1 and L_0 have different zeros. Using relation (13) considering the STF a combination of CT and DT filters, leads to the definition of a 1^{st} order CTΔΣ STF

$$STF_{1CT} = L_0(s)NTF_1(z) \tag{14}$$

with

$$L_0(s) = I(s) = \frac{1}{s}, NTF_1(z) = (1 - z^{-1}). \tag{15}$$

In figure 9 the generic 1^{st} to 5^{th} order CTΔΣ modulator STFs and their frequency response have been plotted showing the desirable alias attenuation increasing with higher order.

There are two main higher order loop filter structures, namely chain of integrators(CI) with distributed feedback(FB) or CI with weighted feedforward(FF) summation, abbreviated CIFB and CIFF. Also by including local feedback loops forming a resonator from two integrators, the desired zero optimization can be obtained. In odd order modulators, the input stage is usually the normal integrator with subsequent resonators to minimize the input-referred noise from following stages[3, Sec. 4.4].

In figure 10, two 3^{rd} order CIFB and CIFF structures are illustrated, both including resonators to optimize the NTF zeros. Also an additional FB DAC a_0 used for ELD compensation is included. The feedback filter for the two structures, ignoring the resonators and the ELD compensation for simplicity, yield

$$L_{1,FB} = -\underbrace{a_1c_1c_2c_3I(s)^3}_{3^{rd}\,order\,path} - \underbrace{a_2c_2c_3I(s)^2}_{2^{nd}\,order\,path} - \underbrace{a_3c_3I(s)}_{1^{st}\,order\,path} \tag{16}$$

$$L_{1,FF} = -a_3c_1c_2c_3I(s)^3 - a_2c_1c_2I(s)^2 - a_1c_1I(s). \tag{17}$$

As can be seen from (16) and (17), both L_1's are of similar structure and thus yield the same degree of inband noise. Consider the NTFs at low frequencies

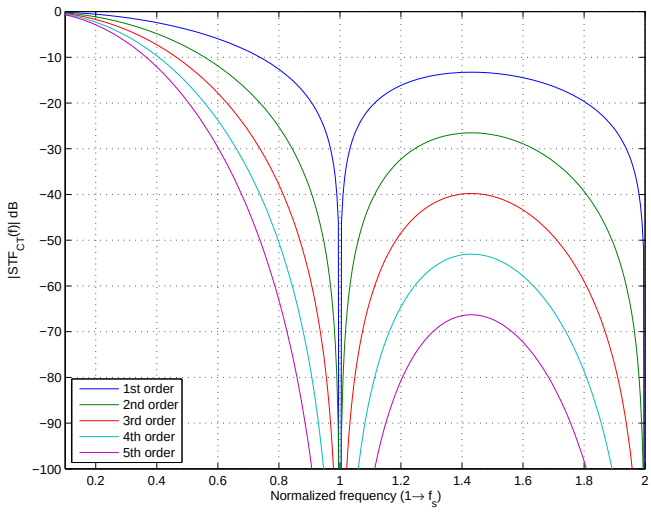


Figure 9: STF_{CT}, $\left(\frac{(1-z^{-1})}{s}\right)^N$, for a generic 1^{st} to 5^{th} order $\Delta\Sigma$ system, no resonator poles for lower inband noise. Notice that higher order(larger loop-gain) translates to higher anti-aliasing rejection

with $I(s) = \frac{1}{s}$ result in the observation that the outermost path, the 3^{rd} order path, dominates the noise-shaping characteristics. The signal filter for the two structures are

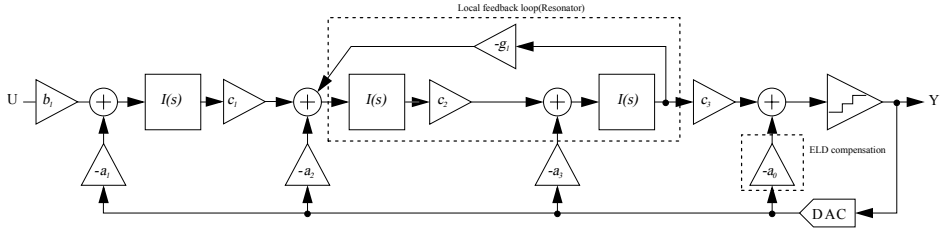
$$L_{0,FB} = b_1 c_1 c_2 c_3 I(s)^3 \tag{18}$$

$$L_{0,FF} = b_1 c_2 c_3 a_3 I(s)^3 + b_1 c_2 a_2 I(s)^2 + b_1 a_1 I(s). \tag{19}$$

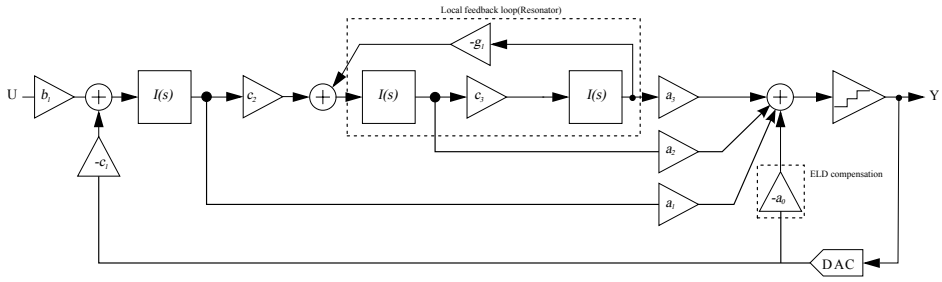
Due to the major difference in the signal filter of the two structures, the amount of anti-aliasing differ greatly when compared. FB systems have superior anti-aliasing suppression in comparison to FF structures, as evident from the different STF_{CT}'s due to L_0 each possess.

A drawback of the FB filter implementation is the large integrator output swings. This will increase OpAmp requirements and require, to avoid overload, internal coefficients c_i that are quite small. As will be seen in later sections, small coefficients in CT$\Delta\Sigma$ lead to integrators with low transconductance values, which again lead to a higher noise contribution.

In contrast, the feedforward branches in the CIFF structure result in a low amount of signal present at the outputs, thus relaxing the requirements of scaling and swing while lowering the power consumption. However, this desirable benefit



(a) Feedback



(b) Feedforward

Figure 10: 3rd order loop filter realization structures with local feedback loops for additional inband noise suppression and ELD compensation DAC. Notice the FB/FF difference in coefficient definitions. Integrator transfer functions represented using the CT $\mathcal{S}$-domain, here all are equal $I(s)$

comes at the cost of high frequency peaking causing possible overload in the case of input signals close to that frequency. Another advantage that lowers the power dissipation is the fact that it only uses one internal FB DAC in comparison to the CIFB structure's N DACs. In a 5th order setup, having 4 less DACs can result in quite substantial power savings. The NTF without and with the resonator for optimal zero placement for the CIFB structure is given below, ignoring ELD a_0,

$$NTF_{3FB} = \frac{s^3}{s^3 + \underbrace{a_3c_3s^2}_{1^{st}\,order\,path} + \underbrace{c_2c_3a_2s}_{2^{nd}\,order\,path} + \underbrace{a_1c_1c_2c_3}_{3^{rd}\,order\,path}} \tag{20}$$

$$NTF_{3FB,Opt} = \frac{s^3 + c_2g_1s}{s^3 + a_3c_3s^2 + (c_2g_1 + a_2c_2c_3)s + a_1c_1c_2c_3} \tag{21}$$

and plotted with values obtain from synthesis in figure 11. The inband noise difference is the theoretical 8 dB for a 3rd order.

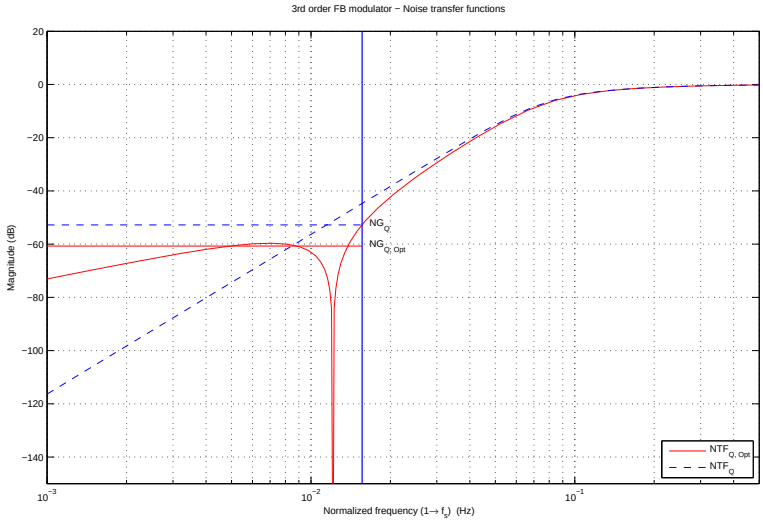


Figure 11: NTF magnitudes for a 3rd order FB modulator with and without zero optimization by resonator. $OSR = 32$, $f_B = \frac{1}{2OSR}$ represented by the vertical line. The horizontal lines are the noise gain located at -60.73 and -52.76 dB for the optimized and non-optimized respectively, separated by the theoretical 8 dB

2.3.2 Filter implementations and comparisons

There are mainly three approaches of integrator implementations standing out in the design of the CT loop filter; operational amplifier(OpAmp) based active RC-filters, operational transconductance amplifier(OTA) based gmC-filters or LC-resonator filters. Integrators based on an OTA and a capacitor, called a gmC-integrator, exhibit advantages such as tunability and low current consumption in addition to small excess phase shifts. The disadvantages of the gmC-integrator is that the dynamic range requirements of the OTA's limits is usability in low-voltage operations. This can somewhat be compensated with the use an extra amplifier, making it an active gmC-integrator, but at the cost of additional power consumption[2, Section 3.7.1]. The current-mode counterpart to the gmC, and its special case, is the relative new approach of log-domain integrators. Low-power consumption at low voltages have motivated the research into the development of these types of filters, but at the cost of limited bandwidth in CMOS of only a few MHz due to the demand of large $\frac{W}{L}$ ratios[19].

Another common integrator is the active RC-integrator known for its linearity,

parasitic insensitivity and low power consumption, all achieved with a relatively simple design. Many of the integrator limitations depends on the accuracy and characteristics of its external components. A summary of the different integrators and their various properties are listed in table 3. If low-power at low voltages

Property	*gmC*	*Active-gmC*	*Log-domain*	*Active-RC*
Frequency Range	Highest	High	Low	High
Tunability	High	High	Highest	Low
Insensitive to mismatch	High	Medium	Low	Low
Linearity	Low	High	Medium	Highest
Dynamic range	Medium	Low	Medium	High
Power	Low	High	Lowest	Medium
Low voltage applicability	Low	Medium	Highest	High

Table 3: Comparison of different filter implementation approaches[2, Table 3.7]. Properties are rated low(est), medium and high(est)

are desired and the frequency range is limited to a few MHz, the obvious choice is log-domain integrator. If high linearity together with a large frequency range is demanded, the active-RC integrator is the preferred choice. Lastly, if linearity is not of main concern, but low power is, the gmC-integrator make for the most suitable alternative. Due to location-dependent properties in ΔΣ ADCs, published low-pass ΔΣ modulators show a combination of these integrators is often utilized for reaching optimal efficiency[2, Table 3.8]. In this project an active-RC integrator was investigated.

2.3.3 Operational considerations of an active RC-integrator

Figure 12 shows a fully differential active RC-integrator with the OpAmp, input resistors R and integration capacitors C. Ideally, the transfer function is given by

$$Int(s) = \frac{1}{sRC} = k_i \frac{f_S}{s}, \tag{22}$$

where f_S is the sampling frequency and k_i the associated scaling coefficient. Important characteristics of the active RC-integrator include the amplifiers DC gain A_0, gain bandwidth(GBW), noise and distortion. As will be demonstrated later, if this integrator is used in the first stage, insufficiencies in either of these properties will add directly to the signal and affect the overall performance. In the presence of finite DC gain, known as integrator leakage(no virtual ground

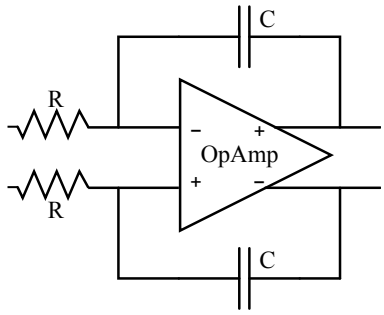


Figure 12: Schematic of a differential active RC-integrator

condition), the integrator transfer function adjusts to[20]

$$Int_{A_0}(s) = \frac{A_0}{sRC(1+A_0)+1}. \tag{23}$$

The effect of finite DC gain is the alteration of the placement/location of the NTF zeros, resulting in increased inband noise. For a 3$^{\text{rd}}$ order system, a maximum tolarable SNR degradation of 1 dB at an OSR of 32, results in a minimum DC gain of approximately 40 dB using results derived in [20]. According to [21], if the DC gain is equal to or larger than the OSR, the SNR only drops 1 dB. Thus, a rule of thumb for single-loop modulators maintaining the ideal noise suppression is set to be $A_0 \approx OSR$.

Non-dominant integrator poles introduced by finite GBW is not considered a major concern in CT circuitry, but affects the poles in a way that degrades the modulator stability. With finite GBW the amplifier transfer function changes to

$$A_0(s) = \frac{A_0}{1+\frac{s}{p_{dom}}}, \tag{24}$$

causing the integrator transfer function for integrator i with $A_0 \approx OSR$ to approximate to

$$Int_{GBW}(s) \approx \frac{1}{sRC} \frac{\frac{GBW}{GBW+\frac{1}{R_iC_i}}}{\frac{s}{GBW+\frac{1}{R_iC_i}}+1} \tag{25}$$

giving rise to equivalent effects similar to that of an integrator gain error and the aforementioned non-dominant pole. Degrading of performance along with stability in zero optimized structures can be seen[2, Sec. 5.4]. The published literature throughout shows that the GBW requirements in CT implementations is much lower compared to their DT counterparts. Recent work based on advanced models in [22] shows a minimal degradation of performance for higher order system

with a GBW of around f_s and even below. However as [23] points out, such results are dependent on a high OSR(>16) for maintaining linear operation of inband signals and having only mildly aggressive noise shaping characteristics. In full implementations, e.q. [24], they chose a GBW of $2f_s$ to avoid any issues with parasitic capacitances, process and temperature variations. Also, internal stages without processing high frequency feedback DAC signals, applicable to FF structures, can have relaxed GBW requirements[23]. The non-dominant pole introduced, can be modelled as a feedback delay and gain error, and be compensated for.

Infront of the quantizer a summation circuit is employed adding the loop filter output(including FF branches in the CIFF structure) and the direct feedback DAC output together. The speed of this adder's OpAmp, if active, needs to especially high for this operation, resulting in a difficult design[23, Sec. 6.3]. The most common OpAmp architectures include the folded-cascode and the two-stage OpAmp. In CT design, the two-stage is more efficient in terms of DC gain than folded-cascode when considering the resistive loads[23]. Figure 13 shows

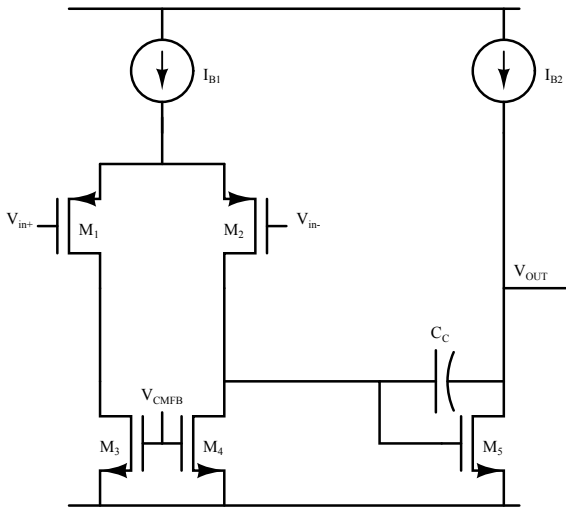


Figure 13: Half circuit of a two-stage fully differential operational amplifier

the basic buildup of a two-stage OpAmp consisting of an input differential pair, active loads and their respective biasing currents.

2.4 Discrete- to continuous-time transformation

Because of the well established techniques for DT implementations, designing a CT loop filter equivalent to a DT will benefit from tools and methods developed in the past. Also, since these methods are robust and well integrated with software, they will significantly speed up the design and simulation procedure of a CT design. Hence, it is useful and highly advisable to start CT design with a DT synthesis and then perform a transformation[25].

The most common approaches are the modified Z-transform and the impulse-invariant transform. R. Schreier have also introduced time-domain approach based on state-space description evaluating matrices[26]. The basic principle and results are the same; matching the DT's impulse response with the CT's sampled response, making the NTFs equivalent.

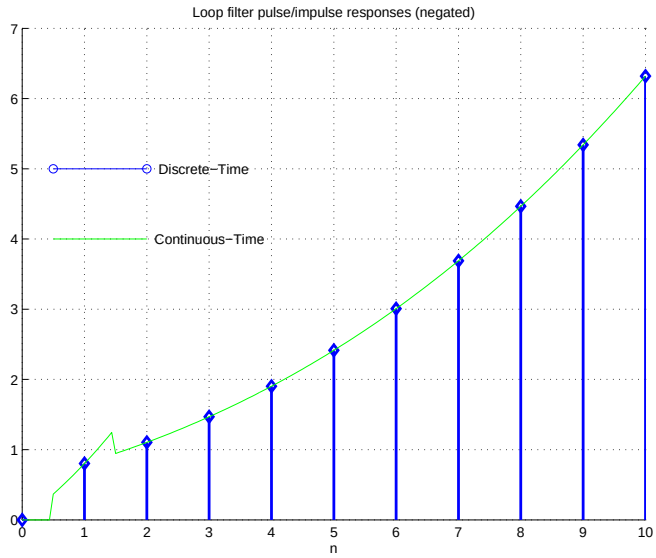


Figure 14: Example of loop filter pulse and impulse response for CT and DT with ELD(tdac=[0.5 1.5]). Notice the CT wave with a delay of $0.5T_S$

2.4.1 State-space analysis

For the two structures, CIFB and CIFF, a state-space notation can be applied and describe the systems accordingly

$$ABCD = \begin{bmatrix} A & B \\ C & D \end{bmatrix}$$

$$x(n+1) = Ax(n) + B\begin{bmatrix} u(n) \\ y(n) \end{bmatrix} \tag{26}$$

$$q(n) = Cx(n) + D\begin{bmatrix} u(n) \\ y(n) \end{bmatrix} \tag{27}$$

where $x(n+1)$ corresponds to the internal states of the structure, $q(n)$ the loop filters output, $u(n)$ the systems input and $y(n)$ the output. A, B, C and D matrices contain the systems coefficients. For instance in the 5^{th} order FB modulator, the matrices become

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ c_1 & 0 & -g_1 & 0 & 0 \\ 0 & c_2 & 0 & 0 & 0 \\ 0 & 0 & c_3 & 0 & -g_2 \\ 0 & 0 & 0 & c_4 & 0 \end{bmatrix} \qquad B = \begin{bmatrix} b_1 & -a_1 \\ \vdots & \vdots \\ 0 & -a_5 \end{bmatrix} \tag{28}$$

$$C = \begin{bmatrix} 0 & \cdots & c_5 \end{bmatrix} \qquad D = \begin{bmatrix} 0 & a_0 \end{bmatrix} \tag{29}$$

and where in general the different coefficients are

- a - FB/FF coefficients from/to the quantizer
- g - Resonator coefficients
- b - Feed-in coefficients from the modulator input to each integrator
- c - Integrator inter-stage coefficients, internal scaling

By using a state-space approach describing internal as well as external states of the modulator, restrictions and matching of internal states can also be obtained. For a general modulator with matrix A describing state interconnections and matrix $B = \begin{bmatrix} B_1 & B_2 \end{bmatrix}$ the inputs of the system(B_2 equal to the FB branches), the following set of equations can be defined for the continuous and discrete case[26, Sec. II c]:

$$x_c' = A_c x_c + B_c \begin{bmatrix} u_c \\ y_c \end{bmatrix} \tag{30}$$

$$x(n) = Ax(n-1) + B\begin{bmatrix} u(n-1) \\ y(n-1) \end{bmatrix} \tag{31}$$

Here, state x_c describes the continuous linear system and state x the discrete. Based on a non-return-to-zero(NRZ) DAC pulse and mathematical manipulations, to ensure that the two systems in (30) and (31) have identical samples, the following conditions must hold:

$$A_c = logA \tag{32}$$

$$B_{c2} = (A - I)^{-1} A_c B_2 \tag{33}$$

which establishes the possibility for discrete-to-continuous time transformation once the discrete A and B matrices are found.

2.5 Overview of CTΔΣ nonidealities

Non-idealities in CTΔΣ modulators can be characterized into two groups; errors that alter the signal- and noise transfer function by changing their poles and zeros, and errors that introduce noise and distortion[2, Sec. 3.8][17]. The three main building blocks of the CTΔΣ, the continuous-time loop filter, the internal quantizer and the feedback DAC, each have errors associated with them. A list of some key errors and their effect on the system is shown in table 4.

Block	*Effect*	*Influences*
Filter	Finite, nonlinear DC gain	Noise floor and distortion
	Finite GBW	Stability and noise floor
	1/f and thermal noise	Noise floor
ADC	Metastability and hysterisis	Input amplitude, noise floor and distortion
DAC	Delay, intersymbol interference and nonlinearity	Stability, input amplitude, noise and distortion
Clock	Jitter	Noise and signal skirt

Table 4: Block nonidealities applicable to CTΔΣ modulator and their impact on the system[2, Table 3.10]

2.5.1 Excess loop delay

The sensitivity to ELD in CT implementations arise from the DT-CT equivalence assuming the quantizer and the DAC operate instantaneously to provide feedback right after sampling the input. Ideally, the FB DAC output responds to the quantizers clock input, but in practice there exist a delay due to the switching

time of the transistors, known as the excess loop delay. The DT-CT transformation is done for a given DAC pulse and any deviation from this pulse, results in a mismatch between the intended and actual transfer function. This scaling mismatch yields increased noise inband and may reduce the maximum stable input of the system.

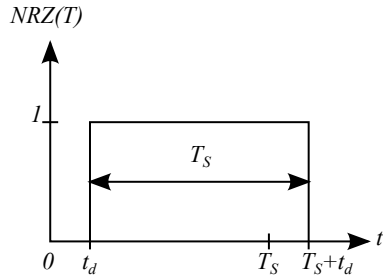


Figure 15: NRZ-DAC pulse with loop delay t_d

The non-return-to-zero(NRZ) pulse seen in figure 15 with delay t_d is the most critical case in which the pulse extends into the next sampling instant. In [2, 27] it is shown that this is equivalent to an increase in order, lowering maximum stable input and altering noise-shaping performance.

In order to deal with the inevitable excess loop delay, for high speed(low sampling periods) especially, it is essential to account for this delay either by choosing insensitive architectures or compensation techniques.

Classic ELD compensation is done using an additional feedback path directly to the quantizers input, as seen in figure 10, at the expense of an extra DAC. This method provides compensation of up to one whole clock cycle[28]. The modified NTF of the 3^{rd} FB system with ELD compensation a_0 coefficient is

$$NTF_{Opt,ELD} = \frac{s^3 + c_2 g_1 s}{(1+a_0)s^3 + a_3 c_3 s^2 + (c_2 g_1 + a_2 c_2 c_3 + a_0 c_2 g_1)s + a_1 c_1 c_2 c_3} \quad (34)$$

3 Method for optimization

In the ideal $\Delta\Sigma$ modulator only the quantization noise is contributing and is affected by both oversampling and the overall noise-shaping of the loop filter. However, in an implementation, also white or frequency dependent noise sources will appear. The typical $\Delta\Sigma$ modulator is designed making circuit noise the dominant contributer to the overall noise power[29]. By estimating the total input-referred noise, the ADC's resolution can be found. When dealing with

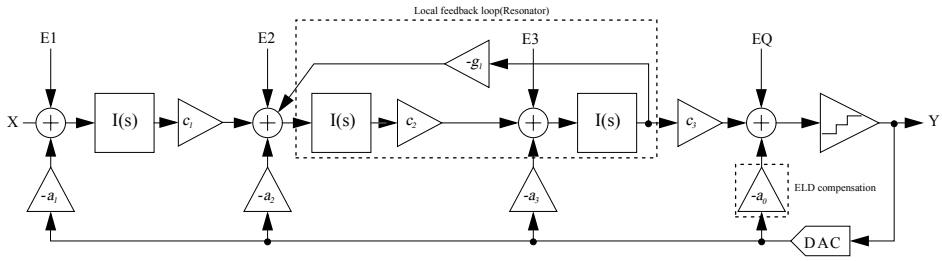


Figure 16: Transfer function definitions of error inputs applicable for a 3rd order FB modulator

nonidealities in $\Delta\Sigma$ design, the occuring location is of great importance. A block schematic including error signals induced at the integrators and the quantizer is depicted in figure 16. Using a 3^{rd} order feedback system as an illustrative example, but transferable to each structure investigated, $E1 - E3$ represents the input referred integrator noise while EQ is the quantization noise. By simple analysis, it becomes evident that the most critical and sensitive node is the input $E1$, with errors occuring here directly adds to the signal. This involves primarily the input referred noise and distortion of the 1^{st} stage aswell as any errors coming from the feedback DAC a_1. This leads to the input stage and DAC having the same requirements to accuracy and resolution as the entire modulator[2, p. 82]. Clearly, these will require a great amount of the overall power to meet the stringent noise demands, consequently leading to that substantial savings can be made in evaluating the system's nonidealities in detail. $E2 - E3$ are suppressed by their preceding integrator and EQ by the entire loop filter's high inband gain. A set of NTFs without a_0 for the system in figure 16 can be defined as equation set (35)–(38)

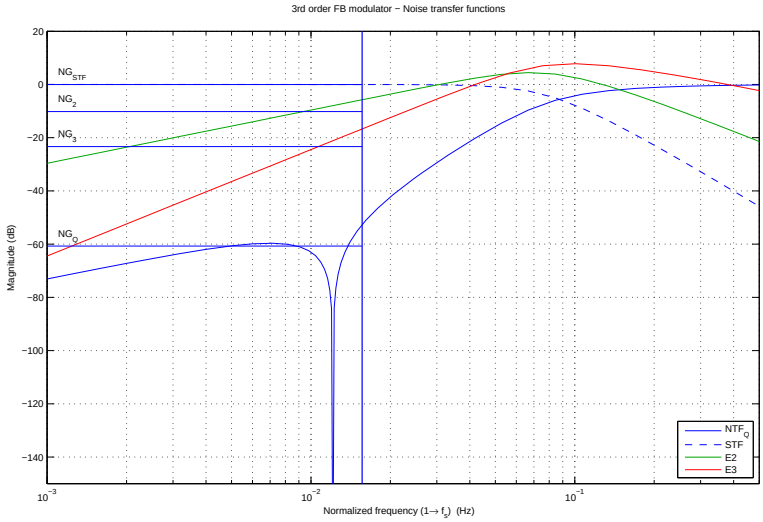


Figure 17: Plot of noise transfer function definitions for the 3rd order FB structure with values obtained in synthesis. NG_{STF}, NG_2, NG_3 and NG_Q are the noise gains for the three integrators and the quantizer respectively

$$NTF_{E1} \equiv STF = \frac{Y}{E1} = \frac{b_1 c_1 c_2 c_3}{s^3 + a_3 c_3 s^2 + (c_2 g_1 + a_2 c_2 c_3)s + a_1 c_1 c_2 c_3} \quad (35)$$

$$NTF_{E2} = \frac{Y}{E2} = \frac{c_1 c_2 c_3 s}{s^3 + a_3 c_3 s^2 + (c_2 g_1 + a_2 c_2 c_3)s + a_1 c_1 c_2 c_3} \quad (36)$$

$$NTF_{E3} = \frac{Y}{E3} = \frac{c_2 c_3 s^2}{s^3 + a_3 c_3 s^2 + (c_2 g_1 + a_2 c_2 c_3)s + a_1 c_1 c_2 c_3} \quad (37)$$

$$NTF_{EQ} \equiv NTF = \frac{Y}{EQ} = \frac{s^3 + c_2 g_1 s}{s^3 + a_3 c_3 s^2 + (c_2 g_1 + a_2 c_2 c_3)s + a_1 c_1 c_2 c_3} \quad (38)$$

The NTFs are plotted in figure 17 with synthesis data. Notice that only the noise sources defined after a resonator will get the desirable inband attenuation of the local feedback loops, e.q. only the quantization noise in the 3rd order system. The level of each transfer function can be adjusted by tuning the coefficients. Integrating their magnitudes over the inband portion of the spectrum, defined as the root-mean-square(RMS) gain, gives a set of noise gain(NG) figures. Evaluating the noise gains can lead to an optimal scaling of stages with an overall noise

budget in mind.

3.1 Noise sources and their contribution

In CMOS $\Delta\Sigma$ integrators noise comes from two main sources: *1/f* flicker and thermal noise[30, 31, 32, 33]. Flicker noise mainly stems from the integrator amplifiers. The total input referred noise at each node is the sum of the OpAmp, feedback DAC(here current DAC) and resistor noise contributions;

$$V_{ni}^2(f)_{tot} = V_{ni,OpAmp}^2(f) + V_{ni,IDAC}^2(f) + V_{ni,R}^2(f). \tag{39}$$

Considering the fully differential active RC-integrator and using a similar approach as in [2, Section 5.6.2] with the noise sources in figure 18, noise power spectral densities(PSDs) of each source can be derived and referred to the input

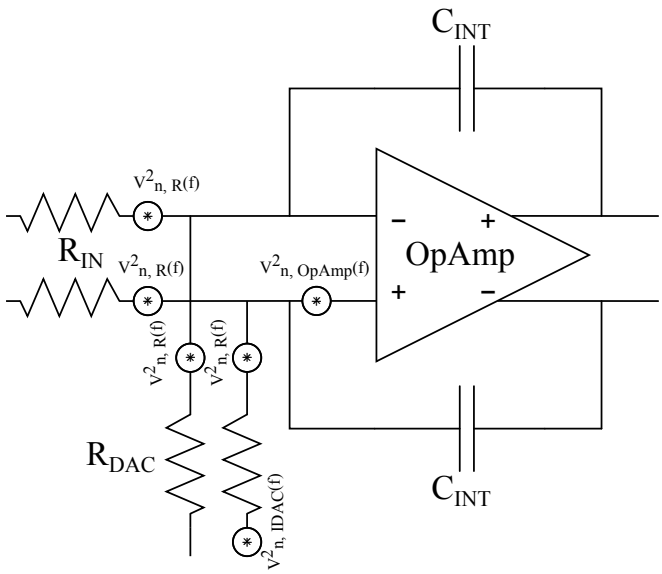


Figure 18: Schematic of the fully differential active RC-integrator used in noise analysis with OpAmp, resistors and DAC sources

From [3, Appendix C] the noise PSD on the differential pair's gates of a simple OpAmp(figure 13), assuming matched components and a high input transconductance g_{m_1}, is

$$V_{ni,OpAmp}^2(f) = \frac{16kT}{3g_{m_1}}\left(1 + \frac{g_{m_3}}{g_{m_1}}\right) \approx \frac{16kT}{3g_{m_1}}, \tag{40}$$

where k is the boltzmann constant and T the absolute temperature. $g_{m_1} = g_{m_2}$ is the transconductance of the input differential pair. Referring the contribution from the resistors R_{IN} and R_{DAC}, with noise PSDs of $V^2_{n,R}(f) = 4kTR$, to the input results in

$$V^2_{ni,R}(f) = 8kTR_{IN}\left(1 + \frac{R_{IN}}{R_{DAC}}\right). \tag{41}$$

In the case of a resonator stage with the additional local feedback path, another term of $\frac{R_{IN}}{R_{Resonator}}$ is added, but since $R_{Resonator}$ is usually much larger than the input resistor it is commonly neglected. The final source stems from the feedback DAC and assuming current based DAC, is derived in [23] here with assumptions $V_{DSat} = 0.9V$ and $V_{Ref} \approx 0.3V$;

$$V^2_{ni,DAC}(f) = \frac{32kT \cdot V_{Ref}R_{DAC}}{3V_{DSat}} \approx 32kT \cdot R_{DAC}. \tag{42}$$

By establishing these main contributers to noise, specific requirements of each component connected to the individual nodes can be developed.

3.2 NTF weighting

To evaluate the impact of the noise sources on the overall performance, the following set of equations are used. The impact is found by weighting the input-referred noise at each node with its corresponding NG

$$\underset{\text{for node x}}{P_{nx}} = \int_0^{f_B} \left|V^2_{ni}(f)_{tot}\right|_x df = V^2_{ni}(f)_{totx} \cdot f_B \tag{43}$$

$$\underset{\text{for node x}}{NG_x} = \int_0^{f_B} \left|NTF_{Ex}(f)\right|^2 df. \tag{44}$$

Here, $|NTF_{Ex}(f)|$ is the magnitude of the NTFs defined in the equation set (35)-(38) and NG the noise gain inband of each NTF. P_{nx} is the noise power inband. To determine the final contribution, P_{ntot}, equation (43) and (44) for each branch is multiplied and added accordingly

$$P_{ntot} = \sum_{x=1}^{x=N+1} P_{nx} \cdot NG_x, \tag{45}$$

where N is the order, $x = 1$ equivalent to the STF($E1$) and $x = N + 1$ the NTF(EQ). By determining the noise transfer function from each integrator input and calculating the inband noise attenuation, a noise budget can be set up, defining block requirements based on noise contributions.

3.2.1 Optimization flow

The overall procedure for optimizing circuit values to a given budget and find the minimum tolerable sizes with respect to noise is done with the following steps

- Determine all noise contributers at nodes defined in figure 16
  - Here the OpAmps, feedback current DACs and resistors are considered
- Derive noise PSDs for each source referred to the node's input
  - By deriving input-referred PSDs, the subsequent transfer function will be applicable to all sources connect to that node
- Evaluate the noise transfer function from each node to output
  - For the 3^{rd} order system, in addition to the STF and NTF, the transfer function from the input of the 2^{nd} and 3^{rd} integrator needs to be found
  - Integration of these functions inband $[0, f_B]$ to find the RMS noise gain
  - Effectively this translates to the internal scaling between the subsequent stages of the modulator
- Sum up all noise contributers at each node, integrate and multiply with the RMS noise gains found in the previous step
  - An overview of the each nodes contribution on the output is established and thus can be adjusted to the maximum tolerable limit
- Adjust R and C(amount of noise) until the desired performance is achieved

4 Modelling and specification

As depicted in the introduction, designing $\Delta\Sigma$ modulators involve extraordinary emphasis on synthesis and modelling compared to other ADCs. Discrete $\Delta\Sigma$ methology is well established and by readily available techniques for performing DT-CT transformation, is the traditional choice. However in CT design the essential dynamic range scaling that limit integrator outputs and finds practical circuit values, is usually advised to be performed also using a behavioral model since the DT synthesis only estimates state values at sampling instants[3].

Many of the $\Delta\Sigma$ architectural parameters are interconnected which makes the subsequent design stages highly dependent on each other. An intriguing goal of this work is to make a part of the process from specification and application to a finished implemented design as automated and correlated as possible. This will also increase the knowledge about performance critical components and help foresee the actual characteristics of a final design.

The goal of the synthesis process is to develop a list of suitable candidates and necessary NTF characteristics for the given high-level requirements. The next step of modelling is a step of both verification and tuning, but also a preparation of specifications towards the circuit-level implementation. Not considering crucial elements in the model may result in unanticipated devastating effects in the implementation. Description and methodology employed in this work is described in the following.

4.1 Design procedure

The basic procedure deployed in the work of this thesis is summarized in key elements below. A great effort went into making these steps as dependent and connected to each other as possible, resulting in easily observing how changes made in one step effected another.

- Synthesis with system specification
  - Flow and instructions based on [1]
  - Evaluate performance, stability, anti-aliasing and peaking
  - Resynthesize with ELD to find altered loop coefficients and compensation coefficient
- Derive noise figures and develop a noise budget
  - Uses the optimization summary flow depicted in 3.2.1
- Modelling the candidates developed from synthesis

  - Ideal modell for verification and scaling
  - Include nonidealities such as ELD, circuit noise and limited DC gain/GBW
  - Evaluate performance with respect to synthesis and budgetting results
- Obtaining the most suitable candidate based on the requirements furfilled, budgeting and modelling results

Some effects found in modelling changes parameters used in synthesis so an iterative process is needed

4.2 Synthesis and system specification

The synthesis for the $\Delta\Sigma$ modulator design was performed in MATLAB using the comprehensive $\Delta\Sigma$ Toolbox developed by R. Schreier[34]. Some of the features supported include NTF synthesis, realization of specific modulator structures, dynamic range scaling, performance and stability estimations. As of July 2009 this toolbox also support realization of CT loop filters. As mentioned in the introduction only the typical CIFB and CIFF was investigated.

Referring to the instructions developed in [1], suitable configurations can be established for a given specification and desired behavior, i.e. application. Key architectural options to be determined are modulator order, oversampling ratio, single or multi-bit quantization, out-of-band gain and pole optimization. Targeting the performance specification set in section 4.2.1, a list of suitable candidates for further investigation was established. The coefficients k_i are obtained and used for dimensioning the model and circuit specification. The equivalence between the toolbox's coefficients k_i and resistors R_i for the i^{th} integrator with capacitors C_i are attained through

$$k_i = \frac{1}{f_s \cdot R_i \cdot C_i} \tag{46}$$

4.2.1 Conversion requirements

The converter performance requirements is depicted below

- 2.5 MHz input signal bandwidth
- 74 dB SNDR
- 84 dB SFDR
- Application: Communication

The work in [1] concluded in two main CT $\Delta\Sigma$ architectures for a this specification; a multi-bit 3^{rd} and single-bit 5^{th} order system with an OSR of 32 leading to a sampling frequency f_S of 160 MHz. If accounting for fullscale components close the carrier frequency and to completely avoid an AAF, the requirement to alias-attenuation at $f_S - f_B$ needs to be as good as the SFDR.

4.2.2 Compensation of ELD

To account for the unavoidable ELD, resampling of the NTF with new DAC timings of [0.5 1.5] instead of [0 1] is performed, establishing a margin of half a period to any delay. The $\Delta\Sigma$ toolbox function *realizeNTF_ct* is now fed with this new timing. The D matrix of the ABCD matrix will now include the a_0 coefficient of the additional compensation branch. Also as an effect of ELD compensation, the loop filter coefficient values will also slightly change in order to maintain the overall NTF.

4.2.3 Obtaining transfer functions and establishing noise figures

Using the modulator in the figure 16 as an example along with the ABCD representation of the loop filter, the transfer function from each summation point can be found using the principle of super position. By altering the B matrix successively as in the equation set 47 for a 3^{rd} order feedback system, the transfer functions can be derived within the state-space notation with the following MATLAB code

$$B_{E1} = \begin{bmatrix} b_1 \\ 0 \\ 0 \end{bmatrix} \; B_{E2} = \begin{bmatrix} 0 \\ c_1 \\ 0 \end{bmatrix} \; B_{E3} = \begin{bmatrix} 0 \\ 0 \\ c_2 \end{bmatrix} \tag{47}$$

```
B=[b(1) 0 0]';
NTF_INT1=tf(ss(Acs,B,Ccs,Dc(1)));
gain_INT1=NTF_INT1*NTF;
```

In this work and depicted in section 3, the total thermal noise on each integrator input is the contribution of the resistors, the OpAmp and the feedback DAC. For example, using equations (43)-(45), if the total noise power at the input stage is

$$P_{n1} = V_{ni}^2(f)_{tot1} \cdot f_B, \tag{48}$$

its affect on the system is

$$P_{n,tot1} = P_{n1} \cdot NG_1 = P_{n1}, \tag{49}$$

recalling that the $NG_1 \equiv STF$ in which the noise gain is 0 dB.

4.3 Behavioral modelling

Because of complexity and stability issues, a behavioral model is an important part of successfully designing a $\Delta\Sigma$ modulator. Such a model is a huge step towards a definite verification. The result from the synthesis should be verified and confirmed to ensure proper operation, but parameters should also be finetuned, especially in continuous-time design. Great tools for modelling are for instance MATLAB SIMULINK or a VERILOGA environment. These tools are also the most widely used platforms for systems involving great amount of control and signaling theory. With a future implementation in mind, using a mixed-signal design kit with support for VERILOGA as well as transistor level design constitutes for an ideal platform. Simple interchangeable VERILOGA blocks with transistor level circuits while maintaining system integrity is desirable. Thus, as this thesis was a comparative study with future implementation in mind, the solution provided by the CADENCE framework was chosen as it enables both modelling and implementation interoperability. However, the degree of difficulty for the initial setup is higher, due to a more sophisticated software, making the need for existing knowledge and procedures crucial. VERILOGA code used in this work is built and based on previous work by employees at HITTITE. Also scripts for collecting data and computing important metrics. This greatly reduced the amount of setup time.

Based on the coefficients and results from the synthesis process, a model of both the multi-bit 3^{rd} order and single-bit 5^{th} order modulator was set up to study and verify the different structures. The modulator model included the entire modulator with and without ELD compensation, noise sources and integrator nonidealities, see E.1. The flow of the model development was to first construct and verify the individual components and then establish the basic core of the structures. Verification included simulation of SNDR, SFDR, OBG, STF peaking and the integrators output swing.

Equally important is the setup of the testbench to get accurate simulations and included a stimuli block, the modulator and a measurement block. The stimuli block produced the input signal and also the control signals to the modulator, such as the clock signal. The measuring block consisted by a simple DAC to produce the modulator spectrum for analysis and derive performance. Based on the DACs output, a SKILL based OCEAN script calculated the SNDR and SFDR. INL and DNL is not applicable to $\Delta\Sigma$ -modulation[6, Ch. 1.5]. OCEAN lets you simulate and analyze circuit data with any simulator integrated in the VIRTUOSO enviroment.

4.3.1 VerilogA Model

The modulator part of the model included fully differential active RC-integrators, summation amplifier, S/H, symmetric quantizer and feedback DACs, all funtionality implemented with mixed-signal VerilogA code. Resistors and capacitors were implemented with sizes obtained from the budgetary noise and performance estimates. The excess loop delay was set to half a period, incorporated with simply inverting the clock signal of the feedback DACs. The integrator non-idealities of finite DC gain and GBW was included in the OpAmp model of the integrator, implemented as a single pole transfer function as in equation (24) with code

```
Vp = vcm + laplace_nd(in_hlf,{Av},{1, 1/(`M_TWO_PI*GBW/Av)});
```

Other then the theory behind, optimization of these metrics was set to a reasonable minimum without disrupting the performance or stability. In regards to the OpAmp and DAC noise, generating sources where implemented at the input and output respectively, as in figure 18. Resistors were set to generate noise. A symmetric quantizer and feedback DAC with 7 and 2 levels for the multi-bit and single-bit modulator was implemented.

4.3.2 Dynamic range scaling

Dynamic range scaling must be done to limit and specify the range of the internal states of the modulator, i.e. the integrator outputs, and obtain practical values. As mentioned, this is usually advised to be done through modelling in CT implementations. The principle of proper nonintrusive scaling is that the NTF needs to remain overall unaltered before and after. For the 3$^{\text{rd}}$ order FB modulator of equation (20), scaling involves a couple of conditions to ensure this, including

$$a_3 c_3 = cons_1 \tag{50}$$
$$a_2 c_2 c_3 = cons_2 \tag{51}$$
$$a_1 c_1 c_2 c_3 = cons_3. \tag{52}$$

For instance, to maintain the same NTF when tuning c_1, c_2 and c_3 with a factor k involve

$$c_1 \cdot k \quad \Rightarrow \quad \frac{a_1}{k} \tag{53}$$
$$c_2 \cdot k \quad \Rightarrow \quad \frac{a_1}{k} \cup \frac{a_2}{k} \tag{54}$$
$$c_3 \cdot k \quad \Rightarrow \quad \frac{a_1}{k} \cup \frac{a_2}{k} \cup \frac{a_3}{k} \tag{55}$$

As mentioned in the methodology introduction, dynamic scaling based on state-space approach can only estimate values based on sampling instants, but was performed to give a starting point and as will be seen was quite reasonable.

4.3.3 Conditions for performance estimates

A SKILL based OCEAN script is set up to evaluate the modulator performance using the measurement DAC's output. A Hanning window was applied to get an accurate result when calculating metrics such as the SNDR. The signal component in the spectral plots consist of three components and thus the summation of these determines the signal power. In order to avoid spreading the signal power, f_s and f_{in} needs to be relative prime to eachother. For instance, to get coherent sampling with a desired input signal frequency f_{in} of $\frac{1}{4 \cdot OSR}$(half the bandwidth) and with 4096 DFT points(NBPT), f_{in} is set to 1210953 Hz and f_S to 160002048 Hz. Further, voltages applied was referred to the power supply(A_{VDD}) of 1.8 V, e.q. $V_{FS} = A_{VDD}$, $Ampl_{sig} = \frac{V_{FS}}{2}$ and $V_{CM} = \frac{A_{VDD}}{2}$. Fullscale signal was applied to the input and consequently the input resistance b_1 was adjusted to limit the signal to the desired stable peak SQNR amplitude. The transient noise minimum and maximum frequencies were set to $[\frac{1}{NBPT \cdot T_S}$, 1G] Hz

4.4 Preliminary budgeting

From the coefficients of the $\Delta\Sigma$ modulator, proper resistor and capacitor values can be found based on the noise budget. The resistor values are adjusted by the integrator capacitor and while this directly regulates the resistors and their noise contributions, the OpAmp noise is controlled by g_{m_1} which is set by its GBW and the Miller compensation capacitor C_C, and consequently its specification to the phase margin(PM)

For budgeting purposes, some rough estimates were made to obtain a complete overview of power consumptions and enable for a comparison of the different structures. A couple of conditions used include

- $\frac{g_m}{I_D}$ is typically in the range of $8 - 20$ and was set to 15
  - OpAmp stage 1: $g_{m_1} = 2\pi C_C GBW_1$
  - OpAmp stage 2: $g_{m_5} = 2\pi C_{Int} GBW_2$
- PM was set to 60°(Appendix: F).
  - Sets the GBW_2 and the compensation capacitor C_C
  - $GBW_2 = 2 \cdot GBW_1$ and $C_C = \frac{C_{Int}}{5}$
  - $\Rightarrow g_{m_5} = 10 g_{m_1}$

To obtain a fully adequate power estimate, the power of the DWA logic and quantizer needs to be established. From [35], a 7 level DWA can be made from approximately 250 gates. On the basis of power dissipation data in the TSMC 0.18μm 1.8V SAGE-X process[36] using S2-port figures of 0.03 μW/MHz, sums up to a total of 1200 μW, assuming all ports are S2. Further from [37], a typical 7 level quantizer at 50 MHz use 150 μA leading to a power consumption of 864 μW and 123 μW for a 160 MHz, 7 and 2 level quantizer respectively. The power consumed in the internal feedback current DACs can be estimated from the maximum differential amplitude voltage and the corresponding equivalent resistor($a_1 - a_3$ in the feedback case). The approximate power consumption of the quantizer, DWA logic and DACs:

- DWA logic applicable to a multi-bit DAC
  - 7 level DWA with 250 gates with a consumption of 0.03 μW/MHz(S2) each
  - Results in a total amount of 1200 μW
- Quantizer using 150 μA at 50 MHz
  - 2 level: 123 μW at 160 MHz
  - 7 level: 864 μW at 160 MHz
- Feedback DACs
  - Determined by voltage amplitude and associated resistor
  - E.g. differential voltage amplitude of 0.9V and $R_i = \frac{1}{f_s \cdot k_i \cdot C_i}$

The effect of DWA on the DACs can be seen in the matching considerations, quantified as Signal-to-Mismatch-Noise Ratio(SMNR)[38]. Without DWA the requirement to matching is equal to the SFDR of 14 bits, equivalent to 0.04%($\frac{7}{2^{14}}$) referred to one least significant bit(LSB). With DWA, it is relaxed to a mere 4.4%LSB or with a margin of two, 2.2%LSB.

4.4.1 Circuit specification and dimensioning

The result of extensive and thorough modelling is a precise platform for the development of implementation requirements for system critical components. Including nonidealities into this model creates a detailed specification for the circuit-level implementation. Based on the published results, starting guidelines included:

- DC gain of all OpAmps was set to 40 dB

  - Easily achieved in a two stage OpAmp

- OpAmp GBW was set to a minimum of f_s
  - $2f_S$ may be more suitable towards implementation to avoid problems with parasitic capacitances, process and temperature variations[24]
  - Internal stages exclusive of feedback can however have reduced GBW requirements
  - Speed requirements of the summing amplifier suggests a particular higher GBW for this OpAmp
- Integrator capacitor values C_{Int} was set to a minimum of 350 fF[39]
- Quantizer parasitic capacitance was assumed to be 50 fF per level[39]
  - 100 fF and 350 fF for the single-bit and multi-bit 7 level quantizer

5 Simulations and results

This section describes the observations and results obtained from the three different parts of this work. Decisions and the final parameters set was an ongoing and iterative process based on results from each part. Throughout the following simulations, mainly the 3$^{\text{rd}}$ order feedback structure was used for illustration.

5.1 Results from synthesis

The following candidates was found from synthesis and further investigated. N is the order and Q_l is number of quantization levels.

N	OSR	Q_l	OBG	*Filter*	*SQNR peak*	*STF peaking*	$\lvert STF\rvert_{f_S-f_B}$
3	32	7	2(1.5)	FB	94.5(84.26) dB	-	−116 dB
3	”	”	”	FF	@ −1 dB	6.74 dB(19.47 MHz)	−66 dB
5	”	2	1.5	FB	84.97 dB	-	−197 dB
5	”	”	”	FF	@ −5 dB	7.11 dB(8.53 MHz)	−74.63 dB

Table 5: Candidates used for further investigating modelling

An OBG of 2 was used in the multi-bit 3$^{\text{rd}}$ order case, both as a consequence of higher tolarable OBG of multi-bit modulators, but also because of spectral tone behavior found in modelling. For an input signal amplitude of 0.9 V, these SQNRs translates to quantization noise of 0.9% and 8% of the total amount of noise with 74 dB SNDR. The remaining amount is allocated to the other nonidealities which are considered the limiting factor in high efficiency ADCs.

An OSR of 32 with a bandwidth f_B of 2.5 MHz gives a sampling frequency f_S of 160 MHz. The SQNR versus the input level is simultated in figure 19, establishing an optimal input level of the two systems. The plot also demonstrates the larger stable input range of a multi-bit structure in comparison to the single-bit 5$^{\text{th}}$ order. In figure 20 the STFs for the 3$^{\text{rd}}$ order systems are plotted which clearly shows the inherent anti-aliasing property occuring at f_S integer intervals. Also the undesirable peaking of the FF structure can be observed. The amount of anti-aliasing is evidently lower in the FF compared to the FB structure, due to the aforementioned different signal filters L_0 they employ.

5.1.1 NTFs and noise gains

The coefficients obtained from the synthesis of the 3$^{\text{rd}}$ order system before and after scaling is summarized in appendix A. Inclusion of the ELD compensation path a_0 alters the values in some degree, however not significant. Scaled and unscaled relations remain the same according to equation set (50)–(52). The

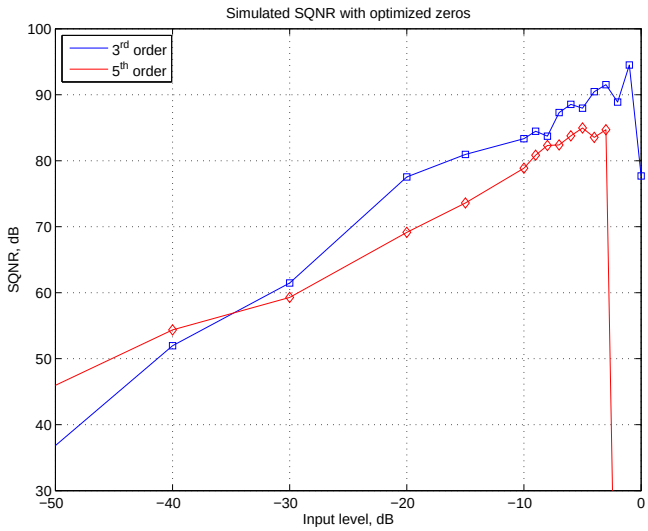


Figure 19: Simulated SQNR against input amplitude of the 3^{rd} and the 5^{th} order system. Notice that the single-bit 5^{th} order system becomes unstable before the multi-bit 3^{rd} order

noise transfer function from each integrator input are plotted and quantified in figure 21, figure 22 and table 6. These functions were obtained from the synthesis results and with the coefficient values. Table 6 can essentially be used as a scaling

Source	*3rd FB*	*3rd FF*	*5th FB*	*5th FF*	
NG_Q	-60.7	-60.7	-65.3	-65.3	dB
NG_5			-30	-44.3	dB
NG_4			-19.6	-40	dB
NG_3	-23.4	-36.6	-8.1	-25.5	dB
NG_2	-10.2	-18.5	-3.5	-14.5	dB
NG_1	0	0	0	0	dB

Table 6: Noise gain(NG) of the NTFs from $[0,\ f_B]$, equivalent to the amount of noise suppression at each node. E_Q, E_1 and $E_2 - E_5$ represents the quantization, signal and internal nodes respectively

platform of the components at each stage. Noticably, internal noise gains are quite different in the FB and FF structure, and in favor of the FF due to the nature of its structure. Obviously, the 5^{th} order FB modulator will struggle to

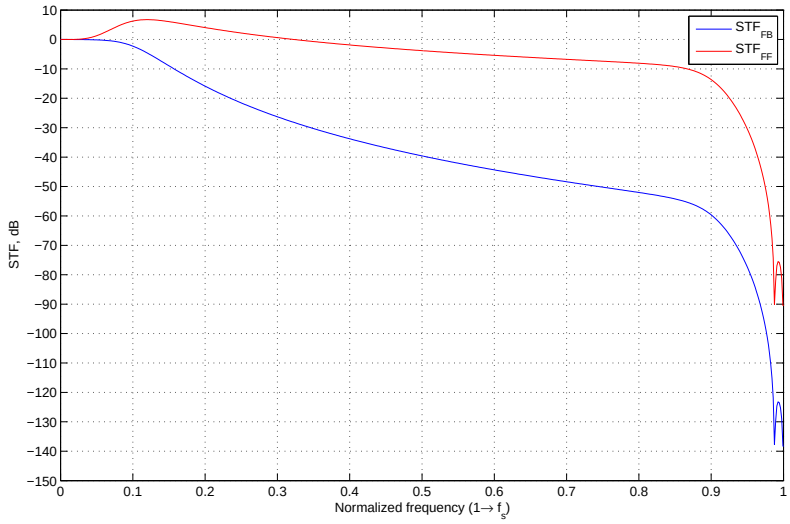


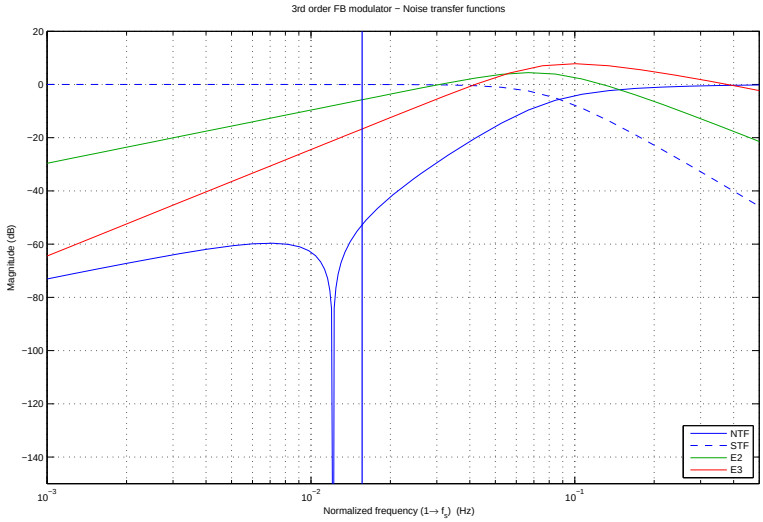
Figure 20: Simulated STFs of a FB and FF 3$^{\text{rd}}$ order CT$\Delta\Sigma$ modulator showing the desirable inherent anti-aliasing property. Also notice the difference in the amount of aliasing attenuation between the systems and the peaking of the FF system

maintain low noise requirements as the amount of noise suppression is fairly low for succeeding stages. Also its small coefficients along with the limited input amplitude will require large capacitor values to sufficiantly attenuate the inband noise.

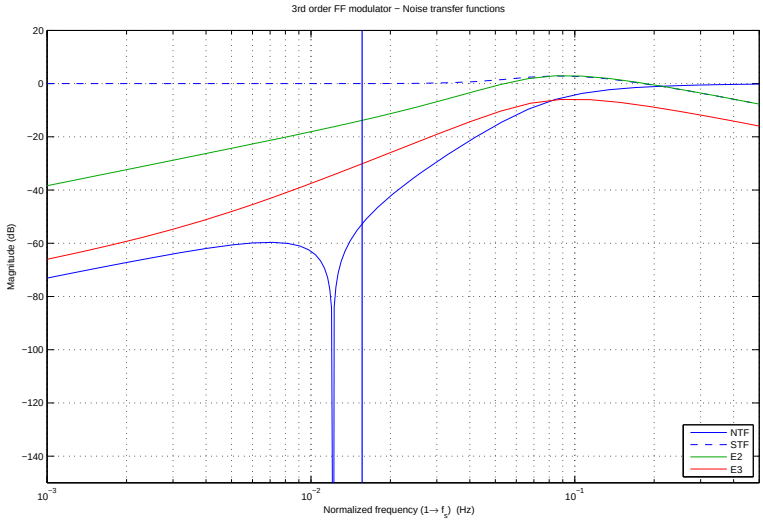
The four structure's transfer functions also show the effect of utilizing resonators in the modulator. Notice that only the noise sources defined after a resonator will get the desirable inband attenuation of the local feedback loops, e.q. only the quantization noise in the 3$^{\text{rd}}$ order system. Using the scaling relations in section 4.3.2, adjustments can be made to customize or tailor specific characteristics desired at each node, for instance meeting a certain requirement set. Also notice the peaking of the internal functions, most evident in the 5$^{\text{th}}$ order feedback.

5.1.2 Noise budget

The total amount of noise available in the two architectures was set from the SQNR peak input amplitude which was at -1 dBFS and -5 dBFS in the 3$^{\text{rd}}$ and 5$^{\text{th}}$ order respectively. This translates to noise powers of $12.8nV^2$ and $8.06nV^2$

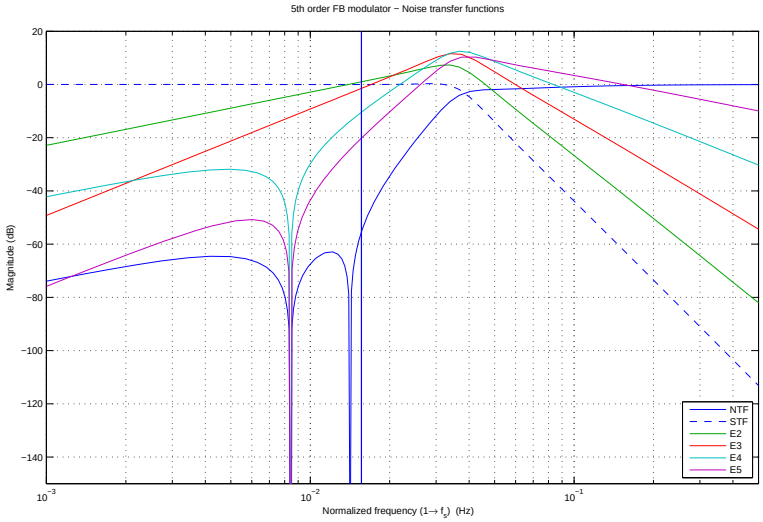


(a) 3rd order FB

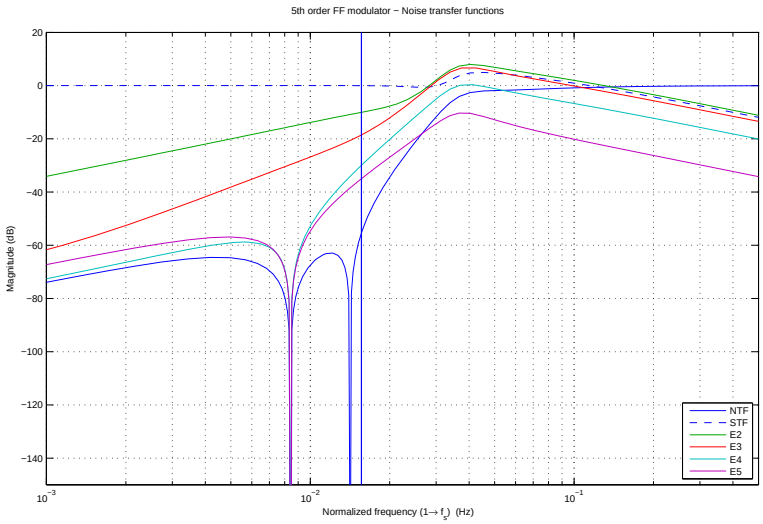


(b) 3rd order FF

Figure 21: Transfer functions from each integrator input for the 3^{rd} order modulators investigated. Notice that only the TFs defined after a resonator gets affected by its zero



(a) 5th order FB



(b) 5th order FF

Figure 22: Transfer functions from each integrator input for the 5^{th} order modulator investigated. Notice that only the TFs defined after a resonator gets affected by its zero

with a fullscale of 0.9 V. Using the formulas in section 3 and performing an iterative process of tuning R and C values, the noise figures in table 7 for the 3rd order[3] are obtained. The feedback DACs are allocated most of the noise. Also notice that the sources $E2$ and $E3$ in the 3rd FF structure, or $E2$-$E5$ in the FF 5th order, is without DAC noise contribution. This enables a large part of the noise to be allocated to the 1st stage as evident from the noise budgets.

Source	*E1*	*E2*	*E3*	*EQ*	
$V_{ni,DAC}(f)$	52.2	69.3	85	63.8	nV
$V_{ni,R}(f)$	40.3	40.2	38.5	13	nV
$V_{ni,OpAmp}(f)$	5.9	9.2	12.5	6.26	nV
$V_{ni}^2(f)_{tot}$	4.4	6.5	8.9	4.3	fV^2
$P_{ni}\,(V_{ni}^2(f)_{tot} \cdot f_B)$	11	16.3	22.19	10.7	nV^2
Increase ref. $E1$	0	3.4	6.1	-0.22	dB

(a) 3rd order FB

Source	*E1*	*E2*	*E3*	*EQ*	
$V_{ni,DAC}(f)$	56.8			63.8	nV
$V_{ni,R}(f)$	41.4	31.1	48.2	37.5	nV
$V_{ni,OpAmp}(f)$	9.73	12.5	12.5	6.26	nV
$V_{ni}^2(f)_{tot}$	5.04	1.1	2.5	5.5	fV^2
$P_{ni}\,(V_{ni}^2(f)_{tot} \cdot f_B)$	12.6	2.81	6.2	13.8	nV^2
Increase ref. $E1$	0	-13.01	-6.16	0.77	dB

(b) 3rd order FF

Table 7: Noise density voltages for the 3rd order feedback and feedforward structure used in the model

Table 8 for the 3rd order[4] modulators show the noise budget based on the noise figures, where each source's noise power are weighted with the NG to get their final contribution. The largest share as expected, due to no suppression, is the 1st stage. In the FF structures almost all of the noise budget can be allocated to the 1st stage. With the quantization noise share in mind, the 3rd and 5th order circuit noise budget was targeting approximately 99% and 92% of the overall noise. Clearly, due to the lower maximum stable input amplitude of the 5th order structures and therefore the reduced total amount of noise available, stringent demands are set especially for these structures.

[3] 5th order noise voltages in appendix B
[4] 5th order noise shares in appendix B

	E1	*E2*	*Remaining*	*Total*	
$P_{ntot}[P_{ni} \cdot NG_i]$	11	1.57	0.1	12.6	nV^2
Share	85.6	12.3	0.8	98.7	%
SNDR	74.67	83.11	95	74.06	dB

(a) 3FB

	E1	*Remaining*	*Total*	
$P_{ntot}[P_{ni} \cdot NG_i]$	12.6	0.041	12.64	nV^2
Share	98.4	0.32	98.68	%
SNDR	74.07	99	74.06	dB

(b) 3FF

Table 8: Circuit noise budget, 3rd order structures. The remaining column represents stage E3 and EQ in the FB structure and stage E2, E3 and EQ in the FF

5.2 Modelling results

The simulation results from the modelling provides a more definite answer on how the final system will perform. The list of important aspects of CT$\Delta\Sigma$ modelling is quite large so many interesting features have been considered beyond the scope of this thesis. However, a couple of principles introduced in the theoretical part of this paper is simulated in addition to the primary goal of synthesis verification. For clarity and if not else specified, all figures and plots are based on an OSR of 32, bandwidth f_B of 2.5 MHz and a sampling frequency f_S of 160 MHz.

The STF peaking distinctive of a feedforward system is shown in figure 23 for a 3rd order modulator. By comparing the peak to synthesis values, which found a 6.74 dB peak at 19.47 MHz, there is a slight difference. The STF peak in figure 23 is roughly at 17.9 MHz with a magnitude of 9.67 dB, 3 dB higher and 1.5 MHz off the synthesis simulation. The input level versus the SQNR, figure 24, are in correspondance with synthesis with a peak at approximately -1 dBFS. As simulated in the synthesis, the SQNR peak is located at -1 dBFS suggesting that the ideal model depicts similar performance. The four out spectra for the ideal structures are shown in appendix D. The desirable effect of the resonators can clearly be seen with one notch in the 3rd order spectrums and two in the 5th order spectrums.

The simulated performance metrics of the ideal structures is listed in table 9 and show similiar result as obtained in the synthesis.

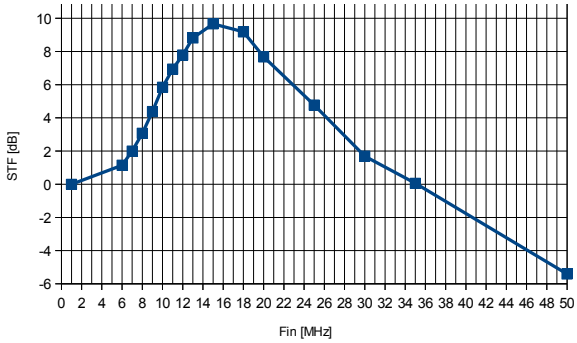


Figure 23: STF as a function of the input signal frequency of an ideal 3rd order feedforward structure illustrating the characteristic peaking. The input amplitude was set to -12 dB to avoid instability issues

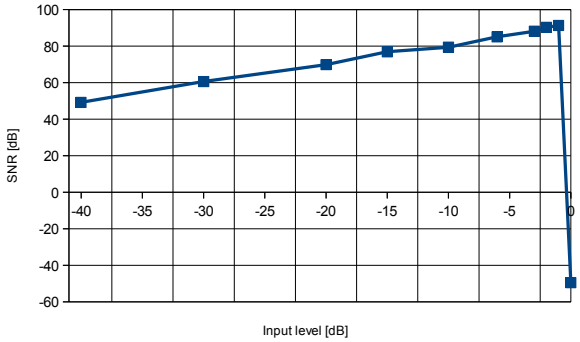


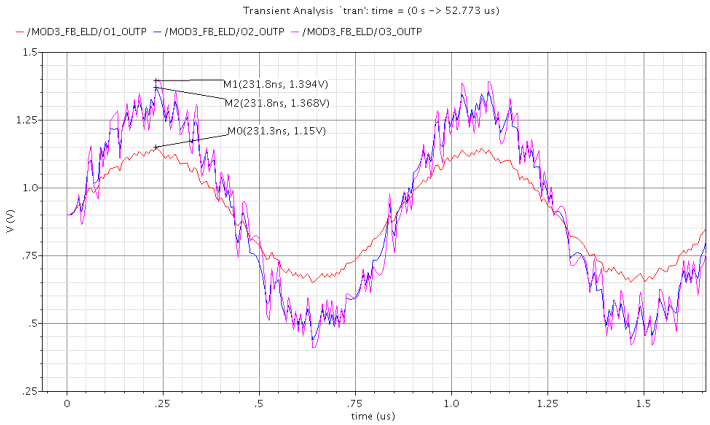
Figure 24: SQNR versus the input level depicting the stable input range for an ideal 3rd order FF modulater

	3FB	*3FF*	*5FB*	*5FF*	
SNDR	92.45	92.9	84.6	84.5	dB
SFDR	102	105.1	96.7	93.14	dB

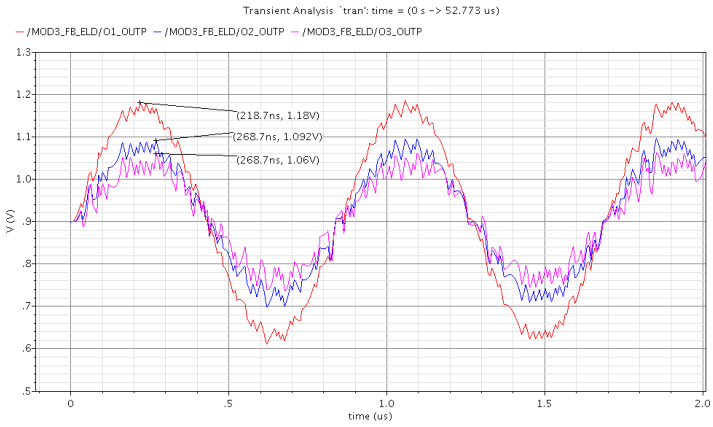
Table 9: Ideal performance metric obtained in modelling

5.2.1 Scaling and FB/FF swing comparison

Dynamic range scaling of the 3rd order FB structure is depicted for observation in figure 25. These waveforms are based only on the built in discrete scaling of the toolbox and as seen delivered quite decent results. Both unscaled and scaled



(a) Unscaled FB



(b) Scaled FB

Figure 25: Positive integrator outputs of the 3rd order FB modulator, (25a) unscaled and (25b) scaled. O1(red), O2(blue) and 03(pink) represents integrator output 1, 2 and 3. Notice the large amount of input signal present in the waveforms specific for feedback structure

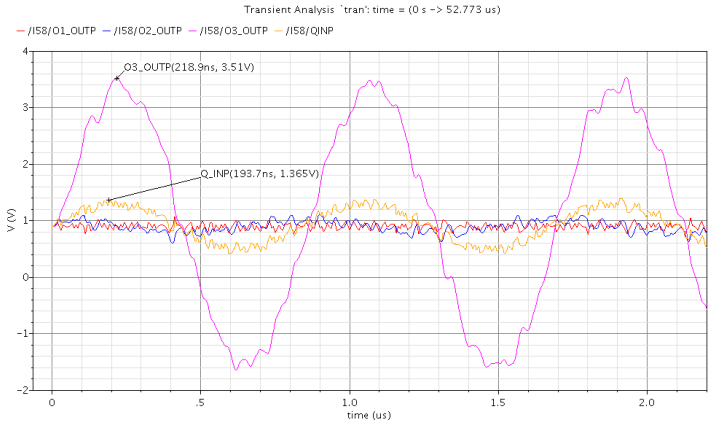
structures have limited outputs and hence, are stable. As the fullscale voltage was set to 1.8 V and common mode to 0.9 V, a differential swing of ± 0.45 V is a practical amount towards implementation, translating to an output swing restricted to $V_{CM} \pm 0.45V$. Both sets of coefficients in this setup furfilled this implementation specification. The scaled waveforms are however closer together, suggesting that similar specified amplifiers can be implemented in respect to output swing leading to lower overall design time. As an illustration of the low-distortion feature in the FF structure, figure 26 is obtained showing the absence of input signal through the signaling chain of the modulator. Also in contrast to the FB, the applied scaling here shows a significant improvement. The unscaled output of the first integrator peaks at 3.51 V while more appropriatly just peaks at 1.172 V when scaled.

5.2.2 Impact of nonidealities

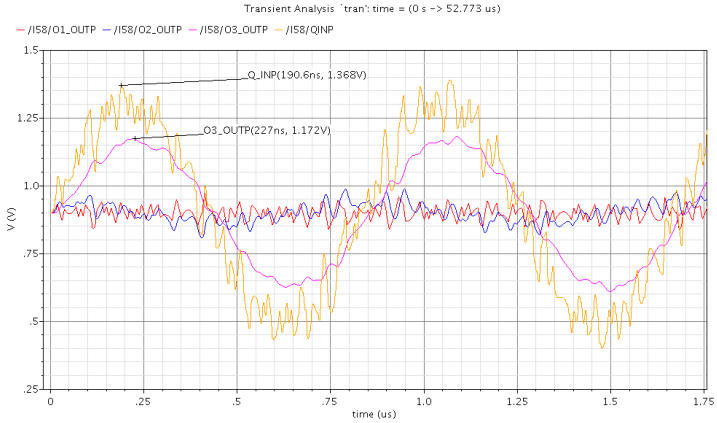
Figure 27 shows the SQNR degradation as a function of amplifier GBW. While minimal degradation is seen with a low GBW of around f_S, integrator swings also needs to be monitored. This can be observed in the OBG plotted in figure 28, where the OBG drastically drops below a certain GBW. Also, when applying a low GBW, output spectrums starts to show peaking behavior. Both plots show what was theoretically claimed in section 2.3.3 to be quite accurate. A GBW product frequency of approximately f_S is not severely degrading performance and can be set as lower limit when considering nonideal effects. Using the ideal, non ELD compensated 3$^{\text{rd}}$ order FB modulator with increasingly delaying DAC pulses, the plot in figure 29 is obtained. The modulator can handle an excess loop delay of approximately 20% before becoming unstable. With the inclusion of the compensation DAC and modified coefficients, a delay t_d of $0.5T_S$ is taken into account. The performance is equivalent to an ideal, non compesated setup as can be seen in the 3$^{\text{rd}}$ order FB spectrum in figure 30, achieving an SQNR of 93 dB.

5.2.3 Noise impact

The ELD compensated nonideal spectras of the four structures can be seen in figure 31 with their performance metrics depicted in table 10. Comparing the noise budget in 5.1.2 with the final performance metrics simulated, the results are of similar nature. This worked as the final verification of the synthesis and noise analysis/budgeting. The 3$^{\text{rd}}$ order structures are close the synthesis results, while the 5$^{\text{th}}$ order suffers a minor deviation from ideally calculated values.



(a) Unscaled FF



(b) Scaled FB

Figure 26: Positive integrator outputs of the 3rd order FF modulator, (26a) unscaled and (26b) scaled. O1(red), O2(blue), 03(pink) and Q(yellow) represents integrator output 1, 2, 3 and the quantizer's input. Notice the low amount of input signal present inside the loop compared to the feedback structure

	3FB	*3FF*	*5FB*	*5FF*	
SNDR	74.04	74.09	73.3	75.1	dB
SFDR	85.4	86.12	83.6	86.16	dB

Table 10: Final nonideal performance obtained in modelling

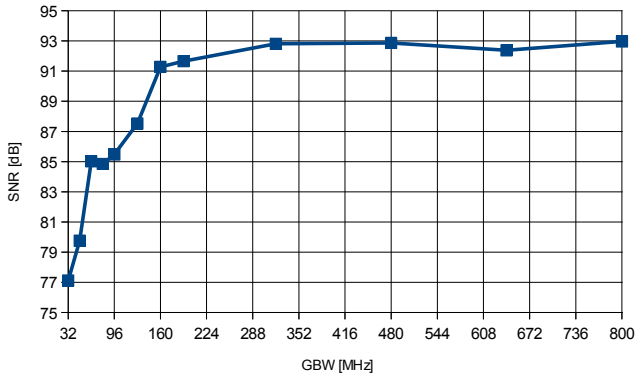


Figure 27: SQNR as a function of the amplifier GBW frequency of an ideal 3$^{\text{rd}}$ order feedforward structure, all integrators use the same GBW product. Notice the drop in SNR starting at f_S

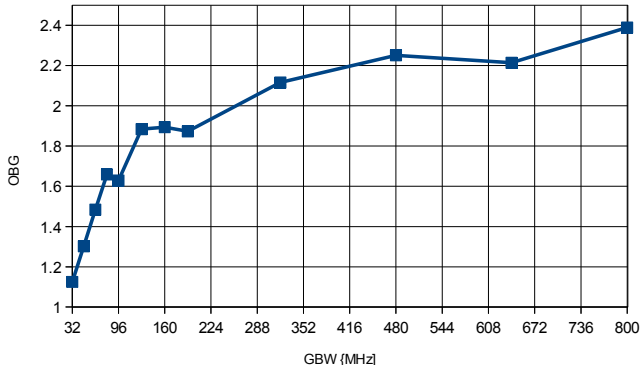


Figure 28: OBG as a function of the amplifier GBW frequency of an ideal 3$^{\text{rd}}$ order feedforward structure, all integrators use the same GBW product. Notice the drastic drop in OBG starting just below f_S

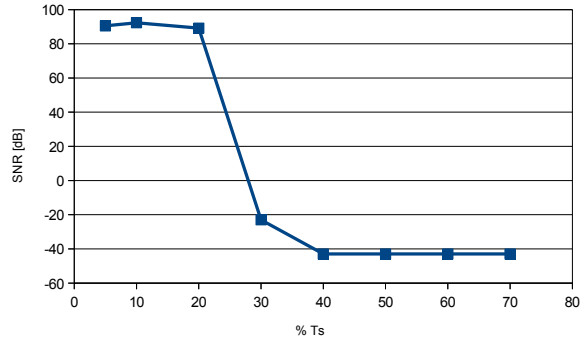


Figure 29: SQNR versus ELD for an ideal 3rd order FB structure

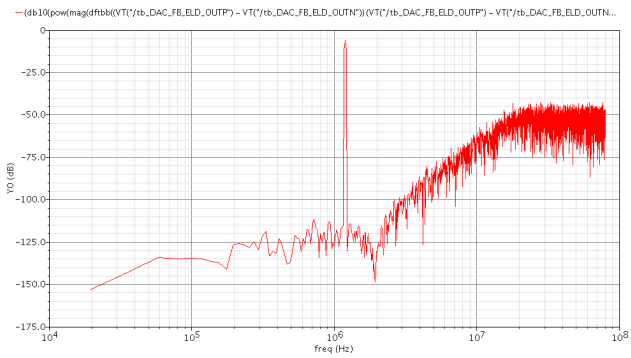
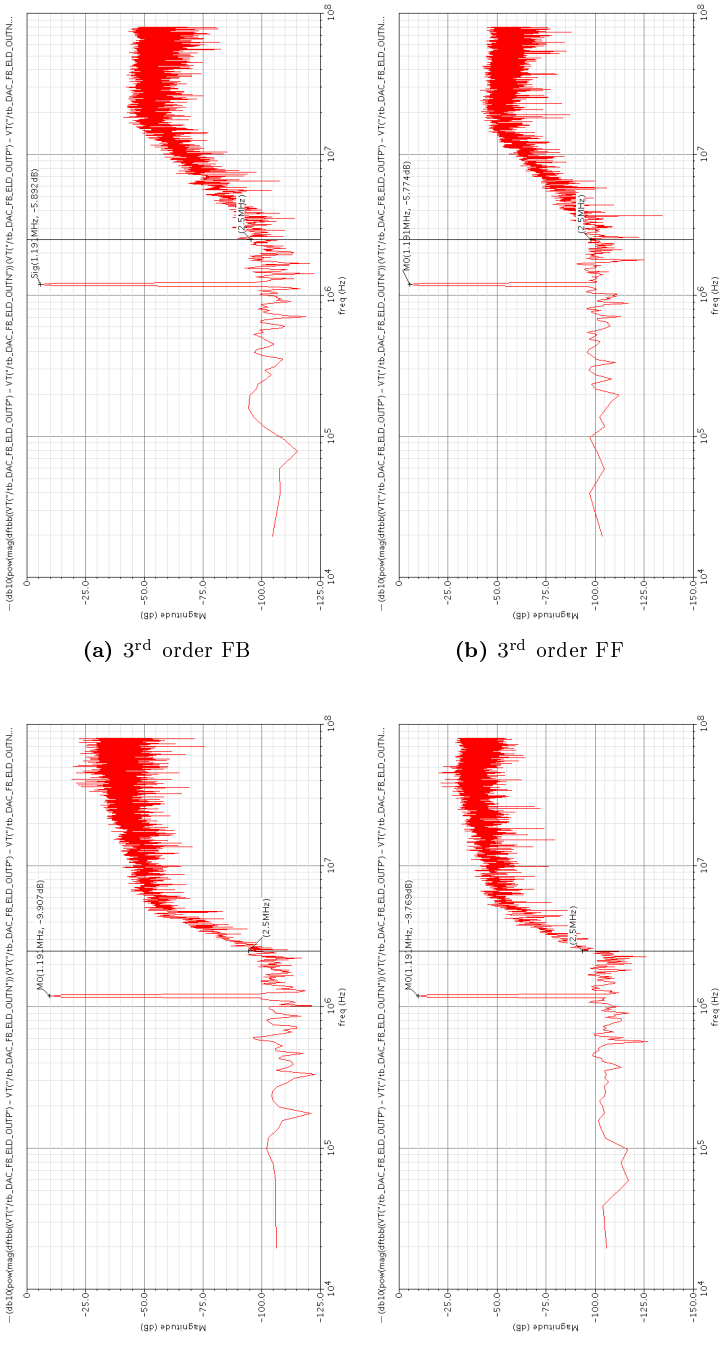


Figure 30: Spectra of an ideal ELD compensated 3rd order FB modulator



(a) 3rd order FB **(b)** 3rd order FF

(c) 5th order FB **(d)** 5th order FF

Figure 31: Output spectra for the nonideal structures with noise, limited DC gain and GBW, $NBPT = 8192$, $f_S = 160006144$ Hz, $f_{in} = 1191452$ Hz, $P_{sig,3^{\text{rd}}} = -1dBFS$ and $P_{sig,5^{\text{th}}} = -5dBFS$

5.2.4 Implementation specification and power budget

The resulting specification of the integrators, using the relations defined in section 4.4, from the noise budget is listed in table 11 for the 3rd order[5] structures. From this an estimated power consumption budget can be set up in order to

Spec	*Int 1*	*Int 2*	*Int 3*	*Sum*	*Unit*
A_0	40	”	”	”	dB
GBW	320	320	320	1280	MHz
Int Cap	1.6	0.65	0.35	0.35	pF
C_C	0.32	0.13	0.07	0.07	pF
g_{m1}	0.64	0.26	0.14	0.56	mS
g_{m5}	6.4	2.6	1.4	0.56	mS
I_{D1}	42.9	17.4	9.4	37.5	uA
I_{D2}	429	174.3	93.8	37.3	uA

(a) 3rd order FB

Spec	*Int 1*	*Int 2*	*Int 3*	*Sum*	*Unit*
A_0	40	”	”	”	dB
GBW	320	320	320	1280	MHz
Int Cap	0.58	0.35	0.35	0.35	pF
C_C	0.116	0.07	0.07	0.07	pF
g_{m1}	0.23	0.14	0.14	0.563	mS
g_{m5}	2.3	1.4	1.4	5.63	mS
I_{D1}	15.5	9.4	9.4	37.5	uA
I_{D2}	155	94	94	24	uA

(b) 3rd order FF

Table 11: Specification of the integrators for the 3rd order structures. Recall g_{m5}, I_{D2} is dependent on β for the summation amplifier, appendix F

compare the different structures. The overall power dissipation for each structure, including their individual block shares, are listed in table 12 and 13. While the amount of power consumption is roughly evenly distributed in the 3rd order structures, almost all of the power in the 5th order structures are dissipated in the integrators.

[5] 5th order integrator specification in appendix C

Structure	*Int.*	*Q*	*DWA*	DAC_1	DAC_2	DAC_3	DAC_4	DAC_5	DAC_{ELD}	*Total* μW
3FB	1515	864	1200	56	32	21			37	3724
3FF	790	864	1200	53					37	2944
5FB	12527	123	N/A	161	186	133	96	45	7	13278
5FF	1892	123	N/A	120					7	2142

Table 12: Power consumption budget

Structure	*Integrators*	*Quantizer*	*DWA*	*DACs*	
3FB	40	23	33	4	%
3FF	27	29	41	3	%
5FB	94	1	N/A	5	%
5FF	88	6	N/A	6	%

Table 13: Power consumption budget, block shares

6 Discussion

The application of the ADC was set to communication with an SNDR of 74 dB, SFDR of 84 dB and a 2.5 MHz input signal bandwidth. Nonidealities such as excess loop delay, circuit noise, finite DC gain and GBW was explored and their impact quantified. Optimization and power estimation for the entire modulator was performed in order to be able to make a comparison between each modulator.

6.1 Modulator order and filter structures

The synthesis simulations found two suitable modulator architectures at an OSR of 32; a multi-bit 3^{rd} order and a single-bit 5^{th} order achieving 94.5 dB SQNR at -1 dBFS and 85 dB SQNR at -5 dBFS respectively. A desirable feature of the 3^{rd} order system included stability enhancing multi-bit quantization. The 5^{th} order system had the single-bit benefit of inherent linearity and thus the omission of any element correction techniques. Both feedback and feedforward configurations of the loop filter was explored in detail. Key benefitial characteristics of the FB structure included a superior alias rejection, while for a FF structure, a low-distortion property applied. The simulated alias attenuation at $f_S - f_B$ was -116 dB and -66 dB for the 3^{rd} order FB and FF structures, and -197 dB and -75 dB for the 5^{th} order FB and FF. With communications as the area of application and the possibility of fullscale components close to the carrier frequency, to completely avoid an AAF require the amount of attenuation at $f_S - f_B$ to as good as the SFDR at 84 dB. This demand is furfilled only by the FB structures. However, the buildup of the FB structure involve $N - 1$ more internal DACs in comparison to the FF. Also the signal feedforwarding in the FF structures, result in a low amount of input signal present inside the filter, reducing integrator output swings and hence relaxing the requirement of the OpAmps. The result of this is lower power consumption, but also stability concerns due to the specific STF peaking only applicable to FF filters. For the 3^{rd} and 5^{th} order FF structures, the simulated STF peak was 6.74 dB at 19.47 MHz and 7.11 dB at 8.53 MHz. In the published literature, due to the many contradicting properties, a combination of both FB/FF branches are often utilized to obtain advantages from both structures. 3^{rd} order modulators are often hybrids combining FB/FF while 5^{th} order FB structures are rarely realized.

6.2 Behavioral modelling

From the established candidates, a behavioral VerilogA model was developed for verification of the synthesized structures and also, by including nonidealities, analyze crucial, performance degrading parts towards a future implementation. Modelling using VerilogA along with the Cadence framework was chosen as

it enables a mixture of model describing blocks and circuit level implementations. The performance of the four structures when ideally modelled showed a great correspondance with the synthesized values. Ideal SQNR performance simulated in modelling was 92.45 dB, 92.9 dB, 84.6 dB and 84.5 dB for the 3^{rd} order FB/FF and 5^{th} order FB/FF structure respectively. Excess loop delay, specific for CT$\Delta\Sigma$ implementations, of up to half a period was accounted for by modifying coefficients and adding a direct feedback DAC. The characteristics of the system with and without ELD compensation remain the same as desired, e.q. the ideal 3^{rd} order ELD compensated modulator achieved 93 dB SQNR. Finite DC gain and limited GBW was also included in the OpAmps and was found to be destructive when lowered below the already published limits of DC gain $\approx OSR$ and GBW $\approx f_S$. A DC gain of 40 dB is easily achieved in a $\Delta\Sigma$ suitable two-stage OpAmp and was therefore chosen equal for all OpAmps. A GBW of $2f_S$ was chosen for integrators to account for implementation specific effects such as parasitic capacitances. The crucial summation amplifier infront of the quantizer needed a significantly higher GBW in the range of $8f_S - 10f_S$ to not affect the performance. If lowered, peaking curvature started to appear in the output spectrums. The design of this circuit is considered one of the main difficult challenges in CT$\Delta\Sigma$ design.

6.3 Noise analysis

After establishing the four structures in both synthesis and behavioral modelling, a noise analysis was performed specific to the noise-shaping $\Delta\Sigma$ modulator to obtain a more detailed specification. The noise sources included the resistors, OpAmps and current DACs. The noise gain from each integrator input node was found and quantified. By referring the noise to the input of each stage and weighting them with the associated noise gain, their contribution to the overall system is found. The 1^{st} stage is by far the most crucial part as errors induced here directly adds to the signal. Inside the loop filter, FF structures have greater noise suppression compared to their counterparts. For instance, as seen in table 6, the NG_2 of the 2^{nd} stage in the FB/FF 3^{rd} order structures, are -10.2 dB and -18.5 dB respectively, which directly translates to the possibility of allocating a larger part of the noise budget in the FF case, to the 1^{st} stage. The 5^{th} order FB structure experienced the worst NG figures with for instance a NG_2 of only -3.5 dB, clearly making the requirements of the subsequent stages high and power hungry. By using the NTF coefficient relations, the NTFs, and consequently the NGs, can be adjusted for to meet certain specific requirements of internal stages. This was not further explored.

Noise density voltages based on noise budgets targeting an SNDR of 74 dB was established and made it possible to optimize R and C values depending on each

stage's contribution. By only considering quantization and the aforementioned nonidealities, the circuit noise took a $\approx 99\%$ share in the 3^{rd} order and a 92% share in the 5^{th} order of the overall budget. With all nonidealities included, the final model performance was simulated to 74.04 dB, 74.09 dB, 73.3 dB and 75.1 dB for the FB/FF 3^{rd} order and FB/FF 5^{th} order structures respectively.

6.4 Power budget

Detailed integrator specifications was developed from the noise analysis. Power consumption for the quantizer, DACs and their logic was also considered, based on already published results and/or internal correspondance. This was done to get a clearer, although quite rough, comparative overview of what the final result with respect to efficiency would become. However, the estimates contain uncertainties and must be verified in a circuit-level implementation for a definite solution. The power consumption of the four structures was calculated to 3724 μW, 2944 μW, 13278 μW and 2142 μW for the 3^{rd} order FB/FF and 5^{th} order FB/FF respectively. In the 3^{rd} order multi-bit setup, the DWA logic takes up a significant amount of the overall power at 33% and 41%. In the 5^{th} order setup, the integrators by far consumes the most amount of power with 94% and 88% shares. Here, the use of single-bit quantization really show its effect. Although the FF structures consume the least amount of power, they lack the alias suppression. With the requirement of an STF attenuation of 84 dB, they would need an additional AAF on the input, increasing complexity and power consumption. The 3^{rd} order FB structure consumes a bit more power, but furfills the anti-alias requirement and can suffice without the use of an AAF.

7 Conclusion

The main objectives of this work was to model and analyze different topologies of the versatile CT$\Delta\Sigma$ A/D converter and make an informed decision on the optimal architecture for the performance requirements of 74 dB SNDR, 84 dB SFDR and an input signal bandwidth of 2.5 MHz. The application of the converter was communication. Extensive and thorough analysis on nonidealities such as excess loop delay, circuit noise, finite DC gain and GBW was explored and their impact quantified. Using R. Schreier $\Delta\Sigma$ toolbox and the CADENCE framework for synthesis and behavioral modellling, architectural properties could be established, verified and optimized.

A 3^{rd} order NTF-aggressive multi-bit modulator and a 5^{th} order single-bit modulator in feedback and feedforward configurations, operating at an OSR of 32, achieved the performance requirements set. The modulators obtained an SQNR of 94.5 dB and 85 dB respectively. The undesirable STF peaking of the FF structures was synthesized to 6.74 dB and 7.11 dB. Alias attenuation was superior in the FB filters with -116 dB and -197 dB for the 3^{rd} and 5^{th} order FB systems, and -66 dB and -75 dB for the 3^{rd} and 5^{th} order FF systems. The development of an in-depth noise analysis specific for $\Delta\Sigma$ modulators, resulted in a budgeting scheme for optimizing and dimensioning crucial parts, useful towards a future implementation. The noise analysis resulted in NG figures in favor of the FF structures and with the 5^{th} order FB modulator experiencing the worst performance with only slight NG improvement in subsequent stages. The behavioral model was in great correspondance with the synthesized and estimated results, and worked both in terms of verifying predicted characteristics, but also specifying crucial parts in detail.

Targeting the 74 dB SNDR with all nonidealities, the 3^{rd} order FB and FF modulator consumed 3724 μW and 2944 μW, and the 5^{th} order FB and FF 13278 μW and 2142 μW. The DWA logic applicable to the multi-bit structure used a significant amount of the overall power in the 3^{rd} order modulator, while almost all the power in the single-bit 5^{th} order structures are consumed in the integrators. Although the feedforward structures consumed the least amount of power under these quite crude estimations, due to the alias attenuation requirement, the 3^{rd} order feedback modulator not needing the additional AAF made it the optimal structure for the given performance specifications.

8 Future Work

A natural step forward in the process would be to include circuit-level components, based on the specifications developed, into the model. Effort went into examining the estimated active RC-integrator specification by a real circuit-level implementation, but due to time constraints were only partly finished. By including a transistor-level implementation for each block, the weaknesses of the model can be found by studying the actual properties such as noise, power consumption and their influence on the system. This can be performed individually for each block to find dependencies while maintaining the functionality and integrity for the overall system. Also slight modifications to further optimize the general structures could be explored and quickly compared.

References

[1] L. Rypestøl, "Synthesis and Modelling of an Effective, High-Resolution A/D Converter," Project - TFE4545 - Analog and Mixed Design, Specialization Course NTNU, Department of Electronics and Telecommunications. 2010.

[2] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion Fundamentals, Performance Limits and Robust Implementations*. Secaucus, NJ, USA: Springer-Verlag New York, Inc., ISBN: 978-3-540-28406-2. Springer Series in Advanced Microelectronics Volume 21, 2006.

[3] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. New York, IEEE press, Wiley-Interscience, ISBN: 0-471-46585-2. 2005.

[4] X. Chen, Y. Wang, Y. Fujimoto, P. Lo Re, Y. Kanazawa, J. Steensgaard, and G. Temes, "A 18 mW CT DS modulator with 25 MHz bandwidth for next generation wireless applications," in *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, pp. 73 –76, sept. 2007.

[5] Z. Li and T. Fiez, "A 14 Bit Continuous-Time Delta-Sigma A/D Modulator With 2.5 MHz Signal Bandwidth," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1873 –1883, sept. 2007.

[6] J. A. Cherry and W. M. Snelgrove, *Continuous-time Delta-sigma Modulators for High-speed A/D- Conversion : Theory, Practice, and Fundamental Performance Limits*. Kluwer Academic Publishers, Hingham, MA, USA, ISBN 978-0792386254. 1999.

[7] International Solid-State Circuit Conference, "ISSCC 2008 press kit," 2008. [Online]. Available: `http://isscc.org/doc/2008/ISSCC_PressKit_2008.pdf`.

[8] B. Jonsson, "A survey of A/D-Converter performance evolution," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, pp. 766 –769, dec. 2010.

[9] International Solid-State Circuit Conference, "ISSCC 2009 press kit," 2009. [Online]. Available: `http://isscc.org/doc/2009/ISSCC_PressKit_2009.pdf`.

[10] J. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, pp. 1 –21, jan. 2011.

[11] H. Inose, Y. Yasuda, and J. Murakami, "A Telemetering System by Code Modulation - Delta-Sigma Modulation," *Space Electronics and Telemetry, IRE Transactions on*, vol. SET-8, pp. 204 –209, sept. 1962.

[12] J. Candy, "A use of double integration in sigma delta modulation," *Communications, IEEE Transactions on*, vol. 33, pp. 249 – 258, mar 1985.

[13] K.-H. Chao, S. Nadeem, W. Lee, and C. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *Circuits and Systems, IEEE Transactions on*, vol. 37, pp. 309 –318, mar 1990.

[14] T. Brooks, D. Robertson, D. Kelly, A. Del Muro, and S. Harston, "A cascaded sigma-delta pipeline a/d converter with 1.25 mhz signal bandwidth and 89 db snr," *Solid-State Circuits, IEEE Journal of*, vol. 32, pp. 1896 –1906, dec 1997.

[15] F. Maloberti, *Data Converters*. Secaucus, NJ, USA: Springer-Verlag New York, Inc., ISBN: 0-387-32485-2. 2007.

[16] M. S. Yves Geerts and W. Sansen, *Design of Multi-Bit Delta-Sigma A/D Converters*. Springer-Verlag New York, Inc., ISBN 978-1-4020-7078-5. The Kluwer International Series in Engineering and Computer Science Volume 686, 2003.

[17] P.-V. B. R.-V. A. Medeiro, Fernando, *Top-Down Design of High-Performance Sigma-Delta Modulators*. Secaucus, NJ, USA: Springer-Verlag New York, Inc., ISBN: 978-1-4419-5067-3. 1999.

[18] Omid Shoaei, "Continuous-Time Delta-Sigma A/D Converters for High Speed Applications," PhD Thesis, Carleton University 1995. [Online]. Available: `http://www.dissonance.com/archive/phd/shoaeithesis.pdf`.

[19] D. Python, M. Punzenberger, and C. Enz, "A 1-V CMOS log-domain integrator," in *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, vol. 2, pp. 685 –688 vol.2, jul 1999.

[20] F. Gerfers, M. Ortmanns, and Y. Manoli, "A 1.5V 12-bit power-efficient continuous-time third-order Sigma; Delta; modulator," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 1343 – 1352, aug. 2003.

[21] B. Boser and B. Wooley, "The design of sigma-delta modulation analog-to-digital converters ," *Solid-State Circuits, IEEE Journal of*, vol. 23, pp. 1298 –1308, dec 1988.

[22] M. Ortmanns, F. Gerfers, and Y. Manoli, "Compensation of finite gain-bandwidth induced errors in continuous-time sigma-delta modulators," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, pp. 1088 – 1099, june 2004.

[23] Xuefeng Chen, "A Wideband Low-Power Continuous-Time Delta-Sigma Modulator for Next Generation Wireless Application," PhD Dissertation, Oregon State University, 2007. [Online]. Available: `http://hdl.handle.net/1957/4276`.

[24] F. Gerfers, M. Ortmanns, and Y. Manoli, "A 1 V, 12-bit wideband continuous-time Sigma-Delta modulator for UMTS applications," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 1, pp. I–921 – I–924 vol.1, may 2003.

[25] O. Oliaei, "Design of continuous-time sigma-delta modulators with arbitrary feedback waveform," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 50, pp. 437 – 444, aug. 2003.

[26] R. Schreier and B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 43, pp. 324 –332, apr 1996.

[27] J. Cherry and W. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 46, pp. 376 –389, apr 1999.

[28] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli, "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma-Delta Modulators," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, pp. 3480 –3487, dec. 2008.

[29] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900mV low-power Delta-Sigma A/D converter with 77-dB dynamic range," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 1887 –1897, dec 1998.

[30] Y. Zhang and A. Leuciuc, "A 1.8 V Continuous-Time Delta-Sigma Modulator with 2.5 MHz bandwidth," in *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, vol. 1, pp. I – 140–3 vol.1, aug. 2002.

[31] P. Silva, K. Makinwa, J. Huijsing, and L. Breems, "Noise analysis of continuous-time $\Delta\Sigma$ modulators with switched-capacitor feedback DAC," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, pp. 4 pp. –3793, 0-0 2006.

[32] B. Li, L.-R. Zheng, and H. Tenhunen, "Hierarchical modeling of sigma delta modulators for noise coupling analysis," in *Mixed-Signal Design, 1999. SSMSD '99. 1999 Southwest Symposium on*, pp. 58 –62, 1999.

[33] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley and Sons, Inc., ISBN 978-0-0-471-14448-9. Univ. of Toronto, 1997.

[34] R. Schreier, "Delta-Sigma Toolbox," 2010. [Online]. Available: `http://www.mathworks.com/matlabcentral/fileexchange/19`.

[35] D.-H. Lee, C.-C. Li, and T.-H. Kuo, "High-speed low-complexity implementation for data weighted averaging algorithm[Sigma-Delta modulator applications]," in *ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on*, pp. 283 – 286, 2002.

[36] TSMC, "TSMC 0.18μm Process 1.8V SAGE-X Standard Cell Library Databook," *Rev. 4.1*, Sept. 2003.

[37] B. Hernes, "Internal correspondance; power estimates for flash quantizer," *Hittite*, 4/18/2011.

[38] I. Løkken, "Digital-to-Analog Conversion in High Resolution Audio," 2008. Doctoral Theses at NTNU, Norwegian University of Science and Technology, Department of Electronics and Telecommunications.

[39] R. Kaald, "Internal correspondance; capacitor values," *Hittite*, 4/4/2011.

A 3^{rd} order unscaled, scaled and ELD compensated coefficients

	Ideal				ELD compensated	
Coeff.	*FB unscaled*	*FB scaled*	*FF unscaled*	*FF scaled*	*FB*	*FF*
a_1	0.1625	0.1897	1.0131	2.5041	0.1897	2.6641
a_2	0.5763	0.2557	0.5763	1.7465	0.2652	2.1632
a_3	1.0131	0.3531	0.1567	1.4336	0.3275	2.0104
g_1	0.0058	0.0074	0.0058	0.0175	0.0095	0.0227
b_1	0.1625	0.1897	1	0.4046	0.1897	0.4958
c_1	1	0.3802	1	0.4046	0.3473	0.4958
c_2	1	0.7854	1	0.8157	0.6117	0.6101
c_3	1	2.8693	1	0.3311	4.0329	0.2547
a_0					0.5818	0.5818

Table 14: Scaled coefficients for the ELD compensated 3^{rd} order modulator defined in section 2.3.1

B Noise density voltages and budget for the 5^{th} order structures

Source	*E1*	*E2*	*E3*	*E4*	*E5*	*EQ*	
$V_{ni,DAC}(f)$	30.7	28.6	33.8	39.7	58	150	nV
$V_{ni,R}(f)$	34.1	19.6	25	25.6	34	26.6	nV
$V_{ni,OpAmp}(f)$	2.34	2.8	3.96	5.24	7.41	10.5	nV
$V_{ni}(f)_{tot}$	2.11	1.21	1.79	2.26	4.57	23.4	fV^2
$P_{ni}\,(V_{ni}^2(f)_{tot} \cdot f_B)$	5.3	3.02	4.47	5.64	11.43	58.4	nV^2
Increase ref. $E1$	0	-4.84	-1.45	0.57	6.7	20.1	dB

(a) 5^{th} order FB

Source	*E1*	*E2*	*E3*	*E4*	*E5*	*EQ*	
$V_{ni,DAC}(f)$	35.6	0	0	0	0	150	nV
$V_{ni,R}(f)$	39.6	46.5	46.6	63.6	78	119	nV
$V_{ni,OpAmp}(f)$	5.11	12.5	12.5	12.5	12.5	10.5	nV
$V_{ni}(f)_{tot}$	2.86	2.32	2.32	4.2	6.24	36.8	fV^2
$P_{ni}\,(V_{ni}^2(f)_{tot} \cdot f_B)$	7.16	5.8	5.8	10.5	15.6	92.1	nV^2
Increase ref. $E1$	0	-1.83	-1.81	3.31	6.75	22.2	dB

(b) 5^{th} order FF

Table 15: Noise density voltages for the 5^{th} order structures

	E1	*E2*	*E3*	*Remaining*	*Total*	
$P_{ntot}[P_{ni} \cdot NG_i]$	5.3	1.36	0.7	0.07	7.41	nV^2
Share	65.5	16.9	8.58	0.91	91.9	%
SNR	75.83	81.7	84.66	94.4	74.36	dB

(a) 5FB

	E1	*Remaining*	*Total*	
$P_{ntot}[P_{ni} \cdot NG_i]$	7.16	0.22	7.38	nV^2
Share	88.8	2.8	91.6	%
SNR	74.5	89.5	74.38	dB

(b) 5FF

Table 16: Circuit noise budget, 5^{th} order structures. The remaining column represent stage E4, E5 and EQ in the FB structure and stage E2, E3, E4, E5, EQ in the FF

C Integrator specifications for the 5^{th} order structures

Spec	*Int 1*	*Int 2*	*Int 3*	*Int 4*	*Int 5*	*Sum*	*Unit*
A_0	40	”	”	”	”	”	dB
GBW	320	320	320	320	320	1600	MHz
Int Cap	10	7	3.5	2	1	0.1	pF
C_C	2	1.4	0.7	0.4	0.2	0.02	pF
g_{m1}	4	2.8	1.4	0.8	0.4	0.2	mS
g_{m5}	40	28	14	8	4	0.24	mS
I_{D1}	268	187.6	94	53.6	26.8	13.4	uA
I_{D2}	2680	1875	940	536	268	15.77	uA

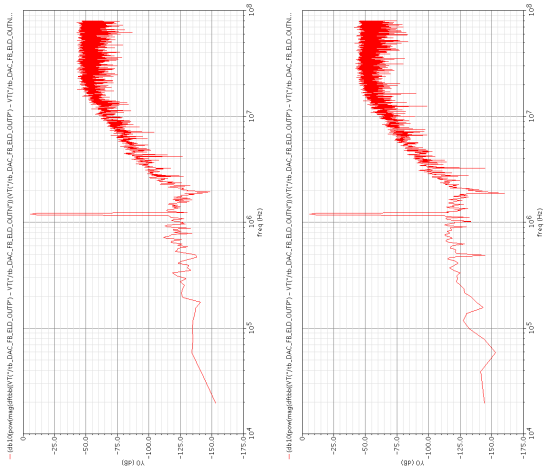
(a) 5^{th} order FB

Spec	*Int 1*	*Int 2*	*Int 3*	*Int 4*	*Int5*	*Sum*	*Unit*
A_0	40	”	”	”	”	”	dB
GBW	320	320	320	320	320	1600	MHz
Int Cap	2.1	0.35	0.35	0.35	0.35	0.1	pF
C_C	0.42	0.07	0.07	0.07	0.07	0.02	pF
g_{m1}	0.84	0.14	0.14	0.14	0.14	0.2	mS
g_{m5}	8.4	1.4	1.4	1.4	1.4	0.083	mS
I_{D1}	56.3	94	94	94	94	13.4	uA
I_{D2}	563	940	940	940	940	5.6	uA

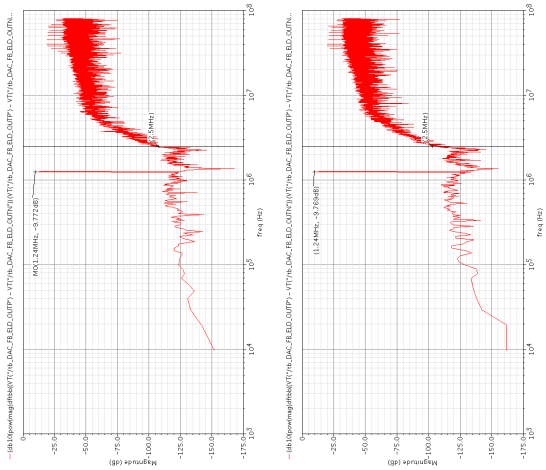
(b) 5^{th} order FF

Table 17: Specification of the integrators for the 5^{th} order structures. Recall g_{m2}, I_{D2} is dependent on β for the summation amplifier

D Ideal spectras for the 3^{rd} FB/FF and 5^{th} FB/FF



(a) Ideal 3^{rd} order FB **(b)** Ideal 3^{rd} order FF



(c) Ideal 5^{th} order FB **(d)** Ideal 5^{th} order FF

Figure 32: Spectra for the ideal structures showing the resonator notches with $OSR = 32$, $P_{sig,3^{\text{rd}}} = -1dBFS$ and $P_{sig,5^{\text{th}}} = -5dBFS$, $f_{in} = 1240282$, $f_S = 160006144$ and $NBPT = 16384$

E Schematics testbench

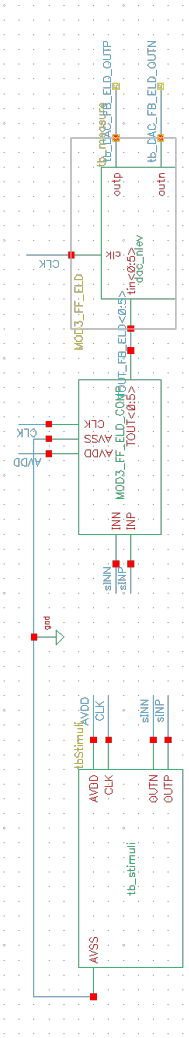
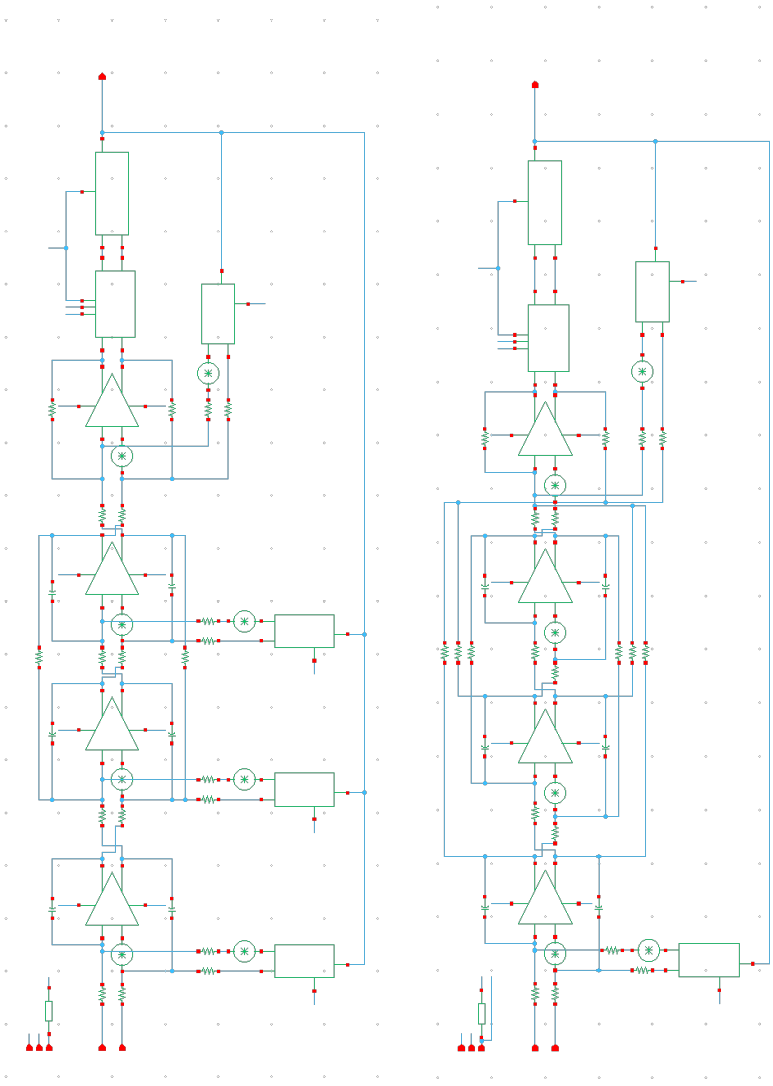


Figure 33: Cadence Virtuoso Schematic of the testbench including the stimuli, modulator and measurement block

E.1 Schematic 3rd order FB modulator



(a) 3rd order FB **(b)** 3rd order FF

Figure 34: Cadence Virtuoso Schematic of a 3rd order FB/FF modulator with noise sources and ELD compensation

F Circuit dimensioning and equations

Finding GBW_2 of the summing amplifier with resistive feedback loop

$$\beta_{FB} = \frac{R_{IN}}{R_{IN} + R_{SUM}} \overset{3rd}{\rightarrow} \frac{R_{c3}}{R_{c3} + R_{Sum}}$$
$$\beta_{FF} = \frac{R_{IN}}{R_{IN} + R_{SUM}} \overset{3rd}{\rightarrow} \frac{R_{INeq}}{R_{INeq} + R_{Sum}}$$
$$\frac{GBW_{SUM2}}{GBW} = \beta$$
$$g_{m2} = GBW_{SUM2} \cdot 2\pi C_L$$

Finding GBW_2 and Miller capacitor C_C from a preset phase margin of 60°.

$$f_{p_1} \cong \frac{1}{2\pi R_1 G_{m_2} R_2 C_C}$$
$$f_{p_2} \cong \frac{G_{m_2}}{2\pi C_L}$$
$$f_Z \cong \frac{G_{m_2}}{2\pi C_C}$$
$$|A_v| = A_1 A_2 = G_{m_1} G_{m_2} R_1 R_2$$
$$f_t = |A_v| f_{p_1} = \frac{G_{m_1}}{2\pi C_C}$$
$$f_z \geq 10 \cdot f_t, PM = 60°$$
$$PM = 180 - tan^{-1}(\frac{f_t}{f_{p_1}}) \left(= tan^{-1}(A_v) = 90°\right) - tan^{-1}(\frac{f_t}{f_{p_2}}) - tan^{-1}(\frac{f_t}{f_z} = 0.1)$$
$$f_{p_2} = 2.2 GBW_1$$
$$g_{m_2} > 10 g_{m_1}$$
$$C_C > 0.22 C_L$$

F.1 Synthesis: Noise gain MATLAB code

./Appendix/NoiseGain.m

```
%% Master thesis, Lars Rypestøl, NTNU Spring 2011
% Noise transfer functions
% Noise gain estimation
close all, clear all, format compact

%Plot settings
P = bodeoptions; % Set phase visiblity to off and frequency units to
     Hz in options
P.PhaseVisible = 'off';
P.FreqUnits = 'Hz'; % Create plot with the options specified by P
P.MagScale='linear';
P.FreqScale='log';
P.xlim=[0.001 0.5];
P.ylim=[-150 20];
P.Grid='on';
fs=160e6;
[f1 f2] = ds_f1f2(32,0);
w = linspace(0.001*2*pi,2*pi*(1/(2*32)),100);

%% 3rd FB
disp('------- 3rd FB')
%Collect ABCD state-space with coefficients
[Acs,Bcs,Ccs,Dc,a,b,c,g,umax]=ABCD(3,32,2,7,'FB','CIFB',1.25e6);
H=tf(ss(Acs,Bcs(:,2),Ccs,Dc(1)));
%EQ
NTF=1/(1-H);
sEQ=sigma(NTF,w);
rmsEQ=dbv(norm(sEQ)/sqrt(100));

%E1 transfer function
B=[b(1) 0 0]'; D=[0];
NTF_INT1=tf(ss(Acs,B,Ccs,D));
gain_INT1=NTF_INT1*NTF;
%Integrating
sE1=sigma(gain_INT1,w);
%Noise gain
rmsE1=dbv(norm(sE1)/sqrt(100))

%E2 transfer function
B=[0 c(1) 0]';
NTF_INT2=tf(ss(Acs,B,Ccs,D));
gain_INT2=NTF_INT2*NTF;
sE2=sigma(gain_INT2,w);
rmsE2=dbv(norm(sE2)/sqrt(100))

%E3 transfer function
```

```
B=[0 0 c(2)]';
NTF_INT3=tf(ss(Acs,B,Ccs,D));
gain_INT3=NTF_INT3*NTF;
sE3=sigma(gain_INT3,w);
rmsE3=dbv(norm(sE3)/sqrt(100))

%No optimization NTFQ, setting resonator to zero
Acs(2,3)=0;
H2=tf(ss(Acs,Bcs(:,2),Ccs,Dc(1)));
NTF2=1/(1-H2);
sEQ2=sigma(NTF2,w);
rmsEQ2=dbv(norm(sEQ2)/sqrt(100))
% Plotting
figure, bodemag(NTF,gain_INT1,'--',gain_INT2,gain_INT3,P)%bodemag(
    NTF, NTF2,'--',P)%
%legend('NTF_{Q, Opt}','NTF_Q','Location','SouthEast')
legend('NTF_Q','STF','E2','E3','Location','SouthEast')
title('3rd order FB modulator - Noise transfer functions')
line([1/(2*32); 1/(2*32)],[50 ; -350],'LineWidth',1)
line([0.001 1/(2*32)],[rmsEQ; rmsEQ])
%line([0.001 1/(2*32)],[rmsEQ2; rmsEQ2],'LineStyle','--')
line([0.001 1/(2*32)],[rmsE3; rmsE3])
line([0.001 1/(2*32)],[rmsE2; rmsE2])
line([0.001 1/(2*32)],[rmsE1; rmsE1])
text(1/60,rmsEQ,'NG_{Q, Opt}','FontSize',8)
% text(1/60,rmsEQ2,'NG_{Q}','FontSize',8)
text(0.0011,rmsE3+4,'NG_3','FontSize',8)
text(0.0011,rmsE2+4,'NG_2','FontSize',8)
text(0.0011,rmsE1+4,'NG_{STF}','FontSize',8)

%% 3rd FF
disp('------- 3rd FF')
[Acs,Bcs,Ccs,Dc,a,b,c,g,umax]=ABCD(3,32,2,7,'FF','CIFF',1.25e6);
H=tf(ss(Acs,Bcs(:,2),Ccs,Dc(1)));
%EQ
NTF=1/(1-H);
sEQ=sigma(NTF,w);
rmsEQ=dbv(norm(sEQ)/sqrt(100))
%E1
B=[b(1) 0 0]'; D=[0];
NTF_INT1=tf(ss(Acs,B,Ccs,D));
gain_INT1=NTF_INT1*NTF;
sE1=sigma(gain_INT1,w);
rmsE1=dbv(norm(sE1)/sqrt(100))
%E2
B=[0 c(2) 0]';
NTF_INT2=tf(ss(Acs,B,Ccs,D));
gain_INT2=NTF_INT2*NTF;
sE2=sigma(gain_INT2,w);
rmsE2=dbv(norm(sE2)/sqrt(100))
%E3
B=[0 0 c(3)]';
```

```
97 NTF_INT3=tf(ss(Acs,B,Ccs,D));
   gain_INT3=NTF_INT3*NTF;
99 sE3=sigma(gain_INT3,w);
   rmsE3=dbv(norm(sE3)/sqrt(100))
101 % Plotting
   figure, bodemag(NTF,gain_INT1,'--',gain_INT2,gain_INT3,P)
103 legend('NTF','STF','E2','E3','Location','SouthEast')
   title('3rd order FF modulator - Noise transfer functions')
105 line([1/(2*32); 1/(2*32)],[50 ; -350],'LineWidth',1)
   %% 5th FB
107 disp('------- 5th FB')
   [Acs,Bcs,Ccs,Dc,a,b,c,g,umax]=ABCD(5,32,1.5,2,'FB','CIFB',1.25e6);
109 H=tf(ss(Acs,Bcs(:,2),Ccs,Dc(1)));
   %EQ
111 NTF=1/(1-H);
   sEQ=sigma(NTF,w);
113 rmsEQ=dbv(norm(sEQ)/sqrt(100))
   %E1
115 B=[b(1) 0 0 0 0]'; D=[0];
   NTF_INT1=tf(ss(Acs,B,Ccs,D));
117 gain_INT1=NTF_INT1*NTF;
   sE1=sigma(gain_INT1,w);
119 rmsE1=dbv(norm(sE1)/sqrt(100))
   %E2
121 B=[0 c(1) 0 0 0]';
   NTF_INT2=tf(ss(Acs,B,Ccs,D));
123 gain_INT2=NTF_INT2*NTF;
   sE2=sigma(gain_INT2,w);
125 rmsE2=dbv(norm(sE2)/sqrt(100))
   %E3
127 B=[0 0 c(2) 0 0]';
   NTF_INT3=tf(ss(Acs,B,Ccs,D));
129 gain_INT3=NTF_INT3*NTF;
   sE3=sigma(gain_INT3,w);
131 rmsE3=dbv(norm(sE3)/sqrt(100))
   %E4
133 B=[0 0 0 c(3) 0]';
   NTF_INT4=tf(ss(Acs,B,Ccs,D));
135 gain_INT4=NTF_INT4*NTF;
   sE4=sigma(gain_INT4,w);
137 rmsE4=dbv(norm(sE4)/sqrt(100))
   %E5
139 B=[0 0 0 0 c(4)]';
   NTF_INT5=tf(ss(Acs,B,Ccs,D));
141 gain_INT5=NTF_INT5*NTF;
   sE5=sigma(gain_INT5,w);
143 rmsE5=dbv(norm(sE5)/sqrt(100))
   % Plotting
145 figure, bodemag(NTF,gain_INT1,'--',gain_INT2,gain_INT3,gain_INT4,
       gain_INT5,P)
   legend('NTF','STF','E2','E3','E4','E5','Location','SouthEast')
147 title('5th order FB modulator - Noise transfer functions')
```

```
    line([1/(2*32); 1/(2*32)],[50 ; -350],'LineWidth',1)
149
    %% 5th FF
151 disp('------- 5th FF')
    [Acs,Bcs,Ccs,Dc,a,b,c,g,umax]=ABCD(5,32,1.5,2,'FF','CIFF',1.25e6);
153 H=tf(ss(Acs,Bcs(:,2),Ccs,Dc(1)));
    %EQ
155 NTF=1/(1-H);
    sEQ=sigma(NTF,w);
157 rmsEQ=dbv(norm(sEQ)/sqrt(100))
    %E1
159 B=[b(1) 0 0 0 0]'; D=[0];
    NTF_INT1=tf(ss(Acs,B,Ccs,D));
161 gain_INT1=NTF_INT1*NTF;
    sE1=sigma(gain_INT1,w);
163 rmsE1=dbv(norm(sE1)/sqrt(100))
    %E2
165 B=[0 c(2) 0 0 0]';
    NTF_INT2=tf(ss(Acs,B,Ccs,D));
167 gain_INT2=NTF_INT2*NTF;
    sE2=sigma(gain_INT2,w);
169 rmsE2=dbv(norm(sE2)/sqrt(100))
    %E3
171 B=[0 0 c(3) 0 0]';
    NTF_INT3=tf(ss(Acs,B,Ccs,D));
173 gain_INT3=NTF_INT3*NTF;
    sE3=sigma(gain_INT3,w);
175 rmsE3=dbv(norm(sE3)/sqrt(100))
    %E4
177 B=[0 0 0 c(4) 0]';
    NTF_INT4=tf(ss(Acs,B,Ccs,D));
179 gain_INT4=NTF_INT4*NTF;
    sE4=sigma(gain_INT4,w);
181 rmsE4=dbv(norm(sE4)/sqrt(100))
    %E5
183 B=[0 0 0 0 c(5)]';
    NTF_INT5=tf(ss(Acs,B,Ccs,D));
185 gain_INT5=NTF_INT5*NTF;
    sE5=sigma(gain_INT5,w);
187 rmsE5=dbv(norm(sE5)/sqrt(100))
    % Plotting
189 figure, bodemag(NTF,gain_INT1,'--',gain_INT2,gain_INT3,gain_INT4,
        gain_INT5,P)
    legend('NTF','STF','E2','E3','E4','E5','Location','SouthEast')
191 title('5th order FF modulator - Noise transfer functions')
    line([1/(2*32); 1/(2*32)],[50 ; -350],'LineWidth',1)
```

F.1.1 ABCD CT state space, continuous to discrete transformation

./Appendix/ABCD.m

```
function [Acs,Bcs,Ccs,Dc,a,b,c,g,umax2,LFc]=ABCD(order,osr,obg,nlev,
    form,typ,ftest)
%% ABCD CT state space, discrete to continuous time transformation
NTF=synthesizeNTF(order,osr,1,obg,0);
%% Parameter
x_ampl_inn_max=0.9; %Fullscale 1.8V
%[fin,fs]=primfreq(ftest,160e6,4096,0);
test_freq=1210953/160002048;
tdac=[0.5 1.5]; %ELD delay 0.5Ts
%ABCD matrix, realize NTF in CT
[ABCDc,tdac2]=realizeNTF_ct(NTF, form, tdac);
[Ac Bc Cc Dc] = partitionABCD(ABCDc);
%Loop filter desciption
LFc = ss(Ac, Bc, Cc, Dc);
% Map CT to DT equivalent
[LF, Gp] = mapCtoD(LFc,tdac2);
%LF=d2d(LF,)
ABCD = [LF.a LF.b; LF.c LF.d];
%Scale discrete ABCD
[ABCDs,umax2,S] = scaleABCD(ABCD,nlev,test_freq,1,[],x_ampl_inn_max
    ,[]);
S = S(1:order,1:order); % Don't worry about the extra states used in
     the d-t model
%Sinv = inv(S);
% Acs=S*Ac*Sinv; Bcs=S*Bc;  Ccs=Cc*Sinv;
Acs=S*Ac/S; Bcs=S*Bc;  Ccs=Cc/S;
ABCDcs = [Acs Bcs; Ccs Dc];
%Obtain scaled coefficients
[a,g,b,c]=mapABCD(ABCDcs, typ);
```