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A 2.4 GHz Ultra-Low-Power Low-Noise-Amplifier

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Problem Description

The low-noise amplifier (LNA) is a special type of electronic amplifier used to amplify very weak signals captured by an antenna. It is often located very close to the antenna, so that losses in the feed line become less critical. LNA is a key component, which is placed at the front-end of a radio receiver circuit. Using an LNA, the noise of all the subsequent stages is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible so that the retrieval of this signal is possible in the later stages in the system. Wireless applications are almost by definition battery powered devices. Power consumption is therefore a major concern for the LNA. The focus of the task is to find an LNA architecture which gives ultra low power consumption. Different LNA solutions should be considered to find the optimal solution in this respect.

Assignment given: 15. January 2010
Supervisor: Trond Ytterdal, IET

Abstract

This master thesis presents the search for and design of a 2.4 GHz ultra-low-power Low Noise Amplifier. The design is carried out in TSMCs 90 nanometer CMOS technology. The design combines current reuse with g_m-boosting and consists of a current-biased inverter utilized as a common gate LNA. The amplifying transistors are voltage-biased with replica biasing. The LNA included biasing draws 200 μA from a 1.2 V powersupply, produces over 20 dB of voltage gain between 2.32 and 2.5 GHz, have an input match of -9.5 dB, an IIP3 of -15.5 dBm and a noise figure of 4.65 dB.

Acknowledgements

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1. Introduction

The demand for low power applications is increasing as technology scales down and more and more applications become battery operated. The reduction of power consumption is therefore an important aspect of winning marked shares. In ordinary circuits the power consumption are going down as technology moves towards finer geometries. In Radio Frequency circuits this reduction in power consumption has not taken place in the same manner. In other words, there should be some potential to reduce the power consumption in RF-circuits.

A recently established Norwegian company, Energy® Micro [3], has introduced a very power efficient microcontroller, the EFM®32 Gecko. The power consumption in this microcontroller is reduced by a factor of four compared to its competitors. This microcontroller is currently without a radio system. A press release [1] [2] from Energy® Micro states that they will incorporate a radio system on their microcontroller. The goal in terms of power consumption for the radio system is to reduce it with a factor of four, compared to other available and comparable systems.

This thesis is a result of an assignment given from Energy® Micro. The assignment was to design an ultra low power Low Noise Amplifier which could contribute to fulfill the demanding restraints in power consumption for the future radio systems on their microcontrollers. A complete design of a LNA is too big an assignment for this master thesis. The goal for the thesis is therefore to show that it is possible to reduce the power consumption in RF circuits and still achieve applicable performance by doing a preliminary design of a LNA.

The LNA is an important component in a radio system. Figure 1 shows a typical receiver structure, with antenna, input filter, LNA, mixer, LP-filter, intermediate frequency amplifier and A/D-converter. The purpose of the LNA is to buffer and amplify the weak radio signals for further signal processing, while adding as little noise and distortion as possible. According to Friis formula [4], this will give more relaxed demands in terms of noise contribution for the latter stages. Friis formula applied to a typical receiver chain, rewritten by means of the first active stage, the LNA, yields the total noise figure in the chain as:

$$F_{TOT} = F_{LNA} + \frac{F_{REST} - 1}{G_{LNA}} \tag{1.1}$$

where F_{LNA} is the noise figure of the LNA, F_{REST} is the noise figure of the subsequent stages and G_{LNA} is the gain in the LNA.

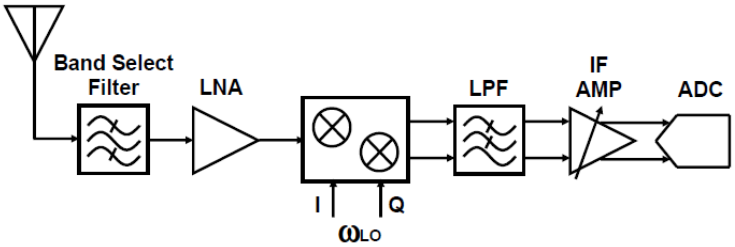


Figure 1: Typical receiver structure [7].

Key parameters with targets for the LNA designed in this thesis are listed in Table 1. The current consumption is the most important parameter.

Key parameters	Target
Current consumption	200 µA
Gain	20 dB
IIP3	-20 dBm
Noise figure	< 6dB
Source impedance	50 Ohm
Bandwidth	200 MHz

Table 1: Target features LNA

As the table shows, the targets for IIP3 and NF are quite relaxed when looked at isolated. But with the low current consumption in mind, the figures can be quite challenging to achieve.

This thesis starts with a literature study where important aspects of low power design are reviewed. Different architectures for reported sub mW LNA will also be presented. Next section presents the chosen architecture, sizing of the transistors, biasing and sizing of the passive components. Then a section with simulation results before a section with discussion and conclusions. At the end a short summary are presented.

1.2 Main contributions

In this thesis the design of a new ultra-low-power narrowband LNA is started. The LNA is single ended and set to operate at 2.4 GHz. The proposed LNA combines a common gate amplifier with g_m-boosting and current reuse. An inverter is utilized as a common gate amplifier, and the use of two transformers boost the transconductance of the transistors in the amplifier. The common gate amplifier is biased by two current-sources, and replica biasing is used to apply the needed gate-voltage. This architecture is not yet seen reported in literature.

2. Prior state of the art

In this chapter relevant findings from books and articles will be presented and comment on. The main search engine has been google.scholar.com. The literature is mainly from sources like IEEE.org, Springerlink.com and books on CMOS and RF-CMOS design.

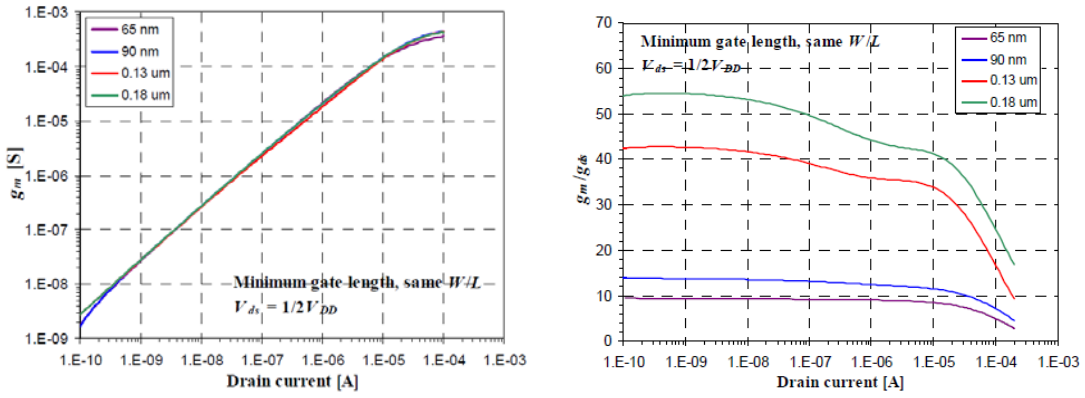
Energy® Micro initially presented a very wide parameter specification in terms of frequency. The frequency band of interest was from 315 MHz to 2.4 GHz. If possible, the LNA should cover the whole frequency band. Since this thesis was done parallel to a preliminary study of RF-systems at Energy® Micro great freedom was given in the search for possible solutions.

The game plan was introductorily to study RF-CMOS, then to search wide for both narrow band LNA, wide band LNA and ultra wide band LNA, combined with low power, current reuse etc, and hopefully end up with a variety of tricks which could be combined to design a LNA that fulfils the requirements.

2.1 General aspects on low power design

The demand for low power operation in analog circuits is increasing due to downscaling in technology and the fact that more and more applications become battery operated. Low power influences the MOSFET transistor in many ways. [13], [14] and [15] are some papers that analyses how the transistor is influenced. The transistor performance can be characterized by many metrics. Some will be commented on in this thesis. The different plots in this passage are all from a lecture in the course TFE09, Low Voltage/Low Power Analog Integrated Circuits. More or less the same plots are found in the before mentioned papers. The plots used in this thesis are more pedagogical and easier to read than those found in the before mentioned papers.

Transconductance does not scale with technology while intrinsic gain degrades as the technology scales down. This can be seen from figure 2.



a) b)

Figure 2: a) Transconductance and b) Intrinsic gain in different technologies [16].

Gate to source and drain to source capacitances are reduced as the technology scales down. This can be seen in figure 3. The transistors used to extract the values are NMOS having minimum drain and source areas and equal W/L-ratio.

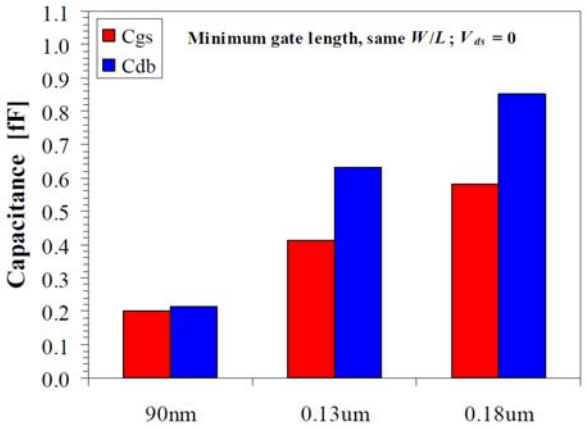


Figure 3: C_{gs} and C_{ds} in different technologies [16].

Maximum operating frequency, f_T, is here defined as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{db})} \tag{2.1}$$

Figure 4 shows two plots, a) f_T as a function of drain current, and b) Drain current as a function of f_T. From figure 2, 3 and 4 one can conclude that there is a potential speed improvement in scaling down the technology since g_m is nearly constant while the capacitances reduces, f_T should increase.

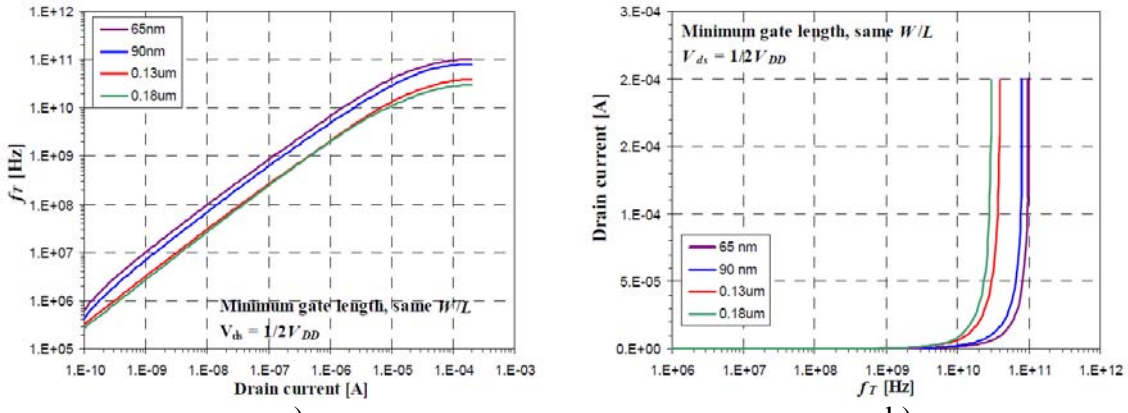


Figure 4: Relationship between f_T and drain current in different technologies [16].

Current efficiency is defined as the ratio between the transconductance and the drain current:

$$\eta_i = \frac{g_m}{I_d} \tag{2.2}$$

In figure 5 the current efficiency is plotted with different technologies. It shows that current efficiency does not scale with technology, but there is a common maximum in weak inversion. The maximum has a numerical value around 27 nearly independent of technology.

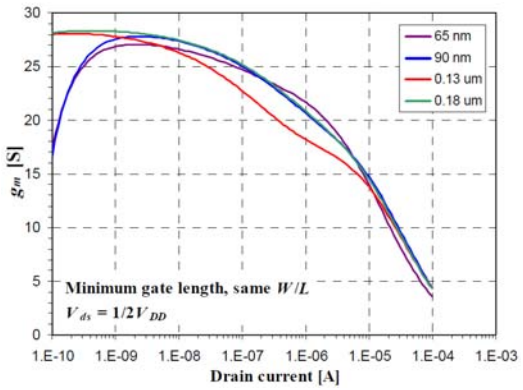


Figure 5: Current efficiency at different technologies [16].

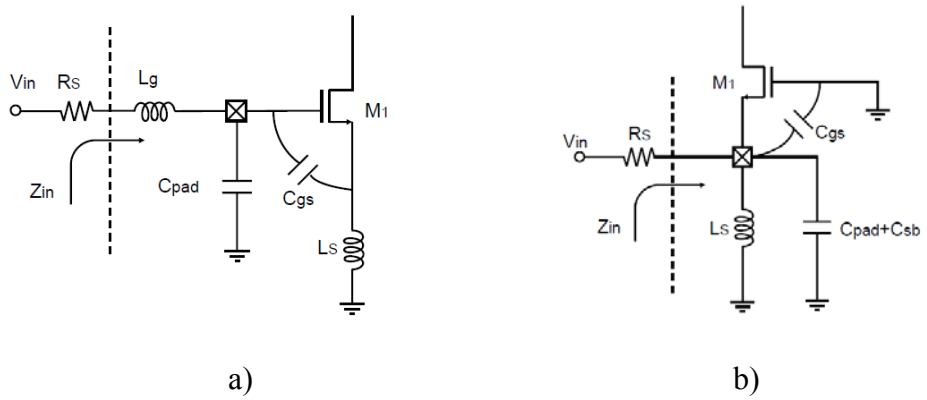
Noise in the transistor increases as the current goes down. It has a minimum in weak inversion [14].

2.2 Low power LNA design

When designing a sub mW LNA there are some aspects worth mentioning. Some of the challenges are presented in [5]. To make a low power LNA it is of course important to keep the current low. This leads to poor performance for the MOSFETs. The choice of topologies is limited due to the downscaling in technology, because the output resistance and the supply voltage are reduced. Onchip passive elements have poor quality factor Q, and has a limited range of values. The article points at four device level properties: 1) there exists characteristic current densities that yield optimal devise transit frequency f_T and unity power gain frequency f_{MAX}; 2) the MOSFET has a large transconductance per unit drain current g_m/I_d in weak inversion; 3) the minimum noise figure decreases as channel length decreases; and 4) MOSFET linearity improves as drain current density increases, with a significant peaking in moderate inversion.

2.3 Common source versus common gate LNA.

There are basically two topologies in LNA-design, the common source amplifier and the common gate amplifier [6]. They can be single ended or differential, come in cascaded versions, and sometimes they are combined in different ways. [7] presents and compares the two basic topologies in a neat and structured way. Figure 6 shows general scheme of the two basic topologies.



a) b)

Figure 6: a) The common source LNA and b) the common gate LNA [7].

2.3.1 Input Matching

For a common source LNA a usual way to obtain the input matching is with inductive degradation. One inductor is placed in series with the source and one in series with the gate. A look at the expression for the input impedance reveals how a 50 Ohm match is made.

$$Z_{in,CS} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \qquad (2.3)$$

The values for Lg and Ls are chosen such that at a desired frequency the two inductors will resonate away C_{gs}, while the last term in the equation creates an ohmic impedance. Since there is no physical ohmic resistance in the input matching network, the input match is noiseless [7].

For the common gate LNA with inductive source degradation, the impedance looking into the source-terminal is $1/g_m$. This provides the possibility of an ohmic input matching only dependent of the transconductance. The source inductor resonates away the capacitance between the source and the gate to provide a pure ohmic input matching. One drawback of the common gate is the presence of a noisy MOSFET channel conductance in the signal path [7].

2.3.2 Noise

The expressions for the noise figure for the two simple LNAs in figure 1 are derived in [7]. The expressions, after some simplification are:

$$F_{\min CS} = 1 + 1.41 \cdot \frac{\gamma}{\alpha} \cdot \frac{\omega}{\omega_T} \tag{2.4}$$

$$F_{\min CG} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m \cdot R_s} \xrightarrow[\frac{1}{g_m} = R_s]{matching} = 1 + \frac{\gamma}{\alpha} \tag{2.5}$$

Where α is a device parameter depending on the channel length, γ is a device parameter depending on V_{ds} and the channel length, and ω_T is the maximum operating frequency of the transistor, here defined as g_m/C_{gs} [6][7]. If one compares the expressions one sees that the noise factor for the common gate is independent of frequency while the noise factor of the common source is a linear function of the ratio between operating frequency ω and ω_T. This feature has made the common gate topology popular in ultra wide band LNAs. Equation (2.5) assumes no gate induced noise since the gate node is shortened to AC-ground. It is easy to see that one can lower the nose factor in the common source by having a large ω_T with respect to ω. To achieve this one would need a large g_m and a small C_{gs}. This is possible with a large drain current.

2.3.3 Gain

The expressions for gain for the two basic topologies derived in [7] are:

$$G_{mCSLNA} = \frac{1}{2R_s} \cdot \frac{\omega_T}{\omega} \tag{2.6}$$

$$G_{mCGLNA} = \frac{1}{2R_s} \tag{2.7}$$

As one can see, the common source LNA has a potential for higher gain than the common gate LNA. The ratio ω_T/ω typically lies between 5~10 [7].

2.3.4 Power consumption

The common source is sensitive to variations of inductance and capacitance in the input matching network. To avoid this problem on can design low-Q input matching network by utilizing a constant g_m optimization approach [7]. This solution usually consumes a high DC-current. Simulations of different common source and common gate topologies show that the common source LNA consumes more power than the common gate LNA [7].

A few more points are discussed in the comparison between the topologies in [7]. The results are summarized in table 2.

	Common source LNA	Common gate LNA
Noise Factor	+	-
Effective Gm	+	-
Power Consumption	-	+
Input Matching	-	+
Parasitic Sensitivity	-	+
Reverse Isolation	-	+

Table 2: Comparison between common source and common gate LNA [7]

2.4 Differential LNAs

Differential amplifiers have some advantages over single ended amplifiers. They usually have higher power supply noise rejection and package parasitics does not influence the operation in the same extent as in single ended amplifiers [26]. [9], [10] and [11] presents different differential LNAs for various purposes. [9] presents a narrowband LNA for IEEE 802.15.4 WSNs, [10] presents a wideband, 1 GHz -10 GHz, LNA and [11] presents a wideband, 170 MHz – 1700 MHz, LNA. The applications they are meant for are not equal, but there is one important common feature for this thesis, that is they all share a relatively high branch current which leads to higher power consumption compared to a single ended LNA.

2.5 Cascaded LNAs

A usual way to obtain gain is by cascading amplifiers [6]. As for differential amplifiers, cascaded amplifiers imply several branches consuming current, and in the end, a high current consumption is the result.

2.6 Four Sub mW LNAs

2.6.1 A 1 GHz single ended common source LNA

A common source LNA that reveals extremely low power consumption is presented in [19]. The LNA is based on sub threshold operation at 1 GHz. The LNA is fabricated in a 0.18 μm CMOS process and has a gain of 13.6 dB while drawing 260 μA from a 1 V supply. An unrestrained bias technique that automatically increases bias currents at high input power levels is used to raise the input referred P1dB to -0.2 dBm. The LNA has a measured noise figure of 4.6 dB and an IIP3 of 7.2 dBm. The architecture is shown in figure 7.

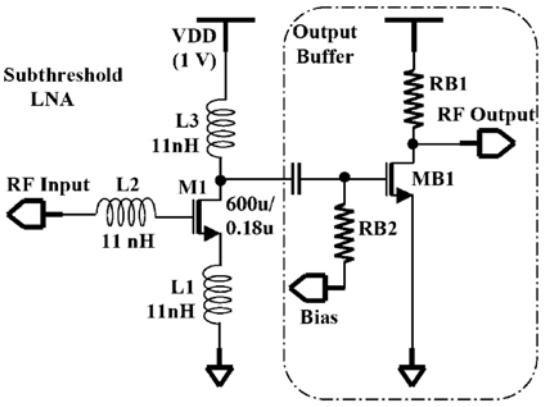


Figure 7: Schematic diagram of the subthreshold LNA and the output buffer [19].

The LNA operates in weak inversion. The challenge when operating in weak inversion is that the transistor has lower f_T and lower transconductance compared to operation in strong inversion. The countermeasures applied in this design is using minimum length to maximize f_T, and using a large width to gain enough transconductance. To counter the large parasitics, and thereby conserve the voltage gain, onchip inductors are utilized to tune out the capacitances associated with the amplifying transistor M1.

2.6.2 The Shunt-Feedback/Common-gate Hybrid differential LNA

A differential amplifier that scores high in terms of low power consumption is presented in [20]. The architecture is based on a common gate amplifier with applied feedback. The amplifier is produced in a 0.13 µm CMOS technology and the key figures are: 13 dB power gain, 3.6 dB noise figure, -15 dB input match, -10 dBm IIP3, 0 – 960 MHz BW and it consumes 720 µW from a 1.2 V supply. The architecture is shown in figure 8.

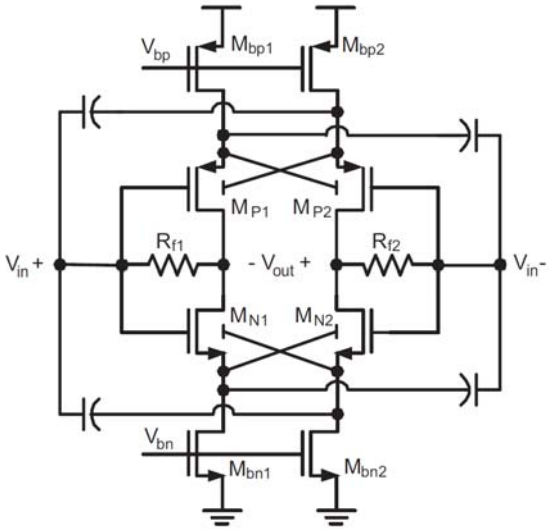


Figure 8: The Shunt-Feedback/Common-Gate Hybrid (SFBCG) amplifier [20].

The goals for the design in [20] have been to lower the power consumption while maintaining a reasonable low noise figure. The applied features to achieve these goals are utilizing current reuse by using both NMOS and PMOS transistors in the common gate, crosscoupling the

inputs to achieve a form of g_m-boosting by utilizing both the common gate and the shunt feedback amplifier, and crossconnecting of the bodies of the transistors to the input nodes to utilize the bodyeffect.

The use of both NMOS and PMOS in a common gate enhances the transconductance to:

$$G_m = g_{mNMOS} + g_{mPMOS} \tag{2.8}$$

The crossconnecting of the inputs results in an input impedance of:

$$Z_{in} \approx \frac{1}{g_{m1} + g_{m2}} = \frac{1}{2g_m} \tag{2.9}$$

Combining the two last equations reveals that on can reduce the current by a factor of 4 and still achieve the same input match as a traditional common gate amplifier, given that the transconductance in the four transistors are equal.

The crossconnecting of the bodies to the opposite source nodes makes the transistors act like dual gate transistors, and the transconductance is further increased from g_m to $g_m + g_{mb}$.

The combination of these three features contributes to maintain a good input match and low noise figure for low currents.

2.6.3 A low voltage 2.4GHz single ended Common gate LNA

Another low power amplifier is presented in [21]. It features a 2.4 GHz common gate amplifier applied with a current reuse technique in 0.18 µm CMOS technology. The key figures of the LNA are: gain 9.6 dB, NF 2.02 db, S_{11} and S_{22} < -20 dB and a DC-power consumption of 460 µW with a supply voltage of 0.6 V. The architecture is shown in figure 9.

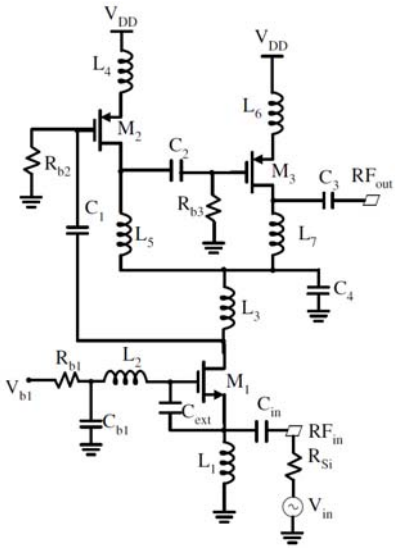
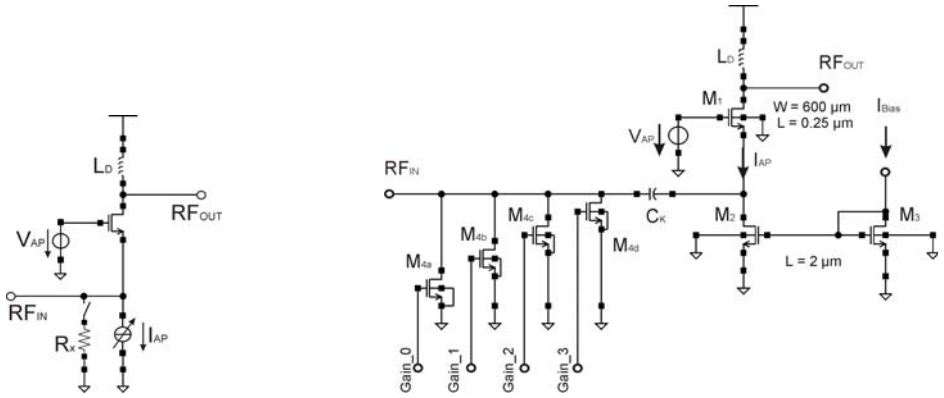


Figure 9: The presented common-gate LNA circuit with current-reuse technique [21].

The architecture can be viewed at as a three stage amplifier where the same current runs through all three stages. The first stage is a common gate amplifier, and the next two stages are common source amplifiers. The choice to use three amplifying stages is reasoned by wanting to compensate for the relatively small gain in a common gate amplifier. The gate inductance to transistor M1 is applied to ensure optimal input matching at the center frequency of interest.

2.6.4 A low power variable gain single ended Common-gate LNA

A low power variable gain common gate LNA is presented in [21]. The amplifier is designed in a 0.25 µm CMOS technology for a center frequency of 868 MHz and achieves the following key figures in maximum gain mode: current consumption 831 µA, gain 12.9 dB, S_{11} -15.51 dB, NF 4.51 dB and IIP3 -6.37 dBm. The principle of operation and the architecture is shown in figure 10 a) and b).



a) b)

Figure 10: Principle of operation a), and realization variable gain CG-LNA b) [21].

The key concept to adjust the gain in this amplifier is to reduce the bias-current and shunt in a resistance to make up for the lost input impedance. The expression for the input impedance when the amplifier operates in a low amplification mode is given by the expression:

$$Z_{in} \approx \frac{1}{g_{m1} + \frac{1}{R_x}} \tag{2.10}$$

The use of four different transistors as resistances gives the opportunity to have 16 different gainsettings. Resistive termination is discussed as very unfavorable for a LNA. But since the solution is only applied to very large input signals, well above the noisefloor, the noiseperformance does not deteriorate. This is derived in the article.

2.7 General aspects on g_m-boosting of common gate LNA

According to table 2, the common source LNA outperforms the common gate LNA with respect to better noise factor and better gain. A way to reduce the noise factor of the common gate LNA is to increase the transconductance. According to equation (2.4) the noise factor can be traded against input matching by increasing the transconductance i.e. increasing the current lowers the input impedance and the noise factor [7]. A more clever way to do this is by inserting an inverting gain between the source and the gate node of the common gate LNA, shown in general in figure 11.

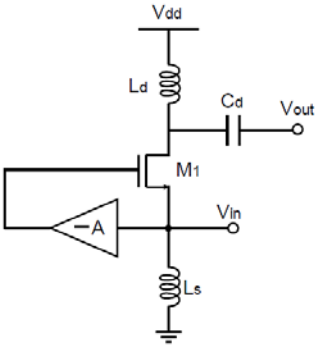


Figure 11: General scheme of g_m-boosted common gate LNA [7].

The architecture in figure 11 is analyzed in [7] and the resulting noise figure after simplification is:

$$F_{\min CG} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{(1+A)^2 g_m \cdot R_s} \xrightarrow[\frac{1}{(1+A)g_m} = R_s]{matching} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+A} \qquad (2.11)$$

Equation (2.11) suggests that an inverting gain between the source node and the gate node clearly reduces the noise figure. Further one can see that since the effective G_m is increased, the power consumption can be reduced by the same factor, while still achieving a good input match. Equation (2.11) also indicates that the noise factor can be reduced to an arbitrary low value as long as A is increased. This is not the case, since the equation does not take into account gate induced noise. Gate induced noise must now be considered since the gate node now no longer are shorted to AC-ground. It will increase with increasing A [8].

2.7.1 Possible implementations of inverting gain A.

In a differential common gate LNA, an inverting gain between source and gate can be implemented by capacitive crossconnecting [8] [26] [28]. Another way to implement the inverting gain is to use an active device like a common source [17] [18]. The drawbacks of an active solution are noise generated in achieving the inverting gain is directly coupled to the gate, in addition to increased power consumption and complexity. Onchip transformers are passive solutions for realizing an inverting gain [7] [8] [28]. The benefits of using a passive device in preference of an active device are negligible extra noise added and no complex biasing or feedback is needed. Figure 12 shows the general scheme of a g_m-boosted common gate LNA with a transformer.

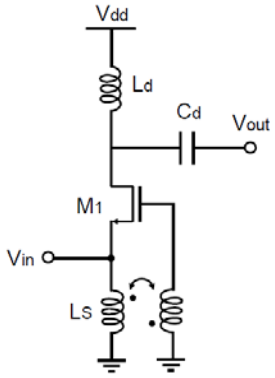


Figure 12: Gm-boosted common gate LNA with transformer [7].

The coupling between the inductors of the transformer ensures the opposite phase between the gate node and the source node of the LNA [8]. A noise analysis of the architecture in figure 12 is performed in [8]. The resulting noise figure, including gate induced noise is:

$$F_{\min CGLNA} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+nk} + \frac{\delta\alpha}{5} \cdot \left(\frac{\omega}{\omega_T}\right)^2 \cdot \frac{(1+2nk+n^2)^2}{(1+nk)^3} \tag{2.12}$$

where n is the turn ratio of the primary to the secondary inductor and k is the coupling coefficient. The inverting gain is in the ideal case made up of nk. If one assumes ideal coupling and turn ratio equal one, (2.12) simplifies to [8]:

$$F_{\min CGLNA} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+nk} + \frac{\delta\alpha}{5} \cdot \left(\frac{\omega}{\omega_T}\right)^2 \cdot (1+n) \tag{2.13}$$

Equation (2.13) shows that an inverting gain between the source node and the drain node reduces the channel noise and increases the gate induced noise. With the derivative of equation (2.13) set equal to zero, one obtains the optimum turn ratio with respect to minimum noise figure as [8]:

$$n_{opt} = \left(\frac{\omega}{\omega_T}\right)^2 \cdot \sqrt{\frac{5\gamma}{\delta\alpha^2}} - 1 \tag{2.14}$$

which is when the cannel-noise-reduction and gate-induced-noise-increment cancel. The corresponding noise figure is [8]:

$$F_{opt} \approx 1 + 2\sqrt{\frac{\delta\gamma}{5}} \cdot \left(\frac{\omega}{\omega_T}\right)^2 \tag{2.15}$$

An interesting observation in (2.13) is the frequency dependency of the noise factor when g_m-boosting is applied. This is due to that the gate-node no longer can be viewed at as AC-ground. An optimum inverting gain A often lies between 2~3, and the coupling coefficient is typically between 0.6~0.9 for onchip transformers [8].

A simple model for the *Q*-factor of an inductor is derived in [6]. This *Q*-factor describes the relationship between the inductor and serial resistance as:

$$Q = \frac{2 \cdot \pi \cdot f \cdot L}{R_s} \tag{2.16}$$

where f is the operating frequency, L is the inductance in Hendry and R_s is the serial resistance in Ohms. Typical *Q*-factor for onchip inductors are in the range from as low as wanted up to around 15 [35]. High *Q*-factor requires the use of special processing steps and is therefore costly and challenging to achieve. A typical value of the *Q*-factor realizable with normal process-steps is up to about 6-8 [32] [35].

2.8 Current reuse

Current reuse is a well known technique to utilize the current in an efficient way. This concept basically consists of using the same current in several components. This literarily means stacking different components instead of cascading. This is very power efficient. A drawback can be lack of voltage headroom. Among many, the LNAs presented in [20], [21], [27] and [29] utilizes this feature.

2.9 Replica biasing

Replica biasing basically consists of a downscaled version of the circuit that is supposed to be biased. The desired bias voltages is generated by diodeconnecting the transistors in the replica branch which corresponds to the transistors in the main branch that needs voltage biasing. This will provide a biasing that is very stable with respect to process variations, because the transistors are equal [12]. Replica biasing is typically used in the design of VCOs, to ensure minimum variation of the frequency in different process corners [24] [25].

2.10 Conclusions

The literature study revealed some interesting aspects and techniques regarding how to design a very low power LNA. Simplicity in design seems to be an important aspect for ultra low power operation [19]. Cascaded topologies naturally have higher power consumption than single stage amplifiers. The stringent current demand in this thesis excludes the use of such a solution.

The low current available excludes in many ways the opportunity to design a wide band amplifier. The relatively low transconductance one gets with 200 μA in accompany with large parasitic capacitances due to large transistors reveals the need for tuning inductances to ensure a sufficient gain at high frequencies. When using inductances to tune out capacitances the resonance frequency is often quite narrow. This is not always the case, but with a low transistor maximum operating frequency, f_T, it will be very difficult to realize a wideband LNA. The chosen frequency for this design is 2.4 GHz.

The g_m-boosted common gate amplifier seems like a promising architecture over different common source amplifiers. When it comes to choosing differential or single ended approach, the choice in this thesis is single ended. Differential approach has some advantages in common gate gm-boosted topologies because of the opportunity to cross-couple the input signals to the gate nodes. A simple calculation of transconductance with (2.2) reveals that a branch current of 100 μA only gives about 2 μS of transconductance at a current efficiency of 20. This is too little transconductance even for the solution presented in [20]. Such a low transconductance in an ordinary differential g_m-boosted solution like the one in [8] would require a boosting gain of minimum 5 to achieve matching with the source impedance in a differential structure. This is somewhat large according to the results derived in the same article.

Operation in weak inversion seems like the only option for the low current available. This mode also gives the least noise when the current is very low. Choosing a length near minimum seems like a good choice due to the fact that the transistor is fastest around minimum length.

An architecture that provides high transconductance for a given current is the inverter structure. If it is used as a common gate amplifier and biased such that both the NMOS- and the PMOS-transistors are on, the total transconductance that contributes to the gain at the output and the input match at the input are the sum of the transconductances according to (2.8). The inverter is also an excellent example of current reuse, since the same bias current runs through both transistors [20].

To get an inverting gain the use of a transformer seems like a good choice. The transformer is a passive device and contributes with almost no additional noise. The only additional noise is ideally from the serial resistance in the inductors.

Replica biasing is proven to be a robust biasing against process variations, and seems like a good choice when it comes to provide the DC-voltages needed in the circuit. This requires excellent matching between the transistors.

The choice of process for this design is 90 nm CMOS from TSMC. The version available at NTNU is a student version, where process parameters are inaccessible. The main reason to choose this process is that it is the only process set up and working with Cadence at NTNU. Figure 2, 4 and 5 shows that there is a substantial difference between 0.18 μm and 90 nm, but smaller differences between 90 nm and 65 nm. 65 nm will probably provide better results and the ability to reduce power consumption even further due to better f_T. This comes with the prize of higher production cost. Another reason to choose 90 nm is a whish from Energy® Micro.

2.10.1 The proposed architecture

The choice of architecture was motivated by trying something that was not yet published. This because no LNAs found in the literature achieves the goals for this thesis. A new combination of current reuse and g_m-boosting seemed like a possible solution worth looking into. The principle of operation of the proposed LNA is shown in figure 13.

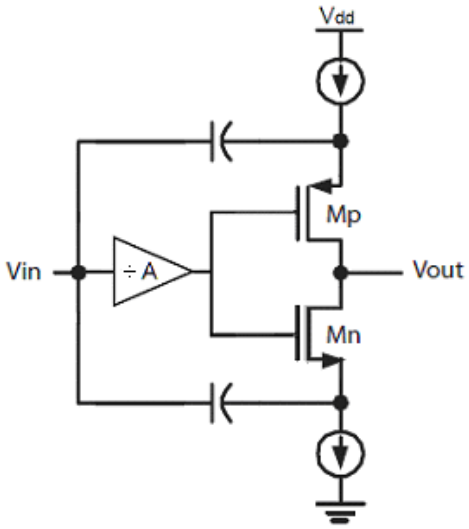


Figure 13: Principle of operation.

The total transconductance available in the circuit is according to equation (2.8): $G_{mTOT} = g_{mNMOS} + g_{mPMOS}$. The effective transconductance in the circuit is according to [7]: $G_m = (1+A)g_m$. This gives an expression for the input impedance as:

$$Z_{in} = \frac{1}{(1+A)G_{mTOT}} \tag{2.17}$$

The intrinsic gain in this amplifier can be expressed like:

$$A_0 = \frac{g_{mNMOS} + g_{mPMOS}}{g_{dsNMOS} \parallel g_{dsPMOS}} \tag{2.18}$$

Expressions for noise figure and linearity are not derived in this thesis.

3. Design

The transistors in this design are simulated with Eldo. Ezwave is used to plot the results from the simulations and some simple post simulation processing to achieve the noise figure of the design. The Optimizer in Eldo is used in finding the different geometries and sizes for the components used in this design. Testbenches used to generate the plots can be viewed in the Appendixes. The libraries used in the simulations are typical, slow-slow, fast-fast, slow-fast and fast-slow.

3.1 The proposed LNA

A detailed figure of the architecture is shown in figure x. The sizes of the components are summarized in table 7 under the passage *Sizing of passive components*.

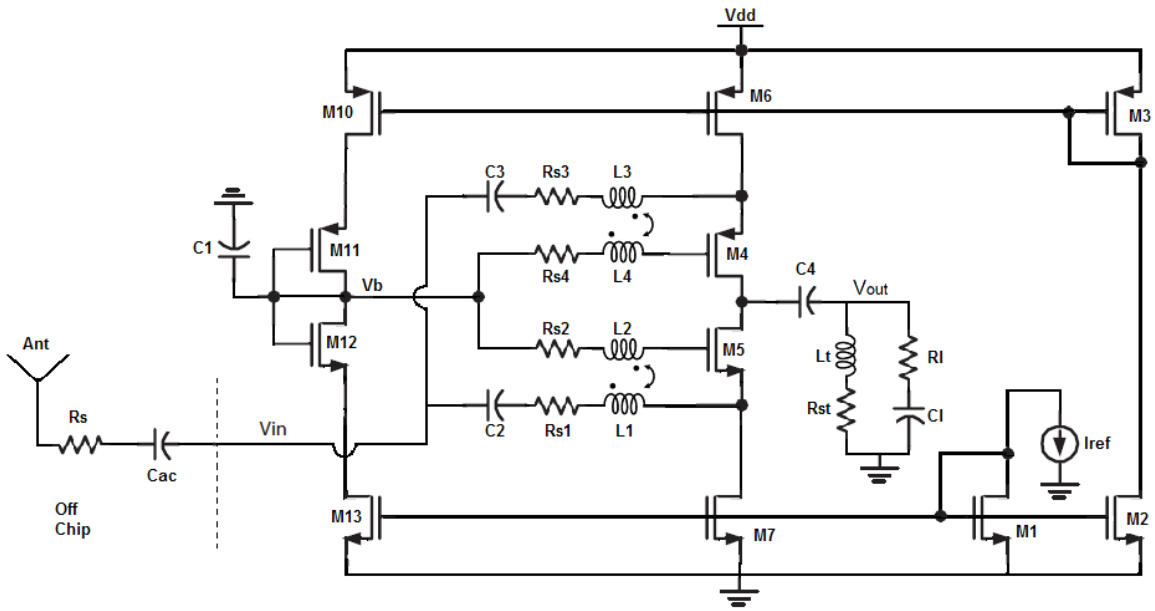


Figure 14: The proposed LNA.

The amplifying transistors are called M4 and M5. M6 and M7 are the current sources providing biasing current. Transistors M1 to M3 are current mirrors used to distribute the reference current I_{ref}. Transistors M10 to M13 form the replica bias branch. Inductors L_1-L_2 and L_3-L_4 are mutual inductors which form the two transformers

3.1.1 Theory of operation

The input signal is connected to the two input nodes of the amplifier through some DC-blocking capacitors and the primary inductors of the transformers. The gate biasing voltage is

connected to the gates through the secondary inductors of the transformers. The transformers invert the phase of the input signal and feed it to the gate nodes at the resonance frequency to provide the g_m-boosting. C_1 is a disconnecting capacitor inserted to provide AC-ground at the biasing node. The output is fed through a DC-blocking capacitor and into the load. A tuning inductor is connected to the output to tune out capacitances connected to the output node.

3.2 Transistor sizing

The goals for sizing the transistors was a total transconductance at about 8-10 μS, as high f_T as possible and as large intrinsic gain as possible. 8-10 μS will require g_m-boosting with an inverting gain around 2. To size the transistors a testbench which simulated on several transistors in parallel was used. The goal for sizing the transistors was to find an optimal ratio between the width and the length that gave a good tradeoff between g_m, g_m/g_{ds}, f_T, $f_T/f*g_m/g_{ds}$ and η_i. For the NMOS transistor a length of 0.15 μm and a W/L-ratio of 5 seemed like a good tradeoff. For the PMOS transistor a length of 0.15 μm and a W/L-ratio of 12 gave a usable result. The results from the simulations are pictured in figure 14 and 15. The definition for f_T used here is rather pessimistic. It includes C_{gd}, C_{gs}, C_{gb} and C_{ds}. The width of the NMOS and PMOS are respectively 0.75 μm and 1.8 μm. The figures depicted in the plots are also summarized in table 3.

The decision to use replica bias assumes the use transistors in parallel in order to achieve matching and thereby robustness for process variations. For a current of 200 μA 200 transistors in parallel was used. This would ideally give the possibility to use as low biasing current as 1 μA. Parallelization of transistors is not an optimal choice for high speed due to larger parasitic capacitances which gives smaller f_T. A similar plot as the one in figure 14 for a single NMOS transistor is showed in figure 16. The gate area is equal for the two cases in figure 14 and figure 16.

The number of fingers in the different transistors is dependent on the width. The maximum width of a finger in this design is 3 μm.

Figure 14, 15 and 16 all have the same setup. The top plot shows g_m, the next shows R_{ds}, the next g_m/ R_{ds}, the next η_i, the next $f_T/f*g_m/g_{ds}$, the next f_T and last f_T/f. All figures are plotted as a function of length. The marker is set at the chosen length, 0.15 μm.

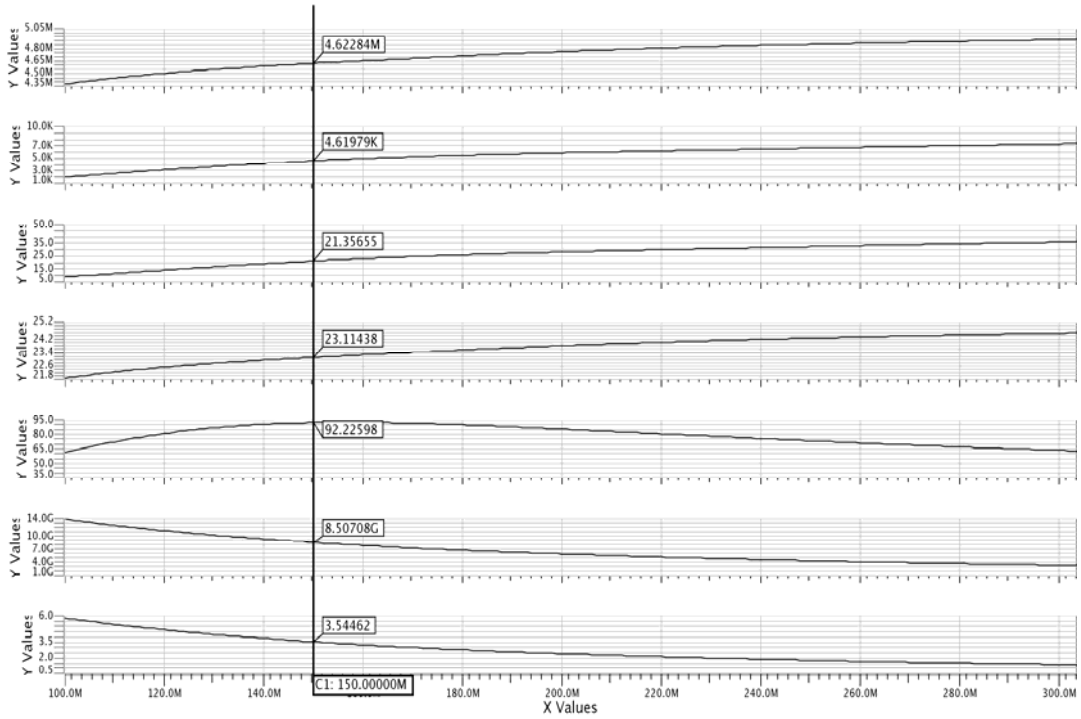


Figure 15: Different figures of merit for a 0.75 µm wide NMOS-transistor as a function of length with *mult* set to 200.

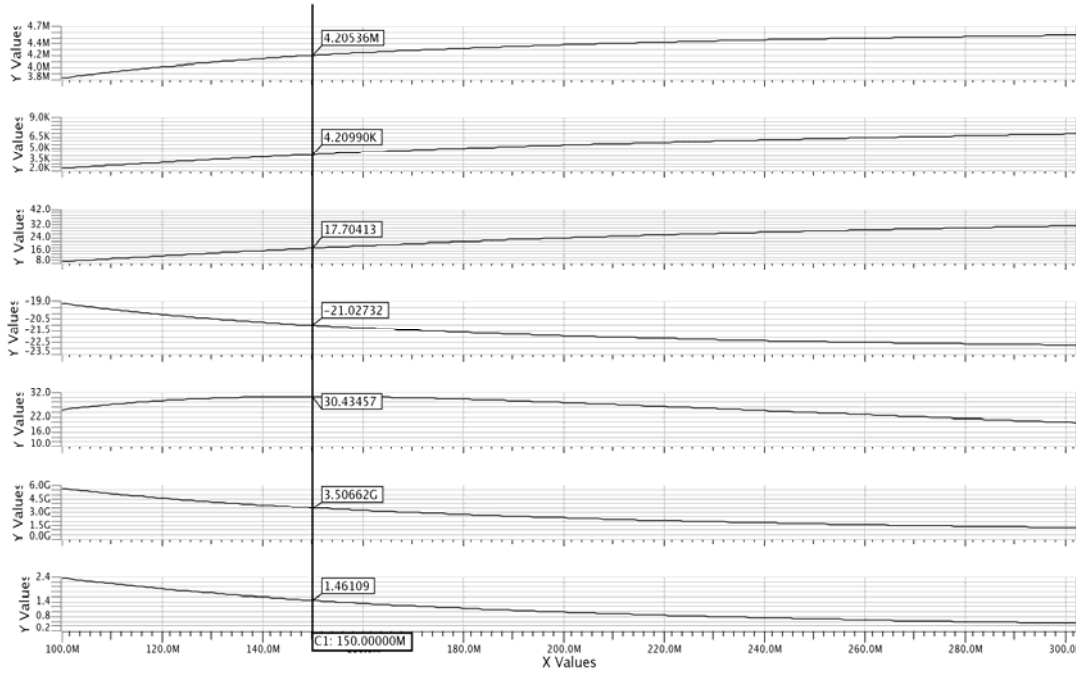


Figure 16: Different figures of merit for a 1.8 µm wide PMOS-transistor as a function of length with *mult* set to 200.

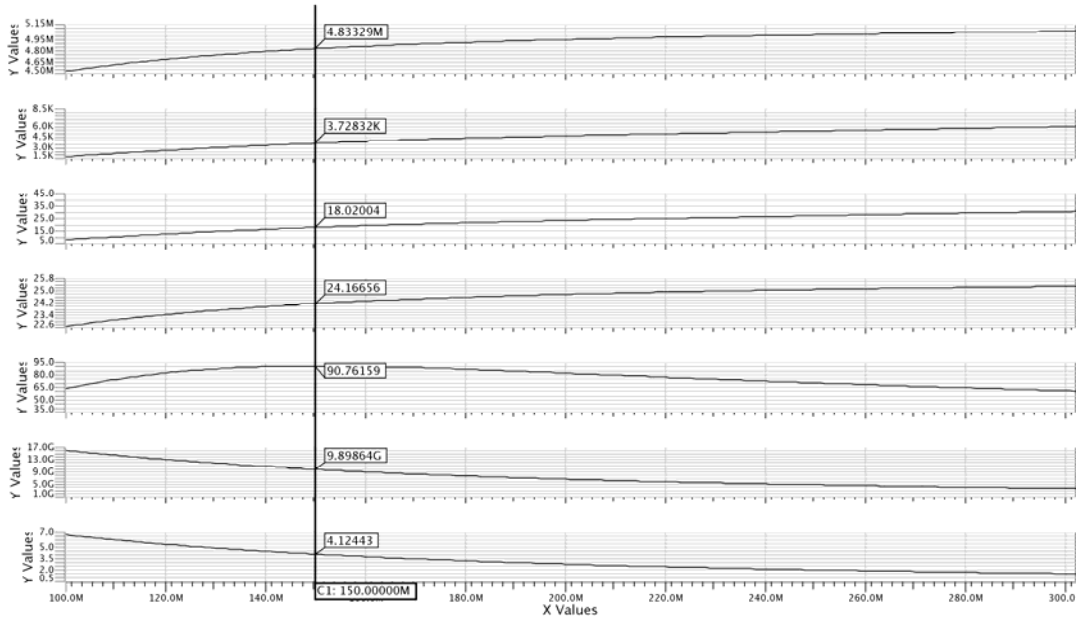


Figure 17: Different figures of merit of a 150 µm wide NMOS-transistor as a function of length.

	NMOS	PMOS	NMOS_1
w (µm)	0.75	1.8	150
l (µm)	0.15	0.15	0.15
mult	200	200	1
nfing	1	1	50
g_m (mS)	4.6	4.2	4.8
R_{ds} (kΩ)	4.6	4.2	3.7
g_m/g_{ds}	21.4	17.7	18.0
η_i	23.1	21.0	24.2
$f_T/f*g_m/g_{ds}$	92.2	30.4	90.8
f_T (GHz)	8.5	3.5	9.9
f_T/f	3.5	1.5	4.1

Table 3: Summary of results from the figures 14, 15 and 16.

f_T is a bit low due to large transistors and small current. A rule of thumb in ordinary IC-design says that one should stay a factor 10 below f_T. According to [6] one can operate with f_{max} larger than f_T when inductors are used to tune out capacitances. The prize to pay is higher noise.

An interesting observation is that $f_T/f*g_m/g_{ds}$ is larger for the setup with many small transistors in parallel than for the setup with one large transistor. The reason for this is larger output resistance in the first setup.

3.3 Biasing

The biasing current available on chip is according to Energy® Micro 2 µA. This current is represented as an ideal current source. The current is fed to a NMOS transistor and mirrored around in the circuit. The amplifying transistors are current-biased by two current-sources, realized as transistors. The sizing of width and length of the current mirrors and current sources was done by using the optimizer in Eldo. To be able to match the transistors the width and length of transistors M1, M2, M3, M6 and M7 was parameterized. One length and width for the NMOS transistors and one length and width for the PMOS transistors were used. The results from the optimizer are summarized in table 4.

The replica biasing for providing the DC gate-voltages for the amplifying transistors was now straight ahead to create by copying the amplifier-branch and scale it down with the multiplication-option in the simulator. Both the replicas of the amplifying transistors are diode-connected. The DC voltage is directly fed to the gates of amplifying transistors M4 and M5. The current mirrors providing DC-bias to the PMOS current-source are scaled down so that the current in the mirror branch is about 1 µA. The current in the replica-branch is about 2 µA while the current in the amplification branch is about 195 µA. The geometries from the sizing are summarized in table 4. Subscript marks NMOS or PMOS.

	$M1_N$	$M2_N$	$M3_P$	$M6_P$	$M7_N$
w (µm)	6.26	6.26	4.66	4.66	6.26
l (µm)	2.21	2.21	1.78	1.78	2.21
mult	2	1	1	200	200
nfing	3	3	2	2	3

Table 4: Geometries for biasing transistors.

After sizing the all the transistors a simple DC-testbench was used to look at respectively g_{m4} and g_{m5}, g_{mTOT}, R_{out}, g_{mTOT}/R_{out} and I_{dM4} and I_{dM5} as a function of biasing voltage V_b for the amplifier. The biasing voltage is represented as an ideal voltage source and connected to the gates of M4 and M5. The plot is shown in figure 17. The plot reveals that the ideal gate biasing voltage is 0.52 V. This gives a total transconductance of 8.65 mS and an intrinsic gain of 19, or 25 dB. The draincurrent in the two amplifying transistors are 195.76 µA.

A simple AC-simulation of the amplifier with replica biasing, without transformers and load, and with capacitors C_1 to C_3 set to 1 F was also performed. This is a very unrealistic scenario, but it shows the potential of the amplifier and the stability of the biasing over different process corners. Figure 18 shows the result from the AC-simulation.

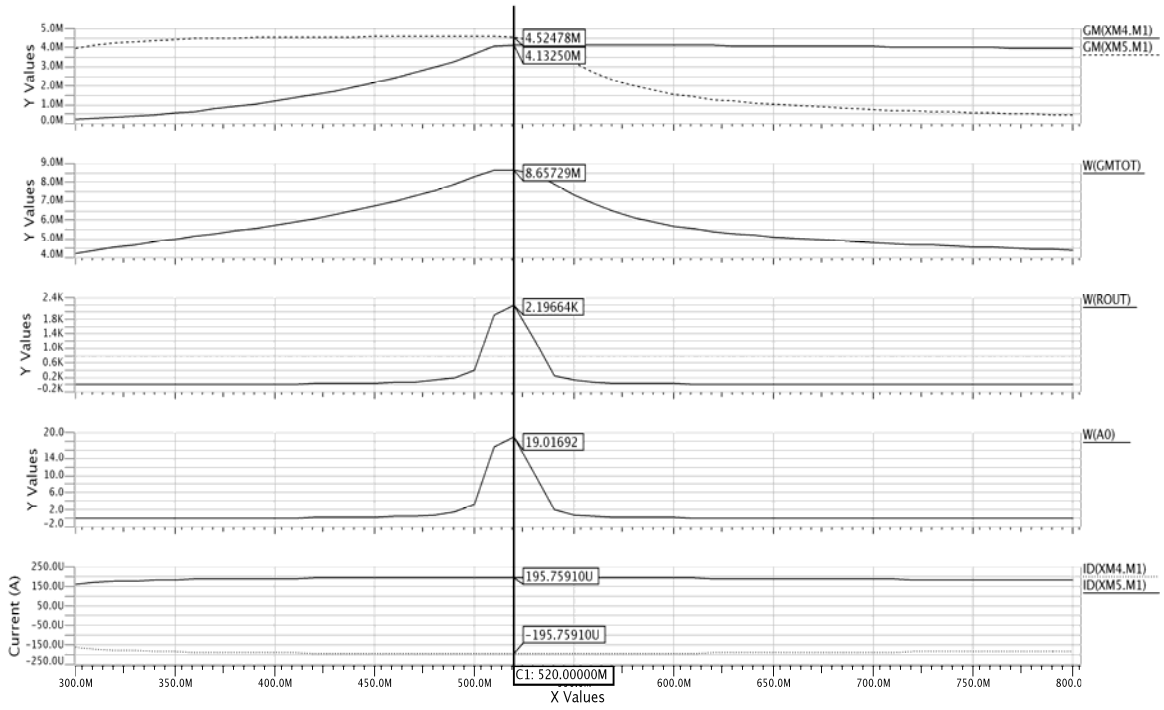


Figure 18: DC-figures of the proposed amplifier.

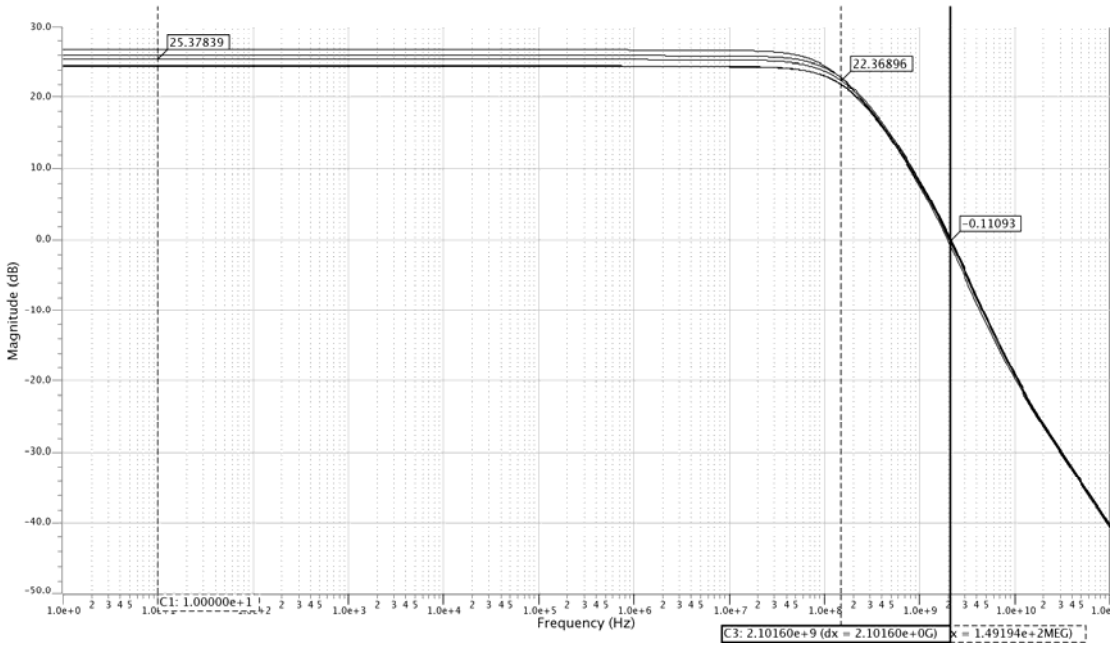


Figure 19: AC simulation of amplifier without load, with replica biasing.

As figure 18 shows, the biasing is fairly stabile for corner simulations. The markers are set on the result from simulating with the typical library. They show a DC gain of 25.4 dB, f_{-3dB} of 160 MHz and f_{0dB} of 2.1 GHz.

3.4 Realistic load

The load, e.g. the input impedance of the subsequent mixer was supposed to be provided by Energy® Micro. This was never provided, so to get a realistic load to the amplifier a PMOS common source stage with NMOS active load was quickly designed. This stage has a f_T of about 10 GHz. The input impedance of this stage was extracted using a port simulation setup in Eldo. The serial input impedance was extracted at frequencies around 2.4 GHz. The results from this simulation are summarized in table 5. This load is used in the simulations. The serial capacitance is somewhat low, but since the gainstage operates with high overdrive it makes sense.

Parameter	Value
R_{series}	145 Ω
C_{series}	32 fF

Table 5: Input impedance extraction from a PMOS common source.

3.5 Sizing of the passive components

The architecture in figure 14 was modeled in spice syntax and simulated with AC-analysis. The complete LNA are shown again for convenience in figure 20. The optimizer was utilized to find suiting component sizes within reasonable limits. The transconductance available in the amplifier is according to equation (2.8) and the results in figure 17 around 8.7 mS. Using the equation for input impedance for the amplifier (2.17) set equal to 50 Ohm reveals the need for an inverting gain of about 1.3 to achieve input matching. This corresponds to 2.3 dB. The goals for the optimizer were set to achieve a 3 dB gain between the source and gate nodes accompanied with a phase difference of 180 degrees. 3 dB is a bit higher than the theoretically needed boosting gain. This is chosen because the bias voltage probably will drop a bit due to the inductors placed between the biasing node V_b and the gates of M4 and M5.

The architecture was initially simulated with a single transformer. The choice was motivated by the wish to keep the numbers of inductors down and thereby save area. This solution made it difficult to simultaneously invert the phase of the signals at both the gate nodes with respect to the source nodes of transistors M4 and M5. This is because there is a substantial difference in the parasitic capacitance at the two inputs. The parasitics associated with the PMOS current source M6 is larger than the parasitics of M7.

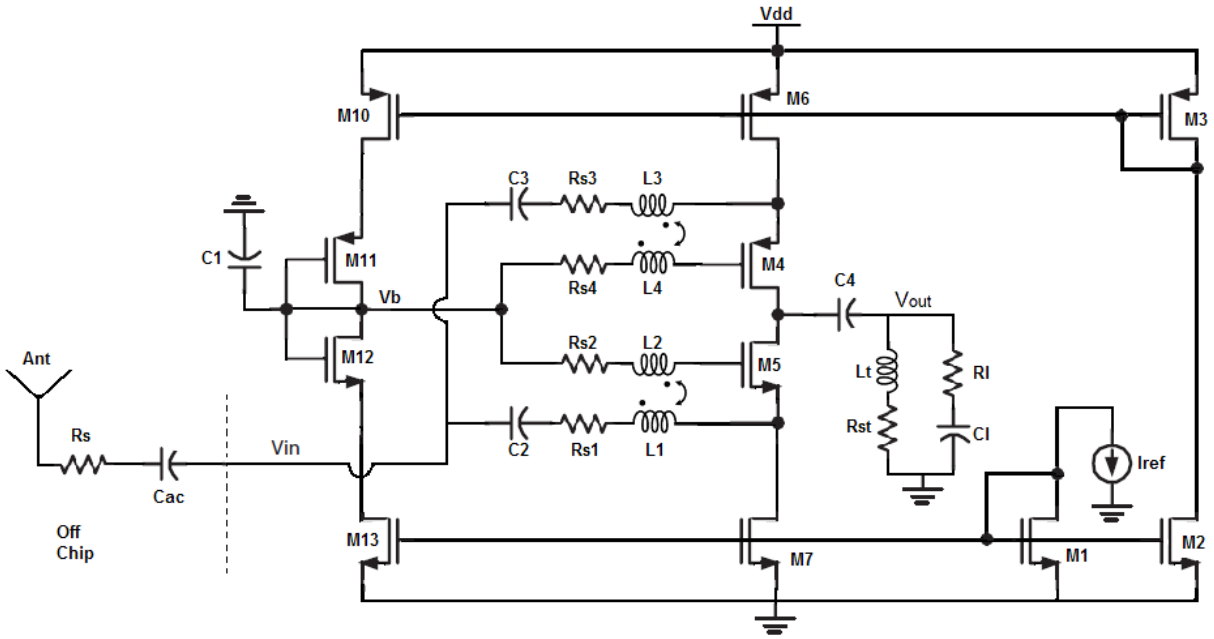


Figure 20: The proposed LNA.

The bodies of the transistors are coupled to the source nodes. This eliminates the bodyeffect and keeps the threshold voltage low, increasing the voltage headroom [23]. The drawback of this choice in this thesis might be that the source to bulk capacitance may become large and thereby degrade the performance in addition to that the bodyeffect in a common gate amplifier will contribute to increase the effective transconductance, and thereby provide the possibility to reduce the current consumption even further [20].

The capacitor C_1 is added to provide an AC-ground to the bias voltage. If it is not added the bias voltage tends to fluctuate in phase with the input signal. This is due to parasitic capacitive connection between the input and bias node through the transistors M6-M10-M11 and M7-M13-M12. The larger the disconnecting capacitor is, the better the results get. It will be a choice whether or not this should be an on- or offchip component. C_{ac} is in this design treated as an offchip capacitance. The DC-blocking capacitor C_4 at the output node is inserted to preserve the operation of the circuit when the tuning inductance L_t is connected as it is. A way to omit the use of this capacitor is to place a small capacitor between L_t and ground. L_t is used to tune out the load capacitance and other capacitances associated with the output node. The resistances in series with the inductors are models of the serial resistance which accompanies the inductors. The values are calculated according to equation (2.16). The connection factor of the mutual inductances is set to 0.85 and the Q-factor is set to 7. Both choices should be achievable according to [8] and [35].

The results from the simulation are shown in figure 21. The setup of the figure are from top to bottom: magnitude source and gate M5, phase source and gate M5, magnitude source and gate M4 and phase source and gate M4. Table 6 summarizes the results from figure 20 and table 7 summarizes the geometries and component values for the whole design.

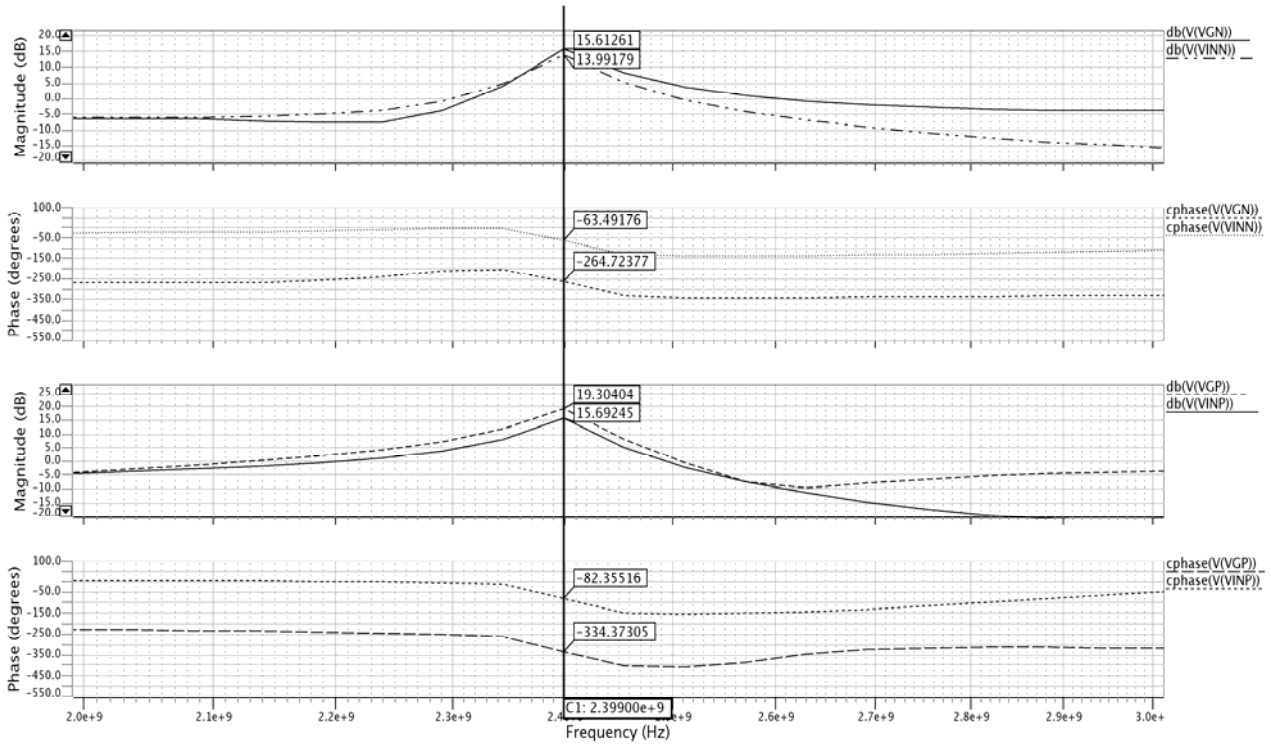


Figure 21: Sizing of passive components.

Node	Magnitude (dB)	Phase (deg)	Phasediff	Magnitudediff
$M4_{source}$	15.7	-82.4	252.0	3.6
$M4_{gate}$	19.3	-334.4		
$M5_{source}$	14.0	-63.5	201.2	1.6
$M5_{gate}$	15.6	-264.7		

Table 6: Summary of results from figure 21.

As figure 21 shows the g_m-boosting achieved in this simulation is not flawless. The phase of the signals at the source nodes are not perfectly inverted at the gate nodes. The set goals for gain is not completely achieved either. However, this result is what gave the best results in the following simulations of the LNA.

	$M1_N$	$M2_N$	$M3_P$	$M4_P$	$M5_N$	$M6_P$	$M7_N$	$M10_P$	$M11_P$	$M12_N$	$M13_N$
w (μm)	6.26	6.26	4.66	1.8	0.75	4.66	6.26	4.66	1.8	0.75	6.26
l (μm)	2.21	2.21	1.78	0.15	0.15	1.78	2.21	1.78	0.15	0.15	2.21
mult	2	1	1	200	200	200	200	2	2	2	2
nfing	3	3	2	1	1	2	3	2	1	1	3
	C_{ac}	C_1	C_2	C_3	C_4	C_{load}					
Farad	5n	3p	1p	1p	5n	32f					
	L_1	L_2	L_3	L_4	L_t		Q	k			
Hendry	6.49 n	7.10 n	3.54 n	7.63 n	9.12 n		7	0.85			
	R_{s1}	R_{s2}	R_{s3}	R_{s4}	R_{st}	R_s	R_{load}			I_{ref}	V_{dd}
Ohm	14.00	15.30	7.63	16.44	19.65	50	145			2 uA	1.2 V

Table 7: A complete overview of transistor geometries and sizes of passive devices for the proposed LNA.

4. Simulation Results

The whole architecture was simulated as it is shown in figure 20 with the parameters summarized in table 7. The testbenches used to generate the plots can be viewed in the appendix. The different results are shown in the subsequent figures and summarized in table 9.

4.1 Gain and bandwidth

Figure 22 and 23 shows plots of the voltage gain and bandwidth with the typical library and all the corner libraries.

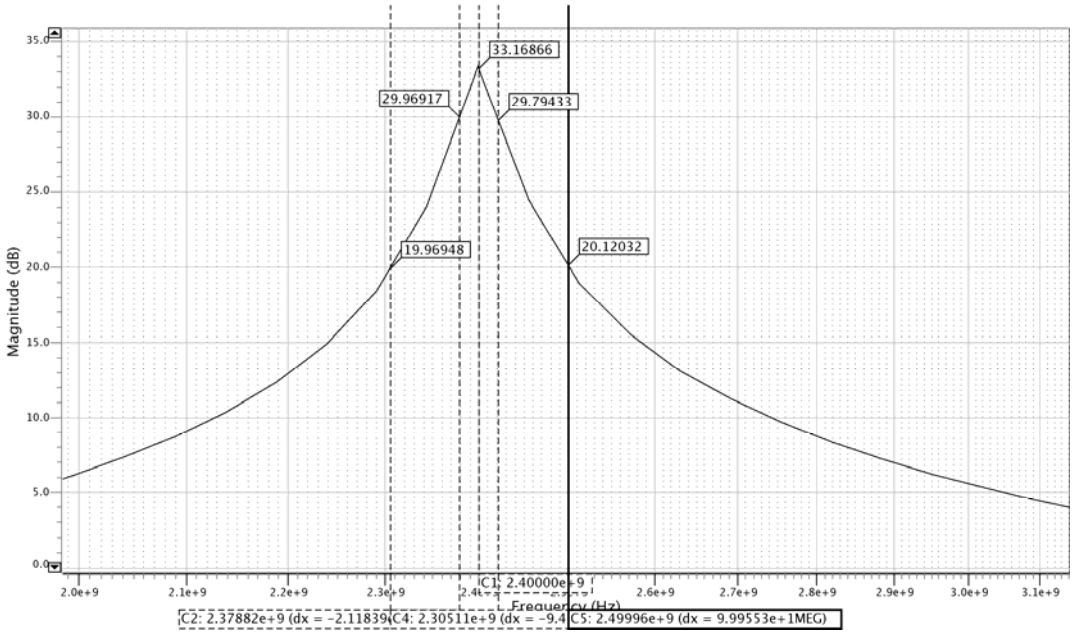


Figure 22: Gain and bandwidth at resonance.

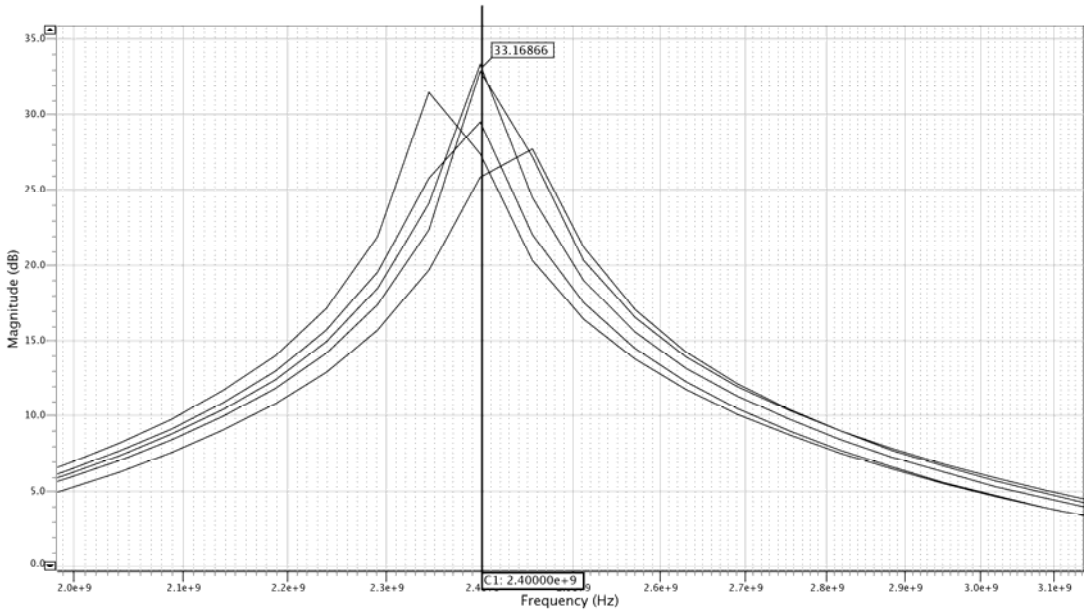


Figure 23: Gain and bandwidth at resonance, cornersimulation.

The gain at 2.4 GHz is 33 dB. The -3dB bandwidth of the resonance peak with the typical library is from 2.38 GHz to 2.42 GHz. The gain is over 20 dB from 2.3 GHz to 2.5 GHz. All libraries achieve a gain over well above 20 dB at 2.4 GHz.

4.2 Noise figure

The noise figure is calculated with Ezwave. The formula used for this calculation is from the definition of noise factor, cited in [6] as:

$$F \equiv \frac{V_{noTOTAL}^2}{V_{noR_s}^2} \rightarrow nf = 10\log(F) \tag{2.19}$$

The data needed to calculate the noise figure comes from two simulations, one simulation where all devices contribute to the noise at the output and one simulation where only the source impedance R_s contributes to the noise at the output. This is done by adding the *nonoise* to the different devices in the testbench. Since Eldo gives the noise spectral density, V_{no}, when using the command .noise, the calculation of noise figure from Ezwave uses 20 log instead of 10 log.

The resulting noise figure is shown in figure 22. All libraries are simulated and plotted together.

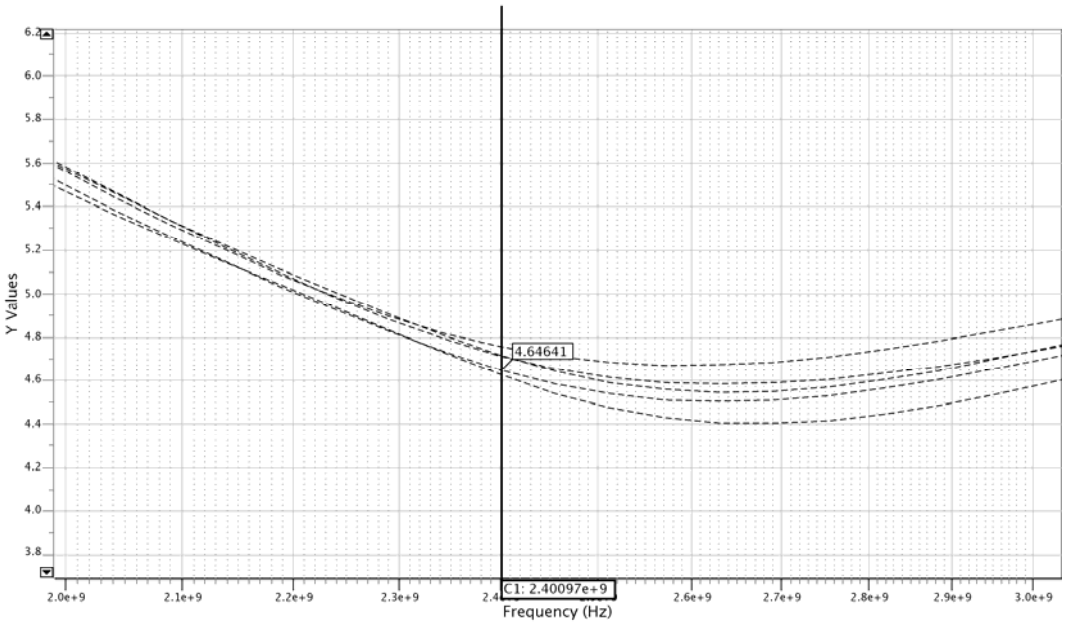


Figure 24: Noise figure in dB as a function of frequency, cornersimulation.

The plot shows the noise figure for all the corner simulations as a function of frequency. The marker is placed at the simulation with the typical library. The noise figure varies from 4.62 dB to 4.75 dB with the value from simulation with the typical library at 4.65 dB.

4.3 Linearity

IIP3 was directly extracted from the testbench. The result varies from -15.25 dBm to -15.53 dBm. The result with the typical library was -15.45 dBm. The .aex file from this simulation can be viewed in the appendix.

There was no specified goal for the 1 dB compression point, $1dB_{Cp}$, but it was simulated and the result with the typical library was -23.2 dBm. This is in reasonable accordance with the relationship between IIP3 and $1dB_{Cp}$ derived in [36], which states that $1dBC_p \approx 9.6 + IIP3$.

IIP3	-15.45dBm
$1dB_{Cp}$	-23.2 dBm

Table 8: IIP3 and $1dB_{Cp}$

4.4 Input match

Input match, S_{11} as a function of frequency is plotted in figure 23. The y-axis is in dB. The results vary from -10 dB to -8.8 dB with a result from the simulation with the typical library of -9.51 dB.

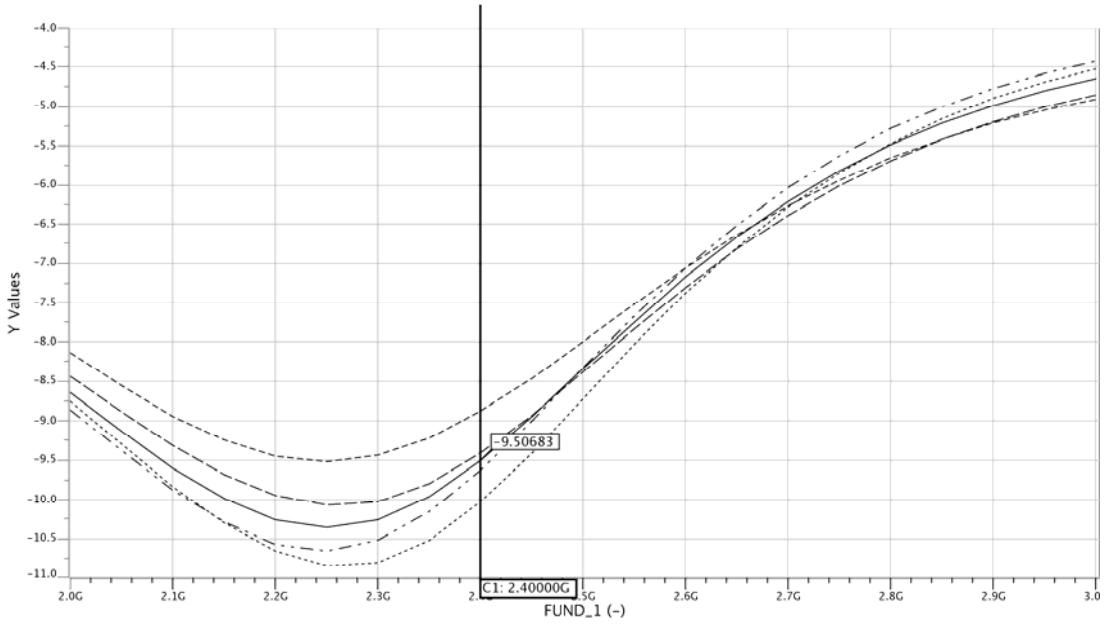


Figure 25: Input match S_{11} in dB as a function of frequency.

4.5 Current consumption

The average current consumption is extracted from a transient simulation with a sinewave with a frequency of 2.4 GHz and a magnitude of 0.1 mV_{pp}. The result is generated by extracting the average current delivered from the powersupply V_{dd}.

The total current consumption in the proposed amplifier with this simulation setup varied from 180 µA to 204 µA in the corner simulations. The result from the simulation with the typical library was 199 µA. This corresponds to a power consumption of 239 µW.

A summary of the achieved results are given in table 9. The target parameters are repeated for convenience.

Key parameters	Target	Achieved
Current consumption	200 µA	199 µA
Gain	20 dB	> 30 dB from 2.38 - 2.42 GHz
IIP3	-20 dBm	-15.45 dBm
$1dB_{Cp}$	-	-23.2 dBm
Noise figure	< 6dB	4.65 dB
Source impedance	50 Ohm	S_{11}= -9.5 dB
Bandwidth	200 MHz	> 20 dB gain from 2.3 – 2.5 GHz

Table 9: Results versus specifications.

As table 9 shows, as far as power consumption is reviewed, this design is very power efficient. The reported current consumption is measured for the whole circuit. The gain is clearly the result of a resonance peak. It exceeds the intrinsic gain in the amplifier and the -3 dB bandwidth is quite narrow. The gain is over 20 dB for 200 MHz.

5. Discussion and conclusions

The results achieved in this thesis are overall quite good. However, the results are from pre layout simulations, e.g. without layout parasitics. Layout was planned but not finished. With no experience with layout and little time left it proved difficult to perform a feasible layout. A bad layout will definitely reduce the performance in such an extent that no conclusions can be drawn from it.

The results gained in the simulations are optimized with the typical library. Replica biasing proves to be quite robust in this design. An almost symmetrical design with use of as much matching as possible is clearly a good choice to achieve adequate results in corner simulations. The performance does not degrade unacceptably in corner simulations. Even so, it is probably possible to achieve even lesser degradation in cornersimulations if wanted.

The input match gained here is relatively low, even though [7] claims that -10dB usually is a feasible input match. The reason for this result is probably from insufficient g_m-boosting. The difference in phase between the source and the gate for transistor M5 was 250 degrees. This should ideally have been 180 degrees. The inverting gain is also a bit too small according to the simple calculations conducted before sizing the passive devices. The reason for these two deviations is not investigated.

Since no layout was performed it is difficult to compare this relatively immature design with other comparable designs. However, there is a bit margin in most of the target parameters and nothing points in the direction that they are unattainable. The question is to what extent the performance degrades after layout is performed.

Overall performance for this amplifier shows that there should be possible to design a LNA with reasonable performance in spite of very low power consumption, e.g. it is probably possible to reduce the power consumption when designing an LNA, compared to what is yet published. The prize to pay to achieve the performance gained in this thesis is relatively high die area due to large transistors, large decoupling capacitors and two mutual inductors, and a somewhat low input match.

5.1 Future work

In this design lay out is not performed for either the transistors or the inductors. The inductors in this thesis are modeled with serial resistance only. Lack of process variables have made if difficult to use a more exact model. The library available at NTNU is a student version of the 90 nm CMOS TSMC process, without key parameters needed to perform inductor lay-out. Among others, [26], [32], [33] and [34] presents models and different realizations of onchip inductors and transformers.

Effects from pads and bondwires are not included in the simulations. [30] presents a model that can be used to simulate parasitics associated with the coupling pads.

The LNA would most likely require some sort of ESD-protection. This is not considered in this thesis. [11] and [31] presents some solutions on how to implement this.

The LNA is currently operating with only one gainsetting. Variable gain is probably needed to accommodate large input signals. [22] presents one way to implement variable gain to a common gate amplifier biased with current sources. The procedure described in this article should be possible to implement also in this design.

In this design the source is connected to the bulk to give voltage headroom by lowering the threshold voltage. If one utilizes the bodyeffect by connecting bulk to ground for NMOS and V_{dd} for PMOS this capacitance will be a lot smaller. In addition this will probably increase the effective transconductance and thereby increase the gain and lower the noise figure. This should be examined. In [20] a 10-15% increase in effective transconductance is claimed achieved. The profit in this design should be half of this due to the fact that this is a single ended design. One should be careful though, since the threshold voltage will increase, resulting in smaller voltage headroom for the amplifier. Another possibility is to use bulk drivers. They can be applied to influence the effective gm, the threshold voltage and the parasitic source to bulk capacitance. This is not considered in this thesis.

The simulations are performed with a temperature at 27 degrees Celsius. Age and mismatch are not considered in this thesis. There are in other words still many corners to simulate to validate the potential in the amplifier.

A possibility to digitally tune the resonance frequency of the amplifier should be implemented. This will make the design more robust with respect to process variations and mismatch. This can be done by inserting arrays of capacitors and using switches and a digital control word to tune the resonance frequency. It is also possible to lay out the inductors with several outputs, and in the same way vary the inductance to tune the resonance frequency.

6. Summary

In this thesis different aspects of general low power design and LNA-design have been studied. A new architecture for an ultra low power LNA is proposed and simple simulation results are presented. Simulations show that there should be possible to design a 2.4 GHz LNA that works sufficiently at 200 μA. The proposed architecture achieved a voltage gain over 20 dB from 2.32 to 2.5 GHz, a noise figure of 4.65 dB, IIP3 of -15.45 dBm and a input match of -9.5 dB. There is still a lot of work do and many simulations to perform before one can inconclusively conclude that the proposed architecture is a feasible solution, although the results generated in this thesis seem promising.

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Appendix

Testbenches for various simulations are appended for interested readers. All the results and plots in this thesis should be possible to reproduce using the following testbenches with TSMC's 90 nm CMOS libraries. The devices have the same names as in figure 19. Many of the names of the nodes used in the testbenches are not found in figure 19. This is because it would have unnecessarily cluttered the figure.

Contents

Appendix A: Transistor sizing

A1 NMOS sizing

```
*nmosdimm.cir

.opt nowarn=240 eps=1e-6

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

.param w1 = 3
.param l1= .1
.param id = 200u
.param r=5

id1 0 g dc id
id2 0 g1 dc id

.subckt nmos200 g
xm1 g g 0 0 nsvt w={l1*r} l=l1 nfing={ceil(l1*r/3)} mult=200
.ends nmos3

.subckt nmos g
xm1 g g 0 0 nsvt w={l1*r*200} l=l1 nfing={ceil(l1*r*200/3)} mult=1
.ends nmos300

x1 g nmos200
x2 g1 nmos

.op
.dc param l1 0.1 0.5 .001
*.step param r 1 15 1

*veff
.extract dc label=veffx1 vdss(x1.xm1.m1)
.extract dc label=veffx2 vdss(x2.xm1.m1)


*plot ft and ft/f
.defwave ftx1/f=gm(x1.xm1.m1)/(2*3.14*abs(cgs(x1.xm1.m1))+abs(cgd(x1.xm1.m1))
+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1)))/2.4g
.plot w(ftx1/f)

.defwave ftx2/f=gm(x2.xm1.m1)/(2*3.14*abs(cgs(x2.xm1.m1))+abs(cgd(x2.xm1.m1))
+abs(cgb(x2.xm1.m1))+abs(cds(x2.xm1.m1)))/2.4g
.plot w(ftx2/f)

.defwave ftx1=gm(x1.xm1.m1)/(2*3.14*abs(cgs(x1.xm1.m1))+abs(cgd(x1.xm1.m1))
+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1)))
.plot w(ftx1)

.defwave ftx2=gm(x2.xm1.m1)/(2*3.14*abs(cgs(x2.xm1.m1))+abs(cgd(x2.xm1.m1))
+abs(cgb(x2.xm1.m1))+abs(cds(x2.xm1.m1)))
.plot w(ftx2)

*plot intrinsic gain, gm/gds
.defwave A0x1=gm(x1.xm1.m1)/gds(x1.xm1.m1)
.plot w(A0x1)

.defwave A0x2=gm(x2.xm1.m1)/gds(x2.xm1.m1)
.plot w(A0x2)

*plot ft/f*A0
.defwave ft/fA0x1=(gm(x1.xm1.m1)*gm(x1.xm1.m1)/(2.4g*gds(x1.xm1.m1)*2*3.14*abs(cgs(x1.xm1.m1))
+abs(cgd(x1.xm1.m1))+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1))))
.plot dc w(ft/fA0x1)

.defwave ft/fA0x2=(gm(x2.xm1.m1)*gm(x2.xm1.m1)/(2.4g*gds(x2.xm1.m1)*2*3.14*abs(cgs(x2.xm1.m1))
+abs(cgd(x2.xm1.m1))+abs(cgb(x2.xm1.m1))+abs(cds(x2.xm1.m1))))
.plot dc w(ft/fA0x2)
```

```
*plot ft*A0
.defwave ftA0x1=(gm(x1.xm1.m1)*gm(x1.xm1.m1)/(gds(x1.xm1.m1)*2*3.14*abs(cgs(x1.xm1.m1))
+abs(cgd(x1.xm1.m1))+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1))))
.plot dc w(ftA0x1)

.defwave ftA0x2=(gm(x2.xm1.m1)*gm(x2.xm1.m1)/(gds(x2.xm1.m1)*2*3.14*abs(cgs(x2.xm1.m1))
+abs(cgd(x2.xm1.m1))+abs(cgb(x2.xm1.m1))+abs(cds(x2.xm1.m1))))
.plot dc w(ftA0x2)

.plot dc gm(x1.xm1.m1)
.plot dc gm(x2.xm1.m1)
.plot dc id(x1.xm1.m1)
.plot dc id(x2.xm1.m1)
.plot dc vdss(x1.xm1.m1)
.plot dc vdss(x2.xm1.m1)

*plot currentefficiency
.defwave curreffx1 = gm(x1.xm1.m1) / id(x1.xm1.m1)
.plot dc w(curreffx1)

.defwave curreffx2 = gm(x2.xm1.m1) / id(x2.xm1.m1)
.plot dc w(curreffx2)

*plot output resistance
.defwave rdsx1=1/gds(x1.xm1.m1)
.plot w(rdsx1)
.defwave rdsx2=1/gds(x2.xm1.m1)
.plot w(rdsx2)
```

A2 PMOS sizing

```
*pmosdimm.cir

.opt nowarn=240 eps=1e-6

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

.param w1 = 3
.param l1= .1
.param id = 200u
.param r=12

vdd vdd 0 dc 1.2
id1 g 0 dc id

.subckt pmos g vdd
xm1 g g vdd vdd psvt w={l1*r} l=l1 nfing=1 mult=200
.ends nmos300

x1 g vdd pmos

.op
.dc param l1 0.1 0.5 .001

*veff
.extract dc label=veffx1 vdss(x1.xm1.m1)

*plot ft/f
.defwave ftx1/f=gm(x1.xm1.m1)/(2*3.14*abs(cgs(x1.xm1.m1))+abs(cgd(x1.xm1.m1))
+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1)))/2.4g
.plot w(ftx1/f)

*plot ft
.defwave
ftx1=gm(x1.xm1.m1)/(2*3.14*abs(cgs(x1.xm1.m1))+abs(cgd(x1.xm1.m1))+abs(cgb(x1.xm1.m1))+abs(cds
(x1.xm1.m1)))
.plot w(ftx1)


*plot intrinsic gain A0, gm/gds
.defwave A0x1=gm(x1.xm1.m1)/gds(x1.xm1.m1)
.plot w(A0x1)


*plo ft/f*A0
.defwave ft/fA0x1=(gm(x1.xm1.m1)*gm(x1.xm1.m1)/(2.4g*gds(x1.xm1.m1)*2*3.14*abs(cgs(x1.xm1.m1))
+abs(cgd(x1.xm1.m1))+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1))))
.plot dc w(ft/fA0x1)


*plot ftA0
.defwave ftA0x1=(gm(x1.xm1.m1)*gm(x1.xm1.m1)/(gds(x1.xm1.m1)*2*3.14*abs(cgs(x1.xm1.m1))
+abs(cgd(x1.xm1.m1))+abs(cgb(x1.xm1.m1))+abs(cds(x1.xm1.m1))))
.plot dc w(ftA0x1)

.plot dc gm(x1.xm1.m1)
.plot dc gm(x2.xm1.m1)
.plot dc id(x1.xm1.m1)
.plot dc id(x2.xm1.m1)
.plot dc vdss(x1.xm1.m1)
.plot dc vdss(x2.xm1.m1)

*plot currentefficiency
.defwave curreffx1 = gm(x1.xm1.m1) / id(x1.xm1.m1)
.plot dc w(curreffx1)

*plot output resistance
.defwave rdsx1=1/gds(x1.xm1.m1)
.plot w(rdsx1)
```

Appendix B: Biasing

```
*dimensioning current mirrors and current sources


.opt nowarn=240 eps=1e-7 noascii opseldo_detail=all opseldo_netlist aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

.paramopt w1 = (.12,.1,20,*)
.paramopt l1 = (.1,.1,10,*)
.paramopt w2 = (.12,.1,10,*)
.paramopt l2 = (.1,.1,10,*)


*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing={ceil(w1/3)} mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing={ceil(w1/3)} mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing={ceil(w2/3)} mult=1

*current sources for lna goal id=200 v3=.6
xm4 3 2 vdd vdd psvt w=w2 l=l2 nfing={ceil(w2/3)} mult=200
xm5 3 ib 0 0 nsvt w=w1 l=l1 nfing={ceil(w1/3)} mult=200

.extract dc label=id4 id(xm4.m1) goal=-207u
.extract dc label=id5 id(xm5.m1) goal=207u
.extract dc label=vout v(3) goal=.600
.extract dc label=vb v(vbt) !goal=.515
.extract dc label=w1 w1
.extract dc label=l1 l1
.extract dc label=w2 w2
.extract dc label=l2 l2
.extract dc label=rds4 1/gds(xm4.m1)
.extract dc label=rds5 1/gds(xm5.m1)

.op
.probe
.optimize param=w1,l1,w2,l2

*****************************************************************************************

*dc-simulation

.opt nowarn=240 eps=1e-7 noascii aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm4 vout vb vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vb vinn vinn nsvt w=.75 l=0.15 nfing=1 mult=200

*current sources
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200
```

```
*bias voltage source
.param vb=.5
vb vb 0 vb

.op
.probe
.dc param vb .3 .8 .01

*plots and extractions
.defwave gmtot=(gm(xm4.m1)+gm(xm5.m1))
.plot w(gmtot)

.defwave rout=1/(gds(xm4.m1)+gds(xm5.m1))
.plot w(rout)

.defwave a0=(gm(xm4.m1)+gm(xm5.m1))/(gds(xm4.m1)+gds(xm5.m1))
.plot w(a0)

.extract dc label = Rout 1/(gds(xm4.m1)+gds(xm5.m1))

.extract dc label = vds4 vds(xm4.m1)
.extract dc label = vds5 vds(xm5.m1)
.extract dc label = vds6 vds(xm6.m1)
.extract dc label = vds7 vds(xm7.m1)

.extract dc label = vgs4  vgs(xm4.m1)
.extract dc label = vgs5  vgs(xm5.m1)
.extract dc label = vgs6 vgs(xm6.m1)
.extract dc label = vgs7  vgs(xm7.m1)

.extract dc label = id1 id(xm1.m1)
.extract dc label = id2 id(xm2.m1)
.extract dc label = id3 id(xm3.m1)
.extract dc label = id4 id(xm4.m1)
.extract dc label = id5 id(xm5.m1)
.extract dc label = id6 id(xm6.m1)
.extract dc label = id7 id(xm7.m1)


.extract dc label = rds7 1/gds(xm7.m1)
.extract dc label = rds4 1/gds(xm4.m1)
.extract dc label = rds5 1/gds(xm5.m1)
.extract dc label = rds6 1/gds(xm6.m1)

.extract dc label = gm4 gm(xm4.m1)
.extract dc label = gm5 gm(xm5.m1)
.extract dc label = GMtot gm(xm4.m1)+gm(xm5.m1)

*.alter
*.lib key=mos ~/cmos090eldo/cmos090_ff.mod
*.alter
*.lib key=mos ~/cmos090eldo/cmos090_ss.mod
*.alter
*.lib key=mos ~/cmos090eldo/cmos090_fs.mod
*.alter
*.lib key=mos ~/cmos090eldo/cmos090_sf.mod
*.end

*********************************************************************************************

*ac-simulation of the whole amp with replica bias

.opt nowarn=240 eps=1e-7 noascii aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
cac vinrf vin 1

*source
vrf vrf 0 ac 1
rs vrf vinrf 50
```

```
.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm4 vout vb vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vb vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2

*ac-ground for biasing voltage
cex vb 0 1

c3 vin vinn 1
c4 vin vinp 1

.op
.probe
.ac dec 100 1 100g

.plot v(vout)

.alter
.lib key=mos ~/cmos090eldo/cmos090_ff.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_ss.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_fs.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_sf.mod
.end
```

Appendix C: Active load input impedance extraction

```
*pmos gainstage as load

.opt nowarn=240 eps=1e-6 ammeter engnot noascii aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

*bias-sources
vdd1 vdd1 0 dc 1.2

iref 0 ib dc 2u

.param w1 = 6.2605
.param l1 = 2.2088

*current mirror
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=2 mult=2

*gainstage
xm8 20 ib 0 0 nsvt w=w1 l=l1 nfing=2 mult=80 nonoise
xm9 20 vout1 vdd1 vdd1 psvt w=.65 l=.15 nfing=1 mult=50 nonoise

*frequency of interest
.param frequ=2.4g

* voltage source
V1 vout1 1 iport=1 rport=50

*gatebias extracted from the LNA output
.param vdc=.9
vdc 1 0 dc vdc

*analysis
.op
.ac dec 10 1 10G

.extract dc label=gm gm(xm9.m1)
.extract dc label=id id(xm9.m1)
.extract dc label=ftCS gm(xm9.m1)/(2*3.14159*(abs(cgd(xm9.m1))+abs(cgs(xm9.m1))
+abs(cgb(xm9.m1))+abs(cds(xm9.m1))))

*serial impedance extraction
.extract ac label="R_serial" yval(zr(1,1),frequ)

* plot the resistance over the defined frequency range
.plot ac zr(1,1)

*extracted lumped reactance value at the frequency of interest
.defwave cap_ind= eval(zi(1,1)>0?zi(1,1)/(2*3.14159*freq):1/(zi(1,1)*2*3.14159*freq))
.extract ac label=" C_serial if<0 or L_serial if>0 " yval(w(cap_ind),frequ)

* plot the reactance value over the defined frequency range
.plot ac zi(1,1)
.plot ac wr(cap_ind)
```

Appendix D: LNA simulations

D1 Sizing of the passive components and Gain simulations

```
*sizing of passive components
.opt nowarn=240 eps=1e-7 noascii opseldo_detail=all opseldo_netlist aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
vdd1 vdd1 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
.param cac=5n
cac vinrf vin1 cac

vrf vrf 0 ac 1
rs vrf vinrf 50

.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm4 vout vgp vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vgn vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2

*ac-ground for voltage bias
.param cex=3p
cex vb 0 cex

*load extracted from gainstage
rl vout1 vout2 145
cl vout2 0 32f


*trasformers
*q-factor
.param pi = 3.14
.param f = 2.4g
.param w = {2*pi*f}
.param q = 7

.paramopt lt1=(8.5n,1n,15n,*)
.paramopt lt2=(10n,1n,15n,*)
.paramopt lt3=(7.5n,1n,15n,*)
.paramopt lt4=(5n,1n,15n,*)

l1 vinn vinn2 lt1
rs1 vinn2 vinn1 value = {w*lt1/q}
l2 vb1 vgn lt2
rs2 vb1 vb value = {w*lt2/q}
k1 l1 l2 0.85

l3 vinp vinp2 lt3
rs3 vinp1 vinp2 value = {w*lt3/q}
l4 vb2 vgp lt4
```

```
rs4 vb vb2 value = {w*lt4/q}
k2 l3 l4 0.85


.paramopt cfn=(1p,1f,1p,*)
.paramopt cfp=(900f,1f,1p,*)

c3 vin1 vinn1 cfn
c4 vin1 vinp1 cfp

*output node
.paramopt ltank=(7n,1n,15n,*)
.param cac1=5n

cac1 vout vout1 cac1
ltank vout1 vout3 ltank
rsltank vout3 0 value={w*ltank/q}


.extract ac label=phase_n (yval(vp(vinn),2.45g)-yval(vp(vgn),2.45g)) goal=-180
.extract ac label=phase_p (yval(vp(vinp),2.45g)-yval(vp(vgp),2.45g)) goal=-180
.extract ac label=gain_p (yval(vdb(vgp),2.45g)-yval(vdb(vinp),2.45g)) goal=3
.extract ac label=gain_n (yval(vdb(vgn),2.45g)-yval(vdb(vinn),2.45g)) goal=3
.extract ac label=mag_vinn yval(vdb(vinn),2.45g) goal=6
.extract ac label=mag_vinp yval(vdb(vinp),2.45g) goal=6

.extract dc label=lt1 lt1
.extract dc label=lt2 lt2
.extract dc label=lt3 lt3
.extract dc label=lt4 lt4
.extract dc label=cfn cfn
.extract dc label=cfp cfp
.extract dc label=ltank ltank

.op
.probe
.ac dec 100 1 100g
.optimize param=lt1,lt2,lt3,lt4,cfn,cfp,ltank

*plots and extractions
.defwave gmtot=(gm(xm4.m1)+gm(xm5.m1))
.plot w(gmtot)
.defwave rout=1/(gds(xm4.m1)+gds(xm5.m1))
.plot w(rout)
.defwave a0=(gm(xm4.m1)+gm(xm5.m1))/(gds(xm4.m1)+gds(xm5.m1))
.plot w(a0)

.plot vgs(xm1.m1) vgs(xm2.m1) vgs(xm3.m1) vgs(xm4.m1) vgs(xm5.m1) vgs(xm6.m1) vgs(xm7.m1)
.plot vds(xm1.m1) vds(xm2.m1) vds(xm3.m1) vds(xm4.m1) vds(xm5.m1) vds(xm6.m1) vds(xm7.m1)
.plot id(xm1.m1) id(xm2.m1) id(xm3.m1) id(xm4.m1) id(xm5.m1) id(xm6.m1) id(xm7.m1)
.plot gm(xm4.m1) gm(xm5.m1) !im(rs)

.extract dc label = Rout 1/(gds(xm4.m1)+gds(xm5.m1))

.extract dc label = vds4 vds(xm4.m1)
.extract dc label = vds5 vds(xm5.m1)
.extract dc label = vds6 vds(xm6.m1)
.extract dc label = vds7 vds(xm7.m1)
.extract dc label = vgs4  vgs(xm4.m1)
.extract dc label = vgs5  vgs(xm5.m1)
.extract dc label = vgs6 vgs(xm6.m1)
.extract dc label = vgs7  vgs(xm7.m1)
.extract dc label = id1 id(xm1.m1)
.extract dc label = id2 id(xm2.m1)
.extract dc label = id3 id(xm3.m1)
.extract dc label = id4 id(xm4.m1)
.extract dc label = id5 id(xm5.m1)
.extract dc label = id6 id(xm6.m1)
.extract dc label = id7 id(xm7.m1)
.extract dc label = id8 id(xm8.m1)
.extract dc label = id9 id(xm9.m1)
.extract dc label = id10 id(xm10.m1)
.extract dc label = id11 id(xm11.m1)
.extract dc label = id12 id(xm12.m1)
.extract dc label = id13 id(xm13.m1)
.extract dc label = rds7 1/gds(xm7.m1)
.extract dc label = rds4 1/gds(xm4.m1)
```

```
.extract dc label = rds5 1/gds(xm5.m1)
.extract dc label = rds6 1/gds(xm6.m1)

.extract dc label = gm4 gm(xm4.m1)
.extract dc label = gm5 gm(xm5.m1)
.extract dc label = GMtot gm(xm4.m1)+gm(xm5.m1)

*.alter
*.lib key=mos ~/cmos090eldo/cmos090_ff.mod
*.alter
*.lib key=mos ~/cmos090eldo/cmos090_ss.mod
*.alter
*.lib key=mos ~/cmos090eldo/cmos090_fs.mod
*.alter
*.lib key=mos ~/cmos090eldo/cmos090_sf.mod

.end
```

D2 Noise figure extraction

```
*noise extraction, two simulations, one with noise on for all and one with noise on for Rs
only

.opt nowarn=240 eps=1e-7 noascii opseldo_detail=all opseldo_netlist aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
.param cac=5n
cac vinrf vin1 cac

vrf vrf 0 ac 1
rs vrf vinrf 50

.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2 nonoise
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1 nonoise
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1 nonoise

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200 nonoise
xm4 vout vgp vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200 nonoise
xm5 vout vgn vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200 nonoise
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200 nonoise

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2 nonoise
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2 nonoise
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2 nonoise
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2 nonoise

*ac-ground for voltage bias
.param cex=3p
cex vb 0 cex

*load extracted from gainstage
rl vout1 vout2 145 nonoise
cl vout2 0 32f

*transformers
*q-factor
.param pi = 3.14
.param f = 2.4g
.param w = {2*pi*f}
.param q = 7

.param lt1=6.4907n
.param lt2=7.0957n
.param lt3=3.5375n
.param lt4=7.6262n

l1 vinn vinn2 lt1
rs1 vinn2 vinn1 value = {w*lt1/q} nonoise
l2 vb1 vgn lt2
rs2 vb1 vb value = {w*lt2/q} nonoise
k1 l1 l2 0.85

l3 vinp vinp2 lt3
rs3 vinp1 vinp2 value = {w*lt3/q} nonoise
l4 vb2 vgp lt4
rs4 vb vb2 value = {w*lt4/q} nonoise
k2 l3 l4 0.85
.param cfn=1p
.param cfp=1p
```

```
c3 vin1 vinn1 cfn
c4 vin1 vinp1 cfp

.param ltank=9.1054n
.param cac1=5n

cac1 vout vout1 cac1
ltank vout1 vout3 ltank
rsltank vout3 0 value={w*ltank/q} nonoise

.op
.probe
.ac dec 100 1 100g
.noise v(vout) vrf 100

.alter
.lib key=mos ~/cmos090eldo/cmos090_ff.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_ss.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_fs.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_sf.mod
.end
```

D3 Linearity

```
*iip3 extraction

.opt nowarn=240 eps=1e-7 noascii aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
.param cac=5n
cac vinrf vin1 cac

vrf vinrf 0 rport=50 iport=1 FOUR fund1 fund2 Pdbm (1,0) pin -90 (0, 1) pin -90
.param pin=-20
.param fund_1=2.4g fund_2=2.401g

.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm4 vout vgp vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vgn vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2

*ac-ground for bias voltage
.param cex=3p
cex vb 0 cex

*load extracted from gainstage
rl vout1 vout2 145
cl vout2 0 32f

*transformers
*q-factor
.param pi = 3.14
.param f = 2.4g
.param w = {2*pi*f}
.param q = 7

.param lt1=6.4907n
.param lt2=7.0957n
.param lt3=3.5375n
.param lt4=7.6262n

l1 vinn vinn2 lt1
rs1 vinn2 vinn1 value = {w*lt1/q}
l2 vb1 vgn lt2
rs2 vb1 vb value = {w*lt2/q}
k1 l1 l2 0.85

l3 vinp vinp2 lt3
rs3 vinp1 vinp2 value = {w*lt3/q}
l4 vb2 vgp lt4
rs4 vb vb2 value = {w*lt4/q}
k2 l3 l4 0.85

.param cfn=1p
.param cfp=1p
```

```
c3 vin1 vinn1 cfn
c4 vin1 vinp1 cfp

.param ltank=9.1054n  !9.372142e-09
.param cac1=5n

cac1 vout vout1 cac1
ltank vout1 vout3 ltank
rsltank vout3 0 value={w*ltank/q}

*Steady-State analysis definition
.sst fund1=fund_1 nharm1=10 fund2=fund_2 nharm2=10
.option sst_spectrum=1
* Plots
.plot fsst vdb(vinrf) vdb(vout2)
.plot fsst PdBm(vrf)
.plot fsst PdBm(rl)
.plot tsst v(vout2)
* functions for direct IIP3-OIP3 extracts
.extract fsst label=IIP3_ref iipx(PdBm(vrf), PdBm(rl), fund_1, 2*fund1-fund2)

.alter
.lib key=mos ~/cmos090eldo/cmos090_ff.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_ss.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_fs.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_sf.mod
.end

********************************************************************************************************

*iip3.aex file

EXTRACT for SST results FSST
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 0
    *IIP3_REF = -1.5454E+01

EXTRACT for SST results FSST
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 1
    *IIP3_REF = -1.5516E+01

EXTRACT for SST results FSST
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 2
    *IIP3_REF = -1.5254E+01

EXTRACT for SST results FSST
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 3
    *IIP3_REF = -1.5321E+01

EXTRACT for SST results FSST
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 4
    *IIP3_REF = -1.5537E+01

********************************************************************************************************

*1dbcp simulation

*Power Efficiency and 1dB Compression Point Extraction

.opt nowarn=240

*eldo accuracy
.option eps=1e-6

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

*CG-LNA
.include new.ckt
x1 in load new
```

```
RL load 0 145
*cl load 0 32f
Vin IN 0 RPORT=50 iport=1 FOUR fund1 PdBm (1) Pin -90
* Power sweep
.param Pin=-80
.step param Pin -80 20 1
* Steady-State analysis definition
.sst fund1=2.4GigaHz nharm1=10
.option sst_max_liniter=100
* Plots
.plot tsst v(load)
.plot fsst vdb(load)
* Power efficiency: Pout at fund1 / Pdc
.extract fsst label=PE YVAL(Pm(RL), fund1)/YVAL(Pm(x1.Vdd), 0)
.extract MAX(meas(PE))
* Power added efficiency: (Pout-Pin) at fund1 / Pdc
.extract fsst label=PAE (YVAL(Pm(RL), fund1) - YVAL(Pm(Vin), fund1))/YVAL(Pm(x1.Vdd), 0)
.extract MAX(meas(PAE))
* Gain
.extract fsst label=Gain YVAL(PdBm(RL), fund1) - YVAL(PdBm(Vin), fund1)
* 1dB compression point
.extract fsst label=POUTdBm YVAL(PdBm(RL), fund1)
.extract fsst label=PINdBm Yval(PdBm(Vin), fund1)
.extract sweep label=IP1dB yval(meas(PINdBm), xcompress(meas(POUTdBm), 1.0))
.extract sweep label=OP1dB compress(meas(POUTdBm), 1.0)
.end

********************************************************************************************

*new.ckt

.subckt new vinrf vout1

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
.param cac=5n
cac vinrf vin1 cac

.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm4 vout vgp vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vgn vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2

*ac-ground for voltage bias
.param cex=3p
cex vb 0 cex

*transformers
*q-factor
.param pi = 3.14
.param f = 2.4g
.param w = {2*pi*f}
.param q = 7

.param lt1=6.4907n
.param lt2=7.0957n
.param lt3=3.5375n
.param lt4=7.6262n
```

```
l1 vinn vinn2 lt1
rs1 vinn2 vinn1 value = {w*lt1/q}
l2 vb1 vgn lt2
rs2 vb1 vb value = {w*lt2/q}
k1 l1 l2 0.85

l3 vinp vinp2 lt3
rs3 vinp1 vinp2 value = {w*lt3/q}
l4 vb2 vgp lt4
rs4 vb vb2 value = {w*lt4/q}
k2 l3 l4 0.85

.param cfn=1p
.param cfp=1p

c3 vin1 vinn1 cfn
c4 vin1 vinp1 cfp

.param ltank=9.1054n  !9.372142e-09
.param cac1=5n

cac1 vout vout1 cac1
ltank vout1 vout3 ltank
rsltank vout3 0 value={w*ltank/q}

.ends
```

D4 S_{11} extraction

```
.opt nowarn=240 eps=1e-7 noascii aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
.param cac=5n
cac vinrf vin1 cac

Vin IN 1 RPORT=50 iport=1 FOUR fund1 PdBm (1) p1 -90
vdc 1 0 dc .6
.TEMP 27.0

.param w1 = 6.2605
.param l1 = 2.2088
.param w2 = 4.6608
.param l2 = 1.7809

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm4 vout vgp vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vgn vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2

*ac-ground for biasing voltage
.param cex=3p
cex vb 0 cex

*load extracted from gainstage
rl vout1 vout2 145
cl vout2 0 32f

*transformers
*q-factor
.param pi = 3.14
.param f = 2.4g
.param w = {2*pi*f}
.param q = 7

.param lt1=6.4907n
.param lt2=7.0957n
.param lt3=3.5375n
.param lt4=7.6262n

l1 vinn vinn2 lt1
rs1 vinn2 vinn1 value = {w*lt1/q}
l2 vb1 vgn lt2
rs2 vb1 vb value = {w*lt2/q}
k1 l1 l2 0.85

l3 vinp vinp2 lt3
rs3 vinp1 vinp2 value = {w*lt3/q}
l4 vb2 vgp lt4
rs4 vb vb2 value = {w*lt4/q}
k2 l3 l4 0.85

.param cfn=1p
.param cfp=1p
```

```
c3 vin1 vinn1 cfn
c4 vin1 vinp1 cfp

.param ltank=9.1054n  !9.372142e-09
.param cac1=5n

cac1 vout vout1 cac1
ltank vout1 vout3 ltank
rsltank vout3 0 value={w*ltank/q}

.param fund_1=2g

.op
.sst fund1=fund_1 nharm1=5
.param p1=-100
.step param fund_1 2g 3g 1meg
* s-params on port1
.extract fsst label=STEADY_STATE_S11 yval(sdb(1,1), fund1)
.plot fsst yval(sdb(1,1), fund1)
```

D5 Current consumption

```
*current comsumption

.opt nowarn=240 eps=1e-7 noascii aex

*Library
.lib key=mos ~/cmos090eldo/cmos090_tt.mod

vdd vdd 0 dc 1.2
vdd1 vdd1 0 dc 1.2
iref 0 ib dc 2u

*offchip ac-coupling
.param cac=5n
cac vinrf vin1 cac

vrf vrf 0 sin(0 0.0001 2.4g 0 0)
rs vrf vinrf 50

.param w1 = 6.2605    !8.875
.param l1 = 2.2088    !1.6028
.param w2 = 4.6608    !5.3823
.param l2 = 1.7809    !2.464

*Current mirrors
xm1 ib ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2
xm2 2 ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=1
xm3 2 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=1

*lna
xm6 vinp 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=200
xm4 vout vgp vinp vinp psvt w=1.8 l=0.15 nfing=1 mult=200
xm5 vout vgn vinn vinn nsvt w=0.75 l=0.15 nfing=1 mult=200
xm7 vinn ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=200

*replica bias
xm10 vipb 2 vdd vdd psvt w=w2 l=l2 nfing=2 mult=2
xm11 vb vb vipb vipb psvt w=1.8 l=.15 nfing=1 mult=2
xm12 vb vb vinb vinb nsvt w=.75 l=.15 nfing=1 mult=2
xm13 vinb ib 0 0 nsvt w=w1 l=l1 nfing=3 mult=2

*ac-ground for voltage bias
.param cex=3p
cex vb 0 cex

*load extracted from gainstage
rl vout1 vout2 145
cl vout2 0 32f

*transformers
*q-factor
.param pi = 3.14
.param f = 2.4g
.param w = {2*pi*f}
.param q = 7

.param lt1=6.4907n    !7.114190e-09
.param lt2=7.0957n    !5.579831e-09
.param lt3=3.5375n    !4.263061e-09
.param lt4=7.6262n    !6.935493e-0

l1 vinn vinn2 lt1
rs1 vinn2 vinn1 value = {w*lt1/q}
l2 vb1 vgn lt2
rs2 vb1 vb value = {w*lt2/q}
k1 l1 l2 0.85

l3 vinp vinp2 lt3
rs3 vinp1 vinp2 value = {w*lt3/q}
l4 vb2 vgp lt4
rs4 vb vb2 value = {w*lt4/q}
k2 l3 l4 0.85

.param cfn=1p
.param cfp=1p
```

```
c3 vin1 vinn1 cfn
c4 vin1 vinp1 cfp

.param ltank=9.1054n  !9.372142e-09
.param cac1=5n

cac1 vout vout1 cac1
ltank vout1 vout3 ltank
rsltank vout3 0 value={w*ltank/q}

.op
.probe
.tran .1p 15n

.extract tran label = iavgr average(i(vdd))

.extract dc label = id1 id(xm1.m1)
.extract dc label = id2 id(xm2.m1)
.extract dc label = id3 id(xm3.m1)
.extract dc label = id4 id(xm4.m1)
.extract dc label = id5 id(xm5.m1)
.extract dc label = id6 id(xm6.m1)
.extract dc label = id7 id(xm7.m1)
.extract dc label = id10 id(xm10.m1)
.extract dc label = id11 id(xm11.m1)
.extract dc label = id12 id(xm12.m1)
.extract dc label = id13 id(xm13.m1)

.extract dc label = gm4 gm(xm4.m1)
.extract dc label = gm5 gm(xm5.m1)
.extract dc label = GMtot gm(xm4.m1)+gm(xm5.m1)


.alter
.lib key=mos ~/cmos090eldo/cmos090_ff.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_ss.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_fs.mod
.alter
.lib key=mos ~/cmos090eldo/cmos090_sf.mod

.end

********************************************************************************************

*power.aex


TITLE *current comsumption
EXTRACT for TRANSIENT ANALYSIS
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 0       !typical
    *IAVGR = -1.9864E-04
    *ID1 =  1.9464E-06
    *ID2 =  1.0522E-06
    *ID3 = -9.4852E-07
    *ID4 = -1.9562E-04
    *ID5 =  1.9562E-04
    *ID6 = -1.9562E-04
    *ID7 =  1.9562E-04
    *ID10 = -1.9550E-06
    *ID11 = -1.9549E-06
    *ID12 =  1.9576E-06
    *ID13 =  1.9576E-06
    *GM4 =  4.1384E-03
    *GM5 =  4.4916E-03
    *GMTOT =  8.6300E-03

EXTRACT for TRANSIENT ANALYSIS
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 1       !fast-fast
    *IAVGR = -1.7936E-04
    *ID1 =  1.7797E-06
    *ID2 =  9.7363E-07
    *ID3 = -8.2769E-07
    *ID4 = -1.7661E-04
```

```
    *ID5 =  1.7661E-04
    *ID6 = -1.7661E-04
    *ID7 =  1.7661E-04
    *ID10 = -1.7655E-06
    *ID11 = -1.7654E-06
    *ID12 =  1.7675E-06
    *ID13 =  1.7675E-06
    *GM4 =  3.8736E-03
    *GM5 =  4.2112E-03
    *GMTOT =  8.0848E-03

EXTRACT for TRANSIENT ANALYSIS
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 2       !slow-slow
    *IAVGR = -2.0396E-04
    *ID1 =  1.9872E-06
    *ID2 =  1.0657E-06
    *ID3 = -1.0038E-06
    *ID4 = -2.0088E-04
    *ID5 =  2.0088E-04
    *ID6 = -2.0088E-04
    *ID7 =  2.0088E-04
    *ID10 = -2.0075E-06
    *ID11 = -2.0075E-06
    *ID12 =  2.0097E-06
    *ID13 =  2.0097E-06
    *GM4 =  4.1340E-03
    *GM5 =  4.5105E-03
    *GMTOT =  8.6445E-03

EXTRACT for TRANSIENT ANALYSIS
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 3       !fast-slow
    *IAVGR = -1.9801E-04
    *ID1 =  1.9554E-06
    *ID2 =  1.0631E-06
    *ID3 = -9.4258E-07
    *ID4 = -1.9499E-04
    *ID5 =  1.9499E-04
    *ID6 = -1.9500E-04
    *ID7 =  1.9499E-04
    *ID10 = -1.9488E-06
    *ID11 = -1.9488E-06
    *ID12 =  1.9528E-06
    *ID13 =  1.9528E-06
    *GM4 =  4.0234E-03
    *GM5 =  4.5442E-03
    *GMTOT =  8.5676E-03

EXTRACT for TRANSIENT ANALYSIS
  TEMPERATURE =  2.7000E+01 Celsius
  ALTER index 4       !slow-fast
    *IAVGR = -1.9889E-04
    *ID1 =  1.9377E-06
    *ID2 =  1.0430E-06
    *ID3 = -9.5417E-07
    *ID4 = -1.9587E-04
    *ID5 =  1.9587E-04
    *ID6 = -1.9587E-04
    *ID7 =  1.9587E-04
    *ID10 = -1.9577E-06
    *ID11 = -1.9577E-06
    *ID12 =  1.9593E-06
    *ID13 =  1.9593E-06
    *GM4 =  4.2532E-03
    *GM5 =  4.4332E-03
    *GMTOT =  8.6864E-03
```