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Fast Surveillance of the MKD High Voltage Pulse Generator

Part of the LHC Beam Dump System at CERN

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Problem Description

This project concerns the development of an electronic module for the fast surveillance of the MKD high voltage pulse generator of the LHC Beam Dumping System (LBDS).

The high voltage pulse generators of the LHC Beam Dumping System are built on the basis of a fully redundant hardware architecture. A correct surveillance of the pulsed current in the different redundant circuits of a generator is required in order to guarantee its availability and to be able to perform an early detection of an impedance sharing modification between the redundant circuits.

The work will consist in
- the capture of functional requirements,(Preliminary studies)
- the study of the possible technical solution,
- the design and the development of an electronic module able to acquire the pulse signals,
- the development of the embedded software to perform the signals analysis,
- the integration of the module within the existing control environment.

Typical keywords for this project are:
Analog and digitial electronics, Embedded software, VHDL, FPGA, PROFIBUS-DP and PLC.

Assignment given: 01. May 2006
Supervisor: Ragnar Hergum, IET

Abstract

This paper contains the analysis, development, production and testing of a surveillance system for the monitoring of the MKDG, a high voltage pulse kicker in the MKD-system. The MKD-system is a part of the LHC Beam Dump System situated at point 6 in the LHC. The surveillance is active whenever the MKDs are operational.

The system is reporting any deviations from normal behaviour and runs an extensive analysis of the MKDG whenever there is a beam dump. The results are checked before a new run in the LHC can be initiated.

The final result is a working prototype which monitors and analyzes the MKDG and communicates the results to a PLC. The accomplished resolution is 10 bits for all six channels and this is acceptable.

Preface

This master thesis is a conclusion of my 9 month stay at CERN and my time as a student at NTNU.

The work on this thesis has been the greatest educational and personal experience in my life. Just to get the opportunity to create something for the largest machine in the world, here at CERN, and to do this in wonderful countries like France and Switzerland has been extraordinary.

I want to thank Etienne Carlier for giving me directions and responsibility and for trusting my choices along the way. I also want to thank Nicolas Voumard and Gregor Grawer for helping me on the technical part; they have been a great resource.

Last I wish to thank Øystein Midttun and Torbjørn Houge for introducing me to the world of Telemark-skiing, and making my winter sport experiences complete!

Prévessin, 6th October 2006

Øyvind Aakvik

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Abbreviations

Ac	Acquisition
ADC	Analog-to-Digital Converter
BGA	Ball-Grid Array
CERN	Conseil Européen pour la Recherche Nucléaire - European Organization for Nuclear Research
Comp	Compensation
DPRAM	Dual-Port Random Access Memory
Ev	Evaluation
eV	electron Volts
FPGA	Field-Programmable Gate Array
FreeW	Free-wheel
G	Giga = 10^9
IPOC	Internal Post Operation Check
KPS	Kicker Pulse Surveillance
LBDS	LHC Beam Dump System
LHC	Large Hadron Collider
MKD	Magnet Kicker Dump
MKDG	MKD generator
Opamp	Operational amplifier
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
Prin	Principal
SMD	Surface Mounted Device
T	Tera = 10^{12}
VHDL	VLSI Hardware Description Language
VLSI	Very Large Scale Integrated circuit

1 Introduction

This chapter starts with an introduction of CERN and step by step narrowing it down and in the last section of this chapter, ending up in a description of the field of interest for this project. The content of this chapter is just to introduce CERN, the LHC and its dump-systems to the reader.

1.1 CERN

CERN (Conseil Européen pour la Recherche Nucléaire) is the world's largest particle physics laboratory. It was founded back in 1954, formed as collaboration between 12 countries with a goal to gather the intellect of the nations and create a centre of nuclear research. This collaboration has expanded over the years, and there are now 20 member states. These member states are funding the projects and are therefore allowed to contribute in the decision-making process of the Council. There are also many countries and organizations which are involved as observers, which means that they are not in any way involved in the decision-making, but only observe and participate in projects at CERN.

Figure 1. Building 40 and 39 on the Meyrin-site of CERN.

There are at the moment a little less than 3000 employees at CERN, additionally there are 6500 visiting personnel, representing 500 different universities and over 80 different countries, doing research at CERN. The newest accelerator project at CERN is the development of the Large Hadron Collider (LHC).

1.2 LHC

The Large Hadron Collider (LHC) is the name of the world's largest machine ever. The particle accelerator is being built in a circular tunnel 27 km in circumference. This tunnel is situated between 50 to 175 meters underground, in which straddles the Swiss and French borders on the outskirts of Geneva. The same tunnel originally housed the accelerator for the LEP project, which was terminated and removed form the tunnel in 2005.

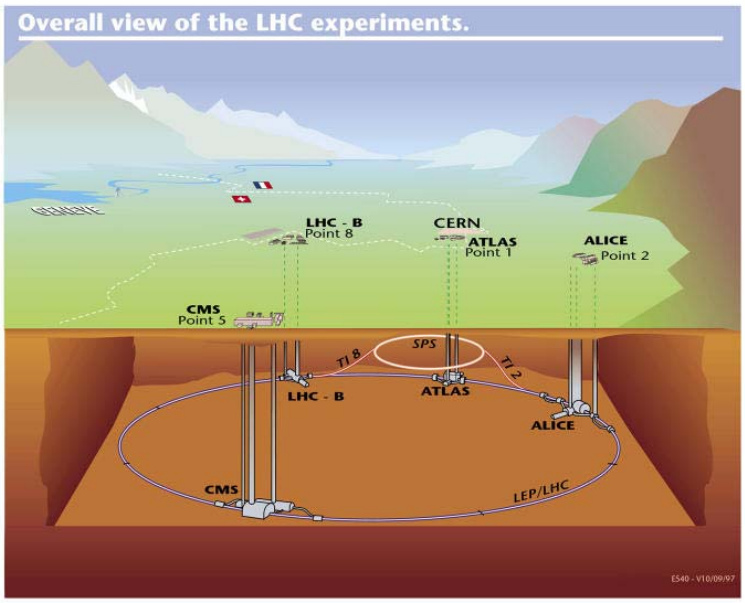

Figure 2. Overall view of the LHC experiment.

The purpose of the LHC is to collide two counter rotating beams of protons or heavy ions. The purpose is to make them collide inside one of the four detectors (Alice, Atlas, CMS and LHCb) places around the ring. Proton-proton collisions are foreseen at energies of 7 TeV per beam. The project is expected to be operational in autumn 2007.

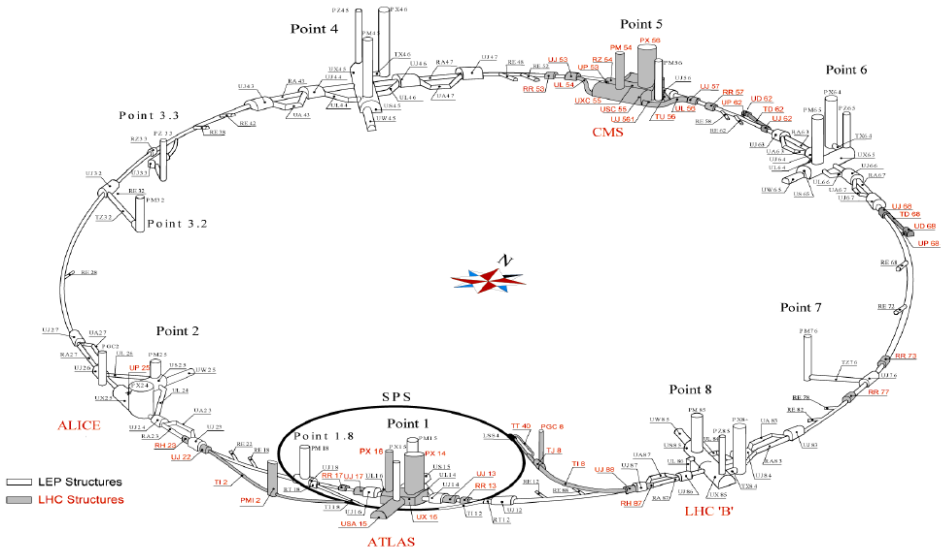

Figure 3. LEP and LHC underground structures.

The accelerator is using super-conductive magnets to guide and accelerate the two counter-rotating particle beams in the ring. Traveling close to the speed of light, it takes the beam less than 90μs to complete one lap in the 27km long accelerator. Each beam has a particle-free gap of 3μs.

The high amount of energy of the beams makes absolute control of them at all times necessary. Should the beams deviate from their path around the ring, this could result in severe or even fatal equipment damage.

1.3 LBDS

The LHC Beam Dumping System (LBDS) is the safety net of the LHC. This is located at Point 6, situated up to the right in Figure 3. At the end of a physics run or in case of emergency, both beams must be extracted from the accelerator and lead into two separate dump block caverns placed approximately a kilometre away from where the beam leaves the accelerator. A schematic layout of the LBDS can be seen in Figure 4. These dump blocks are built to fully absorb the energy of the beam. The pattern made by the beam on the dump blocks will look like the one shown in Figure 5. The reason of this shape is that the beams are being diluted to spread the beams energy over a larger impact area.

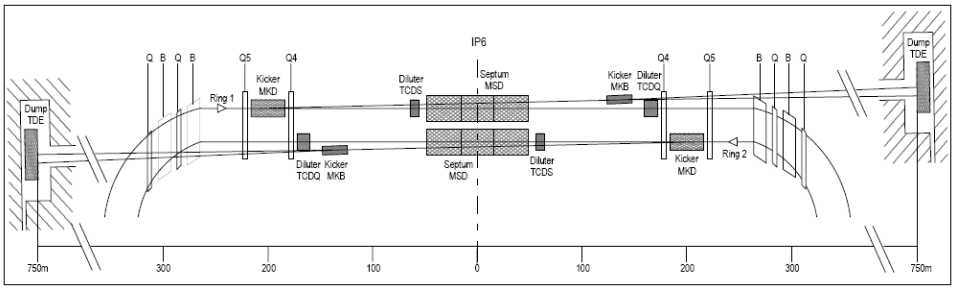

Figure 4. Schematic top view layout of beam dumping system elements around LHC point 6.

To extract the beams, 15 electro-magnets for each beam are placed side by side, which combined deliver a magnetic force strong enough to divert the beam from the ring and into the dump blocks. To avoid partial deflection of the beam, each of the magnets must be turned on in the 3μs particle-free gap.

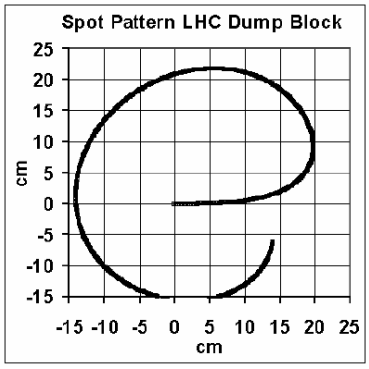

Figure 5. Beam spot figure on absorber block.

The current into the extraction magnets are provided by high-voltage kicker generators, the generator is called a Magnet Kicker Dump Generator (MKDG). When a beam dump is requested it is crucial that at least 14 of the 15 generators

are functional. If not, the beam is not properly extracted. The locations of the MKD-systems are at the two 200 meter marks in Figure 4.

To verify that each of the 15 high-voltage pulse generators is fully functional a system to analyze each generator after each run is required. Any small deviations from normal behaviour can then be detected and checked before the next run is initiated.

1.4 MKD

The Magnet Kikcer Dump (MKD) is a system consisting of a pulse-generator and an electromagnet. Its task is to horizontally deflect the beam and to send it in the direction of the dump caverns called TCDS. When this is done by 15 MKDs together the beam is extracted completely. Each electromagnet is deflecting the beam an angle of 0.27 mrad. This means that if one MKD is failing the beam would not be properly deflected. The worst case is if the first of the 15 MKDs is failing. This means that the beam deflection will be just below 92% of the total, resulting in possible damage to the LBDS-system. It is therefore crucial that all the 15 MKDs are working.

1.5 MKDG

The Magnet Kicker Dump Generator (MKDG) is a high-voltage pulse generator. Its purpose is to deliver a high-voltage pulse to the extraction kicker magnets. This pulse has to reach its maximum value in the time of the particle-free gap in the beam. The MKDG is built with redundancy and contains two equal branches which can cover for each other if one is malfunctioning. This means that at maximum beam energy level and normal behaviour the MKDG is only working at half of what it is capable of, meaning less strain on the electronics and a higher durability.

Each branch can be divided into sub-circuits; these are called the principal-, the compensation- and the free-wheel circuit. The different sub-circuits are illustrated in Figure 6. Each of these sub-circuits has a current pickup sensing the current going through. In sum, there are six current pickups that can be utilized for the analysis of the MKDG. The functional description of the generator falls outside the scope of this paper.

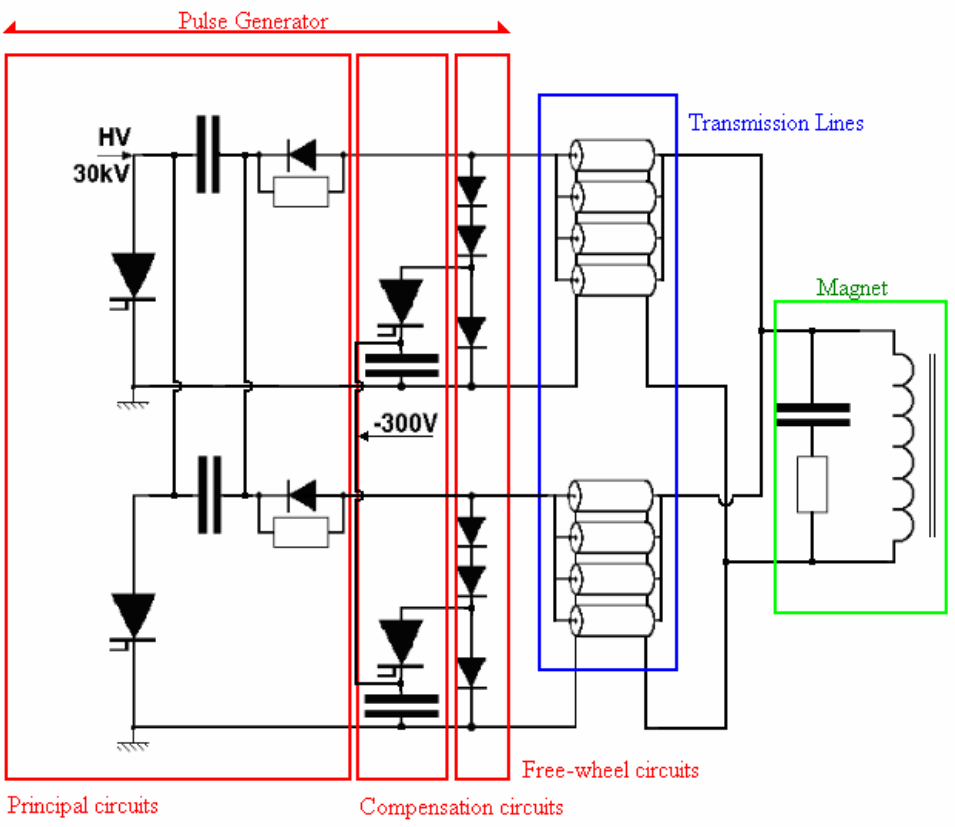

Figure 6. Dual branch generator circuit principal layout.

2 System requirements

The Kicker Pulse Surveillance (KPS) is to handle the Internal Post Operation Check (IPOC) of a Magnet Kicker Dump Generator (MKDG) in the Magnet Kicker Dump-System (MKD-system).

The task is to develop a full functional prototype, able to acquire the six output signals from the MKDG, to analyze them and then communicate the results to a PLC via a Profibus DP-network.

The firmware on the KPS has to be implemented in VHDL, and the code has to be structured as a state machine with a finite lifecycle. The system should have to be rearmed before use after an analysis. It will spend most of its time in a wait-state, waiting for the MKDG to pulse.

The KPS has to be able to adjust the analysis to the beam energy level and the margins of tolerated error communicated over the Profibus DP-network.

The KPS has to be able to make a thorough analysis of the MKDG to ensure that it is ready for a new run.

The system has to be able to handle and acquire input voltages from -33V up to 55V, and be able to withstand in a worst case scenario input voltages from -66V up to 100V.

The whole system should be fitted on a 160mm x 100mm sized printed circuit board (PCB).

3 Preliminary Studies

3.1 Introduction

This chapter present this projects earliest conducted studies, before starting the design of the Kicker Pulse Surveillance-prototype (KPS). It contains a complex study of six outputs on the MKDG and some information on the programmable device and the communication interface.

3.2 Tools

The tools used for the preliminary studies were an oscilloscope with a data-output terminal and a computer with Matlab. The oscilloscope provided the raw-data for the analysis. Matlab and Excel were used for the processing, analysis and for drawing and displaying plots.

3.3 Measurements on the MKDG

This section presents the measurements conducted on the MKDG. The section is the base for the designing of the analog hardware and the digital firmware. The plots in sections 3.3.1, 3.3.2 and 3.3.3 shows the behaviour of the currents in the pick-ups named CTs1, CTc1 and CTf1 respectively. The pickup names are from the “MKD system, Extended Circuit Diagram – High Voltage Power Part” – schematics [8]. The objective of these measurements is to characterize the different parts of the MKDG.

3.3.1 Principal Circuit

The plots in Figure 7 and Figure 8 illustrates the behaviour of the voltage in the pickup induced by the currents in the principal circuit for branches A and B and Figure 9 shows the current in the two branches together, for comparison. The currents are measured at nine different beam energy levels, starting at 450 GeV, which is the injection beam energy level, hence the lowest for the LHC, and ending at 7 TeV, which is theoretically the highest beam energy level for the LHC.

The sensitivity of the pickup is 10 mV/A, resulting in a 5 mV/A sensitivity on the output of a 50Ω terminated transmission line.

The range of the signal is as Figure 9 shows, from approximately +50 V to -30 V. The input range should at least be 80 V. The ground level of the signal is at 3/8 of the total range.

There is a factor of 16 from the lowest input signal to the highest. This change can be represented is 4 bits.

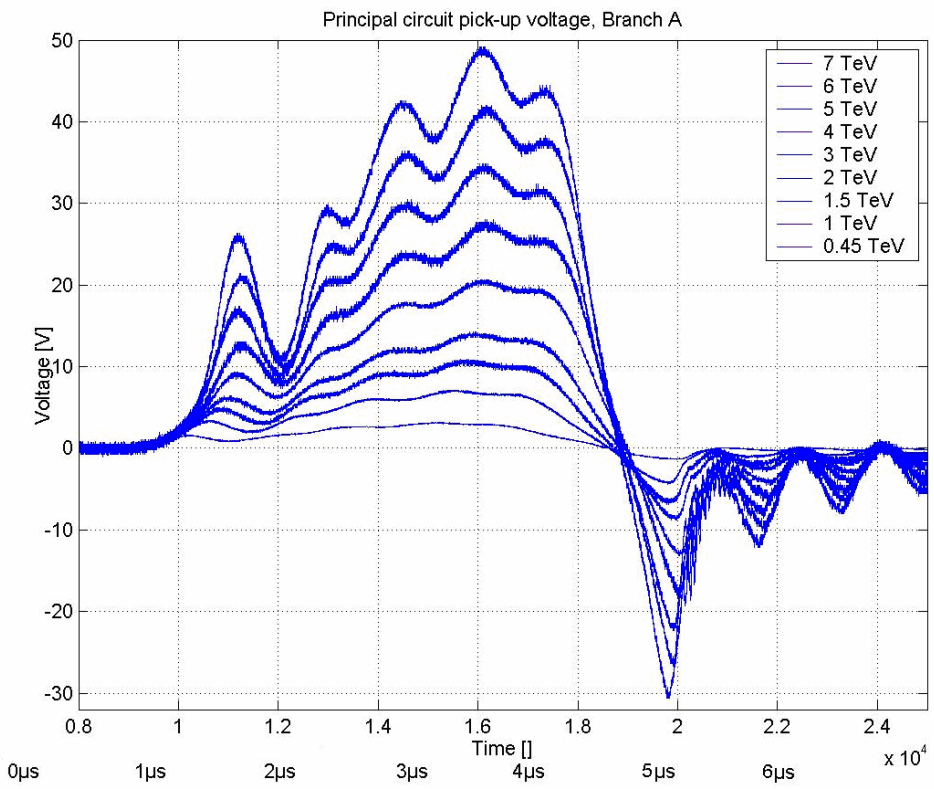

Figure 7. Principal circuit pick-up voltage, Branch A. The lowest graph is for the 450 GeV and the highest for the 7 TeV.

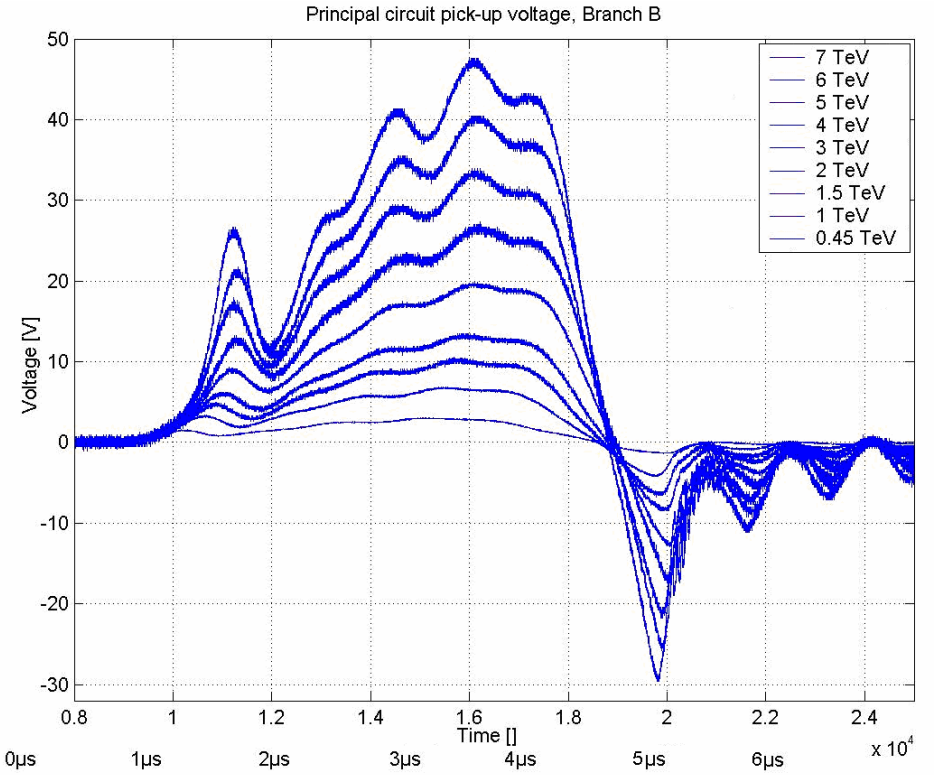

Figure 8. Principal circuit pick-up voltage, Branch B. The lowest graph is for the 450 GeV and the highest for the 7 TeV.

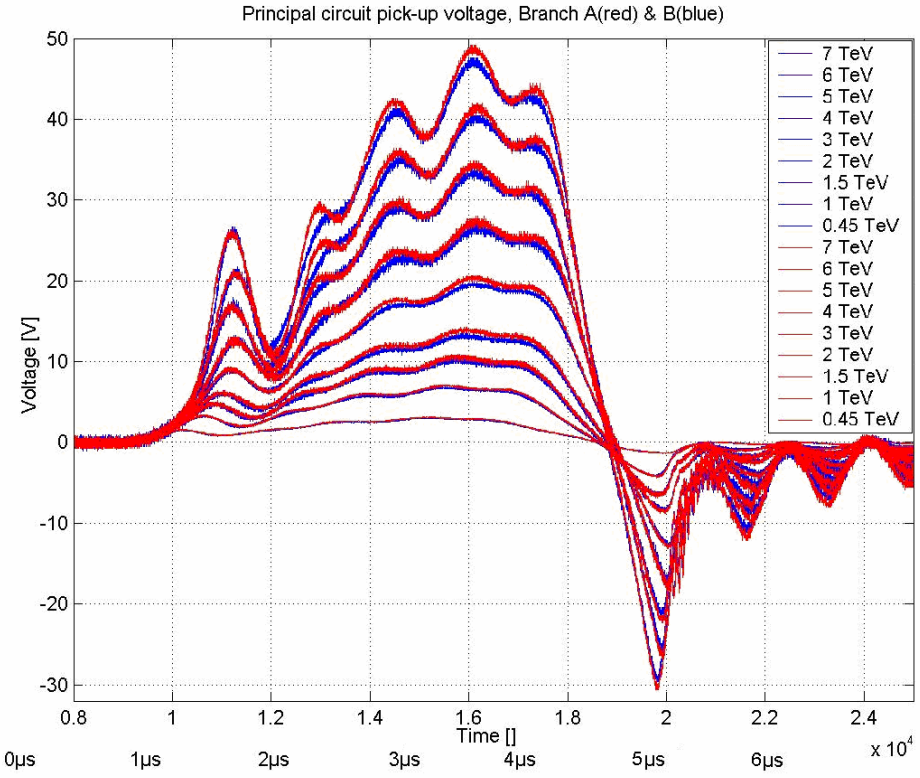

Figure 9. Principal circuit pick-up voltage, Branch A(red) and B(blue)

3.3.1.1 Measurements Analysis

The required analyses on the principal circuits are to confirm that both the positive and the negative peak currents through the pick-ups are within the margins and to confirm that the positive peak currents are at maximum before 4 μs.

3.3.1.1.1 Analog Domain

Processing of the measurements reveals that the maximum and minimum amplitudes are linearly proportional with respect to the beam energy levels. These dependencies can be seen in Figure 10 and Figure 11. Calculations show that these graphs are above 99% linear and have a crossing through origo.

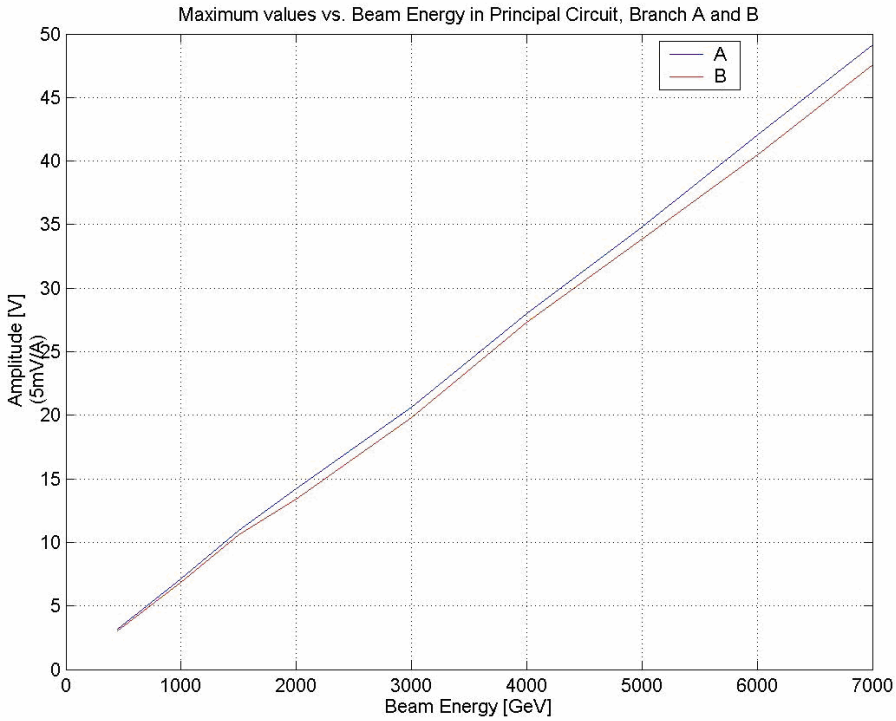

Figure 10. Maximum values of both branches w.r.t. beam energy.

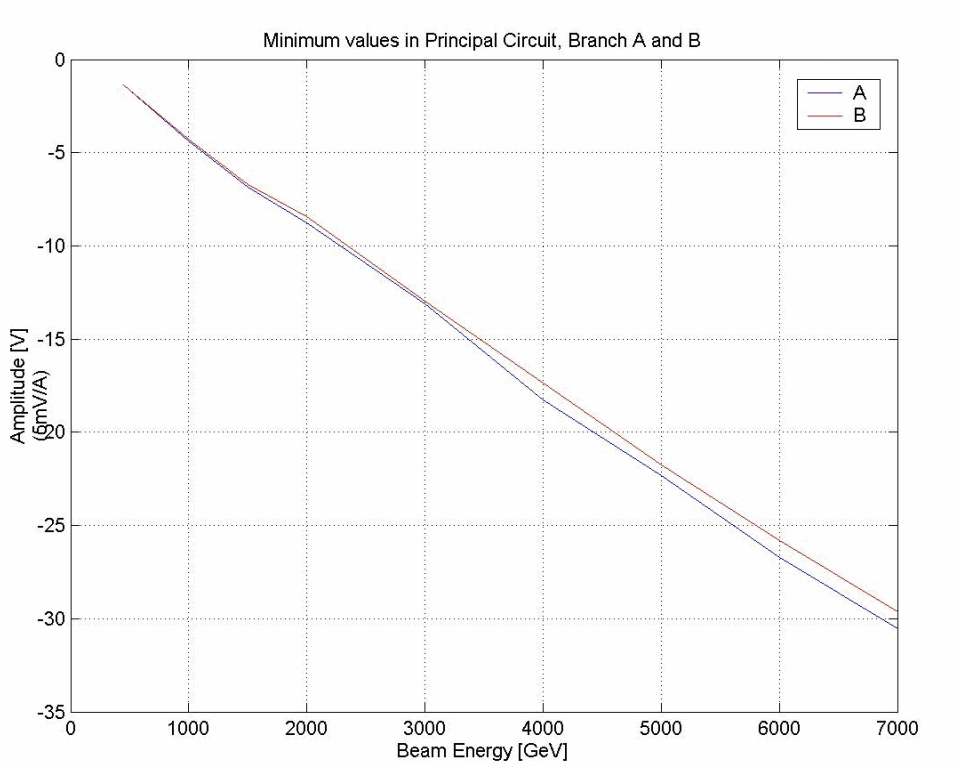

Figure 11. Minimum values of both branches w.r.t. beam energy.

Figure 10 shows the maximum amplitude of the two branches with respect to the beam energy, when both are pulsing. The linearity of the current with respect to the beam energy is appreciated and will simplify the implementation of the analysis in hardware.

The function for the plot in Figure 10 is:

$$\text{Maximum values}[\text{V}] = \frac{52\ \text{V}}{7500\ \text{GeV}} * \text{BeamEnergy}[\text{GeV}]$$

The function for the plot in Figure 11 is:

$$\text{Minimum values}[\text{V}] = \frac{32\ \text{V}}{7500\ \text{GeV}} * \text{BeamEnergy}[\text{GeV}]$$

The functions are interpolated to 7500 GeV to ease the implementation in hardware, since 7500 GeV corresponds to FFFF_{hex} in digital representation. The obtained functions are middling functions, made from the values of both branches.

These functions are only to be used in the computation of the margins for the deviation within the branches. This means that these functions are to be multiplied with the allowed percentage of deviation within the branches. Since the linearity of the plot is not total, the set percentage for the margins may have a

deviation of about 1%. This means that setting the margins to 10%, can at some beam energy levels mean that the actual margin is only 9% or as much as 11%.

The range of the signal on the input is as previously mentioned from approximately +50V to -30V, but this is for 7 TeV, the system has to take into account the possibility of the generator pulsing at 7.5 TeV. To do this an additional 10% is added, making the input signal range approximately from +55V to -33V. The total range is then approximately 88V.

3.3.1.1.2 Digital domain

The analog input signal range has to be annotated down to a small signal electronics level before entering the converter:

$$\text{Input annotation} = \frac{\text{Maximum input range of input signal}}{\text{Maximum input range of converter}} = \frac{88\,\text{V}}{4\,\text{V}} = 22\ \text{times}$$

If using a 12 bit ADC the resolution of the measurements is:

LSB: $$\frac{88\,\text{V}}{2^{12}} = 21.4\,\text{mV}$$

If the ADC is 12 bits there is no need for all the 16 bits of resolution that the beam energy are presented in. This is solved by looking at the 12 MSB of the beam energy. The range of the beam energy, as with the output of the converters will then be $000_{hex} - FFF_{hex}$ or $0_{dec} - 4095_{dec}$.

There are three functions necessary for the principal circuit. The first function is for the acquisition. This is the threshold for detecting that there is current in the pickup. It is set to approximately 50% of the maximum of the pulse with respect to the beam energy. The second and third function is for the analysis. These functions output the margins for the allowed deviation between the two branches.

Equation 1. Threshold function in binary:

$$\text{Trigger - level[LSB]} = \frac{2}{8} * \text{BeamEnergy[GeV]}$$

Equation 2. Maximum-value function in binary:

$$\text{Maximum - value conversion, analog to digital} \Rightarrow$$

$$\frac{\text{Maximum - value}}{\text{LSB}} = \frac{52\ \text{V}}{21.4\ \text{mV}} = 2442\ \text{LSB}$$

$$\text{Maximum - value margin[LSB]} = \frac{2442}{4095} * \text{Beam Energy[GeV]} * \frac{\text{Margin[\%]}}{100}$$

$$\text{Maximum - value margin[LSB]} = \frac{2442}{4095 * 100} * \text{Beam Energy[GeV]} * \text{Margin[\%]}$$

$$\text{Maximum - value margin[LSB]} \approx \frac{49}{2^{13}} * \text{Beam Energy[GeV]} * \text{Margin[\%]}$$

Equation 3. Minimum-value function in binary:

$$\text{Minimum - value conversion analog to digital} \Rightarrow$$

$$\frac{\text{Minimum - value}}{\text{LSB}} = \frac{32\text{V}}{21.4\text{mV}} = 1503\ \text{LSB}$$

$$\text{Minimum - value margin[LSB]} = \frac{1503}{4095} * \text{Beam Energy[GeV]} * \frac{\text{Margin[\%]}}{100}$$

$$\text{Minimum - value margin[LSB]} = \frac{1503}{4095} * \text{Beam Energy[GeV]} * \frac{\text{Margin[\%]}}{100}$$

$$\text{Minimum - value margin[LSB]} = \frac{1503}{4095 * 100} * \text{Beam Energy[GeV]} * \text{Margin[\%]}$$

$$\text{Minimum - value margin[LSB]} \approx \frac{15}{2^{12}} * \text{Beam Energy[GeV]} * \text{Margin[\%]}$$

3.3.2 Compensation circuit

The plot in Figure 12 illustrates the behaviour of the voltage in the pickup induced by the currents in the compensation circuit for branch B. The current is measured at nine different beam energy levels, starting at 450 GeV, which is the injection beam energy level for the LHC, and ends at 7 TeV, which is the highest beam energy level.

The sensitivity of the pickup is 1 mV/A, resulting in a 0.5 mV/A sensitivity on the output of a 50Ω terminated transmission line.

The range of the signal is as Figure 12 shows, from 0 V to approximately 9.5 V. This is when the spike at the beginning is excluded. The ground level of the signal is at zero of the total range.

There is a factor of 16 from the lowest input signal to the highest. This change can be represented is 4 bits.

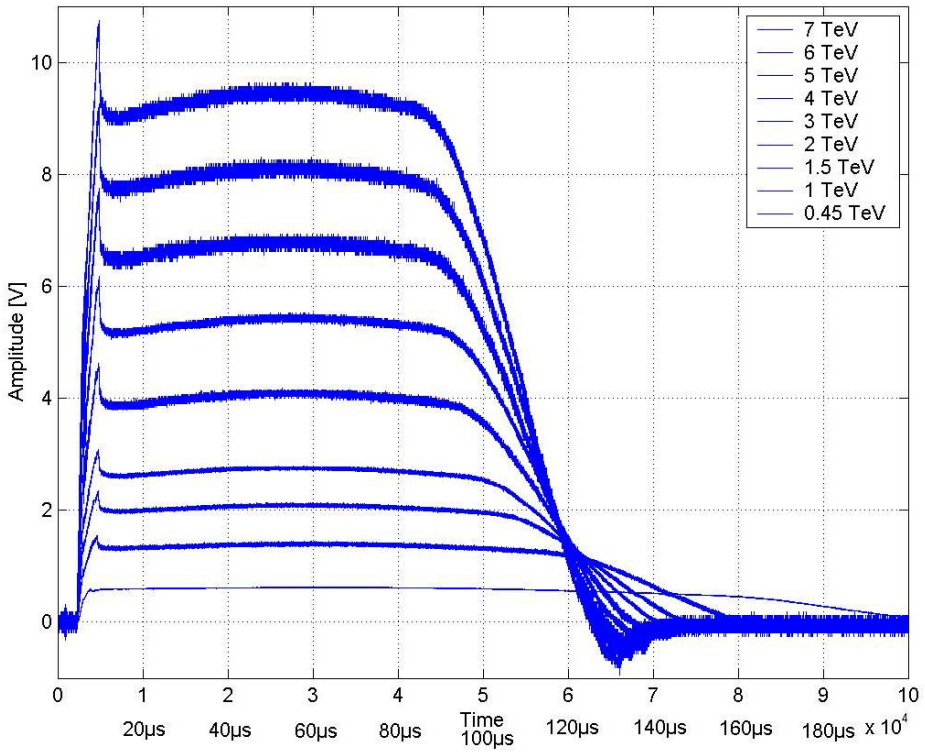

Figure 12. Compensation circuit pick-up voltage for branch B. The lowest graph is for the 450 GeV and the highest for the 7 TeV.

3.3.2.1 Measurements Analysis

The acquisition points needed on the compensation circuit is a confirmation of that the start and stop of the pulse and the maximum value of the midsection on the pulse are within the margins.

3.3.2.1.1 Analog Domain

Processing of the measurements reveals that the behaviour of the midsections maximum amplitude is linearly proportional with respect to the beam energy. This is illustrated in Figure 13. Calculations show that these graphs are above 99% linear and have a crossing through origo.

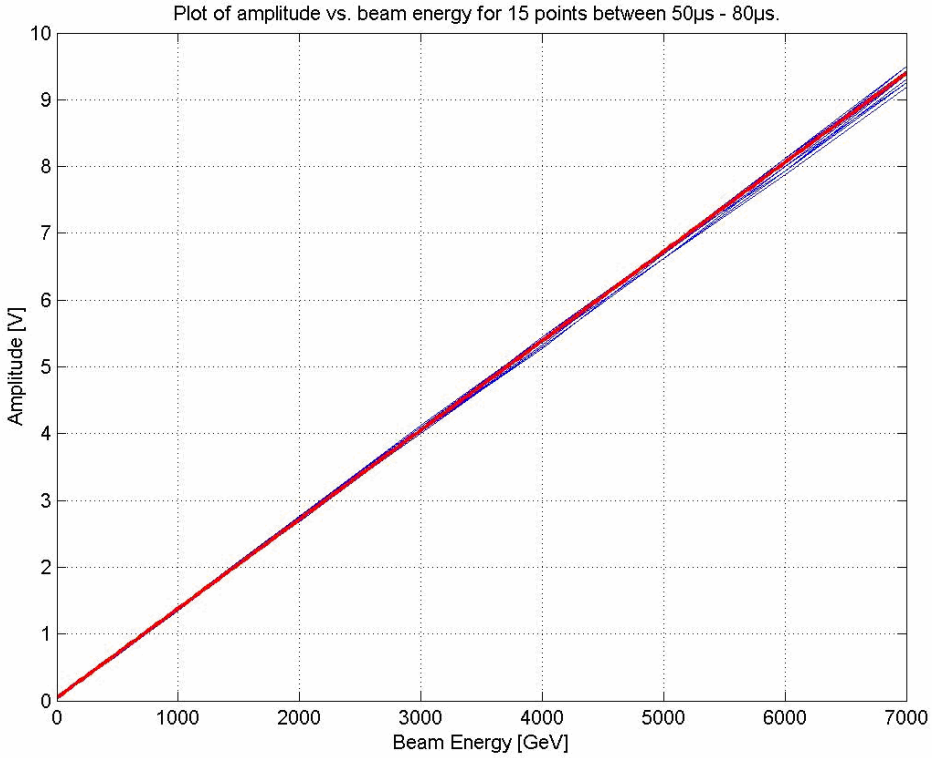

Figure 13. Amplitude vs. beam energy for 15 points between 50µs and 80µs.

Figure 13 shows the amplitude of the midsection of the pulses in Figure 12. The points are taken at 15 different points between 50µs and 80µs and on nine different beam energy levels. The thick (red) line in Figure 13 shows the linear approximation of these points.

The function for the plot in Figure 13 is:

$$\text{Maximum values}[\text{V}] = \frac{10\ \text{V}}{7500\ \text{GeV}} * \text{BeamEnergy}[\text{GeV}]$$

The function is also here, as with the principal circuit, interpolated to 7500 GeV to ease the implementation in hardware, since 7500 GeV corresponds to $FFFF_{hex}$ in digital representation.

The function is only to be used in the computation of the margins for the deviation within the branches. This means that the function is to be multiplied with the allowed percentage of deviation within the branches.

The range of the signal on the input is as illustrated in Figure 8 from approximately 0 V to 9.34 V, but this is for 7 TeV, the system has to take into account the possibility of the generator pulsing at 7.5 TeV. To do this an additional 10% is added, making the input signal range approximately from 0 V to +10.3 V.

The threshold for the triggering of a counter to measure the start and stop of the pulse can be set to half the beam energy level. This can be done since the maximum amplitude at the maximum beam energy level corresponds approximately to the maximum values of the ADC. Meaning that setting the threshold to half the value of the beam energy will be the same as setting the threshold at approximately 50% of the maximum pulse value with respect to the beam energy.

3.3.2.1.2 Digital domain

The analog input signal range has to be annotated down to a small signal electronics level before entering the converter:

$$\text{Input annotation} = \frac{\text{Maximum input range of input signal}}{\text{Maximum input range of converter}} = \frac{10.3\ \text{V}}{4\ \text{V}} = 2.58\ \text{times}$$

If using a 12 bit ADCs the resolution of the measurements is:

LSB: $$\frac{10.3\ \text{V}}{2^{12}} = 2.52\ \text{mV}$$

As in the principal circuit, if the ADC is 12 bits there is no use for all 16 bits of resolution that the beam energy are presented in. Only the 12 MSB of the beam energy are used. The range of the beam energy, as with the output of the converters will then be 000_{hex} – FFF_{hex} or 0_{dec} – 4095_{dec}.

There are two functions necessary for the compensation circuit. The first function is for the acquisition. This is the threshold for triggering a sampling of the start- and the stop-time of the pulse. It is set to approximately 50% of the maximum of the pulse with respect to the beam energy. This function can be made more accurate, but this might not be necessary. The second function is for the analysis. The function outputs the margin for the allowed deviation between the two branches.

Equation 4. Threshold function in binary:

$$\text{Threshold}[\text{LSB}] = \frac{1}{2} * \text{BeamEnergy}[\text{GeV}]$$

Equation 5. Maximum-value function in bits:

$$\text{Maximum - value conversion analog to digital} \Rightarrow$$

$$\frac{\text{Max Value}}{\text{LSB}} = \frac{10\,\text{V}}{2.52\,\text{mV}} = 3968\,\text{LSB}$$

$$\text{Maximum - value margin}[\text{LSB}] = \frac{3968}{4095} * \text{BeamEnergy}[\text{GeV}] * \frac{\text{Margin}[\%]}{100}$$

$$\text{Maximum - value margin}[\text{LSB}] = \frac{3968}{4095 * 100} * \text{BeamEnergy}[\text{GeV}] * \text{Margin}[\%]$$

$$\text{Maximum - value margin}[\text{LSB}] \approx \frac{5}{2^9} * \text{BeamEnergy}[\text{GeV}] * \text{Margin}[\%]$$

3.3.3 Free-Wheel Circuit

The plots in Figure 14 and Figure 15 illustrates the behaviour of the voltage in the pickup in the branches A and B, as a function of time at different beam energy levels. Figure 16 shows both functions in one plot. A zoom in on the spikes in the first 10μs of these three plots are depicted in Figure 17. The current is measured at nine different beam energy levels, from 450 GeV to 7 TeV.

The sensitivity of the pickup is 2 mV/A, resulting in a 1 mV/A sensitivity on the output of a 50Ω terminated transmission line.

The range of the signal is as Figure 12 shows, from 0 V to approximately 4.9 V. This is when the spike at the beginning is excluded. The ground level of the signal is at zero of the total range.

There is a factor of 16 from the lowest input signal to the highest. This change can be represented is 4 bits.

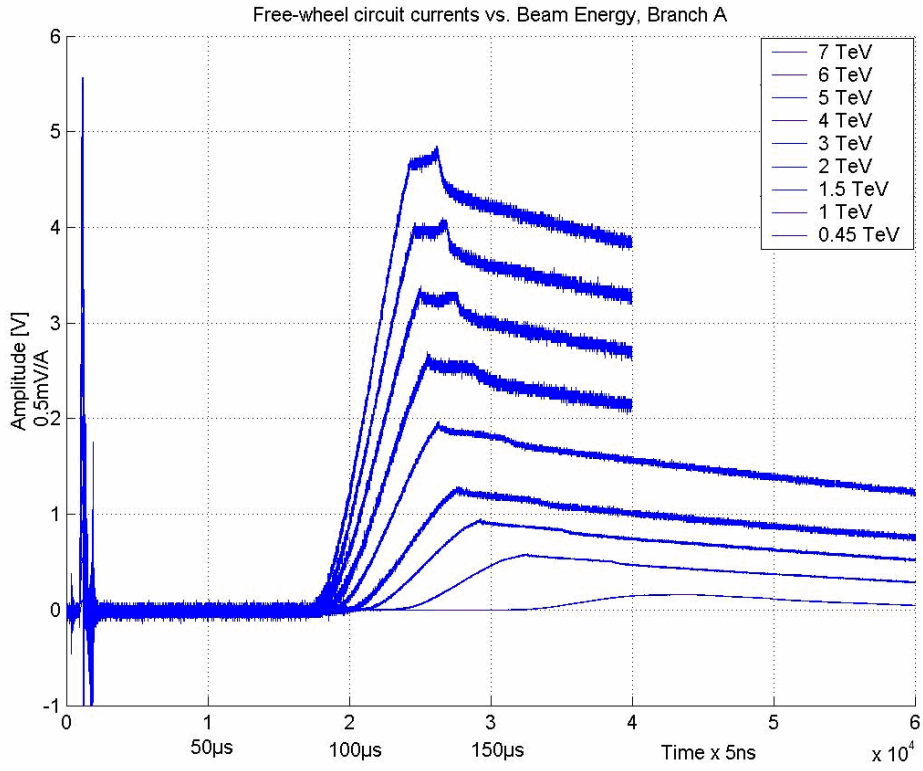

Figure 14. Free-wheel circuit currents vs. Beam Energy, Branch A. The lowest graph is for the 450 GeV and the highest for the 7 TeV.

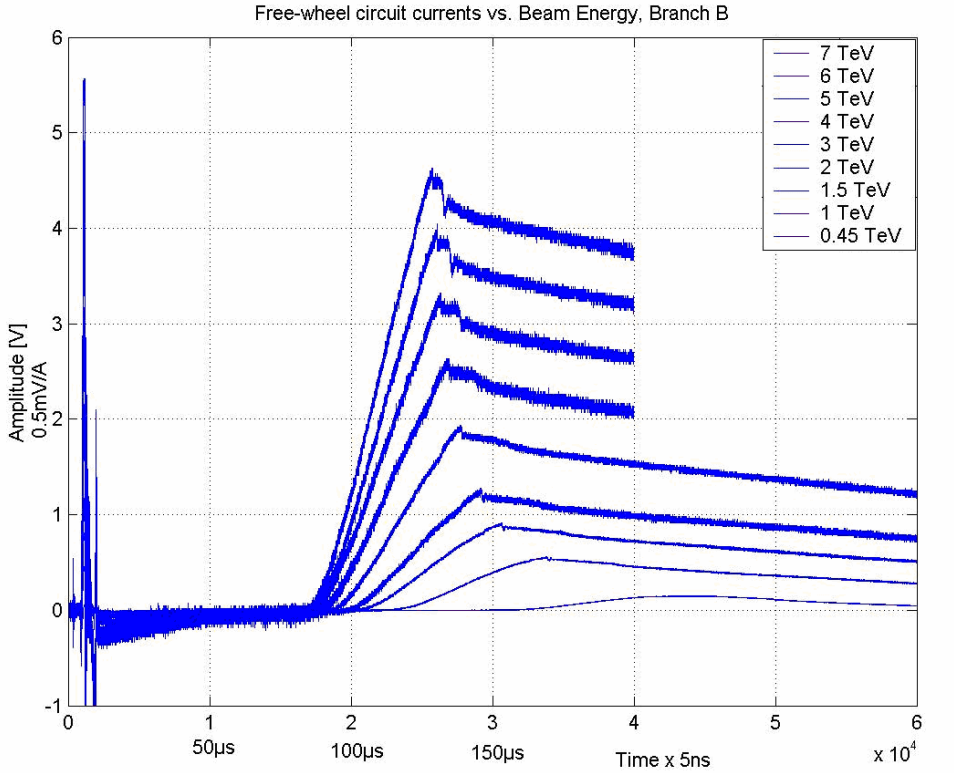

Figure 15. Free-wheel circuit currents vs. Beam Energy, Branch B. The lowest graph is for the 450 GeV and the highest for the 7 TeV.

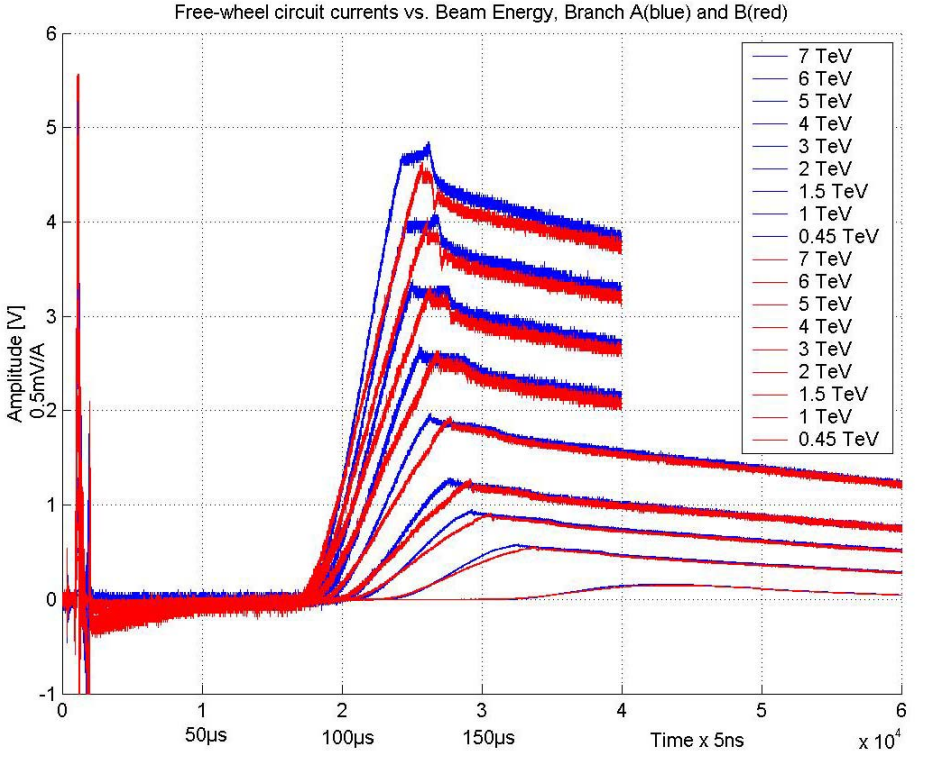

Figure 16. Free-wheel circuit currents vs. Beam Energy, Branch A(blue) and B(red)

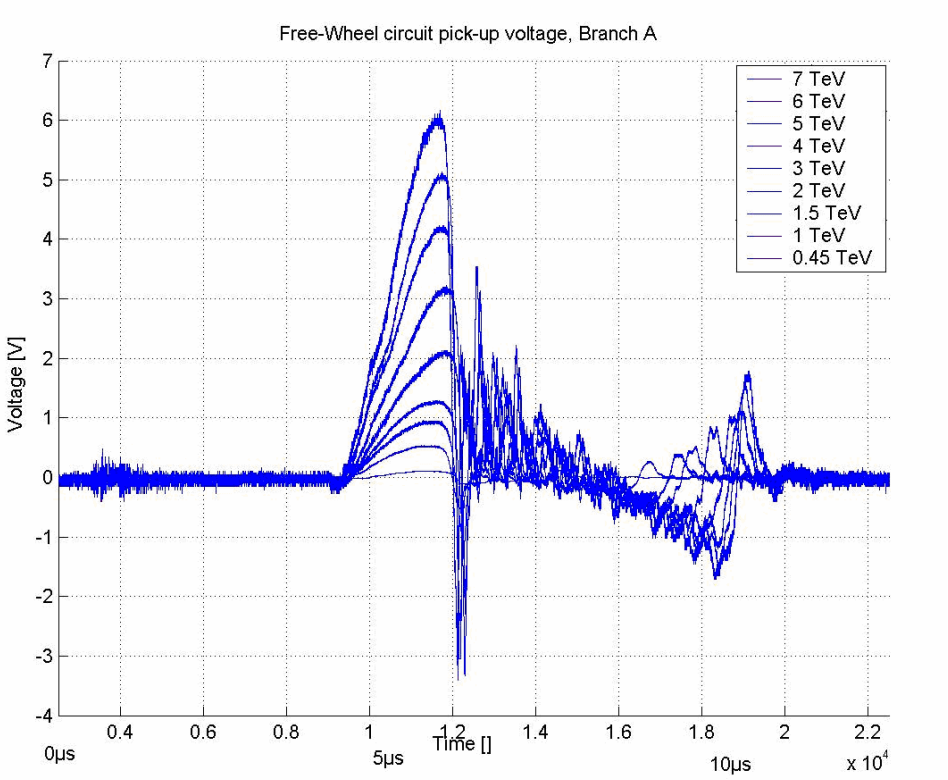

Figure 17. Free-wheel circuit currents vs. Beam energy, branch A, zoom on start-spike. The lowest graph is for the 450 GeV and the highest for the 7 TeV.

3.3.3.1 Measurements Analysis

The required analysis on the free-wheel circuit is to confirmation that the first and then the second pulse comes simultaneously in the two branches, that there are now current in the section between the two pulses and that the maximum value of the second pulse is within the margins.

3.3.3.1.1 Analog domain

Processing of the measurements reveals that the behaviour of the second pulse maximum amplitude with respect to the beam energy is linearly proportional with respect to the beam energy levels. This is illustrated in Figure 18. The linear approximation to the measurement is close to 100% accurate.

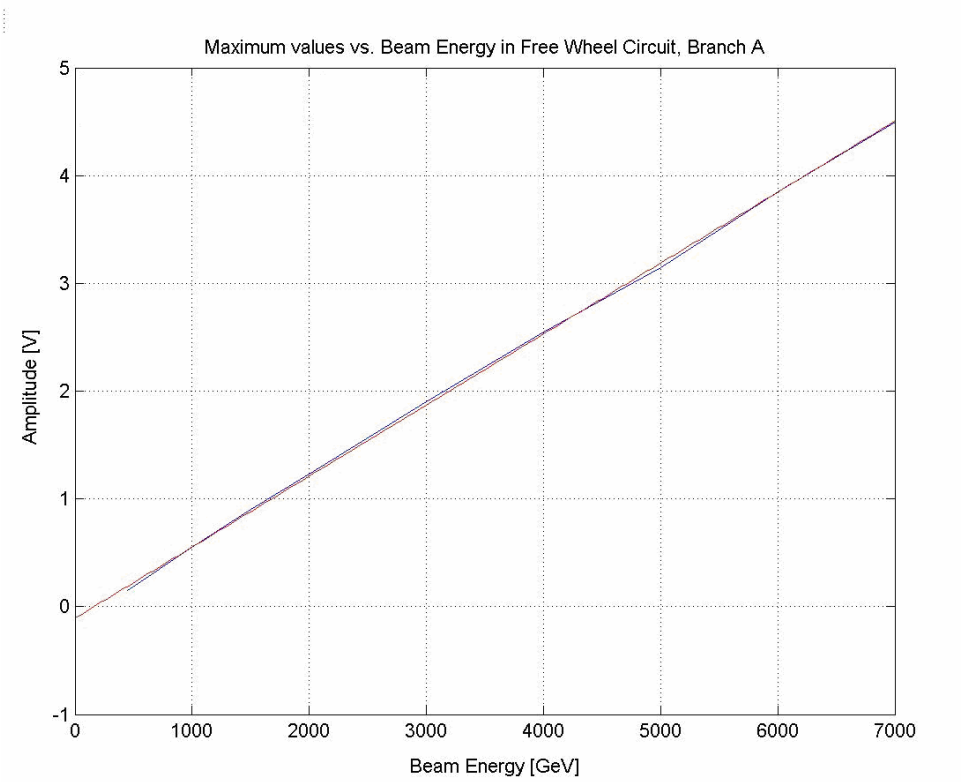

Figure 18. Maximum values vs. beam energy in Free-wheel circuit in branch A(blue), and linear approximation function(red).

Figure 18 shows the maximum amplitude of the second pulse starting at about 90μs in Figure 16. The function is not totally linear so a linear approximation has been made. This is laid on top(red) of the point of the maximum amplitude(blue).

The function for the plot in Figure 18 is:

$$\text{Maximum values}[\text{V}] = \frac{5.4\ \text{V}}{7500\ \text{GeV}} * \text{BeamEnergy}[\text{GeV}]$$

The function is also here, as with the principal and compensation circuit, interpolated to 7500 GeV to ease the implementation in hard-ware, since 7500 GeV corresponds to FFFF_{hex} in digital representation.

The function is only to be used in the computation of the margins for the deviation within the branches. This means that the function is to be multiplied with the allowed percentage of deviation within the branches.

The range of the signal on the input is as illustrated in Figure 17 from approximately 0 V to 4.9 V, but this is for 7 TeV, the system has to take into account the possibility of the generator pulsing at 7.5 TeV. To do this an additional 10% is added, making the input signal range approximately from 0 V to +5.4 V.

The threshold for the triggering of a counter to measure the start of the two pulses, the thresholds can also here as with the compensation circuit, be set to half the beam energy level. This can be done since the maximum amplitude at the maximum beam energy level corresponds approximately to the maximum values of the ADC. Meaning that setting the threshold to half the value of the beam energy will be the same as setting the threshold at approximately 50% of the maximum pulse value with respect to the beam energy.

3.3.3.1.2 Digital Domain

The analog input signal range has to be annotated down to a small signal electronics level before entering the converter:

$$\text{Input annotation} = \frac{\text{Maximum input range of input signal}}{\text{Maximum input range of converter}} = \frac{5.4\,\text{V}}{4\,\text{V}} = 1.35 \text{ times}$$

If using a 12 bit ADCs the resolution of the measurements is:

LSB: $$\frac{5.4\,\text{V}}{2^{12}} = 1.32\,\text{mV}$$

The used ADCs are 12 bits so there is also here no point in using all 16 bits of resolution that the beam energy are presented in. This is solved by looking at the 12 MSB of the beam energy. The range of the beam energy is $000_{hex} - FFF_{hex}$ or $0_{dec} - 4095_{dec}$.

There are three functions necessary for the free-wheel circuit. The first two functions are for the acquisition; one for the threshold for sampling the start-time of the two pulses and the other for the threshold for the no pulse section. The threshold for the first and second pulse is set to approximately 50% of the maximum of the pulse with respect to the beam energy. This function can be made more accurate, but this might not be necessary. The third function is for the analysis. This is linearly proportional to the beam energy and output the margins for the allowed deviation between the two branches.

Equation 6. First and second threshold function in binary:

$$\text{Threshold[LSB]} = \frac{1}{2} * \text{BeamEnergy[GeV]}$$

Equation 7. No pulse section threshold function in binary:

$$\text{Threshold[LSB]} = \frac{1}{2^6} * \text{BeamEnergy[GeV]}$$

Equation 8. Maximum-value function in binary:

$$\text{Maximum - value conversion, analog to digital} \Rightarrow$$

$$\frac{\text{Max Value}}{\text{LSB}} = \frac{4.82\ \text{V}}{1.32\ \text{mV}} = 3652\ \text{LSB}$$

$$\text{Maximum - value margin[LSB]} = \frac{3652}{4095} * \text{BeamEnergy[GeV]} * \frac{\text{Margin[\%]}}{100}$$

$$\text{Maximum - value margin[LSB]} = \frac{3652}{4095 * 100} * \text{BeamEnergy[GeV]} * \text{Margin[\%]}$$

$$\text{Maximum - value margin[LSB]} \approx \frac{9}{2^{10}} * \text{BeamEnergy[GeV]} * \text{Margin[\%]}$$

3.4 FPGA

For these kinds of applications the preferred device to use is a FPGA. The flexibility and low cost makes it a perfect choice for prototyping and minor production quantities.

The use of FPGAs in electronics at CERN is rather common and the most used device in the Electronics Control-section is the Xilinx Spartan 3, XC3S1000-4FT256, thus the knowledge and data on this device is extensive.

3.4.1 Xilinx Spartan 3, XC3S1000-4FT256.

This device has great possibilities. It has:

- 256 pins including power and ground.
- 173 pins can be assigned as in- or outputs.
- 15000 flip-flops and 4-input LUTs.
- 24 block RAMs, each can contain 18kbits.
- 24 18bit multipliers.
- 4 DCM, digital clock managers.
- 1 Boundary Scan.

All this helps making it into a very powerful and user-friendly device. [9]

Figure 19. Picture shows a Xilinx Spartan 3, XC3S1000-4FT256C (17x17mm).

3.5 Profibus DP

The KPS and a PLC are to communicate through an industrial network standard called Profibus DP. Profibus DP is the most used third-party embedded fieldbus standard today. This is because of its robustness and the rather high transfer rates. The maximum transfer rate is 12Mbit/s.

Communication over a Profibus DP-network is common in electronics at CERN, thus the problem has been solved before. It has been solved by using a module provided by HMS Industrial Networks in Sweden. This module is called AnyBus-S and is configured as a slave in this network.

3.5.1 AnyBus-S module

The time saved by using this module is a great advantage in a time-limited design process. This module has a 34 pin connector, using 25 of them to communicate with a FPGA, a CPLD or a microcontroller of any sort. The module is depicted in Figure 20 and Figure 21.

There can be 126 other slaves connected to one master. To utilize 127 slaves, this has to be done in the modules software, this because in hardware the two rotary switches on the front panel only allow 100 different addresses. The interface towards the Profibus DP-network is a 9-pins D-connector. Other interfaces on the module are, as can be seen in Figure 20, two rotary switches and a 34-pin connector as before mentioned, an end termination on/off switch and 4 LEDs, although one of the LEDs are not in use. [5][6]

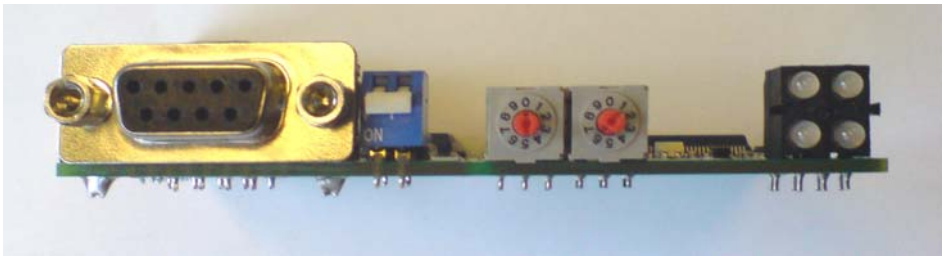

Figure 20. User interface of the AnyBus-S module.

3.5.1.1 Initialization

When powering up the AnyBus-S module, it has to be initialized. This is done by writing three messages to the Mailbox In area, and then verifying the response from the network master, this is read from the Mailbox Out area. The middle one of the three messages contains information about the length of the input and output frames.

The initialization sequence is described in detail in the AnyBus Slave Design Guide [5], alternative 1.

3.5.1.2 Interface

The module is easy to use because the interface to the module is equivalent to that of a RAM. The thing is that the AnyBus-S module interface actually is a Dual-Port RAM, which the user can access on one side and the network can access on the other side. Every time there is an update on this RAM a bit is sat and either the user or the network reads the content of the RAM.

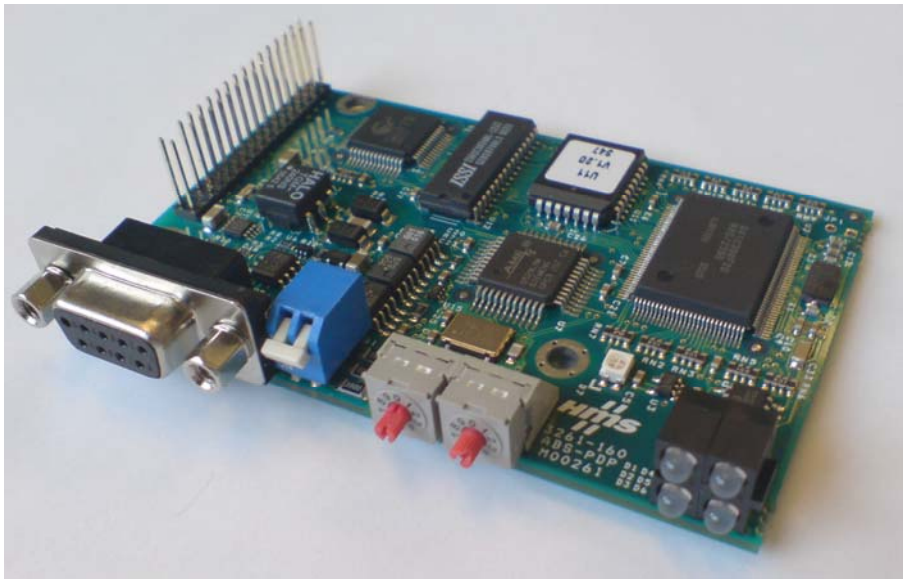

Figure 21. The AnyBus-S module.

4 VHDL Entity description

4.1 Introduction

This chapter presents the structure of the VHDL-code used to configure the FPGA on the KPS. The code is presented in steps starting at the top of the hierarchy, presenting block-diagram, tables and text explaining every sub-entity. The development of firmware for the FPGA was an important part of this project.

4.2 Tools

Xilinx™ ISE 7.1i was used for handling every aspect of the VHDL-code, from code-editing to making the programming-file for the FPGA. The early stage simulations and debugging of the code was done in the ModelSim™ XE III 6.0a Simulator. The finishing touches of debugging was done using ChipScope™ Pro 7.1i, a add-on program for Xilinx™ ISE enabling realtime debugging on the FPGA. This is done my implementing a separate core in the FPGA which communicates with the Chipscope™-application on the PC through the JTAG-interface. Every value inside the FPGA can then be monitored.

4.3 KPS

The Kicker Pulse Surveillance (KPS)-entity is the top-entity containing all firmware descriptions for the FPGA. These descriptions are divided into smaller entities. The system hierarchy of entities is shown in Figure 22 and the entities with connections are illustrated in Figure 23. The entity-names with numbers behind in Figure 22 are instantiated multiple times. The analysis part of the system is designed with 12bits and the transfer part is 8bits.

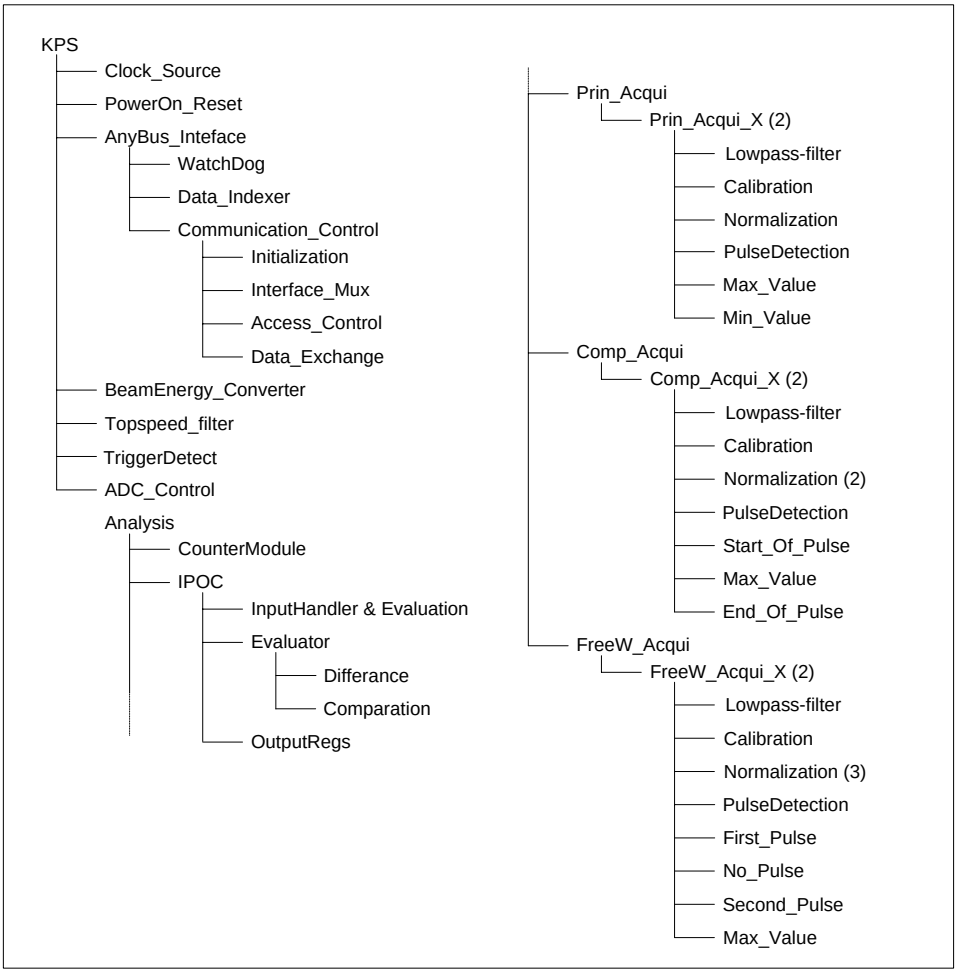

Figure 22. Hierarchical presentation of the entities in the KPS.

There are eight sub-entities in the KPS-entity:

The Clock_Source-entity consists of a Xilinx Clock-DLL. This is providing the FPGA with a clean clock-signal out of the input from the external crystal.

The PowerOn_Reset-entity is making sure that the FPGA is properly reset during power up.

The TriggerDetect-entity detects the triggering pulse and indicates that there has been a triggering until reset.

The Topspeed_filter-entity is an oversampling-filter converting four samples in to one.

The ADC_Control-entity handles the signals concerning the ADCs and the Opamps.

The Analysis-entity is doing all the acquisition and analysis of the input values.

The BeamEnergy_Converter-entity is converting the beam energy level into thresholds and margins used in the acquisition and analysis of the input signals.

The AnyBus_Interface-entity controls the transfers between the external AnyBus-module and the rest of the FPGA.

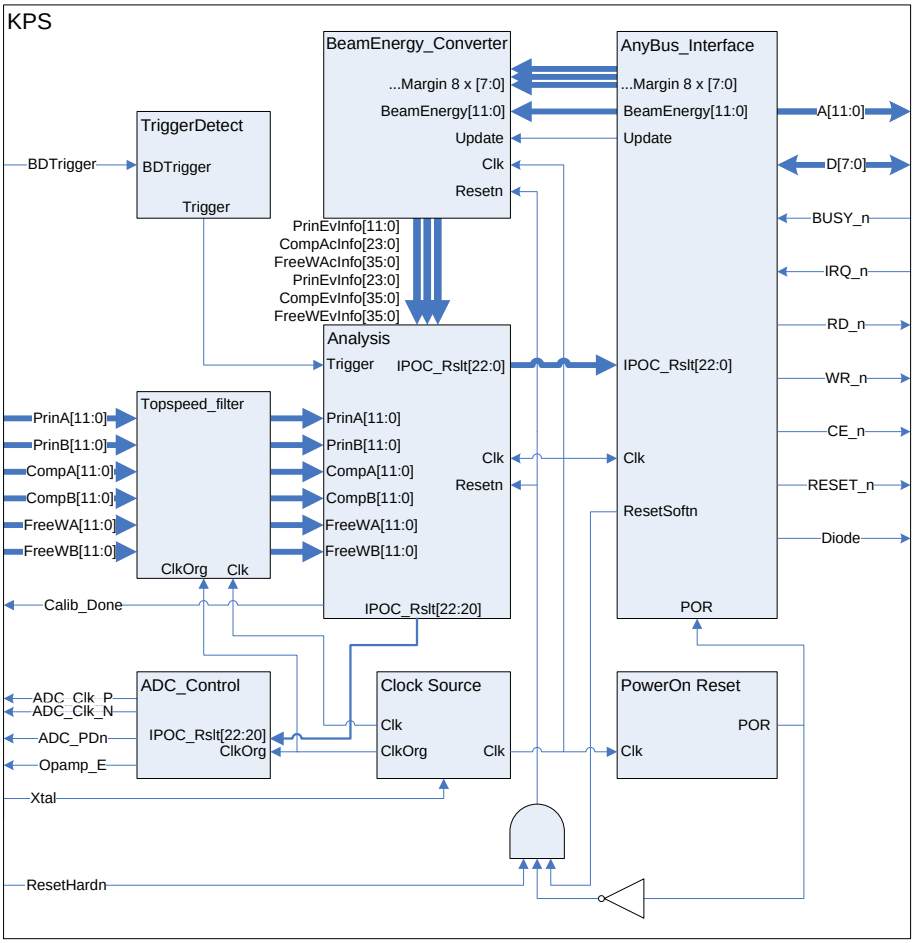

Figure 23. Block diagram of KPS-entity.

Table 1. Description of in- and outputs of the KPS-entity.

BDTrigger	in	Input for beam dump triggering signal.
PrinA[11:0]	in	Signals from the ADC sampling the principal circuit pickups branches A and B.
PrinB[11:0]	in	
CompA[11:0]	in	Signals from the ADC sampling the compensation circuit pickups branches A and B.
CompB[11:0]	in	
FreeWA[11:0]	in	Signals from the ADC sampling the free-wheel circuit pickups branches A and B.
FreeWB[11:0]	in	
Calib_Done	out	Connected to the left-most LED. Signal is high and LED is on when calibration complete.
ADC_Clk_P	out	Positive and negative differential clock signal.
ADC_Clk_N	out	
ADC_PDn	out	To power down ADCs.
Opamp_E	out	To power down the Opamps.
Xtal	in	Input from crystal oscillator.
ResetHardn	in	Input from pushbutton.
A[11:0]	out	For addressing the AnyBus-S module.
D[11:0]	inout	Bidirectional databus for data exchange with the AnyBus-S module.
BUSY_n	in	Control signals for AnyBus-S module.
IRQ_n	in	
RD_n	out	
WR_n	out	
CE_n	out	
RESET_n	out	
Diode	out	Connected to LED, indicates correct initialization of AnyBus-S module.

4.3.1 UserSettings-package

This is a package-file containing all the presets that can be made to the KPS system. These are all constants that set the initial values for registers in some of the many entities.

4.3.2 Clock_Source

This is a sub-entity of the KPS-entity, illustrated in Figure 23. The Clock_Source entity will provide a clock signal to all the entities requiring it. It will utilize the architecture-specific Clock-DLL (Delay-Locked Loop) of the Xilinx Spartan 3 family. The entity will provide a clean, stable clock signal from the hardware crystal oscillator on the board. The Clock-DLL will ensure fast transitions and a 50% duty cycle. It will cancel out any clock delay within the FPGA which minimizes clock skews and timing problems. The entity outputs a 10 and 40 MHz clock-signal.

Table 2. Description of in- and outputs of the Clock_Source-entity.

Xtal	in	Input from crystal oscillator.
Clk	out	10 MHz clock divided and shaped in DCM.
Clk_Org	out	40 MHz clock undivided and shaped in DCM.

4.3.3 PowerOn_Reset

This is a sub-entity of the KPS-entity, illustrated in Figure 23. The PowerOn_Reset-entity will issue a power-on reset (POR) pulse to the AnyBus_Interface-entity to bring it into a known and defined state. The entity will be implemented using registers from the Xilinx Primitives library, which have a known start-up value.

Table 3. Description of in- and outputs of the PowerOn_Reset-entity.

Clk	in	System-clock. 10MHz.
POR	out	Reset signal which stays high for 5 clock-cycles after power on.

4.3.4 TriggerDetect

This is a sub-entity of the KPS-entity, illustrated in Figure 23. The TriggerDetect-entity is set to keep the output high when there has been issued a beam dump. The output returns to low when it is reset.

Table 4. Description of in- and outputs of the TriggerDetect-entity.

BDTrigger	in	Input from the beam dump triggering signal
Trigger	out	Indication of that a beam dump triggering has occurred.

4.3.5 Topspeed_filter

This is a sub-entity of the KPS-entity, illustrated in Figure 23. The Topspeed_filter is working as a bridge between the FPGA and the ADCs, converting four and four samples from the ADCs running at 40MHz to one sample for the FPGA running at 10MHz. Its function is an oversampling filter removing noise from the inputs of the FPGA.

Table 5. Description of in- and outputs of the Topspeed_filter-entity.

Clk	in	System-clock. 10MHz.
ClkOrg	in	Original Clock. 40MHz.
PrinA[11:0]	in	40MHz input.
PrinB[11:0]	in	40MHz input.
CompA[11:0]	in	40MHz input.
CompB[11:0]	in	40MHz input.
FreeWA[11:0]	in	40MHz input.
FreeWB[11:0]	in	40MHz input.
PrinAout[11:0]	out	10MHz output.
PrinBout[11:0]	out	10MHz output.
CompAout[11:0]	out	10MHz output.
CompBout[11:0]	out	10MHz output.
FreeWAout[11:0]	out	10MHz output.
FreeWBout[11:0]	out	10MHz output.

4.3.6 ADC_Control

This is a sub-entity of the KPS-entity, illustrated in Figure 23. The ADC_Control is controlling all the control-signals to the ADCs and Opamps. This means powering up the ADCs and Opamps on reset and powering them down when the KPS-status is set to “Finished”.

Table 6. Description of in- and outputs of the Topspeed_filter-entity.

ClkOrg	in	Original Clock. 40MHz.
Active[2:0]	in	Input from the IPOC_rslt, only the KPS-status. (3bits)
P_Clk_P	out	Positive output clock to the principal ADC.
P_Clk_N	out	Negative output clock to the principal ADC.
C_Clk_P	out	Positive output clock to the compensation ADC.
C_Clk_N	out	Negative output clock to the compensation ADC.
F_Clk_P	out	Positive output clock to the free-wheel ADC.
F_Clk_N	out	Negative output clock to the free-wheel ADC.
P_PDn	out	Power-down signal for principal ADC. Active-low.
C_PDn	out	Power-down signal for compensation ADC. Active-low.
F_PDn	out	Power-down signal for free-wheel ADC. Active-low.
Opamp_E	out	Power-down signal for the Opamps. Active-high.

4.3.7 Analysis

This is a sub-entity of the KPS-entity, illustrated in Figure 23. This entity handles all acquisition and analysis of the signals from the KPS. The entity is illustrated in Figure 24 and the different in- and outputs are described in Table 7.

The Prin_Acqui-, Comp_Acqui- and FreeW_Acqui-entities acquires the two principal circuit signals, the two compensation circuit signals and the two free-wheel circuit-signals respectively. These entities are better describes in sections 4.3.7.1, 4.3.7.2 and 4.3.7.3.

The IPOC-entity is making the analysis when the three acquisition entities are finished. The analyses are made with respect to the three inputted evaluation vectors (-EvInfo). The entity is better described in section 4.3.7.5.

The evaluation and acquisition information are updated each time the AnyBus-S module receives a beam energy or margin update. This information is then sent from the BeamEnergy_Converter, described in section 4.4.

The CounterModule-entity is the heartbeat of the system and coordinates all the different acquisitions and analysis. It is set of by the beam dump trigger. The entity is better described in section 4.3.7.4.

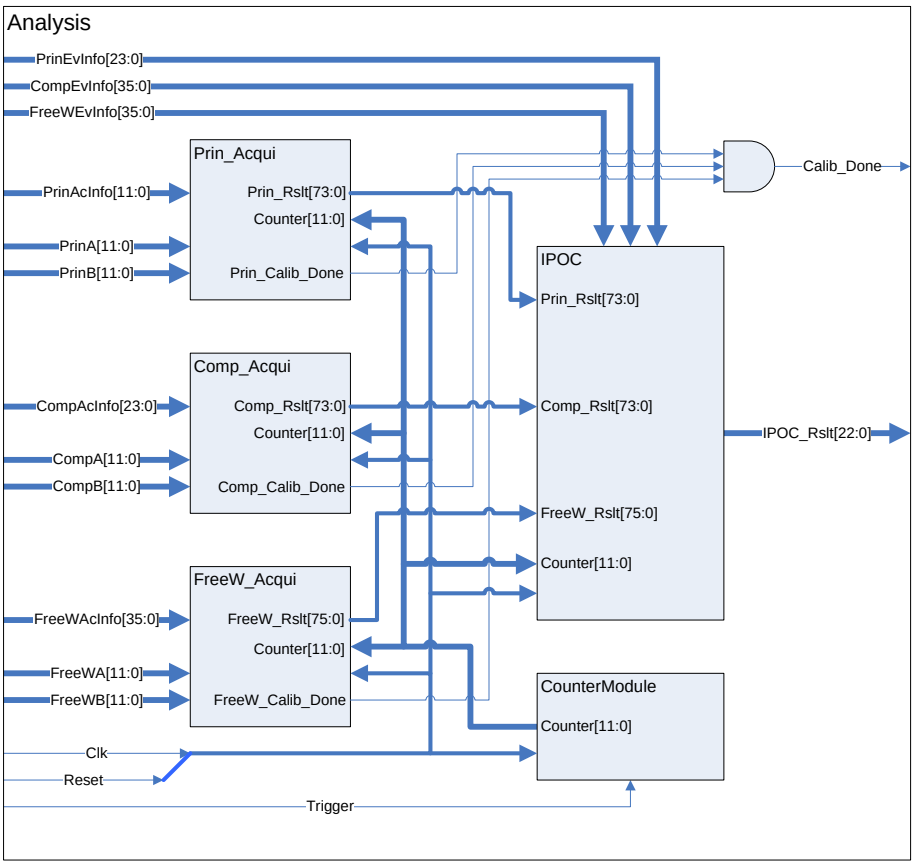

Figure 24. Block diagram of the Analysis-entity.

Table 7. Description of in- and outputs of the Analysis-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Trigger	in	Trigger signal from TriggerDetect-entity.
Counter[11:0]	in	Input-signal from the CounterModule-entity, which outputs the number of clock-cycles since the Trigger-signal was set.
PrinAcInfo[11:0]	in	Inputs from the BeamEnergy_Converter-entity containing the thresholds for sampling in the acquisitions for the Prin_Acqui-, the Comp_Acqui- and the FreeW_Acqui-entities.
CompAcInfo[23:0]	in	
FreeWAcInfo[35:0]	in	
PrinEvInfo[23:0]	in	Inputs from the BeamEnergy_Converter-entity containing the margin of allowed error between the two branches for the Prin_Acqui-, Comp_Acqui- and the FreeW_Acqui-entities.
CompEvInfo[35:0]	in	
FreeWEvInfo[35:0]	in	
PrinA[11:0]	in	Inputs for the ADC sampling the principal circuit current pickup in branch A and B.
PrinB[11:0]	in	
CompA[11:0]	in	Inputs for the ADC sampling the compensation circuit current pickup in branch A and B.
CompB[11:0]	in	
FreeWA[11:0]	in	Input for the ADC sampling the free-wheel circuit current pickup in branch A and B.
FreeWB[11:0]	in	
CalibDone	out	Connected to the left-most LED. Signal is high and LED is on when calibration complete.
IPOC_Rslt[22:0]	out	Output for the result of the analysis of the MKDG. See .

4.3.7.1 Prin_Acqui

This entity is a sub-entity of the Analysis-entity, illustrated in Figure 24. This entity contains two equal entities, named Prin_Acqui_X, illustrated in Figure 26. The Prin_Acqui-entity is illustrated in Figure 25 and the different in- and outputs are described in Table 8.

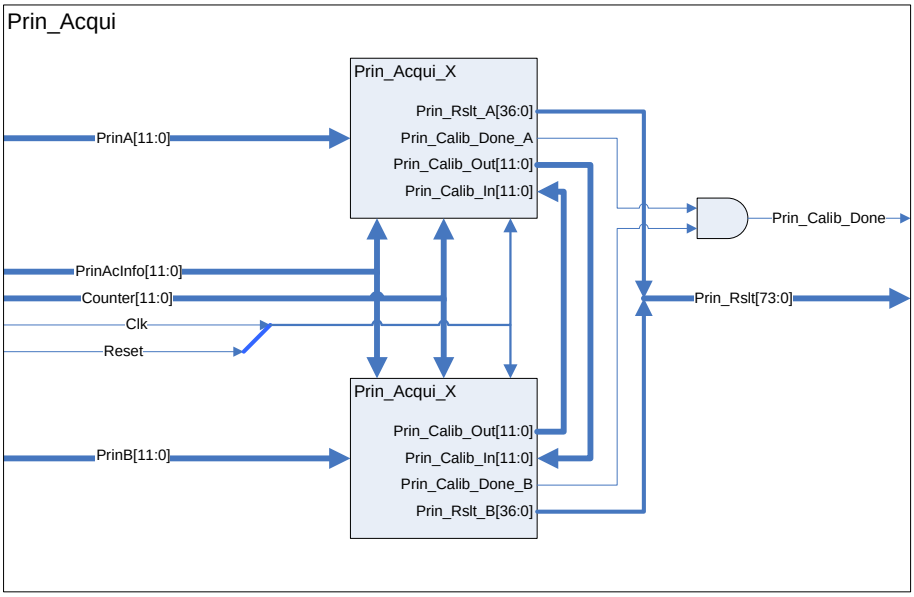

Figure 25. Block diagram of the Prin_Acqui-entity.

Table 8. Description of in- and outputs of the Prin_Acqui-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Counter[11:0]	in	Input-signal from the CounterModule-entity, which outputs the number of clock-cycles since the Trigger-signal was asserted.
PrinA[11:0]	in	Input for the ADC sampling the principal circuit current pickup in branch A and B.
PrinB[11:0]	in	
Prin_Rslt[73:0]	out	**Results. Goes to the IPOC-entity.**
Prin_Rslt_A[36:0]		Built up by two signals. Outputs for the results of the acquisition of the signals from branch A and B.
Prin_Rslt_B[36:0]		

4.3.7.1.1 Prin_Acqui_X

This is a sub-entity of the Prin_Acqui-entity, illustrated in Figure 25. This entity is used two times in the design, one for each branch, and contains all the processes for acquiring one of the signals from the two principal circuit pickups.

There are three sub-entities concerning the acquisition in this entity; one is running continuously and the last two are time dependent and are only active in a given time period after a beam dump has been issued. The time is controlled by the Control-process.

Table 9. Time dependency of the processes in the Prin_Acqui_X-entity.

Time after Trigger	Description
	The PulseDetector-entity is always running, except when KPS is calibrating.
0 - 10µs	The MaxValue-entity finds the largest inputted.
0 - 10µs	The MinValue-entity finds the lowest value inputted.

By adding new processes in this entity one can extend the analysis of the principal circuit. The entity is illustrated in Figure 26 and the different in- and outputs are described in Table 10.

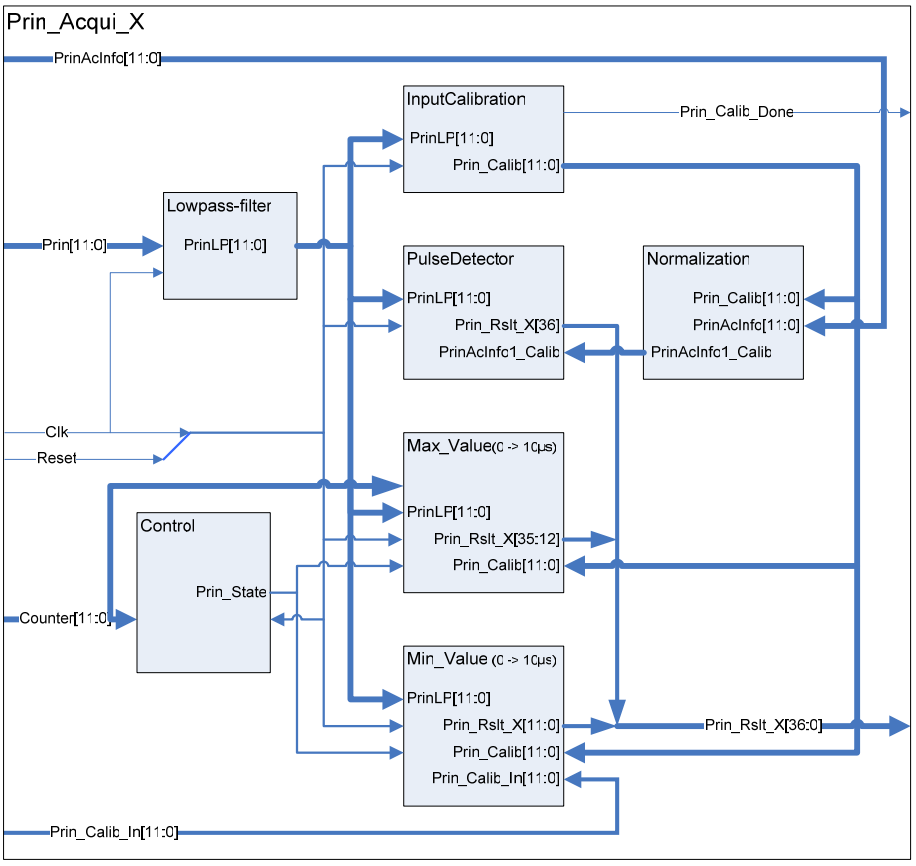

Figure 26. Block diagram of the Prin_Acqui_X-entity.

Table 10. Description of in- and outputs for the Prin_Acqui_X-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset is active low.
Prin[11:0]	in	Input for the ADC sampling the principal circuit.
Counter[11:0]	in	Signal from the CounterModule, which outputs the number of clock-cycles since the Trigger-signal was asserted.
PrinAcInfo[11:0]	in	Threshold for the PulseDetector-entity.
Prin_Calib_In	in	Input for the calibration level from the opposite branch.
Prin_Calib_Done	out	Goes high when calibration is done.
Prin_Rslt_X[36:0]	out	**Results. Goes to the IPOC-entity.**
Prin_Rslt_X[36]		Result from the PulseDetector-entity.
Prin_Rslt_X[35:12]		Result from the MaxValue-entity.
Prin_Rslt_X[11:0]		Result from the MinValue-entity.

4.3.7.1.1.1 Lowpass-filter

The Lowpass-filters order is set with a constant in the UserSettings-configuration file. The choices are to disable it or having a 2^{nd}, 4^{th} or 8^{th} order low-pass filter.

Table 11. Description of in- and outputs of the Lowpass-Filter-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Input	in	Input values in which the filter is calculating from.
Output	out	The filtered values.

4.3.7.1.1.2 InputCalibration

InputCalibration is for finding the average of the input signal and setting this as the zero-level for any calculations. The calibration is active 20 clock cycles after reset. It is therefore crucial that there is no other activity on the input other than maybe noise from the pickup. The purpose of this functionality is to remove any offset caused by deviations in the analog circuitry.

Table 12. Description of in- and outputs of the InputCalibration-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Input[11:0]	in	Input values from the ADC, in which the average is calculated from.
Output[11:0]	out	The average value. The output is held at a constant value after 20 clock-cycles.
Calib_Done	out	Goes high when the calibration is done.

4.3.7.1.1.3 Normalization

Normalization is for adapting the calculated thresholds for the acquisition. This means that the zero-level set by the calibration is added as an offset to the threshold to make them exactly alike for both branches.

Table 13. Description of in- and outputs of the Normalization-entity.

Clk	in	System clock. Running at 10MHz.
Input[11:0]	in	Input of the trigger level.
Calib_In[11:0]	in	Input from the InputCalibration-entity.
NormalizedOutput[11:0]	out	The normalized trigger level.

4.3.7.1.1.4 PulseDetector

PulseDetector is to detect if there is any current in the pickup. This entity's output goes high whenever the value on the input excides the value of an inputted threshold. The threshold changes with respect to the beam energy level.

Table 14. Description of in- and outputs of the PulseDetector-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Input[11:0]	in	Input values from the ADC.
Threshold[11:0]	in	The threshold in which the input has to be above to trigger a pulse detected report.
PulseDetector	out	The signal goes high when reporting a pulse detected.

4.3.7.1.1.5 MaxValue

MaxValue basically just compare one input value to another, remembering both the highest input value and at what time it was taken.

Table 15. Description of in- and outputs of the MaxValue-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Counter[11:0]	in	Input-signal from the CounterModule-entity, which outputs the number of clock-cycles since the Trigger-signal was asserted.
State	in	The entity is active when signal value is "FindMax".
State	in	The entity is active when signal value is "FindMax".
Input[11:0]	in	Input values from the ADC.
LevelOutput[11:0]	out	Outputs the highest input value.
TimeOutput[11:0]	out	Outputs the time of the highest input value.

4.3.7.1.1.6 MinValue

MinValue is like MaxValue, just compare one input value to another, but this remembers the lowest value inputted. The time of when the lowest value was found is of no importance so it is not remembered.

Table 16. Description of in- and outputs of the MinValue-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
State	in	The entity is active when signal value is “FindMin”.
Input[11:0]	in	Input values from the ADC.
LevelOutput[11:0]	out	Outputs the lowest input value.

4.3.7.2 Comp_Acqui

This is a sub-entity of the Analysis-entity, illustrated in Figure 24. This entity contains two equal entities, named Comp_Acqui_X, illustrated in Figure 28. The Comp_Acqui-entity is illustrated in Figure 27 and the different in- and outputs are described in Table 17.

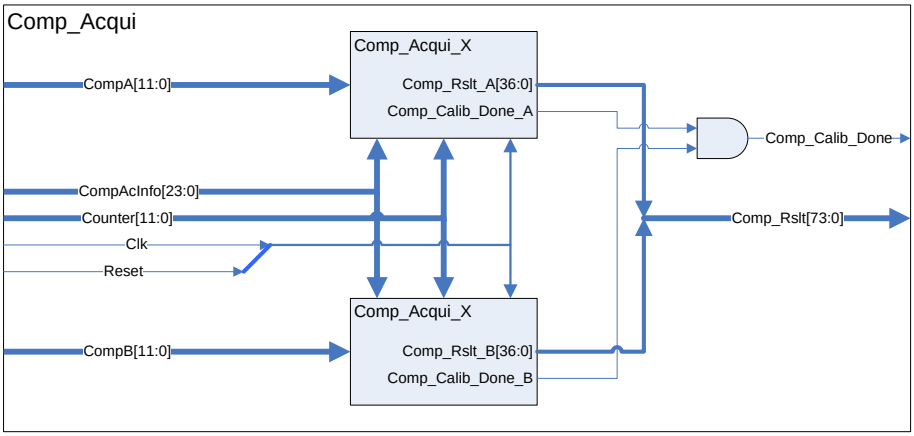

Figure 27. Block diagram of the Comp_Acqui-entity.

Table 17. Description of in- and outputs of the Comp_Acqui-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Counter[11:0]	in	Input-signal from the CounterModule-entity, which outputs the number of clock-cycles since the Trigger-signal was asserted.
CompA[11:0]	in	Input for the ADC sampling the compensation circuit current pickup in branch A and B.
CompB[11:0]	in	
Comp_Rslt[73:0]	out	**Results. Goes to the IPOC-entity.**
Comp_Rslt_A[36:0]		Built up by two signals. Outputs for the results of the acquisition of the signals from branch A and B.
Comp_Rslt_B[36:0]		

4.3.7.2.1 Comp_Acqui_X

This is a sub-entity of the Comp_Acqui-entity, illustrated in Figure 27. This entity is instantiated two times in the design and contains all the modules for acquiring one of the signals from the two compensation circuit pickups.

There are four sub-entities concerning the acquisition in this entity; one is running continuously and the last three are time dependent and are only active in a given time period after a beam dump has been issued. The time is controlled by the Control-process.

Table 18. Time dependency of the processes in the Comp_Acqui_X-entity.

Time after Trigger	Description
	The PulseDetector-entity is always running, except when KPS is calibrating.
0 - 30µs	The StartOfPulse-entity is set to sample the Counter-signal once each run when ever the input signal goes above a preset value.
30 - 80µs	The MaxValue-entity is set to find the highest input value in this window.
80 - 200µs	The StopOfPulse-entity is set to sample the Counter-signal once each run when ever the input signal goes below a preset value.

By adding new processes in this entity one can extend the analysis of the compensation circuit. The entity is illustrated in Figure 28 and the different in- and outputs are described in Table 19.

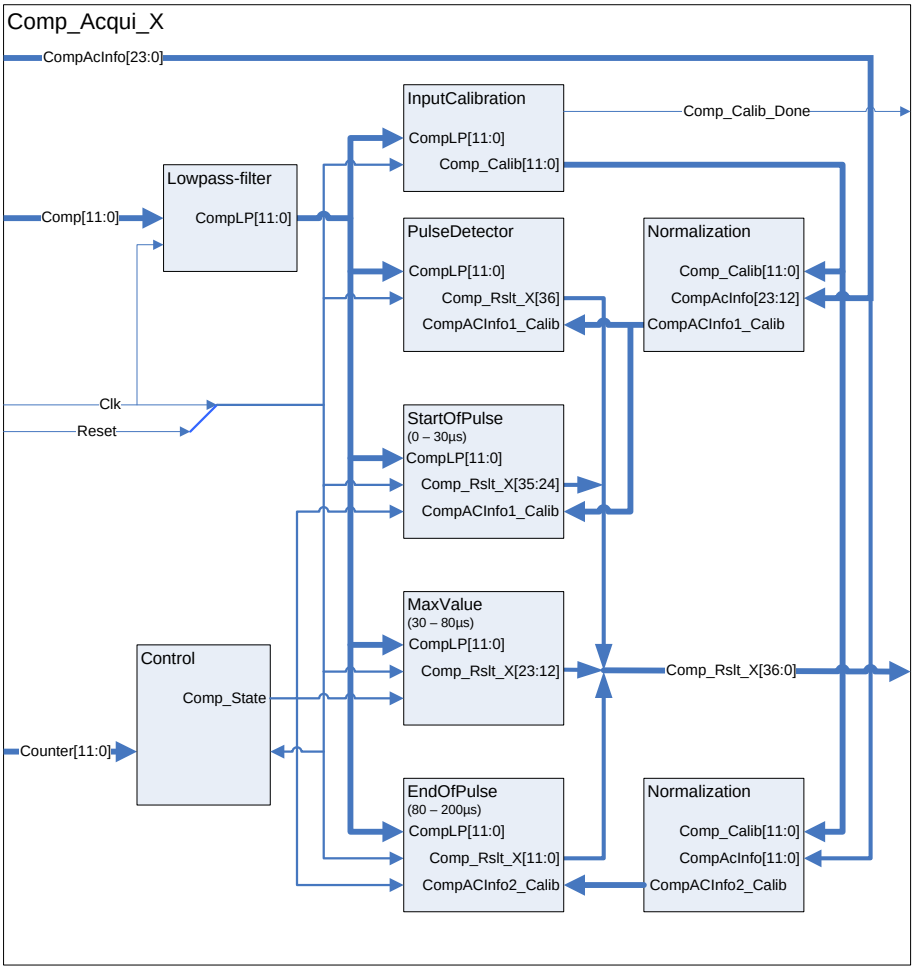

Figure 28. Block diagram of the Comp_Acqui_X-entity.

Table 19. Description of in- and outputs for the Comp_Acqui_X-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset is active low.
Counter[11:0]	in	Signal from the CounterModule, which outputs the number of clock-cycles since the Trigger-signal is asserted.
Comp[11:0]	in	Input for the ADC sampling the compensation circuit.
Comp_Calib_Done	out	Goes high when calibration is done.
CompAcInfo[23:0]	in	**Thresholds.**
CompAcInfo[23:12]		Threshold for the PulseDetector- and StartOfPulse-entity.
CompAcInfo[11:0]		Threshold for the EndOfPulse-entity.
Comp_Rslt_X[36:0]	out	**Results. Goes to the IPOC-entity.**
Comp_Rslt_X[36]		Result from the PulseDetector-entity.
Comp_Rslt_X[35:24]		Result from the StartOfPulse-entity.
Comp_Rslt_X[23:12]		Result from the MaxValue-entity.
Comp_Rslt_X[11:0]		Result from the EndOfPulse-entity.

4.3.7.2.1.1 Lowpass-filter

This is the same as in the principal circuit. See section 4.3.7.1.1.1.

4.3.7.2.1.2 InputCalibration

This is the same as in the principal circuit. See section 4.3.7.1.1.2.

4.3.7.2.1.3 Normalization

This is the same as in the principal circuit. See section 4.3.7.1.1.3

4.3.7.2.1.4 PulseDetector

This is the same as in the principal circuit. See section 4.3.7.1.1.4.

4.3.7.2.1.5 StartOfPulse

The StartOfPulse remembers the first time an input value goes above the inputted threshold.

Table 20. Description of in- and outputs of the StartOfPulse-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
State	in	The entity is active when signal value is “FindSOP”.
Threshold	in	The threshold in which the input has to be above to trigger one sampling of the counter.
Input[11:0]	in	Input values from the ADC.
LevelOutput[11:0]	out	Outputs the lowest input value.

4.3.7.2.1.6 MaxValue

This is the same as in the principal circuit. See section 4.3.7.1.1.5.

4.3.7.2.1.7 EndOfPulse

The EndOfPulse remembers the first time an input value goes below the inputted threshold.

Table 21. Description of in- and outputs of the EndOfPulse-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
State	in	The entity is active when signal value is “FindEOP”.
Threshold	in	The threshold in which the input has to be below to trigger one sampling of the counter.
Input[11:0]	in	Input values from the ADC.
LevelOutput[11:0]	out	Outputs the lowest input value.

4.3.7.3 FreeW_Acqui

This is a sub-entity of the Analysis-entity, illustrated in Figure 24. This entity contains two equal entities, named FreeW_Acqui_X, illustrated in Figure 30. The FreeW_Acqui-entity is illustrated in Figure 29 and the different in- and outputs are described in Table 22.

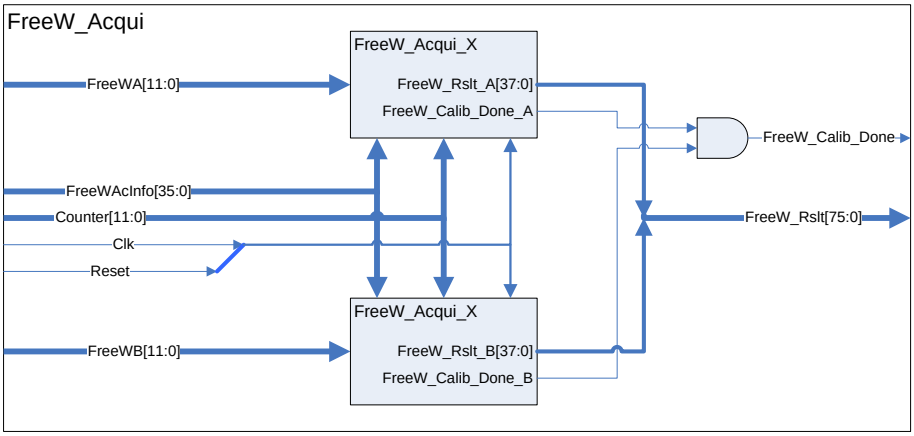

Figure 29. Block diagram of the FreeW_Acqui-entity.

Table 22. Description of in- and outputs of the FreeW_Acqui-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Counter[11:0]	in	Input-signal from the CounterModule-entity, which outputs the number of clock-cycles since the Trigger-signal was asserted.
FreeWA[11:0]	in	Input for the ADC sampling the free-wheel circuit current pickup in branch A and B.
FreeWB[11:0]	in	
FreeW_Rslt[75:0]	out	**Goes to the IPOC-entity.**
FreeW_Rslt_A[37:0]		Built up by two signals. Output for the result of the acquisition of the signal from branch A and B.
FreeW_Rslt_B[37:0]		

4.3.7.3.1 FreeW_Acqui_X

This entity is a sub-entity of the FreeW_Acqui-entity, illustrated in Figure 29. This entity is used two times in the design and contains all the modules for acquiring one of the signals from the two free-wheel circuit pickups.

There are five sub-entities concerning the acquisition in this entity; one is running continuously and the last four are time dependent and are only active in a given time period after a beam dump has been issued. The time is controlled by the Control-process.

Table 23. Time dependency of the processes in the FreeW_Acqui_X-entity.

Time after Trigger	Description
	The PulseDetector-entity is always running, except when KPS is calibrating.
0 - 15µs	The StartOfPulse-entity is set to sample the Counter-signal once each run whenever the input signal goes above a preset value.
15 - 80µs	The No_Pulse-process is set to Trigger if one of the input-values are over a certain level.
80 - 250µs	The StartOfPulse -entity is set to sample the Counter-signal once each run when ever the input signal goes above a preset value.
80 - 250µs	The MaxValue-entity is set to sample the Counter-signal once each run when ever the input signal goes below a preset value.

By adding new processes in this entity one can extend the analysis of the free-wheel circuit. The entity is illustrated in Figure 30 and the different in- and outputs are described in Table 24.

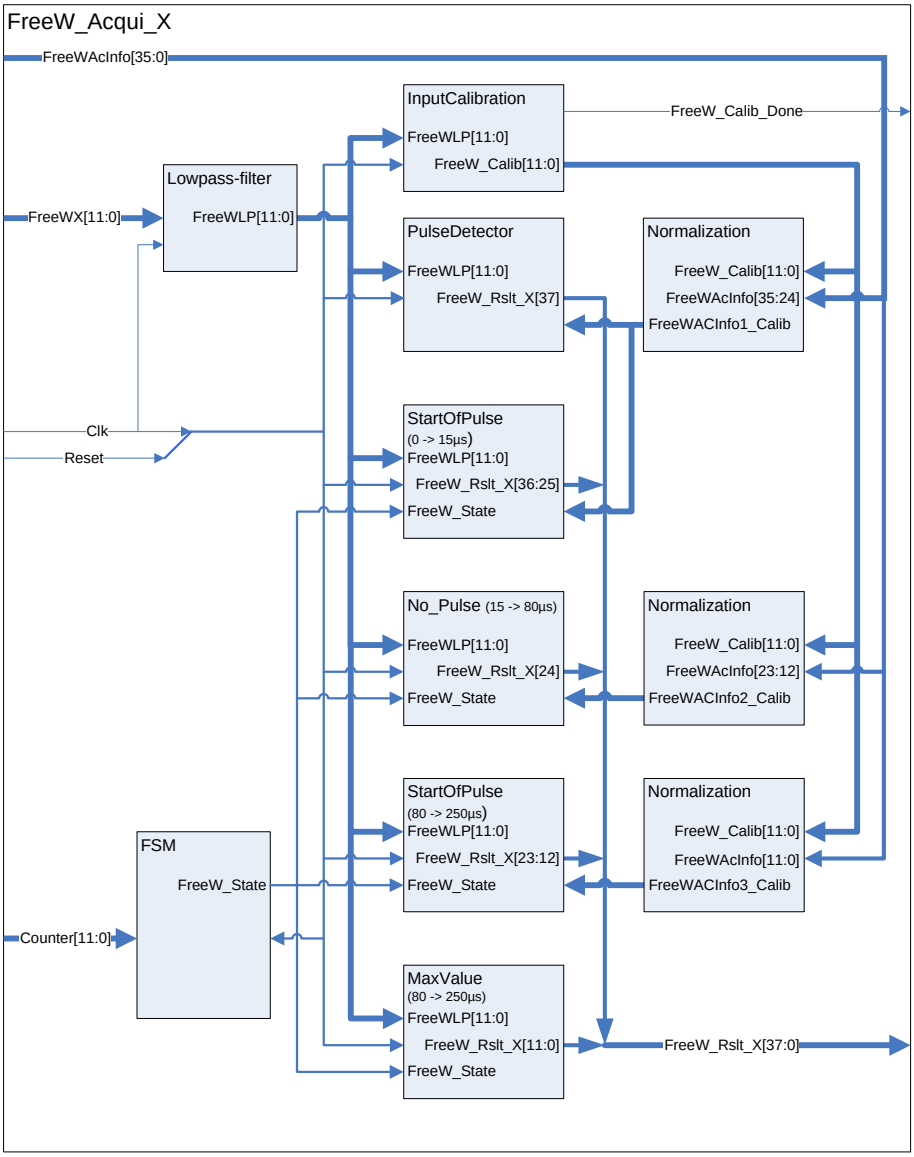

Figure 30. Block diagram of the FreeW_Acqui_X-entity.

Table 24. Description of in- and outputs for the FreeW_Acqui_X-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset is active low.
FreeW[11:0]	in	Input for the ADC sampling the compensation circuit.
Counter[11:0]	in	Signal from the CounterModule, which outputs the number of clock-cycles since the Trigger-signal is asserted.
FreeW_Calib_Done	out	Goes high when calibration is done.
FreeWAcInfo[35:0]	in	**Thresholds.**
FreeWAcInfo[35:24]		Threshold for the PulseDetector- and First_Pulse-entity.
FreeWAcInfo[23:12]		Threshold for the No_Pulse-entity.
FreeWAcInfo[11:0]		Threshold for the Second_Pulse-entity.
FreeW_Rslt_X[37:0]	out	**Results. Goes to the IPOC-entity.**
FreeW_Rslt_X[37]		Result from the PulseDetector-entity.
FreeW_Rslt_X[36:25]		Result from the First_Pulse-entity.
FreeW_Rslt_X[24]		Result from the No_Pulse-entity.
FreeW_Rslt_X[23:12]		Result from the Second_Pulse-entity.
FreeW_Rslt_X[11:0]		Result from the MaxValue-entity.

4.3.7.3.1.1 Lowpass-filter

This is the same as in the principal circuit. See section 4.3.7.1.1.1.

4.3.7.3.1.2 InputCalibration

This is the same as in the principal circuit. See section 4.3.7.1.1.2.

4.3.7.3.1.3 Normalization

This is the same as in the principal circuit. See section 4.3.7.1.1.3

4.3.7.3.1.4 PulseDetector

This is the same as in the principal circuit. See section 4.3.7.1.1.4.

4.3.7.3.1.5 First_Pulse

First_Pulse is the same entity as Start_Of_Pulse from the compensation circuit. See section 4.3.7.2.1.5.

4.3.7.3.1.6 No_Pulse

No_Pulse is the same entity as PulseDetector, only the output is inverted. See section 4.3.7.1.1.4.

4.3.7.3.1.7 Second_Pulse

Second_Pulse is the same entity as Start_Of_Pulse from the compensation circuit. See section 4.3.7.2.1.5.

4.3.7.3.1.8 MaxValue

This is the same as in the principal circuit. See section 4.3.7.1.1.5.

4.3.7.4 CounterModule

This entity is a sub-entity of the Analysis-entity, illustrated in Figure 24. This entity is basically two counters. There is a small counter which is set of by the TriggerDetect-entity, this because of the latency in the digital system. The main counter counts from 0 to 2020 and starts counting after the smaller counter has finished counting to a certain preset time, given in the UserSettings-package.

Table 25. Description of in- and outputs of the CounterModule-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Trigger	in	Trigger signal from TriggerDetect-entity.
Counter[11:0]	out	Main-counter output signal from the CounterModule-entity. Outputs the number of clock-cycles since the Trigger-signal was asserted.

4.3.7.5 IPOC

This entity is a sub-entity of the Analysis-entity, illustrated in Figure 24. This entity handles all the analysis of the acquired data from the MKDG. It starts analyzing as soon as the acquisition of the signals from the MKDG is finished. The analysis is based upon information received from the Beam Energy Converter, presented in section 4.4.

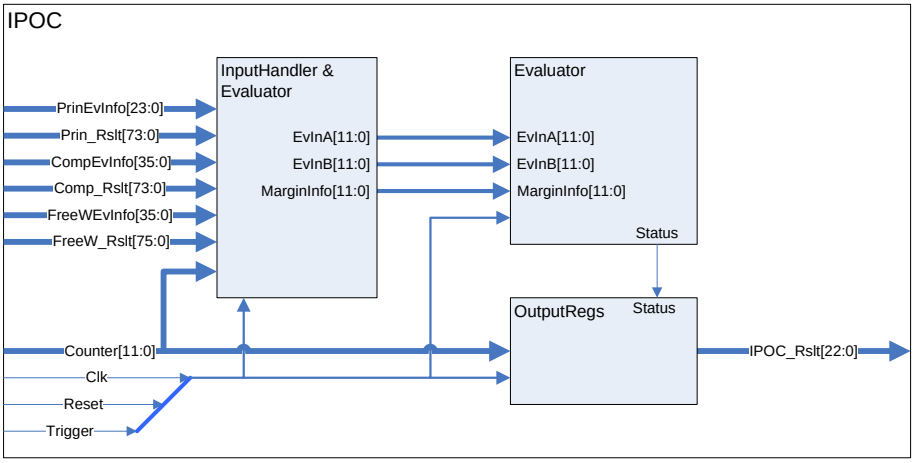

Figure 31. Block diagram of the IPOC-entity.

Table 26. Description of in- and outputs of the IPOC-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Trigger	in	Trigger signal from TriggerDetect-entity.
Counter[11:0]	in	Signal from the CounterModule-entity, which outputs the number of clock-cycles since the Trigger-signal was asserted.
PrinEvInfo[23:0]	in	Inputs from the BeamEnergy_Converter-entity containing the margin of allowed error between the two branches for the Prin_Acqui-, Comp_Acqui- and the FreeW_Acqui-entity.
CompEvInfo[35:0]	in	
FreeWEvInfo[35:0]	in	
Prin_Rslt[73:0]	in	Results from the acquisition of the three pickups in each of the two branches principal-, compensation- and free-wheel-circuitry.
Comp_Rslt [73:0]	in	
FreeW_Rslt[75:0]	in	
IPOC_Rslt[22:0]	out	Output for the result of the analysis of the MKDG. See .

Table 27. Description of the IPOC output-vector IPOC_Rslt.

Bit n°		**Description**
22 - 20	**KPS-status**	
	000 = Resetting	Gives the present status of the acquisition unit.
	001 = Armed	
	010 = Acquisition	
	100 = Analysis	
	111 = Finished	
19-18	**Trigger vs. Current**	
	00 = Waiting	Categorizes the type of pulsing action going on in the MKDG
	01 = Erratic	
	10 = Pulse Missing	
	11 = Pulsing	
17-12	**Current detection**	
17	Principal A	Indicates which parts of the MKDG has pulsed. Not Pulsed = '0' Pulsed = '1'
16	Principal B	
15	Compensation A	
14	Compensation B	
13	Free-wheel A	
12	Free-wheel B	
11 - 0	**Analysis Result**	
11	Principal Maximum within margins.	Binary results of the IPOC. The analysis is either within the preset margins or not. Not OK = '0' OK = '1'
10	Principal A Max reached in time.	
9	Principal B Max reached in time.	
8	Principal Minimum within margins.	
7	Compensation Start of Pulse within time.	
6	Compensation End of Pulse within time.	
5	Compensation Maximum within margins.	
4	Free Wheel First Pulse within time.	
3	Free Wheel No Current A	
2	Free Wheel No Current B	
1	Free Wheel Second Pulse within time.	
0	Free Wheel Maximum within margins.	

4.3.7.5.1 Evaluator

This entity is a sub-entity of the IPOC-entity, illustrated in Figure 31. This is a block used in most of the IPOC. This is basically a subtractor, returning the absolute value of the answer and then checks if the answer is less then the MarginInfo-vector. If it is less the Status-signal is set to one if not; it is set to zero. The entity is illustrated in Figure 32 and the different in- and outputs are described in Figure 32.

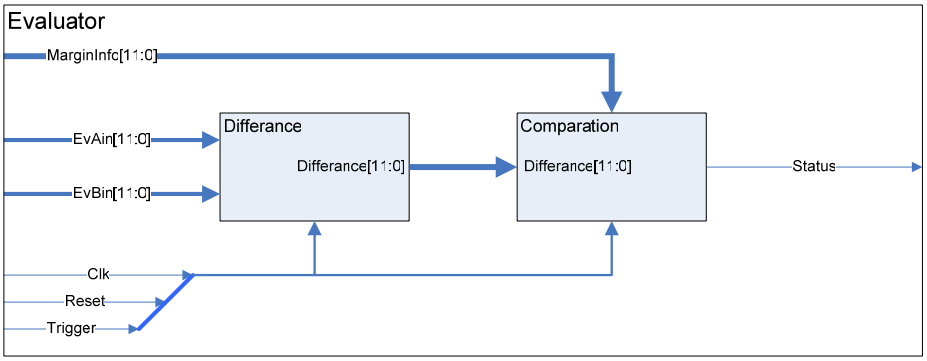

Figure 32. Block diagram of the Evaluator-entity.

Table 28. Description of in- and outputs of the Evaluator-entity.

Clk	in	System clock. Running at 10MHz.
Reset	in	System reset. Active low.
Trigger	in	Trigger signal from TriggerDetect-entity.
MarginInfo[11:0]	in	Evaluation information.
EvAIn[11:0]	in	Result from branch A.
EvAIn[11:0]	in	Result from branch B.
Status	out	Result of analysis. Within margins or not within margins. One or zero.

4.3.8 BeamEnergy_Converter

This entity is a sub-entity of the AnyBus_Interface-entity, illustrated in Figure 34. This entity makes 14 calculations. Six of them are thresholds for the acquisition and the eight others are for the evaluation of the results. The signals concerning acquisition have the letters 'Ac' in them and the signals concerning evaluation have the letters 'Ev' in them. The entity is illustrated in Figure 33 and the different in- and outputs are described in Table 29.

Not all the calculations are with respect to the beam energy level, the time margins are the same for all the beam energy levels. In addition, the calculations for the evaluation info are made with respect to the percentage margins provided by the PLC over the Profibus DP-network. These equations can be found in section 3.3.1.1.2, 3.3.2.1.2 and 3.3.3.1.2.

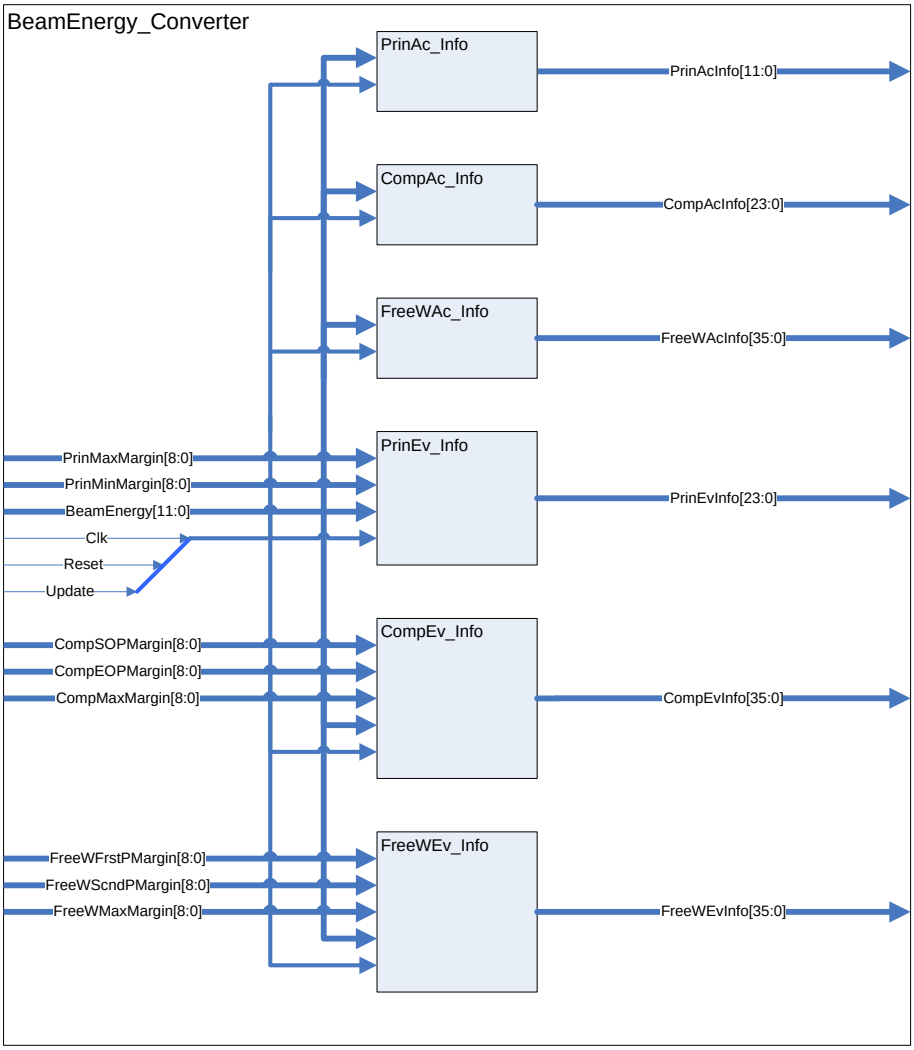

Figure 33. Block diagram of the BeamEnergy_Converter-entity.

Table 29. Description of in- and outputs of the BeamEnergy_Converter-entity.

Clk	in	System-clock. 10MHz.
Reset	in	Reset signal with reset the entity to injection level beam energy.
Update	in	Signal from the Anybus_Interface-entity, goes high one clock cycle when new data received.
BeamEnergy[11:0]	in	Present beam energy level from the PLC
PrinMaxMargin[7:0]	in	Percentage margin information from the PLC.
PrinMinMargin[7:0]	in	Percentage margin information from the PLC.
CompSOPMargin[7:0]	in	Time margin information from the PLC.
CompEOPMargin [7:0]	in	Time margin information from the PLC.
CompMaxMargin[7:0]	in	Percentage margin information from the PLC.
FreeWFrstPMargin[7:0]	in	Time margin information from the PLC.
FreeWScndPMargin[7:0]	in	Time margin information from the PLC.
FreeWMaxMargin[7:0]	in	Percentage margin information from the PLC.
PrinAcInfo[11:0]	out	**Goes to Prin_Acqui_X-entity.**
PrinAcInfo[11:0]		Threshold for the PulseDetector-entity
CompAcInfo[23:0]	out	**Goes to Comp_Acqui_X-entity.**
CompAcInfo[23:12]		Threshold for the PulseDetector-entity and the StartOfPulse-entity.
CompAcInfo[11:0]		Threshold for EndOfPulse-entity.
FreeWAcInfo[35:0]	out	**Goes to FreeW_Acqui_X-entity.**
FreeWAcInfo[35:24]		Threshold for the PulseDetector-entity and the StartOfPulse-entity.(1^{st} pulse)
FreeWAcInfo[23:12]		Threshold for the No_Pulse-process.
FreeWAcInfo[11:0]		Threshold for the StartOfPulse-entity.(2^{nd} pulse)
PrinEvInfo[23:0]	out	**Goes to IPOC-entity.**
PrinEvInfo[23:12]		Margin calculations for the principal maximum analysis.
PrinEvInfo[11:0]		Margin calculations for the principal minimum analysis.
CompEvInfo[35:0]	out	**Goes to IPOC-entity.**
CompEvInfo[35:24]		Margins for acceptable time deviation for the start of the pulse. (No calculations)
CompEvInfo[23:12]		Margins for acceptable time deviation for the stop of the pulse. (No calculations)
CompEvInfo[11:0]		Margin calculations for the compensation maximum analysis.
FreeWEvInfo[35:0]	out	**Goes to IPOC-entity.**
FreeWEvInfo[35:24]		Margins for acceptable time deviation for the first pulse. (No calculations)
FreeWEvInfo[23:12]		Margins for acceptable time deviation for the second pulse. (No calculations)
FreeWEvInfo[11:0]		Margin calculations for the free-wheel maximum analysis.

4.3.9 AnyBus_Interface

This is a sub-entity of the KPS-entity, illustrated in Figure 23. The AnyBus_Interface-entity takes care of the communication between the AnyBus-S module and the FPGA. It is set up to get the beam energy level and the error margins from a PLC and to send reports back to the PLC. The entity is illustrated in Figure 34. The different in- and outputs are described in Table 30.

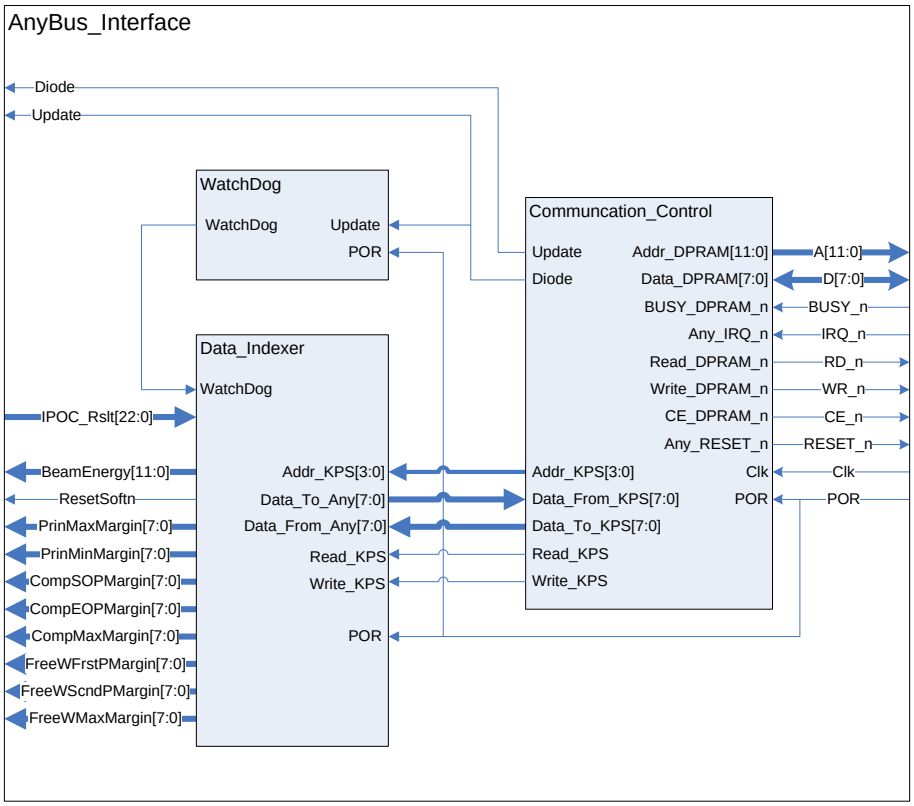

Figure 34. Block diagram of the AnyBus_Interface-entity.

The information exchanged through the Profibus DP interface consists of 11 bytes from a PLC to the KPS and four bytes from the KPS to a PLC. The bytes to the KPS contain the present beam-energy level and the eight different margins allowed for the different analyses. The bytes from the KPS contain a Watchdog bit, the result of the IPOC and the firmware version number. The Watchdog bit is to verify that the board is still operational. The content of each transferred byte are presented in Table 32.

Table 30. Description of in- and outputs of the AnyBus_Interface-entity.

Clk	in	System-clock. 10MHz.
POR	in	Reset signal from PowerOn_Reset-entity.
IPOC_Rslt[22:0]	in	Results from the analysis of the MKD.
BeamEnergy[11:0]	out	Beam energy information. 12 MSBs of the original 16 bit beam energy representation vector received from the Profibus DP Master
ResetSoftn	in	Reset signal received from the Profibus DP Master
PrinMaxMargin	out	Margin info for principal circuit maximum-amplitude analysis.
PrinMinMargin	out	Margin info for principal circuit minimum-amplitude analysis.
CompSOPMargin	out	Margin info for compensation circuit start-of-pulse-analysis.
CompEOPMargin	out	Margin info for compensation circuit stop-of-pulse-analysis.
CompMaxMargin	out	Margin info for compensation circuit maximum-amplitude-analysis.
FreeWFrstPMargin	out	Margin info for free-wheel circuit start-of-first-pulse-analysis.
FreeWScndPMargin	out	Margin info for free-wheel circuit start-of-second-pulse-analysis.
FreeWMaxMargin	out	Margin info for free-wheel circuit maximum-amplitude-of-second-pulse-analysis.
A	out	For addressing of the AnyBus-S module.
D	inout	Bidirectional data bus for data exchange with the AnyBus-S module.
BUSY_n	in	Control signals for AnyBus-S module.
IRQ_n	in	
RD_n	out	
WR_n	out	
CE_n	out	
RESET_n	out	
Diode	out	Connected to LED, indicates correct initialization of AnyBus-S module.
Update	out	This signal goes high whenever there is an update from the AnyBus-S module.

4.3.10 AnyBus_Interface_Settings-package

This package contains some important setting for the transfer- and receive-number of bytes in the AnyBus-S module. It should be said that it is not enough to only change the constants in this package, changes needs also to be made in the Data_Indexer-entity.

4.3.10.1 Data_Indexer

This entity is a sub-entity of the AnyBus_Interface-entity, illustrated in Figure 34. This entity handles the organization of the bytes that are being sent. Since the Profibus DP-network makes transfers in bytes, data has to be put together in bytes. This is the entity where the bytes are put together before sending and taken apart on receiving. The content of each transferred byte are presented in Table 32. The task of the entity is also to give access to write or read the bytes the Access_Control-entity requests. The different in- and outputs are described in Table 31.

Table 31. Description of in- and outputs of the Data_Indexer-entity.

WatchDog	in	A bit that toggles to make sure the KPS is working.
IPOC_Rslt[22:0]	in	The results of the analysis of the MKD.
BeamEnergy[11:0]	out	Beam energy information. 12 MSBs of the original 16 bit beam energy representation vector. Received from the Profibus DP master.
ResetSoftn	out	Reset signal received from the Profibus DP master
PrinMaxMargin	out	Margin info for principal circuit maximum-amplitude analysis.
PrinMinMargin	out	Margin info for principal circuit minimum-amplitude analysis.
CompSOPMargin	out	Margin info for compensation circuit start-of-pulse-analysis.
CompEOPMargin	out	Margin info for compensation circuit stop-of-pulse-analysis.
CompMaxMargin	out	Margin info for compensation circuit maximum-amplitude-analysis.
FreeWFrstPMargin	out	Margin info for free-wheel circuit start-of-first-pulse-analysis.
FreeWScndPMargin	out	Margin info for free-wheel circuit start-of-second-pulse-analysis.
FreeWMaxMargin	out	Margin info for free-wheel circuit maximum-amplitude-of-second-pulse-analysis.
POR	in	Reset signal from PowerOn_Reset-entity.
Read_KPS	in	Signal goes high if Communication_Control-entity wants to read from Data_Indexer-entity.
Write_KPS	in	Signal goes high if Communication_Control-entity wants to write to Data_Indexer-entity.
Addr_KPS[3:0]	in	Address information to index the correct bytes in the entity.
Data_From_Any[7:0]	in	Data is presented if Communication_Control-entity wants to write to Data_Indexer-entity.
Data_To_Any[7:0]	out	Data is presented if Communication_Control-entity wants to write to Data_Indexer-entity.

Table 32. Description of the in- and out-bytes for the AnyBus_Interface-entity.

Byte n^{o}		**Description**
Data from KPS		
Byte0	out	WatchDog and IPOC Result bits 22 down to 16.
Byte1	out	IPOC Result bits 15 down to 8.
Byte2	out	IPOC Result bits 7 down to 0.
Byte3	out	Firmware version number.
Data to KPS		
Byte4	in	Beam Energy bits 15 down to 8.
Byte5	in	Beam Energy bits 7 down to 0.
Byte6	in	Reset. (only MSB-byte)
Byte7	in	Principal circuits maximum value margin.
Byte8	in	Principal circuits minimum value margin.
Byte9	in	Compensation circuits start of pulse time margin.
Byte10	in	Compensation circuits end of pulse time margin.
Byte11	in	Compensation circuits maximum value margin.
Byte12	in	Free-wheel circuits first pulse time margin.
Byte13	in	Free-wheel circuits second pulse time margin.
Byte14	in	Free-wheel circuits maximum value margin.

4.3.10.2 Communication_Control

This entity is a sub-entity of the AnyBus_Interface-entity, illustrated in Figure 34. This is the control center of the communication with the AnyBus-S module. First it initializes the AnyBus-S module and then detaches the Initialization-entity, giving access to the Data_Exchange-entity. The entity is illustrated in Figure 35. The different in- and outputs are described in Table 33.

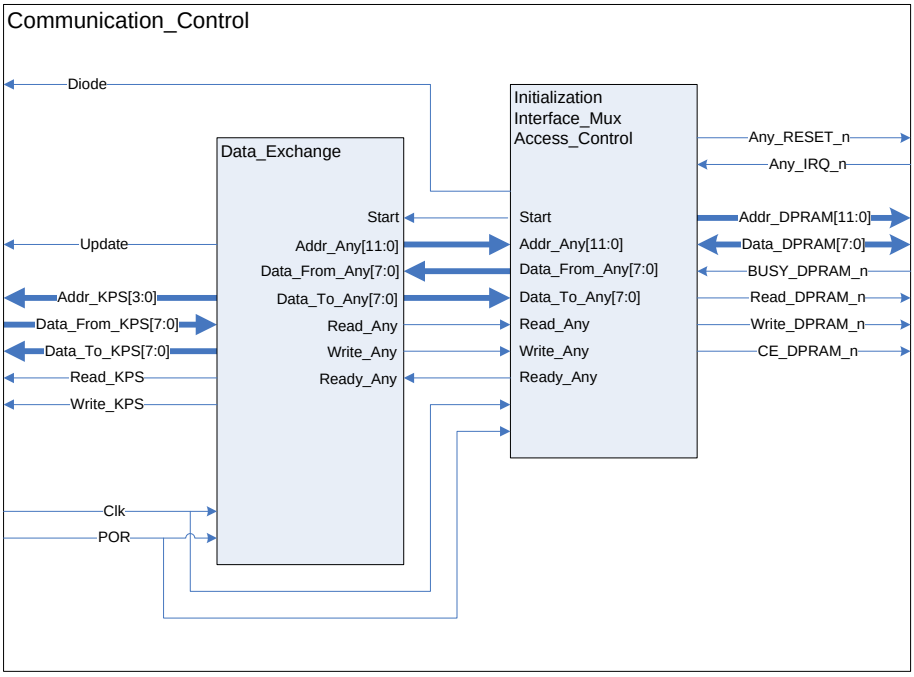

Figure 35. Block diagram of the Communication_Control-entity.

Table 33. Description of in- and outputs of the Communication_Control-entity.

Clk	in	System-clock. 10MHz.
POR	in	Reset signal from PowerOn_Reset-entity.
Update	out	This signal goes high whenever there is an update from the AnyBus-S module.
Addr_KPS[3:0]	out	Address information to index the correct bytes in the entity.
Data_From_KPS[7:0]	in	Data is presented if Communication_Control-entity wants to write to Data_Indexer-entity.
Data_To_KPS[7:0]	out	Data is presented if Communication_Control-entity wants to write to Data_Indexer-entity.
Read_KPS	out	Signal goes high if Communication_Control-entity wants to read from Data_Indexer-entity.
Write_KPS	out	Signal goes high if Communication_Control-entity wants to write to Data_Indexer-entity.
Addr_DPRAM[11:0]	out	For addressing of the AnyBus-S module.
Data_DPRAM[7:0]	inout	Bidirectional data bus for data exchange with the AnyBus-S module.
Any_RESET_n	out	Control signals for AnyBus-S module
Any_IRQ_n	in	
BUSY_DPRAM_n	in	
Read_DPRAM_n	out	
Write_DPRAM_n	out	
CE_DPRAM_n	out	
Diode	out	Connected to LED, indicates correct initialization of AnyBus-S module.
Update	out	This signal goes high whenever there is an update from the AnyBus-S module.

4.3.10.2.1 Data_Exchange

The Data_Exchange-entity is a sub-entity of the Communication_Control-entity, illustrated in Figure 35. The different in- and outputs are described in Table 34. The entity's task is to transfers bytes between the KPS and the AnyBus-S module. It requests a locked access to the AnyBus out-area. When this is granted it reads the data, then releases the area locked. This ensures that this entity will not be allowed to access the area again, before the AnyBus-S module has updated it. This exchange of data happens continuously as long as the KPS is active.

Table 34. Description of in- and outputs of the Data_Exchange-entity.

Clk	in	System-clock. 10MHz.
POR	in	Reset signal from PowerOn_Reset-entity.
Start	in	Indicates that the initial procedure has ended.
Update	out	This signal goes high whenever there is an update from the AnyBus-S module.
Addr_KPS[3:0]	out	Address information to index the correct bytes in the Data_Indexer-entity.
Data_From_KPS[7:0]	in	Where data is presented from Data_Indexer-entity, if Read_KPS is high.
Data_To_KPS[7:0]	out	Where data is presented to Data_Indexer-entity, if Write_KPS is high.
Read_KPS	out	Signal goes high if read from Data_Indexer-entity.
Write_KPS	out	Signal goes high if write to Data_Indexer-entity.
Addr_Any[11:0]	out	For addressing of the AnyBus-S module.
Data_From_Any[7:0]	in	Where data is presented from AnyBus-S module, if Read_Any is high.
Data_To_Any[7:0]	out	Where data is presented to AnyBus-S module, if Write_Any is high.
Read_Any	out	Signal goes high if read from Anybus-S module.
Write_Any	out	Signal goes high if write to Anybus-S module.
Ready_Any	in	Goes high when the AnyBus-S module is able to receive commands.

4.3.10.2.2 Initialization, Interface_Mux and Access_Control

These entities are sub-entity of the Communication_Control-entity and illustrated as one entity in Figure 35. The entity's tasks are to initialize and control the access to the AnyBus-S module. Everything, except Message_Rom, a sub-entity of the Initialization, is left as it was made by Anders Vad Nilsen, a former employee at CERN. [7]

4.3.10.2.2.1 Message_Rom

This entity is a sub-entity of the Initialization-entity. The Message_Rom-entity is made to be synthesized as a 128 x 8bit ROM. It contains all the data that is to be sent to and received from the Profibus DP master for correct initialization of the communication channel.

4.4 KPS behaviour

This section describes the behaviour and lifecycle of the KPS.

4.4.1 Power up

When the KPS is powered up, the first thing it does is initializing the AnyBus-S module, and establishing the Profibus DP communication channel.

4.4.2 Reset

The KPS has three types of resets, the first; for powering up, second; a push-button on the front-panel and third; the possibility to reset the board through the Profibus DP.

The power up reset is mainly to make sure that the AnyBus-S module is initialized and configured on power up.

The pushbutton reset is resetting all the modules within the FPGA, except for the AnyBus_Interface. The AnyBus_Interface is only reset on power up or when the FPGA is reconfigured.

The reset through the Profibus DP has the same function as the pushbutton.

Resetting sets the KPS-status to “Armed”.

4.4.3 Armed

This is the waiting state of the board. It is in this state the KPS will spend most of its time. The board is now waiting for a triggering of a beam dump or some erratic currents in the MKDG. The board is continuously getting updates on the present beam energy level in the LHC.

If any currents are detected in the MKDG, with or without a triggering signal, this is reported through the Profibus DP. The report contains information on the type of error and in which part of the generator it occurred.

Whenever there are currents detected in the MKDG or a beam dump triggering is issued the KPS-status changes to “Acquiring”.

4.4.4 Acquiring

When the KPS-status is set to Acquiring, one of two things must have happened; there has been an erratic triggering of the MKDG or a beam dump has been issued.

If there has been an erratic triggering, the KPS will report this and the KPS-status will have the present status until a beam dump is issued.

When a beam dump is issued the acquisition of data for the analysis of the MKDG starts. After 200µs the KPS-status is set to "Analysis".

4.4.4.1 Parting the different modes

The "Trigger vs. Current" bits in the IPOC-result-report gives a more precise characteristic of what is occurring in the MKDG.

Table 35. Different modes in MKDG.

Waiting	The board is waiting for a trigger of or a pulse in the MKDG.
Erratic	There is current in the MKDG, but no beam dump has been issued.
Pulse missing	A beam dump has been issued, but at least one pulse is missing.
Pulsing	A beam dump has been issued and all the pulses are there. Everything is as it should be

4.4.5 Analysis

After the KPS has acquired all the data from the pulsing of the MKDG, the KPS-status is set to Analysis, this happens 200µs after the triggering of a beam dump. When the analysis is finished, the results are communicated to the Profibus DP Master. The boards lifecycle is now finished and the KPS-status is set to "Finished".

4.4.6 Finished

The KPS has now finished its tasks. The lifecycle is ended and acquiring electronics are powered down. The results of the analysis are available through the Profibus DP. The KPS can only be taken out of this state by a reset, meaning pushing the pushbutton or resetting through the Profibus DP.

5 Hardware

5.1 Introduction

This chapter describes the considerations and conclusions made in the development of a prototype for the acquisition of the signals from the six pickup outputs on the MKDG. The different modules needed from the acquisition to the reporting of the analysis are illustrated in Figure 36.

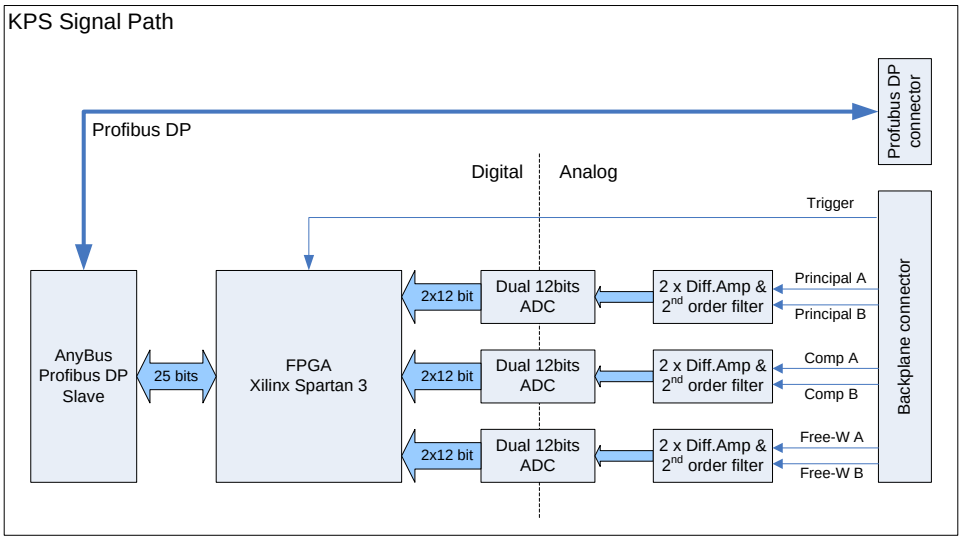

Figure 36. Block diagram of the system.

5.2 Tools

PSpice was used to simulate and confirm the analog front-end of the ADCs. This is a very convenient program since reliable mathematical models can be made for all the components. This means that the simulations are close to real life. The differential 2nd order active filter and amplification is calculated using Active Filter Pro, a freeware program developed and provided by Texas Instruments. The schematics and layout of the board were done in PCAD 2004.

5.3 Analog Acquisition Circuitry

The analog circuitry presented in this section is used to shape the signals from the three pairs of current-pickups on the MKDG, before they enter the ADCs. There are three pickups in each of the two branches in the MKDG. The pickup transforms the current into a voltage which can be read on a 50Ω transmission line output. These six outputs are connected directly to the inputs of the circuits presented in Figure 38 through Figure 43.

Figure 37 is the same as Figure 38 only the different parts of the circuit has been boxed in with different coloured frames. The content of these frames are described below, but a more thorough description can be found in sections 5.3.1 to 5.3.5.

The circuit has seven single-ended signal inputs; six of these inputs are connected directly to the six outputs of the MKDG. The seventh is the beam dump triggering signal, purposed to trigger the acquisitions and analysis.

After entering the board all the seven signals are annotated to get them down to an electronics small-signal level. This is in all the seven cases a voltage divider, an example of such a divider can be seen inside the blue frame in Figure 37.

Next the six signals from the pickups are filtered through an active second order Butterworth differential filter in which there is also a conversion of the single-ended signal into a differential output-signal, the filter can be seen inside the green frame in Figure 37.

The common mode voltage for the output of the Opamp is set to 2V, this because the input of the ADC has to be between 1V and 3V. The common mode input can be seen inside the yellow frame in Figure 37.

As the input signals have different voltage ranges there has to be different offsets for the signal. The principal circuit need to represent negative voltages and the two others only positive. This biasing can be seen inside the red frame in Figure 37.

The differential signal output from the Opamp is again put through a filter, this time a simple RC-filter designed to work as a buffer between the ADC and Opamp. The filter can be seen inside the violet frame in Figure 37.

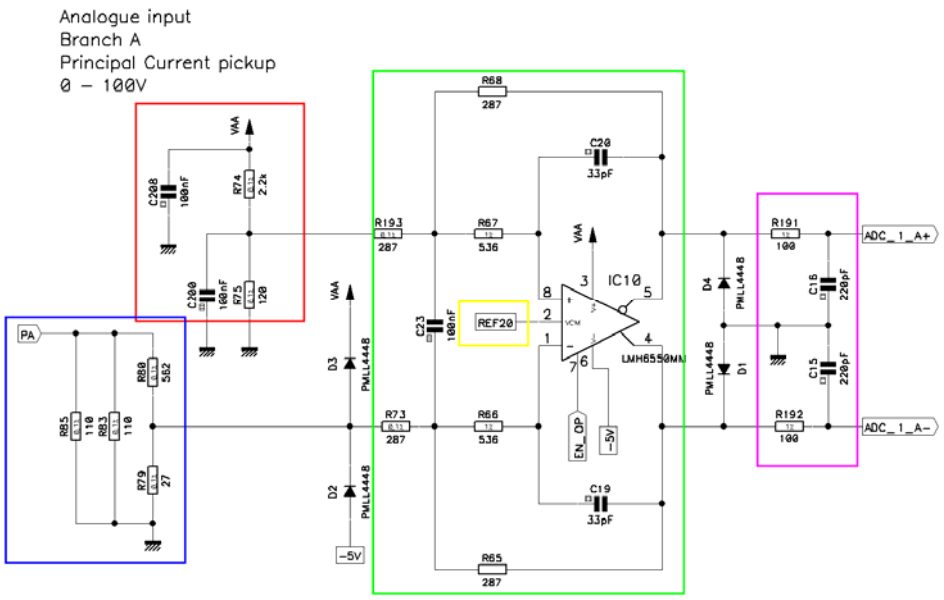

Figure 37. Principal circuit with its different part boxed in.

5.3.1 Annotation

The annotations of the signals after entering the board are different for the three circuits due to different sensitivity in the pickups and the different current levels in the MKDG. The different annotations can be seen in Table 36.

To annotate the input signals voltage dividers are used, this part of the circuit can be seen inside the blue frame in Figure 37. The resulting impedance of these voltage dividers seen from the input has to be 50Ω. Since these annotation circuits has to handle and withstand peak voltages up to 100V and peak currents up to 2A, resulting in a peak power dissipation of up to 200 watts, it is not enough letting the divider handling all the current. The overall resistors used in this design can handle 100mW. Since the duration of these currents are just within micro seconds the resulting power dissipation is a lot less.

The problem is solved by adding one (for the compensation and free-wheel) and two (for the principal) resistors in parallel to the voltage divider. It has been taken into account that the resulting impedance seen on the input still has to be 50Ω.

Table 36. Annotation for the four different input types on the KPS.

Principal circuit	More than 22 times
Compensation circuit	More than 2.58 times
Free-wheel circuit	More than 1.35 times
Trigger-input	More than 5 times

Note that these annotation circuits are dimensioned only for short high voltage pulses. Applying any high continuous voltages AC or DC would result in circuit damage.

5.3.2 Butterworth-filter

The Butterworth-filter inside the green frame in Figure 37 works as an anti-aliasing filter for the ADC. Since the ADC is set to work at minimum 10MHz, the cut-off frequency of this filter is set to 5MHz. This is a second order differential filter. By using such a configuration one can convert a single-ended signal into a differential one. This indicates that the second input has to be fixed at a constant voltage. The gain of the pass-band of the filter is one, so the differential output has the same resulting amplitude as the amplitude of the single-ended input.

5.3.3 Signal biasing for the ADC

The ADCs differential input handles input voltages from 1V to 3V. This is as mention before the reason why the Opamps have an input common mode voltage of 2V. What having a common mode voltage at 2V means is that the output signal zero level of the Opamps are at 2V. This means that the values on the input can be negative. As discussed in the preliminary studies, the principal circuit is the only circuit with a negative voltage signal of any importance. The compensation and free-wheel have only a positive voltage signal of importance. This means that having the Opamps output signal zero level at 2V would mean that 80% of the ADC input range is used for the principal circuit and as little as 50% for the two others. By adding an offset to the input signal these percentages can be made 100%. A better way to do this than to add an offset to the signal from the pickup is to apply this offset to the other input of the differential filter; the input not used by the signal from the pickup.

The offset of the principal circuit is different from the other two, since the input signal has negative values of interest. This offset is made of a voltage divider, and can be seen in Figure 37, inside the red frame. The voltage needed to offset the other two circuits is the same as for the common mode voltage: 2V.

5.3.4 High-Speed Clamping Diodes

The ADCs are not design to handle negative voltages, so this has to be taken in to account when designing the circuitry. The only case where any of the outputs of the Opamps goes outside its range and to a negative voltage is when only one of the two branches is firing and the beam energy is above 4 TeV. The ADCs are single supply and can not handle negative voltages. To prevent this negative voltage from entering the input of the ADCs there are clamping diodes from the Opamps outputs and to ground. These are dimensioned to sink the current that the Opamp uses to try to bring the output-node to a negative voltage. They can be seen between the green and the violet frame in Figure 37. The diodes to the left of the green frame are for preventing the input voltage to the Opamp to exceed ±5V.

5.3.5 RC-filter

Before the signal enters the ADC it passes through another filter, this filter works mainly as a buffer between the Opamp and the ADC and is necessary due to the heavy switching on the input of the ADC and the fact that this can disturb the behaviour of the Opamp. The Butterworth filter has a cut-off frequency at 5 MHz. The RC-filters cut-off frequency is at 7 MHz which is rather pointless, but again, its purpose is mainly buffering.

5.3.6 Devices

The differential operational amplifiers used in the circuit are from National Semiconductors called LMH6550MM [12]. The high-speed clamping diodes are from Philips and are called PMLL4448. The common resistors and capacitors used for the board are the SMD 0805-packages, but other packages are also used; the smallest 0603 and the larger ones 1210 and 2512.

5.3.7 Schematics

The analog circuit schematics of the KPS are illustrated in Figure 38 to Figure 43. The figures show that the circuits single-ended input are on the left side and the differential output on the right side.

What is noticeable is that the circuits input within each branch are mirrored with respect to one another; more precisely, the circuitry around the Opamp is mirrored, except for the Opamp itself. The circuit in Figure 38 is a mirror of the circuit in Figure 39, Figure 40 a mirror of Figure 41 and Figure 42 a mirror of Figure 43.

The only difference this makes is that the polarity of the output is changed, and that is the aim of this, as it eases the routing to the input of the ADCs.

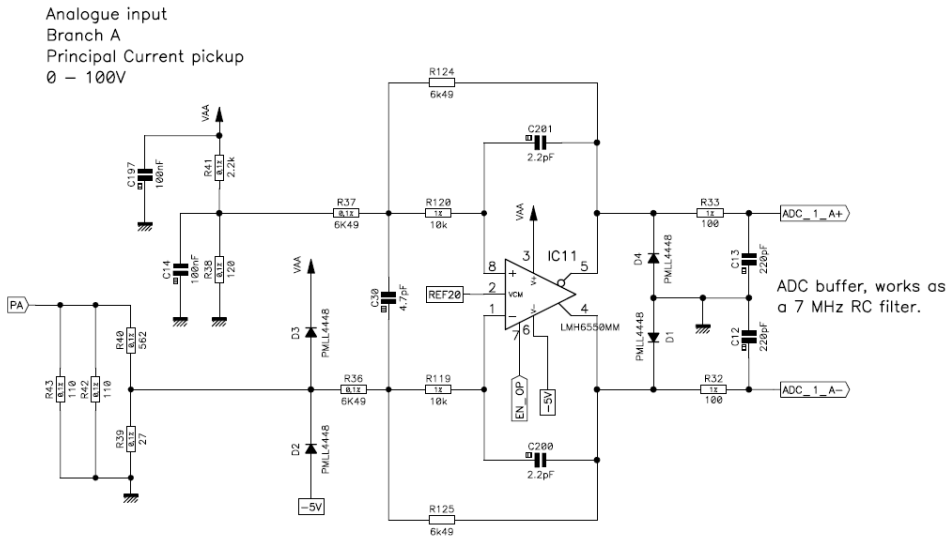

Figure 38. Annotation and filter for the principal current pickup in branch A.

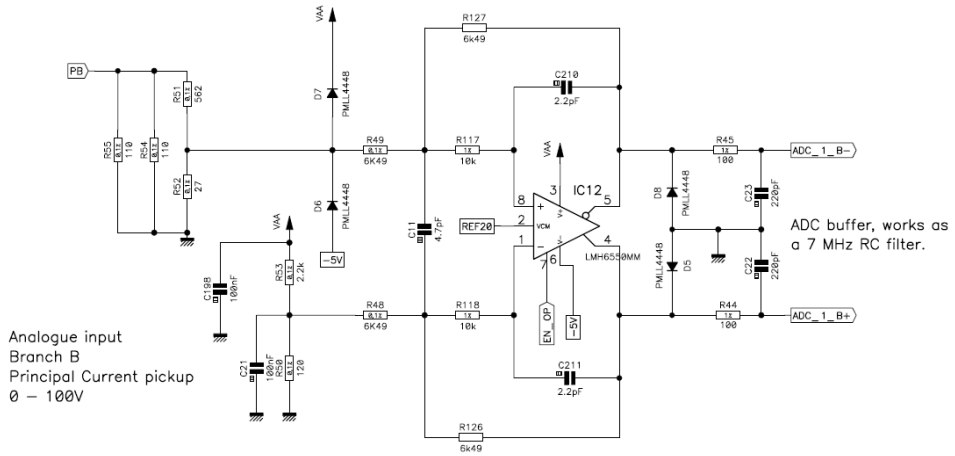

Figure 39. Annotation and filter for the principal current pickup in branch B.

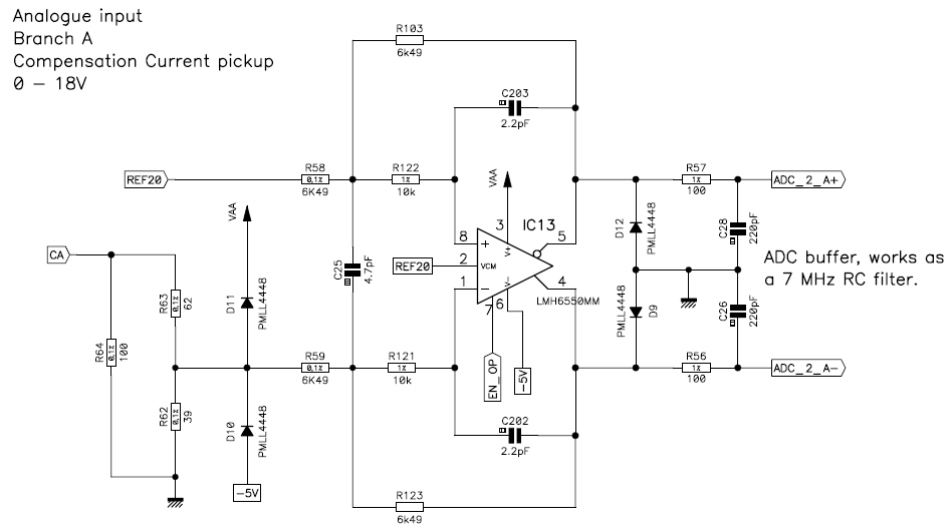

Figure 40. Annotation and filter for the compensation current pickup in branch A.

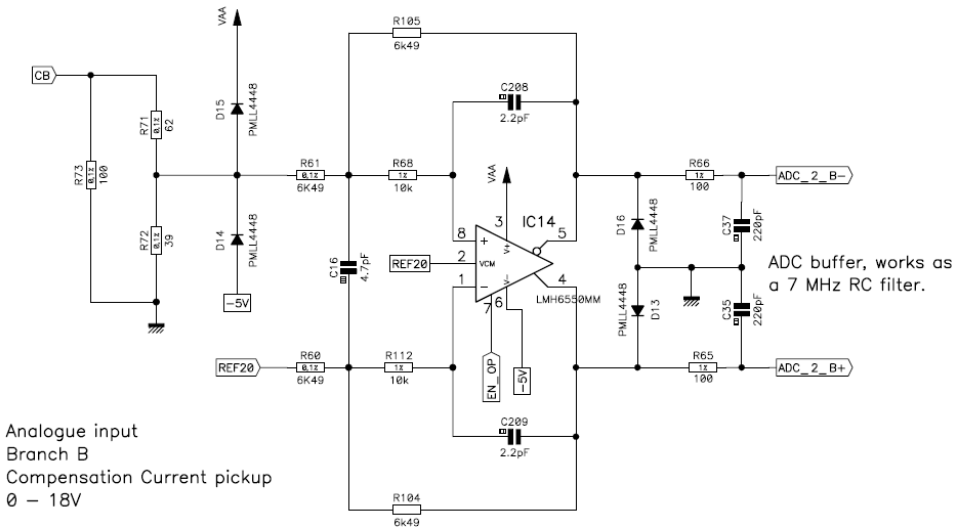

Figure 41. Annotation and filter for the compensation current pickup in branch B.

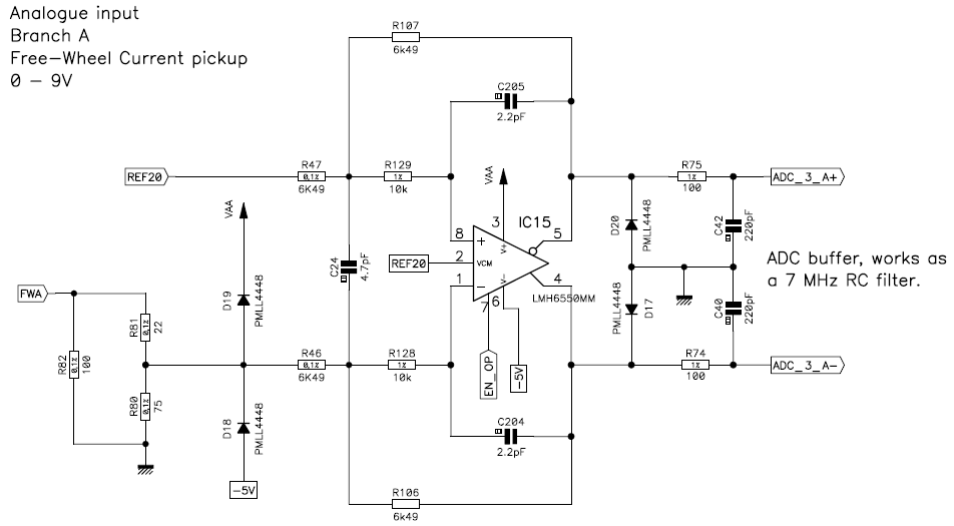

Figure 42. Annotation and filter for the free-wheel current pickup in branch A.

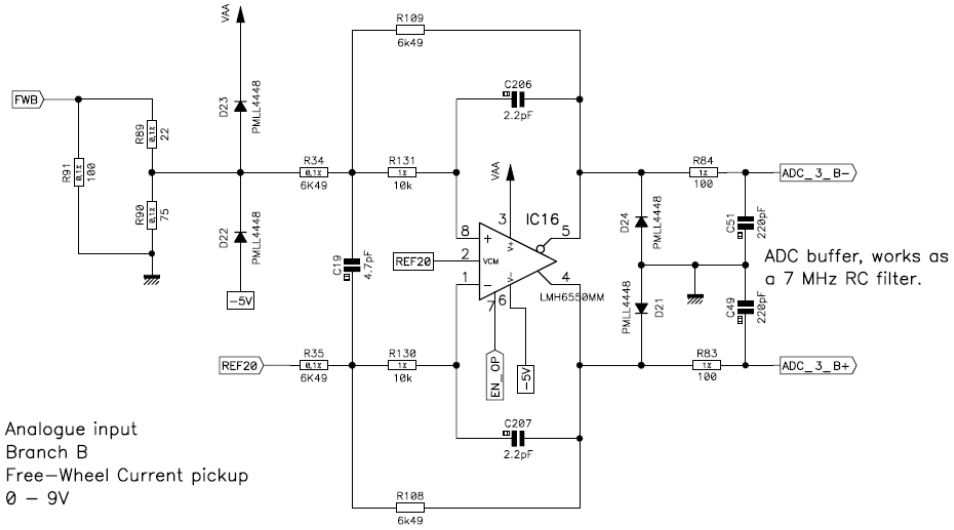

Figure 43. Annotation and filter for the free-wheel current pickup in branch B.

5.4 Digital acquisition, analysis and reporting circuitry

The digital circuitry consists mainly of a FPGA, a Flash-PROM for holding the configuration data for the FPGA, the six ADCs and the AnyBus-S module.

5.4.1 FPGA

The FPGA used in this design is a Xilinx Spartan 3 called XC3S1000-4FT256C. This is a BGA-chip which automatically insinuates that the PCB-card used in this design is either four or even six layers, depending on the number of pins utilized on the chip. Because a lot of the IOs of the FPGA are used, the PCB is six layers.

The resources utilized in the FPGA are about 30% so a lot of functionality can still be added. The FPGA is running on a 40 MHz clock and the VHDL-code can manage a clock frequency of 127 MHz so there is a good margin for all signals in the FPGA to get where they are going in time.

5.4.2 Flash-PROM

The FPGA needs a source of data when it is reconfigured on power up. This source is a Xilinx Flash-PROM called XCF04SVO20C [10]. This is a
4 MB storage device holding data even though it is powered down.

5.4.3 ADC

The six ADCs used on this board are dual 12-bits, 40MSPS, named ADC12D040 from National Semiconductors [11]. Dual means that one package contains two ADCs. This is convenient in terms of getting the same conditions for all the three signal pairs and in addition begin space-saving. These chips can run at maximum 55MHz, but specifications are guarantied only up to 40MHz.

5.4.4 AnyBus-S module for the Profibus DP

The AnyBus-S module is produced and delivered from HMS Industrial Networks in Sweden [5][6]. This module is easy to implement and work with.

5.4.5 Power Supply and References

The power supply voltages needed for this board are ± 5V, 3.3V, 2.5V and 1.2V. A reference voltage of 2.00V is also needed. The power supply voltages for the Spartan-3 FPGA were already designed and verified by use in other designs in the department so there was no point in redesigning these, although some minor modifications were made. All the regulators for positive voltages are using the +5V provided by the power supply in the crate.

The crate also provides a ±15V, the -15V was used to power the regulator making the -5V. To ease the gap between the input-voltage and the output-voltage for the regulator, two high power rating resistors are added in series with the input of the regulator. This creates a voltage drop over the resistors resulting in a decreased input voltage for the regulator, again resulting in lower thermal stress on the regulator.

Before the external voltages are entering the regulators they are filtered through a LC-filter, illustrated in Figure 44. There are three of these filters on the board; one for the -15V and two parallel ones for the +5V. The two in parallel are for the digital +5V and for the analog +5V.

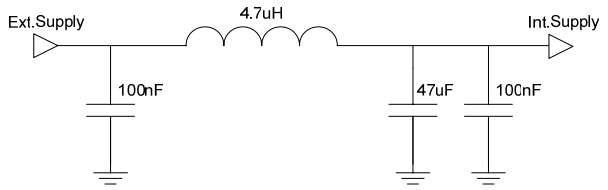

Figure 44. LC-filter for filtering the supply voltages.

5.4.6 Devices

The 3.3V is regulated with a LM1117DT-3 [15] and the 1.2V with a LP3964EMP-ADJ [14]. Both are from National Semiconductors. The 2.5V was made from a XC6201P252PR from Torex [13]. The -5V are made with the help of a LM2991S [16].

The 2.00V biasing voltage reference was made from a voltage regulator as well, as oppose to a voltage reference chip. This is because it has to be able to deliver a relatively large amount of current and most voltage references are not able to do this. This trade off was made since the absolute accuracy of the voltage is less important than its ability to be stable. This voltage was made from a LM317LZ also from National Semiconductors [17].

All the regulators are linear (LDO) and not the switching type.

5.5 Board layout

The board size is 160x100mm, also known as a euro-card. It has six layers. The layout is done carefully with loyalty to as many of the written rules about mixing analog and digital circuitry as possible. [1][2][3][4]

The power-supply for the different parts are low pass-filtered before routed away from each other. The return current for the digital circuitry does not pass over any analog circuitry and visa versa.

The analog and digital parts are separated. The grounds for the digital and analog are separated with a cut, joint together in one point under the power supplies, the cut can be seen as the thick blue line in Figure 45.

The analog parts are routed and laid out with close to perfect symmetry. The power-supplies and reference-voltage does not in any case cross under either the operational amplifiers or the gain-setting resistors. The ground plane is opened up under both the amplifier and the gain-setting resistors as well. This is to prevent capacitive coupling of high-frequency noise into the analog signals. The open grounds are illustrated as blue boxes in Figure 45.

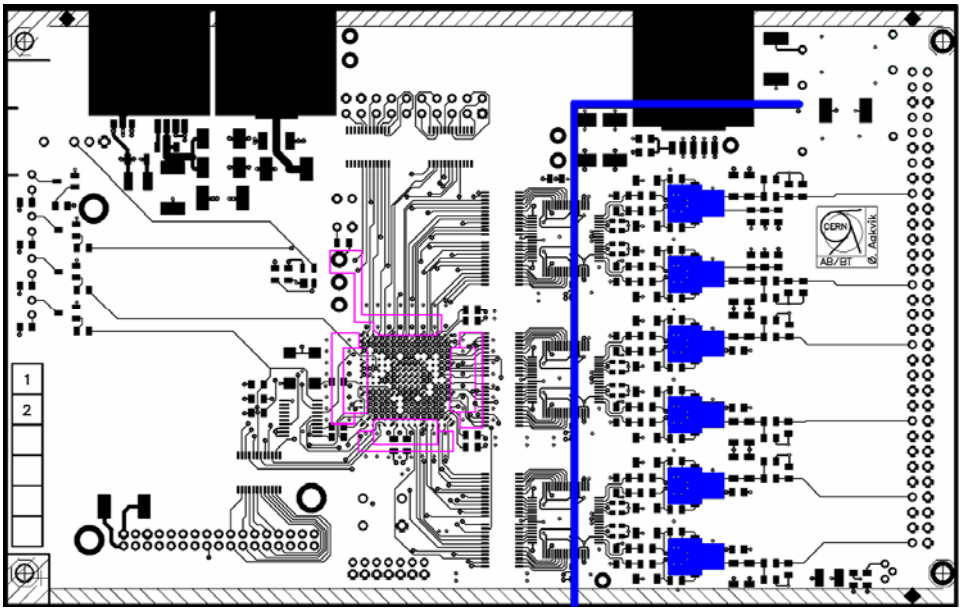

Figure 45. An illustration of ground cuts (blue line and boxes).

The clock lines from the crystal and to the FPGA and from the FPGA to the three ADCs are made as short as possible. The lines to the ADCs are made differential and stack on top of each other with grounded tracks over and under. This is illustrated in Figure 46. The purpose is to isolate the clock from feeding into the rest of the circuitry.

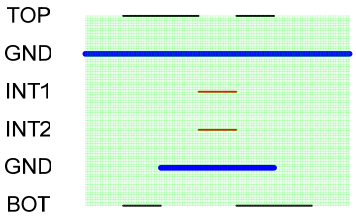

Figure 46. Layout of differential clock lines to the ADCs.

Some rules are also broken, one of these are the rule of placement for digital and analog circuitry with respect to a boards connector, which states that the digital part of the board should be closest to the connector, or even more precise, that the parts with highest frequency should be closest to the connector. In this layout it is exactly the opposite, this because the acquired signals are presented on the connector and the digital reporting of the analysis is done through the AnyBus-S module mounted on the opposite side of the connector. Forcing this rule on this board would be unpractical and a bad choice. Figure 47 shows a top view of the layout, with frames encapsulating the digital (red) and the analog (blue) parts of the board.

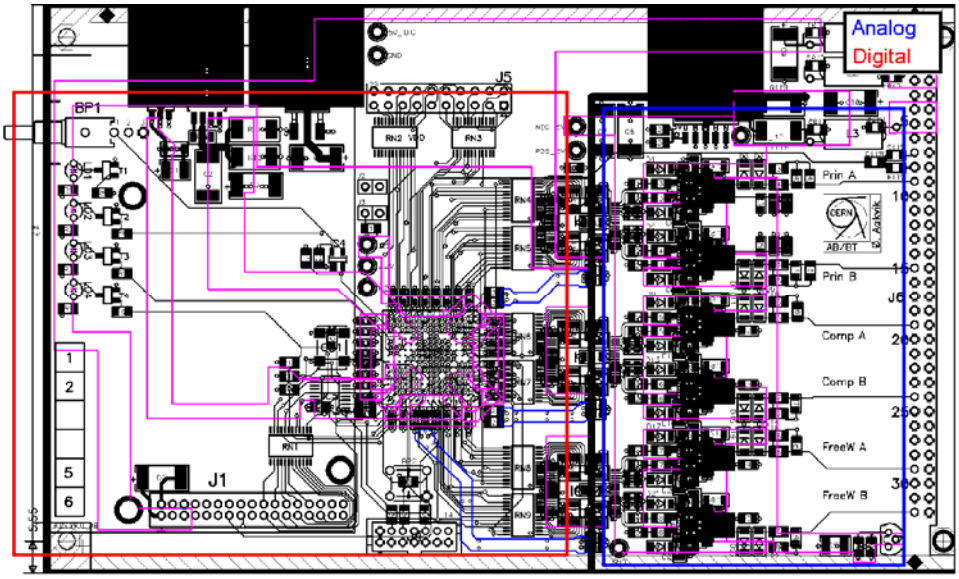

Figure 47. The top view component-layout of the board, with frames encapsulating the digital (red) and analog (blue) part of the board.

6 User Interfaces

6.1 Front Panel-interface

The front panel of the KPS is illustrated in Figure 48.

The four leftmost diodes are connected to the AnyBus-S module. The two left ones indicate if the communication channel is established, the top one is red if not, and the bottom one is green if it is. The top right one is for diagnostics [6]. The bottom left one is not in use.

The four lined up green LEDs are for the KPS, the leftmost lights up when calibration is done, the second from the left is an extra, the third from the left lights up when the FPGA has connected to the AnyBus-S module, and if it is blinking the configuration has failed. The rightmost LED lights up when the FPGA has been configured.

Reset button is for resetting the KPS. This button has the same function as the reset through the Profibus DP-network

Rotary address switches for the AnyBus-S module. These must be set to a unique address. The left rotary switch is ones and the right one is tens.

End termination switch. If this board is at the end of a communication chain, this switch should be turned on.

Profibus DP-connector. It is where the module is connected to the Profibus DP-network.

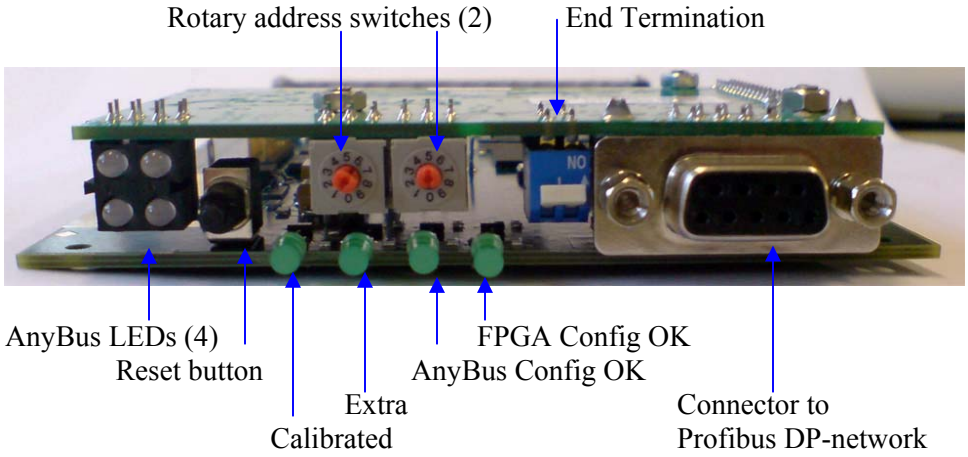

Figure 48. Frontpanel of KPS.

6.2 KPS_test-interface

The software-interface of the board is illustrated in Figure 49. This is mainly developed to test and verify the communication with the KPS. This communication will be handles by a actual PLC in the future.

The interface is divided into two sections; the bottom one is for sending data to the KPS, and the top one for receiving the data from the KPS. The writing (red) marked with "Testing" is only used when running the digital circuitry test with the FPGA configured with the file Test_ADC.mcs.

The IPOC_rslt-vector can be decoded with the help of Table 27.

The margins entered are by default 10% and 10 us/10, which is 1us. The values entered can be between 0 and 255.

The beam energy is default 450 GeV. The maximum input value is 7500 GeV.

The Reset-button resets the KPS. The KPS is then ready for a new analysis.

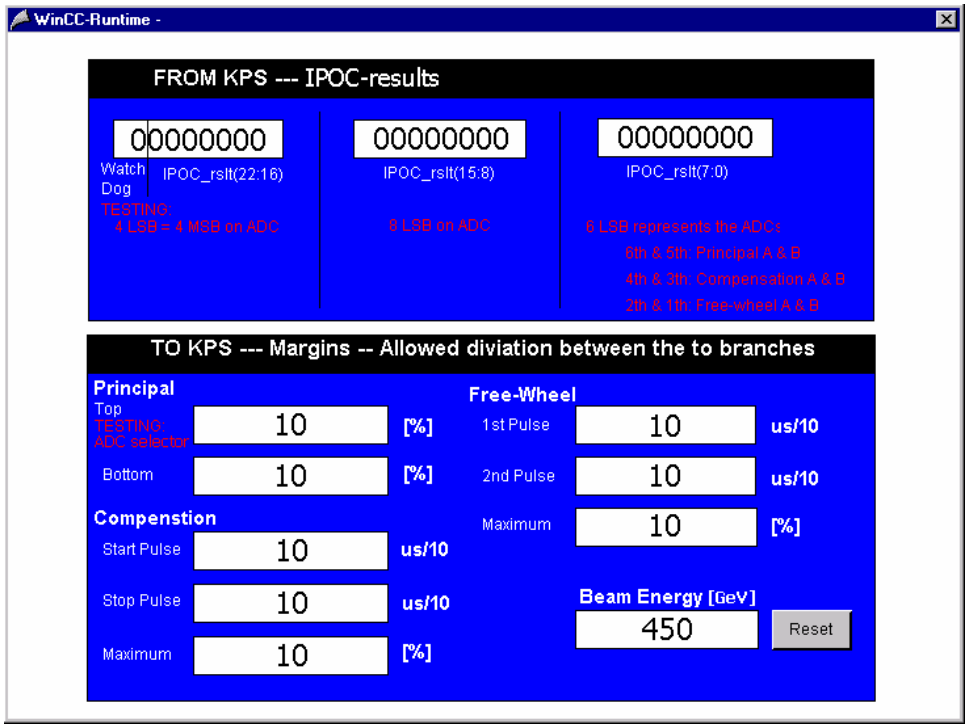

Figure 49. Software-interface of the KPS.

7 Measurements and test

7.1 Introduction

This section contains an overall description of how to do measurements and conduct simple tests to make sure the behaviour of the KPS is correct. Complete descriptions of the test procedures are located in the Appendix

The first step is an easy measurement procedure done on the KPS-board with and without power. The second step includes configuring the FPGA to test its IOs and the communication to the Profibus DP Master PC. The third tests are conducted when the card is connected to the MKDG and Profibus DP-network and is about how to confirm a correct KPS behaviour.

7.2 Test Equipment

The test equipment needed to conduct the different tests is specified here.

Step 1:

- FLUKE 112: Multimeter.
- HAMEG HM7042-5: Triple power supply for powering the KPS.

Step 2 and 3:

- FLUKE 112: Multimeter.
- HAMEG HM7042-5: Triple power supply for powering the KPS.
- PC with Siemens Step 7 and WinCC: for testing the Profibus communication.
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- LeCroy WaveRunner: Digital oscilloscope.
- MKDG: Ready to pulse at all energy levels.
- Manual/Automatic Pulse Generator.
- KPS circuit schematics.

7.3 Test Procedure

All test procedures are set up in this format and can be found in the appendix:

Test Case ID: <ID identifying the test>

Purpose
<The purpose of the test>

Setup
<How is the system set up before testing>

Equipment
<Which equipment is used to perform the test>

Dependencies
<Does the test rely on another test?>

Description
<How will the test be performed>

Expected Results
<The expected results of the test>

Table XX: <Step by step list of the test.>

TEST ID			
Step	**Action**	**Expected Result**	**Observed Result**
1	-	-	-

7.4 Step 1: Measurements

Measuring the impedance level between the different voltage levels is a good way to find out if the powering of the card is connected correctly. This is primarily to find if there are any short-circuits between the different parts. This is done before any voltage is applied to the card. When this test is complete the power can be applied. The power supply current-limiter fuse should be used to prevent any burnout due to undetected short circuits. When the KPS is powered up, the next things to do is measure and confirm the different voltage levels on their dedicated test pins. When these are confirmed the time has come to test the digital circuitry.

7.5 Step 2: Testing of digital circuitry

The digital circuitry consists of a pushbutton, a 15V trigger input, four LEDs, a test-connector, six ADCs and the AnyBus-S module.

The first test is to confirm that everything is connected as it should. This can be done before connecting it to the generator and can also be done before mounting the AnyBus-S module. The digital outputs are connected to a 1Hz signal toggling the LEDs, the test-connectors and the AnyBus-S module-connector. By using an oscilloscope all outputs can be tested. The trigger input and the pushbutton is tested by applying a 15V pulse for the trigger, this would lead to halting the 1Hz blinking LEDs turning it constantly on. Pressing the pushbutton makes the LEDs start blinking again.

The second test is to establish the communication channel over the Profibus DP-network. This test must be made after mounting the AnyBus-S module. After connecting the Profibus DP communication-cable and running the right program on the PC, this should result in a LED on the AnyBus-S module turning from red to green. This means that the module has been initialized correctly and communication channel has been established.

The third test is to make sure that none of the output pins of the ADCs are stuck at either zero or one. This test is conducted while the KPS is connected to the MKDG, this simply because CERN has no lab-equipment that can simulate the pulsing amplitude and speed that the MKDG outputs. The test is conducted with the MKDG set to pulse at 4 TeV. The interface to the KPS used in this test is the Profibus DP Master PC. Six output bits from the KPS are now dedicated to communicate the status of the ADC outputs. When the MKDG is done pulsing, the KPS should output a one for the ADCs working correctly and a zero for the ones that are not.

To visually inspect the bits on a malfunctioning ADC, the “number” of the ADC has to be communicated to the KPS. The KPS then sends back a 12 bit vector of the analysis of this ADC, this contains a one for the working outputs and a zero for the non-working. Non-working meaning stuck at either zero or one.

If an error occurs, the test should be verified with more tests, such as a test rerun or eventually a probing of the actual pin.

7.6 Step 3: Testing the KPS behaviour

7.6.1 Installing

The first step is to insert the board in the crate and connecting the Profibus DP connector. If the board is at the end of a Profibus DP chain either the cable termination or the board termination switch has to be turned on. Turning both on could result in malfunctioning.

7.6.2 Configuring

This can be disregarded if the PROM already is loaded.
The next step would be to load the PROM with a configuring file. For this iMPACT from Xilinx ISE can be used. The JTAG is connected to the board and the PROM is programmed. If the PROM is reprogrammed, the FPGA will be configured as soon as the reconfiguring button next to the JTAG interface connector on the board is pushed.

7.6.3 Resetting

In any case, the board should be reset before use, either by pushing the push-button or via the Profibus DP. When resetting the board the margins for the analysis is set to its default and the beam energy level is set to the injection energy level. The KPS-status is now armed. It is now waiting for the triggering of a beam dump or any erratic currents in the MKDG.

7.6.4 Setup

Before the board is ready for use, the beam energy and the margins for the analysis have to be sent to the card via the Profibus DP. The beam energy is a 16 bit vector going from 0000_{hex} to $FFFF_{hex}$, ranging from 0 to 7500 GeV. The range of the margins is from 00_{hex} to FF_{hex}, ranging from 0 to 256 % for the measurement on voltage levels and 0 to 25.6μs for those to do with timing.

7.6.5 Checking the accuracy

The test is done at 450 GeV for the principal- and compensation-circuits analysis and 2000 GeV for the free-wheel circuit analysis. The external power-supply is used as input instead of the MKDG outputs. The voltage on the external power-supply is set to just above the threshold calculated in Equation 1, Equation 4 and Equation 6. It is important to be above this threshold because voltages below 50% will not trigger any analysis.

The following will be to set the allowed margin for the principal maximum value analyses to zero percent. Next step is forcing a trigger of the circuit with the help of the Manual/Automatic Pulse Generator. The report states maximum values not within margins. Reset the circuit and increase the margin to one percent. Trigger again. The analysis should now state that the maximum is within margins.

Redo the test with the compensation and the free-wheel maximum analysis.

7.6.6 Forcing erratic report

Having the KPS connected to the MKDG, removing the Trigger and then triggering the MKDG, the board can be forced to report erratic currents in the MKDG. This will not trigger any analysis of the MKDG, but a report on which parts of the MKDG triggered the event.

7.6.7 Forcing pulse missing report

Instead of removing the Trigger connection, one or more of the connections from the current pickups are removed. Now when there is a beam dump, the KPS will send a pulse missing report. This report contains information on which part of the MKDG malfunctioned. There will not be done any analysis on the parts with now detected pulse in, only the parts of the MKDG that seems to work.

8 Discussion

When looking back on the process of developing the KPS-module at the result of this process, it has progressed very smoothly.

The project started with the preliminary studies of the MKDG. These studies resulted in revealing a nice and appreciated linear behaviour of the MKDG with respect to the beam energy, a great advantage when converting this behaviour into mathematical functions.

The development of the FPGAs firmware went very well, this due to knowledge about VHDL-programming through several courses at the University. A lot of time has been spent making the code easy to understand and to make common blocks that can be reused. Common blocks are a big advantage in this application as there are six analysis modules containing a lot of the same logic.

The communication between the KPS and the PLC has been nothing but unproblematic and works fine.

The most difficult part has been accomplishing the wanted resolution from the ADCs. Mixing digital and analog circuitry and demanding high resolution of the ADCs has been a big challenge. The circuit-board is some what noisy and the wanted 10 bit resolution is achieved by oversampling and digital filtering. This is very disappointing as the high-speed rules of layout and design has been followed thoroughly. The noise is the third harmonics of the clock and it leaks into every signal on the board, this was to some extent foreseen and countermeasures to prevent this from happening were made in the layout of the circuit board. I have absolutely no idea how to make this circuit board less noisy.

A 10 bit resolution means that the minimum detectable deviation in the MKDG is about 2%. Since four of the bits are reserved to represent the dynamic range of the signal, there is six bits left to distinguish the differences within a certain beam energy level. Six bits is 64 levels, had there been 100 levels one could say that the resolution was 1% and with 50 levels one could say 2 %, but with 64 levels this resolution is about 2%. This is more than enough to distinguish a good MKDG from a bad one.

The board size is as required; 160mm x 100mm, and consists off over 400 parts.

The remaining part is to fully integrate the KPS in the automated interlock-system in each of the 30 MKDs.

9 Conclusion

The goal of the project was to develop a surveillance system to confirm the correct behaviour of one MKDG.

Preliminary studies have been conducted and the behaviour of the MKDG has been revealed. On the basis of these revelations, a working prototype of the board has been made and tested on the system.

The analysis on the MKDG is completed and a resolution of 10 bits has been accomplished.

The KPS communicates with a PLC and can be fully operated by the PLC.

The analog and digital circuitry fits on a 160mm x 100mm PCB.

The system has undergone extensive testing and been rated successful.

When looking beyond the disappointment of the noise on the circuit board and comparing the resulting KPS-system to the system requirements. The conclusion is that the KPS is within the specifications; hence the goal of the project is accomplished.

10 List of References

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Appendix A

Tests

Test Case ID: T-KPS-0

Purpose
The purpose is measuring the impedance values between test pins, this to rule out any short-circuits and/or wrong impedance levels between the voltage planes.

Setup
The board is not connected to anything. It does not matter if the Anybus-S module is mounted or not.

Equipment
- FLUKE 112: Multimeter.
- KPS circuit schematics

Dependencies
None.

Description
The multimeter is set to measure impedance. One probe is connected to ground. Then the other probe is used to measure the impedance between the different pins.

Table T0: Impedance measurement checklist.

TEST ID T-KPS-0			
Step	**Action**	**Expected Result**	**Observed Result**
1	Connect one probe to the ground of the card.		
2	Measure test pin marked 1.2V	209Ω ±5%	
3	Measure test pin marked 2.5V	424Ω ±5%	
4	Measure test pin marked 3.3V	582Ω ±5%	
5	Measure test pin marked +5V	560Ω ±5%	
6	Measure test pin marked -15V	>1MΩ ±5%	
7	Measure test pin marked -5V	903Ω ±5%	
8	Measure test pin marked 2V	139Ω ±0.2%	
9	Measure on pin Trigger	34kΩ ±2%	
10	Measure on pin PrinA	50.7Ω ±0.2%	
11	Measure on pin PrinB	50.7Ω ±0.2%	
12	Measure on pin CompA	50.6Ω ±0.2%	
13	Measure on pin CompB	50.6Ω ±0.2%	
14	Measure on pin FreeWA	49.4Ω ±0.2%	
15	Measure on pin FreeWB	49.4Ω ±0.2%	

Test Case ID: T-KPS-1

Purpose
The purpose is measuring the different voltage levels on the KPS.

Setup
Connect to a lab power-supply with an electronic current limiter fuse. The limit for the two voltages used is set to 900mA.

Equipment
- FLUKE 112: Multimeter.
- HAMEG HM7042-5: Triple power supply.

Dependencies
The test relies on the previous test: T-KPS-0.

Description
The multimeter is set to measure DC voltage. One probe is connected to ground and the other is used to measure the voltage on the test pins.

Table T1: Voltage measurement checklist.

TEST ID T-KPS-1			
Step	**Action**	**Expected Result**	**Observed Result**
1	Connect one probe to the ground of the card.		
2	Measure test pin marked 1.2V	1.2V ±2%	
3	Measure test pin marked 2V	1.99V ±0.5%	
4	Measure test pin marked 2.5V	2.5V ±1%	
5	Measure test pin marked 3.3V	3.3V ±1%	
6	Measure test pin marked +5V	+5V ±5%	
8	Measure test pin marked -5V	-5V ±5%	
7	Measure test pin marked -15V	-15V ±5%	

Test Case ID: T-KPS-2

Purpose
The purpose is testing the connections to the LEDs, the trigger-input, the push-button and the test-connector.

Setup
The KPS is connected in the crate, the Test_FPGA.mcs is downloaded to the PROM and only the trigger signal is connected.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- Manual/Automatic Pulse Generator.
- LeCroy WaveRunner: Digital oscilloscope.

Dependencies
The test relies on the two previous tests: T-KPS-0 and T-KPS-1.

Description
The KPS is installed in the crate and the trigger-signal from the Manual/Automatic Pulse Generator is connected to the trigger-signal input. The PROM is loaded through the JTAG-inteface with the file: Test_FPGA.mcs and the FPGA is reconfigured by pressing the configuration button next to the JTAG.

The program will make three of the front LEDs blink with 1Hz, the fourth one is to confirm correct configuration of the FPGA and this one is just blinking when the configure-button is pressed. The program is interfaced through the Trigger-signal and the pushbutton.

Expected Results
When there is a pulse on the Trigger-signal-input the LEDs will stop blinking and the signals to the test-pin-connector will stop toggling. Pressing the pushbutton will bring the LEDs and test-pins back to blinking and toggling.

Table T2: Testing connection to different I/O.

TEST ID: T-KPS-2			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: Test_FPGA.mcs		
3	Press the reconfigure pushbutton.	3 LEDs starts blinking and test-connector pins toggles. (1Hz)	
4	Make a triggering pulse on the Trigger-signal-input.	LED stops blinking and goes ON and test-connector pins go HIGH.	
5	Pressing the pushbutton	3 LEDs starts blinking and test-connector pins toggles. (1Hz)	

Test Case ID: T-KPS-3

Purpose
The purpose is testing that the Profibus-DP network is working.

Setup
The KPS is installed in the crate and the Test_ADCs.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP Master.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- Manual/Automatic Pulse Generator.

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1 and T-KPS-2.

Description
The PROM is loaded with the file: Test_ADCs.mcs and the KPS is connected to the PC simulating the Profibus-DP Master. The PC is running KPS_Test. The address of the of the KPS is set to 6.

Expected Results
The expected result is that the red light on the AnyBus-S module switches to green and that the interface-blocks in the KPS_Test program on the Profibus-DP Master PC changes from gray to white.

Table T3: Testing AnyBus-S module.

TEST ID: T-KPS-3			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Set the address of the KPS to 6.		
3	Configure the PROM with the file: Test_ADCs.mcs		
4	Press the reconfigure pushbutton.	The red light on the Anybus-S module turns to green and that the interface-blocks changes from gray to white.	

Test Case ID: T-KPS-4

Purpose
The purpose is testing that none of the converters have pins stuck at zero or one.

Setup
The KPS is fully installed in the crate and the Test_ADCs.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP Master. All interfacing of the test is through the PC Profibus-DP master interface.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- Manual/Automatic Pulse Generator.

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1 and T-KPS-3.

Description
The PROM is loaded with the file: Test_ADCs.mcs and the KPS is connected to the PC simulating the Profibus-DP Master. The Profibus-DP master simulation PC is running KPS_Test. The MKDG is set to pulse at 450 GeV, the pulsing continues in steps of 1000 GeV until 7 TeV or the status bits show all ADCs OK.

Expected Results
After pulsing at 4 TeV the expected result is to have all converters returning an OK status. This will be returned in the six LSBs of the IPOC-results.

Table T4: Testing connection to different I/O.

TEST ID: T-KPS-4			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: Test_ADC.mcs		
3	Press the reconfigure pushbutton.		
4	Starting to pulse at 450 GeV.		
5	Pulsing at 1 TeV		
6	Pulsing at 2 TeV		
7	Pulsing at 3 TeV	The six LSBs of the IPOC-results are all ones, test OK. If NOT OK pulse at higher energy	
8	Pulsing at 4 TeV	The six LSBs of the IPOC-results are all ones, test OK. If NOT OK pulse at higher energy	
9	Pulsing at 5 TeV	The six LSBs of the IPOC-results are all ones, test OK. If NOT OK pulse at higher energy	
10	Pulsing at 6 TeV	The six LSBs of the IPOC-results are all ones, test OK. If NOT OK pulse at higher energy	
11	Pulsing at 7 TeV	The six LSBs of the IPOC-results are all ones, test OK. If NOT OK go to step 12.	
12	Converter malfunction returns a zero in the six LSBs of the IPOC-results. IPOC-result bit 5 represents Prin A, bit 4; Prin B, bit 3; Comp A, bit 2; Comp B, bit 1; FreeW A and bit 0; FreeW B. To have a closer look at the bit making the error use the “principal circuit maximum value”-margin entry box on the Profibus-DP Master and type: 1 for viewing the Prin A ADC analysis. 2 for viewing the Prin B ADC analysis. 3 for viewing the Comp A ADC analysis. 4 for viewing the Comp B ADC analysis. 5 for viewing the FreeW A ADC analysis. 6 for viewing the FreeW B ADC analysis. This will display the 12 bit analysis-vector of the ADC in the bits 19 down to 8 and return a one for bits that are OK and a zero for those NOT OK. Not OK meaning either stuck at one or zero.		

Test Case ID: T-KPS-5

Purpose
The purpose is testing the accuracy of the principal circuit.

Setup
The KPS is installed in the crate and the KPS_prom.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP master and the lab power-supply is used to generate the two inputs to the KPS principal circuit. The manual/automatic pulse generator is connected to the KPS trigger-signal-input.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- Manual/Automatic Pulse Generator.
- HAMEG HM7042-5: Triple power supply for powering the KPS.
- FLUKE 112: Multimeter.
- Banana-plugs to BNC adapter.
- 1 to 2 T-connection BNC

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1, T-KPS-2 and T-KPS-3.

Description
The PROM is loaded with the file: KPS_prom.mcs and the KPS is connected to the PC simulating the Profibus-DP Master. The Profibus-DP Master PC is running KPS_Test. The lab power-supply simulates the pickup signals from the MKDG.

Both the inputs get the same signal so the differences between the two should be close to zero. The margins of the analysis is first set to 0%, the result should then be negative. Then for the next analysis the margins are set to 1%, the result should be positive.

Expected Results
The expected result is that the circuit can differentiate between a 0% and a 1% margin.

Table T5: Testing the accuracy of the principal circuit.

TEST ID: T-KPS-5			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: KPS_prom.mcs		
3	Press the reconfigure pushbutton.	The red light on the Anybus-S module turns to green.	
4	Adjust the lab power-supply to 3.50V and turn it **OFF!**		
5	Connect the lab power-supply to both the KPS Principal circuit branch inputs through the banana-plugs to BNC adapter.		
6	Press Reset on the KPS board.*	The left most light blinks and ends up green. IPOC-results on the Profibus-DP Master should display armed status.	
7	On the Profibus-DP Master: Set a 0% margin for the principal circuit maximum margin.		
8	Three steps should happen relatively quick: 1: Turn on the lab power-supply 2: Press the Trigger-button 3: Turn off the lab power-supply	Result of analysis appears on the Profibus-DP Master PC. Principal maximum result is negative. If not go to step 6 and try one more time(only one)	
9	Press Reset on the KPS board.*	The left most light blinks and ending up green. IPOC-results on the Profibus-DP Master should display armed status.	
10	On the Profibus-DP Master: Set a 1% margin for the principal circuit maximum margin.		
11	Three steps should happen relatively quick: 1: Turn on the lab power-supply 2: Press the Trigger-button 3: Turn off the lab power-supply	Result of analysis appears on the Profibus-DP Master PC. Principal maximum result is positive. If not go to step 9 and try one more time(increase the margin percentage untill is works)	

*Important that there are no signals present on the input when resetting.

Test Case ID: T-KPS-6

Purpose
The purpose is testing the accuracy of the compensation circuit.

Setup
This is done in almost the exact way as for the principal circuit.

The KPS is installed in the crate and the KPS_prom.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP master and the lab power-supply is used to generate the two inputs to the KPS compensation circuit. The manual/automatic pulse generator is connected to the KPS trigger-signal-input.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- Manual/Automatic Pulse Generator.
- HAMEG HM7042-5: Triple power supply for powering the KPS.
- FLUKE 112: Multimeter.
- Banana-plugs to BNC adapter.
- 1 to 2 T-connection BNC

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1, T-KPS-2 and T-KPS-3.

Description
The PROM is loaded with the file: KPS_prom.mcs and the KPS is connected to the PC simulating the Profibus-DP Master. The Profibus-DP Master PC is running KPS_Test. The lab power-supply simulates the pickup signals from the MKDG.

Both the inputs get the same signal so the differences between the two should be close to zero. The margins of the analysis is first set to 0%, the result should then be negative. Then for the next analysis the margins are set to 1%, the result should be positive.

Expected Results
The expected result is that the circuit can differentiate between a 0% and a 1% margin.

Table T6: Testing the accuracy of the compensation circuit.

TEST ID: T-KPS-6			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: KPS_prom.mcs		
3	Press the reconfigure pushbutton.	The red light on the Anybus-S module turns to green.	
4	**Adjust the lab power-supply to 1.50V and turn OFF!**		
5	Connect the lab power-supply to both the KPS Compensation circuit branch inputs through the banana-plugs to BNC adapter.		
6	Press Reset on the KPS board.*	The left most light blinks and ends up green. IPOC-results on the Profibus-DP Master should display armed status.	
7	On the Profibus-DP Master: Set a 0% margin for the compensation circuit maximum margin.		
8	Three steps should happen relatively quick: 1: Turn on the lab power-supply 2: Press the Trigger-button 3: Turn off the lab power-supply	Result of analysis appears on the Profibus-DP Master PC. Compensation maximum result is negative. If not go to step 6 and try one more time(only one)	
9	Press Reset on the KPS board.*	The left most light blinks and ending up green. IPOC-results on the Profibus-DP Master should display armed status.	
10	On the Profibus-DP Master: Set a 1% margin for the compensation circuit maximum margin.		
11	Three steps should happen relatively quick: 1: Turn on the lab power-supply 2: Press the Trigger-button 3: Turn off the lab power-supply	Result of analysis appears on the Profibus-DP Master PC. Compensation maximum result is positive. If not go to step 9 and try one more time(increase the margin percentage untill is works)	

*Important that there are no signals present on the input when resetting.

Test Case ID: T-KPS-7

Purpose
The purpose is testing the accuracy of the free-wheel circuit.

Setup
This is done in almost the exact way as for the principal and compensation circuit.

KPS is installed in the crate and the KPS_prom.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP master and the lab power-supply is used to generate the two inputs to the KPS free-wheel circuit. The manual/automatic pulse generator is connected to the KPS trigger-signal-input.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- Manual/Automatic Pulse Generator.
- HAMEG HM7042-5: Triple power supply for powering the KPS.
- FLUKE 112: Multimeter.
- Banana-plugs to BNC adapter.
- 1 to 2 T-connection BNC

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1, T-KPS-2 and T-KPS-3.

Description
The PROM is loaded with the file: KPS_prom.mcs and the KPS is connected to the PC simulating the Profibus-DP Master. The Profibus-DP Master PC is running KPS_Test. The lab power-supply simulates the pickup signals from the MKDG.

Both the inputs get the same signal so the differences between the two should be close to zero. The margins of the analysis is first set to 0%, the result should then be negative. Then for the next analysis the margins are set to 1%, the result should be positive.

Expected Results
The expected result is that the circuit can differentiate between a 0% and a 1% margin.

Table T7: Testing the accuracy of the free-wheel circuit.

TEST ID: T-KPS-7			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: KPS_prom.mcs		
3	Press the reconfigure pushbutton.	The red light on the Anybus-S module turns to green.	
4	Adjust the lab power-supply to 1.50V and turn **OFF!**		
5	Connect the power-supply when turned OFF. Connect the lab power-supply to both the KPS free-wheel circuit branch inputs through the banana-plugs to BNC adapter.		
6	Press Reset on the KPS board.*	The left most light blinks and ending up green. IPOC-results on the Profibus-DP Master should display armed status.	
7	On the Profibus-DP Master: Set a 0% margin for the free-wheel circuit maximum margin.		
8	**On the Profibus-DP Master:** **Set the beam energy to 2000 GeV.**		
9	Three steps should happen relatively quick: 1: Turn on the lab power-supply 2: Press the Trigger-button 3: Turn off the lab power-supply	Result of analysis appears on the Profibus-DP Master PC. Free-wheel maximum result is negative. If not go to step 6 and try one more time(only one)	
10	Press Reset on the KPS board.*	The left most light blinks and ending up green. IPOC-results on the Profibus-DP Master should display armed status.	
11	On the Profibus-DP Master: Set a 1% margin for the free-wheel circuit maximum margin.		
12	**On the Profibus-DP Master:** **Set the beam energy to 2000 GeV.**		
	Three steps should happen relatively quick: 1: Turn on the lab power-supply 2: Press the Trigger-button 3: Turn off the lab power-supply	Result of analysis appears on the Profibus-DP Master PC. Free-wheel maximum result is positive. If not go to step 9 and try one more time(increase the margin percentage untill is works)	

*Important that there are no signals present on the input when resetting.

Test Case ID: T-KPS-8

Purpose
The purpose is testing pulse missing reporting.

Setup
The KPS is installed in the crate and the KPS_prom.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP master and the MKDG.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- MKDG.

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1, T-KPS-2 and T-KPS-3.

Description
The PROM is loaded with the file: KPS_prom.mcs and the KPS is connected to both the PC simulating the Profibus-DP Master and the MKDG. The PC is running KPS_Test and the MKDG is set to pulse at 2000 GeV. One or more of the six signals is removed and the MKDG is triggered.

Expected Results
The expected result is that the KPS reports a pulse missing and which pulse(s) that are missing.

Table T8: Testing pulse missing report.

TEST ID: T-KPS-8			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: KPS_prom.mcs		
3	Press the reconfigure pushbutton.	The red light on the Anybus-S module turns to green.	
4	Press Reset on the KPS board.*	The light next to the pushbutton goes off a short time ending up green. IPOC-results on the Profibus-DP Master should display armed status.	
5	Type in beam energy level 2000 GeV on the Profibus-DP Master PC.		
6	Remove one or more of the six pickup signals.		
7	Trigger the MKDG.	The IPOC-results returns a pulse missing report and states which signals are missing.	

Test Case ID: T-KPS-9

Purpose
The purpose is testing erratic reporting.

Setup
The KPS is installed in the crate and the KPS_prom.mcs is downloaded to the PROM. The KPS is connected to the PC simulating a Profibus-DP master and the MKDG.

Equipment
- The crate for the KPS-board.
- Portable PC: for downloading configuring files.
- Xilinx JTAG: JTAG programming unit for the FPGA.
- PC with Siemens Step 7 and WinCC.
- MKDG.

Dependencies
The test relies on the two previous tests: T-KPS-0, T-KPS-1, T-KPS-2 and T-KPS-3.

Description
The PROM is loaded with the file: KPS_prom.mcs and the KPS is connected to both the PC simulating the Profibus-DP Master and the MKDG. The PC is running KPS_Test and the MKDG is set to pulse at 2000 GeV. The Trigger-signal is removed from the KPS-input and the MKDG is triggered.

Expected Results
The expected result is that the KPS reports erratics and which pulse(s) triggered this.

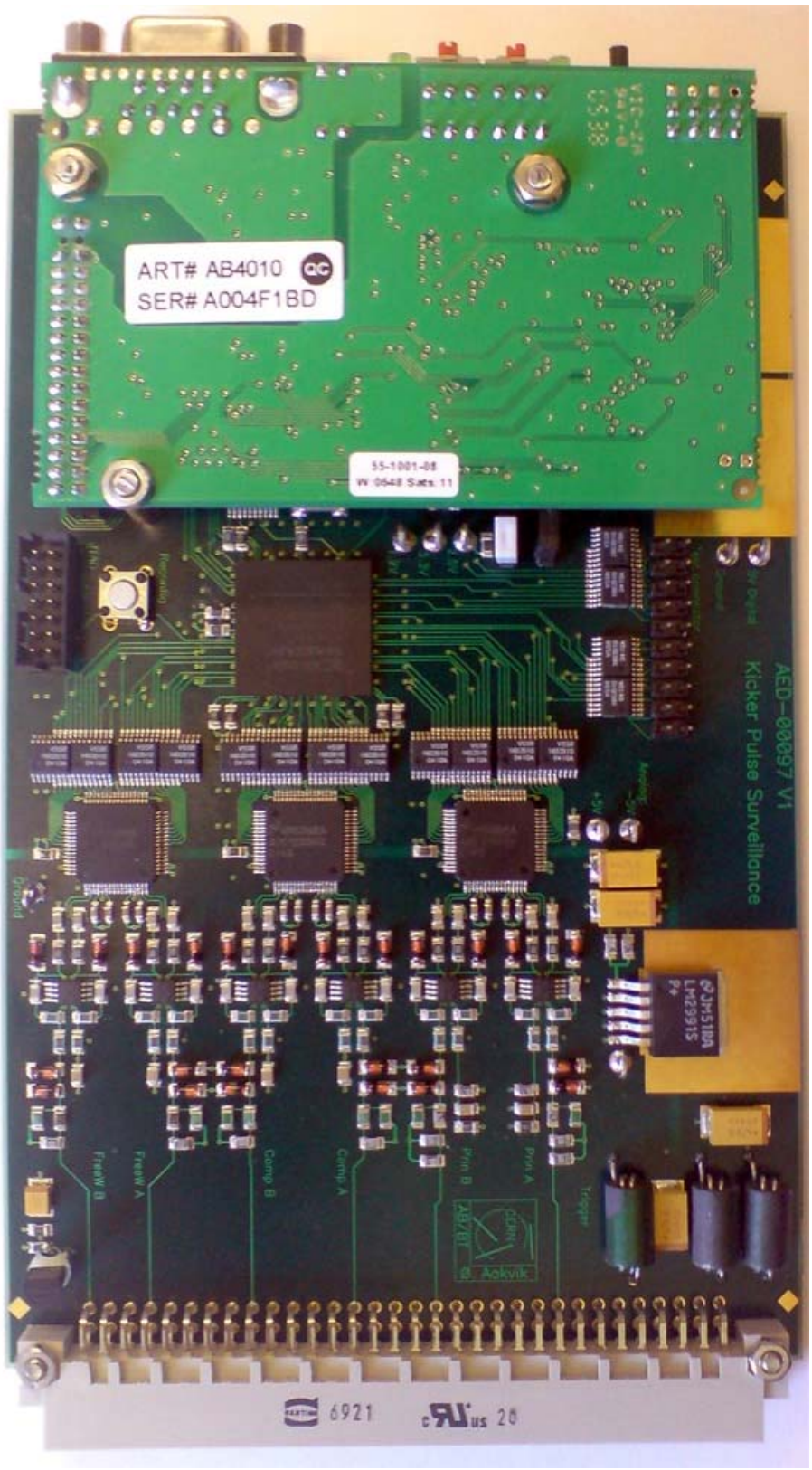
Table T9: Testing erratic report.

TEST ID: T-KPS-9			
Step	**Action**	**Expected Result**	**Observed Result**
1	Establish contact with the KPS via the JTAG	Green light on JTAG unit.	
2	Configure the PROM with the file: KPS_prom.mcs		
3	Press the reconfigure pushbutton.	The red light on the Anybus-S module turns to green.	
4	Press Reset on the KPS board.*	The light next to the pushbutton goes off a short time ending up green. IPOC-results on the Profibus-DP Master should display armed status.	
5	Type in beam energy level 2000 GeV on the Profibus-DP Master PC.		
6	Set the MKDG to fire at 2000 GeV.		
7	Remove the Trigger-signal.		
8	Trigger the MKDG.	The IPOC-results returns a erratic report and states which signals triggered it.	

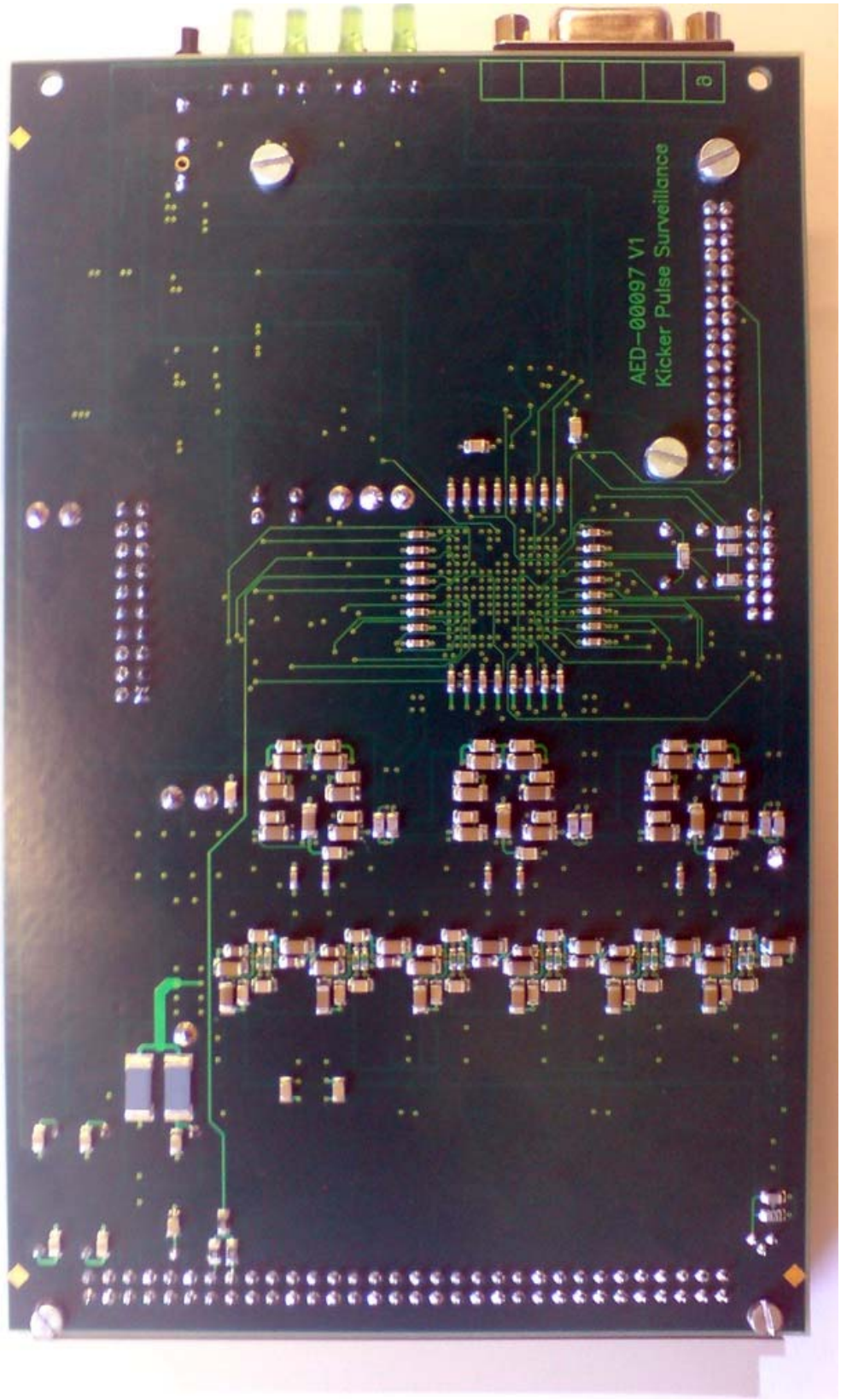
Appendix B

Pictures of the circuit board

Top-view of the circuit board



Bottom-view of the circuit board



Front- and side-view of the circuit board