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**Datum 971125**

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**ELFA artikelnr.**  
**71-307-35 BST82 N MOSFET SOT23**

**Antal sidor: 13**

# DATA SHEET

## **BST82**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical  
D-MOS transistor

BST82

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low  $R_{DS(on)}$

QUICK REFERENCE DATA

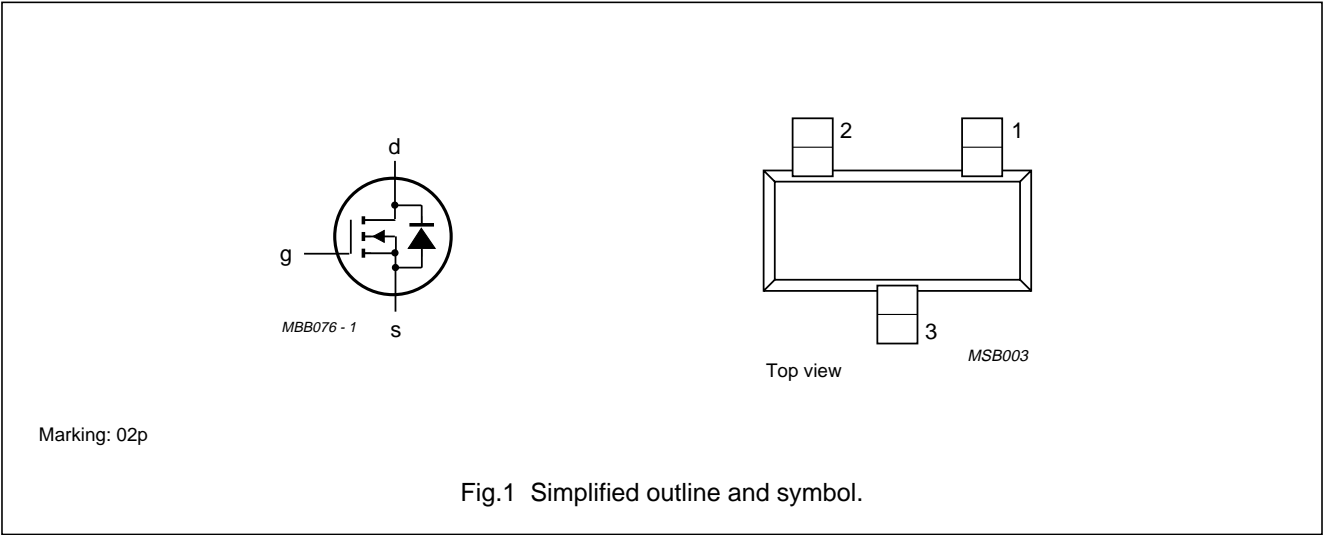
|  |               |      |             |
|--|---------------|------|-------------|
| Drain-source voltage   | $V_{DS}$      | max. | 80 V        |
| Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)          | $V_{DS(SM)}$  | max. | 100 V       |
| Gate-source voltage (open drain)                                     | $\pm V_{GSO}$ | max. | 20 V        |
| Drain current (DC)   | $I_D$         | max. | 175 mA      |
| Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ | $P_{tot}$     | max. | 300 mW      |
| Drain-source ON-resistance   |               |      |             |
| $I_D = 150\text{ mA}; V_{GS} = 5\text{ V}$                           | $R_{DS(on)}$  | typ. | 7 $\Omega$  |
|  |               | max. | 10 $\Omega$ |
| Transfer admittance  |               |      |             |
| $I_D = 175\text{ mA}; V_{DS} = 5\text{ V}$                           | $ Y_{fs} $    | typ. | 150 mS      |

PINNING - SOT23

1 = gate

2 = source

3 = drain



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## N-channel enhancement mode vertical D-MOS transistor

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BST82

### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

|   |               |      |                 |
|---|---------------|------|-----------------|
| Drain-source voltage  | $V_{DS}$      | max. | 80 V            |
| Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms) | $V_{DS(SM)}$  | max. | 100 V           |
| Gate-source voltage (open drain)                            | $\pm V_{GSO}$ | max. | 20 V            |
| Drain current (DC)  | $I_D$         | max. | 175 mA          |
| Drain current (peak)  | $I_{DM}$      | max. | 600 mA          |
| Total power dissipation up to $T_{amb} = 25$ °C (note 1)    | $P_{tot}$     | max. | 300 mW          |
| Storage temperature range                                   | $T_{stg}$     |      | –65 to + 150 °C |
| Junction temperature  | $T_j$         | max. | 150 °C          |

### THERMAL RESISTANCE

|                                   |               |   |         |
|-----------------------------------|---------------|---|---------|
| From junction to ambient (note 1) | $R_{th\ j-a}$ | = | 430 K/W |
|-----------------------------------|---------------|---|---------|

### Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

# N-channel enhancement mode vertical D-MOS transistor

BST82

## CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$I_D = 10\text{ }\mu\text{A}$ ;  $V_{GS} = 0$

$V_{(BR)DSS}$  min. 80 V

Drain-source leakage current

$V_{DS} = 60\text{ V}$ ;  $V_{GS} = 0$

$I_{DSS}$  max. 1.0  $\mu\text{A}$

Gate-source leakage current

$V_{GS} = 20\text{ V}$ ;  $V_{DS} = 0$

$I_{GSS}$  max. 100 nA

Gate-source cut-off voltage

$I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

$V_{(P)GS}$  min. 1.5 V  
max. 3.5 V

Drain-source ON-resistance

$I_D = 150\text{ mA}$ ;  $V_{GS} = 5\text{ V}$

$R_{DS(on)}$  typ. 7  $\Omega$   
max. 10  $\Omega$

Transfer admittance

$I_D = 175\text{ mA}$ ;  $V_{DS} = 5\text{ V}$

$|Y_{fs}|$  typ. 150 mS

Input capacitance at  $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}$ ;  $V_{GS} = 0$

$C_{iss}$  typ. 15 pF  
max. 30 pF

Output capacitance at  $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}$ ;  $V_{GS} = 0$

$C_{oss}$  typ. 13 pF  
max. 20 pF

Feedback capacitance at  $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}$ ;  $V_{GS} = 0$

$C_{rss}$  typ. 3 pF  
max. 6 pF

Switching times (see Figs 2 and 3)

$I_D = 175\text{ mA}$ ;  $V_{DD} = 50\text{ V}$ ;  $V_{GS} = 0\text{ to }10\text{ V}$

$t_{on}$  typ. 4 ns  
max. 10 ns

$t_{off}$  typ. 4 ns  
max. 10 ns

N-channel enhancement mode vertical  
D-MOS transistor

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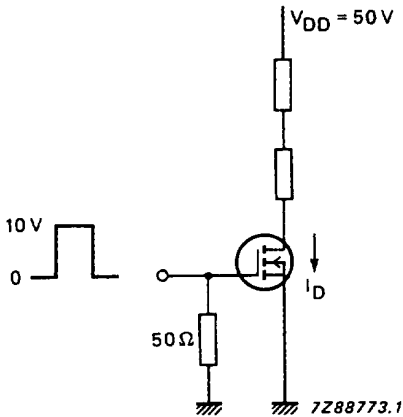


Fig.2 Switching times test circuit.

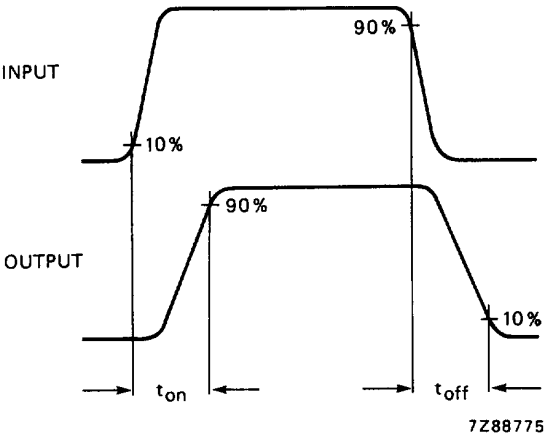


Fig.3 Input and output waveforms.

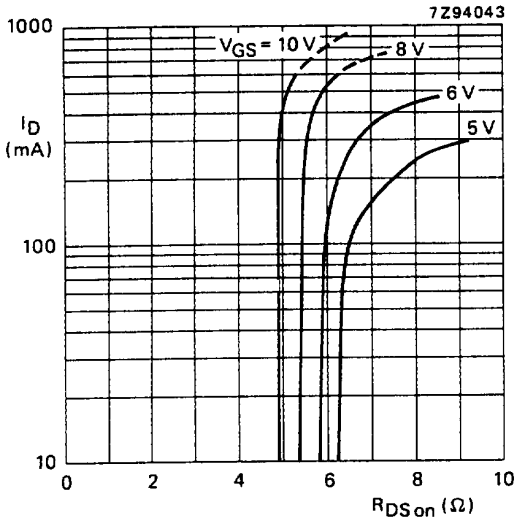


Fig.4  $T_j = 25\text{ }^{\circ}\text{C}$ ; typical values.

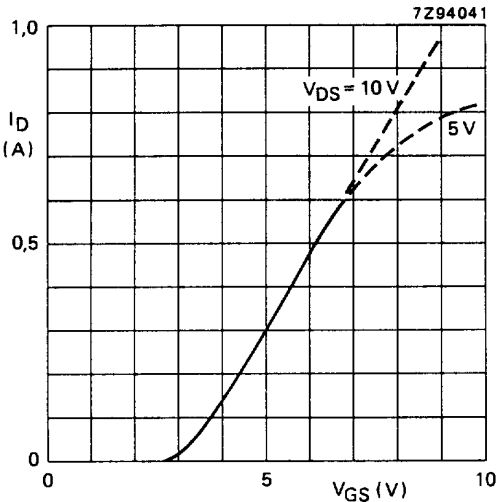


Fig.5  $T_j = 25\text{ }^{\circ}\text{C}$ ; typical values.

# N-channel enhancement mode vertical D-MOS transistor

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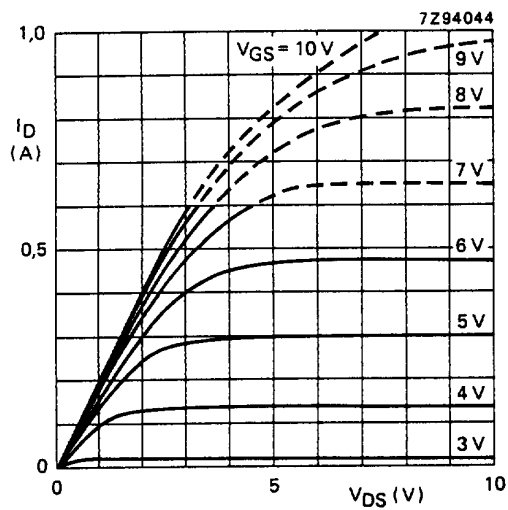
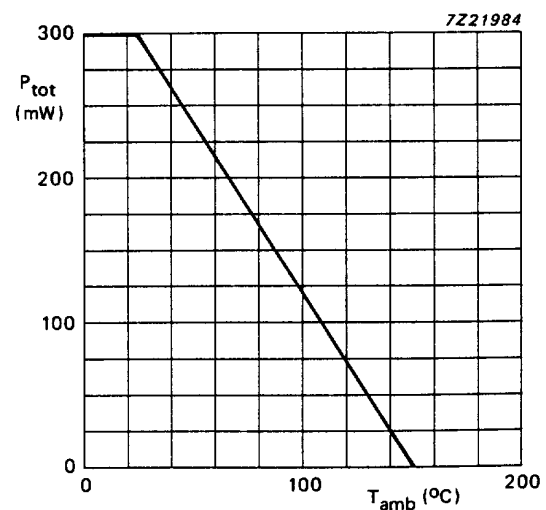
Fig.6  $T_j = 25\text{ }^{\circ}\text{C}$ ; typical values.

Fig.7 Power derating curve.

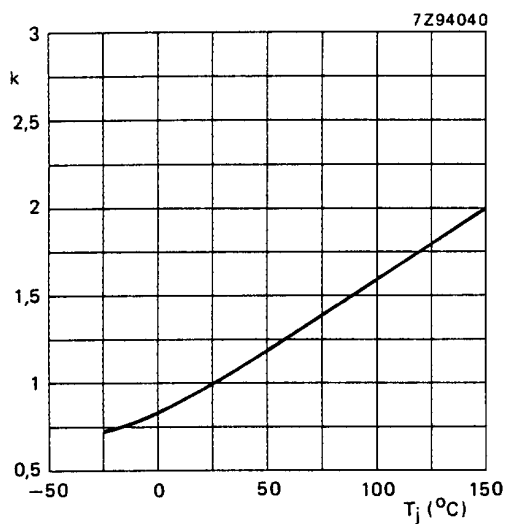


Fig.8

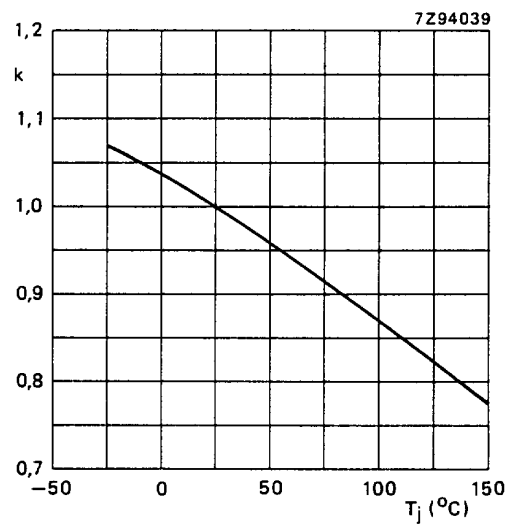


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\text{ }^{\circ}\text{C}}$$

$V_{GS(th)}$  at 1 mA; typical values.

# N-channel enhancement mode vertical D-MOS transistor

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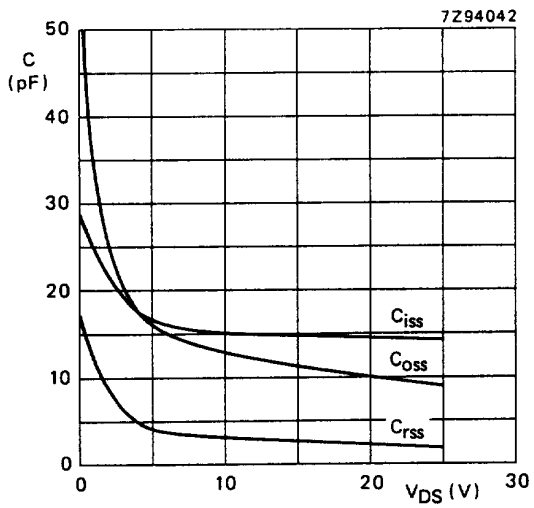


Fig.10  $T_j = 25\text{ }^{\circ}\text{C}$ ;  $V_{GS} = 0$ ;  $f = 1\text{ MHz}$ ; typical values.



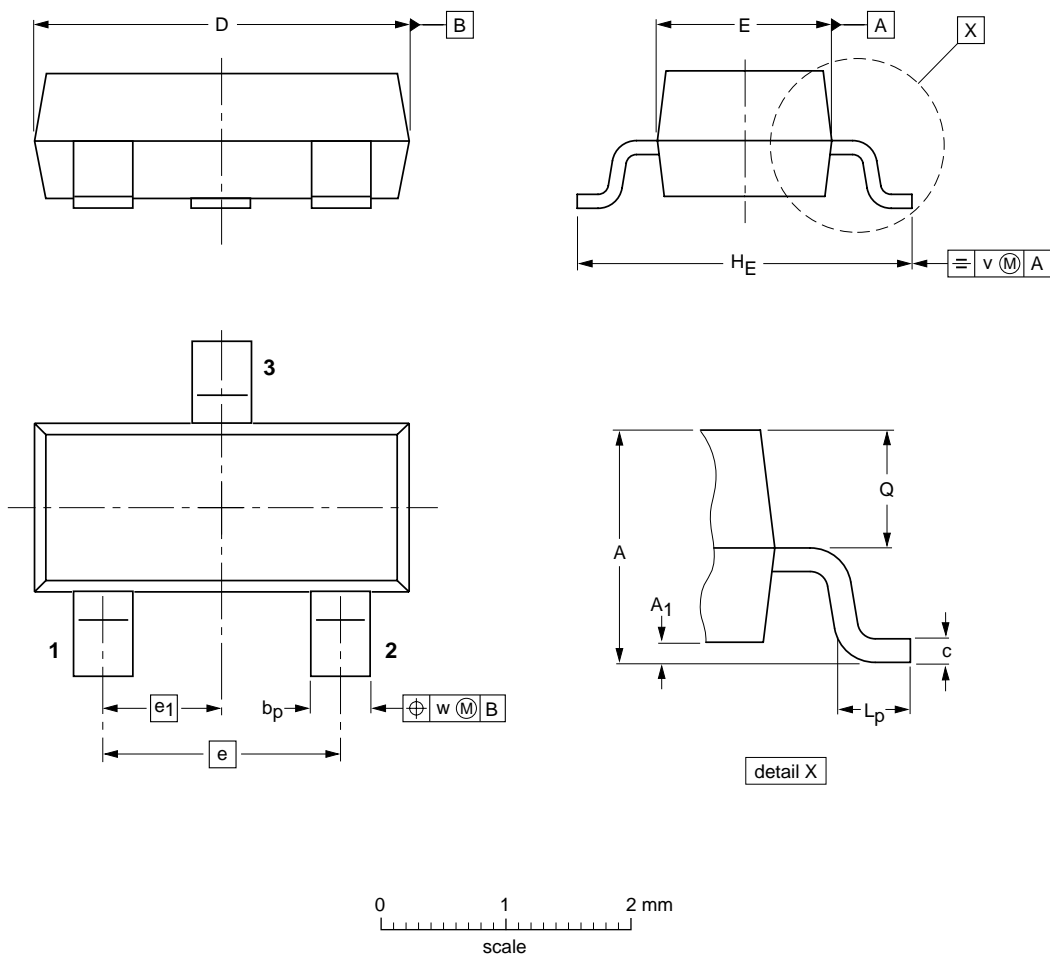
N-channel enhancement mode vertical  
D-MOS transistor

BST82

PACKAGE OUTLINES

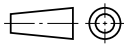
Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

| UNIT | A          | A <sub>1</sub><br>max. | b <sub>p</sub> | c            | D          | E          | e   | e <sub>1</sub> | H <sub>E</sub> | L <sub>p</sub> | Q            | v   | w   |
|------|------------|------------------------|----------------|--------------|------------|------------|-----|----------------|----------------|----------------|--------------|-----|-----|
| mm   | 1.1<br>0.9 | 0.1                    | 0.48<br>0.38   | 0.15<br>0.09 | 3.0<br>2.8 | 1.4<br>1.2 | 1.9 | 0.95           | 2.5<br>2.1     | 0.45<br>0.15   | 0.55<br>0.45 | 0.2 | 0.1 |

| OUTLINE<br>VERSION | REFERENCES |       |      |  | EUROPEAN<br>PROJECTION  | ISSUE DATE |
|--------------------|------------|-------|------|--|---|------------|
|                    | IEC        | JEDEC | EIAJ |  |   |            |
| SOT23              |            |       |      |  |  | 97-02-28   |

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# N-channel enhancement mode vertical D-MOS transistor

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**DEFINITIONS**

| Data sheet status   |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| Application information   |   |
| Where application information is given, it is advisory and does not form part of the specification. |   |

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NOTES

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