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Dynamic Bias for RF Class A Power Amplifiers

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Problem Description

Radio frequency power amplifiers are a major area of interest in the telecommunication filed. Increasing importance of wireless communications is pushing the requirements for power amplifiers. In particular high order linear modulations (for example 16/64/256 QAM), lead to a trade off between efficiency and linearity. A class A amplifiers can be used, but its efficiency is very low unless the bias point varies according to envelope of the RF input signal. This technique is called dynamic biasing.
A class A amplifier will be dynamically biased and its behavior evaluated first through powerful simulators as ADS and MATLAB. In particular a set of suitable bias points will be chosen and stationary and non stationary conditions analyzed. Finally, some laboratory measurements will be arranged and results compared.
Some other topics may be closely related: complex linear modulation systems, complex channel access methods, DC-RF isolation techniques, smart power supplies and linearization techniques.

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Supervisor: Morten Olavsbråten, IET

Dynamic Bias for RF Class A Power Amplifiers

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"The best way to make your dreams come true is to wake up."
— Paul Valery

Abstract

This thesis focuses on class A radio frequency power amplifiers in dynamic supply modulation architectures (dynamic bias). These are promising efficiency enhancement techniques where the device is driven harder by varying its bias signals. Non linearities that arise are considered as digitally compensated through, for example, digital predistortion (DPD). Bias signals are meant as functions of the PA's output power level ($Pout$). Therefore, the input power level (Pin) as well as the feeding signlas are thought as quantities the amplifier need to give a certain $Pout$. The selected set of bias points the device sweeps through is called bias trajectory or bias path.

A tool to find a suitable bias trajectory is developed considering the requirements a class A power amplifier should satisfy: high power added efficiency, acceptable gain and output phase variations as $Pout$ changes (allowing a DPD algorithm to be effective), low harmonic distortion and not too complicated bias signals patterns. The tool consists of two softwares: ADS and Matlab. ADS simulates the device under test while Matlab allows the user to analyze the data and find a suitable bias path. Once a trajectory is identified, ADS can sweep along it and give more information on linearity and efficiency through, for instance, 2-tone harmonic balance simulations. Note that only static characterstics are evaluated and memory effects disregarded.

The path seaching algorithm is then applied to a HBT transistor, at a frequency of $1.9GHz$ and to a complete pHEMT class A PA (frequency of $6Ghz$). In both cases a suitable trajectory is identified and analyzed back in ADS. The Matlab plots are qualitatively similar to each other when switching form one device to another. The HBT transistor has then been tested in the laboratory and static measurements have been performed showing good agreement with simulations.

Keywords: Bias trajectory, dynamic bias, efficiency, HBT, linearity, pHEMT, power amplifier

Contents

Chapter 1

Introduction

In telecommunications the power amplifier (PA) is usually the last amplifier of a transmission chain and converts the DC power given by an adequate supply into a signal carrying information. The signal should be strong enough to reach the receiver when transmitted through an antenna. A relevant parameter characterizing power amplifiers is efficiency, which describes how good is the power conversion process [1]. Another important aspect of PAs is linearity, which is often defined as the ability of the device to preserve the information content of the signal [1]. Usually linearity requirements contradict the efficiency requirement, leading to relevant trade-offs. For instance, PAs in general show high efficiency where the relation between input power and output power is non linear. If a power amplifier works in that region when an amplitude modulated signal is present at its input, the information content gets corrupted.

Different applications yield different efficiency specifications. For example, in wireless mobile devices (like cell phones) the PA's efficiency limits the battery or talk time, while in base-stations the relevant issues are energy costs and environmental impacts [2, 3]. In radio base-stations, the inefficient operation of the power amplifier heats up the system. Thus the generated heat has to be removed using, for example, cooling fans. This adds electrical expenses and increases the system complexity [4].

Efficiency requirements are also becoming more and more critical since the demand for high speed broadband communication services is increasing dramatically worldwide. Therefore more electrical energy is needed; energy that usually comes from not environmentally friendly sources such as fossil fuels. Estimations show that telecom industry consumed $164TWh$ in 2007 which is 1% of the global energy consumption [2]. This

clearly assesses the environmental impact of the energy consumption in telecom industry. In wireless networks, the radio base-stations (RBS) are the power hungriest parts, consuming more than 90% of the total energy [2]. Since the power amplifier's efficiency determines the RBS efficiency, it's improvement affects the overall system efficiency [4].

1.1 Linearity Requirements

In general, modulated signals used in modern wireless communications have wide bandwidth and high peak to average power ratio (PAPR). For instance, high order QAM modulations (256QAM or 128QAM), used in RBS to RBS links to achieve high channel capacities, have a PAPR of about $7 - 8dB$ (see Figure 1.1 and Figure 1.2, where some probability distribution functions, from matlab simulations, are shown) while an OFDM signal can easily have a PAPR of $10dB$. With these kind of modulations, power amplifiers linearty requirements become critical since any amplitude or phase distortion will cause loss of information worsening the Bit Error Rate and will give an unacceptable Adjacent Channel Power Ratio (ACPR). Therefore linear class A or AB power amplifiers should be used and operated at backed-off power levels. That leads to good linearity but usually very low efficiency [5].

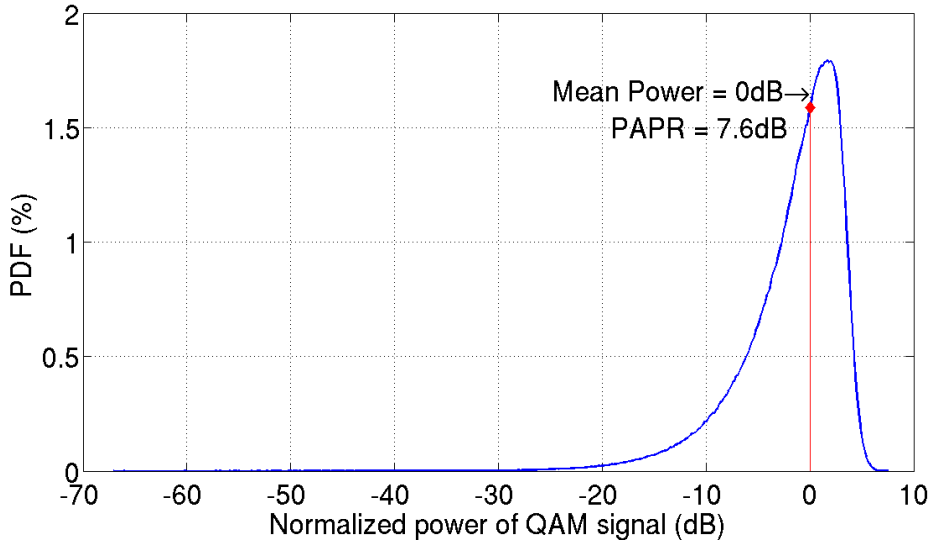

Figure 1.1: Probability Distribution Function of a 128-QAM modulated signal

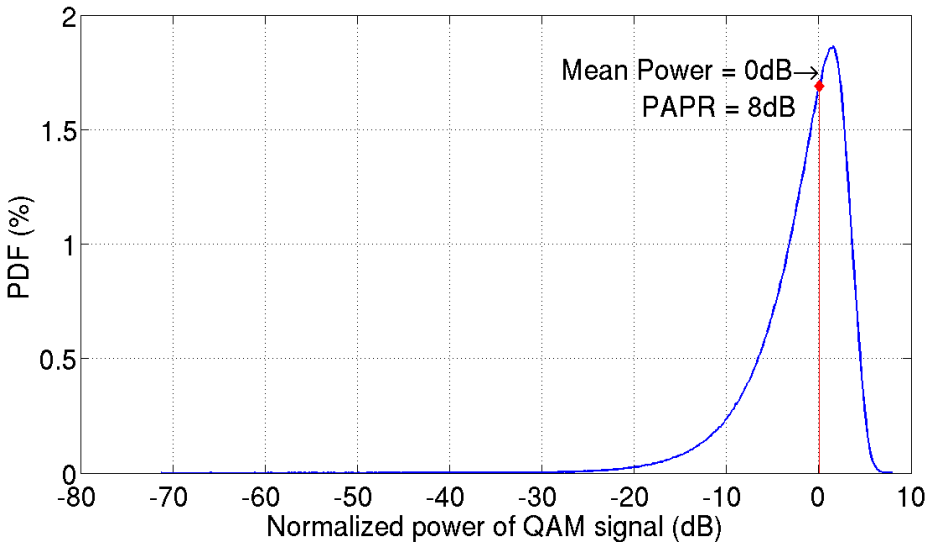

Figure 1.2: Probability Distribution Function of a 256-QAM modulated signal

1.2 Dynamic Biasing Techniques

To improve efficiency, one can act on the PA's bias voltages and vary them according to the envelope of the modulated signal at the input of the power amplifier (Figure 1.3). These techniques are generally called dynamic biasing.

Modulation techniques such as envelope elimination and restoration (EER) and envelope tracking (ET) are well known [6, 7, 8]. Both EER and ET dynamically supply an envelope signal to the drain of the RF amplifier as a bias signal. Thus, fast DC-DC converters are needed (bandwidth of more then ten times the bandwidth of the envelope if switching converters are used) and are actually the bottle neck of the system [9]. The dynamic bias switching (DBS) is another dynamic biasing technique [9, 10]. Feeding voltages are here discretized and the system switches through them according to the signal envelope level.

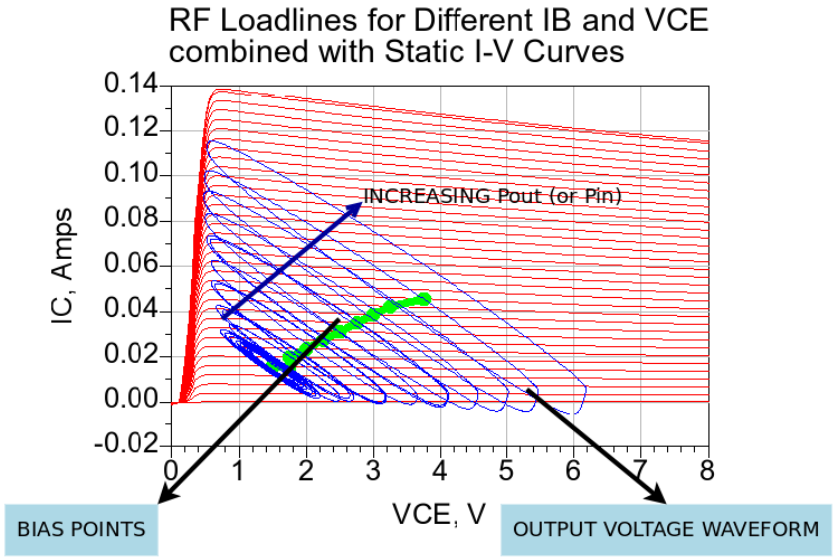

Figure 1.3: Bias points (green) and load lines (blue) of a dynamically biased class A power amplifier for a 1-tone sinusoidal input

1.3 Another point of view

Although all these techniques lead to higher efficiency and have different drawbacks, they all consider bias signals as functions of the input power level (Figure 1.4). Intuitively that sounds obvious but another idea has been proposed: treat the bias signals as functions of the output power level [11].

Generally speaking, a modern transmitter includes a modulator, raised cosine filters, mixers, adders and a power amplifier. Modulator's task is to send symbols and code them into some of the carrier's physical properties. In a QAM modulation system these are amplitude and phase. At the power amplifier's output, the symbol has to be as close as possible to what the modulator wants the device to transmit.

If a classic class A power amplifier with fixed bias voltages is used, its input power level is the only variable that defines the output power level at the fundamental frequency. That poses high requirements on amplifier's linearity as well as limits the device's efficiency dramatically.

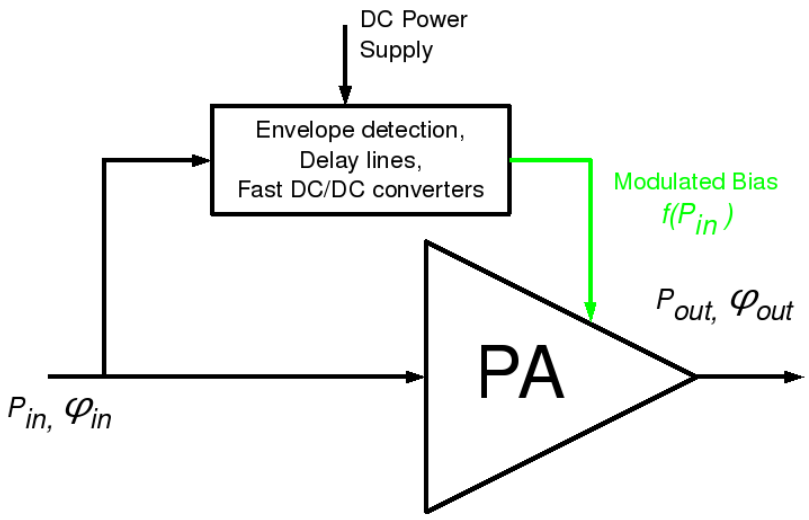

Figure 1.4: Modulated bias as function of the PA's input power level

If the PA is dynamically biased with feeding voltages and currents defined as functions of the input power level (through some envelope detectors and high speed DC/DC converters) then efficiency increases [6, 7, 8, 9, 10] but the amplifier may not be driven as hard as possible. These techniques need also much analog circuitry.

A different point of view is obtained if the modulator controls the bias signals. Then the modulator itself can act on the amplifier's input power level as well as on its bias voltages and currents to obtain the desired output, as shown in Figure 1.5. Thus, device's gain and output phase do not really need to be constant as output power changes and one can think of the input power level and bias signals as functions of the output power level [11]. In other words, given a certain output power level, what Pin, Vgs (Ib) and Vds (Vce) values are actually required to reach it? In practice, the modulator predistorts the signal's amplitude and phase compensating the PA non linear effects. Digital predistortion techniques should be used. For instance, a simple third order polynomial digital predistorter (DPD) can reduce the ACPR by a factor of 10dB [12].

This method, theoretically, allows the modulator to drive the power amplifier harder yielding much higher efficiency just by taking advantage of the enormous computational power of modern FPGAs and DSPs. For example, high PAE points can be chosen for different output power levels, although there are some drawbacks. First, there are other

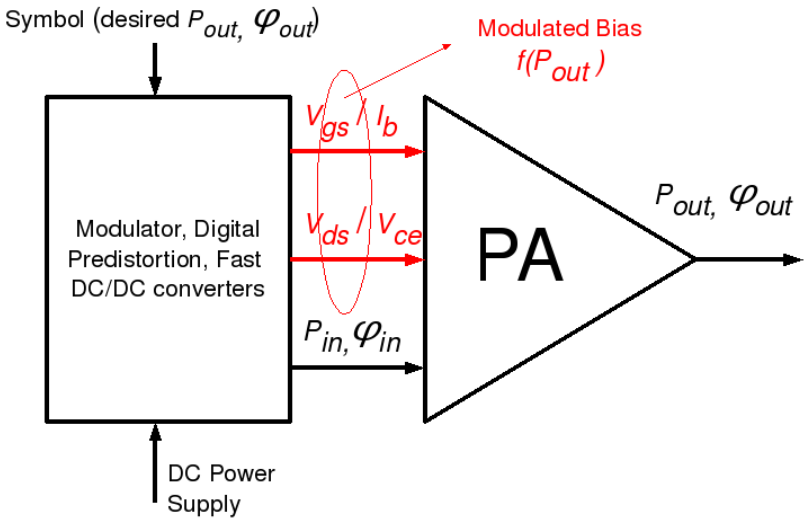

Figure 1.5: Modulated bias as function of the PA's output power level

amplifier's non linearities that produce harmonics especially where efficiency is high due to clipping and saturation effects. The third harmonic is particularly relevant since high third order distortion causes intermodulation products to arise when the input tone is not pure. Two additional elements worth of consideration are the two bias signals Vgs (Ib) and Vds (Vce) as functions of Pout. The (Vgs, Vds, Pin) points (when a FET is used) or (Ib, Vce, Pin) points (when a BJT is used) choices do not have to lead to complicated non linear functions since they would require high bandwidth feeding DC/DC converters, especially on the drain where the amount of current to control is high.

1.4 Bias Trajectory

So far, bias signals of class D, class E and class B power amplifiers have been considered as dynamically modulated through a function of the output power level and very high efficiencies have been reported (static measurements) [11]. Here, the same technique is applied to linear class A power amplifiers and both the gate (base) and drain (collector) bias signals are dynamically modulated making the analysis more complicated but leading to apparently linear and very efficient devices.

This thesis focuses on a dynamically biased class A RF power amplifier where both the bias signals vary as functions of the output power level (the modulator controls the DC supplies). For a FET amplifier:

$$V_{gs} = f(P_{out}) \tag{1.1}$$

$$V_{ds} = f(P_{out}) \tag{1.2}$$

A combined Agilent Advanced Design System (ADS) - Matlab tool to find a suitable bias trajectory (the selected bias points) has been developed. Some requirements the PA should satisfy have been taken in account: high power added efficiency, acceptable gain and output phase variations (as the output power changes), acceptable harmonic distortion and not too complicated bias signals patterns. Memory effects are not considered [13].

The tool has been applied to a complete $6GHz$ class A pHEMT power amplifier as well as to an unmatched HBT transistor (at the frequency of $1.9GHz$) giving in both cases a certain bias path the smart biasing system should follow. The HBT transistor has then been tested in the laboratory and static measurements have been performed showing good agreement with simulations.

Chapter 2

Simulation Procedure

The following chapter focuses on the operative procedure one should follow while using the tool described in this thesis (Figure 2.2). The ADS - Matlab interlink and and the data processing operations are explained. The important concept of the (Ib, Vce, Pin) space is also introduced (or (Vgs, Vds, Pin) space for a FET). Circuit analysis and the algorithm for the bias path identification are presented in Chapter 3.

2.1 ADS Environment

To find a suitable bias trajectory all the transistor's consistent bias points have to be considered and somehow evaluated. Here this is done through ADS one tone harmonic balance simulations. All the points are tested at different input power levels Pin (available power from the source) and signals analyzed up to a certain harmonic order. Consistent bias points are points where the transistor's ADS model is valid and the simulator's solver converges giving acceptable results. That means transistor's characteristics, performances and limits should be taken in account when setting up the bias signals sweeps as well as the Pin sweep. To guarantee convergence, a high order harmonic analysis is suggested (for instance, 31) and a Krylov solver is preferred. Keep in mind that in the simulation environment the source is matched and the amplifier's output is terminated for all the estimated harmonics.

Even if the sweep steps are not that narrow (for a HBT transistor: Ib step $30\mu A$, Vce step $0.25V$, Pin step $0.5dBm$) and ADS does not need much time to complete its task (20-30 minutes on an Ubuntu Linux PC with $3Gb$ of RAM and an Intel Dualcore

$2.53GHz$ processor), the amount of data the simulator produces is still huge ($500Mb - 1.5Gb$). In fact, it is big enough to make an analysis through the ADS graphic window impossible, and possibly troublesome for the operative system since too much memory is needed.Even if the graphic window opens, the system slows down dramatically.

Hence, data has to be analyzed in another way. In particular, Matlab, as a general purpose and very versatile simulation environment, can be used. In fact, a text file in the so called Generic MDIF format [14] is manually exported from ADS and read in Matlab (remember that complex numbers should be exported in the real/imaginary format). Matlab then picks up all the relevant information and calculates some parameters the same way ADS does.

2.2 From ADS to Matlab

In the following paragraphs the simulation procedure will be presented as being applied to a current driven HBT transistor. Thus, the bias signals will often be mentioned simply as Ib (base current) and Vce (collector to emitter voltage). The same procedure applies to voltage controlled FET transistors as well (simply, instead of Ib there is Vgs and instead of Vce there is Vds).

2.2.1 The mdif class and the (Ib, Vce, Pin) space concept

The reading and processing procedures in Matlab are integrated into a single step through a class called `mdif`, developed *ad hoc*. The core of the class are two private functions called `read_mdif_file` and `mdif2mat`. The first one roughly reads the MDIF file and has not been written here but taken from a free toolbox called Matlab Milou developed by Christian Fager and Kristoffer Andersson from Chalmers University of Technology.

The second one selects the data Matlab needs to analyze the microwaves circuit. Hence, this Matlab function is closely related to the ADS harmonic balance simulation template with swept input power level (from Design Guide, see [14]). As explained above, collector voltage and base current are swept as well. Given the ADS default set up, the following node names and current probe names should not be changed: **Vinput**, **Vload**, **Vs_high**, **Vs_low**, **Is_high** and **Is_low**. Finally, the DC current source on the

base has to be named **Ilow** (if a FET transistor is used then **Vlow**) and the DC voltage source on the collector should be called **Vhigh**.

The function `mdif2mat` returns a three dimensional Matlab `cell` variable and here the concept of the so called (Ib, Vce, Pin) space is introduced (Figure 2.1). The circuit has been analyzed at different (Ib, Vce, Pin) points through three sweeps: Ib, Vce and Pin. For each point, all the node voltages as well as all the probe currents have been estimated for different harmonic frequencies in regime conditions (that is what a harmonic balance simulation does). Hence, one can consider voltages and currents as functions of the (Ib, Vce, Pin) point, yielding the idea of the (Ib, Vce, Pin) space. In other words, given a (Ib, Vce, Pin) point, a certain voltage or current is measured for different frequencies that are multiple of the fundamental and stored in an array where the index is the harmonic number.

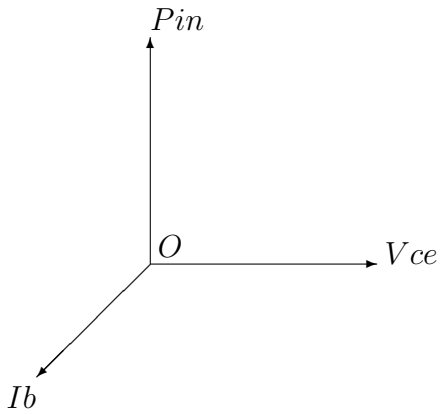

Figure 2.1: The (Ib, Vce, Pin) space

The three dimensional cell is then nothing but a discretized (Ib, Vce, Pin) space where each unit is a certain (Ib, Vce, Pin) point and contains all the relevant voltages and currents as arrays.

2.2.2 The mdif class methods

After all the necessary voltages, currents and other parameters have been read from the MDIF file and stored in the three dimensional `cell` variable, the `mdif` object can be created. As any other class, the `mdif` class has some basic required methods, listed in Table 2.1.

The class constructor `mdif` takes the MDIF file name as an input argument and calls the private function `mdif2mat` to read it. Then, the `cell` variable is returned together with the following arrays: the Ib sweep range, the Vce sweep range, the Pin sweep range and `f`, the harmonic frequencies. All of them then combine into a `mdif` object.

The `mdif` object can be thought as a Matlab rappresentation of the device under test since it contains all the important data.

Class method name	Description
`mdif`	`mdif` class object constructor
`subsasgn`	Overloads the subsasgn operator
`subsref`	Overloads the subsref operator
`display`	Displays the contents of a `mdif` object

Table 2.1: Required class methods

Now, for every single (Ib, Vce, Pin) point some parameters are calculated:

- Power added efficiency (PAE)
- Overall efficiency (OAE)
- Transducer power gain
- Output phase
- Output power, fundamental
- Output power, first harmonic
- Output power, third harmonic

This is accomplished by a set of class methods described in Table 2.2. Each of them calculates a certain parameter for every (Ib, Vce, Pin) point in the space, returning a matrix. The parmeter is then nothing but a scalar function of the (Ib, Vce, Pin) point.

All these methods perform exactly the same calculations ADS does. Hence, a complete analysis of the PA in Matlab is then possible. Some formulas are given below to make sure the meaning of some very important parameters is well understood.

Power added efficiency:

$$PAE_{\%} = 100\frac{Pout_W - Pin_W}{Pdc_W} \tag{2.1}$$

Overall efficiency:

$$OAE_{\%} = 100\frac{Pout_W}{Pdc_W + Pin_W} \tag{2.2}$$

Where $Pout_W$ is the output power at the fundamental frequency in Watts, Pin_W is the available power from the source in Watts and Pdc_W is the DC power delivered by the power supply. Although signals at the power supply nodes may have harmonics, Pdc_W considers always only DC currents and voltages.

Transducer power gain:

$$G_{dB} = Pout_{dBm} - Pin_{dBm} \tag{2.3}$$

Where $Pout_{dBm}$ is the output power at the fundamental frequency in dBm and Pin_{dBm} is the available power from the source in dBm.

The methods ending with `_mesh` return matrices with flipped coordinates: (Vce, Ib, Pin) instead of (Ib, Vce, Pin). Therefore, Matlab 3D plot functions can be used to rappresent graphically how the parameters listed above vary in the (Ib, Vce, Pin) space.

In fact, since the MDIF file carries a lot of data, the `mdif` object occupies a lot of memory as well. That means it takes time to save and load it as a `mat` file whenever needed, which might be annoying when data analysis is performed and variables loaded and cleared all the time. Therefore, all the relevant matrices should be calculated once, saved and then recalled. A `mat` file containing all the quantities described before does not occupy more then 4-5Mb and can be easily handled by Matlab, speeding up the simulations.

Class method name	Description
`PAE`	Power added efficiency (%)
`PAE_mesh`	Power added efficiency in meshgrid format (%)
`OAE`	Overall efficiency per each point (%)
`OAE_mesh`	Overall efficiency in meshgrid format (%)
`P_gain_transducer`	Transducer power gain per each point (dB)
`P_gain_transducer_mesh`	Transducer power gain in meshgrid format (dB)
`phase`	Output phase at the fund. frequency (deg)
`phase_mesh`	Output phase at the fund. frequency in meshgrid format (deg)
`Pout_fund_W`	Output power, fundamental (W)
`Pout_fund_W_mesh`	Output power, fundamental, in meshgrid format (W)
`Pout_second_W`	Output power, second harmonic (W)
`Pout_second_W_mesh`	Output power, second harmonic, in meshgrid format (W)
`Pout_third_W`	Output power, third harmonic (W)
`Pout_third_W_mesh`	Output power, third harmonic, in meshgrid format (W)

Table 2.2: Relevant class methods

The script in Appendix A shows how to use the `mdif` class to transfer data from ADS to Matlab, process them and save all the matrices in a compact `mat` file.

2.2.3 Exporting the I-V plane

To represent the bias points in the transistor's I-V plane in Matlab, the device's output characteristics should be exported from ADS as well. Then, another MDIF text file is saved in ADS after a simple DC simulation template has been run (from Design Guide, see [14]). A Matlab script called `v_i_dc.m` then reads the file and saves the transistor's I-V plane in a `mat` file. The program does not need any particular classes, only the function `read_mdif_file` is required (see Section 2.2.1) and some attention is needed when selecting variable names.

2.3 Matlab Environment

After importing and processing data from ADS the analysis has to be performed and a suitable path identified. The analysis is executed through the following tools:

`slices_vs_contours.m`, plots PAE, OAE, transducer power gain, output phase, output power at the fundamental freq., output second harmonic and output third harmonic as 3D slices in the (Ib, Vce, Pin) space. This is far the most important and powerful analyzing tool.

`Pout_fund_vs_PAE.m`, plots output power (fundamental freq.) contours and PAE contours in the Vce, Pin plane for each Ib value.

`outPhase_vs_Pout.m`, plots output phase contours and output power (fundamental freq.) contours in the Vce, Pin plane for each Ib value.

Then, to find a bias trajectory the script `path_seek.m` should be first correctly set up and then started. If a path is successfully found, the program will plot and save some data. If an error occurs or the trajectory is not good enough, then the user should modify the script set up or even go back to the ADS one tone harmonic balance simulation (`path_seek.m` gives some smart error codes, suggesting what the user should modify).

2.4 Back to ADS

If a bias trajectory is identified, then the tool `path_seek.m` automatically saves its (Ib, Vce, Pin) coordinates into a discrete format text file (`.dscr`, see [14]). This can be read back in ADS.

This allows ADS to sweep along the path according to its (Ib, Vce, Pin) points when simulating the device. In particular, the following tools have been created:

Stability, tests the stability of the amplifier for every single point of the trajectory.

Two tones harmonic balance simulation, analyzes the amplifier's linearity and measures its intermodulation products as it moves along the path.

One tone harmonic balance simulation, cross checks ADS and Matlab data

Dynamic load line analysis, a one tone harmonic balance simulation that plots the dynamic load line and the bias point of the transistor in the I-V plane as the amplifier moves along the path. Shows, qualitatively, how the transistor works and distorts the signal.

If the results from this further simulations are satisfying, then a suitable trajectory has been found. If they are not, then the user should search for another one or even restart from the ADS one tone harmonic balance simulations.

The complete simulation procedure is described in the flowchart of Figure 2.2.

2.5 Simulation and Data Analysis

A link has been established between ADS and Matlab through two text files. Matlab's main job is data analysis. Matlab lets the user analyze the ADS data through some three dimensional plots and finds a suitable bias trajectory, while ADS simulates the circuit (Chapter 3). Therefore, the amplifier's model and the simulations in ADS play a major role in the developed tool. This separation of tasks should be well understood, since if there is something wrong in ADS the problem will certainly appear later in Matlab or on the field.

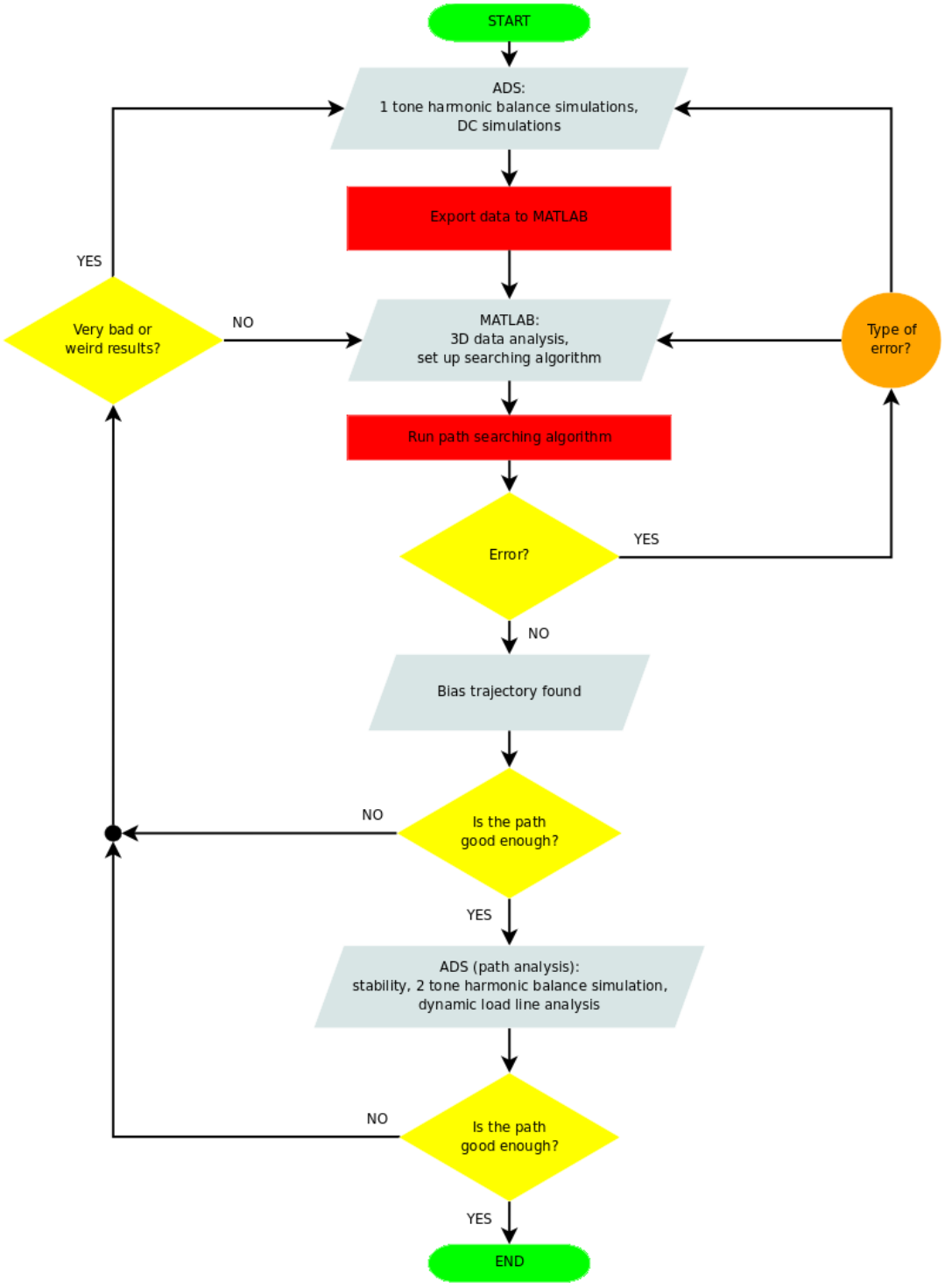

Figure 2.2: Simulation Procedure Flowchart

Chapter 3

Circuit Analysis and Searching Algorithm

As explained in Chapter 2, different amplifier's bias points are assessed in ADS through harmonic balance simulations. Three variables are swept: Ib (Vgs with a FET), Vce (Vds with a FET) and Pin (available power from the source). The resulting amount of data is actually too large for the ADS graphic window to handle it. Thus, rough data are transferred to Matlab. They consist of circuit node voltages and circuit branch currents at frequencies that are multiple of the fundamental per each (Ib, Vce, Pin) point. Matlab reads the data and calculates the following parameters for every point of the (Ib, Vce, Pin) space: output power level $Pout$, PAE, OAE, output phase, transducer gain, second harmonic power and third harmonic power.

Now, all these quantities have to be analyzed, the searching algorithm set up and then run. This part explains how a three dimensional analysis of the circuit in the (Ib, Vce, Pin) space can be performed and how that affects the searching algorithm. Finally a detailed description of the algorithm is given.

3.1 Circuit Analysis

All the quantities listed above come as matrices and can be thought of as scalar functions of the (Ib, Vce, Pin) point. Therefore they can be plotted in Matlab using 3D slice graphics with contours (Chapter 2). Slices show very well how the amplifier under test behaves at different bias points and input power levels Pin.

In addition, $Pout$ contours, output phase contours and PAE contours can be plotted in the Vce, Pin plane for certain Ib values. Basically, the (Ib, Vce, Pin) space can be sliced along the Ib axis and the slice analyzed separately.

The presented analysis is a novel idea within the RF power amplifier design technieques and may be also used for applications different than dynamic bias systems, leading to new developements in the field.

3.1.1 Slice Plots

Some 3D plots from a HBT transistor are shown and qualitatively analyzed. Three major regions of interest can be easily identified:

Linear class A region, where gain as well as output phase are almost constant and $Pout$ contours are perpendicular to the Pin axis and equally spaced (Figure 3.3 and Figure 3.4). Here the relation between Pin and $Pout$ is linear, the phase difference between input and output is constant, the harmonic distortion is neglectable for lower input power levels (Figure 3.5 and Figure 3.6), but the efficiency is very low (Figure 3.2). In the I-V plane this area corresponds to the active region of the device (Figure 3.1).

Deep class AB, class B region, here gain and phase are not that constant anymore and $Pout$ contours start to bend upwards (Figure 3.3 and Figure 3.4). Then, the relation between Pin and $Pout$ may not be that linear and the difference between input and output phase could show some variations and some harmonic distortion may occur even with lower Pin levels (Figure 3.5 and Figure 3.6). But now the power added efficiency is much higher (Figure 3.2). The device, in this case, is biased with a very low Ib current (or Vgs voltage) as shown in Figure 3.1.

Switching region, here the device works as a switch. The PAE is extremely high for high Pin levels (Figure 3.2), but the relation between Pin and $Pout$ is far from being linear, gain is not constant at all and the output phase varies a lot (see Figure 3.3 and Figure 3.4). Finally, the harmonic distortion is very high. This very efficient area is used in harmonic-tuned switching power amplifiers [1]. They are usually used with fixed power level modulations (for instance, FSK). The transistor, here, works on the knee of its output characteristics (Figure 3.1), with very low Vce voltages (or Vds).

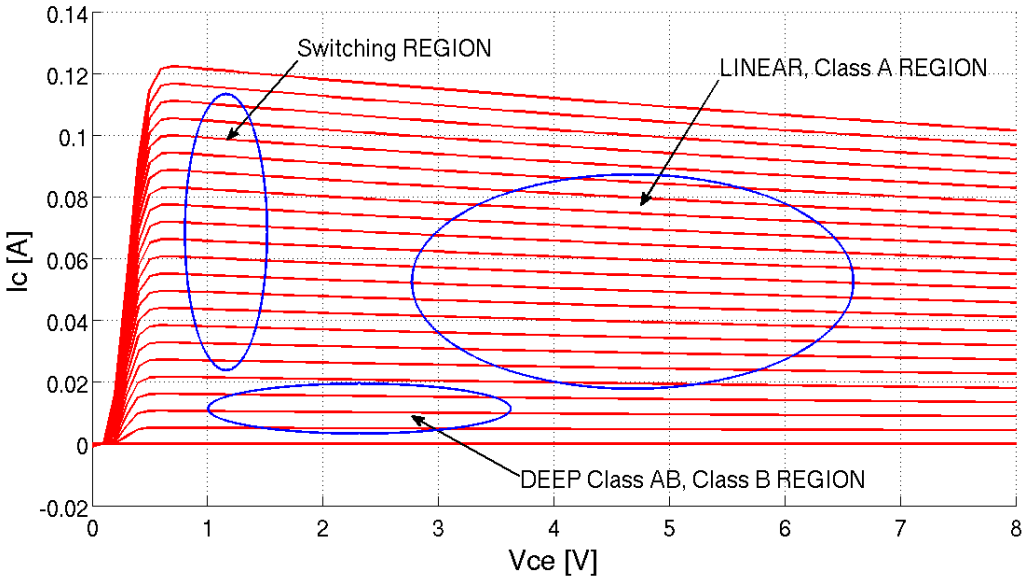

Figure 3.1: Regions in transistor's I-V plane

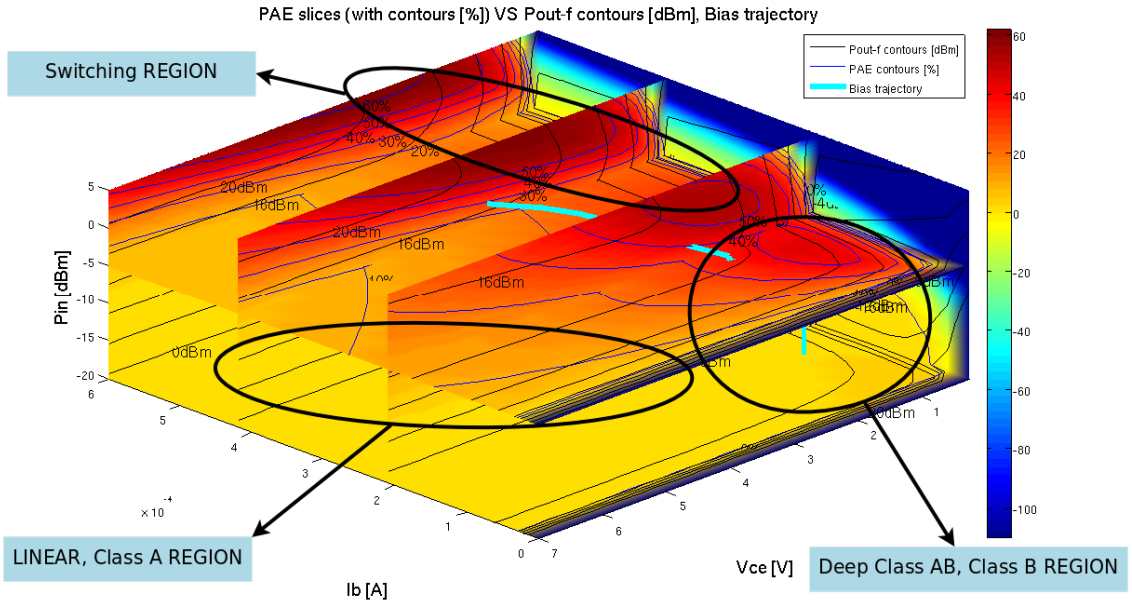

Figure 3.2: PAE slices with contours *vs Pout* countours, notice the bias trajectory

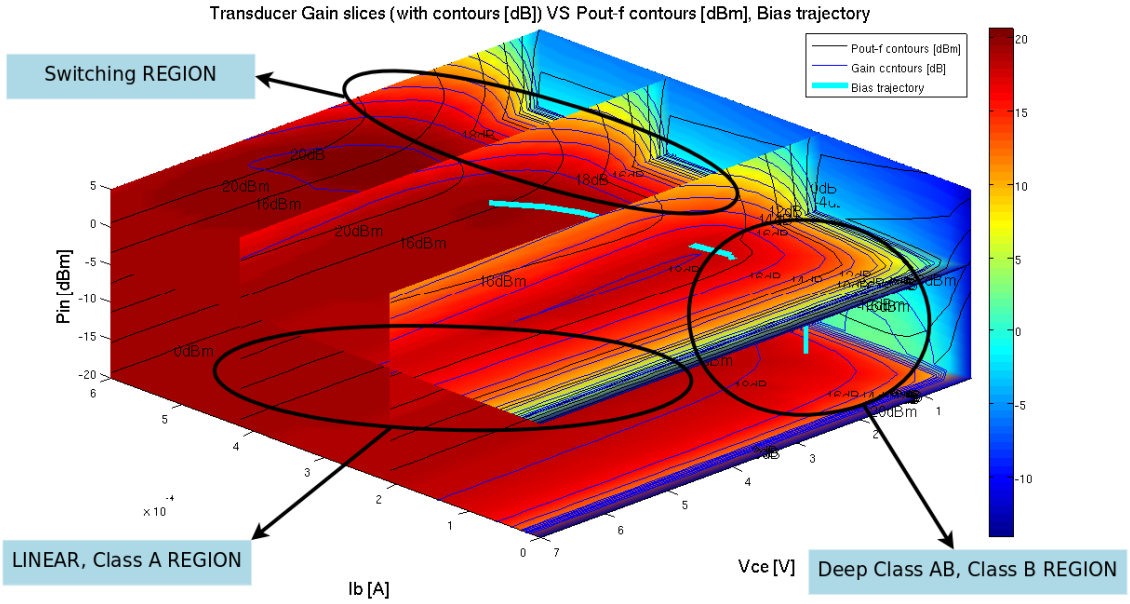

Figure 3.3: Transducer Gain slices with contours *vs Pout* countours, notice the bias trajectory

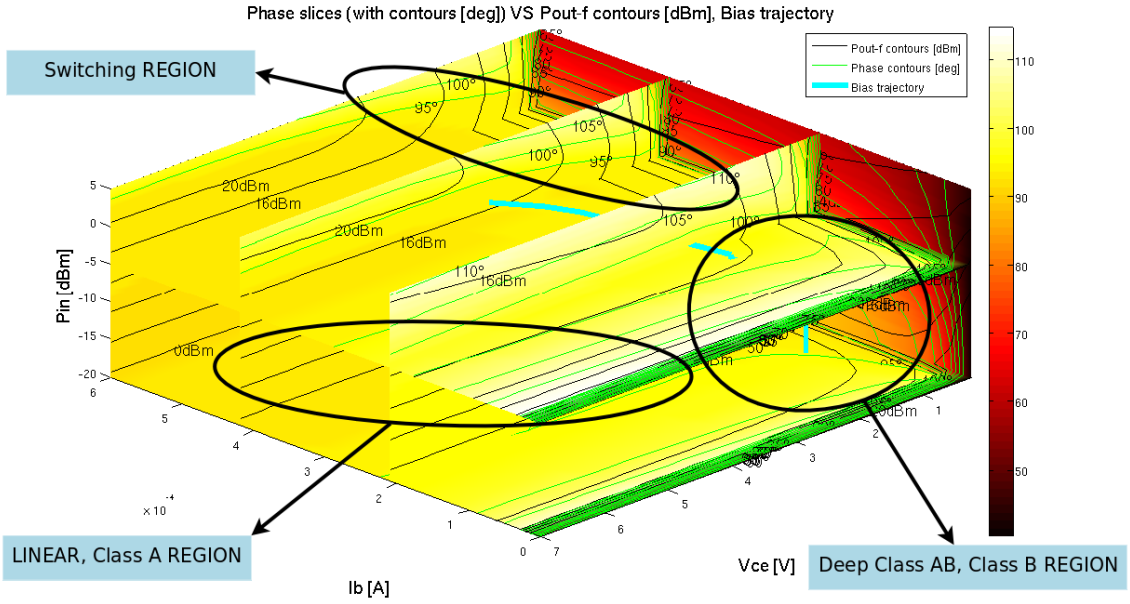

Figure 3.4: Output Phase slices with contours *vs Pout* countours, notice the bias trajectory

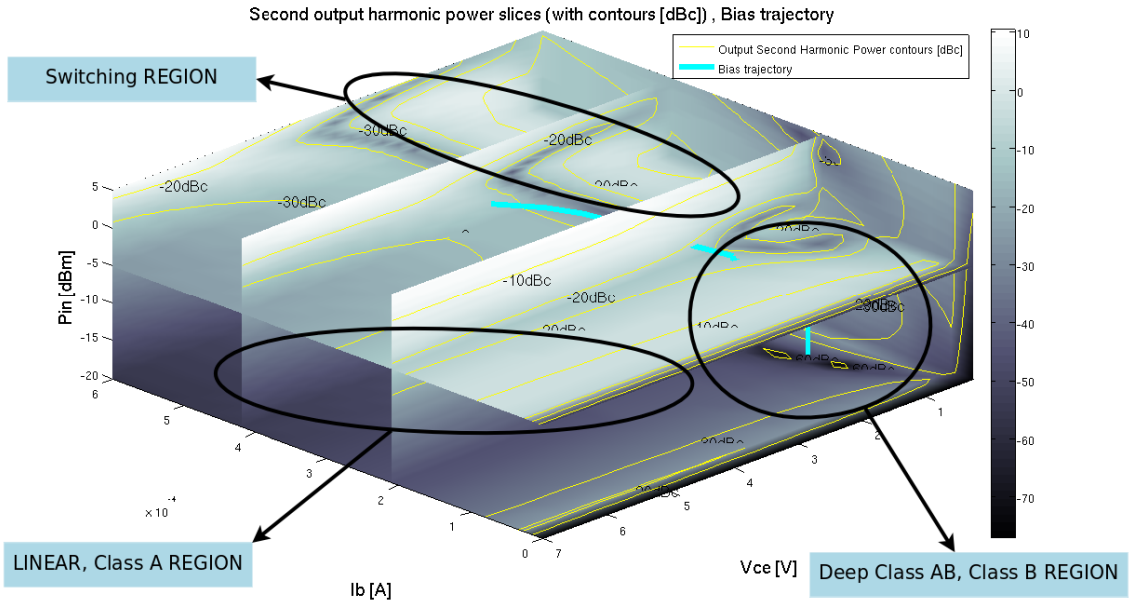

Figure 3.5: Second Harmonic slices with contours

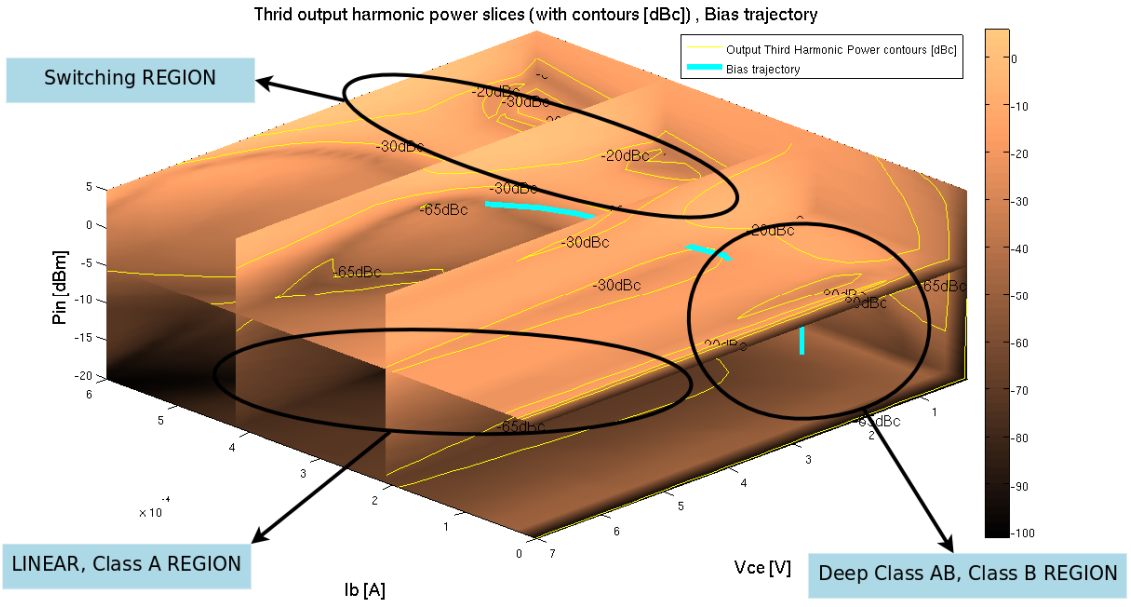

Figure 3.6: Third Harmonic Slices with contours

3.1.2 Analyzing slices

Although the main purpose of dynamic biasing is to increase the efficiency of a class A amplifier, linearity has to be considered as well. Linearity is somehow synonymous of the name *Class A* itself and suggests that an acceptable bias trajectory should not cross the switching region as well as the Class B region for high Pin levels. The path could start for example in the Class B region where efficiency is higher and linearity good for low input power levels. Then, as Pin increases, it should move toward the linear Class A region, staying as close as possible to the very efficient switching zone (see the cyan trajectory in the slice figures). As close as possible means close enough not to get high harmonic distortion.

Since the algorithm's performance depends a lot on the start point selection (point having the lowest $Pout$), its constraints should be set properly. In fact the algorithm seeks for high-efficiency, low harmonic distortion points and tries to keep output phase and gain as flat as possible. Therefore, the starting point gain and phase play a major role since their values will define which power gain and which output phase the software will try to follow. In order to guarantee acceptable linearity, they should be close, if not the same, to the gain and output phase the amplifier exhibits in its linear region. Hence, a linear and efficient area has to be identified and then the searching script will automatically choose the point having the highest PAE within it. For instance, that could be the Class B region (for low input powers).

The gain and the output phase the transistor has in its linear region can be found out through slice plots. Another Matlab tool allows the user to cut the (Ib, Vce, Pin) space for a certain Ib and plot the output phase contours as well as the PAE contours on the resulting Vce, Pin plane. The output phase the device exhibits in its linear region can be easily read out from these diagrams (Figure 3.7 and Figure 3.9). Figure 3.8 and Figure 3.10 show how PAE varies for the same Ib currents. All the plots come from a HBT transistor.

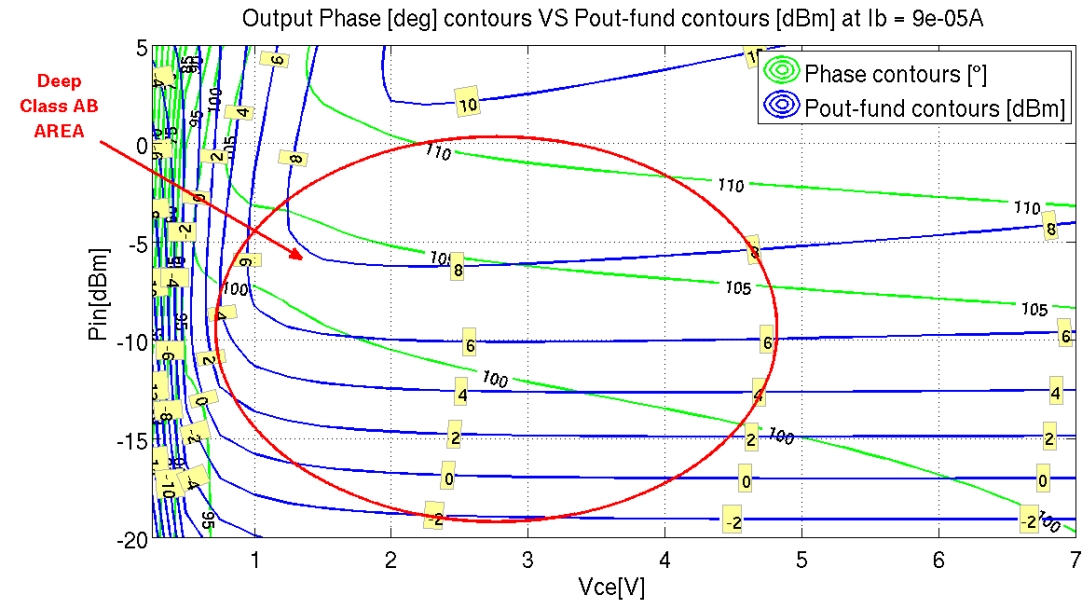

Figure 3.7: Low *Ib* slice with *Pout* and Output Phase contours (notice the Class AB region)

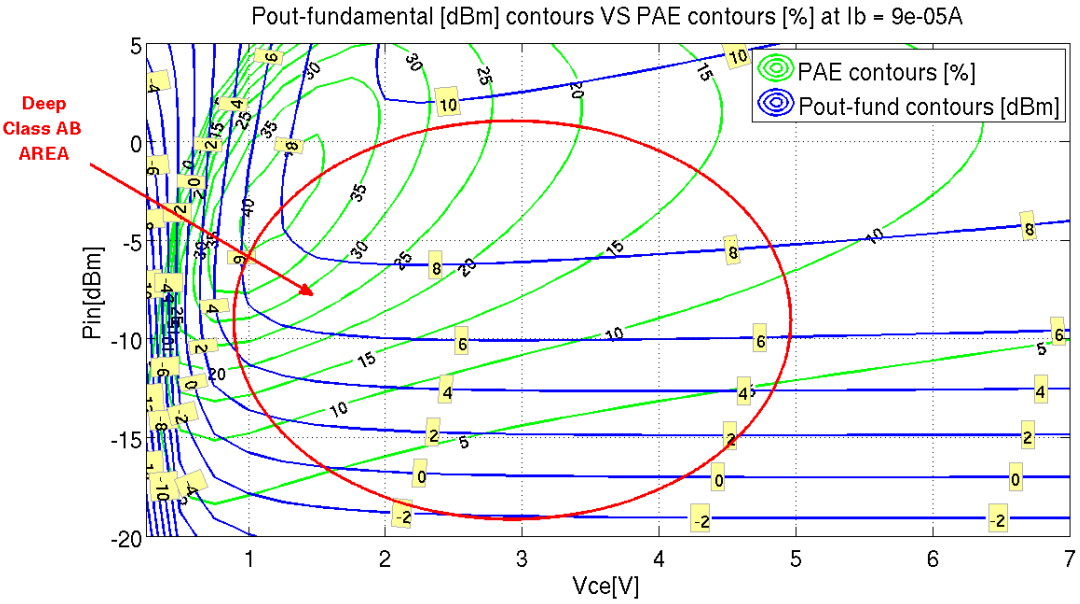

Figure 3.8: Low *Ib* slice with *Pout* and PAE contours (notice the Class AB region)

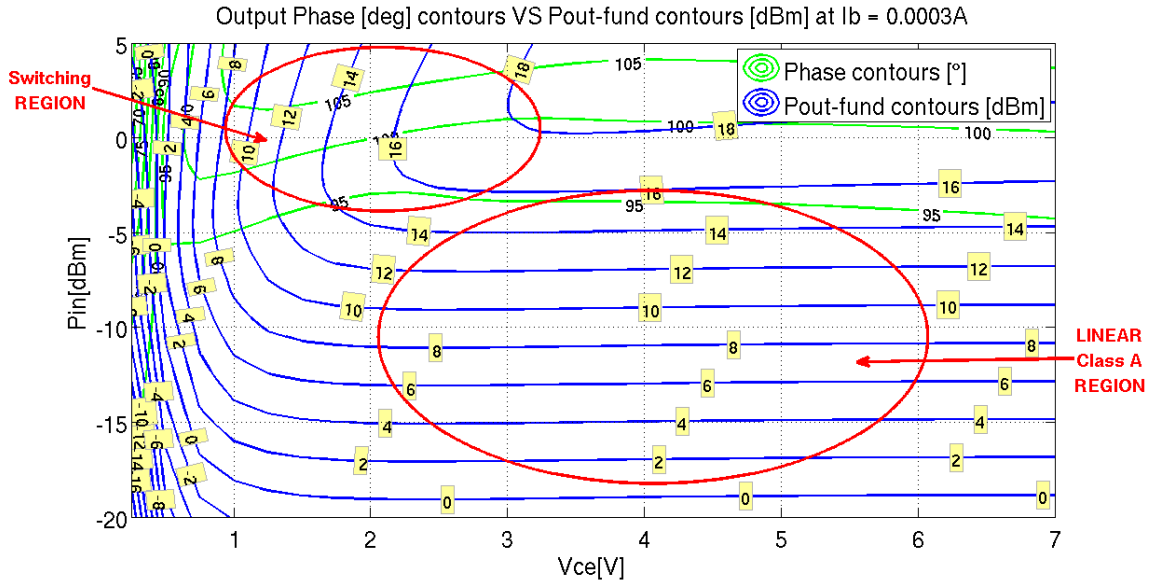

Figure 3.9: High *Ib* slice with *Pout* and Output Phase contours (notice the Class A region and the switching region)

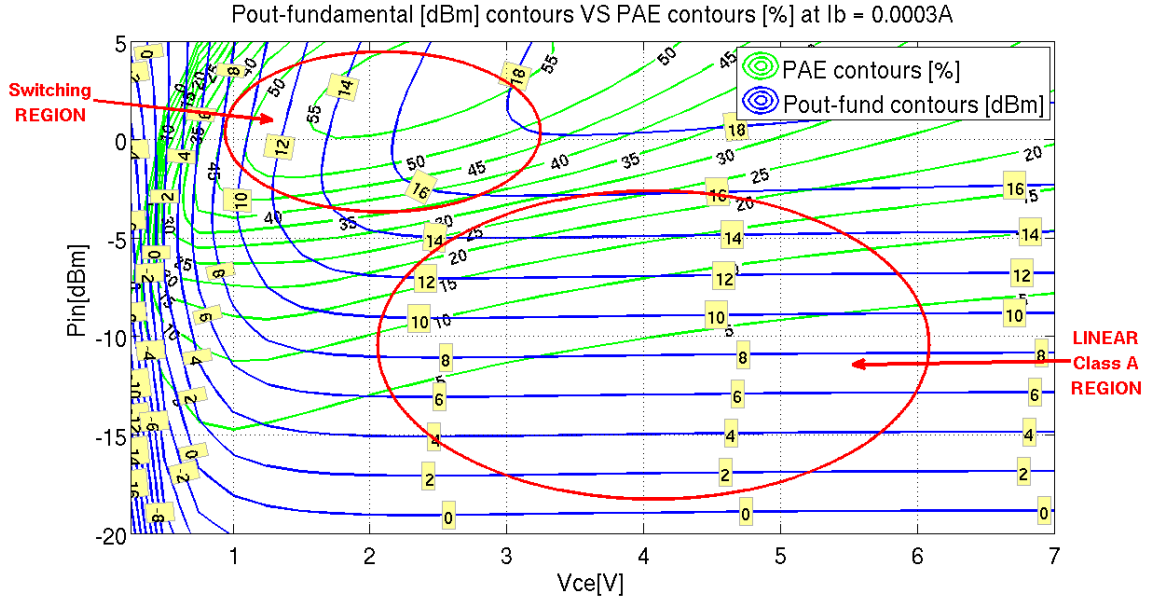

Figure 3.10: High *Ib* slice with *Pout* and PAE contours (notice the Class A region and the switching region)

3.2 Searching Algorithm

As explained in Chapter 1 different bias points have to be selected for different output power levels, defining a bias trajectory (bias signals as functions of $Pout$). The algorithm developed in Matlab (file `path_seek.m`) should be first correctly set up and then run. An iterative procedure then leads the user to an acceptable bias path (see Figure 2.2). During the explanation the algorithm is considered as applied to a HBT amplifier (it works the same way with any other FET amplifier).

The steps the script follows are shown in the flowchart of Figure 3.11. In the following paragraphs each of them is presented.

3.2.1 Constraints

First, the software has some constraints the user should define. They are listed below, although a detailed explanation is given step by step as the algorithm is presented.

Output power range (dBm), the algorithm will try to find a bias path for the user defined output power range

Global Ib and Vce constraints, points having lower or higher Ib and Vce are not considered and automatically discarded. These constraints can be used not to let the transistor reach troublesome saturation or breakdown regions.

Start point constraints, constraints the user can act on to make the algorithm find a suitable starting point within a certain region. The area should be identified through some slice plots analysis (Section 3.2.3).

Ω cost function weights, weights of the coefficients that combine into the Ω function. The user can leverage on them to give parameters more ore less importance in the overall cost function (for example give more weight to the factor associated with the third harmonic).

(Ib, Vce, Pin) space distance normalization coefficients , the algorithm uses a normalized (Ib, Vce, Pin) distance where the normalization coefficients are user defined.

Class A bias point, a normal class A bias point has to be chosen. This allows the user to compare the performances of a dynamically biased amplifier to those of a classic one.

3.2.2 Sorting 3D Points

At the beginning, the script sorts the (Ib, Vce, Pin) points according to their output power levels, forming the so called $Pout$ groups. For the HBT, power levels from $0dBm$ to $20dBm$ with a step of $1dB$, have been considered. The first group contains points that give between $-0.5dBm$ and $0.5dBm$ of power, the second one contains those that give between $0.5dBm$ and $1.5dBm$ of power and so on. Points with output power levels between $19.5dBm$ and $20.5dBm$ are in the last output power group. The program will later select one point per each group and thus find a suitable bias path for the amplifier.

Note that if the power range step is too narrow compared to that one used in the ADS one tone harmonic balance simulation at the beginning, no points could be found for a certain $Pout$ group. If that happens, an error occurs and the user should modify the step. As a rule of thumb, a step two times larger or of the same size as the Pin step in ADS should be used.

The output power range can be given, as in the case of an already designed amplifier one wants to apply the dynamic bias technique on, or could be a part of the problem, as in the case of a simple transistor experiment. In the second case, a reasonable $Pout$ range can be found through ADS one tone harmonic balance simulations and Matlab slice analysis.

As a cross check, once a path has been found, the user should make sure that, at peak, when the highest output power is delivered, the collector/drain current does not exceed twice the maximum static limit and the collector/drain voltage does not reach the break down region. The ADS tool that plots the dynamic load line in the I-V plane as the amplifier moves along the trajectory makes this analysis possible Section 2.4.

While sorting points in terms of their output power levels, those with Ib or Vce higher than than the global Ib and Vce constraints are discarded (see Section 3.2.1). That is because high base currents lead to saturation phenomena while too high collector voltages may push the transistor into the breakdown region. Therefore, one should carefully check the device's physical characteristics and set the limits correctly.

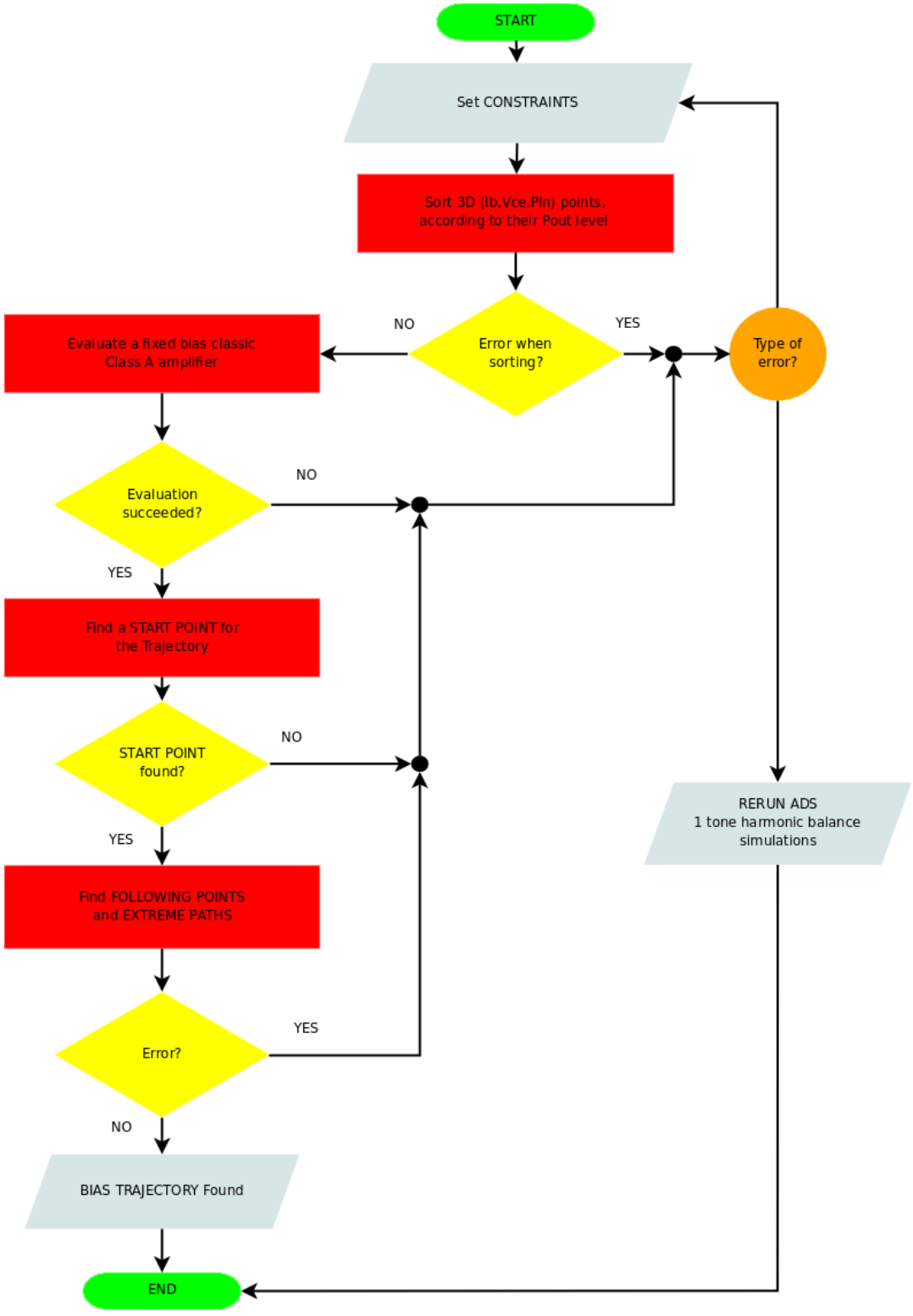

Figure 3.11: Steps the script `path_seek.m` follows

3.2.3 Start Point

Afterwards, the program seeks for a start point within the first output power group. The steps listed below are followed in sequence and the start point constraints are applied.

1. A square in the Ib, Vce plane is defined and forces the algorithm to choose a start point within its limits. In this way, the user can precisely control where the trajectory should start from (see Section 3.1.2).

2. Points with transducer gain lower than a certain value are discarded. Since the algorithm later tries to keep the gain as flat as possible along the path, this limit should be close to the minimum gain the amplifier exhibits in its linear region (see Section 3.1.2).

3. Points with output phase out of a user defined range are discarded. Later, when searching for a path, the program tries to keep the output phase as flat as possible, thus this range should not differ too much from the phase the amplifier's output has in its linear region (see Section 3.1.2).

4. Points having second harmonic power level and third harmonic power level higher than certain limits are discarded. These are linearity constraints that make sure the algorithm chooses a linear enough point depending on the application.

5. Finally, among the points left (if any), the one having the highest power added efficiency is chosen.

If constraints are too strict, then no points within the first *Pout* group may satisfy them. Hence, when that happens an error occurs and the user should ease the start point selection criteria.

3.2.4 Following Points of the Path

Once the first point has been set, the following ones are chosen through a more complicated procedure. The software proceeds sequentially, considering one output power group at a time in ascending order.

Given the current step n, the algorithm considers the point selected the step before $(n-1)$ and excludes, among the current group n, all the points having lower bias signals (Ib and Vce) as well as lower available powers from the source (Pin). This makes Ib and Vce not too complicated functions of $Pout$ (easing requirements for DC/DC converters without sacrifying much of the amplifier's performance) and guarantees a monotonic $Pin - Pout$ relation.

If no points satisfy these monotonicity criteria, then an error occurs. This may happen because, given a certain $Pout$ group, nothing guarantees that among its points there are some having higher Ib,Vce and Pin then the point selected the step before (usually there are, but in some cases there may not be any). The user should then ease the constraints (like increasing the Ib and Vce global limits of not forcing one variable among Ib, Vce and Pin to be monotonic) or rerun the complete ADS one tone harmonic balance simulation from the beginning and set wider Ib,Vce or Pin sweeps.

If no errors have occurred, then all of the M points left are suitable candidates. Then, M different trajectories are evaluated. Each of them has, as its last nth-step point, one among the M left ones, while all the others (steps $1, \ldots, n-1$ are the points the algorithm has selected before. Therefore, all the M trajectories differ only in their nth-step point. Six parameters have been introduced to evaluate these paths and choose the most suitable one. For each of the M paths the following coefficients are calculated:

$\boldsymbol{\alpha}$, average power added efficiency ($PAE_{\%}$), (%)

$$\alpha = -\frac{1}{n}\sum_{i=1}^{n} PAE_{\%,i} \tag{3.1}$$

$\boldsymbol{\beta}$, transducer gain (G_{dB}) flatness index, (dB)

$$\beta = \sum_{i=2}^{n} \left| G_{dB,i} - G_{dB,i-1} \right| \tag{3.2}$$

$\boldsymbol{\gamma}$, output phase (φ_{deg}) flatness index, (deg)

$$\gamma = \sum_{i=2}^{n} \left| \varphi_{deg,i} - \varphi_{deg,i-1} \right| \tag{3.3}$$

$\boldsymbol{\delta}$, average second harmonic output power (SH_{dBc}), (dBc)

$$\delta = \frac{1}{n} \sum_{i=1}^{n} SH_{dBc,i} \tag{3.4}$$

$\boldsymbol{\epsilon}$, average third harmonic output power (TH_{dBc}) (dBc)

$$\epsilon = \frac{1}{n} \sum_{i=1}^{n} TH_{dBc,i} \tag{3.5}$$

dist, normalized distance between current point and previous one in the (Ib, Vce, Pin) space

$$dist = \sqrt{\left(\frac{Ib_n - Ib_{n-1}}{Ib_{NORM}}\right)^2 + \left(\frac{Vce_n - Vce_{n-1}}{Vce_{NORM}}\right)^2 + \left(\frac{Pin_n - Pin_{n-1}}{Pin_{NORM}}\right)^2} \tag{3.6}$$

where n is the current step, $n-1$ is the previous one and i is the step index $(i = 1, \ldots, n)$.

Each evaluated path has its own parameters. Therefore, $\alpha, \beta, \gamma, \delta, \epsilon$ and $dist$ are actually arrays with their indexes identifying a certain path.

The arrays are then normalized to their absolute maxima and, point by point, linearly combined into a cost function called $\mathbf{\Omega}$:

$$\Omega = w_\alpha \alpha_{norm} + w_\beta \beta_{norm} + w_\gamma \gamma_{norm} + w_\delta \delta_{norm} + w_\epsilon \epsilon_{norm} + w_d dist_{norm} \tag{3.7}$$

with

$$w_\alpha + w_\beta + w_\gamma + w_\delta + w_\epsilon + w_d = 1 \tag{3.8}$$

Ω is an array as well, thus each path has its own Ω coefficient.

Finally, the path having the lowest Ω parameter is chosen, its point from the current output power group (n) selected for the final path and the algorithm moves on until a complete path is identified. This path is called the tuned trajectory. The flowchart of the algorithm is presented in Figure 3.12.

Normalization is necessary to give all the parameters the same importance. Then, the weighted sum makes some parameters more relevant and others less relevant, depending on what kind of tuned path the software should seek for. For example w_α defines how much PAE should count, w_β defines how much gain flatness should be considered, w_γ sets phase flatness importance and so on.

The minus sign in the α parameter formula (3.1) simply turns the maximization problem into a minimization one.

The distance parameter *dist* has been introduced not to have abrupt jumps in the final trajectory and therefore obtain a more continuous curve in the (Ib, Vce, Pin) space. The distance dependency on each of the three coordinates can be set through appropriate normalization coefficients. If one variable has not to vary too much while moving from one trajectory point to the next one, then it should be weighted more, giving a higher distance.

Hence, the searching criteria can be modified through the following parameters yielding different trajectories:

$\boldsymbol{w_\alpha}$**:** Power added efficiency weight

$\boldsymbol{w_\beta}$**:** Gain flatness weight

$\boldsymbol{w_\gamma}$**:** Output phase flatness weight

$\boldsymbol{w_\delta}$**:** Second harmonic output power weight

$\boldsymbol{w_\epsilon}$**:** Third harmonic output power weight

$\boldsymbol{w_d}$**:** Distance weight

As explained above, the distance normalization coefficients can be tuned as well:

$\boldsymbol{Ib_{NORM}}$**:** Ib normalization coefficient

$\boldsymbol{Vce_{NORM}}$**:** Vce normalization coefficient

$\boldsymbol{Pin_{NORM}}$**:** Pin normalization coefficient

There is no rule on how to set all the coefficients described before and the user can even not consider (3.8). But if (3.8) is followed, then one knows exactly how much each parameter counts in the final cost function (3.7).

As a rule of thumb, one could start with the coefficients listed in Table 3.1.

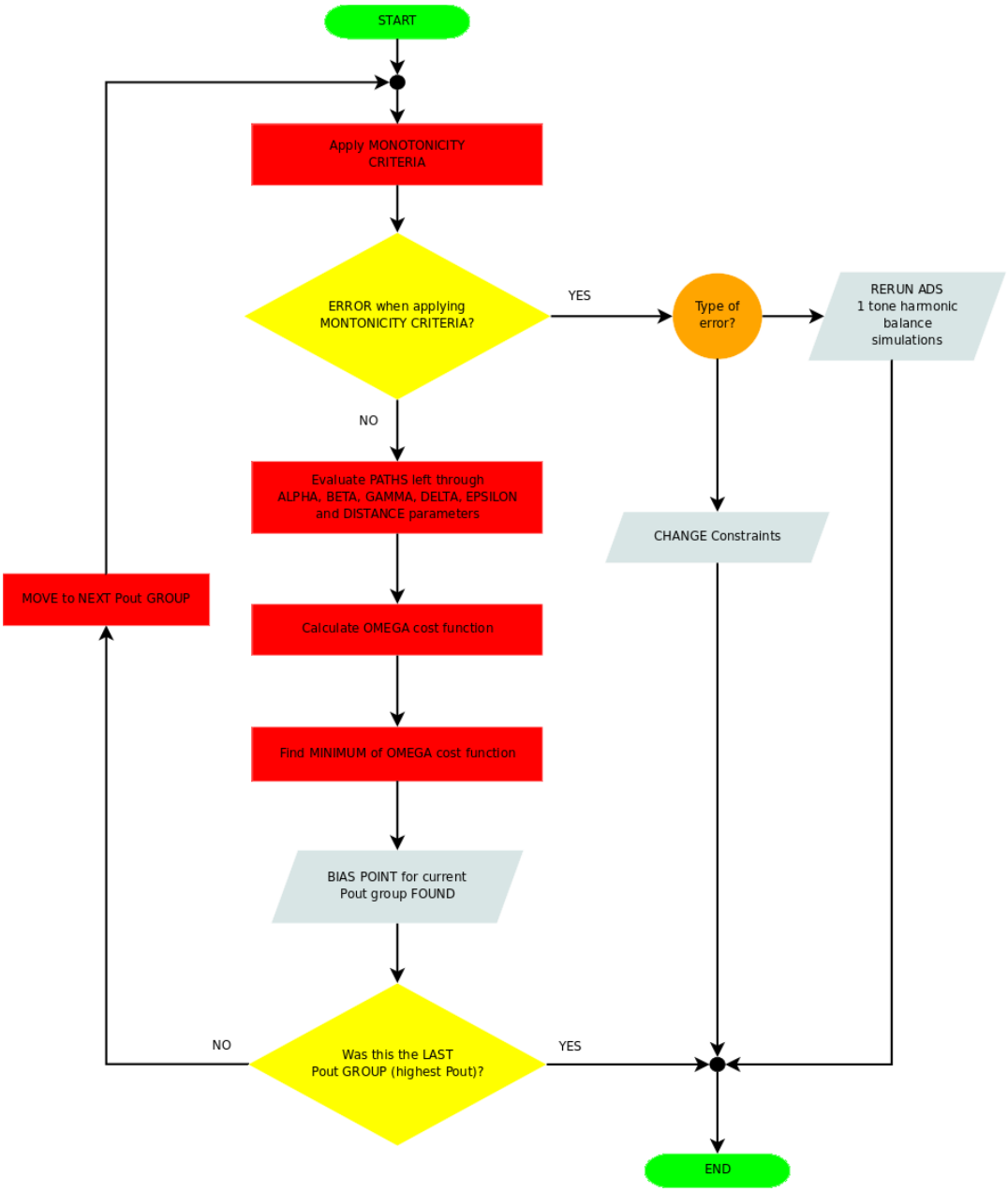

Figure 3.12: Algorithm Flowchart

Coefficient	Suggested initial value
w_α	1/6
w_β	1/6
w_γ	1/6
w_δ	1/6
w_ϵ	1/6
w_d	1/6
Ib_{NORM}	$max(Ib)$, from ADS sweep
Vce_{NORM}	$max(Vce)$, from ADS sweep
Pin_{NORM}	$max(Pin)$, from ADS sweep

Table 3.1: Suggested initial coefficients

3.2.5 Extreme paths

To help the user while varying the weights and the normalization coefficients introduced in Section 3.2.4, the scripts searches for some other paths. They are called the extreme paths since they are optimized for only one of the following parameters: $\alpha, \beta, \gamma, \delta$ and ϵ. These trajectories are found the same way the tuned one is (Section 3.2.4) and have the same starting point, but the cost function to minimize contains only one of the parameters listed before. Is the same as having the Ω cost function (3.7) with all the weights set to 0, but only one to 1 (w_d must be 0, always). Therefore, the script finds the following extreme paths:

Maximum PAE, Path optimized for highest power added efficiency, minimum α (3.1)

Best gain flatness, Path optimized for gain flatness, minimum β (3.2)

Best phase flatness, Path optimized for phase flatness, minimum γ (3.3)

Minimum second harmonic, Path optimized for minimum second harmonic distortion, minimum δ (3.4)

Minimum third harmonic, Path optimized for minimum third harmonic distortion, minimum ϵ (3.5)

All these trajectories rappresent the best performances the algorithm can reach when optimizing only one parameter ($\alpha, \beta, \gamma, \delta$ and ϵ), given a certain set up. The tuned

trajectory is somehow a way in between the extremes and the user can act on the coefficients introduced in Section 3.2.4 to move the tuned path closer or farther to some optimized trajectories, thus enhancing some of its characteristics and sacrifying others. If the results are not good enough, then the set up should be changed or even the ADS simulation rerun from the beginning.

If the algorithm cannot find one of these trajectories for the reason explained at the beginning of Section 3.2.4, an error occurs.

3.2.6 Class A path

Finally, a classic class A amplifier is considered. Once a suitable fixed bias point is selected, the program estimates the amplifier's performances along the output power range defined in Section 3.2.1. This allows the user to compare a classic class A amplifier with a dynamically biased one.

If all output power levels within the selected range cannot be reached with the chosen bias point, then an error occurs and the point has to be changed (once more, slice plots should be used as guidelines).

3.3 Interaction with the user

The tool interacts with the user through the Matlab command window and some powerful plots where all the relevant quantities of the tuned path as well as of the extreme paths and the class A one are presented (for instance, PAE along the path as function of $Pout$, transducer gain along the path as function of $Pout$, $Pin - Pout$ plots...). In this way, the user can compare the tuned trajectory performances with all the others and then modify the coefficients. All the figures shown in Section 3.1.1 and Section 3.1.2 are presented again and explained in Chapter 4 where the tool is applied to a HBT transistor.

Chapter 4

Dynamically biased HBT transistor

A single HBT transistor has been selected as a test device for the algorithm described in Chapter 3. Single InGaP HBT devices are available at the Microwave Laboratory of the Department of Electronics and Telecommunications (NTNU). They are integrated on GaAs microwave microchips that include some calibration features like shorts, opens and known length lines (see Figure 6.2 and Figure 6.3). Therefore, it is possible to simulate an amplifier, analyze it, find a suitable trajectory and then test it in the laboratory.

This chapter describes the simulations as well as the analysis performed on the HBT. A bias trajectory is found and analyzed back in ADS. Measurements are discussed and commented in Chapter 6.

4.1 The HBT transistor

The heterojunction bipolar transistor (HBT) is an improvement of the bipolar junction transistor (BJT) and, as the name suggests, employs an emitter-base heterojunction [15]. The use of a heterojunction increases the common-emitter current gain and reduces the injection of holes from the base to the emitter dramatically. Therefore, the base can be very thin and heavily doped while maintaining high emitter efficiency and high current gain. A thin base region reduces the transit time and increases the cutoff frequency [15].

Hence, HBTs can handle signals of very high frequencies, up to several hundred GHz [16]. Modern ultrafast circuits, mostly high power RF systems (power amplifiers) make large use of HBTs.

The selected device is an InGaP emitter HBT (GaAs substrate) from TriQuint Semiconductor foundry (see Figure 4.1).

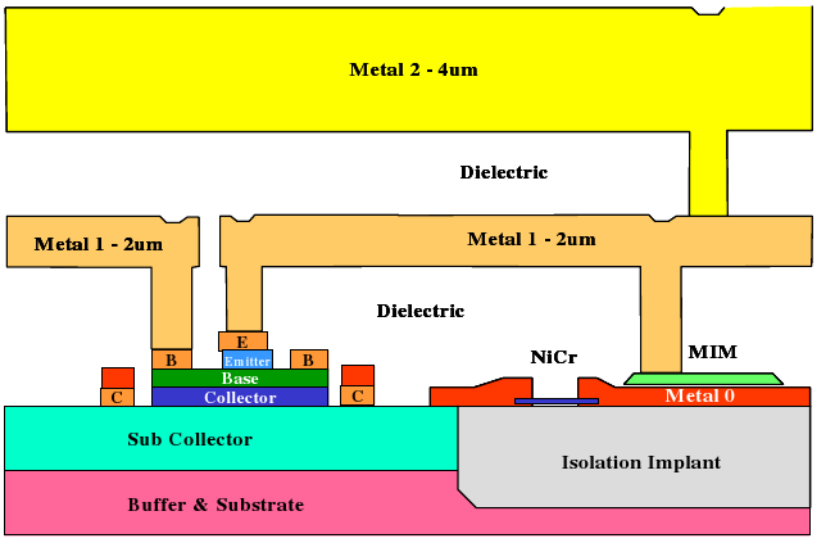

Figure 4.1: TriQuint's TQHBT3 process cross section [17]

Among the available devices the largest three fingers single HBT has been selected. There are some other bigger transistors made of multiple HBTs in parallel but they have been discarded to keep the test device as simple as possible, therefore avoiding model problems as well as possible layout inconveniences.

The emitter of the transistor under test has three $3\mu m$ wide (w_{FINGER}) and $50\mu m$ long (l_{FINGER}) fingers. The selected working frequency is $1.9GHz$. At this frequency some relevant device characteristics are given in [17] although there the fingers are shorter ($l_{\text{FINGER}} = 30\mu m$). Some maximum ratings are listed in Table 4.1.

Description	Parameter	Value	Unit
Junction Current Density	J_{max}	20	kA/cm^2
Breakdown C-B voltage, open emitter	BV_{cbo}	24	V
Breakdown B-E voltage, open collector	BV_{beo}	7	V
Breakdown C-E voltage, open base	BV_{ceo}	14	V

Table 4.1: TriQuint HBT Maximum Ratings, [17]

The device's emitter area is:

$$A_{\mathrm{E}} = n_{\mathrm{FINGERS}} \cdot w_{\mathrm{FINGER}} \cdot l_{\mathrm{FINGER}} \tag{4.1}$$

The maximum DC junction current is:

$$I_{max} = A_{\mathrm{E}} \cdot J_{max} \tag{4.2}$$

Given the HBT under test, according to (4.1) and (4.2) the DC emitter (collector) current should not exceed $90mA$. At peak, the same current can reach at maximum twice I_{max}, that is $180mA$.

The tested amplifier has no matching networks as well as no stabilization circuits (see Figure 4.2). This makes the transistor unmatched as well as potentially unstable. Therefore, stability has to be checked after a bias trajectory is found. On the other hand, the circuit is very simple and can be easily tested in the laboratory with two bias tees to feed the device.

As a bipolar, the HBT is current driven. Hence, a constant current source is used to bias the transistor on the base.

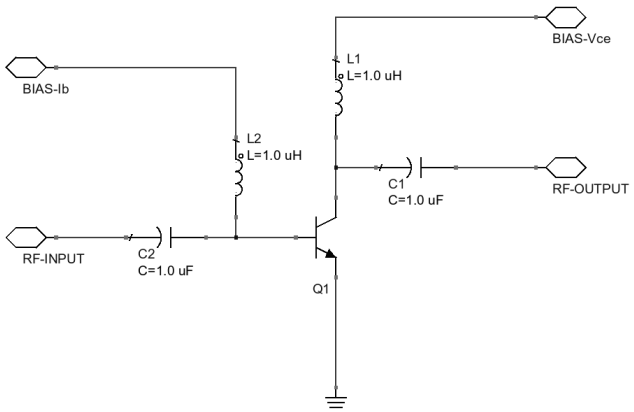

Figure 4.2: Test HBT Amplifier

4.2 ADS One Tone Harmonic Balance Simulation

As explained in Chapter 2 and Chapter 3, a one tone harmonic balance simulation is first run and the variables Ib, Vce and Pin swept. In this way the amplifier is evaluated in a discretized region of the (Ib, Vce, Pin) space.

For the HBT transistor the following sweeps are defined:

***Ib* sweep:** from 0 to $600\mu A$ with a step of $30\mu A$. According to [17] the device's current gain β is 130; then with the upper Ib limit of $600\mu A$ the resulting Ic is $78mA$, which is under the limit of $90mA$ (see Section 4.1).

***Vce* sweep:** from $0.25V$ to $7V$ with a step of $0.25V$. The upper limit of $7V$ is half the collector-emitter breakdown voltage with open base, $14V$ (see Table 4.1).

***Pin* sweep:** from $-20dBm$ to $5dBm$ with a step of $0.5dB$. This range has been selected since it is used in [17]. In fact, it has been noticed that with higher Pin ($7-8dBm$) the ADS solver doesn't converge (probably breakdown effects lead the solver to two or more solutions).

In Figure 4.3 the ADS simulation set up is shown.

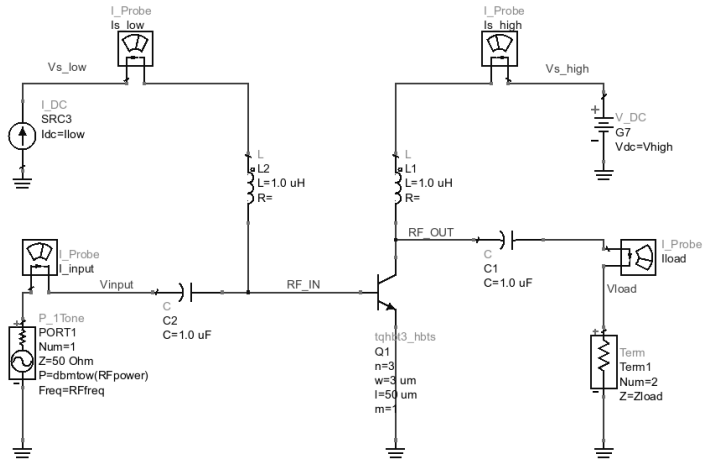

Figure 4.3: One tone harmonic balance simulation of the HBT

4.3 Matlab Slice Plots

The following section presents the three dimensional slice plots obtained in Matlab after data from ADS simulations has been imported. Most of them were presented in Chapter 3. Here they are shown again in larger format to let the reader analyze them better. Matlab plots are analyzed to set up the searching algorithm constraints properly (see Section 3.2.1).

4.3.1 Output power range

From Figure 4.4, Figure 4.6 and Figure 4.9 one can notice that the transistor delivers up to $20dBm$ of output power without reaching high saturation areas. The same plots suggest $0dBm$ as the minimum output power (given the current Ib, Vce and Pin sweeps). Therefore a $Pout$ range from 0 to $20dBm$, with a step of $1dB$ is selected (twice the Pin step used in ADS). A $20dB$ range is wide enough to contain, for example, the most significant power intervals of high order QAM modulations (see Figure 1.1 and Figure 1.2).

4.3.2 Global Ib and Vce constraints

Points with:

- Ib lower than $60\mu A$
- Ib higher than $600\mu A$
- Vce lower than $0.25V$
- Vce higher than $7V$

are not considered. This constraints do not discard many points since they almost match the Ib and Vce ranges used in ADS (see Section 4.2). In fact, the breakdown phenomena have been already taken in account when setting the ADS sweeps. Here, only the points having Ib lower than $60\mu A$ are excluded. This makes sure the device will not work in deep class B zones, with very low Ib. From the slices one can see how non linear that region is.

4.3.3 Start point constraints

The device should start (lowest $Pout$) from a very linear and possibly efficient point. Since the output power is very low, the deep class AB region can be used. For low Pin, it guarantees good linearity and higher efficiency than any other consistent region one can think of. In terms of linearty the second harmonic can be as low as $-30dBc$ while the third one lower than $-50dBc$ (see Figure 4.7 and Figure 4.8). Figure 4.11 shows that an efficiency of 5% can be reached for low Pin.

As explained in Section 3.1.2, the start point gain and phase are very important and should be close to the values the device exhibits in its linear region. From Figure 4.5 one can see that gain in the linear region is higher than $15dB$ while Figure 4.6 and Figure 4.9 show that there the output phase varies between $90\,^\circ$ and $95\,^\circ$. Since in the deep class AB region the phase is a bit different (Figure 4.10) a wider range should be chosen when setting the start point phase constraints.

Start point Ib and Vce limits:

$60\mu A \leq Ib \leq 200\mu A$

$0.25V \leq Vce \leq 1.5V$

Transducer gain lower limit: $15dB$

Output phase limits: $90\,^\circ \leq \varphi_{deg} \leq 100\,^\circ$

Second harmonic upper limit: $-30dBc$

Third harmonic upper limit: $-50dBc$

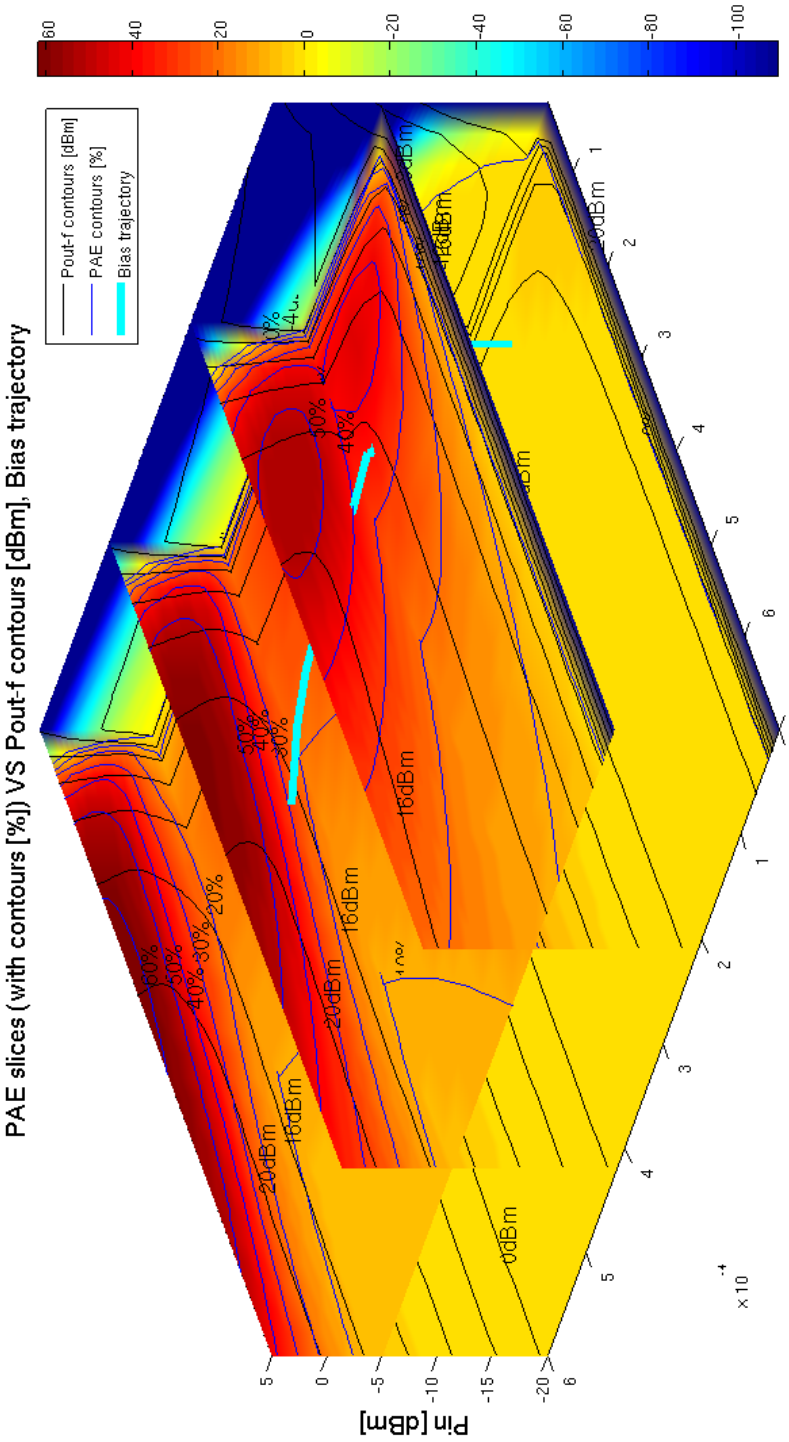

Figure 4.4: HBT Power Added Efficiency Slices

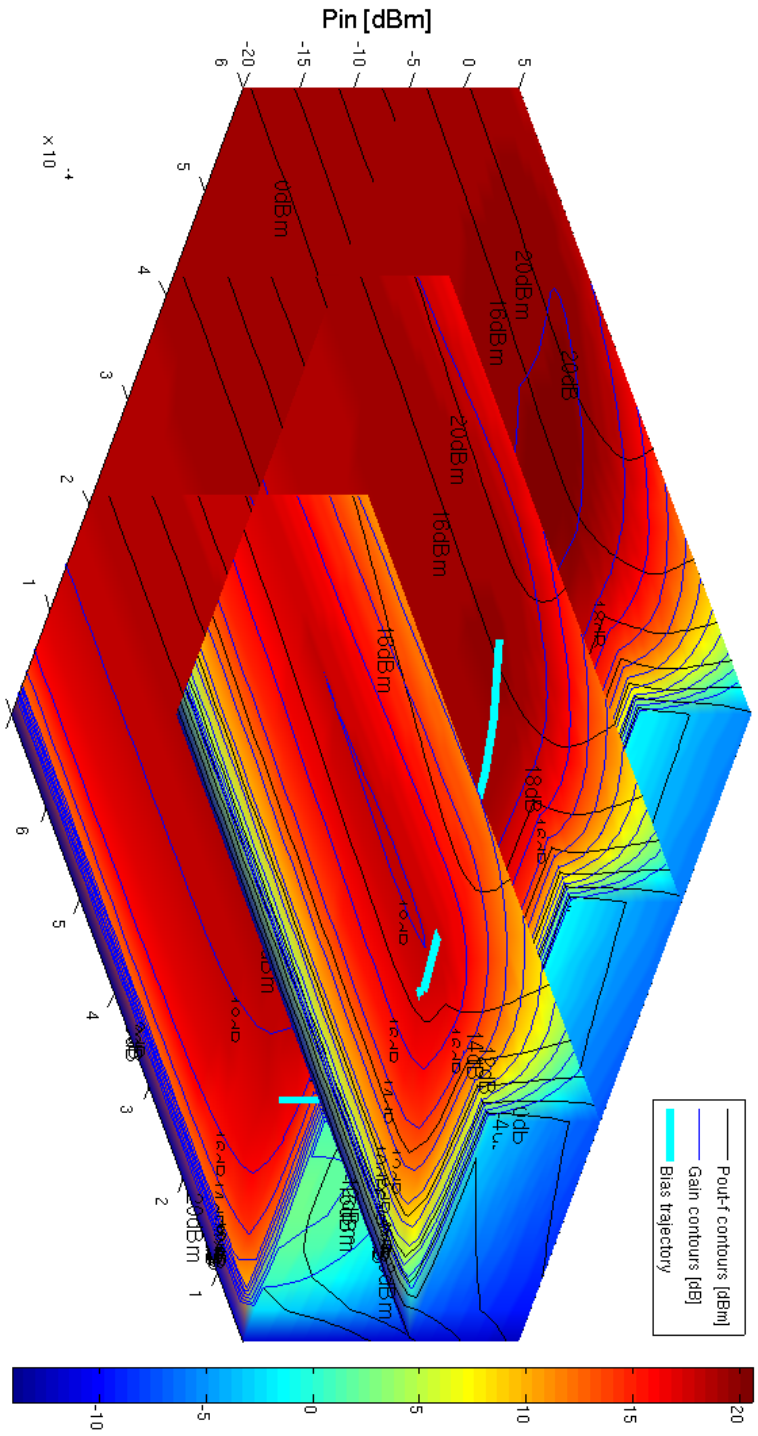

Figure 4.5: HBT Transducer Gain Slices

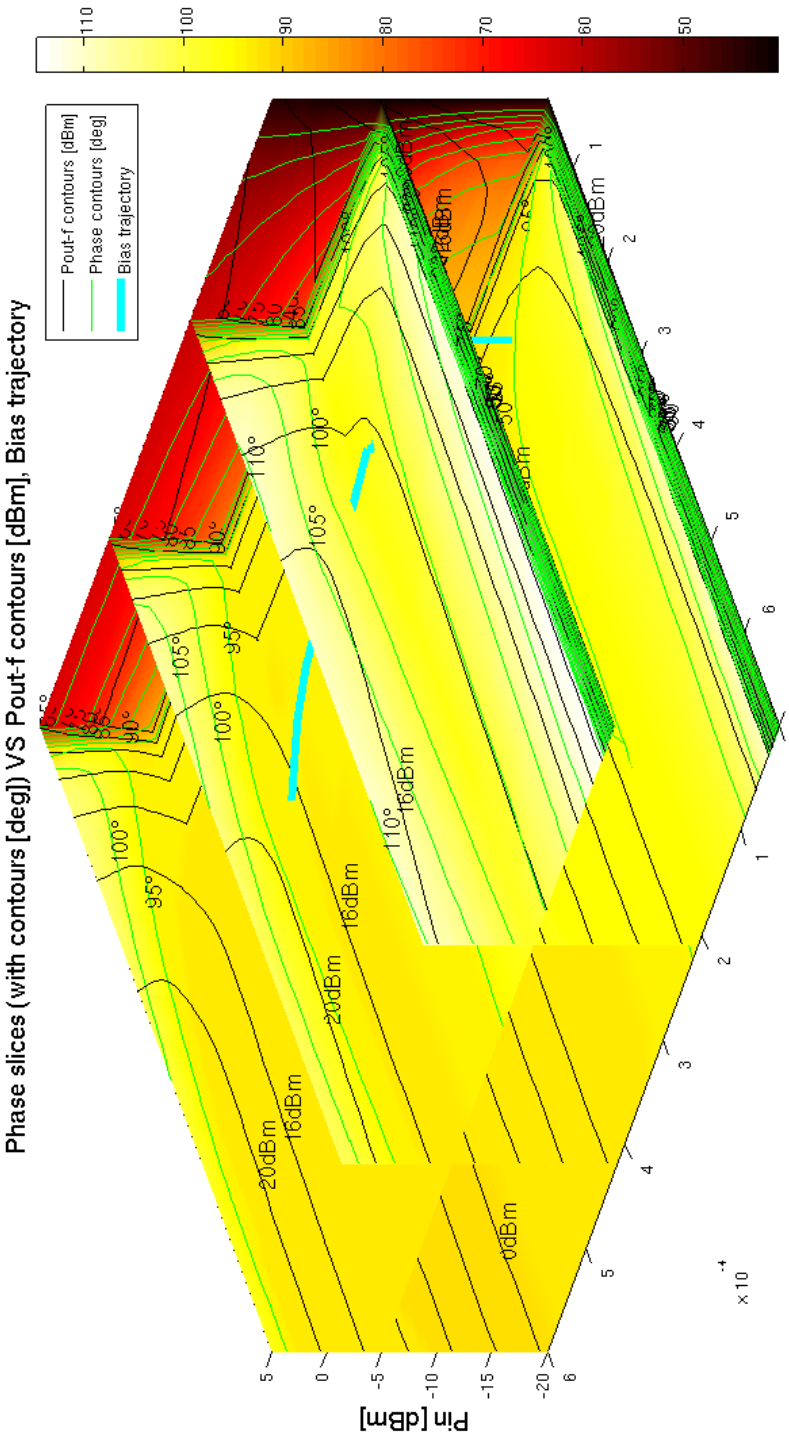

Figure 4.6: HBT Output Phase Slices]

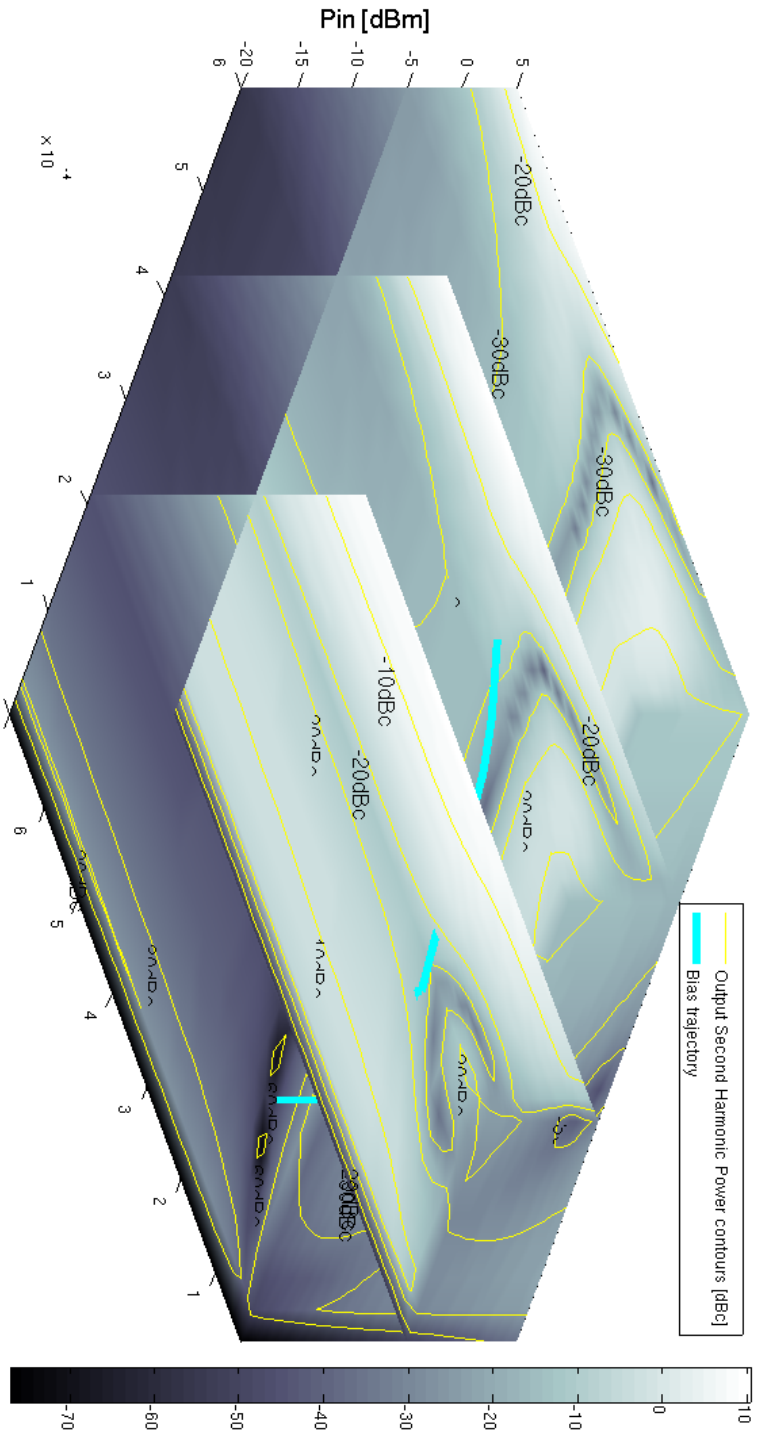

Figure 4.7: HBT Second Harmonic Slices

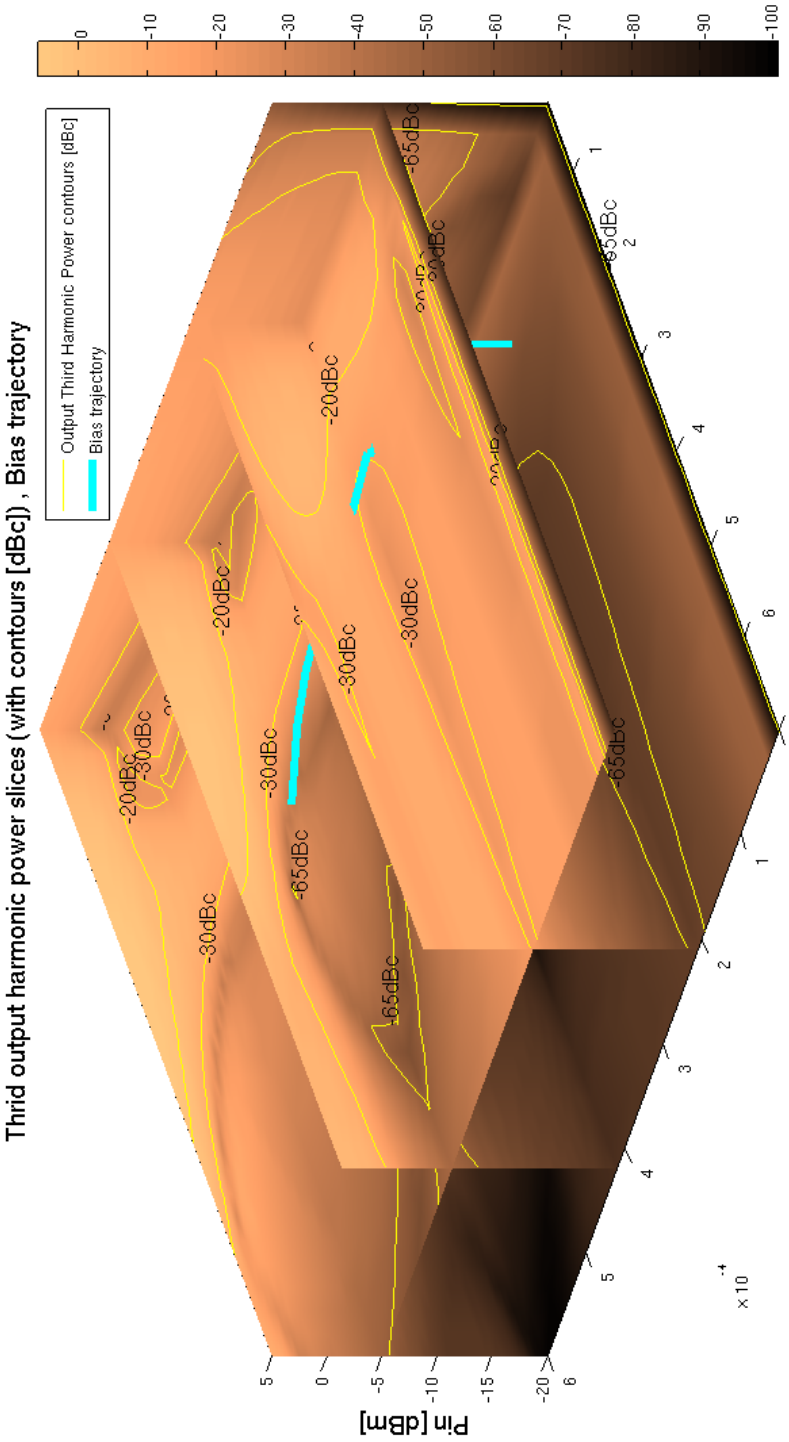

Figure 4.8: HBT Third Harmonic Slices

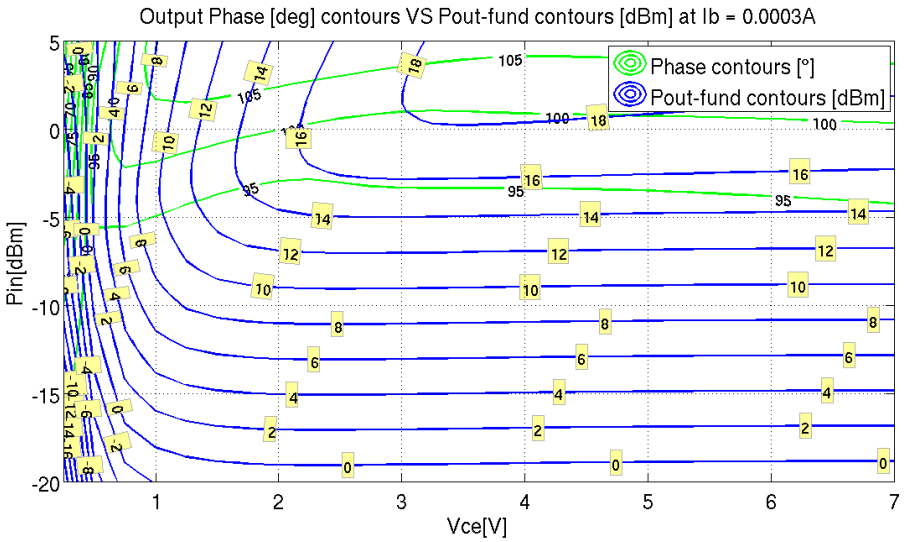

Figure 4.9: Slice at $Ib = 300\mu A$ with $Pout$ and Output Phase contours

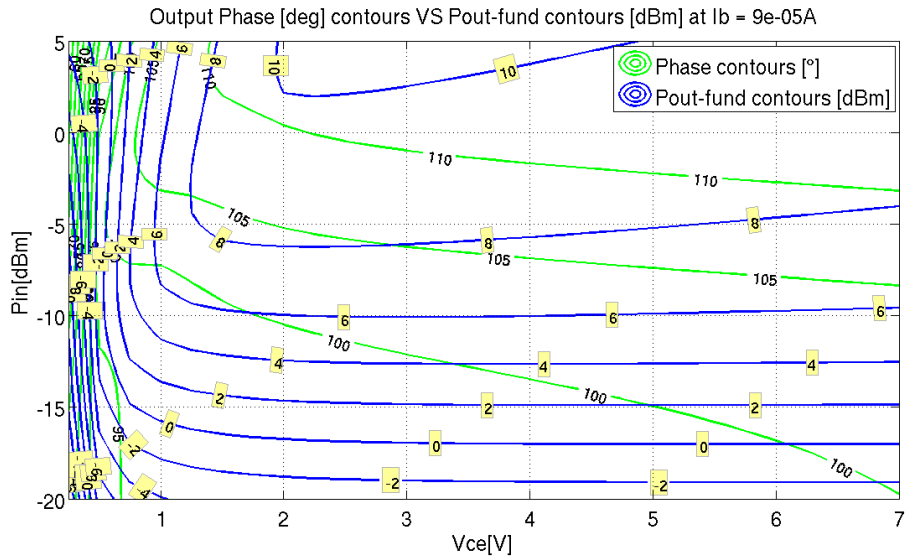

Figure 4.10: Slice at $Ib = 90\mu A$ with $Pout$ and Output Phase contours

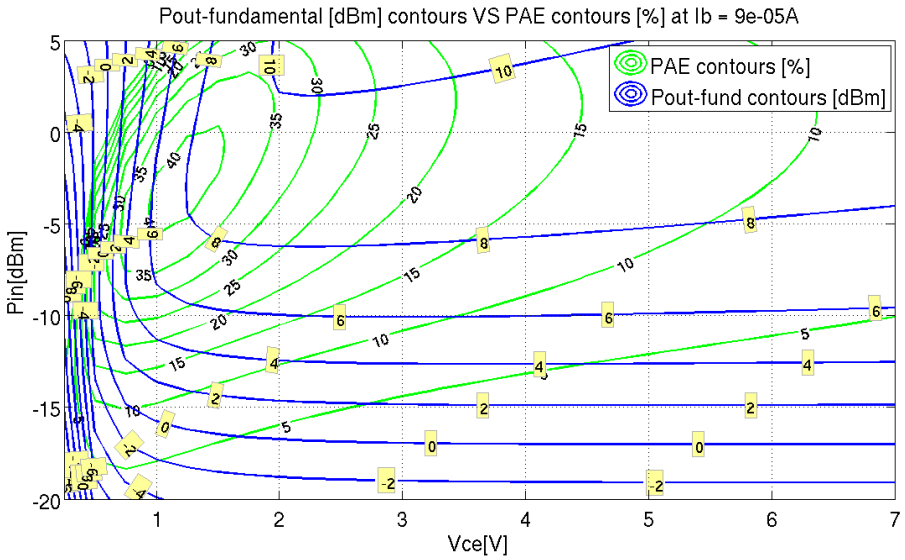

Figure 4.11: Slice at $Ib = 90\mu A$ with $Pout$ and PAE contours

4.4 Cost function weights

Before running the seaching algorithm the Ω cost function weights (Section 3.2.4) should be set . Then an iterative process starts and the user can tune them while searching for a trajectory. The results presented later in this chapter have been found with the weights listed in Table 4.2.

Coefficient	Final value
w_α	1/5
w_β	1/5
w_γ	1/5
w_δ	0
w_ϵ	1/5
w_d	1/5

Table 4.2: HBT path search, final Ω function weights

One can notice that the second harmonic distortion is not considered ($w_\delta = 0$). In fact, the second order non linearities are not that relevant, much more important are the third order ones.

4.5 (Ib,Vce,Pin) space distance normalization coefficients

The distance normalization coefficients (Section 3.2.4) are set as well. As for the Ω cost function weights, the user can tune them. The coefficients in Table 4.3 have led to the final results.

Coefficient	Final value
Ib_{NORM}	$0.00015A$
Vce_{NORM}	$2.3V$
Pin_{NORM}	$5dBm$

Table 4.3: HBT path search, final distance normalization coefficients

4.6 Class A bias point

The HBT is finally evaluated as a class A PA (Section 3.2.6). The bias point having $Ib = 420\mu A$ and $Vce = 5V$ has been chosen, therefore all the power levels in range can be reached (see Figure 4.6 or Figure 4.9).

4.7 Results

After a tuned bias path has been identified, the Matlab script returns some plots. The path is analyzed back in ADS as well, where a two tone harmonic balance simulation can be performed.

4.7.1 Results in Matlab

Matlab returns the following plots:

- Bias trajectory in the (Ib, Vce, Pin) space, Figure 4.12
- Bias trajectory in the transistor's I-V plane, Figure 4.13
- PAE as a function of $Pout$, Figure 4.14
- Transducer gain as a function of $Pout$, Figure 4.15
- Pin - $Pout$ plot, Figure 4.16
- Output phase as a function of $Pout$, Figure 4.17
- Ib Control Function (Ib as function of $Pout$), Figure 4.18
- Vce Control Function (Vce as function of $Pout$), Figure 4.19
- Second Harmonic Distortion, Figure 4.20
- Third Harmonic Distortion, Figure 4.21

The blu continuous curves are the tuned trajectory's characteristics. Curves from a not dynamically biased class A PA are added as well (magenta marked continuous curves). Finally, the figures contain also the extreme paths (see Section 3.2.5):

- maximum PAE path (magenta dashed curves)
- maximum gain flatness path (green dashed curves)
- maximum output phase flatness path (cyan dashed curves)
- minimum second harmonic distortion path (yellow dashed curves)
- minimum third harmonic distortion path (black dashed curves)

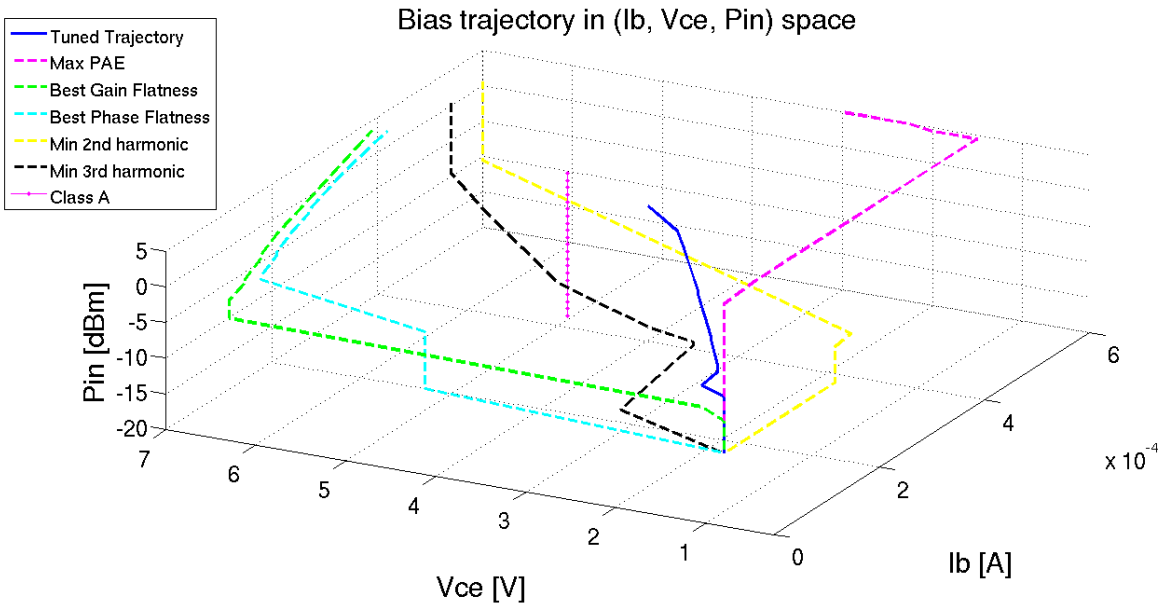

Figure 4.12: Trajectory in the (Ib, Vce, Pin) space

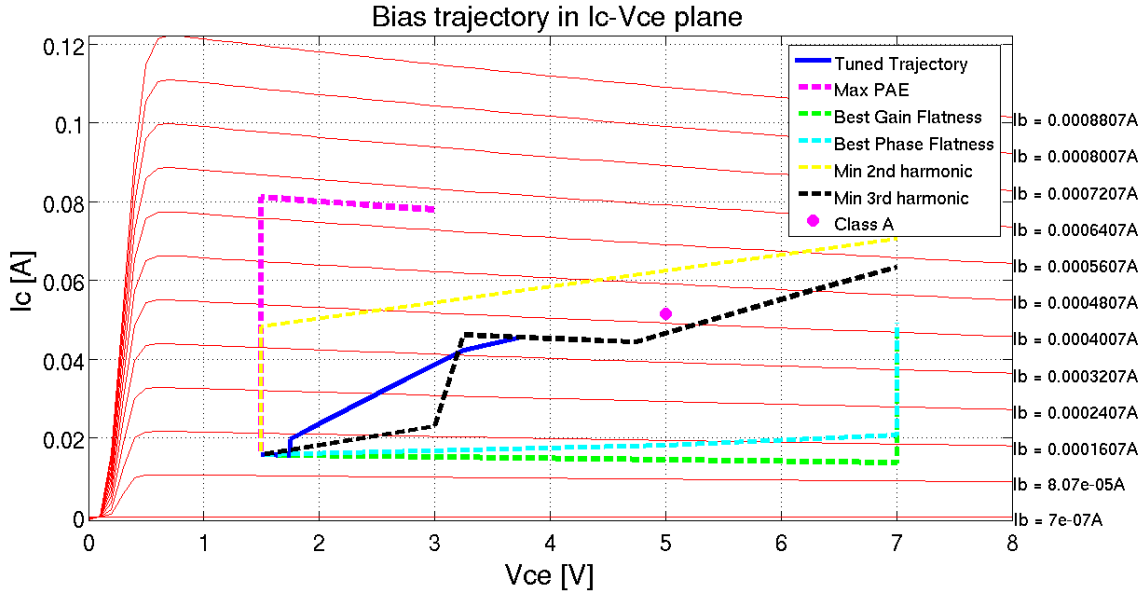

Figure 4.13: Trajectory in the HBT I-V plane

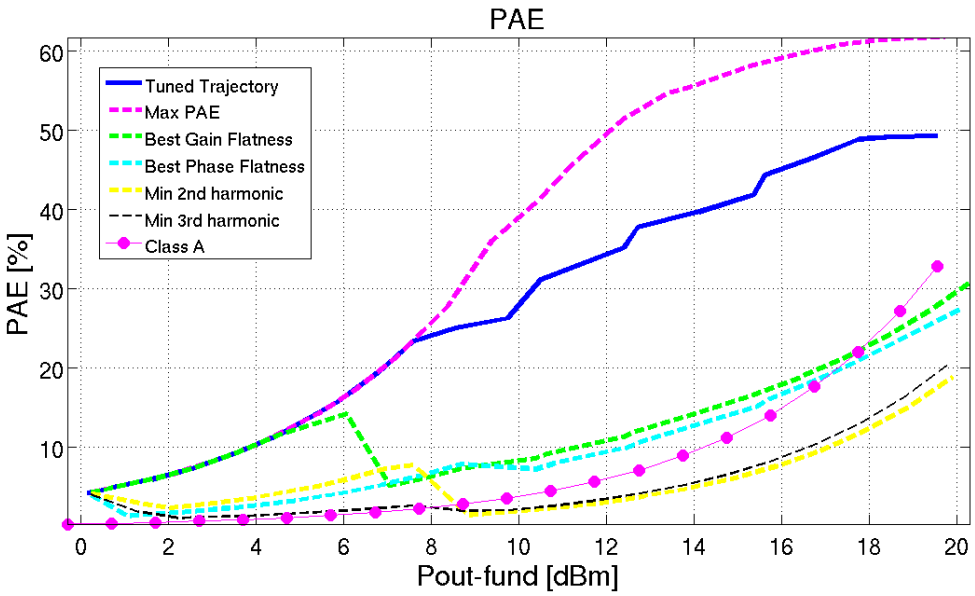

Figure 4.14: HBT Path, Power Added Efficiency

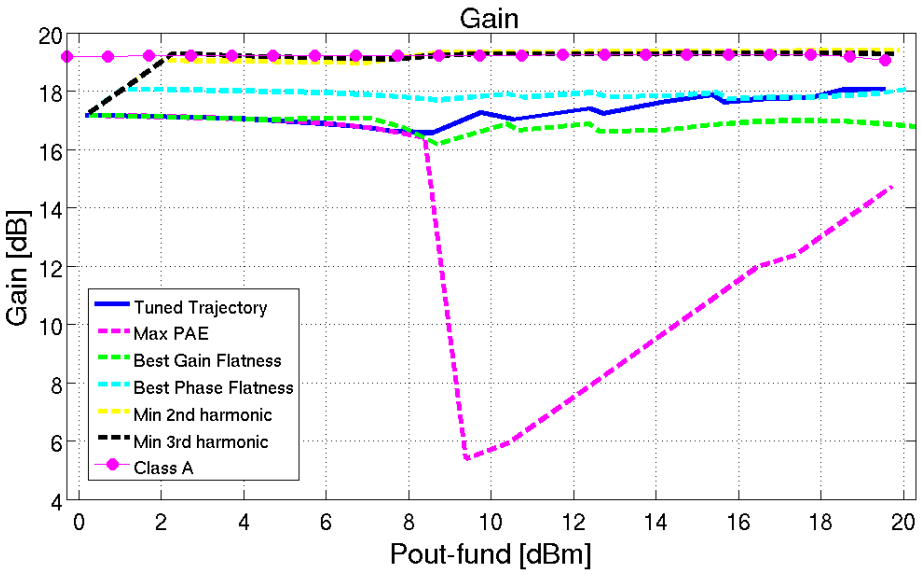

Figure 4.15: HBT Path, Transducer Gain

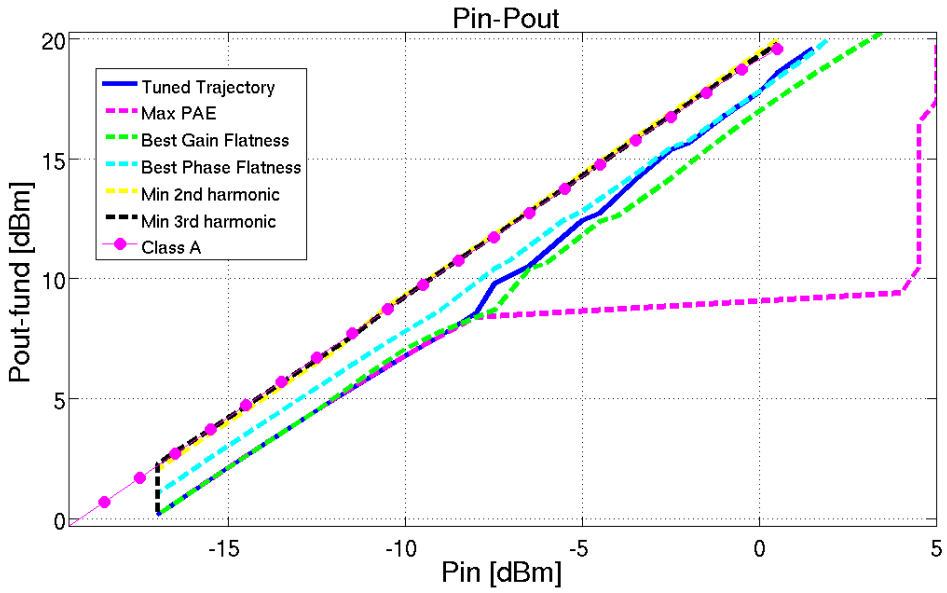

Figure 4.16: HBT Path, $Pin - Pout$

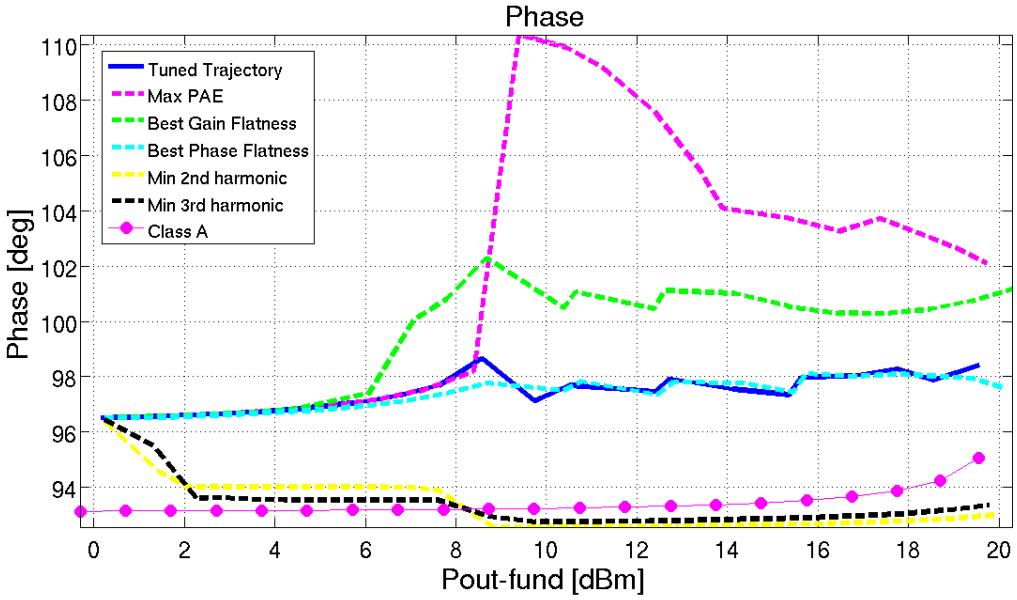

Figure 4.17: HBT Path, Output Phase

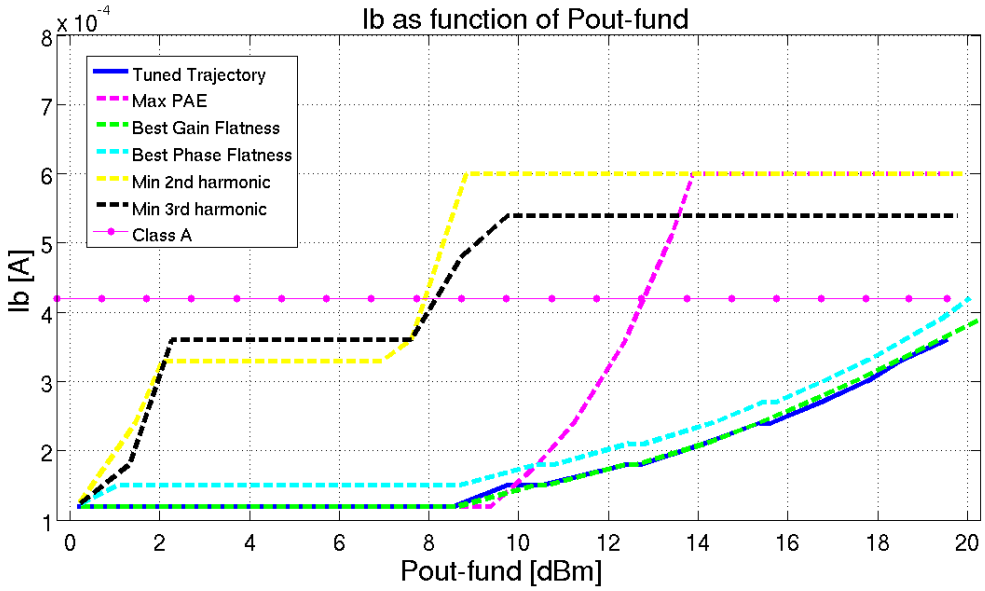

Figure 4.18: *Ib* Control Function

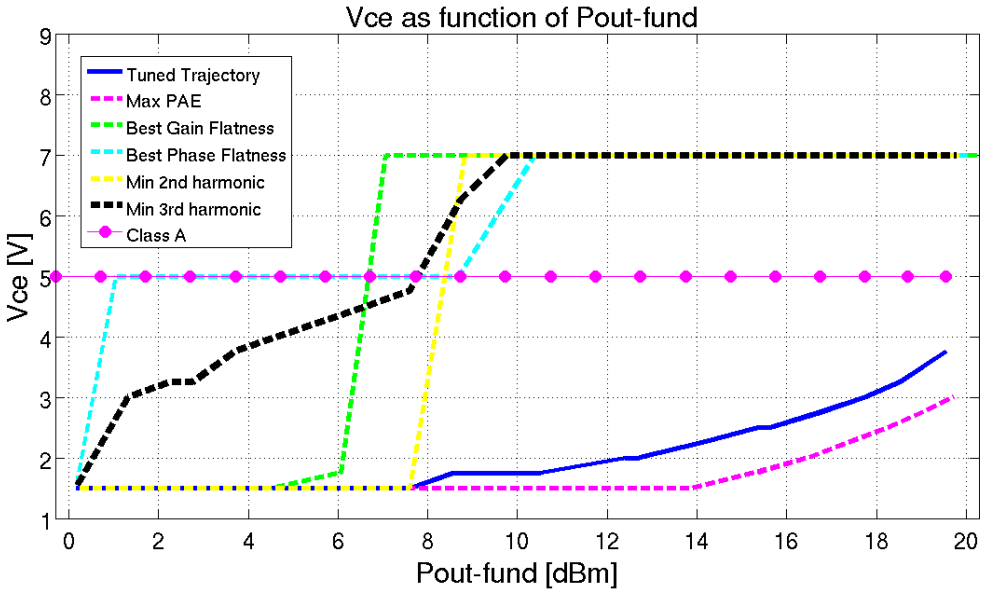

Figure 4.19: *Vce* Control Function

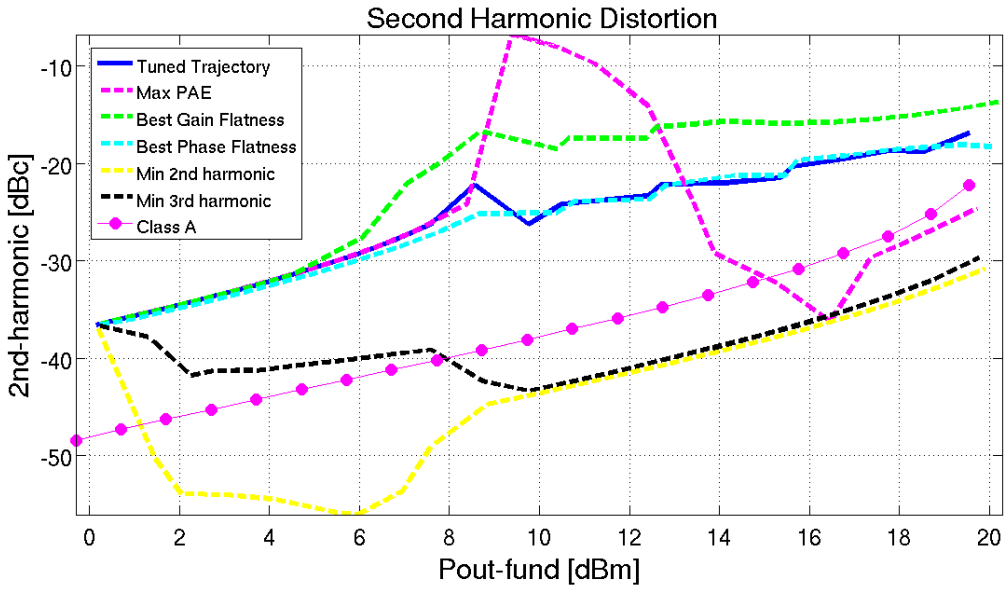

Figure 4.20: HBT Path, Second Harmonic Distortion

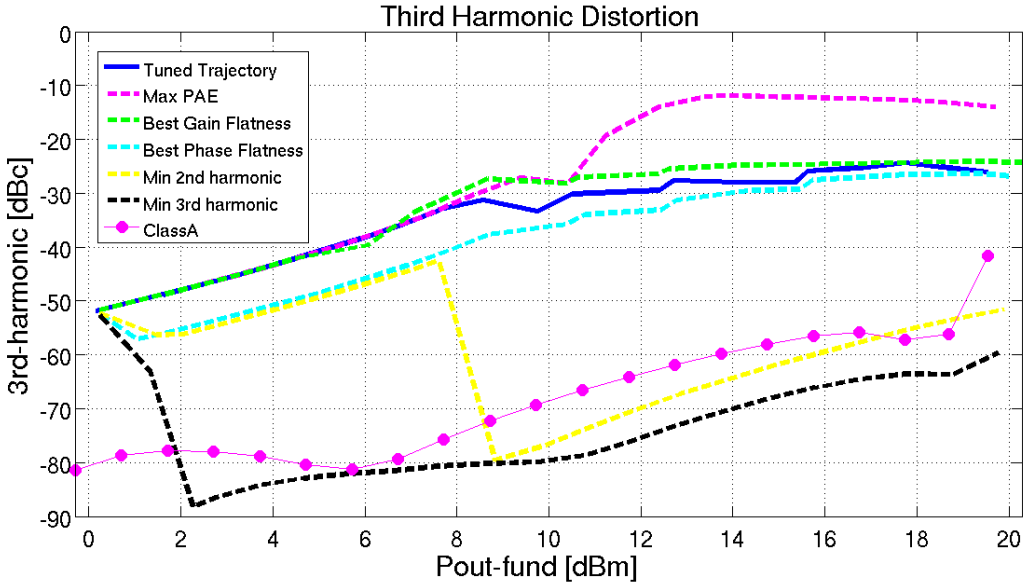

Figure 4.21: HBT Path, Third Harmonic Distortion

4.7.2 Results in ADS

Frist, the stability of the amplifier is checked at each point of the bias trajectory. In fact the HBT amplifier is conditionally stable at its input when connected to a matched source and at its output when terminated ($Z_0 = 50\Omega$). This, at the frequency of $1.9GHz$. As expected, the device is not well matched to 50Ω.

The PA's dynamic load line can be plotted in ADS for each point of the bias path. All the HBT dynamic load lines are shown in Figure 1.3.

Finally, a two tones harmonic balance simulation is run along the path at the frequency of $1.9GHz$. Some relevant quantities are reestimated since arising intermodulation products misspend more and more power thus worsening gain and efficiency. Therefore, PAE and gain from the two tones simulation are compared with PAE and gain form the Matlab results (they are actually ADS one tone simulation data). The tones are $10kHz$ distant in frequency. The following plots are considered:

- PAE as a function of $Pout$, both from one 1-tone and 2-tones simulations, Figure 4.22
- Transducer gain as a function of $Pout$, both from one 1-tone and 2-tones simulations, Figure 4.23
- Pin - $Pout$ plot, both from one 1-tone and 2-tones simulations, Figure 4.24
- Third order intermodulation products (IMP) *versus* $Pout$, Figure 4.25
- Fifth order intermodulation products *versus* $Pout$, Figure 4.26

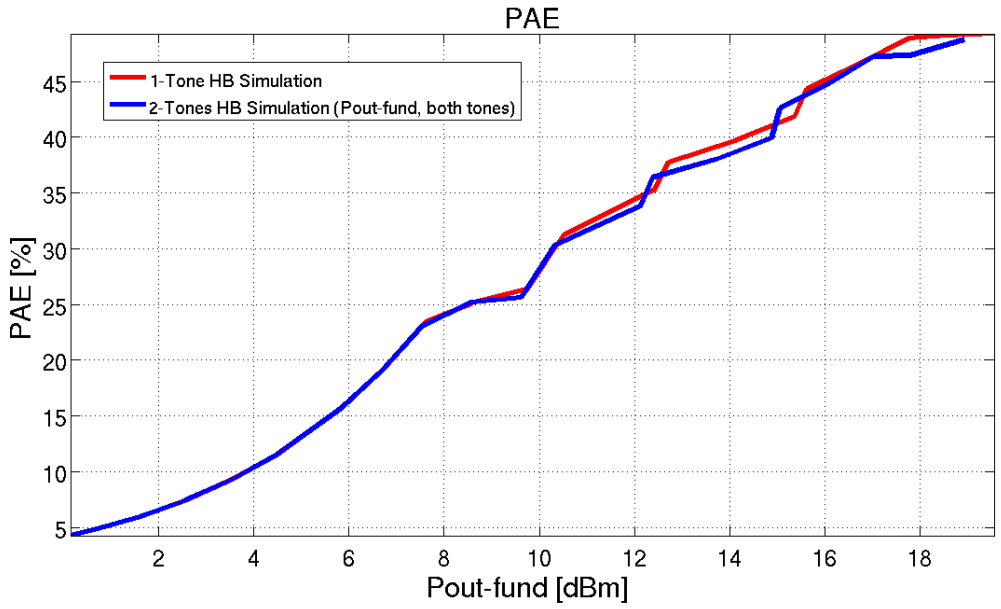

Figure 4.22: HBT Path, 1-Tone *vs* 2-Tones PAE

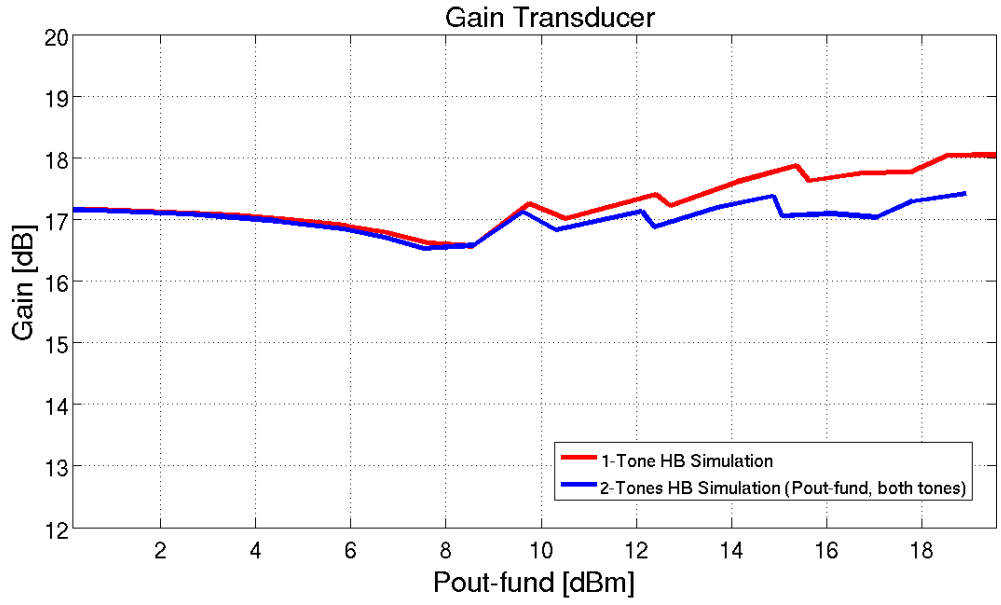

Figure 4.23: HBT Path, 1-Tone *vs* 2-Tones transducer gain

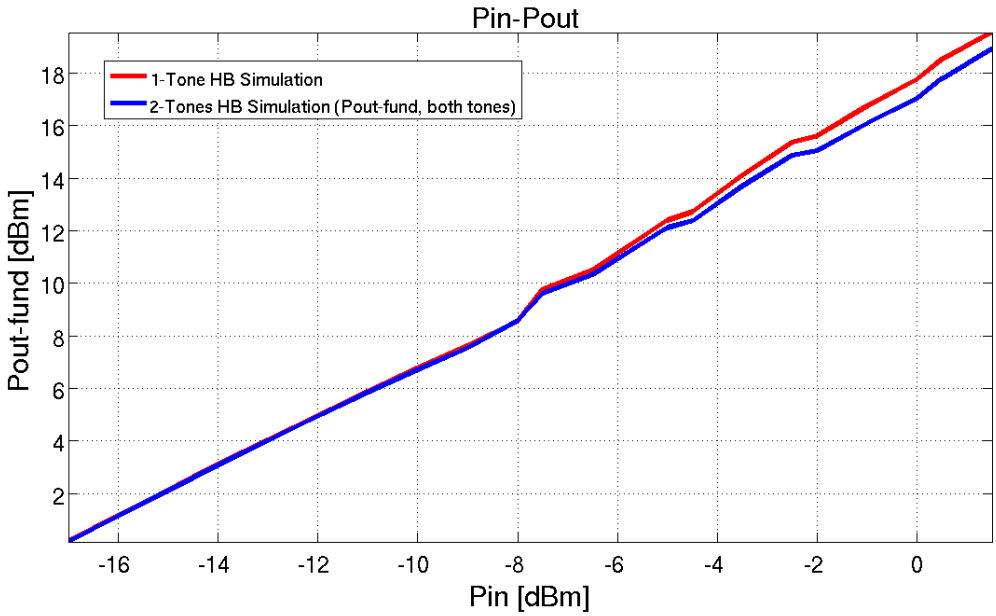

Figure 4.24: HBT Path, 1-Tone *vs* 2-Tones Pin-Pout plot

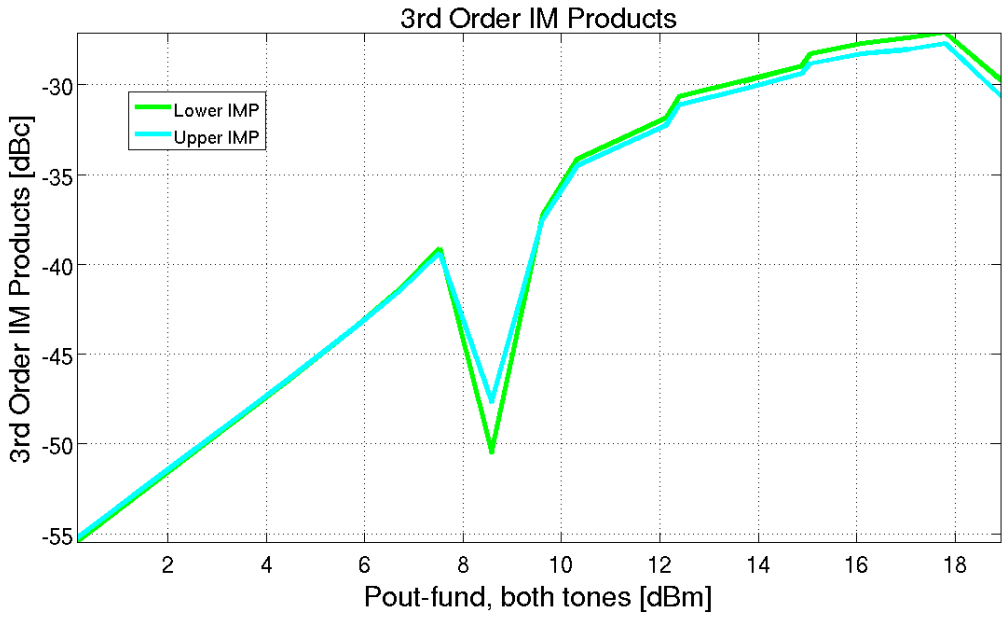

Figure 4.25: HBT Path, 3rd order intermodulation products

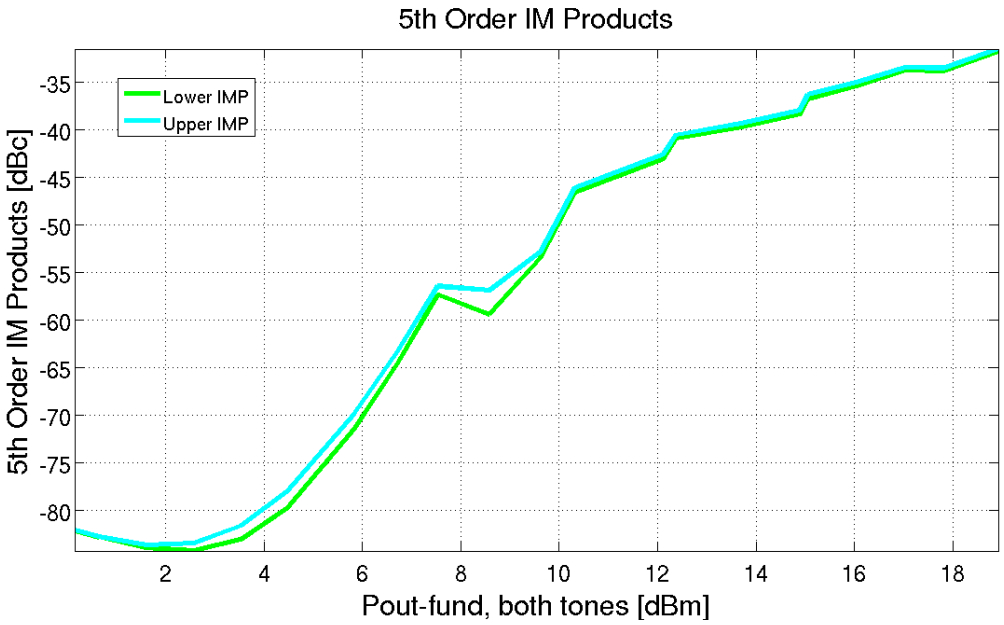

Figure 4.26: HBT Path, 5th order intermodulation products

4.8 Comments

The tuned trajectory found for the HBT transistor has an average PAE of 27.5% while the class A average PAE is 8.0% (Figure 4.14). Gain and output phase variations are limited: $1.5dB$ of maximum variation for the gain and $2\,^{\circ}$ for the phase (see Figure 4.15 and Figure 4.17). Yet, Ib and Vce do not have complicated control functions (Figure 4.18 and Figure 4.19). Harmonic distortion is relevant, in particular the second harmonic reaches $-17dBc$ (Figure 4.20) and the third one $-25dBc$ (Figure 4.21).

According to the two tones ADS simulation, at high $Pout$, the third order IMP grow up to $-27dBc$ and the fifth order IMP to $-31dBc$ (Figure 4.25 and Figure 4.26). These values are acceptable, since the PA will not always deliver the highest output power and a simple digital predistortion system could reduce the intermodulation products even more [12].

The IMP affect the device's efficiency as well as its gain. Figure 4.22 and Figure 4.23 show PAE and transducer gain *versus* $Pout$ from a one tone and a two tone simulation (frequency spacing of $10kHz$). With two tones at the input, the gain is $1dB$ smaller (for high $Pout$) and the average power added efficiency is a bit lower as well (26.7%). These differences are not that significant for the reasons mentioned above.

In Figure 4.18, Figure 4.19 and Figure 1.3 one can notice that the device works as a class A for low output power levels. As soon as $Pout$ increases, distortion increases and the system moves its bias point. This is even more clear from the tables containing the tuned path parameters and its (Ib, Vce, Pin) coordinates in Appendix B.

Since the HBT amplifier is conditionally stable along the path when matched sources and termination loads are used (at the frequency of $1.9GHz$), the device can be tested in the laboratory where wideband matched signal generators and analyzers are available.

The load lines (Figure 1.3) are elliptical and not straight lines because the amplifier is connected to a slightly capacitive impedance (the DC block). The collector current is far under its peak limit of $180mA$ when the device is delivering the maximum output power. Moreover, the plot shows how the device clips in saturation and interdiction, especially when $Pout$ is high.

Chapter 5

Dynamically biased pHEMT class A power amplifier

The algorithm from Chapter 3 is here applied to a pHEMT power amplifier. At the time this report is written the device has not been fabricated yet, therefore measurements cannot be performed. The PA has been designed in ADS and is supposed to be a monolithic microwave integrated circuit (MMIC).

The simulations as well as the analysis of the amplifier are here described. The same procedure as in Chapter 4 is followed and the same considerations applied, thus less details are described. Some insights are given when differences arise.

The amplifier is based on a FET device, thus the bias signals are Vgs, Vds and not Ib, Vce. The (Ib, Vce, Pin) space is here the (Vgs, Vds, Pin) space.

5.1 The pHEMT Power Amplifier

The device is a simple class A PA. It has been designed to deliver up to $1W$ $(30dBm)$ of output power and to work at the $Vgs = 0.7, Vds = 9V$ bias point. The working frequency is $6GHz$.

The amplifier is based on a pHEMT transistor (pseudomorphic High Electron Mobility Transistor). The HEMT is a field effect transistor that uses a heterojunction as its conductive channel. The heterojunction creates a two dimensional quantum well in the conduction band of undoped GaAs. Therefore, electrons from the near n-doped region

get trapped and form a highly conductive thin layer (two dimensional electron gas). Since the undoped GaAs does not have impurities, the electron mobility in the layer is very high and the channel has a very low resistivity [18]. Therefore, HEMTs are used in applications where high gain and low noise at high frequencies are required.

A HEMT where the two different materials used in the heterojunction do not have the same lattice constant is called pHEMT or pseudomorphic HEMT.

The device used in this amplifier is a pHEMT (enhancement mode) from the TriQuint Semiconductor foundry (see Figure 5.1).

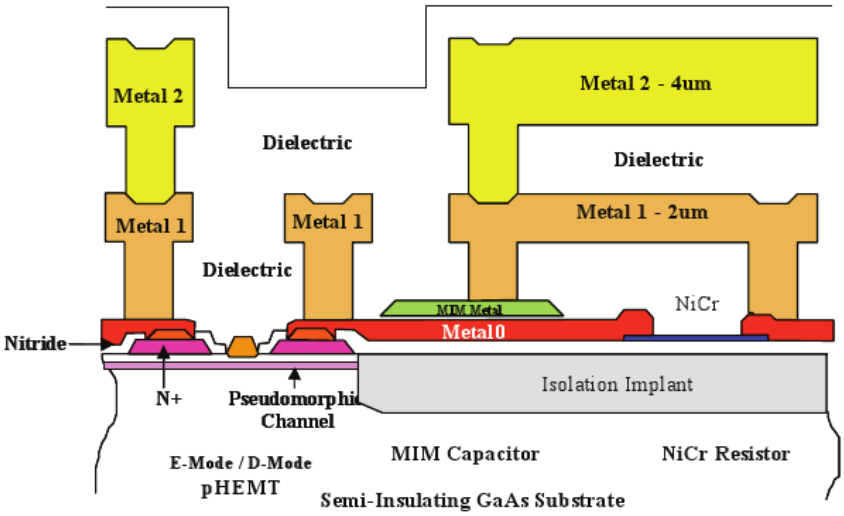

Figure 5.1: TriQuint's TQPED process, $0.5\mu m$ pHEMT Cross-Section [19]

The gate of the transistor used here has nine $240\mu m$ wide (w_{FINGER}) fingers. Some maximum ratings are listed in Table 5.1.

Description	Parameter	Value	Unit
Maximum channel current per gate unit length	I_{max}	320	mA/mm
Breakdown D-G voltage	BV_{dg}	$15min, 18typ$	V

Table 5.1: TriQuint pHEMT Maximum Ratings, [19]

The device's maximum channel current is:

$$I_{MAX} = n_{\text{FINGER}} \cdot w_{\text{FINGER}} \cdot I_{max} \tag{5.1}$$

Given the pHEMT under test, according to (5.1) the channel current should not exceed $691.2mA$.

The tested amplifier is matched for gain at its input as well as at its output when both source and load have an impedance of $Z_0 = 50\Omega$. The device is also unconditionally stable at the selected bias point. Nevertheless, stability should be rechecked after a bias trajectory is found. The circuit is shown in Figure 5.2.

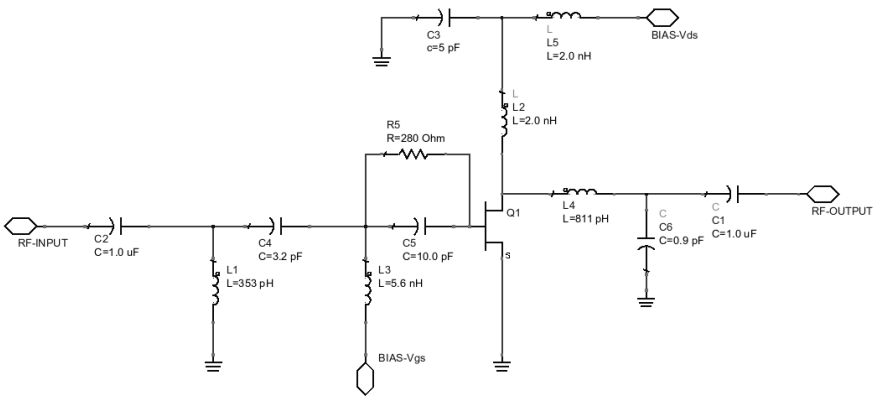

Figure 5.2: Class A pHEMT Power Amplifier

5.2 ADS One Tone Harmonic Balance Simulation

A one tone harmonic balance simulation is first run on the amplifier and the variables Vgs, Vds and Pin swept. The following sweeps are defined:

***Vgs* sweep:** from $0.25V$ to $1.25V$ with a step of $0.02V$. Vgs is swept from below the device threshold ($Vth \approx 0.35V$, see [19]) up to saturation.

***Vds* sweep:** from $1.50V$ to $14V$ with a step of $0.25V$. The upper limit of $14V$ has been set not to reach the drain-gate breakdown voltage ($15V$ min) when the lowest Vgs is applied (see Table 5.1).

***Pin* sweep:** from $-8dBm$ to $22dBm$ with a step of $1dB$. A 30dB interval can contain most of a QAM modulated signal's dynamic range (see Figure 1.1 and Figure 1.2). Its upper limit of $22dBm$ has been selected to let the device reach 30dBm of output power (estimating a gain of $\sim 10dB$).

5.3 Matlab Slice Plots

The three dimensional slice plots from Matlab are here presented and the searching algorithm constraints set (Section 3.2.1).

5.3.1 Output power range

As expected, the transistor can deliver up to $30dBm$ of output power although saturation phenomena arise (Figure 5.3, Figure 5.5 and Figure 5.8). A $20dB$ range, from $10dBm$ to $30dBm$, is chosen since it can contain the most significant power intervals of a high order QAM modulated signal (Figure 1.2). The selected step is $1dB$ (same as the Pin sweep step used in ADS).

5.3.2 Global Ib and Vce constraints

Points with:

- Vgs lower than $0.25V$
- Vgs higher than $0.95V$
- Vds lower than $1.5V$
- Vds higher than $9.5V$

are not considered. This constraints limits the upper Vgs voltage to $0.95V$, therefore the device does not get into high saturation areas. Vds is limited to $9.5V$ since the drain-gate breakdown may occur at $15V$ (see Table 5.1).

5.3.3 Start point constraints

The start point (lowest $Pout$) should be very linear and possibly efficient. Once more, the deep class AB region fulfills these requirements (for low Pin levels). Second harmonic can be as low as $-50dBc$ while the third one lower than $-60dBc$ (see Figure 5.6 and Figure 5.7). Figure 5.10 shows that an efficiency of 5% can be obtained.

The start point gain and phase should be close to the values the device exhibits in the linear region. In that area the gain is higher than $10dB$ (Figure 5.4) and the output phase varies between $80\,^\circ$ and $85\,^\circ$ (Figure 5.5 and Figure 5.8).

Start point Vgs and Vds limits:
$0.25V \leq Vgs \leq 0.55V$
$1.5V \leq Vds \leq 3V$

Transducer gain lower limit: $10.5dB$

Output phase limits: $80\,^\circ \leq \varphi_{deg} \leq 85\,^\circ$

Second harmonic upper limit: $-50dBc$

Third harmonic upper limit: $-60dBc$

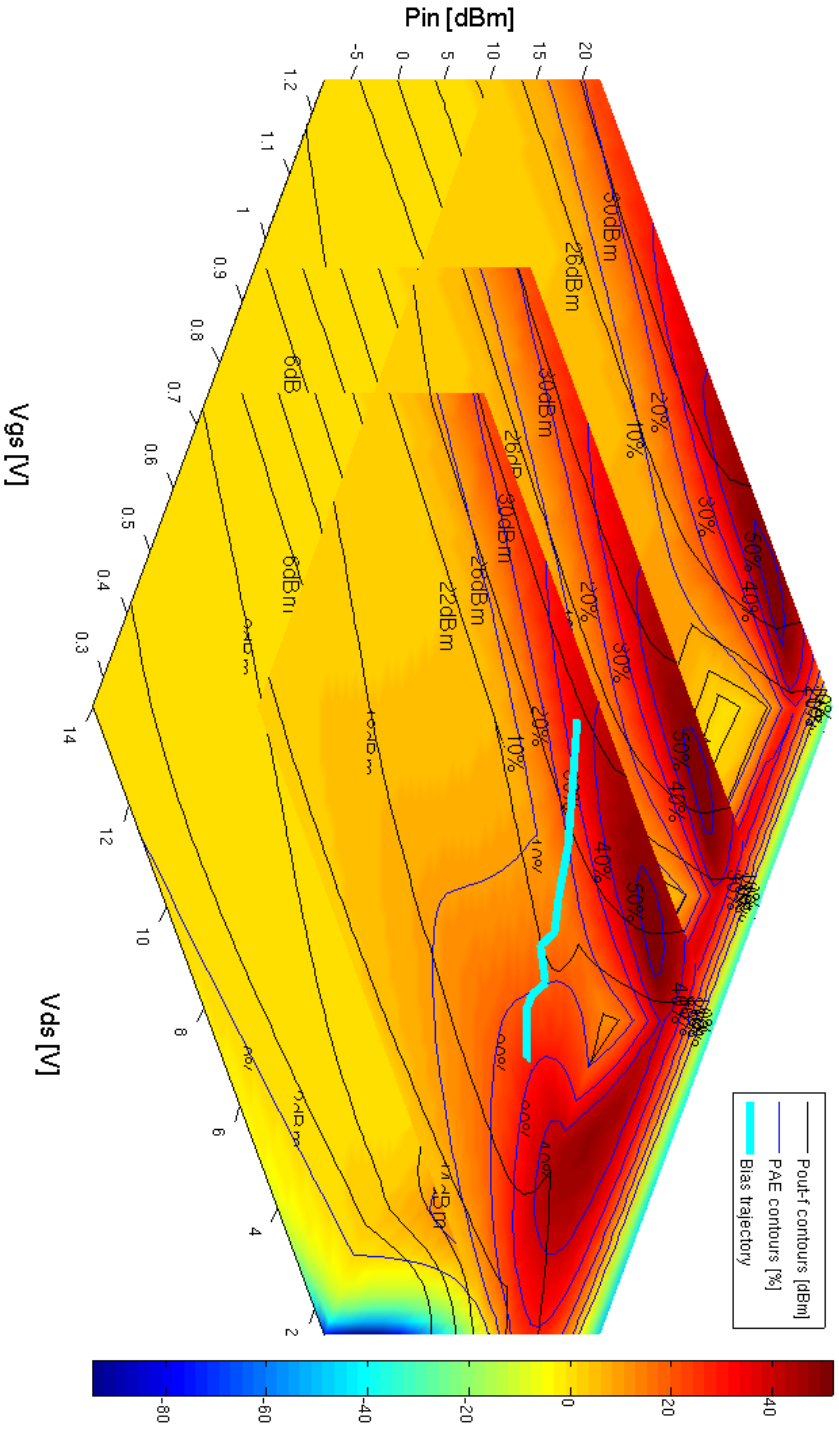

Figure 5.3: pHEMT Amplifier, Power Added Efficiency Slices

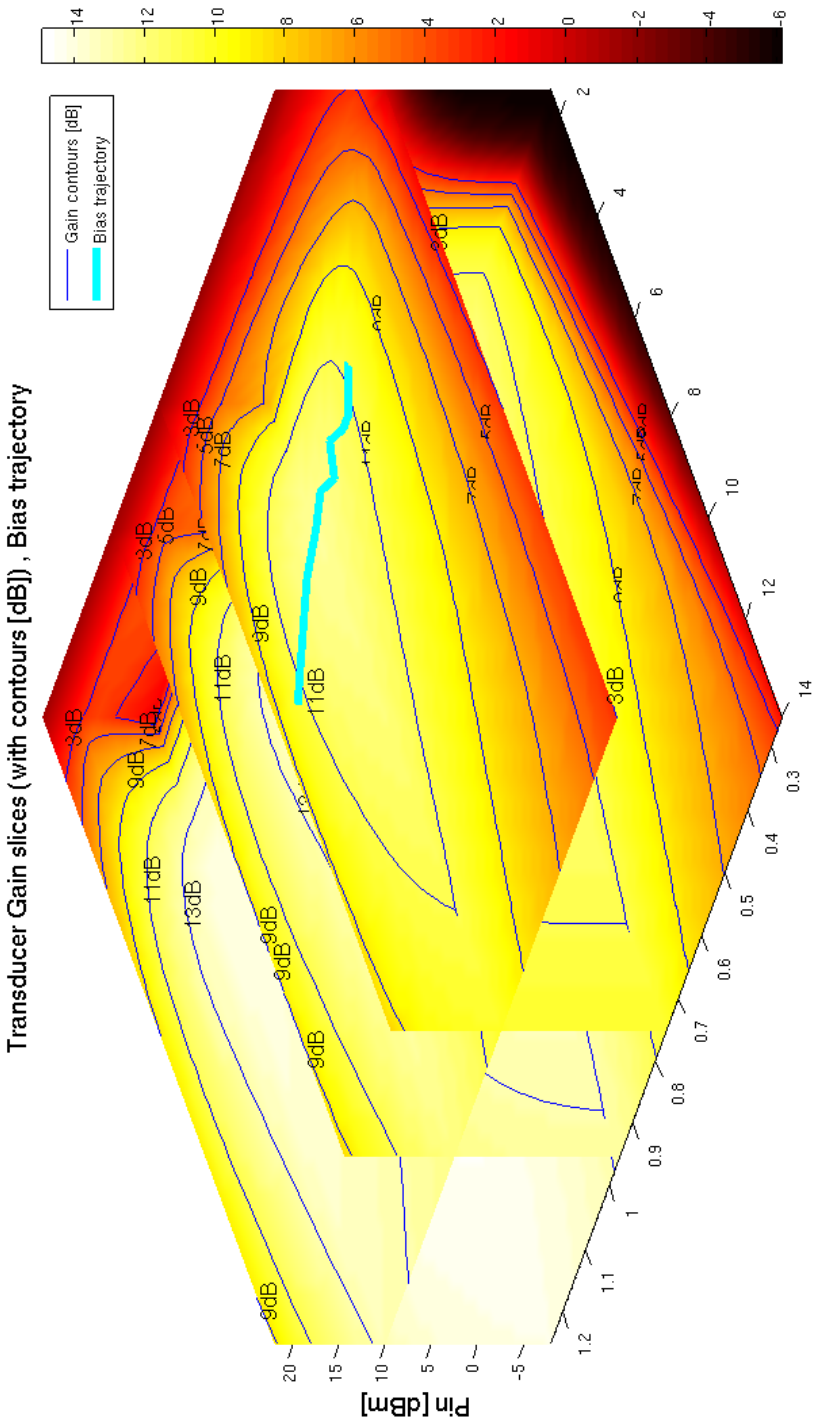

Figure 5.4: pHEMT Amplifier, Transducer Gain Slices

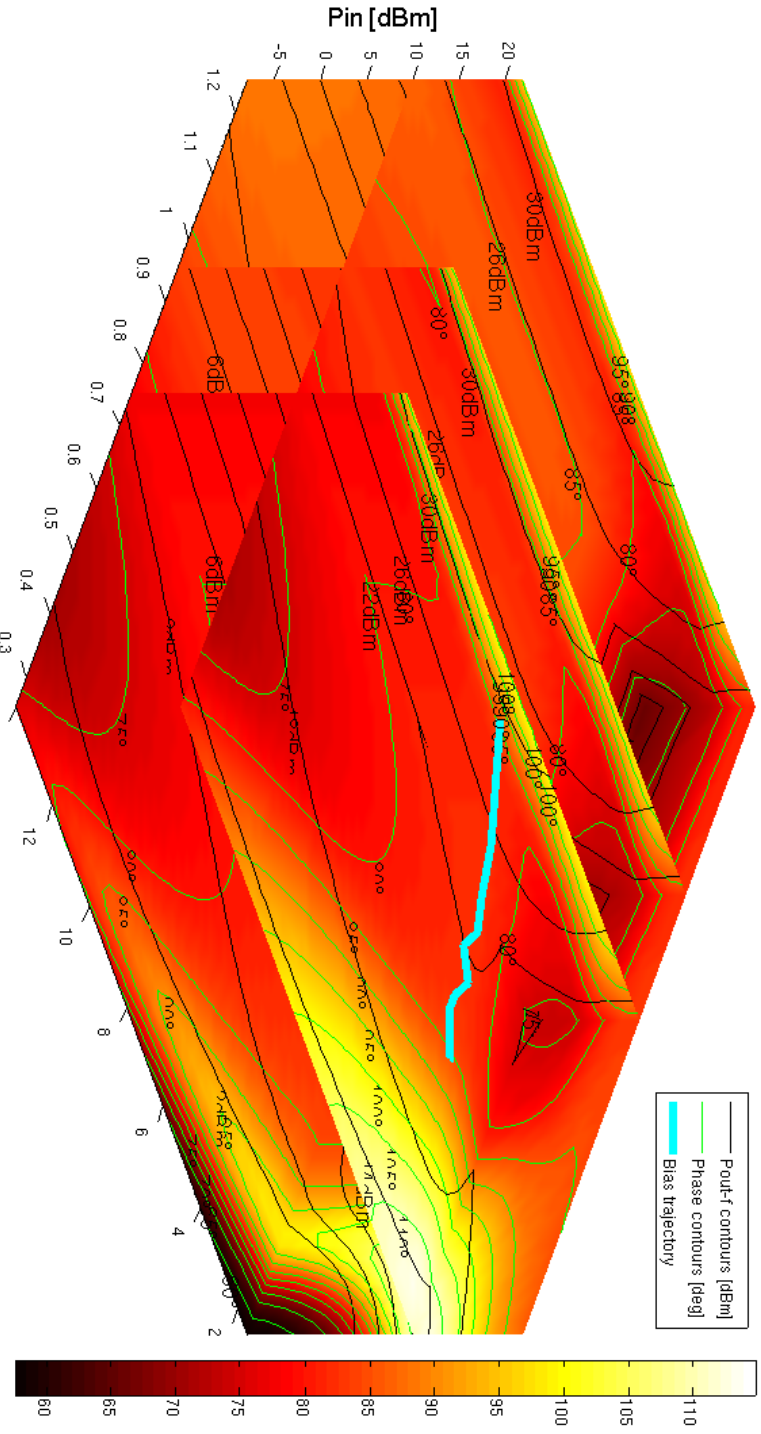

Figure 5.5: pHEMT Amplifier, Output Phase Slices]

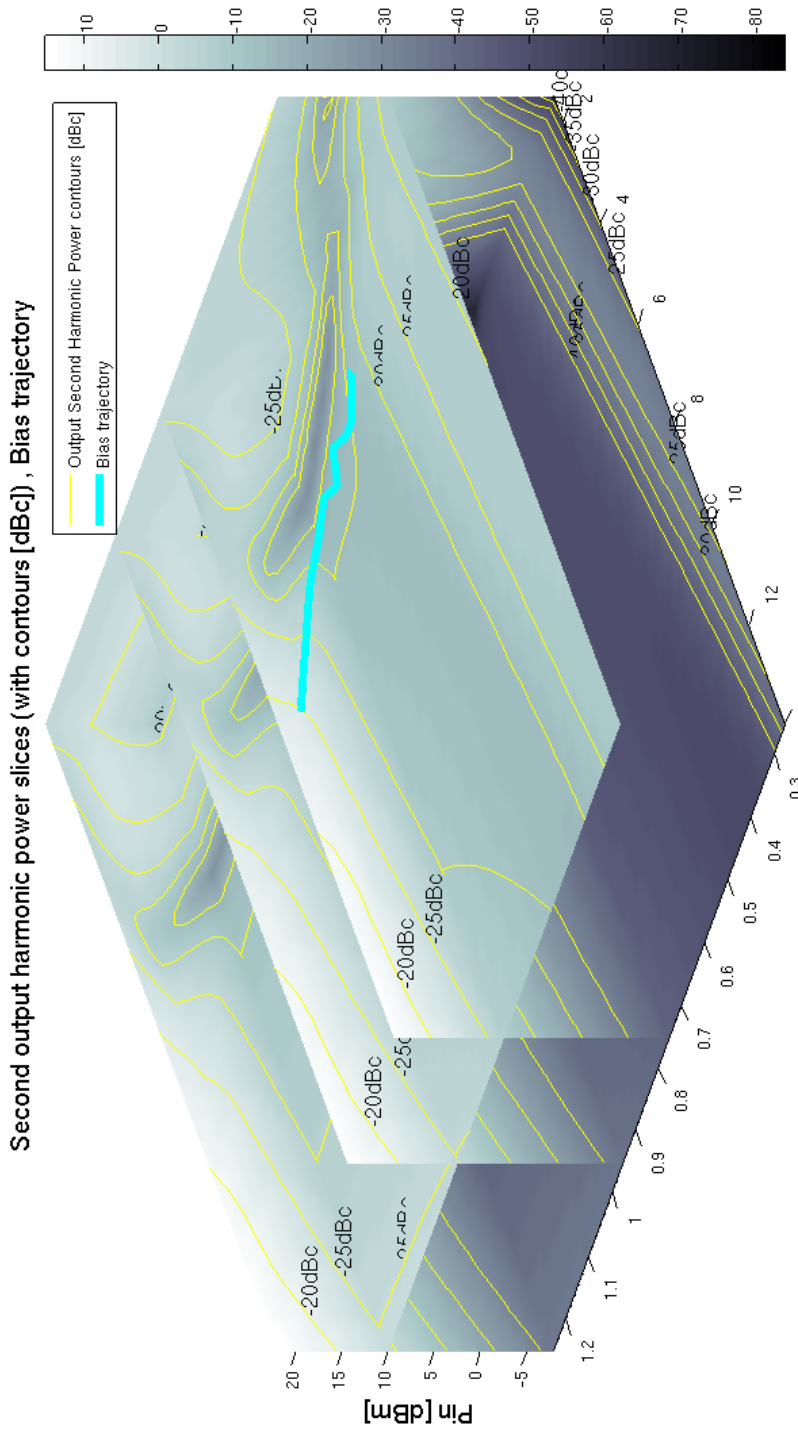

Figure 5.6: pHEMT Amplifier, Second Harmonic Slices

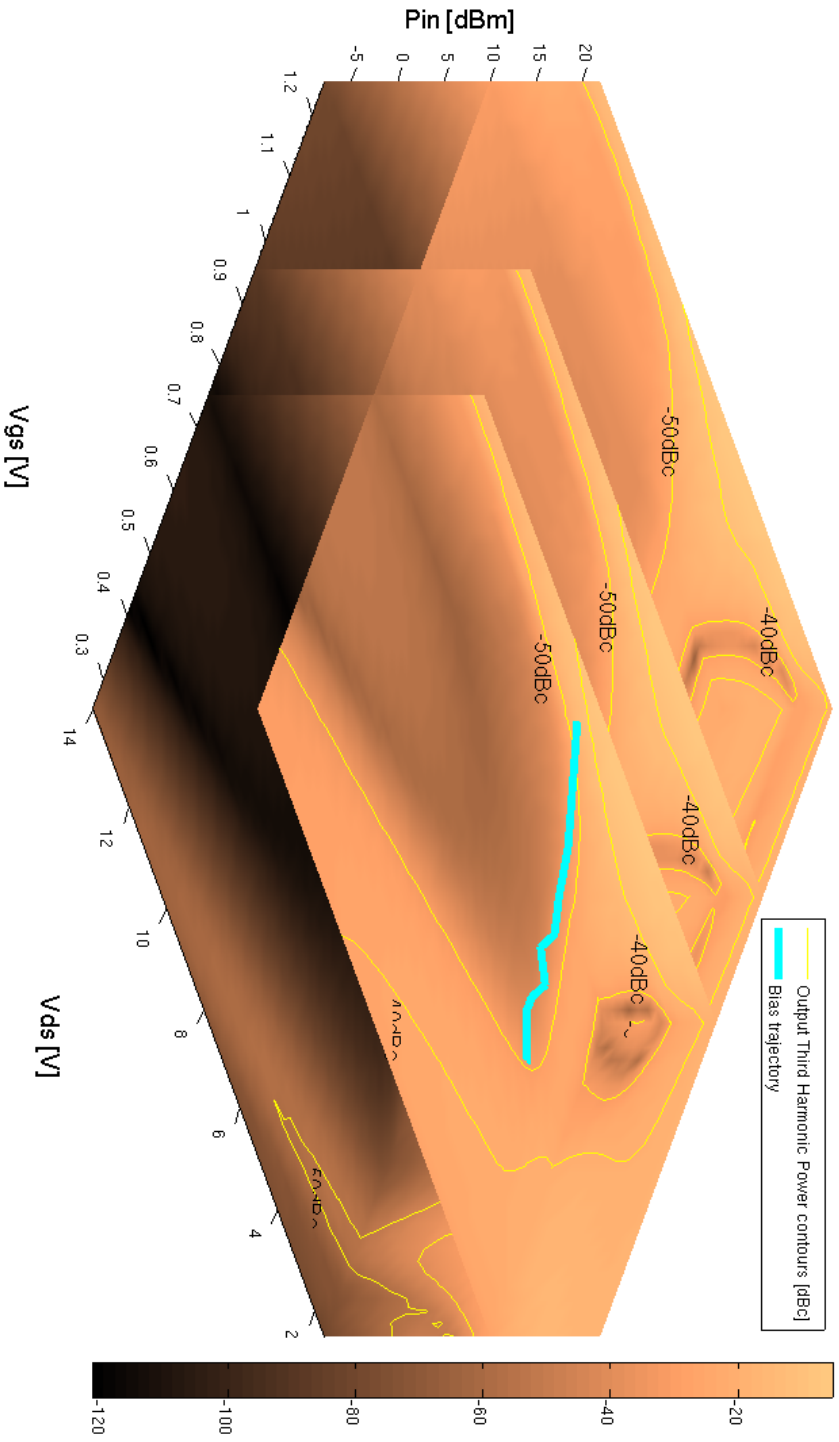

Figure 5.7: pHEMT Amplifier, Third Harmonic Slices

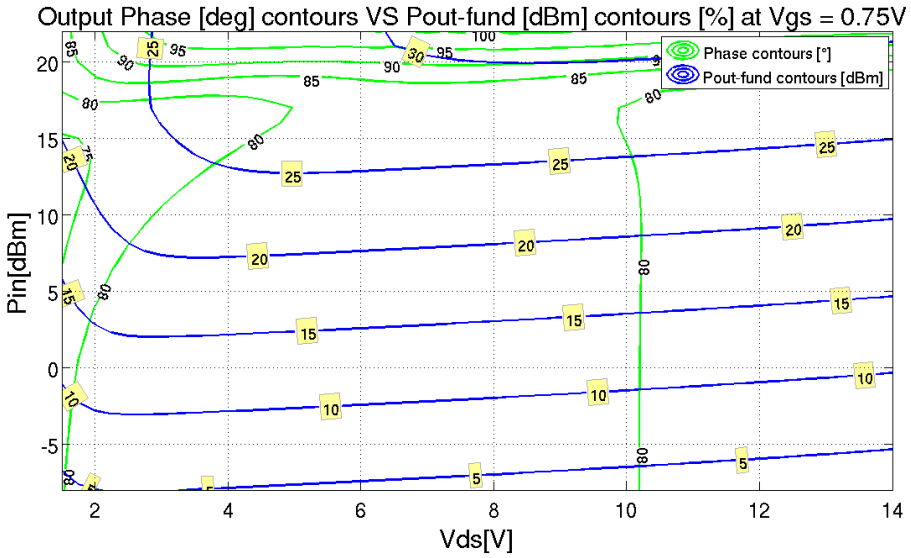

Figure 5.8: Slice at $Vgs = 0.75V$ with $Pout$ and Output Phase contours

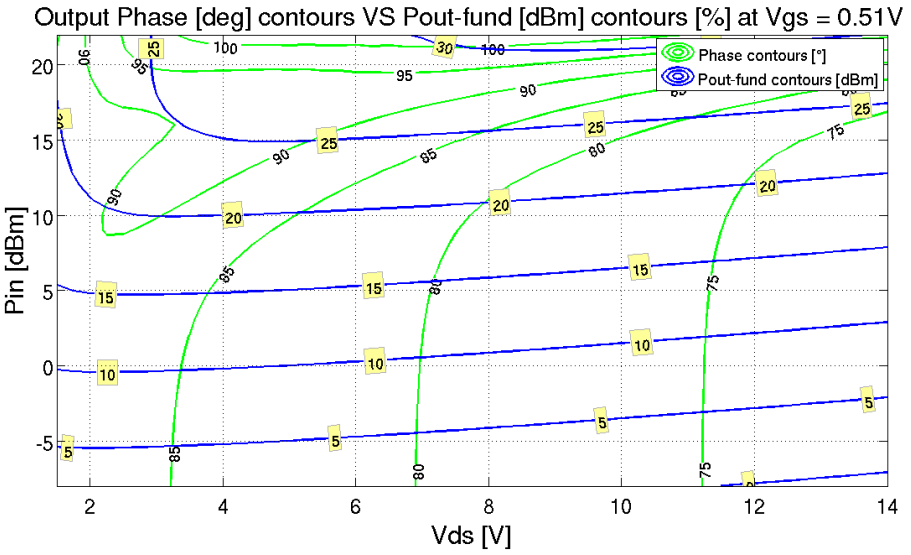

Figure 5.9: Slice at $Vgs = 0.51V$ with $Pout$ and Output Phase contours

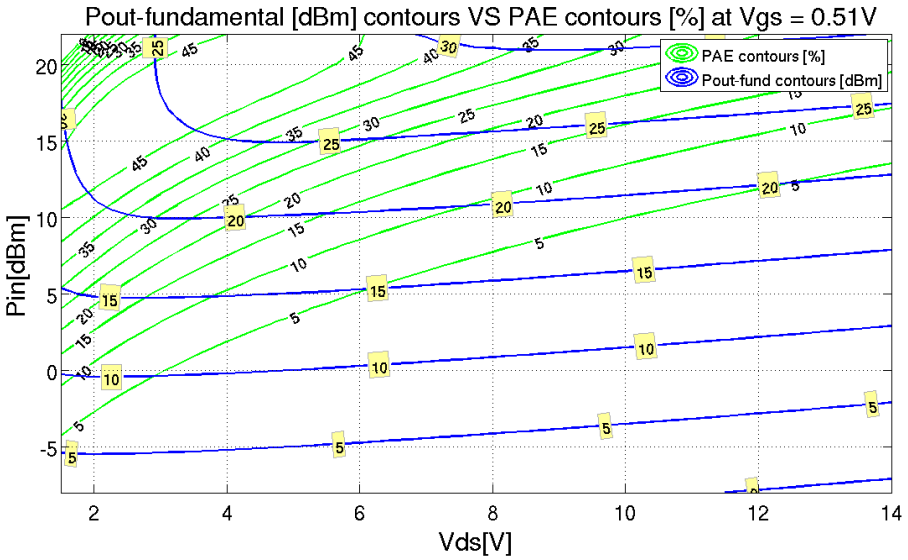

Figure 5.10: Slice at $Vgs = 0.51V$ with $Pout$ and PAE contours

5.4 Cost function weights

The results presented later have been found with the Ω cost function weights shown in Table 5.2 (see Section 3.2.4). Once more, the second harmonic distortion is not considered ($w_\delta = 0$).

Coefficient	Final value
w_α	1/5
w_β	1/5
w_γ	1/5
w_δ	0
w_ϵ	1/5
w_d	1/5

Table 5.2: pHEMT amplifier path search, final Ω function weights

5.5 (Vgs,Vds,Pin) space distance normalization coefficients

The distance normalization coefficients (Section 3.2.4) listed in Table 5.3 have led to the final results.

Coefficient	Final value
Vgs_{NORM}	0.5
Vds_{NORM}	$9.5V$
Pin_{NORM}	$22dBm$

Table 5.3: pHEMT Amplifier path search, final distance normalization coefficients

5.6 Class A bias point

The pHEMT amplifier is finally evaluated at its class A bias point ($Vgs = 0.71V$ and $Vds = 9V$).

5.7 Results

The final trajectory is presented together with its Matlab and ADS analysis.

5.7.1 Results in Matlab

- Bias trajectory in the (Vgs, Vds, Pin) space, Figure 5.11
- Bias trajectory in the transistor's I-V plane, Figure 5.12
- PAE as a function of $Pout$, Figure 5.13
- Transducer gain as a function of $Pout$, Figure 5.14
- Pin - $Pout$ plot, Figure 5.15
- Output phase as a function of $Pout$, Figure 5.16
- Vgs Control Function (Vgs as function of $Pout$), Figure 5.17
- Vds Control Function (Vds as function of $Pout$), Figure 5.18
- Second Harmonic Distortion, Figure 5.19
- Third Harmonic Distortion, Figure 5.20

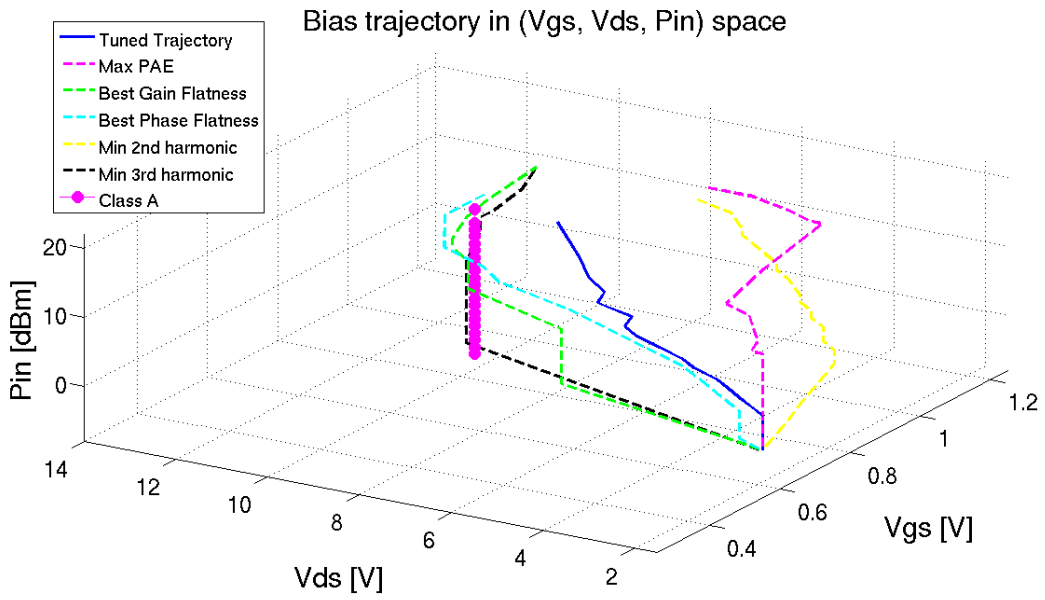

Figure 5.11: Trajectory in the (Vgs, Vds, Pin) space

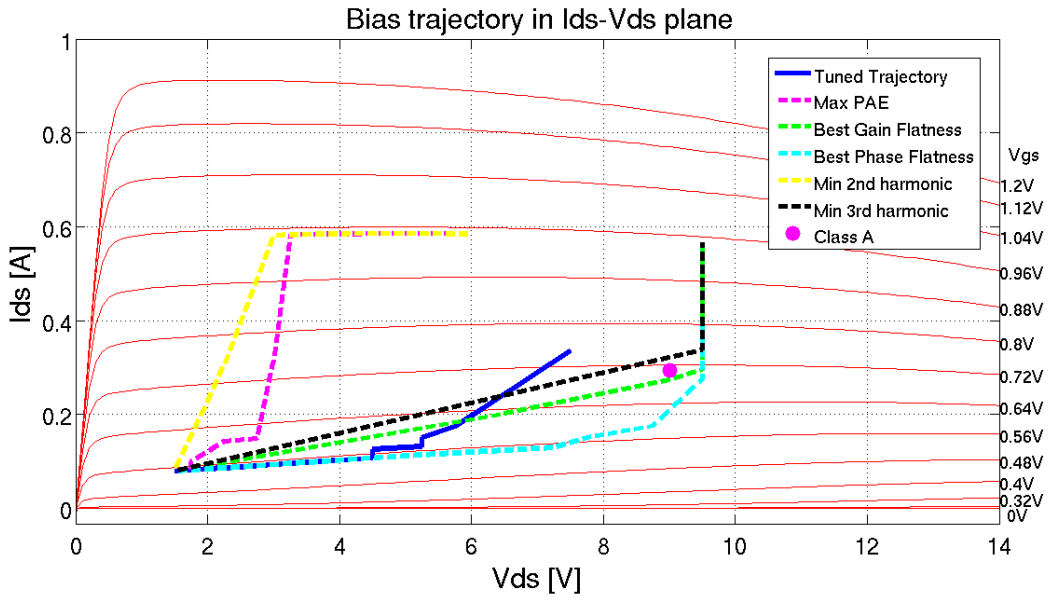

Figure 5.12: Trajectory in the pHEMT I-V plane

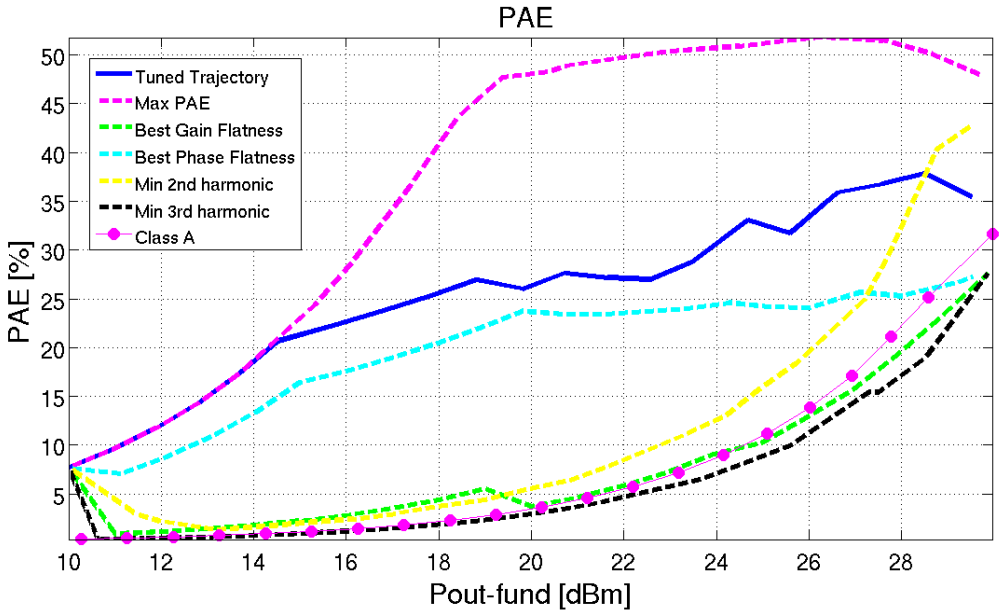

Figure 5.13: pHEMT Amplifier Path, Power Added Efficiency

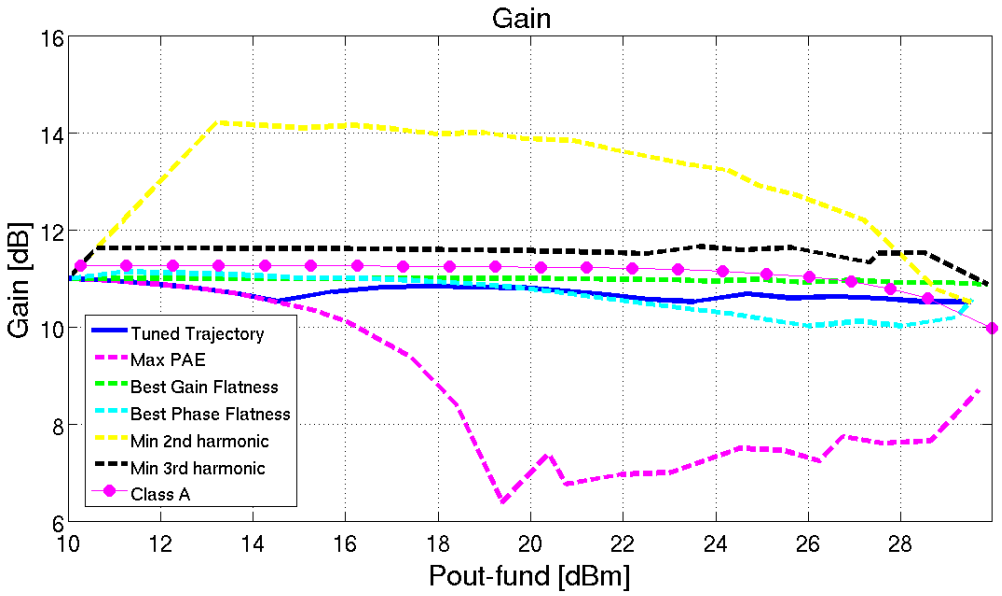

Figure 5.14: pHEMT Amplifier Path, Transducer Gain

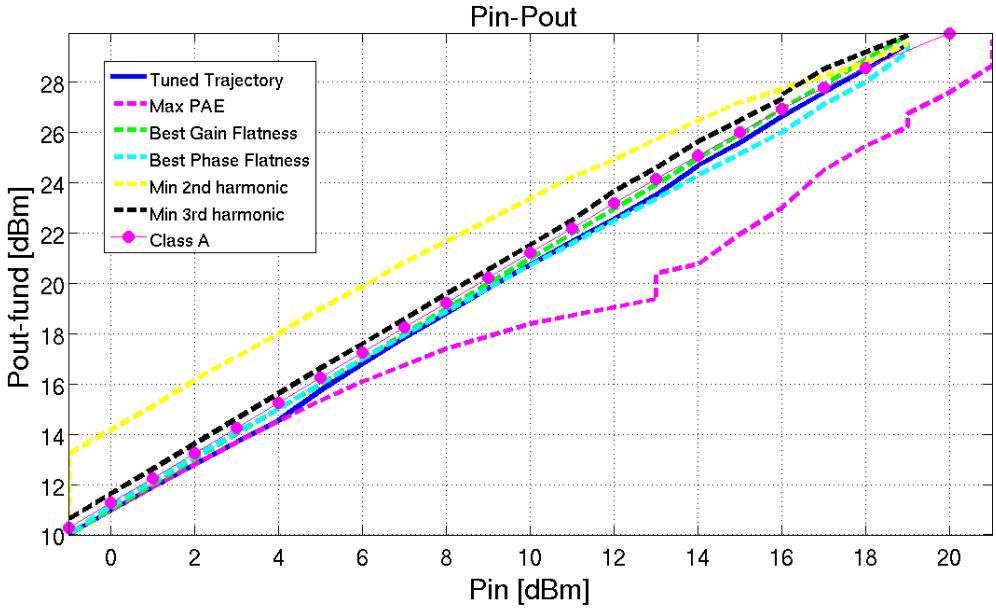

Figure 5.15: pHEMT Amplifier Path, $Pin - Pout$

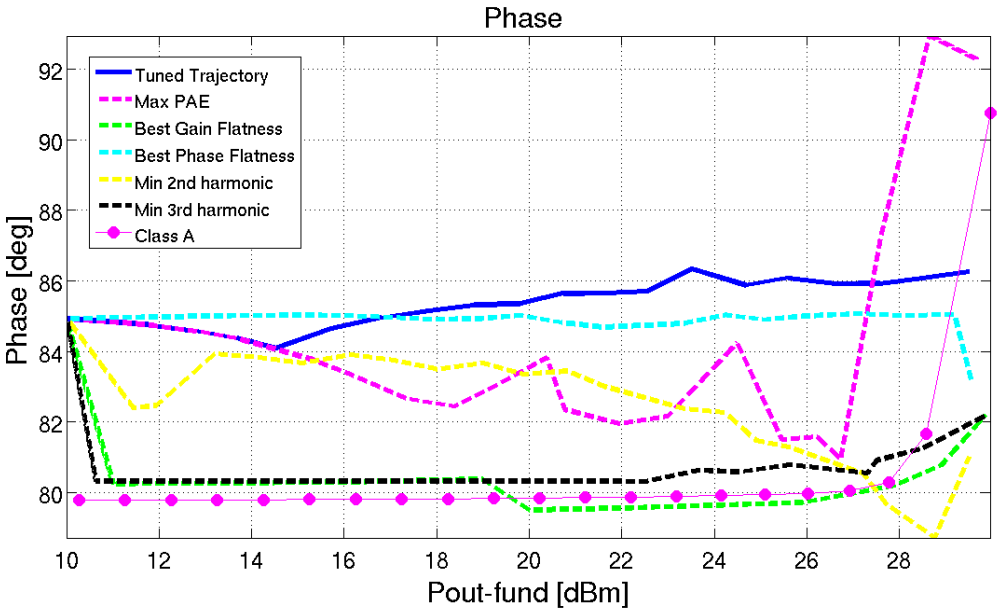

Figure 5.16: pHEMT Amplifier Path, Output Phase

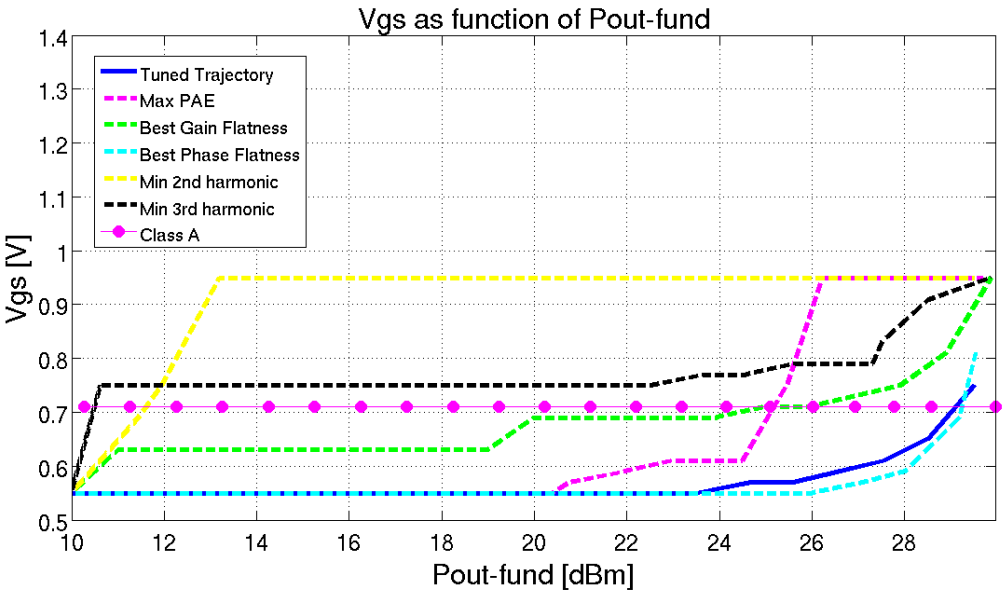

Figure 5.17: Vgs Control Function

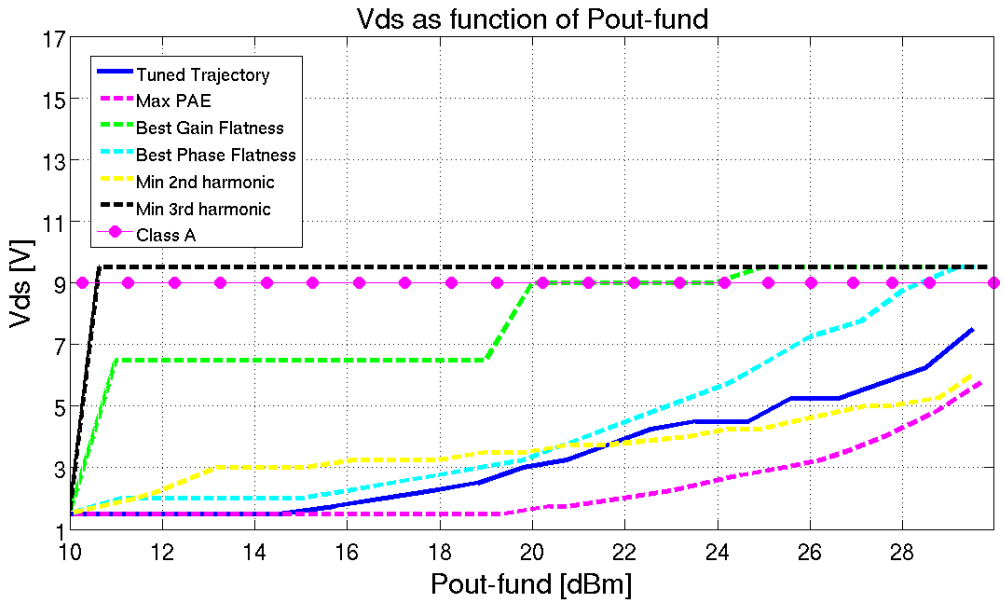

Figure 5.18: Vds Control Function

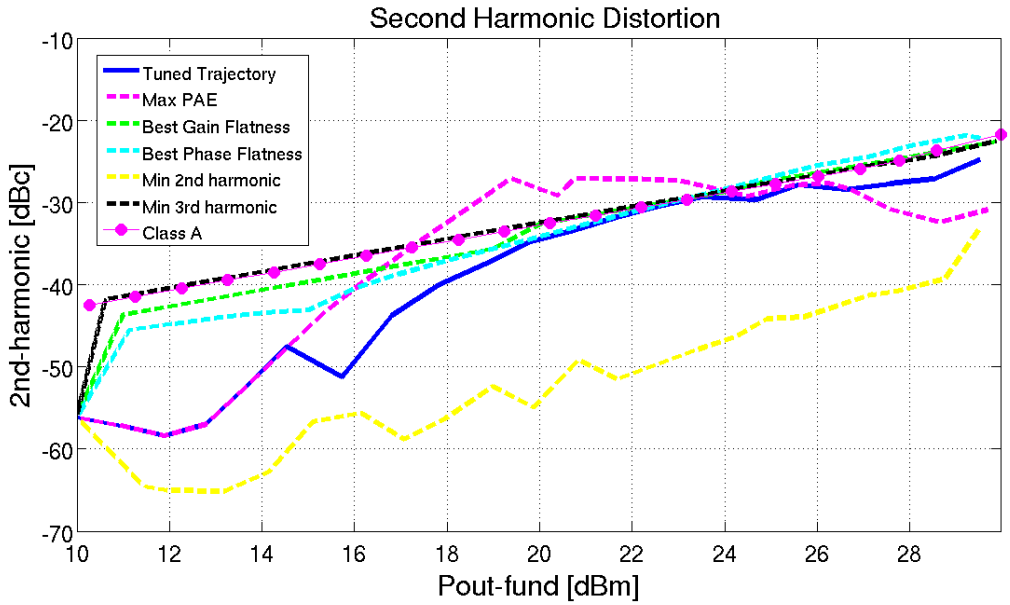

Figure 5.19: pHEMT Amplifier Path, Second Harmonic Distortion

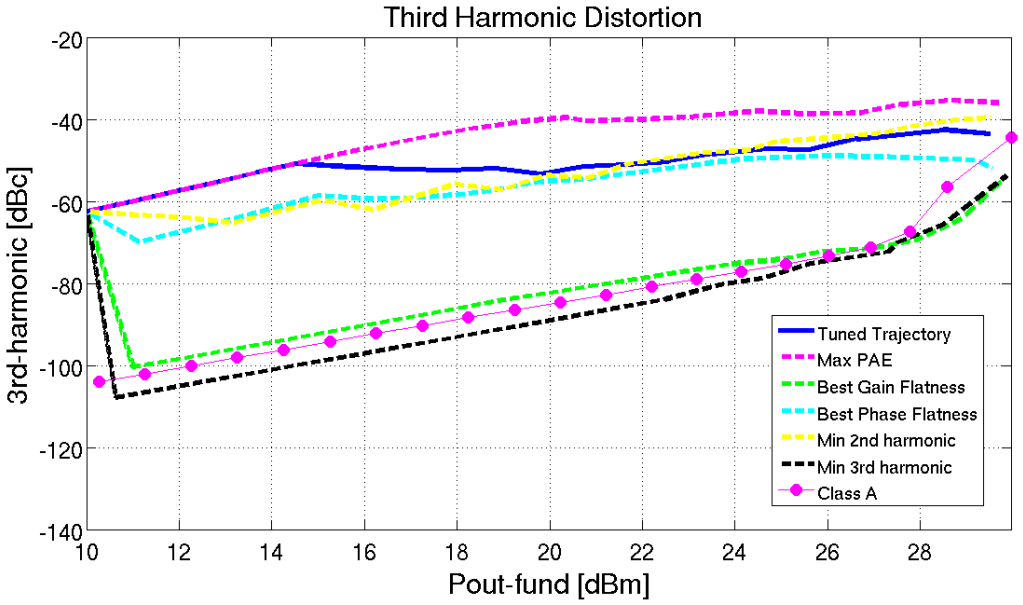

Figure 5.20: pHEMT Amplifier Path, Third Harmonic Distortion

5.7.2 Results in ADS

The amplifier is unconditionally stable at all the points of the tuned bias trajectory. Its S_{11} parameter is always lower than $-20dB$ while the S_{22} does not exceed $-10dB$. Therefore the device is well matched to 50Ω along all the path.

The dynamic load lines of the PA are plotted in Figure 5.21.

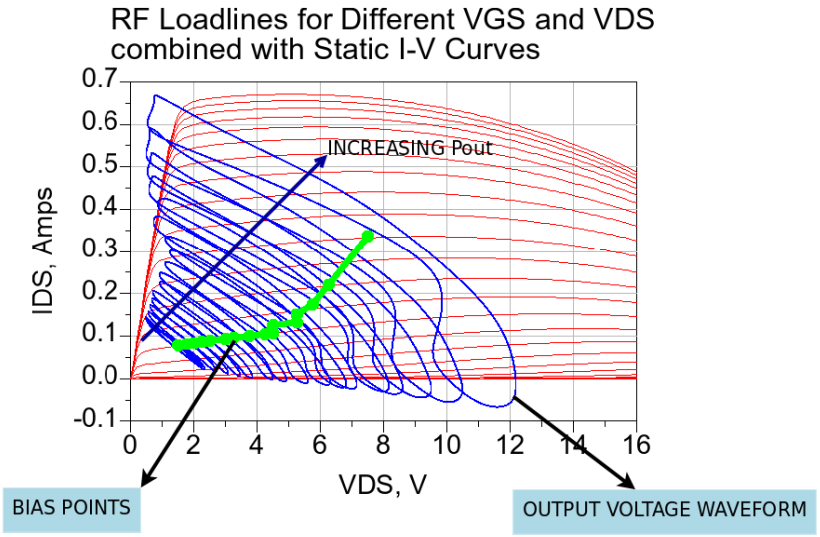

Figure 5.21: Bias points (green) and load lines (blue) of a dynamically biased class A pHEMT power amplifier for a 1-tone sinusoidal input

Finally, a two tones harmonic balance simulation is run along the path (at $6GHz$ with $10kHz$ of spacing). The following plots are shown:

- PAE as a function of $Pout$, both from one 1-tone and 2-tones simulations, Figure 5.22
- Transducer gain as a function of $Pout$, both from one 1-tone and 2-tones simulations, Figure 5.23
- Pin - $Pout$ plot, both from one 1-tone and 2-tones simulations, Figure 5.24
- Third order intermodulation products *versus* $Pout$, Figure 5.25
- Fifth order intermodulation products *versus* $Pout$, Figure 5.26

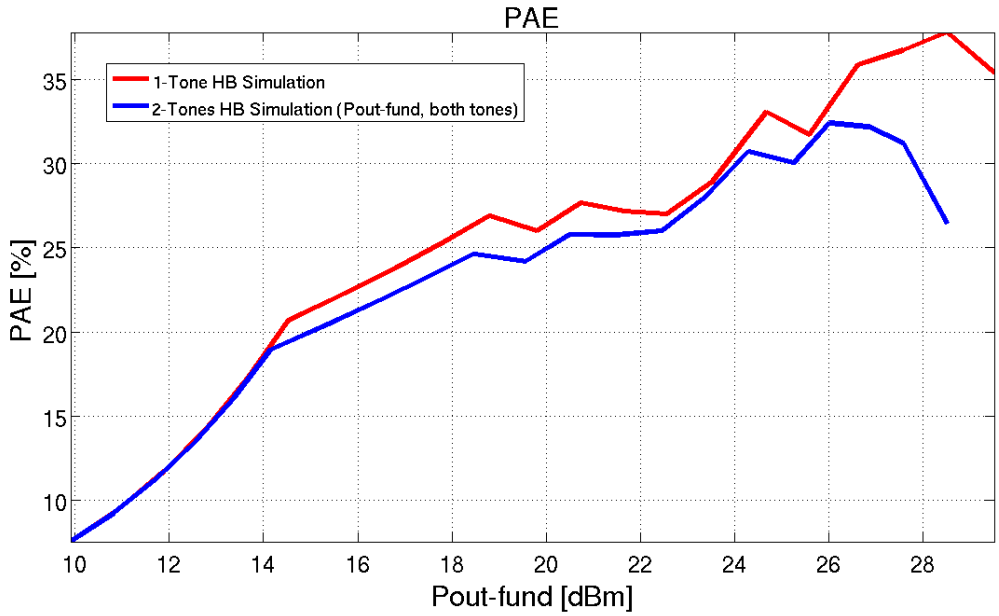

Figure 5.22: pHEMT Amplifier Path, 1-Tone *vs* 2-Tones PAE

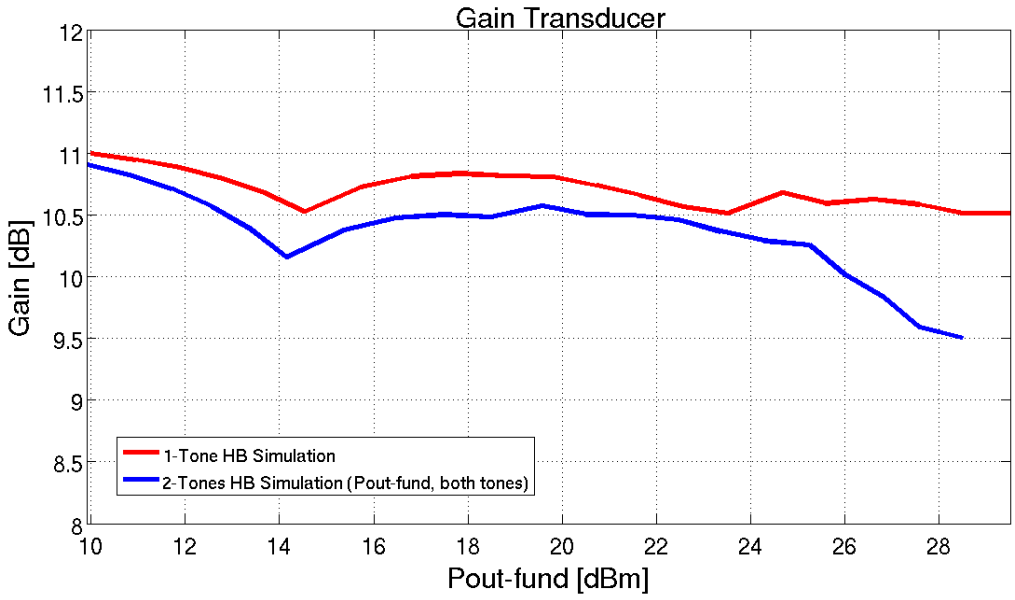

Figure 5.23: pHEMT Amplifier Path, 1-Tone *vs* 2-Tones transducer gain

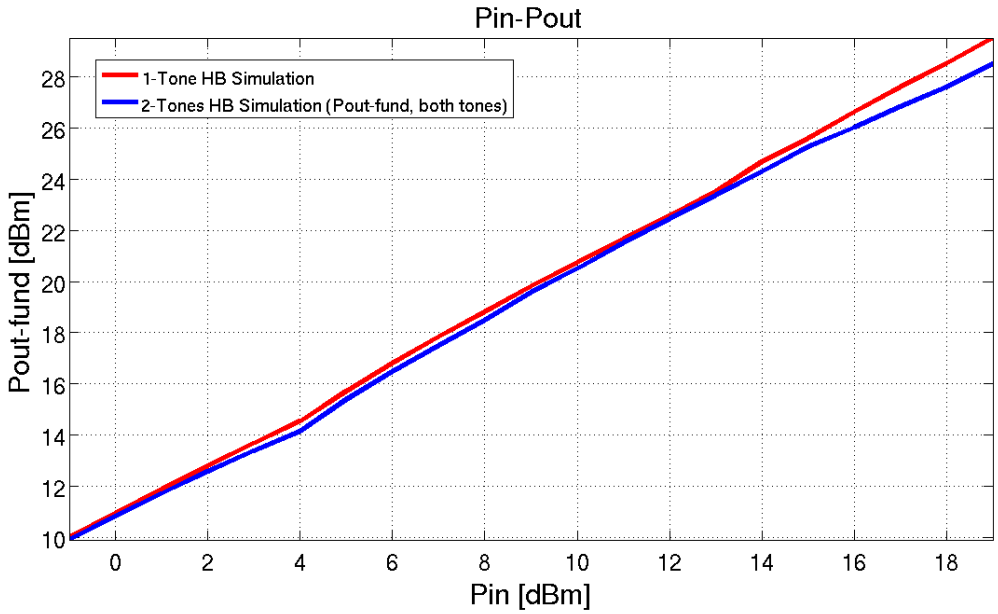

Figure 5.24: pHEMT Amplifier Path, 1-Tone *vs* 2-Tones Pin-Pout plot

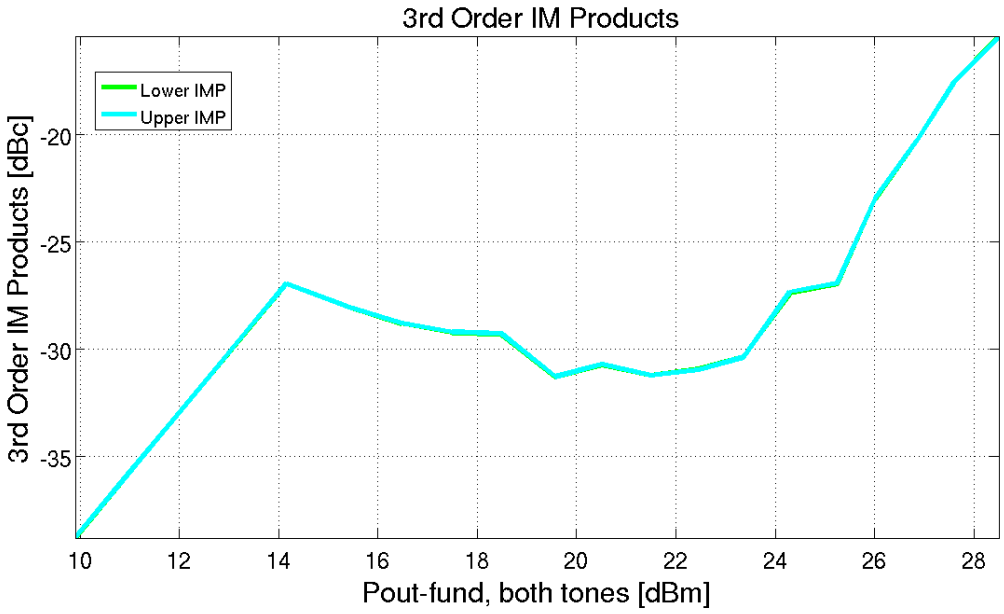

Figure 5.25: pHEMT Amplifier Path, 3rd order intermodulation products

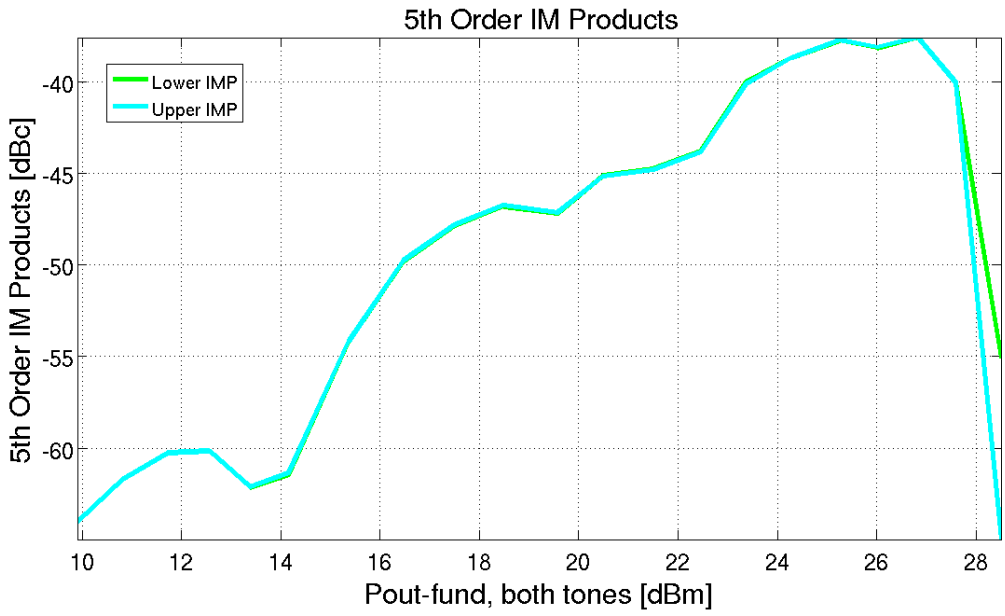

Figure 5.26: pHEMT Amplifier Path, 5th order intermodulation products

5.8 Comments

The tuned trajectory has an average PAE of 25.1%, while the class A average PAE is 7.8% (Figure 5.13). Once more, gain and output phase variations are limited: $0.5dB$ of maximum variation for the gain and $2.2°$ for the phase (see Figure 5.14 and Figure 5.16). Furthermore, Vgs and Vds do not have complicated control functions (Figure 5.17 and Figure 5.18).

Compared to the HBT, harmonic distortion is here definitely lower: the second harmonic reaches $-25dBc$ (Figure 5.19) and the third one $-43dBc$ (Figure 5.20). This happens because the amplifier has a matching network in low pass configuration at its output. The network partially reflects the harmonics back, thus they appear as attenuated. The attenuation varies with frequency (the third harmonic is reflected more than the second one), but does not vary with the evaluated (Vgs, Vds, Pin) point. Therefore, the PA's output harmonics can be still considered as valid indexes of non linearity and should be kept as low as possible.

According to the two tones ADS simulation, at high $Pout$, the third order IMP grow up to $-15dBc$ and the fifth order IMP to $-38dBc$ (Figure 5.25 and Figure 5.26). The third order intermodulation products are high, but, as explained in Section 4.8, they could be dramatically lower, since the PA will not always deliver the highest output power and usually a digital predistortion system is used.

Figure 5.22 and Figure 5.23 show how the IMP affects the amplifier's PAE and transducer gain. Data from a one tone and a two tone simulation (frequency spacing of $10kHz$) are compared. With two tones at the input, the gain is up to $1dB$ smaller and the average power added efficiency drops to 22.8%. These differences might shrink in case the tricks described above are used.

In Figure 5.17, Figure 5.18 and Figure 5.21 one can notice that the device works as a class A for low $Pout$. As soon as the output power increases, distortion increases as well and the system moves its bias point. First only Vds varies. For high $Pout$ levels Vgs changes as well (see Appendix C).

The load lines (Figure 5.21) are not straight lines because the amplifier is connected to a slightly capacitive impedance and because non linear effects arise in saturation and interdiction. The drain-source current is under its peak limit of $691.2mA$ at maximum $Pout$ and Vds does not reach values that can cause a drain-gate breakdown.

Finally, the best phase flatness path is worth mentioning. It has a lower average PAE (19.8%, see Figure 5.13) but the third order harmonic distortion is smaller (Figure 5.20), and it can be shown in ADS that intermodulation products are slightly lower.

Chapter 6

Measurements and Conclusions

In Chapter 4 the algorithm has been applied to a HBT transistor and a bias trajectory has been identified. Then, the device has been tested in the laboratory and the path evaluated.

In the following chapter measurements are described and results commented. For each of the trajectory bias points the following static measurements are executed: DC measurements, one tone measurements and two tones measurements. Power added efficiency, gain, harmonic distortion and intermodulation products are all experimentally estimated while phase measurements could not be performed.

To measure the phase difference between the HBT's input and output the reference sections of the instruments should be exactly the transistor's base and collector. The HBT under test is actually an integrated device and a probe station is used to connect the signal generator and the RF analyzer (Figure 6.2 and Figure 6.3). There are many discontinuities and the probes do not lay down exactly on the transistor's terminals but short lines are present, therefore direct phase measurements are unfeasible. Indirect measurements through QAM modulated signals could be performed in the future (the rotation of the constellation can be estimated).

6.1 Measurement setup

An automated measuring system is used (Figure 6.1). It combines the Rhode & Schwarz SMU200A vector signal generator, the Rhode & Schwarz FSQ40 signal analyzer and the Agilent E5270A configurable measurement mainframe with multiple DC bias sources. A probe station carries the microwave integrated circuit and its cables connect the device's base to the signal generator and the device's collector to the analyzer. The transistor is fed by the Agilent power supply through two wideband ($1Ghz - 12.4GHz$) Hewlett-Packard HP11590A bias tees. A bias tee basically contains a coil and a capacitor. The coil works as a RF choke while the capacitor is a DC block. The HBT's emitter is tied to ground through a VIA on the chip itself.

All the instruments are connected into a GPIB network and are remotely operated from a personal computer. Therefore, measurements are highly automated. Simple Matlab scripts can first configure the instrumentation and then read, process and plot the measured data.

Figure 6.1: Measurement setup in the Microwave Laboratory

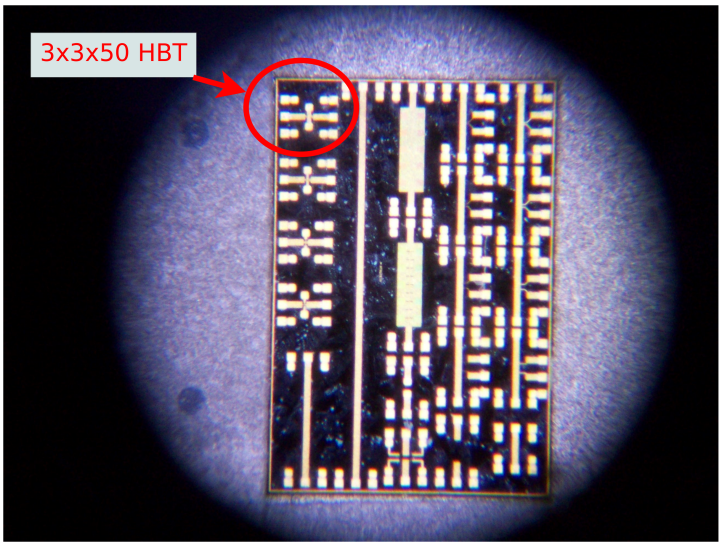

Figure 6.2: NTNU107A Monolithic Microwave Integrated Circuit Overview

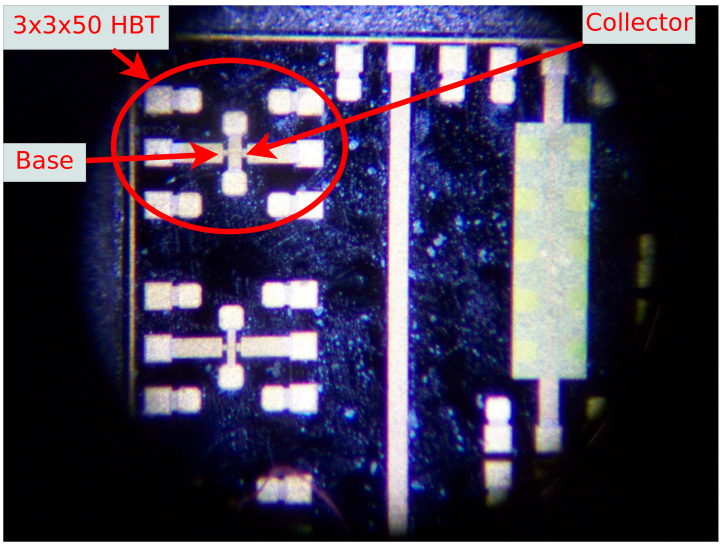

Figure 6.3: The HBT under test

6.2 Losses

Cables and bias tees losses have been measured at the base side as well as at the collector side. In both cases, the tip of the probe has been connected to a short present on the microchip and the reflection coefficient measured with a calibrated Hewlett-Packard 8510C network analyzer. Assuming the short as ideal, the measured return loss is twice the connection loss.

At the base side, losses have been measured only at the fundamental frequency ($1.9Ghz$) while the collector connection losses have been measured at the fundamental frequency ($1.9Ghz$), at the second harmonic ($3.8GHz$) and at the third harmonic ($5.7GHz$).

Losses are compensated in Matlab. The software increases the power level the generator delivers, hence compensating the base connection attenuation. The attenuation at the collector side is compensated by simply adding the measured losses to the magnitudes the analyzer reads at different frequencies. Measured losses are listed in Table 6.1.

	$1.9GHz$	$3.8GHz$	$5.7GHz$
BASE Side	1.86dB		
COLLECTOR Side	1.71dB	2.73dB	2.76dB

Table 6.1: Base and collector connections losses at different frequencies

The power supply compensates the DC losses between the instrument and the DC switchboard through its sense terminals. DC losses that occur between the switchboard and the transistor are non considered relevant, therefore they have not been measured.

6.3 DC measurements

Simple DC measurements for each of the trajectory bias points are executed. First, the Ib current and the Vce voltage are set and read back. Afterwords, the Vbe voltage as well as the Ic current are measured.

Table 6.2 shows the independent Ib and Vce variables. The ideal values the supply is supposed to deliver can be compared with the actual voltages and currents the device gives.

$Index$	Ib $Ideal$ (A)	Ib $Measured$ (A)	Vce $Ideal$ (V)	Vce $Measured$ (V)
1	1.2000E-04	1.2005E-04	1.5000	1.5004
2	1.2000E-04	1.2005E-04	1.5000	1.5002
3	1.2000E-04	1.2005E-04	1.5000	1.5002
4	1.2000E-04	1.2005E-04	1.5000	1.5002
5	1.2000E-04	1.2005E-04	1.5000	1.5004
6	1.2000E-04	1.2005E-04	1.5000	1.5005
7	1.2000E-04	1.2005E-04	1.5000	1.5002
8	1.2000E-04	1.2005E-04	1.5000	1.5004
9	1.2000E-04	1.2005E-04	1.5000	1.5004
10	1.2000E-04	1.2005E-04	1.7500	1.7503
11	1.5000E-04	1.5005E-04	1.7500	1.7503
12	1.5000E-04	1.5010E-04	1.7500	1.7503
13	1.8000E-04	1.8010E-04	2.0000	2.0002
14	1.8000E-04	1.8010E-04	2.0000	2.0002
15	2.1000E-04	2.1005E-04	2.2500	2.2510
16	2.4000E-04	2.4005E-04	2.5000	2.5000
17	2.4000E-04	2.4005E-04	2.5000	2.5000
18	2.7000E-04	2.7000E-04	2.7500	2.7500
19	3.0000E-04	2.9995E-04	3.0000	3.0000
20	3.3000E-04	3.3000E-04	3.2500	3.2500
21	3.6000E-04	3.6000E-04	3.7500	3.7510

Table 6.2: Ib and Vce, DC measurements

Table 6.3 shows the dependent Ic and Vbe variables. Values from the DC simulations can be compared with the measured ones.

$Index$	Ic $Simulated$ (A)	Ic $Measured$ (A)	Vbe $Simulated$ (V)	Vbe $Measured$ (V)
1	0.0157	0.0150	1.3058	1.3009
2	0.0157	0.0151	1.3058	1.3004
3	0.0157	0.0151	1.3058	1.3005
4	0.0157	0.0151	1.3058	1.3004
5	0.0157	0.0150	1.3058	1.3006
6	0.0157	0.0150	1.3058	1.3005
7	0.0157	0.0151	1.3058	1.3006
8	0.0157	0.0151	1.3058	1.3007
9	0.0157	0.0151	1.3058	1.3007
10	0.0156	0.0151	1.3045	1.2903
11	0.0197	0.0191	1.3105	1.3049
12	0.0197	0.0191	1.3105	1.3049
13	0.0235	0.0233	1.3136	1.3013
14	0.0235	0.0231	1.3136	1.3069
15	0.0274	0.0271	1.3153	1.3076
16	0.0311	0.0311	1.3160	1.3064
17	0.0311	0.0311	1.3160	1.3066
18	0.0349	0.0350	1.3157	1.3041
19	0.0386	0.0388	1.3146	1.3006
20	0.0422	0.0426	1.3127	1.2957
21	0.0455	0.0459	1.3070	1.2849

Table 6.3: Ic and Vbe, DC measurements

6.4 One tone measurements

Many samples of the same MMIC are available at the laboratory. Therefore, one tone measurements are performed twice on each of two samples. Results are then averaged for each device and an overall mean is calculated afterwords.

A procedure is followed when executing measurements: first the bias point is set, then the RF signal is applied and finally the harmonics at the output are measured. In this way, uncertain states are avoided. Moreover, some delays are used to make sure the measurements are taken when the amplifier is in a steady-state condition. The following plots compare one tone measurements with data from simulations:

- PAE as a function of $Pout$, Figure 6.4
- Transducer gain as a function of $Pout$, Figure 6.5
- Pin - $Pout$ plot, Figure 6.6
- Second Harmonic Distortion, Figure 6.7
- Third Harmonic Distortion, Figure 6.8

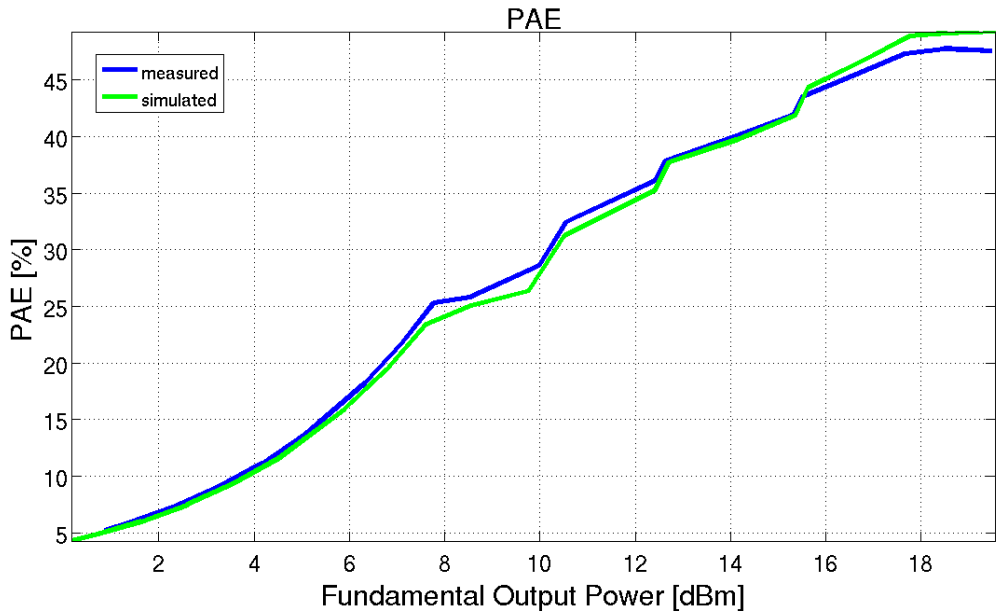

Figure 6.4: One tone measurements, Power Added Efficiency

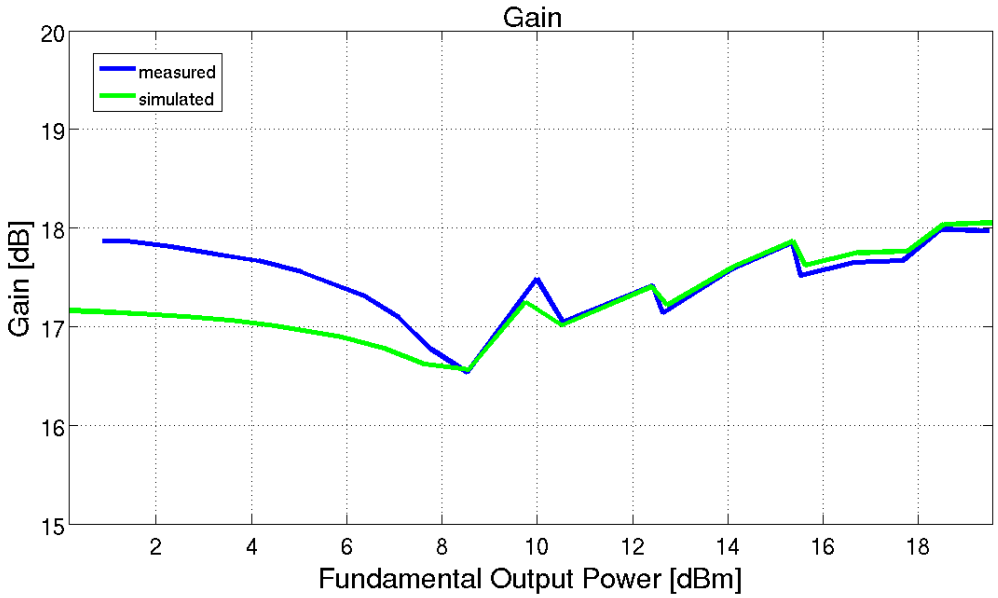

Figure 6.5: One tone measurements, Transducer Gain

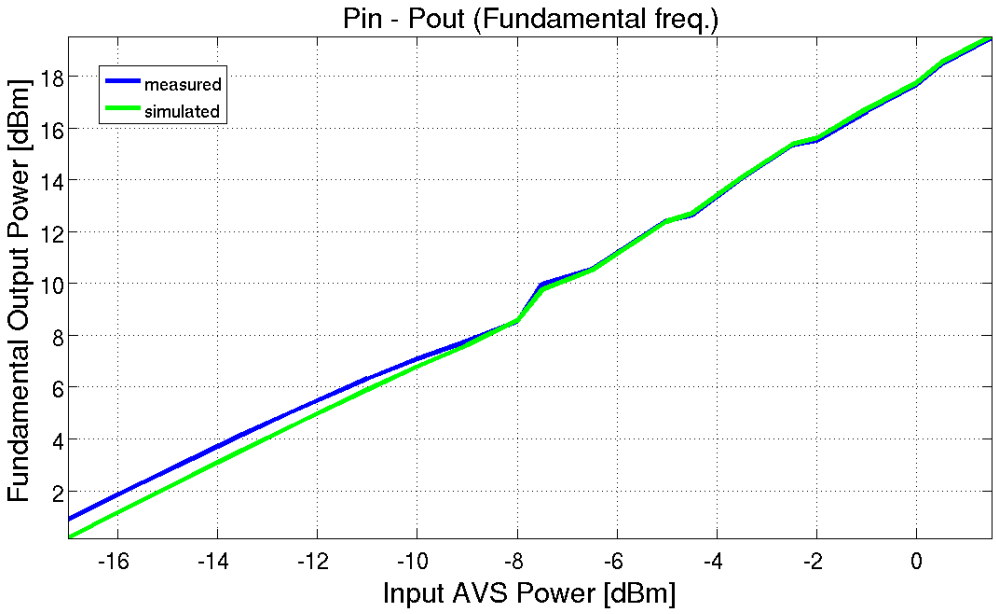

Figure 6.6: One tone measurements, *Pin - Pout*

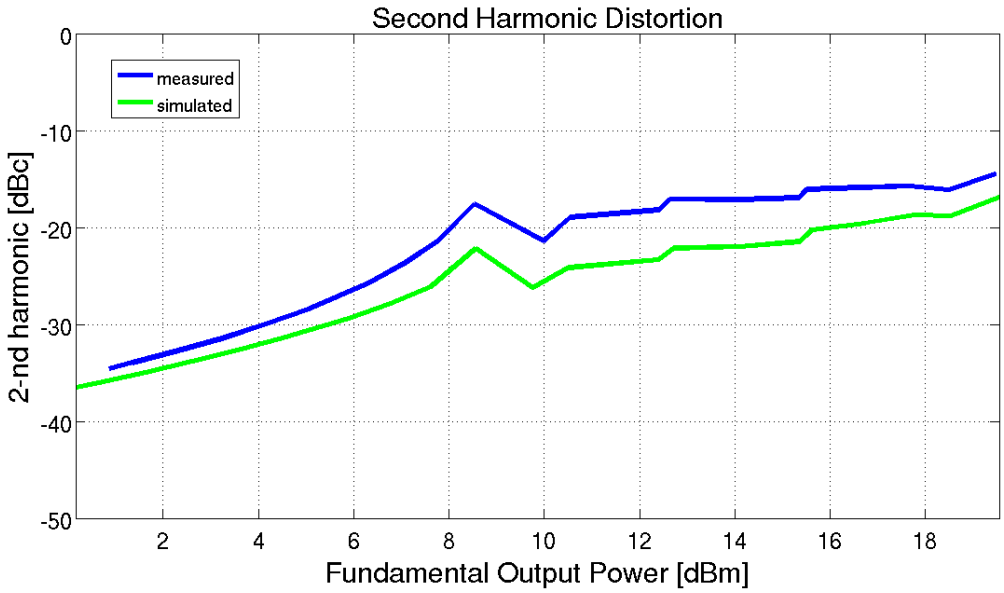

Figure 6.7: One tone measurements, Second Harmonic Distortion

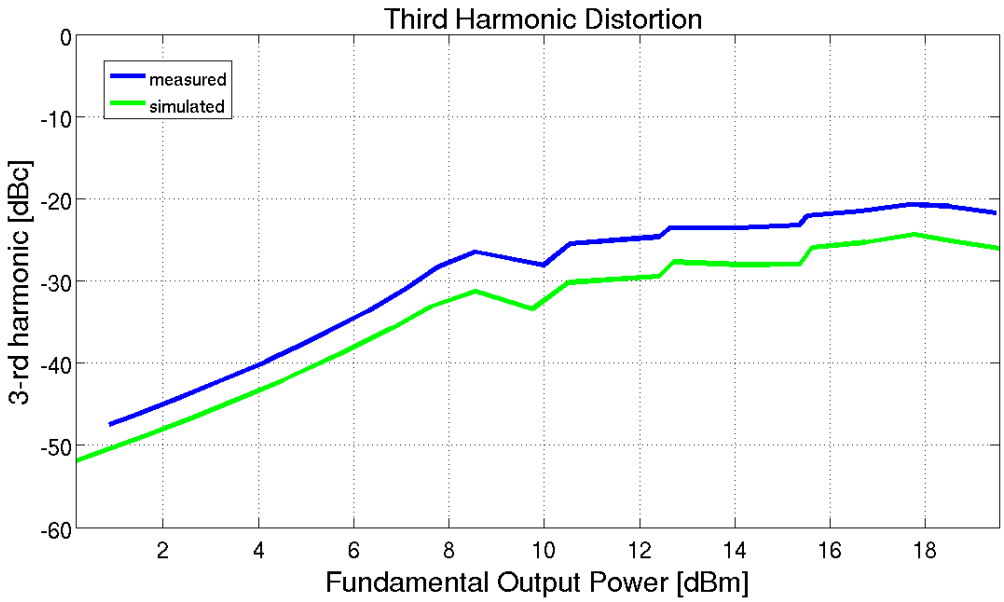

Figure 6.8: One tone measurements, Third Harmonic Distortion

6.5 Two tones measurements

As before, the two tones measurements are executed twice on each of the two samples. Results are then averaged.

The same procedure as in Section 6.4 is followed: first the bias point is set, then the RF signal is applied and finally the tones at the output are measured.

When two tones are present at the input, the second order non linearities produce very low frequency signals the DC choke can not stop (few kHz). These tones, when high, do not allow the power supply to measure the correct DC currents and voltages (power added efficiency has to be estimated). Therefore, Matlab takes many samples of the supplied currents and voltages and calculates their average values.

The following plots compare the two tones measurements with the two tones simulations:

- PAE as a function of $Pout$, Figure 6.9
- Transducer gain as a function of $Pout$, Figure 6.10
- Pin - $Pout$ plot, Figure 6.11
- Third order intermodulation products *versus* $Pout$, Figure 6.12
- Fifth order intermodulation products *versus* $Pout$, Figure 6.13

In addition, the plots listed below compare some two tones and one tone measurements:

- PAE as a function of $Pout$, both from one 1-tone and 2-tones measurements, Figure 6.14
- Transducer gain as a function of $Pout$, both from one 1-tone and 2-tones measurements, Figure 6.15
- Pin - $Pout$ plot, both from one 1-tone and 2-tones measurements, Figure 6.16

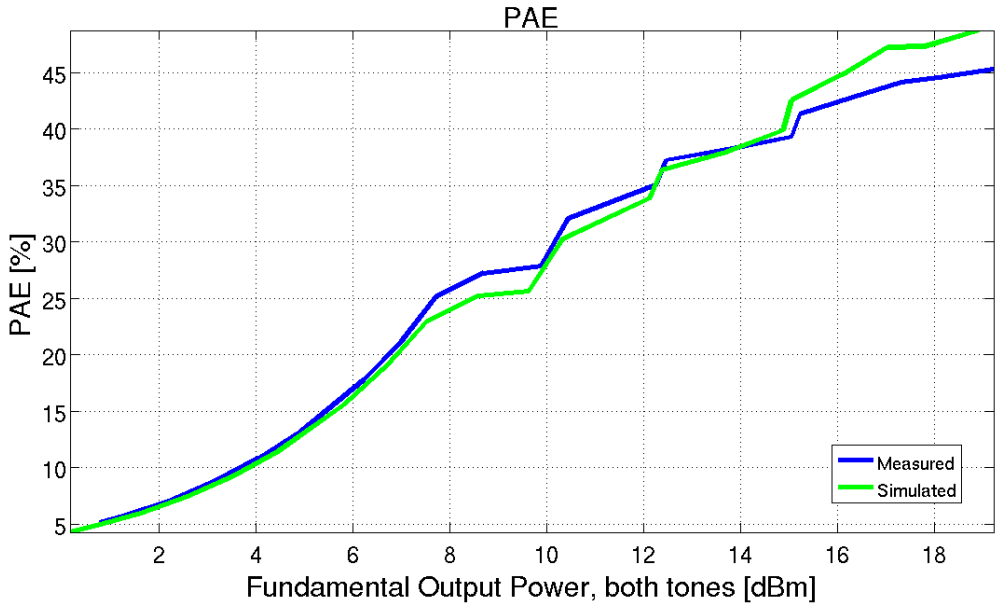

Figure 6.9: Tow tones measurements, Power Added Efficiency

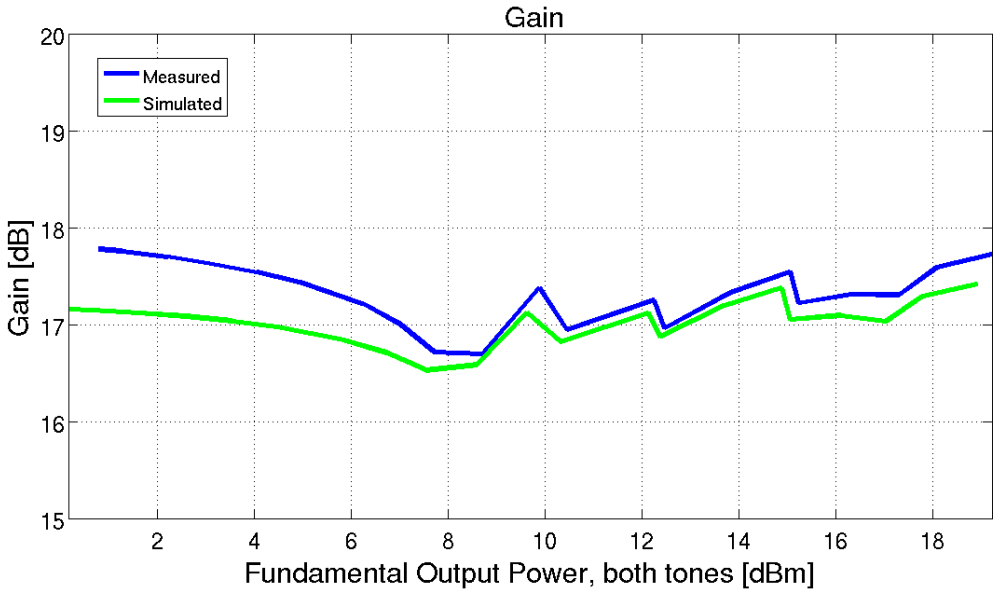

Figure 6.10: Tow tones measurements, Transducer Gain

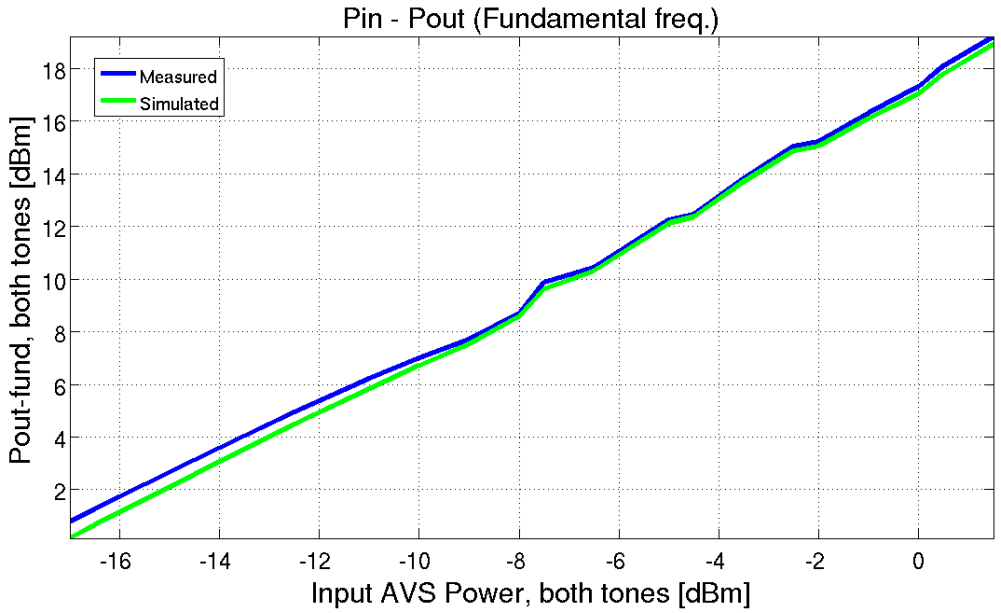

Figure 6.11: Tow tones measurements, *Pin - Pout*

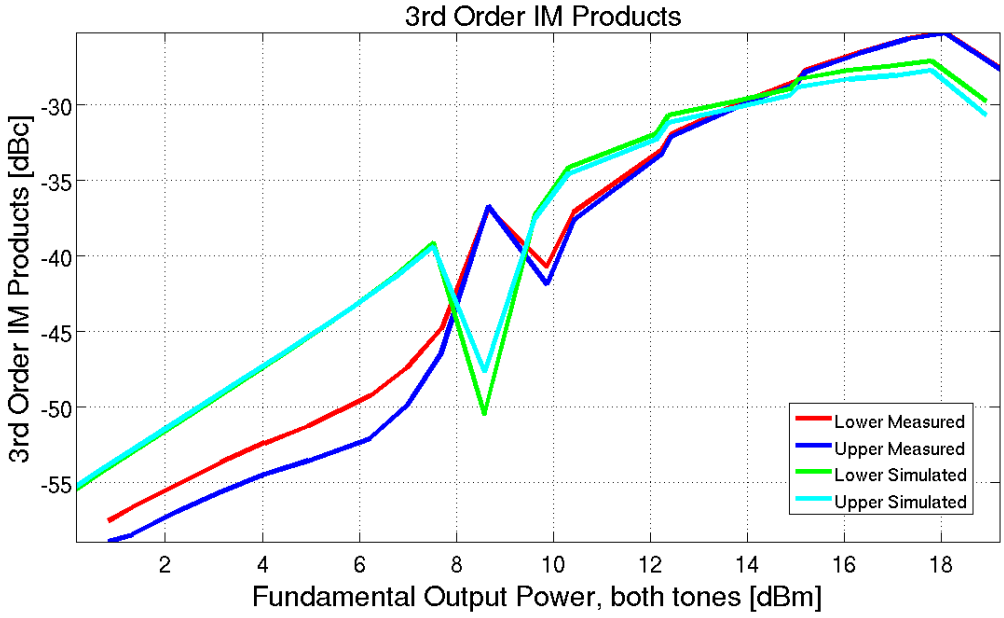

Figure 6.12: Tow tones measurements, Third Order Intermodulation Products

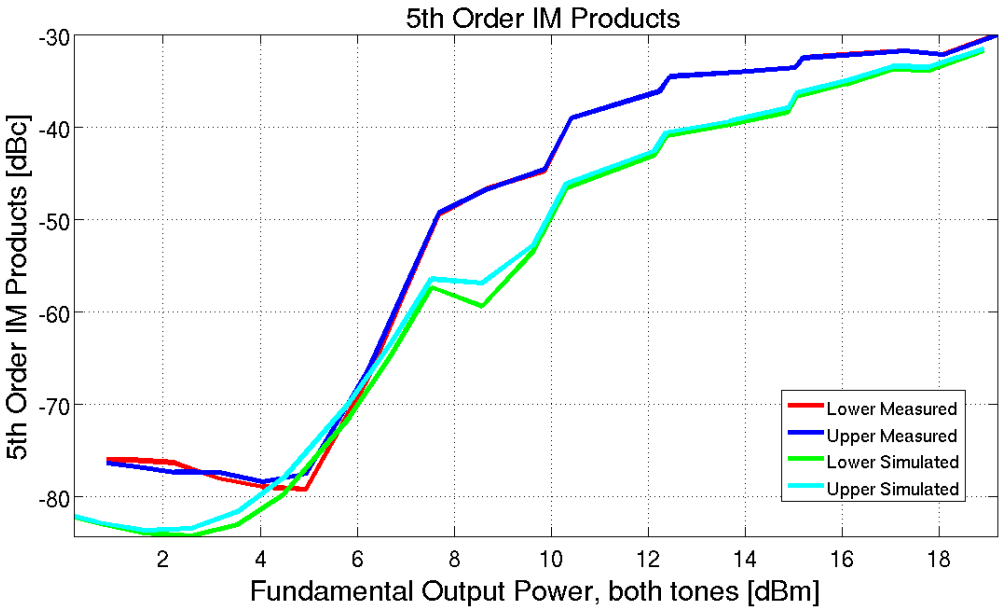

Figure 6.13: Tow tones measurements, Fifth Order Intermodulation Products

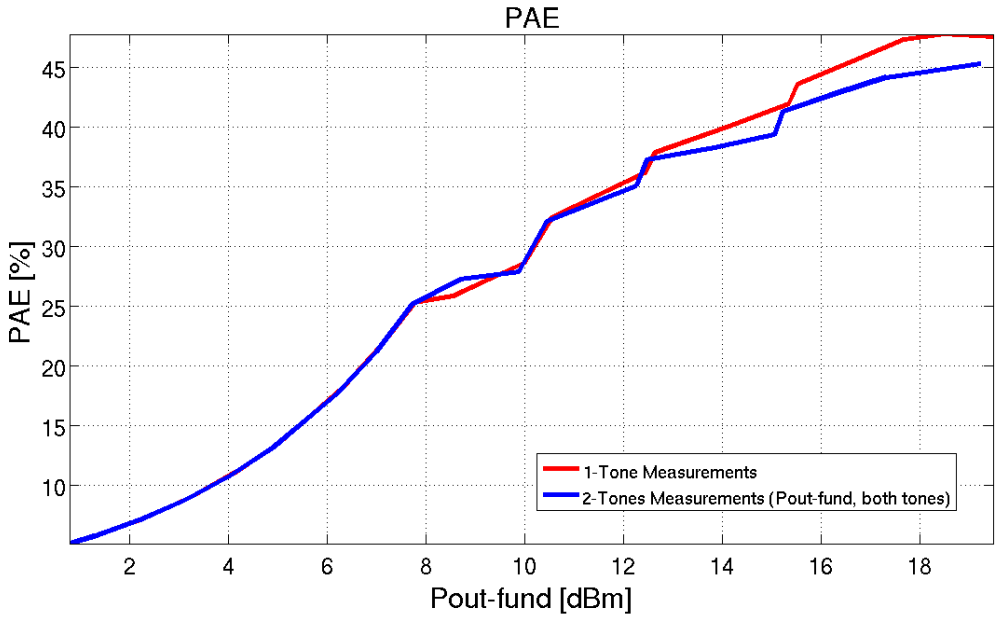

Figure 6.14: One tone measurements *vs* two tones measurements: PAE

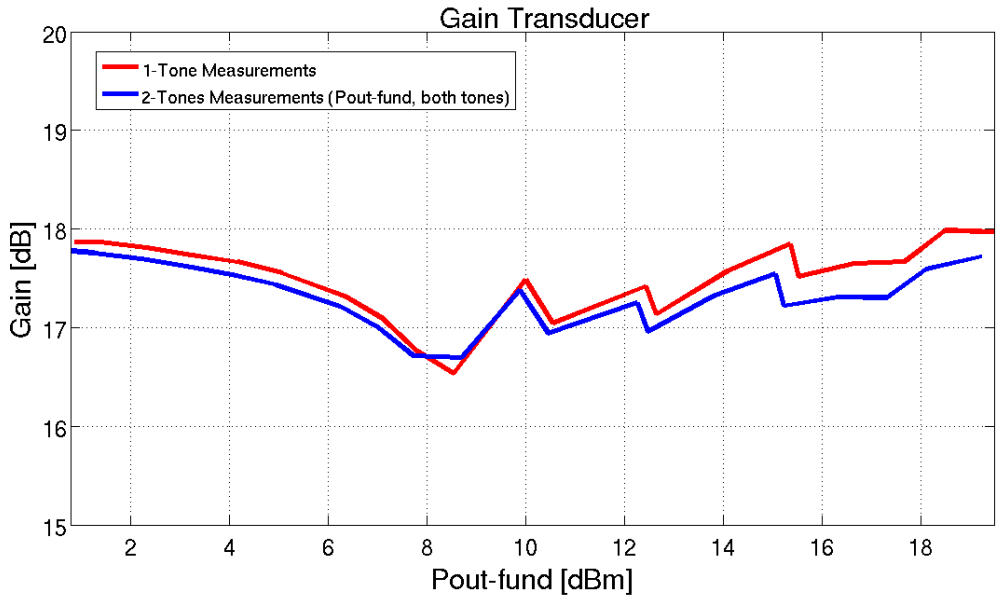

Figure 6.15: One tone measurements *vs* two tones measurements: transducer gain

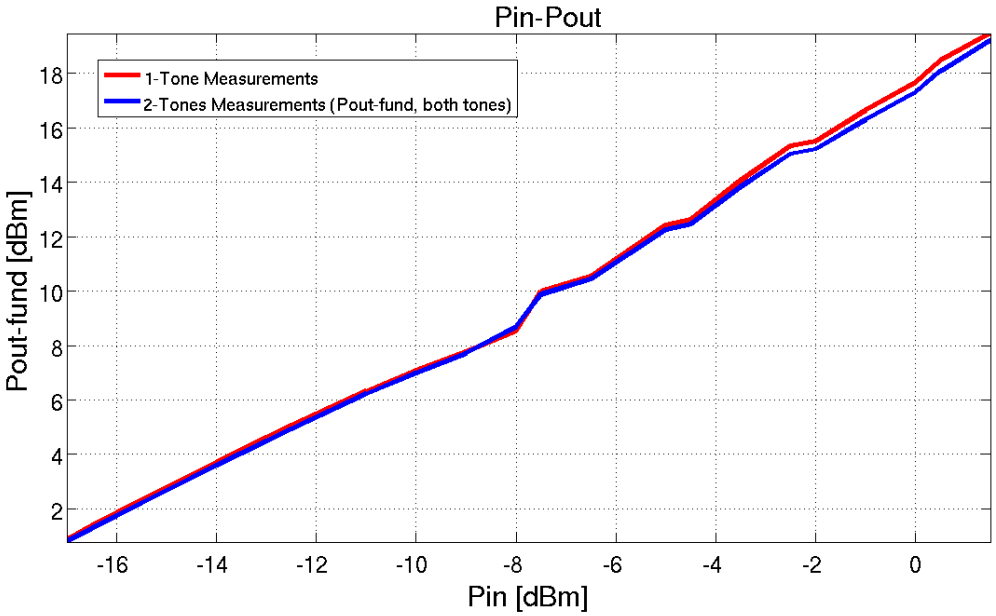

Figure 6.16: One tone measurements *vs* two tones measurements: Pin-Pout plot

6.6 Comments

Measurements show very good agreement with simulations. There are no big discrepancies and only the harmonics are higher than expected. The second harmonic reaches $-14.5dBc$ while the third one $-21dBc$ (see Figure 6.7 and Figure 6.8). Nevertheless, the ADS transistor model, although a relatively simple one, describes the device very well. The fact that two different samples of the same device have been tested and very similar results have been obtained confirms that.

The measured average PAE (Figure 6.4) of the tuned trajectory is 28.2%, which is even higher than what expected (27.5%). The measured gain is a bit higher at the beginning but its maximum variation is, as expected, limited within $1.4dB$ (Figure 6.5).

The intermodulation products (Figure 6.12 and Figure 6.13) behave mostly as ADS predicted. The third order IMP do not exceed $-25dBc$ and the fifth order IMP reach $-30dBc$. Once more, this values are acceptable since the dynamic range of the modulated signal is defined by its probability distribution function (Figure 1.1 and Figure 1.2), hence the PA will not always deliver the highest $Pout$. Therefore, the intermodulation products should be lower. Yet, a DPD system could decrease the ACPR even more [12].

When two tones are present at the input, the average PAE drops to 27.1% (Figure 6.14) and the measured gain is at most $0.4dB$ lower then before (Figure 6.15). This differences are not relevant.

6.7 Conclusions and Future Developments

Experimental results show that the tool developed in this thesis can increase the efficiency of class A power amplifiers dramatically and limit their non linearities. Furthermore, a very efficient bias path for a pHEMT amplifier has been found as well (Chapter 5) and the analysis perforemed in both the cases (HBT and pHEMT) are conceptually identical. Therefore, a general dynamic bias method could be defined since the presented concepts, analysis methods and implementation algorithms are consistent.

As a further step, the Ib and Vce control functions (Figure 4.18 and Figure 4.19) should be interpolated and hence give a continuous bias path. Since the functions are quite simple, second or third order polynomials could interpolate them without big errors. Low order polynomials ease bandwidth requirements for envelope amplifiers

(EA or DC/DC converters). The new continuous path could have slightly different characteristics but may ease gain and phase variations giving smoother functions that can be easily treated by DPD algorithms.

A complete dynamic bias system could be built once a continuous path is defined and a DPD system chosen. In this way the dynamic behavior of the amplifier can be assessed and memory effects (if any) estimated. Moreover, one could think of applying the PA analysis here presented and develop an adaptive dynamic bias system if a feedback line measures the output of the PA and allows the modulator to compare it with the desired signal.

Appendix A

Example of how to use the mdif class

The Matlab script below shows how to use the `mdif` class to transfer data from ADS to Matlab, process them and save the matrices in a compact `mat` file.

```
%% convert.m
%
% Author: Caharija Walter (NTNU - Norway, University of Trieste - Italy)
% Last Revision: 31/03/09
%
% ================================================
% the following script reads an ADS mdif file (.mdf)
% as a mdif object, calculates relevant circuit
% parameters and stores them into a .mat file
%
% mdif class used!!!
% ================================================


%% Set up
clear all


%% Input
% Input .mdf file name containing
% the mdif object to retrieve data from
```

```
infile_name = 'HBT3_3um_50um_ibb0_600vce0_25_7Pin-20_5fine0_5and0_5.mdf';
% Output .par (circuit parameters) file name
outfile_name = ...
    '../data/HBT3_3um_50um_ibb0_600vce0_25_7Pin-20_5fine0_5and0_5.par';


%% Read
A = mdif(infile_name);


%% Apply class methods and get some parameters
% Get Ib, Vce an Pin
Ib = A.Ib;
Vce = A.Vce;
Pin = A.Pin;

% Calculate PAE in both matrix formats (regular and mesh one) (%)
pae = PAE(A);
pae_mesh = PAE_mesh(A);

% Calculate OAE in both matrix formats (regular and mesh one) (%)
oae = OAE(A);
oae_mesh = OAE_mesh(A);

% Calculate output power at the fundamental frequency
% in both matrix formats (dBm)
Pfund_dBm = 10*log10(Pout_fund_W(A))+30;
Pfund_dBm_mesh = 10*log10(Pout_fund_W_mesh(A))+30;

% Calculate output power at the second harmonic in both
% matrix formats (dBm)
Psecond_dBm = 10*log10(Pout_second_W(A))+30;
Psecond_dBm_mesh = 10*log10(Pout_second_W_mesh(A))+30;

% Calculate output power at the third harmonic in both
% matrix formats (dBm)
```

```
Pthird_dBm = 10*log10(Pout_third_W(A))+30;
Pthird_dBm_mesh = 10*log10(Pout_third_W_mesh(A))+30;

% Calculate transduced power gain in both matrix formats (dB)
gain_t_dB = P_gain_transducer(A);
gain_t_dB_mesh = P_gain_transducer_mesh(A);

% Calculate output phase (deg)
phase_deg = phase(A);
phase_deg_mesh = phase_mesh(A);


%% Save as .par file
% -------------------------
% Use
%   load -mat outfile_name
% syntax when reading
% -------------------------
save(outfile_name, 'Ib', 'Vce', 'Pin', 'pae','pae_mesh', ...
    'oae', 'oae_mesh', 'Pfund_dBm','Pfund_dBm_mesh', ...
    'Psecond_dBm', 'Psecond_dBm_mesh', 'Pthird_dBm', ...
    'Pthird_dBm_mesh', 'gain_t_dB', 'gain_t_dB_mesh', ...
    'phase_deg', 'phase_deg_mesh');
```

Appendix B

HBT Tuned Path, Tables

Index	*First Harmonic* (*dBm*)	*Second Harmonic* (*dBc*)	*Third Harmonic* (*dBc*)	*PAE* (%)	*Gain Transducer* (*dB*)	*Output Phase* (*deg*)
1	0.162379	-36.575571	-51.951196	4.273113	17.162379	96.503153
2	0.653021	-36.042108	-50.925533	4.782604	17.153021	96.523001
3	1.630110	-34.953598	-48.828973	5.984532	17.130110	96.571046
4	2.600104	-33.828709	-46.668108	7.474768	17.100104	96.633646
5	3.560583	-32.655879	-44.436474	9.313280	17.060583	96.716106
6	4.508067	-31.418734	-42.123036	11.565620	17.008067	96.826263
7	5.892959	-29.387663	-38.462872	15.859733	16.892959	97.071085
8	6.779031	-27.861252	-35.865174	19.395651	16.779031	97.317927
9	7.618129	-26.134601	-33.121433	23.449056	16.618129	97.672261
10	8.563134	-22.189295	-31.274745	25.071188	16.563134	98.662246
11	9.749470	-26.211861	-33.421843	26.322131	17.249470	97.108382
12	10.512316	-24.150605	-30.201094	31.233654	17.012316	97.674349
13	12.402780	-23.354034	-29.480101	35.213727	17.402780	97.453504
14	12.717394	-22.148621	-27.686120	37.761964	17.217394	97.910358
15	14.105420	-21.978029	-28.025805	39.691123	17.605420	97.535941
16	15.368040	-21.449105	-27.965687	41.874480	17.868040	97.346139
17	15.620761	-20.256259	-25.936887	44.326870	17.620761	97.966756
18	16.748239	-19.540040	-25.320491	46.604856	17.748239	98.024195
19	17.762765	-18.704462	-24.353461	48.876384	17.762765	98.279189
20	18.535735	-18.799433	-25.131423	49.150407	18.035735	97.875588
21	19.548997	-16.852836	-26.056977	49.275879	18.048997	98.410445

Table B.1: HBT tuned path parameters

$Index$	$First$ $Harmonic$ (dBm)	Ib (A)	Vce (V)	Pin (dBm)	Ic (A)
1	0.1624	1.2000E-04	1.5000	-17.0000	0.0157
2	0.6530	1.2000E-04	1.5000	-16.5000	0.0157
3	1.6301	1.2000E-04	1.5000	-15.5000	0.0157
4	2.6001	1.2000E-04	1.5000	-14.5000	0.0157
5	3.5606	1.2000E-04	1.5000	-13.5000	0.0157
6	4.5081	1.2000E-04	1.5000	-12.5000	0.0157
7	5.8930	1.2000E-04	1.5000	-11.0000	0.0157
8	6.7790	1.2000E-04	1.5000	-10.0000	0.0157
9	7.6181	1.2000E-04	1.5000	-9.0000	0.0157
10	8.5631	1.2000E-04	1.7500	-8.0000	0.0156
11	9.7495	1.5000E-04	1.7500	-7.5000	0.0197
12	10.5123	1.5000E-04	1.7500	-6.5000	0.0197
13	12.4028	1.8000E-04	2.0000	-5.0000	0.0235
14	12.7174	1.8000E-04	2.0000	-4.5000	0.0235
15	14.1054	2.1000E-04	2.2500	-3.5000	0.0274
16	15.3680	2.4000E-04	2.5000	-2.5000	0.0311
17	15.6208	2.4000E-04	2.5000	-2.0000	0.0311
18	16.7482	2.7000E-04	2.7500	-1.0000	0.0349
19	17.7628	3.0000E-04	3.0000	0.0000	0.0386
20	18.5357	3.3000E-04	3.2500	0.5000	0.0422
21	19.5490	3.6000E-04	3.7500	1.5000	0.0455

Table B.2: HBT tuned path coordinates

Appendix C

pHEMT PA Tuned Path, Tables

Index	*First Harmonic* (*dBm*)	*Second Harmonic* (*dBc*)	*Third Harmonic* (*dBc*)	*PAE* (%)	*Gain Transducer* (*dB*)	*Output Phase* (*deg*)
1	9.996160	-56.171910	-62.535249	7.700597	10.996160	84.929194
2	10.947252	-57.214415	-60.144075	9.519458	10.947252	84.848168
3	11.881658	-58.425279	-57.740669	11.703020	10.881658	84.735168
4	12.793859	-56.990137	-55.360790	14.285267	10.793859	84.579382
5	13.677235	-52.294064	-53.053586	17.281423	10.677235	84.369600
6	14.524304	-47.542118	-50.874920	20.677772	10.524304	84.097461
7	15.721322	-51.262925	-51.627805	22.260193	10.721322	84.645240
8	16.809402	-43.760402	-52.264466	23.784684	10.809402	84.953084
9	17.831954	-40.016450	-52.435322	25.333781	10.831954	85.148745
10	18.813060	-37.571545	-51.996479	26.919681	10.813060	85.325388
11	19.806975	-34.798214	-53.348015	26.020083	10.806975	85.352171
12	20.736807	-33.386206	-51.558711	27.674363	10.736807	85.632403
13	21.658165	-31.820744	-51.105912	27.173645	10.658165	85.645929
14	22.565211	-30.496118	-50.232174	26.997025	10.565211	85.702375
15	23.516894	-29.364754	-48.521861	28.888629	10.516894	86.342798
16	24.679230	-29.657381	-47.210986	33.081328	10.679230	85.875162
17	25.592250	-27.886518	-47.472407	31.729453	10.592250	86.089454
18	26.624182	-28.457896	-44.797966	35.883579	10.624182	85.915661
19	27.583469	-27.740275	-43.796630	36.753568	10.583469	85.928091
20	28.511634	-27.173042	-42.521867	37.812907	10.511634	86.077265
21	29.513989	-24.819832	-43.580567	35.412161	10.513989	86.252337

Table C.1: pHEMT PA tuned path parameters

$Index$	$First\ Harmonic\ (dBm)$	$Vgs\ (V)$	$Vds\ (V)$	$Pin\ (dBm)$	$Ids\ (A)$
1	9.9962	0.5500	1.5000	-1.0000	0.0789
2	10.9473	0.5500	1.5000	0.0000	0.0789
3	11.8817	0.5500	1.5000	1.0000	0.0789
4	12.7939	0.5500	1.5000	2.0000	0.0789
5	13.6772	0.5500	1.5000	3.0000	0.0789
6	14.5243	0.5500	1.5000	4.0000	0.0789
7	15.7213	0.5500	1.7500	5.0000	0.0814
8	16.8094	0.5500	2.0000	6.0000	0.0839
9	17.8320	0.5500	2.2500	7.0000	0.0863
10	18.8131	0.5500	2.5000	8.0000	0.0888
11	19.8070	0.5500	3.0000	9.0000	0.0936
12	20.7368	0.5500	3.2500	10.0000	0.0959
13	21.6582	0.5500	3.7500	11.0000	0.1006
14	22.5652	0.5500	4.2500	12.0000	0.1052
15	23.5169	0.5500	4.5000	13.0000	0.1075
16	24.6792	0.5700	4.5000	14.0000	0.1258
17	25.5922	0.5700	5.2500	15.0000	0.1324
18	26.6242	0.5900	5.2500	16.0000	0.1515
19	27.5835	0.6100	5.7500	17.0000	0.1754
20	28.5116	0.6500	6.2500	18.0000	0.2203
21	29.5140	0.7500	7.5000	19.0000	0.3362

Table C.2: pHEMT PA tuned path coordinates

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Thanks to my parents for their love, faith and for giving me an education. Many times during the last six years, since I started to attend Electronic Engineering classes at the University of Trieste, I asked myself what I was studying for, especially when subjects were hard to understand and study. There were many possible answers: passion, ambition, commitment, interest... None of them convinced me but, not a long time ago, I understood what knowledge gives: freedom. That is probably the best gift I have been ever given, thanks!

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