NTNU

Norwegian University of
Science and Technology

5.8GHz, 1W high efficiency Power Amplifier in 90nm CMOS

Nina Tofte Røislien

Master of Science in Electronics

Submission date: July 2009

Supervisor: Morten Olavsbråten, IET

Co-supervisor: Trond Ytterdal, IET

Oddgeir Fikstvedt, Texas Instruments

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Problem Description

BACKGROUND:
The demand for high-speed wireless communication systems has grown during the last few years. High levels of integration are desired to achieve a smaller form factor and reduce cost in high volume applications. CMOS technology is the prime contender for achieving this level of integration. Though most of the radio frequency building blocks have been successfully integrated into CMOS process, the power amplifier (PA) is mostly implemented in a different process technology. Although several advances have been recently made on the design and implementetion of CMOS PAs, it still remains the bottleneck in achieving a true single-chip radio solution.

In addition, the 2.4GHz spectrum has become very crowded as it is used by a number of standards including the IEEE 802.15.1, 802.15.3 and 802.14.4. Therefore more and more interest has been shown to the 5.8GHz ISM band.

THESIS:
The student has to design a 5.8GHz high efficiency 1W Power Amplifier in 90nm CMOS technology. The PA can either be single ended or differential (push-pull). The power added efficiency should be around 50% and gain around 25dB.

Assignment given: 19. February 2009
Supervisor: Morten Olavsbråten, IET

CONTENTS

1. INTRODUCTION

Recently CMOS technology has been introduced in RF front-end applications. Traditionally this technology has been confined to the digital and baseband part of radio transceivers.

High level of integration becomes more and more important. This is basically due to the growing wish of saving fabrication cost, but also the need of a smaller form factor. CMOS technology is the prime contender to achieve this level of integration.

The main challenge in the design of a RF PA in CMOS technology is the low breakdown voltage and the hot carrier effect [1]. The oxide breakdown sets a limit on the maximum signal swing on the transistors drain node. An operation above this voltage may destroy the device. The hot carrier effect is more of a reliability issue. This is an effect that increases the threshold voltage and thereby degrades the performance over time. This is also avoided by not over exceeding the maximum voltage ratings.

The breakdown voltage decreases for a smaller scaled technology. The quadratic dependence of the output power on the supply voltage ($P_{out} \propto \frac{{V_{DD}}^2}{R_L}$), require a rapid reduction of the load resistance to maintain a high output power if the supply voltage decrease. If integration is the goal, it is important that the RF front-end PA is made in the same deep-submicron CMOS technology as the rest of the radio. Therefore lower output impedance and a larger current is required compared to traditionally used PA technologies to achieve the same output power. This raises matching issues, and thereby power loss in the parasitic resistors in the matching network (the power loss in the parasitic resistances greatly increase with the current, $P_{loss,parasitic} \propto I^2 R_{parasitic}$). Also a larger transistor is required to handle the larger currents, and thereby increasing the parasitic capacitances. With increased parasitic content in the transistors follows input matching issues due to lower input impedance which also gives power loss of the same reasons as in the output matching network.

It is recommended to use the standard voltage ratings (1.2V for 90nm CMOS) rather than the maximum voltage ratings due to reliability, which makes the design even more of a challenge.

One often used method to utilize a highest possible V_{ds} voltage is the cascode coupling of active devices. This method will raise this maximum allowable voltage with some possible advantages [2]; higher input-output isolation, higher input and output impedance and higher gain. The higher isolation eliminates the Miller effect and thus contributes to a higher bandwidth. The drawbacks are the doubling of capacitance and area together with the possible need of an extra supply voltage. The maximum achievable voltage is a twice the allowable voltage of one single device. To achieve this, extra techniques to distribute the

stress on the two transistors equally might be required. One possible techniques for doing so is the one described in [1] which will be presented shortly in section " Techniques used to relax restrictions due to low voltage breakdown". Another technique [3] used to enlarge the possible supply voltage of a class-E amplifier will be presented in the same section.

Another method to increase the breakdown voltage is to use thick-oxide devices alone or in a cascode coupling. Thick-oxide devices have higher breakdown voltages than the standard devices, but they also have poor high frequency performance in comparison. The thick-oxide device basically has a smaller gain at high frequency compared to the standard device [1].

The master thesis is to design a 5.8GHz high efficiency 1W (30dBm) Power Amplifier in 90nm CMOS-technology. The power added efficiency should be 50% and the gain around 25dB. The approach used is first to study and simulate two different types of promising amplifier topology, and then decide which one is the most promising to take further to a genuine design. At first the thought was to compare the two different types of amplifiers in a completely ideal case, but later on it was found that the losses in output network (especially the output bonding wire) was of too great importance to neglect in this comparison.

Because of the tough efficiency demands, and the fact that there is no linearity requirement, it was decided that the switching type of an amplifier was the only way to go. The switching types of amplifiers will in short sacrifice linearity in advantage of efficiency. Both types of investigated amplifiers have a theoretical efficiency of 100%.

The two types of studied amplifier topology is the class-E amplifier, which have been explored for this kind of use in previous papers [1, 3-7], and the inverted class-D amplifier. The inverted class-D is appealing because of its differential (push-pull) nature, which will give rise to a double voltage swing in comparison with the possible voltage swing in a single ended solution. This double voltage swing will make it possible to utilize a larger load resistance compared to the class-E amplifier (in theory, four times the size: $P_{out} \propto \frac{{V_{out}}^2}{R_L} = \frac{(2V_{out})^2}{4R_L}$).

A non-investigated option could be to use a class-B design with or without harmonic tuning (class-F) in a configuration that splits the signal in two equals and amplifies the signals 180-degrees out of phase with each other. The delayed signal is inverted before the two signal paths recombine (this way it becomes possible to make the class-B amplifier without the standard push-pull configuration and thereby without the pMOS transistor). This would in a perfect case give an efficiency of 78% for class-B, and a theoretical efficiency of up to 100% for a perfect class-F with harmonic tuning of all odd harmonics voltage components.

The goal of this thesis was to make a circuit design, and if time left a layout, which fulfills the given requirements. The efficiency goal defined in this thesis is a PAE of 50%. This efficiency is measured at the maximum output power, and is not reconed to be this high at lower output levels.

It was not expected, given the time considerations, that a prototype would get manufactured.

1.1 THESIS OUTLINE

In this thesis we will first go through some basic parameters used in high frequency design in chapter 2.1, “Important Parameters”. After this some theory behind matching and stability is described in short in chapter 2.2 and 2.3.

The focus in the theory chapter is however the class-E and the inverse class-D amplifier. They will be described in detail.

After the theoretical chapter the actual design of the class-E and the inverse class-D amplifier will be described respectively. The simulation results will be described in chapter 4.

A discussion of the results is made in chapter 5, and finally some conclusions are drawn and some suggested future work is presented in chapter 6.

1.2 METHOD

The method used for this thesis was to first study two different types of promising amplifier technologies and then from simulations, where the most important losses was included, decide which one to take further in to a complete circuit design.

The simulation and circuit design was done with the Cadence Design System with the use of the CMOS090 device library for typical corner. For the schematics the Cadence Composer Schematic was used, and for the simulations the Spectre simulator was used. This method was chosen because Cadence and the necessary libraries were already installed in the NTNU ANA computer lab on a Linux server.

Because of the very limited experience with Cadence used for RF-design amongst the Radio Frequency field of study at NTNU, another design tool Advanced Design System, ADS, would be the preferred option. Also, ADS contains an optimization function that Cadence lacks. Unfortunately it was found to be very time consuming to get libraries for use with the ADS software, and Cadence became the only option.

The Cadence design tool does not exist for use on a windows platform. To be able to work from a windows machine, an X server was installed. This way the outputs are displayed on the windows machine, while the software itself runs on the Linux server.

1.3 TECHNOLOGY LIMITATIONS

The most important limitation with regard to a power amplifier design in the CMOS 90nm technology is as already mentioned the voltage restrictions. The recommended supply voltage is as low as 1.2V.

In [1] it is however stated that the recommended voltage to guarantee a product lifetime of ten years is 5-10% above the maximum allowed supply voltage.

Another important fact in regard to the technology is the very low Q-factor of the inductors. The Q-factor is about 20, which means that one should use as little as possible on-chip inductors. If it is possible one should rather use the bondwires as inductors which has a higher Q-factor of about 150. Large inductors above the bondwire inductance (1nH) should be made off-chip by lumped components.

The smallest inductance possible in the bondwire is about 200pH. To get this small value, several bondwires in parallel are needed. One bondwire has an inductance of about 1nH, so this means five in parallel.

The values above are provided by supervisor Oddgeir Fikstvedt.

The CMOS-technology also contains thick-oxide devices. The thick-oxide devices have a larger breakdown voltage but also a poorer RF-performance [1]. Thick-oxide provides a lower gain at RF. The use of thick-oxide will prevent taking full advantage of the technology when it comes to high frequency performance.

2. THEORY

2.1 IMPORTANT PARAMETERS

2.1.1 TERMS OF EFFICIENCY

2.1.1.1 DRAIN EFFICIENCY

The drain efficiency is defined as the relationship between the fundamental output power and the required dc-power:

$$\eta_d = \frac{P_{out,f_c}}{P_{DC}} \quad (1)$$

2.1.1.2 PAE-POWER ADDED EFFICIENCY

An often used measure of efficiency is the Power Added Efficiency (PAE) defined as:

$$PAE = \frac{P_{out,f_c} - P_{in,f_c}}{P_{DC}} = \eta_d \left(1 - \frac{1}{G}\right) \quad 2)$$

Some will argue that this efficiency measurement is the most correct one (in comparison with the drain efficiency) because it takes the input power into account. The drawback is that the PAE can become negative for gain levels below one (output power less than input power).

2.1.2 POWER GAIN

The power gain is defined as the ratio between the output and input power at the fundamental frequency:

$$G = \frac{P_{out,f_c}}{P_{in,f_c}} \quad 3)$$

2.1.3 STABILITY

Stability is a very important element to consider when designing a power amplifier. Because of the high gain, oscillations are bound to happen if this is not considered.

The most used measurement of stability is the Rollet's stability factor, often called the K-factor. If this K-factor is greater than one (and Δ<1, as defined below), it means that the amplifier is unconditionally stable. That an amplifier is unconditionally stable means that it is stable for all possible input and output impedances that can be found within the Smith-chart (from the centre to the perimeter (gamma=1) at any phase angles). Conditionally stable would on the other hand be an amplifier that is stable when the input and output sees the intended impedances (often 50Ω), but could be unstable when mismatched.

The K-factor does not reveal anything about how unconditionally stable the amplifier is. In other words an amplifier with K-factor of 100 can be closer to oscillations than one with K-factor of one. The μ-factor ("mju-factor") is a better measurement for making comparisons like this, but since this factor is not included in Cadence, the K-factor is used in this thesis.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \quad 4)$$

Where $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$.

Another measure of stability is stability circles. These are drawn in the Smith-chart. This measure can for instance be used for conditionally stable amplifiers. The amplifier will be stable in the area between the circle and the rest of the smith-chart on the side which

contains the centre of the smith-chart. This circles is however not included in Cadence, so they are not used in this thesis.

2.1.4 S-PARAMETERS

S-parameters (scattering parameters) are being used to describe the behavior of RF-circuits. They are intended to be used for linear systems, small signal analysis. Gain, stability, voltage standing wave ratio, reflection coefficients and return loss can all be described by S-parameters.

The S-parameters are easily described by means of a two-port network like the one showed in Figure 1. a_1 is the incident and b_1 is the reflected voltage wave at port 1. a_2 is the incident and b_2 is the reflected voltage wave of port 2.

The S-parameters are defined so that:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad 5)$$

This means that the reflected voltage wave, b_1, consist of the reflected part of the incident voltage wave, a_1, plus the backward amplified part of the incident voltage wave at port 2, a_2.

S_{11} is the input port voltage reflection coefficient, and S_{21} is the forward voltage gain. They are equal to:

$$S_{11} = \frac{b_1}{a_1} \quad 6)$$

$$S_{21} = \frac{b_2}{a_1} \quad 7)$$

When port 2 is terminated in the systems impedance Z_0 so that a_2=0.

S_{22} is the output port voltage reflection coefficient, and S_{12} is the reverse voltage gain. They are equal to:

$$S_{22} = \frac{b_2}{a_2} \quad 8)$$

$$S_{12} = \frac{b_1}{a_2} \quad 9)$$

When port 1 is terminated in the systems impedance Z_0 so that a_1=0.

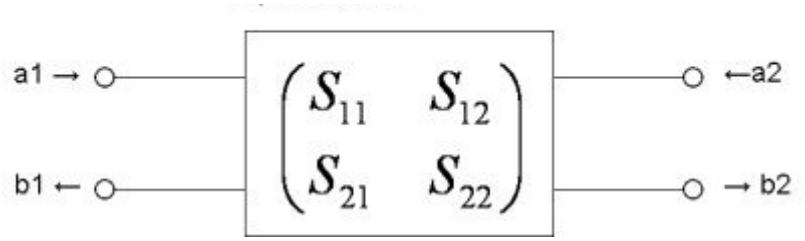


Figure 1: Generalized two-port network [8].

2.1.5 BALUN

A balun is used to transform a single-ended signal (unbalanzed) to a differential signal (balanced) or vice versa. They are often used to transform the impedance as well. There are many different ways to make a balun, presented below is a simple narrow-banded first order balun which is used in the inverse class-D amplifier design. This balun transforms the impedance, so the matching can be partly or completely included in the balun.

The balun is showed in Figure 2.

$$X_B = \sqrt{Z_{BAL} \cdot Z_0} \qquad 10)$$

Equation 20 gives the component values of Figure 2.

Z_{BAL} is the balanced impedance, and Z_0 is the unbalanced termination. X_B is the reactance, capacitive or inductive. This means that the capacitance and inductance be calculated by:

$$C = \frac{1}{2\pi f \cdot X_B} \qquad 11)$$

$$L = \frac{X_B}{2\pi f} \qquad 12)$$

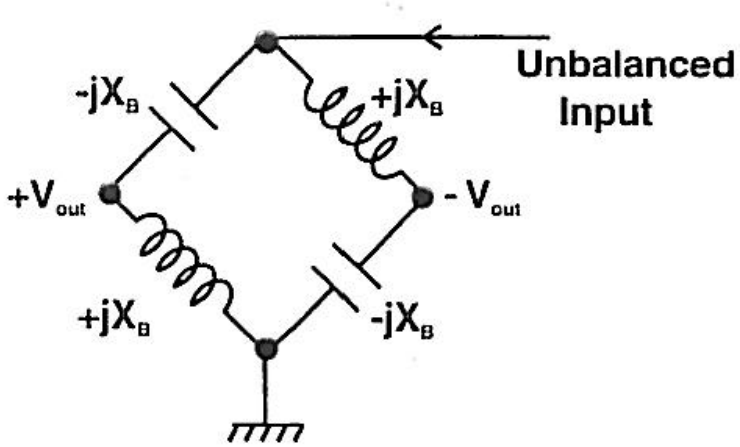


Figure 2: First order LC-balun.

2.1.6 QUALITY FACTOR (Q-FACTOR)

The quality factor of an inductance is defined as:

$$Q = \frac{2\pi f L}{R_s} \qquad 13)$$

Where R_s is the resistance of the non-ideal inductance.

The Q-factor is thus a measure of how much power loss the inductance contributes to. A high Q-factor means that the inductance contributes to a small loss.

As one can see from the equation 13, an inductance with a constant Q-factor will contribute to more loss if the frequency increases.

When making a realistic circuit design it is important to consider that an inductance will never be lossless. There is loss due to the quality factor, and there is loss due to the DC-resistance. If the current through the inductor consists only of a given frequency, the inductance is easy to model by simply including a series resistance with the value given by equation 13. One can also model this resistance as a shunt resistance. Then the value is given by:

$$R_{shunt} = (1 + Q^2) \cdot R_s \qquad 14)$$

If we however have both dc-current and RF-current, we need more realistic models, which are showed in Figure 3a and b.

In Figure 3a, the dc-loss is included in the R_{DC} resistance, while the RF-loss from the non-infinite Q-factor is included via R_p. R_p is the shunt version of R_s which is calculated as follows (we have to subtract R_{DC} so that we don't include it twice):

$$R_p = (1 - Q^2) \cdot (R_s - R_{DC}) \quad 15)$$

In Figure 3b, the dc-path and the RF-path are separated by a large inductance, $L_{RFblock}$, so that the RF-current sees the intended R_s-resistance, and the dc-current sees the R_{DC}-resistance (here it is assumed that the R_s-resistance is larger than the R_{DC}-resistance).

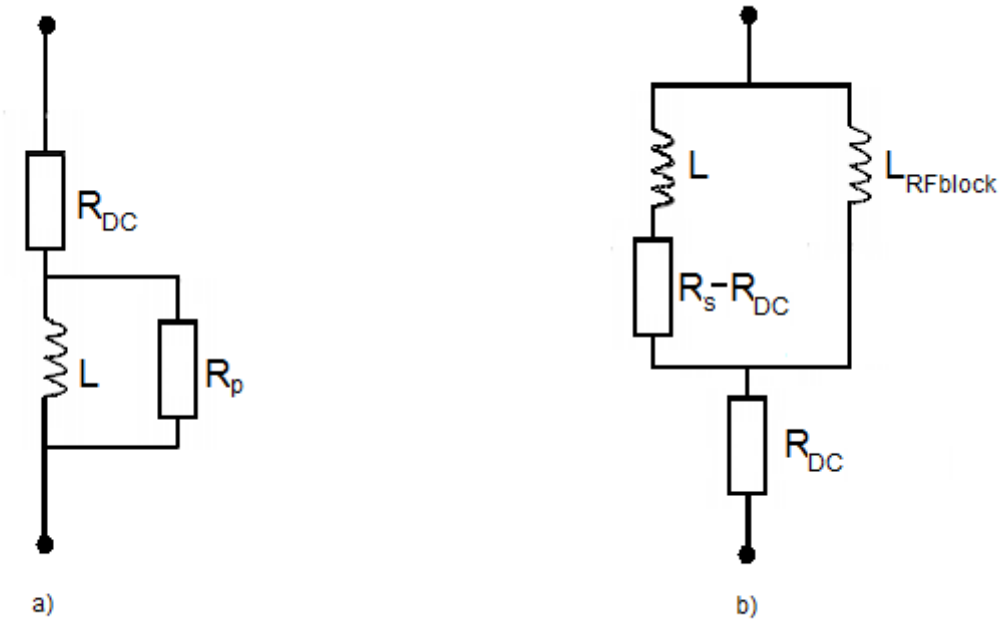


Figure 3: Methods to introduce different loss at RF and DC respectively.

2.2 STABILITY METHODS

All stability methods will function by introducing some kind of loss into the circuit. This can be done in multiple ways, and is often done by some kind of negative feedback. The loss can be on all frequencies, or it can be frequency selective. The frequency selective methods are often used when the instability is outside of the operational frequency band.

Here, only the method used in this thesis will be described. This is a frequency selective method that uses feedback to decrease the gain and thereby making the circuit stable. The feedback is shown in Figure 4.

The feedback in Figure 4 will be high at low frequencies when the inductance acts like a short. At high frequencies this inductance will act as an open circuit and the resistance will decide the feedback. This will result in a large feedback at low frequencies and a smaller feedback at high frequencies. It is important to note that the output voltage will become the same as the input voltage at low frequencies, thereby effectively yielding no gain at all. This

will in this simple configuration interfere with the transistor biasing, and some kind of dc-blockage must be introduced if this is to be avoided.

The stability should always be checked from zero and up to f_{max}.

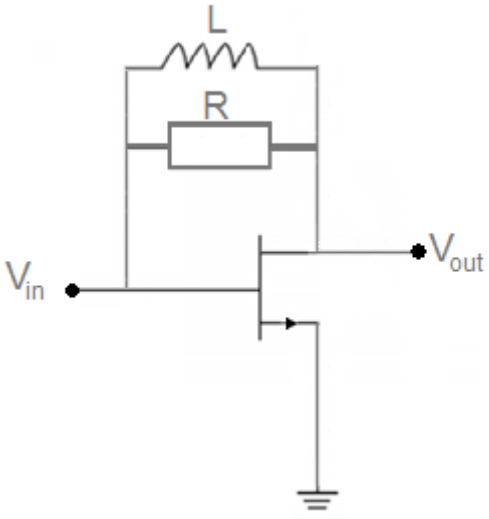


Figure 4: Feedback for stabilization.

2.3 IMPEDANCE MATCHING

The input and output impedances must be matched to the source and the load impedances to prohibit reflections and to maximize power transference. The matching will also have a lot to say for the bandwidth.

The power transference will reach the maximum when the input impedance of the amplifier is the complex conjugated to the source impedance, and the output impedance is complex conjugated to the load impedance.

2.4 THE SWITCHING TYPE OF AMPLIFIER

As already mentioned, the switching type of amplifier sacrifices linear gain in favor of high efficiency. The amplifier classes E, D and F are all of the switching type. In an ideal case this type of amplifier can only be in one of two states, either “on” or “off”. In the “on” state the transistor should have current through, but no voltage across. In the “off” state there should be no current through, but voltage across. This ideal case will by this have no power loss

since there is never a state with simultaneous voltage and current. The efficiency will be a 100 percent.

In real life there are a number of sources which could lead to power loss in the transistor. One of them is the on-resistance. This is a resistance that gives rise to a voltage across the transistor while current runs through. This resistance is included in the formulas that will be presented for the class-E and class-D^{-1} amplifiers.

In [9], another source that leads to power loss is described. This loss is due to the discharge of the transistors output capacitance. Two different simplified models for the switching amplifier are shown in Figure 5. The output capacitance of the transistor is charged while the transistor is off. With the first model, Figure 5a, this charge is lost to ground as soon as the transistor turns on. With the second model Figure 5b, the charge gets transferred to an inductor and shorted to ground when the transistor turns off again. The loss is proportional to the switching frequency, which makes high capacitive technologies (like CMOS) hard to use at high frequencies when there is high efficiency demands. The way to avoid this capacitor loss is to make the voltage across the switching device turn to zero just before the transistor is turned on for the first model, and make the current turn to zero just before opening the switch with the second model. This is called the Zero Voltage Switching or the Zero Current Switching.

The time delay between the on and off state can also lead to simultaneous voltage and current and thereby efficiency loss. This can be resolved by proper design of the load network.

The switching property of the amplifier is dependent on the transistor to alternately be driven properly into compression, and to be turned off properly. This leads to a fast declining efficiency for smaller input signals. This can be very important when back off power operations are used. Technologies to increase this back off power efficiency exists (like Envelope Elimination and Restoration (EER) or Chireix outphasing which both lets the switching amplifier operate on a constant envelope) but will not be presented here.

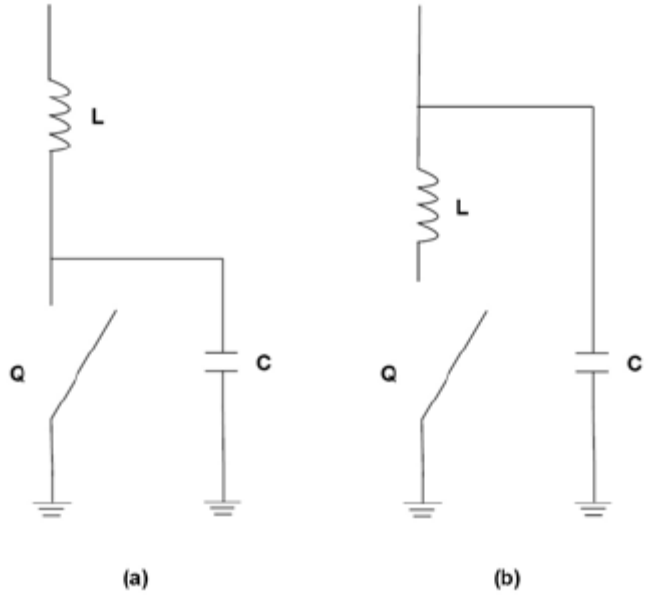


Figure 5: Two types of simplified switch models [9].

2.5 CLASS-E AMPLIFIER

The Class-E amplifier was invented by Nathan O. Sokal and his son Allan D. Sokal in 1975, and is described in [10]. This type of amplifier has become very popular in high efficiency solutions, and is based on a load network that is synthesized in manner to produce a response that prevents simultaneous voltage across and current through the device (even if the device switching times are appreciable fractions of the ac cycle.) This is the main reason to choose the class-E amplifier over the other types of switching amplifiers.

The load network is simply based on a shunt capacitor, a series LC and the load resistance; consequently merely an extra capacitor compared to for instance regular non-switching types of amplifiers.

The innovative research of Sokal resulted in a number of equations which describes a type of load network that is synthesized to have a transient response which maximizes power efficiency. Sokal also thoroughly describes the very important difference of a switching type of amplifier contra amplifiers used as current sources, and the different requirements this places on the load network. For instance a class-C amplifier is assumed to be a high impedance current source while a switched type of amplifier should have low “on” resistance and high “off” resistance. This means that the output current is determined primarily by the input drive and it substantially independent of the output voltage in a class-C amplifier (consequently active region), with a minimum voltage across the device to prevent saturation. With this type of amplifier, efficiency is sacrificed in advantage of

linearity (the class-C amplifier is not the most linear seeing as it leads current for less than half the periode, although it is the one Sokal refers to as an example). In contrast, in a switched type of amplifier saturation is desired and a low “on” resistance is required to achieve maximum efficiency.

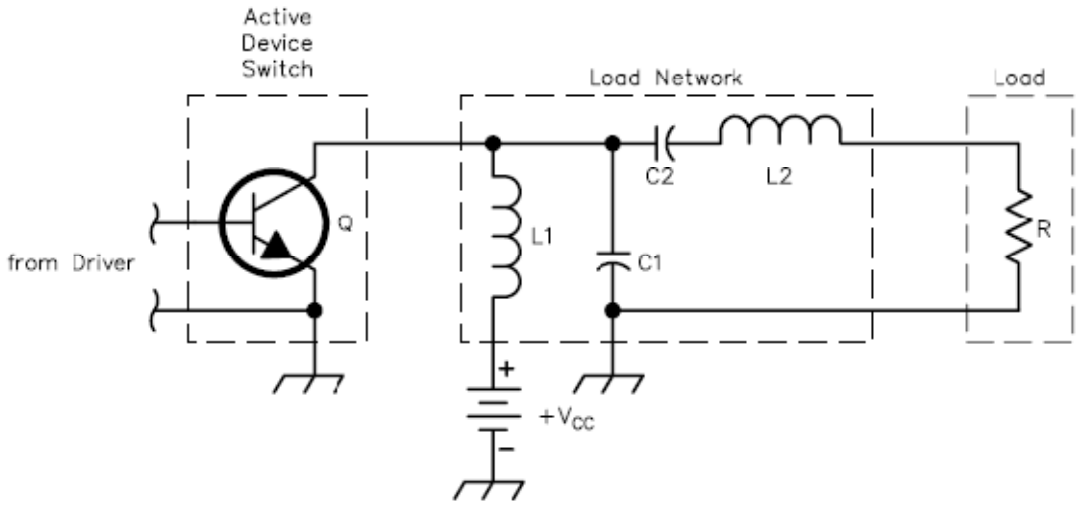


Figure 6: The Class-E amplifier [11].

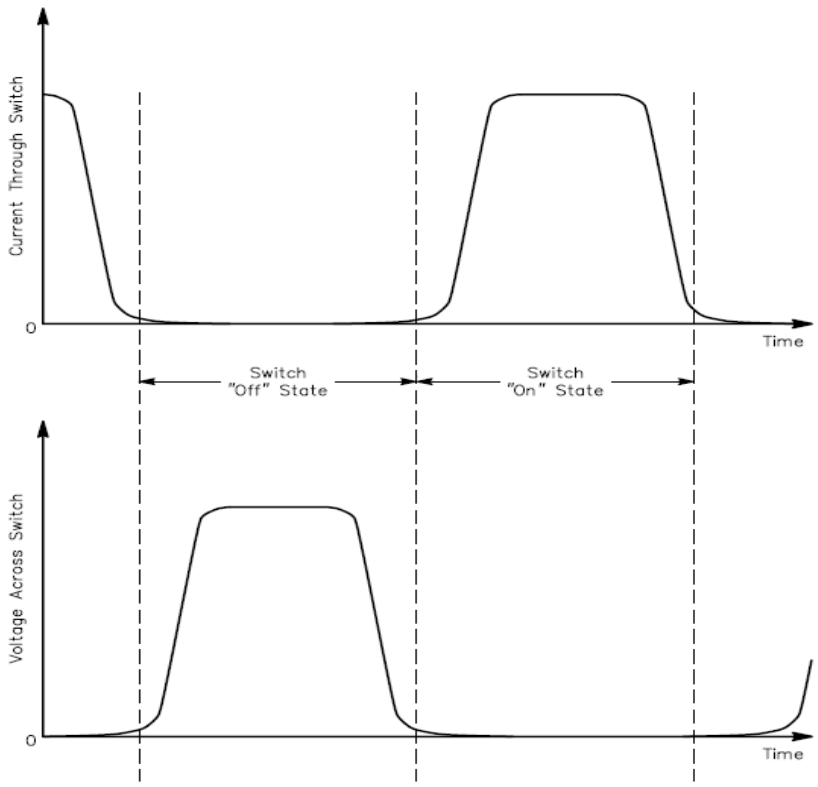


Figure 7: The desired current and voltage waveforms of the Class-E amplifier [11].

The Class-E amplifier is a single ended, switching type of an amplifier. The amplifier is shown in Figure 6. Because it acts as a switch, it needs to be properly driven by a driver. The driver can be optimized towards the design criteria like gain and efficiency. The main criteria on the driver is nevertheless to introduce an appropriate input signal on the active device which rapidly turn the device on and off with as little delay as possible. A small delay can be translated directly into a less demanding load network to obtain high efficiency. Naturally, voltage breakdown needs to be accounted for designing this driver.

The switching property of the amplifier is non-ideal; it can have a nonzero "on" resistance and the "off" resistance is never infinite. Also, a practical device will have a nonzero switching time. In Sokals equations, the nonzero "on" resistance is accounted for in the term $V_{ds,sat}$. This saturation voltage will decrease the overall efficiency because it will appear across the device while current runs trough. This saturation voltage, and the leakage current due to the non-infinite "off" resistance is only dependent of the active device chosen, and not the load network.

The nonzero switching time would in an ordinary switching type of amplifier lead to efficiency loss. The novel principle of this type of amplifier is however to avoid by design the simultaneous imposition of voltage and current, even during a substantial duration in the switching time. Sokal even states that this type of load network will decrease the switching time to such extent that the switching time is load network dependent.

The load network is based upon these objectives:

- During the transition from "on" to "off" the voltage across the active device stays low until the current has stopped flowing. This prevents efficiency loss during switching time duration.
- In the transition from "off" to "on" the voltage reaches zero just before current starts to flow.
- Just before the beginning of the "on" state the voltage has zero slope (dv/dt=0). This is to prevent a slight mistuning having large influence on the efficiency.
- These two last points indicates that the start current in the transition to the "on" state has to be zero. This is because a zero voltage slope and a zero voltage implies that the capacitor C_{ds} is fully discharged. This will lead to a minimization of the switching time.
- Optimally, the current and voltage waveforms should also have short rise and fall times and be flat topped. The article does not say why, but a fair guess is that this square like shape gives rise to odd harmonics that will allow the first harmonic to be larger than the breakdown voltage (odd harmonics brings down the peak value).

Description of the circuit diagram in Figure 6:

V_{cc} is the supply voltage. L_1 is a shunt inductance, later it will be described how a smaller reactance can be beneficial. C_1 is a shunt capacitor. It is important to remember that this capacitance is in parallel with the output capacitance of the active device (C_{ds}) as well as the small parasitic capacitance L_1 might have. The impact of L_1 on the total output capacitance is large if a non-infinite choke is used.

R is the load resistance. The optimum load resistance in this technology will be shown to be way smaller than 50Ω, which will lead to matching issues such as efficiency loss and strong dependency on component values (narrow banded). C_2 and L_2 is a tuning filter where part of L_2 in collaboration with C_2 makes a resonance filter on the operating frequency, and the rest of L_2 shapes the waveforms. A nearly sinusoidal current will flow in the load branch.

2.5.1 FORMULAS DESCRIBING THE CLASS-E AMPLIFIER

The formulas presented below are mainly collected from [10]:

$$V_{ds,pk} = 3.562V_{cc} - 2.562V_{ds,sat} \tag{16}$$

$$R = 0.577\frac{\left(V_{cc} - V_{ds,sat}\right)^2}{P} \tag{17}$$

$$L_2 = \frac{Q_L R}{2\pi f} \tag{18}$$

$$C_1 = \frac{1}{2\pi f R \cdot 5.447} \tag{19}$$

$$C_2 \approx C_1\left(\frac{5.447}{Q_L}\right)\left(1 + \frac{1.42}{Q_L - 2.08}\right) \tag{20}$$

$$I_{DC} = \frac{P}{V_{cc}}\left[\frac{1 - \frac{(2\pi A)^2}{12}}{1 - \frac{(2\pi A)^2}{6} - \frac{V_{ds,sat}}{V_{cc}}\left(1 + A - \frac{(2\pi A)^2}{6}\right)}\right] \tag{21}$$

$$I_{ds,pk} = I_{DC}\left[1 + 1.862\left(1 - \frac{0.5}{Q_L}\right)\right] \quad 22)$$

$$\eta_d = \frac{1 - \frac{(2\pi A)^2}{6} - \frac{V_{ds,sat}}{V_{cc}}\left(1 + A - \frac{(2\pi A)^2}{6}\right)}{1 - \frac{(2\pi A)^2}{12}} \quad 23)$$

$$A \equiv \left(1 + \frac{0.82}{Q_L}\right) f \cdot t_f$$

$$Where\ t_f\ is\ drain\ current\ fall\ time\ during\ transistor\ turnoff \quad 24)$$

Q_L is the Q-factor of the L_2-R branch, and can be any chosen value. Q_L gives the relationship between C_1 and C_2. A high Q_L gives low harmonic content of the output power while a low Q_L leads to higher efficiency i.e. a tradeoff needs to be made.

$V_{ds,sat}$ is the voltage appearing over drain-source when the transistor is “on”. Obviously in an ideal case this voltage would be zero such that no power would be dissipated in the active device. For this specific design it will be shown that $V_{ds,sat}$ must have a certain value above zero to make the transistor conduct enough current because of the transistors non zero “on” resistance. This will lead to a tradeoff between the transistor size and efficiency.

V_{cc} is the supply voltage and should be chosen as high as possible to increase the optimal load resistance.

η_d is the drain efficiency.

One formula describing the drain efficiency for class-E with the use of the on-resistance instead of $V_{ds,sat}$ can be found in [3]:

$$\eta_d \propto \frac{1}{1 + 1.4 \times \left(\frac{r_{on}}{R_L}\right)} \quad 25)$$

One can from this formula and formula no. 8 clearly see the negative influence the on-resistance or its corresponding $V_{ds,sat}$ have on the efficiency.

It should be mentioned that the on-resistance actually decreases with a smaller scaled technology; the problem is that the optimal load resistance decreases more rapidly leading to lost efficiency. This can be seen by Figure 8. This figure does not cover the 90nm

technology, but it is clearly how the on-resistance decrease less rapidly compared to the optimal load resistance when the technology scales down.

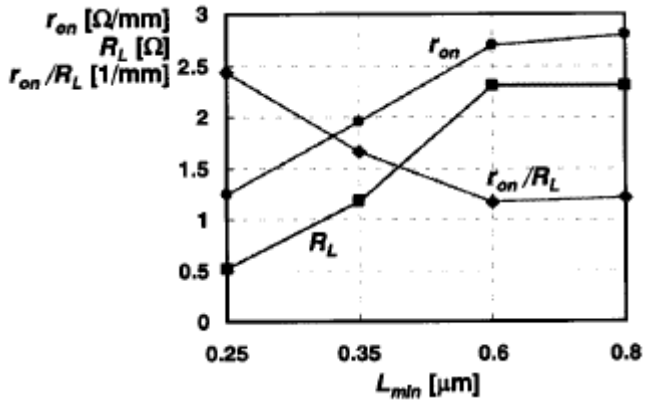


Figure 8: On-resistance for nMOS and the optimum load resistance for Class-E for different scaled CMOS technologies.

2.5.2 DESIGN GUIDELINES FOR CLASS-E AMPLIFIER

The design guidelines presented below are mainly collected from [10]:

- If the voltage never reaches zero before transistor turn on; it means that it is too much damping i.e. Q_L is too low.
- If the voltage becomes negative before transistor turn on; it means that it is too little damping i.e. too large Q_L. If the voltage becomes sufficient negative it can put the transistor in the active inverted mode and inverted drain current may flow reducing the efficiency. It is also a possibility that the transistor gets damaged.

In [11] a graphical design guideline is given and is shown in Figure 9, a more descriptive version can be found in Appendix A, Figure 40.

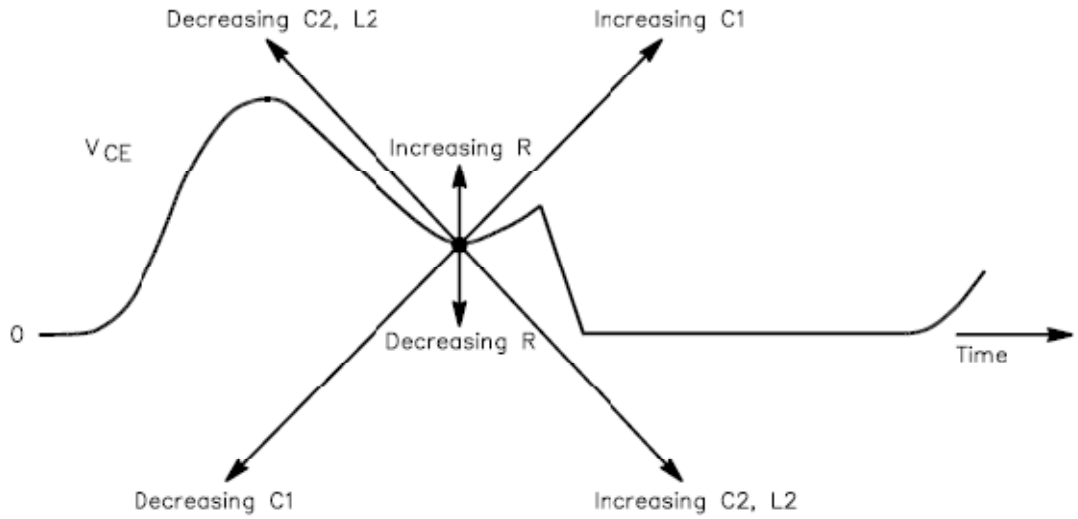


Figure 9: The effect of load network component adjustment on a typical mistuned circuit [11].

2.6 INVERTED CLASS-D AMPLIFIER

The inverted class-D amplifier is the current switching type of the traditional class-D amplifier. It is also called the current mode class-D amplifier, CMCD, whiles the traditional class-D amplifier is called the voltage mode class-D amplifier, VMCD. To get from the VMCD amplifier to the CMCD amplifier, one can simply change all the series components into shunt components, consequently the series transistors into shunt transistors, and the series LC-branch into a shunt LC-branch. The load resistance is also altered from being in series to being in shunt, and from this the amplifier becomes differential instead of single-ended. The current waveform becomes the voltage waveform, and the voltage waveform becomes the current waveform.

From now on, the inverted class-D amplifier will be called the class-D^{-1} amplifier.

The class-D and the class-D^{-1} amplifiers are shown in Figure 10, and the voltage and current waveforms of the class-D^{-1} amplifier is shown in Figure 11.

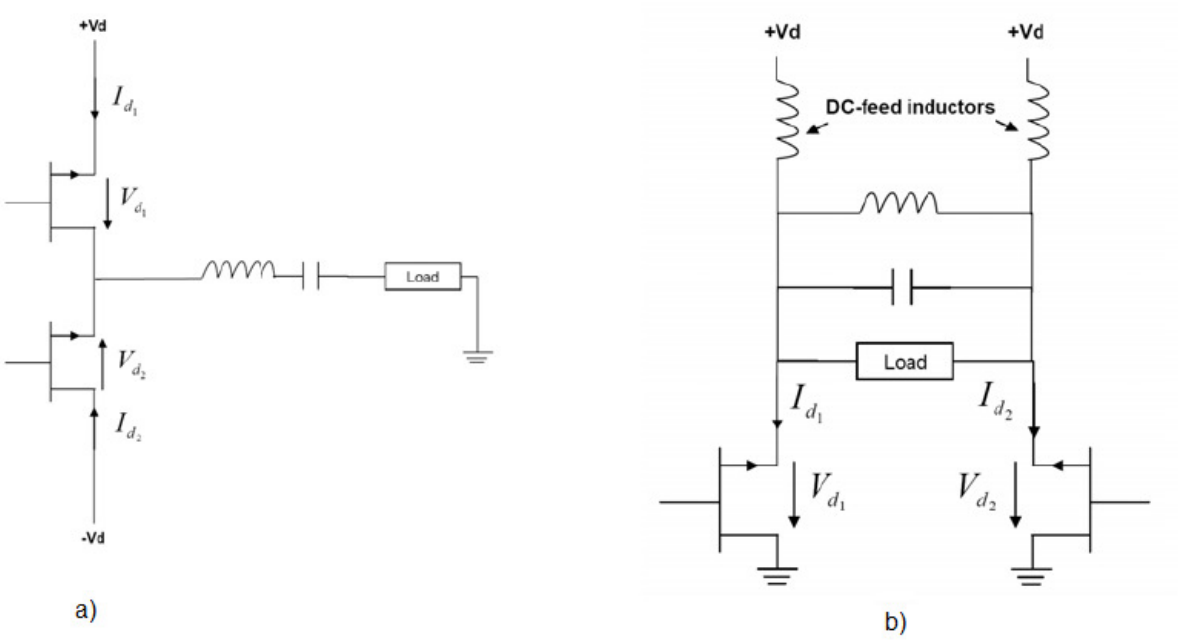


Figure 10: a) The class-D amplifier [9]. b) The class-D^{-1} amplifier [9].

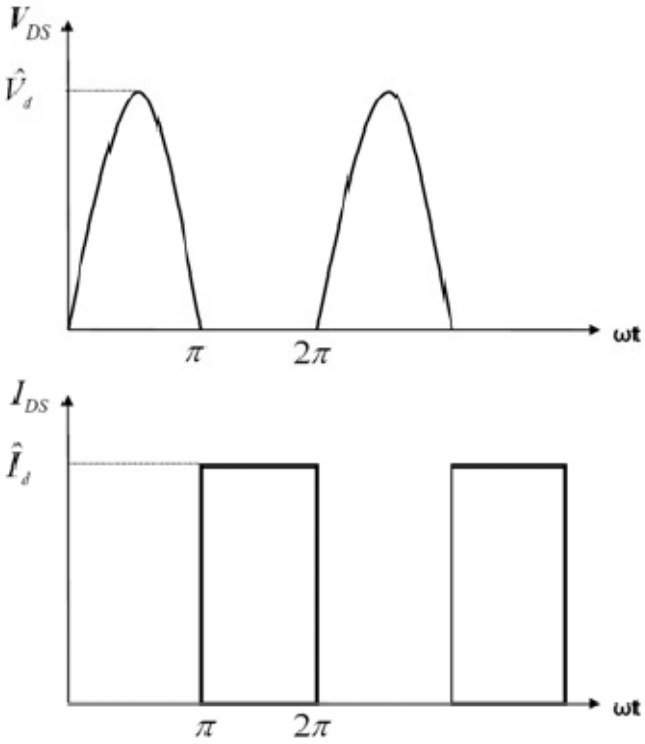


Figure 11: The class-D^{-1} voltage and current waveforms [9].

The class-D^{-1} type of amplifier uses a parallel-tuned resonant circuit, driven by two on-off switches in a push-pull configuration. The inputs are ideally driven such that one of the switches is on while the other is off.

The resonator shorts out all the harmonics while blocking the fundamental frequency. The fundamental frequency current runs through the load resistance and results in output power at the fundamental frequency.

The differential topology allows twice the voltage across the load resistance compared to the class-E configuration for a given transistor voltage. This means that the optimal load resistance will be higher (about four times) compared to the class-E. As described earlier, the higher load resistance will lead to a more efficient and less demanding matching network. All other losses due to non infinite Q-factors in the load network will also decrease proportionally with an increased load.

Another way of describing the two previous advantages is with the measure P_{max}. Together with the class-D and the class-F/F^{-1} this amplifier has the highest P_{max} of the amplifier classes [12]. P_{max} is defined in [12] as:

$$P_{max} = \frac{P_{out,f_c}}{N \cdot \hat{I}_d \cdot V_d} \qquad 26)$$

$\hat{I}_d$ and V_d are the peak current and peak voltage respectively. N is the number of devices. $P_{out,fc}$ is the output power at the carrier frequency.

P_{max} becomes a measure of the current required to achieve a certain output power level and will give an indication of the transistors ability to deliver power at a certain stress level for a given amplifier topology. Even though the class-F/F^{-1} has the same P_{max} as the class-D/D^{-1}, the differential configuration of the class-D/D^{-1} compared to the single ended configuration of the class-F/F^{-1} will give the class-D/D^{-1} higher output power capabilities.

Compared to the class-F amplifier (at least if made as a harmonic tuned class-B), the class-D/D^{-1} will be less linear.

One drawback of this type of amplifier is the risk of both active devices to be on or off simultaneously if not provided with the required 180^{o} out-of-phase signals. This might give loss in efficiency, or worse; it can lead to transistor destruction by second breakdown.

Depending on the gate-bias level, the transistors can be simultaneously on or off when driven by small input voltage swing (power back-off). However, they will not be equally on/off and will thus provide a small output power. The fact that they are simultaneously on, and the fact that they are no longer driven into compression will lead to efficiency loss.

2.6.1 FORMULAS DESCRIBING THE INVERTED CLASS-D AMPLIFIER

In the following, formulas describing the class-D^{-1} amplifier will be presented. The maximum efficiency of 100% will also be demonstrated. The formulas are mainly collected from [9].

The current is a square wave. Because of the switching property of the amplifier, and by looking at Figure 11 it becomes obvious that the current peak must be; $\hat{I}_d = 2I_{DC}$. Since the current is a square wave, it can be described as an infinite Fourier-series containing all odd harmonics:

$$I_d(\omega t) = I_{DC} \cdot \frac{4}{\pi}\left[\sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} sin(n\omega t)\right] \quad 27)$$

The voltage across the load is a sine wave and is described as follows:

$$V_R(t) = V_{peak} \cdot sin(\omega t) = \frac{4}{\pi} \cdot I_{DC} \cdot R_L \cdot sin(\omega t) \quad 28)$$

Were $\frac{4}{\pi} \cdot I_{DC} \cdot R_L$ is the peak drain voltage.

In [9] the average voltage is calculated:

$$V_{dd} = \frac{1}{2\pi}\int_0^{\pi} V_R(t)dt = \frac{1}{2\pi}\int_0^{\pi} = \frac{4}{\pi} \cdot I_{DC} \cdot R_L \cdot sin(\omega t)d\omega t = \frac{4}{\pi^2}\, I_{DC}R_L \quad 29)$$

This means that:

$$I_{DC} = \frac{\pi^2 V_{dd}}{4R_L} \quad 30)$$

As well as:

$$V_{peak} = V_{dd} \cdot \pi \quad 31)$$

Since the two drain currents runs with opposite phase, they can be described as follows:

$$I_{d1}(\omega t) = I_{DC} - I_{DC} \cdot \frac{4}{\pi}\left[\sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} sin(n\omega t)\right] \quad 32)$$

$$I_{d2}(\omega t) = I_{DC} + I_{DC} \cdot \frac{4}{\pi}\left[\sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} sin(n\omega t)\right] \quad 33)$$

If the resonator is perfect and shorts out all these odd-harmonics, the load current will be the difference between the two first harmonics of the drain currents:

$$I_R = I_{d1,n=1} - I_{d2,n=1} = -\frac{8}{\pi} I_{DC} \cdot sin(\omega t) \quad 34)$$

The drain voltages can be derived in a similar manner and are described like this:

$$V_{d1}(\omega t) = V_{dd} + \frac{\pi}{2} V_{dd} sin(\omega t) - V_{dd} \sum_{n=1}^{\infty} \frac{2}{(2n)^2 - 1} cos(2n\omega t) \quad 35)$$

$$V_{d2}(\omega t) = V_{dd} - \frac{\pi}{2} V_{dd} sin(\omega t) - V_{dd} \sum_{n=1}^{\infty} \frac{2}{(2n)^2 - 1} cos(2n\omega t) \quad 36)$$

Which leads to the same load voltage as derived earlier:

$$V_R = V_{d1} - V_{d2} = \pi V_{dd} sin(\omega t) = \frac{4}{\pi} \cdot I_{DC} \cdot R_L \cdot sin(\omega t) \quad 37)$$

One interesting part is that the even-harmonics of the drain voltage waveforms gets canceled out by itself when doing the operation above. This actually means that the drain voltages see infinite impedance at the even-harmonics. As a consequence of this, is that one can disregard the even-harmonics when designing the resonator.

The first harmonic resistance can from the load current and voltage be derived as:

$$Z_L = R_L = \frac{\pi V_{dd} sin(\omega t)}{\frac{8}{\pi} I_{DC} \cdot sin(\omega t)} = \frac{\pi^2 V_{dd}}{8 I_{DC}} \quad 38)$$

The output power and the power consumption are given by formula 36 and 37 respectively:

$$P_{out,f_c} = \frac{|V_R|^2}{2R_L} = \frac{\pi^2 {V_{dd}}^2}{2R_L} \quad 39)$$

$$P_{DC} = V_{dd} \cdot 2I_{DC} = V_{dd} \cdot 2\frac{\pi^2 V_{dd}}{4R_L} = \frac{\pi^2 {V_{dd}}^2}{2R_L} \quad 40)$$

This proves the efficiency of 100%:

$$\eta = \frac{P_{out,f_c}}{P_{DC}} = \frac{\frac{\pi^2 {V_{dd}}^2}{2R_L}}{\frac{\pi^2 {V_{dd}}^2}{2R_L}} = 1 \qquad 41)$$

It is important to note that these formulas are based upon the resonance filter to be completely ideal with infinite impedance for the fundamental frequency, and a short for the odd-harmonics.

2.6.2 UTILIZATION OF C_{DS} IN THE RESONANCE CIRCUIT

One important advantage of the class-D^{-1} amplifier in comparison with the class-D amplifier is that the capacitor C_{ds} of one of the transistors (one at a time) will be in shunt with the resonance branch. This will make it possible to design the resonance network without the use of the capacitor shown in Figure 10b. This is described in [9].

The absorbance of C_{ds} can be easily seen if one uses the simplified switch model of the transistor (Figure 5a) in the class-D^{-1} topology as shown in Figure 12:

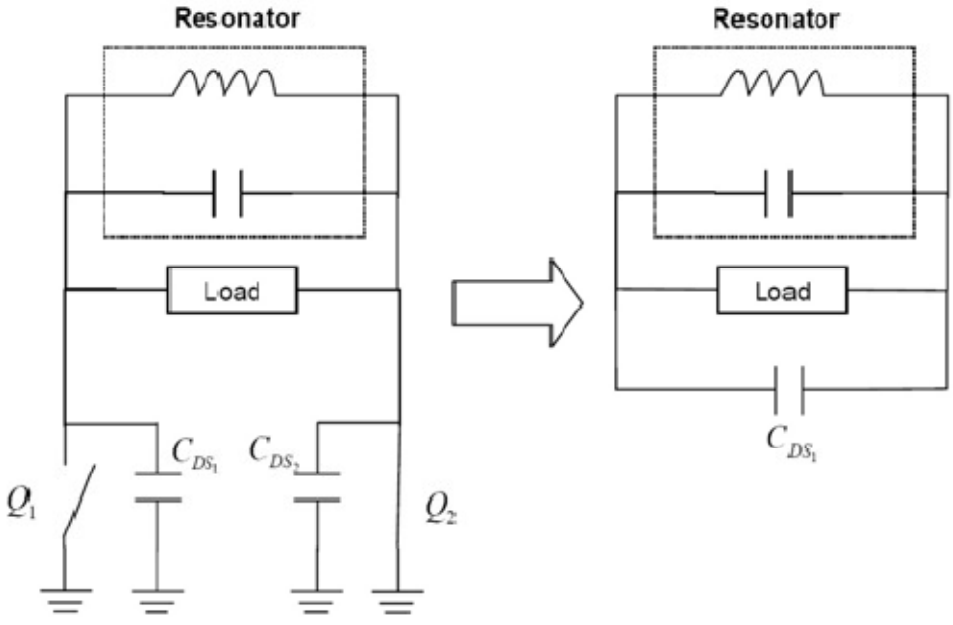


Figure 12: C_{dc} absorbance in the resonance network [9].

The C_{ds} capacitance of the "off" switch becomes in shunt with the resonance branch because the "on" switch in the ideal case is equal to ground.

It is however important to remember that the C_{ds} capacitance can become too large. This is because the inductor cannot be made arbitrarily small (at least not in integrated technologies).

2.7 TECHNIQUES USED TO RELAX RESTRICTIONS DUE TO LOW VOLTAGE BREAKDOWN.

2.7.1 SELF-BIASING

A well known method to enlarge the allowable voltage across an active device without exceeding the oxide breakdown limits is to use a cascode coupling. With the use of self-biasing, one can increase the voltage by a maximum of two times the allowed voltage of a single device.

A cascode coupling and the associated voltage waveforms are showed in Figure 13. A cascode coupling consists of a common-gate and a common-source transistor. The common-source is the input transistor while the common-gate is the output transistor. The common-gate transistor is normally connected directly to a DC-supply through the gate node.

With the coupling showed in Figure 13, the voltage swing on the gate-drain of the common-gate transistor becomes larger than that of the common-source transistor. This means that in this simple configuration, the common-gate transistor becomes the bottleneck. A way of solving this problem is described in [1];

In short this method introduces a voltage swing on the gate node of the common-gate transistor. This voltage swing will be in phase with the signal existing on the two drain nodes, and will enable the drain node of the common-source transistor to get a higher voltage swing. The way this is done is to introduce a simple LP-filter which couples part of the output drain signal back to the gate of the common-gate transistor. This can be seen in Figure 14.

The voltage swing in node D1 of Figure 13 and Figure 14 will always be lower than the voltage/voltage-swing at G2 by an amount of the gate-source voltage of the common-gate transistor. This means that a higher voltage swing at node D1 can be enabled by introducing a higher voltage or voltage swing at G2. Since the LP-filter allows RF-swing at G2, a design that lets the transistors experience the same amount of voltage stress can be made by correctly choosing the filter component values. This filter will also provide the dc-bias for G2. Because no dc-current runs through the gate or the filter capacitor, the dc voltage applied to G2 is the same as the dc voltage applied to D2.

In the article it is also stated that the self-biasing technique does not degrade the maximum power and PAE as long as both transistors are driven from triode into saturation during large signal operation.

A technique called the Bootstrapped cascode amplifier is also presented in [1]. This technique is a modified version of the self-biased one, where a diode-connected transistor and a resistance are included to increase the dc voltage at G2. This can be used in for instance the class-E amplifier were the drain voltage swing can be more than three times the supply voltage. This leads to a small dc-voltage at G2, which needs to be increased if one wants to distribute the voltage stress on the devises equally. The design of the class-E amplifier was not taken far enough to implement this technology, so it will not be described further.

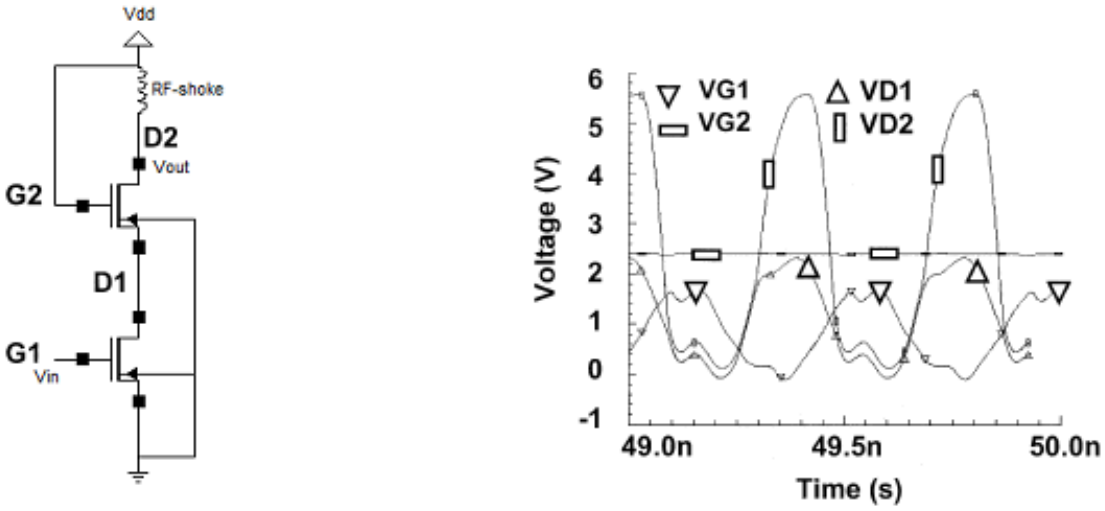


Figure 13: Cascode coupling and the conventional voltage waveforms.

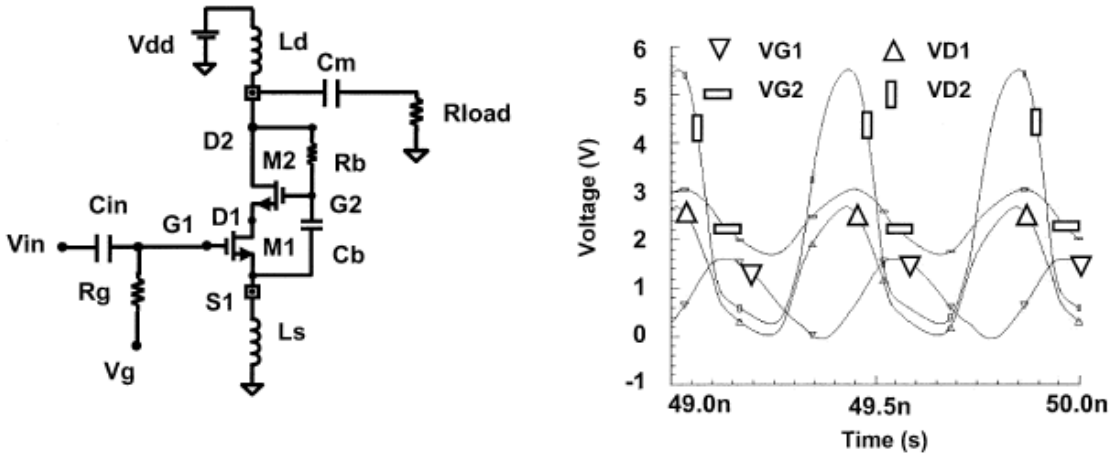


Figure 14: Self-biasing technique and the associated voltage waveforms.

2.7.2 FINITE DC-FEED INDUCTANCE IN THE CLASS-E LOAD NETWORK

In [3] it is described how a less than infinite choke-inductance can be beneficial with respect to output power and efficiency. It is stated that a finite dc-feed inductor allows the load resistance to be increased while still retaining the same supply voltage and output power (the drain-source voltage decreases when the choke decreases). An increased load resistance will decrease the impedance transformation ratio (defined as antenna impedance divided by the optimum load impedance). The loss due to this transformation ratio will then be reduced, and the efficiency increases.

The load network in the class-E amplifier also contributes to power loss, primarily due to the finite quality factor of the inductance. This power loss will be directly proportional to the ratio between this loss resistance and the optimal load resistance. Accordingly a larger load resistance will lead to higher efficiency in more than one way.

The use of a finite dc-inductance will influence the output capacitance. This needs to be compensated for by using a larger C1 capacitance or a larger transistor. By choosing to increase the transistor size, efficiency can be increased due to the lowering of the on-resistance R_{on}.

No formulas for this finite dc-inductance or the new load resistance are presented in [3].

3. AMPLIFIER DESIGN AND SIMULATIONS

3.1 DESIGN OF THE CLASS-E AMPLIFIER

To decide the transistor size, the required current and capacitance must be known. Seeing as how the drain current needed to fulfill the design requirements is dependent on the drain current fall time (eq. 6), the current is rather hard to predict. This is rooted in the fact that the drain current fall time is dependent on the current maxima. An estimate is still possible if we assume an ideal instantaneous fall time of zero. To do this calculation, the $V_{ds,sat}$ must be known. Since $V_{ds,sat}$ is the voltage across the transistors in the “on” state, and since a specific current will be needed, this voltage will decrease if the transistor size increases. A tradeoff between transistor size, needed capacitance and $V_{ds,sat}$ must be made. By simulation of different transistor sizes, the presumably obtainable $V_{ds,sat}$ voltage was set to 0.1V. To get a lower voltage than this, very large transistor sizes were needed. The value of 0.1V is also probably a bit on the optimistic side.

To do this calculation, a cascode arrangement of the transistors is presumed. Seeing as the recommended voltage across one transistor in this technology is 1.2V, a maximum voltage of 2.4 is obtainable in a cascode arrangement (see part 5.1). This means that $V_{ds,pk}$ =2.4V. This assumption might require some additional design techniques to distribute the stress on the two devices equally (also described in section 5.1). In this text it is presumed that this is possible.

With the value of $V_{ds,sat}$=0.1V, the lowest possible current to obtain the goals can be calculated (drain current fall time equals zero):

$$V_{ds,pk} = 3.562V_{cc} - 2.562V_{ds,sat} \quad (42)$$

$$2.4 = 3.562V_{cc} - 2.562 \times 0.1$$

$$\xrightarrow{yields} V_{cc} = 0.745 \quad (43)$$

$$A \equiv 0 \quad (44)$$

$$I_{DC} = \frac{P}{V_{CC}}\left[\frac{1}{1-\frac{V_{ds,sat}}{V_{cc}}}\right] = \frac{1}{0.745}\left[\frac{1}{1-\frac{0.1}{0.745}}\right] = 1.55A \quad (45)$$

The optimal load resistance for 1W output power becomes:

$$R = 0.577\frac{\left(V_{cc} - V_{ds,sat}\right)^2}{P} = 0.577\frac{(0.745-0.1)^2}{1} = 0.24\Omega \quad (46)$$

To decide the peak value of the current, the Q-factor of the total load network must be known. To achieve the highest efficiency possible, a small Q-factor should be chosen. This will however introduce the most harmonics. Since the smallest possible inductance of L2 is about 200pH, if made by several wirebonds in parallel, the smallest possible Q-factor becomes:

$$Q_L = \frac{L_2 \times 2\pi f}{R} = \frac{200pH \times 2\pi \times 5.8e9}{0.24} = 30.36 \quad (47)$$

From this, the peak value of the current is given:

$$I_{ds,pk} = I_{DC}\left[1 + 1.862\left(1 - \frac{0.5}{Q_L}\right)\right] = 1.55\left[1 + 1.862\left(1 - \frac{0.5}{30.36}\right)\right] = 4.39A \quad (48)$$

Notices that this is the smallest possible current required for an ideal case were the current fall time is zero.

From this we know that the transistor needs to be designed to handle at least 4.39A at V_{ds}=0.1V. This could be achieved with a lot of different transistor sizes and combinations of parallel devices and number of fingers. A lot of different transistor sizes and combinations were simulated in this thesis; what's presented here is limited to one of which properties are satisfactory. This transistor has a width of 28000µm, length of 0.1µm and the number of fingers is 1500.

The relationship of the drain-source current versus drain-source voltage for this specific transistor in a cascode arrangement is shown in Figure 14.

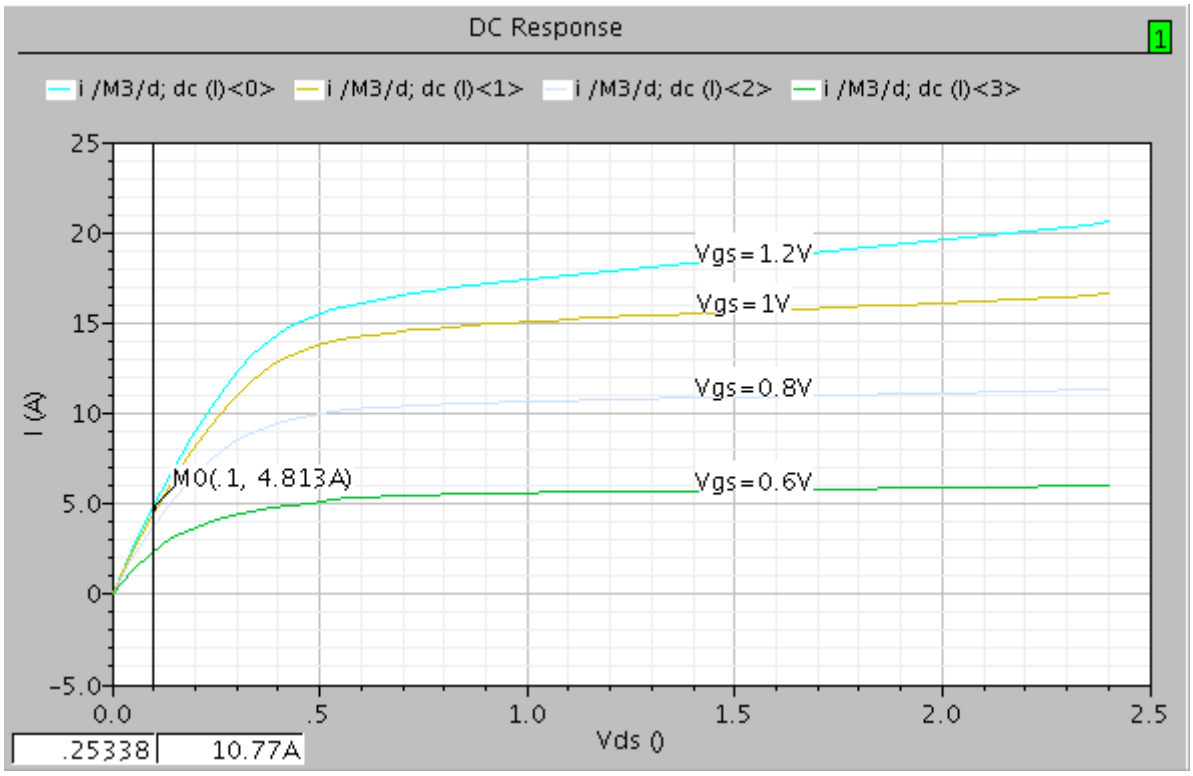


Figure 15: Cascode coupling, I_d versus V_{ds} for different values of V_{gs}, W=28000µm, L=0.1µm, number of fingers= for different values of gate-source voltages. The layout used to do this analysis is shown in

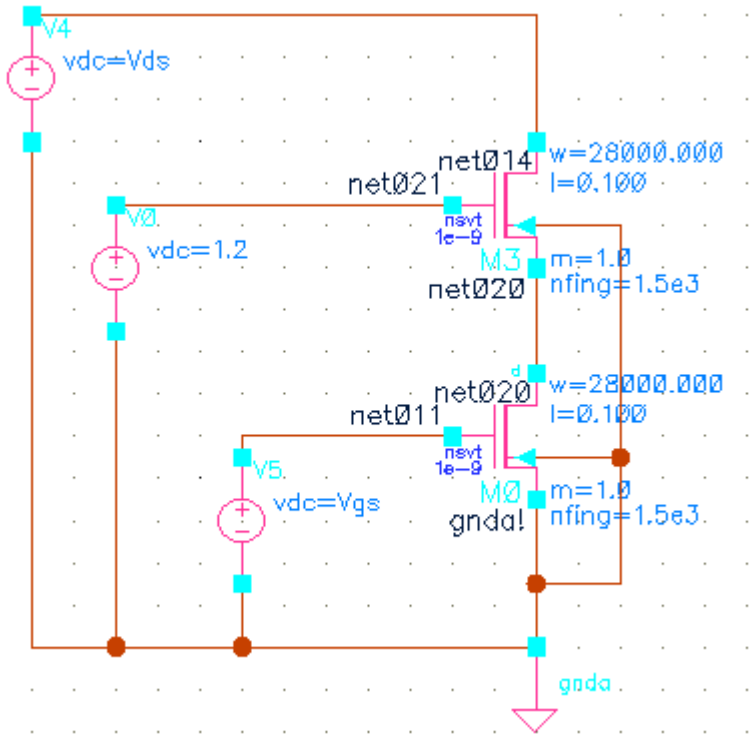


Figure 17: Circuit used for I_{ds} versus V_{gs} and V_{ds} analysis.

Of great importance when deciding the transistor and the surrounding components is the fact that the output capacitance is strongly dependent on the RF-choke inductance. In fact, this inductance is in parallel with the output capacitance of the transistor in a RF-manner.

Thus this inductor must be carefully chosen. The class-E theory is based upon this inductance to be infinite. Although a smaller inductance could be chosen if for instance the active device have a too large output capacitance. It is the total output capacitance that matters. This means that to achieve a specific total output capacitance we have the choice of either increasing the transistor size, or increasing the choke inductance (increasing the choke inductance will however not influence the total capacitance if it already is above a certain value, and the total output capacitance will in this case only be given by the transistors output capacitance). Another choice would be to use an additional capacitance as shown as C1 in Figure 6. It is beneficial to increase the transistor size with regard to the efficiency since this will decrease the $V_{ds,sat}$ voltage.

The transistor size was chosen to be so large that incrementing it further only made a minor impact on the $V_{ds,sat}$ voltage at the drain-source current of 4.39A.

The value of the capacitance was taken into consideration as well when deciding upon the transistor size. It was desired that the transistor should be large enough to minimize the additional capacitance (C1) needed.

Simulations of the total output capacitance versus choke inductance showed that values above 2nH only insignificantly increased this total output capacitance. As seen from Figure 18, im(Y22) increases by a value of $15\text{m}\Omega^{-1}$ when the choke increases from 2nH and all the way up towards infinity. In capacitance this translates to a value of about 0.41pF (using formula 21). This is a pretty small value compared to the wanted total output capacitance that soon will be shown to be 20.1pF. Thus the value of the choke inductance was set to 2nH, and thereby acted satisfactory as an infinite choke. A small value of the choke inductance also has the desired property of minimizing the power loss in this device (the power loss is proportional to the resistance of the choke; $P \propto I^2R$, and the choke resistance is proportional the choke inductance; $R = \frac{\omega L}{Q}$).

As described in 5.1, a technique also exists that uses a finite inductance instead of an infinite to increase the optimal load resistance.

Now that the transistor width and the choke inductance were decided, the only thing missing in regard to the transistor was the number of fingers. To decide this, more simulations with regard to the output capacitance had to be made. To get a feeling on how large the capacitances required need to be, formulas 19 and 20 was used:

$$C_1 = \frac{1}{2\pi f R \cdot 5.447} = \frac{1}{2\pi \times 5.8e9 \times 0.24 \times 5.447} = 20.1pF \qquad 49)$$

$$C_2 \approx C_1\left(\frac{5.447}{Q_L}\right)\left(1 + \frac{1.42}{Q_L - 2.08}\right) = 20.1pF\left(\frac{5.447}{30.36}\right)\left(1 + \frac{1.42}{30.36 - 2.08}\right) = 3.78pF \qquad 50)$$

In these equations, C1 is the total output capacitance of the transistor.

The total output capacitance of the cascode and RF-choke can be found using Y-parameters (or Z):

$$C_{out} = \frac{im(Y_{22})}{2\pi f} \quad 51)$$

$$im(Y_{22}) = C_{out} \times 2\pi f = 20.1pF \times 2\pi \times 5.8e9 = 0.7325\Omega^{-1} \quad 52)$$

The output capacitance versus number of fingers for this specific transistor is shown in Figure 19 (a choke inductance of 2nH was used in the simulations and an additional shunt capacitance of 4.95pF). The layout used during this simulation is shown in Figure 20.

For number of fingers in the range 1000-2000 the total output capacitance has values in the range 732-733mΩ^{-1} when the additional capacitance C1=4.95pF. This satisfies the required value of 0.7325Ω^{-1} found above in formula 22. This range of satisfactory number of fingers can later lead to some freedom in design layout and might also lead to a design more resistant to design variations.

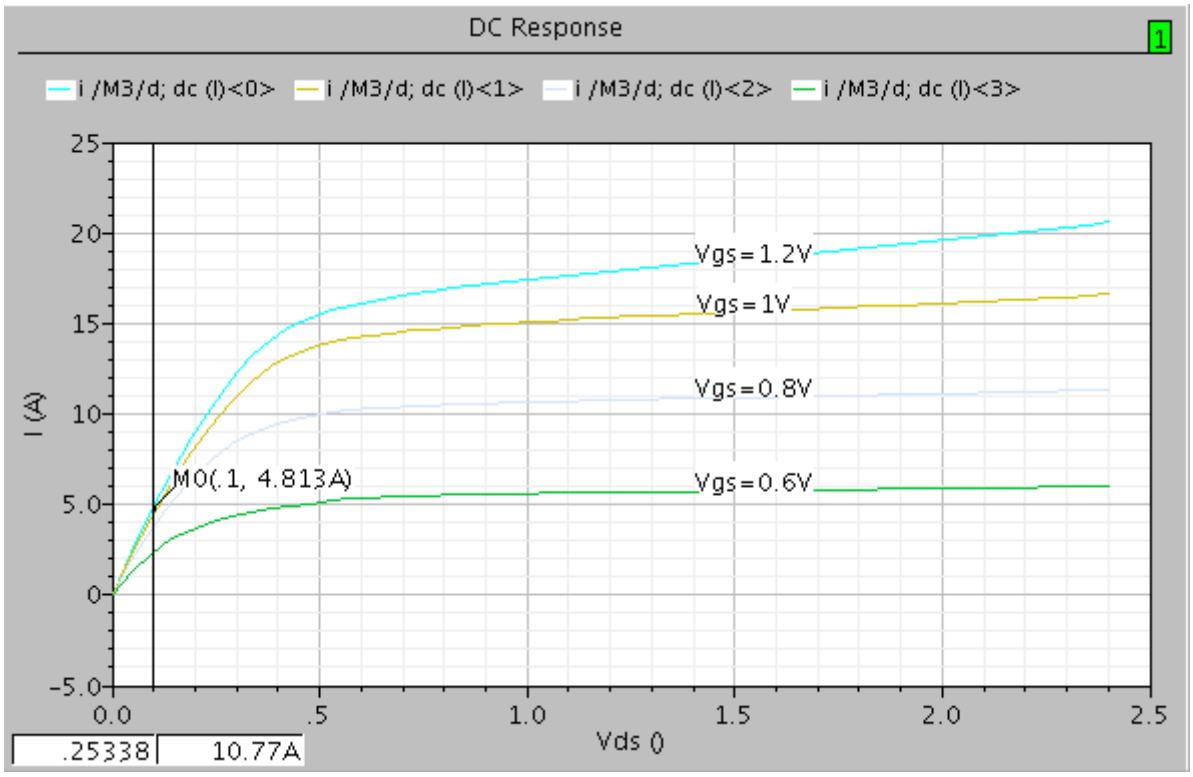


Figure 15: Cascode coupling, I_d versus V_{ds} for different values of V_{gs}, W=28000µm, L=0.1µm, number of fingers=1500.

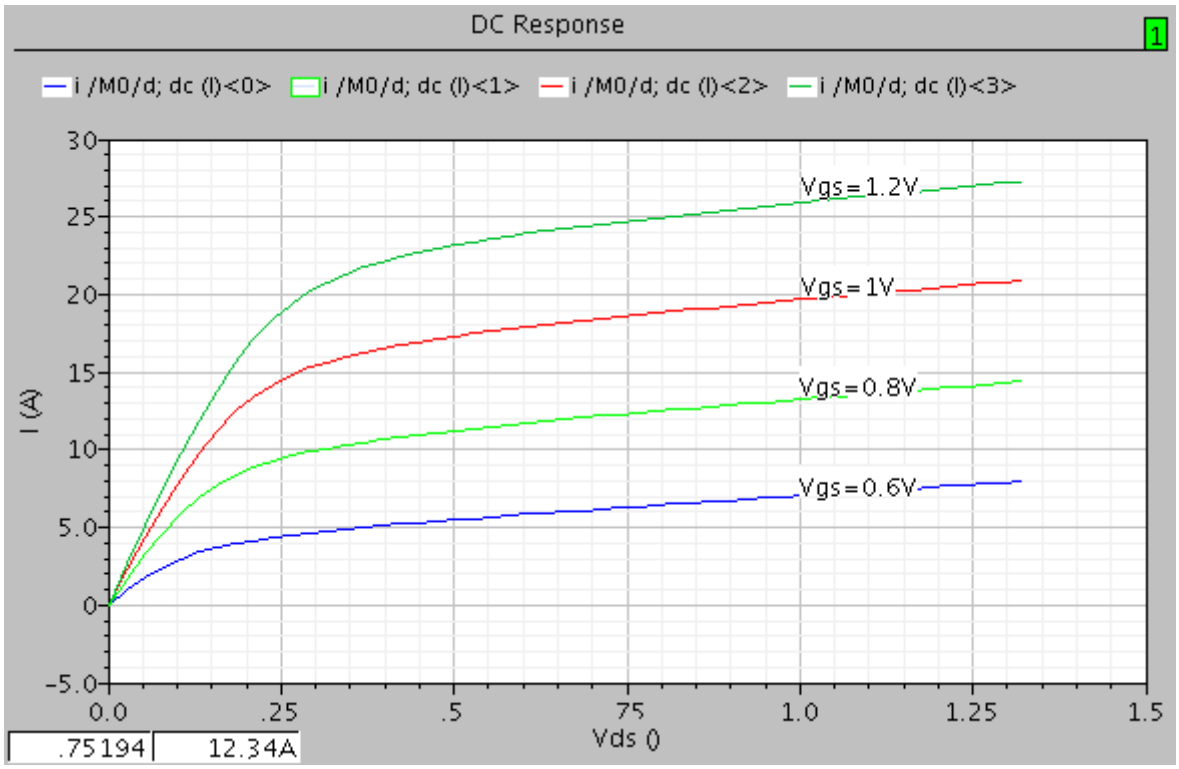


Figure 16: I_d versus V_{ds} for different values of V_{gs}, W=28000µm, L=0.1µm, number of fingers=1500 for single transistor.

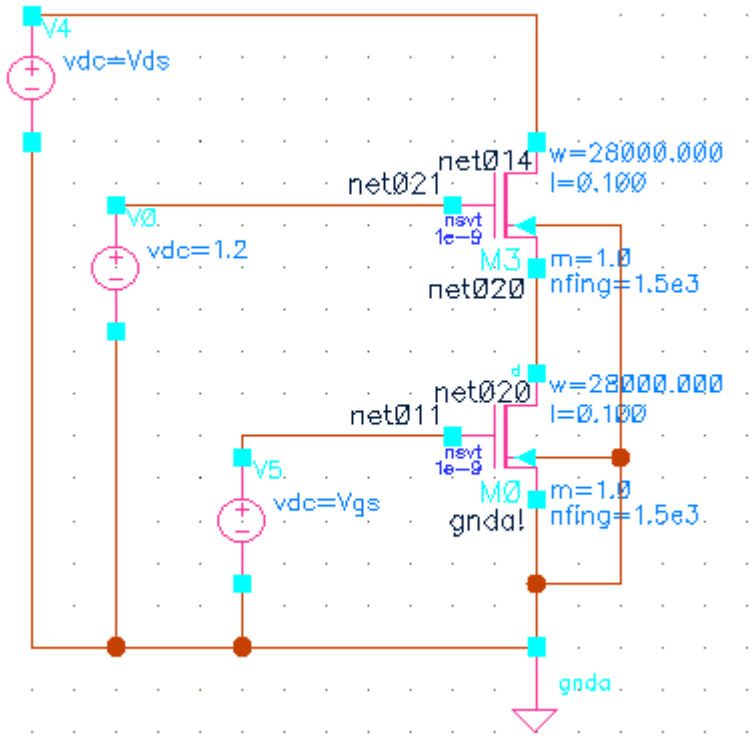


Figure 17: Circuit used for I_{ds} versus V_{gs} and V_{ds} analysis.

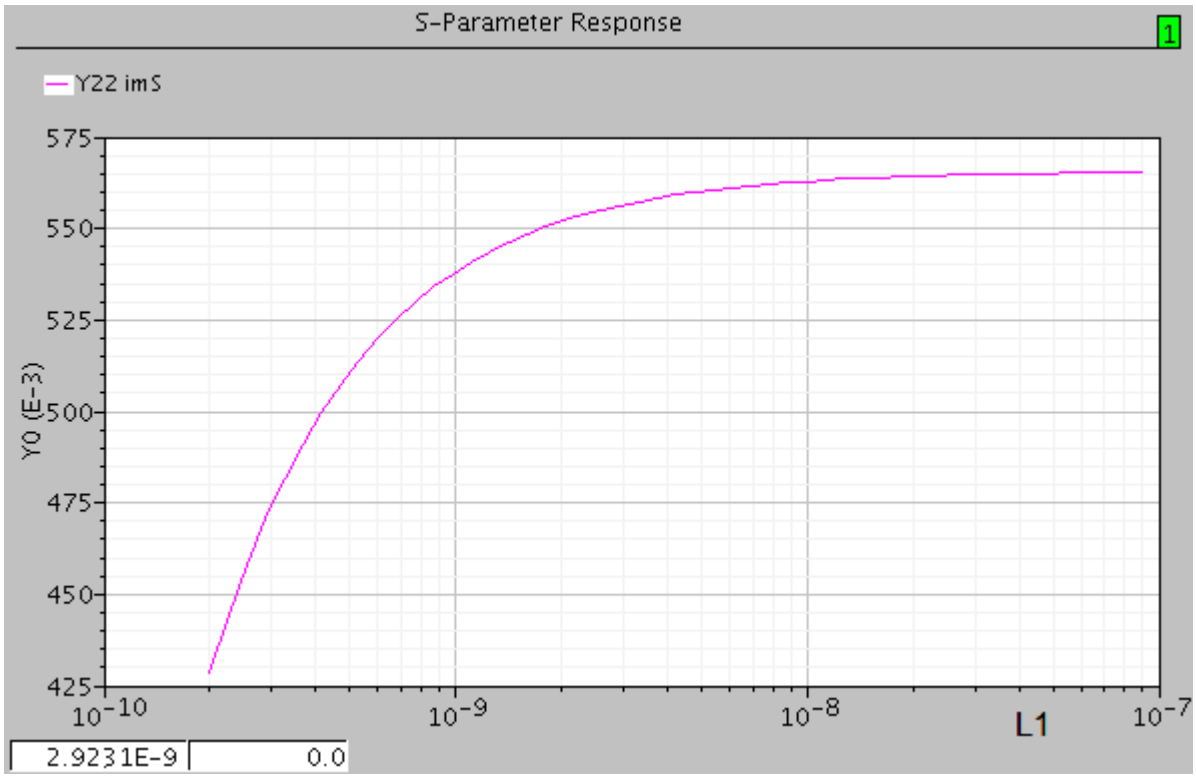


Figure 18: Total Y22 versus choke inductance, cascode coupling.

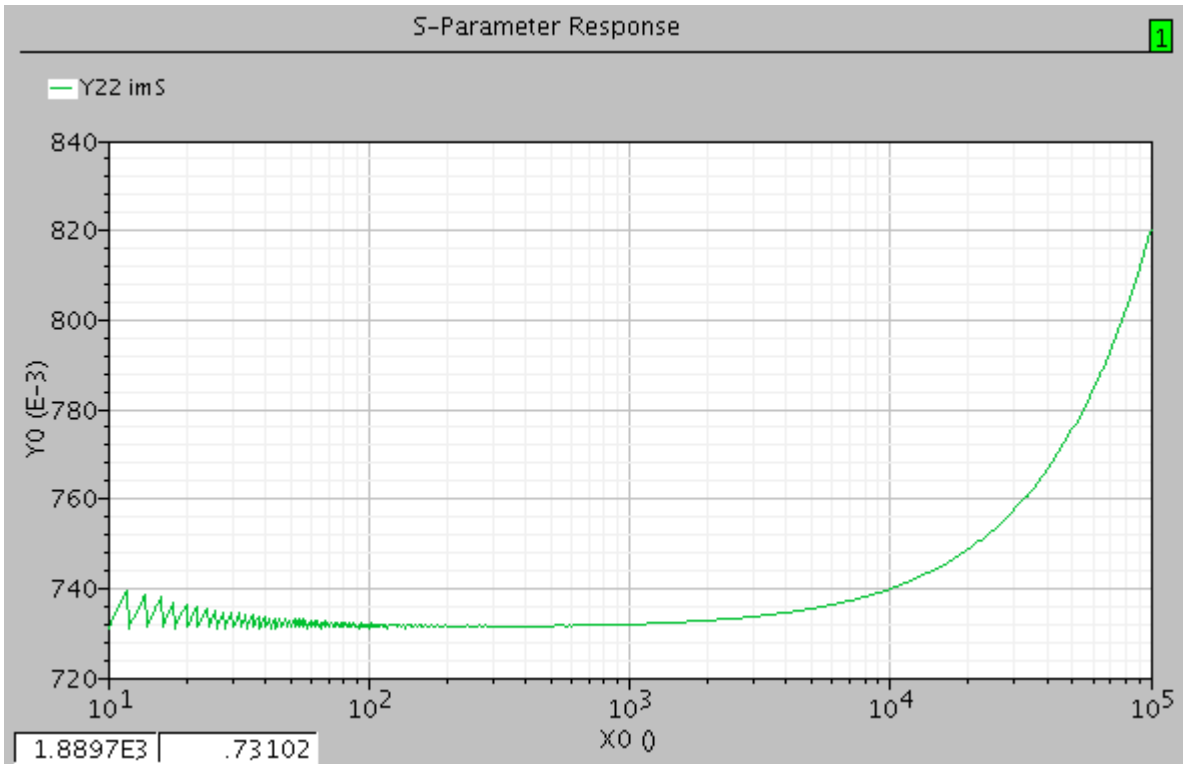


Figure 19: Total output capacitance versus number of fingers for the specific transistor of W=28000um, L=0.1um in a cascode coupling. Additional shunt capacitance of C1=4.95pF is used in the simulation. RF-choke L1=2nH.

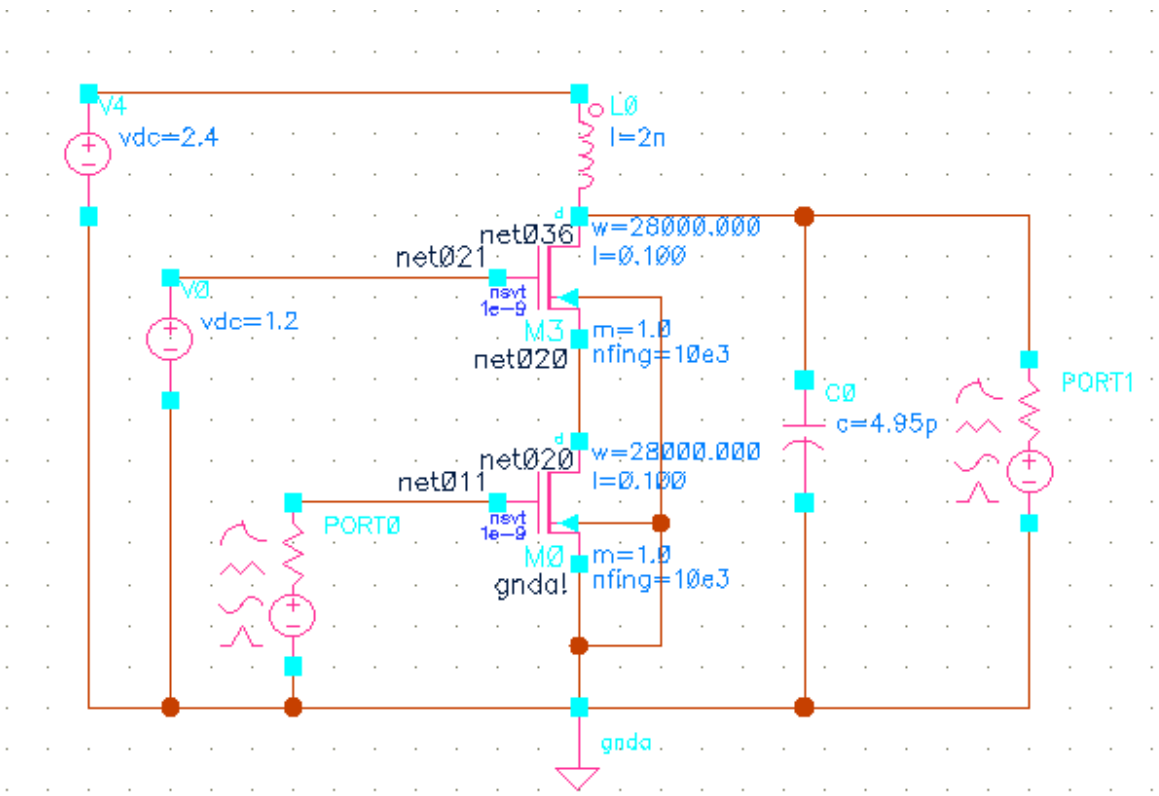


Figure 20: Circuit used for Y-Parameter analysis.

The above calculated component values are only one of many different combinations which have been simulated. Different transistor sizes, V_{ds} voltages, choke inductor values and associated values of the other components have been thoroughly simulated on. However, the best result seems to be for a lowest possible Q-factor in the load network. This gives the least restrictions on efficiency, since more harmonics are allowed. As already mentioned, this low Q-factor is determined by the lowest possible inductance of L_2=200pH, and leads to the component values calculated above.

One important fact is the dependency between loss (and thereby efficiency) and inductor size. As already mentioned, the high frequency loss increases with increased inductance. The inductor value used where RF-current runs through becomes very important in regard to efficiency. This is not only because of the linear dependency of loss and inductor size when the Q-factor remains constant, but also because the Q-factor of available components often reduces for larger values of inductance.

The class-E schematic can be seen in 3.1.1.

In the simulations in the following text the RF-choke was chosen to be 1.3nH which is a standard value (the change from 2nH to 1.3nH did not bring forward any changes in the simulations). The change from 2nH to 1.3nH will not only decrease the impedance because

of the smaller inductance, but also because of a smaller loss resistance. Seeing as only dc-current is supposed to run through this choke, the power loss will not be altered (assuming the dc-resistance in the choke remains constant).

For unknown reasons, some loss in the choke inductance had to be included to get the simulations to run successfully. This had to be done for higher values of choke inductance as well.

Since some loss had to be included in the choke, a realistic Q-factor of 250 was used to do the calculation:

$$R = \frac{\omega L}{Q} = \frac{2\pi \cdot 5.8 \cdot 10^{9} \cdot 1.3 \cdot 10^{-9}}{250} = 190m\Omega \qquad 53)$$

This is therefore no longer an ideal case, although more losses would have to be included to make it realistic.

The techniques used to separate the dc-loss from the RF-loss were not used in the design of the class-E amplifier. These techniques were first introduced late in the design of the inverse-class-D amplifier. This would however not influence the decision of which amplifier who were the best suited for the final design.

This Q-factor of the 1.3nH inductor was obtained from the Murata inductor catalog [13] for the LQW15A_10 Series (High Q/Low DC Resistance Type, 0402 Size). The exact value was not given at 5.8GHz, but looking at Figure 21, a Q-factor of 250 seems reasonable. This inductor has a rated current of 1.2A at a test frequency of 250MHz. This probably means that several larger inductors in parallel needs to be used to withstand the required current (this current will soon be presented.

From Figure 21 the inductance seems to increase with frequency. This increment will however not influence the performance as long as the design is based upon this inductance to be infinite. For a smaller than infinite inductance, it will be shown that the sole parameter that changes due to an alteration in inductance is the optimal value of the load resistance. This will only influence on the matching network design.

With the above calculated loss, three different results are presented in section 4.1, Table 4 that provides some information about the obtainable performance of the class-E amplifier. The load resistance is optimized for highest possible efficiency.

A lot of simulations were done to provide the values in Table 4 (section 4.1). The value of C_1 and L_1 were found to be the least critical ones (if the loss in L_1 remains constant). The rest of the components have very critical values, and a small change make a big difference in the performance.

C_2 and L_2 control the wave-shape of the drain-source voltage. This can also be seen by the design guidelines in Appendix A, Figure 40. They can only be changed a bit before the wave-shape loses its characteristic class-E shape. It was found that the voltage across the cascode in the "on" state is strongly dependent on L_2. For highest possible efficiency, this voltage should be low. Because of the non-ideal behavior of the active devices, this voltage also controls the current drawn by the active devices (on-resistance ≠ 0). This means that high current (which leads to high output power) must be sacrificed in regard to get a high efficiency. A low value of L_2 gives a high voltage across the devices in the "on"-state, and thereby a high output power but a small efficiency. This can be seen in case number two of Table 4 (section 4.1), and some of the simulation waveforms can be seen in appendix A, Figure 41. A small value of L_2 also leads to smaller amplitude of the drain-source voltage which allows an increment in supply voltage, and thereby an increment in load resistance.

The opposite result occurs when L_2 takes a slightly higher value. This is shown in case three in Table 4. Simulation waveforms are shown in Appendix A, Figure 42. An attempt to obtain concurrent high efficiency and high output power is shown in case number one in the same table. Some of the voltage waveforms and the first five harmonics output power for this case are shown in Figure 29. For this case both the efficiency and output power demands are reached. The drawback is the very low load resistance which will be hard to match to 50Ω. Such a match is in theory easily done by a two component matching network. The problem is that this match will be very narrow banded, and very sensitive to component variations. Though this match will in reality need to be made by more than two components and will lead to more loss.

Also, this simulation is made without any loss in the bond-wires. From supervisor Oddgeir Fikstvedt at Texas Instruments the Q-factor of 150 was given for the bond-wires. The loss resistance in the bond-wires can therefore be calculated to be:

$$R = \frac{\omega L}{Q} = \frac{2\pi \cdot 5.8 \cdot 10^9 \cdot 0.2 \cdot 10^{-9}}{150} = 48.6m\Omega \approx 50m\Omega \qquad 54)$$

Since this loss resistance is almost one third of the desired load resistance, it will have a heavy impact on both efficiency and output power. To obtain the same total load, the load resistance must be decreased by 50mΩ to 120mΩ. This means that about 50x100%/(120+50)=29.41% of the total output power is dissipated in the output bond-wiring. This will probably destroy the circuits.

The simulations described above were done without the extra bond-wire inductance of 200pH in the RF-choke. This inductance has however no influence on the performance except when the additional loss resistance of 50mΩ is included.

A simulation that included bond-wire losses of 50mΩ in both the RF-choke and in L_2 gave the results in section 4.1, Table 5. The load used was 170-50=120mΩ, and was also here found to be the most optimal one in regard to efficiency. Because of the voltage loss in the RF-choke, the supply voltage could be increased to 1.2V. The output power for this case is 0.785W, which fits well with the assumed power (1.108Wx(1-0.2941)=0.782W). The total power delivered to the inductor L_2 and the load resistance is $P_{Tot} = \frac{0.785}{1-0.2941} = 1.112W$, which means that 1.112-0.785=0.327W is dissipated in the bond-wire L_2.

Simulations with and without bond-wire loss, and with a higher RF-choke inductance have also been done. These simulations verify that the choke of 1.3nH is sufficiently large to act as an infinite choke, and the results become the same as the ones with 1.3nH. The same losses were included in the simulations with 1.3nH inductance as for the higher valued inductances to get comparable results.

The power gain requirement of 25dB is far from obtained in all the three cases. This probably means that the input current is too high. This can possibly be solved by proper design of input matching network and driver network.

As described in section 5.1, one way to enlarge the optimal load resistance might be to use a less than infinite RF-choke. Table 6 (section 4.1) shows the best simulation results in regard to both output power and efficiency when smaller RF-choke is used. The load resistance is optimized for highest possible efficiency. In this table a loss resistance of 190mΩ in the choke is used to give comparable results with Table 4, case 1. This loss resistance is unrealistically high for these small inductances, but it provides a good comparison. As one can see by Table 6 case 2, there is an increase in optimum load resistance of 10mΩ when the inductance is decreased to 0.2nH.

To give more realistic results for the case of decreased choke inductance, simulations were also done with 50mΩ loss resistance in L2 and with a loss resistance in the choke calculated by a Q-factor of 150 in the bond-wire (200pH) and a Q-factor of 250 on the remaining inductance. This is shown in section 4.1, Table 7. Case 1 and 2 shows great improvements compared to case 1, Table 5. The optimum load resistance is more than twice the size, and the output power and efficiency has greatly improved because of less loss in the inductors.

Sadly one cannot decrease the RF-choke too much. The combination of small inductance and small loss resistance destroy the characteristic waveforms of the class-E amplifier because the total output capacitance becomes too low. To get around this, one possibility is to increase C1. This is done in Table 7, case 3. As one can see from this table, this yields much better performance than the comparable case 1 in Table 5. Here we have the lowest RF-choke, and thereby the least loss such that the efficiency and output power becomes the highest ones obtained (where realistic loss is included in both L2 and RF-choke). There is however a disadvantage compared to the other cases in that such a high capacitance C1 is needed. Also, the optimal load resistance was higher in the two previous cases.

It should be mentioned that it was impossible to exchange some of the high power obtained in this last case to higher efficiency by changing L2.

To sum it up, there is a possibility to enlarge the optimal load resistance. The increase obtained in the simulations is maximum 150% for comparable cases (from 120mΩ to the maximum value of 300mΩ). With this increase in load resistance, the dissipated power in L2 decreases to 50x100%/(300+50)=14.28%. This is still much and could still lead to damage of the device.

The only solution for this problem is to use another technology that will utilize a much higher load resistance. Such a technology could be a differential one, like the inverse class-D, because of the doubling in allowable voltage swing (Since $P \propto \frac{V^2}{R}$, a doubling in voltage will lead to four times the resistance).

Another disadvantage of the class-E amplifier compared to the inverse class-D is the impact that a ground inductance will have on the performance. A ground inductance needs to be included in a complete design between all the on-chip grounds and the external ground. This is because the grounding of the chip is done through the bond-wires which will lead to some additional inductance. Because of the differential manner of the inverse class-D amplifier, the number of grounds internally on the chip is minimal. They will also appear symmetrically. Together this will lead to less influence on the performance compared to the class-E.

Simulations on the class-E amplifier were also done including a ground inductance of 100pH. This inductance was found to be totally devastating performance-wise.

The smallest possible ground inductance will depend on the packaging technique. Supervisor Oddgeir Fikstvedt suggested the value of 100pH for this ground inductance.

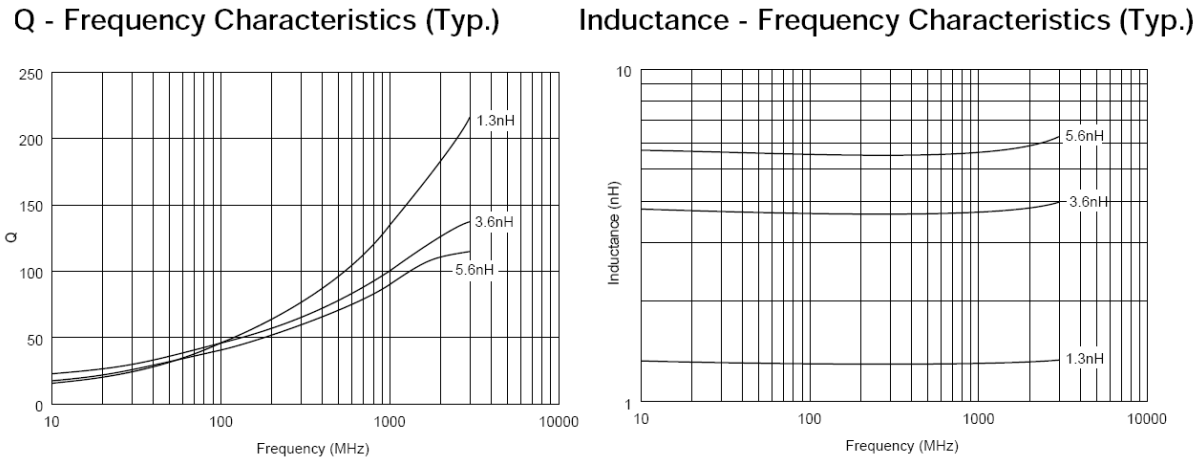


Figure 21: LQW15A_10 Series from Murata.

It should be mentioned that some time was wasted on the transient response in the beginning of the class-E design. This was due to the fact that the first picoseconds of the transient response showed way too high drain-source voltages. A decrease of the choke inductance was the only way to minimize this stabilization time in the simulations. Later it was decided to overlook this phenomenon, and only concentrate on the steady-state analysis. This was justified by looking at this transient response as a phenomenon that occurred because of the sudden idealistic turn-on of the transistors (the drive signal was modeled as a perfect square waveform) and because the simulation started with no charge on the components, and with a probably imperfect model of the transistor as a switching device (at least for high harmonics). In real life this idealistic “turn on” is considered highly unlikely. In fact, the drive signal probably begins like a weak sinus-like waveform and never reaches the idealistic square shape. A totally square shaped waveform would require matching for an infinite amount of harmonics, which is highly unlikely to achieve.

Simulations of a sinusoidal drive signal confirmed a greatly reduced stabilization time.

Another reason worth mentioning that also justifies the use of only steady-state analysis is that the transistor breakdown probably is dependent on the amount of time the device stays with too high voltage. This is though only an assumption, and is not to be mistaken for a fact.

3.1.1 CLASS-E AMPLIFIER SCHEMATIC

The schematic used for the class-E simulations is shown below in Figure 22. The component values used in the simulations can be found in section 4.1 together with the belonging output power and efficiency.

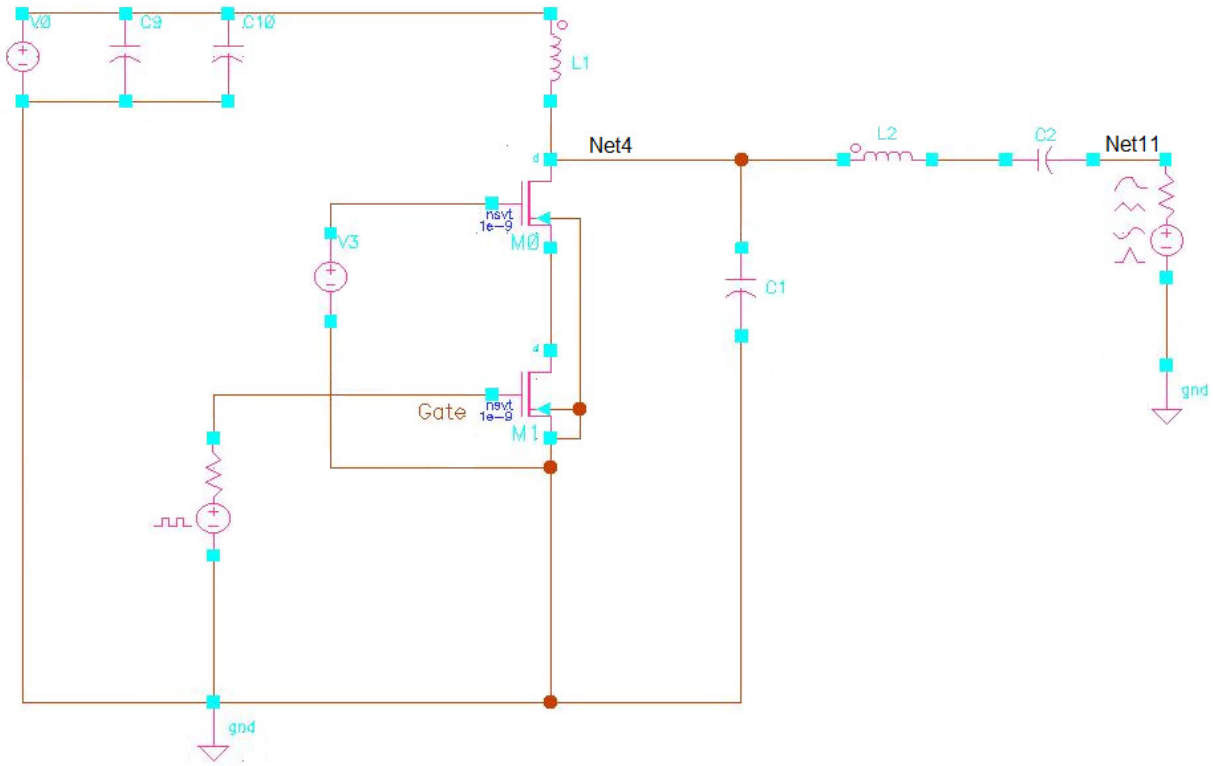


Figure 22: Class-E amplifier

3.2 DESIGN OF THE INVERSE CLASS-D AMPLIFIER

The design of the class-D^{-1} amplifier was the most time-consuming part of this thesis. It instantly showed very promising behavior (in comparison with the class-E amplifier) and was therefore chosen to be the best solution. There was no time to make a prototype, but a design which includes all realistic losses and takes in to account non-ideal sources and grounds is completed.

The cascode coupling was used to maximize the allowable voltage swing. Two main design options were investigated. One was to use two standard transistor devices in the cascode, and the other one was to use a standard device as the common-source transistor and a thick-oxide device as the common-gate transistor. This last possibility was utilized as a way to both benefit from the high breakdown voltage of the thick-oxide, and at the same time utilize the better high-frequency performance of the standard device. After a lot of simulations, it was decided that the cascode with only standard devices was the best way to go because of the tough efficiency requirements (the poor RF-performance of the thick-oxide had too much impact on the overall performance, to reach the design goals one could not make any sacrifices in regard to efficiency).

The design method was to start with a simple design, identical to Figure 10b, and then iteratively transform it more and more into a realistic design. This was done by adding the required bondwires, and by adding realistic losses in these and all the other inductances. The voltage sources were made more realistic by adding the inductance from the required bondwires to get the voltage from off-chip to on-chip. Realistic loss was also included for these inductances.

For comparison with the class-E design, it should be mentioned that a peak efficiency of 63.48% with an output power of 30.03dBm was obtained when using an almost ideal circuit with only a small loss of 190mΩ in the choke inductances. The optimal load resistance was 2.5Ω. This circuit can be seen in Appendix A, Figure 45 and the corresponding waveforms can be seen in Appendix A, Figure 46. The comparable class-E design (Table 4, case 1), gave a peak efficiency of 51.42% with an output power of 30.44dBm (1.108W) and an optimal load resistance of only 170mΩ. It is from these simulations obvious that the inverse class-D amplifier is superior compared to the class-E amplifier for this configuration.

To make a realistic design, it is as already mentioned in 3.1, important to distinguish between the internal and the external ground. The internal ground on-chip will have a small series inductance out of the chip to the external ground off-chip. To have a good ground, this inductance should be as small as possible. By having several ground connections from the internal to the external ground it should be possible to achieve a ground inductance of about 100pH (this value was suggested by supervisor Oddgeir Fikstvedt).

The ground inductance has an influence on the waveforms. Because of the ground inductance, the voltage waveforms get negative values for part of the signal period. This can be seen in Appendix A, Figure 43, where the voltage waveforms of the finished design are shown with and without the ground inductance (these voltage waveforms belong to the schematic in Figure 28). The impact of the ground inductance is much less noticeable for this differential topology than for the class-E amplifier where it was found to be totally destructive. The output power and the belonging efficiency for the finished inverse class-D amplifier without the ground inductance are shown in appendix A, Figure 44.

On the way to a finished design it was decided to raise the voltage limit by 10%. This is the normal limit for staying within the 10 years guaranty [1]. Efficiency wise, it would be stupid not to take advantage of this. This means that the maximum voltage across one transistor is raised from 1.2V to 1.32V, which means that the drain voltage of the total cascode can be 2.64V (with the previous mentioned self-biasing technique to distribute the voltage stress on the devises equally).

An estimate on the current (and the load resistance) was made to choose the most suitable transistor size. The previous presented formulas numbered 30, 31, 38 and 39 were used for this calculation:

With a maximum peak voltage of 2.64V, the average voltage V_{dd} could be calculated:

$$V_{dd} = \frac{V_{peak}}{\pi} = \frac{2.64}{\pi} = 0.84V \qquad 55)$$

With an output power of 1W, the optimal load resistance becomes:

$$P_{out,f_c} = \frac{\pi^2 {V_{dd}}^2}{2R_L} \quad \xrightarrow{yields} \quad R_L = \frac{\pi^2 {V_{dd}}^2}{2P_{out,f_c}} = \frac{\pi^2 0.84^2}{2 \cdot 1} = 3.48\Omega \qquad 56)$$

This leads to a dc-current of:

$$I_{DC} = \frac{\pi^2 V_{dd}}{4R_L} = \frac{\pi^2 \cdot 0.84}{4 \cdot 3.48} = 0.595A \qquad 57)$$

And a necessary peak current of:

$$\hat{I}_d = 2I_{DC} = 2 \cdot 0.595 = 1.191A \qquad 58)$$

With this knowledge, a lot of different transistor sizes were simulated. To get a high efficiency it was important to keep the "on" voltage as low as possible. This means a large transistor width. At the same time was it important to keep a low output capacitance so that it was possible to make the resonance load circuit. It was found that it was advantageous to not use devices in parallel to keep the output capacitance as low as possible. In the finished design a width of W=8000µm with number of fingers=2000 was used. The I_{ds} versus V_{ds} characteristic for this transistor size can be seen in Figure 23. The circuit used to simulate this characteristic is shown in Figure 24. As one can see from Figure 23, the peak current of 1.191A is reached for a V_{ds} voltage of ~0.05V. This will mean a V_{ds} voltage of about 0.1V for the total cascode. It was found that an increase in transistor size above W=8000µm did not lead to improved efficiency. It did on the other hand decrease the required size of the resonance inductance (L in Figure 28) which was a disadvantage.

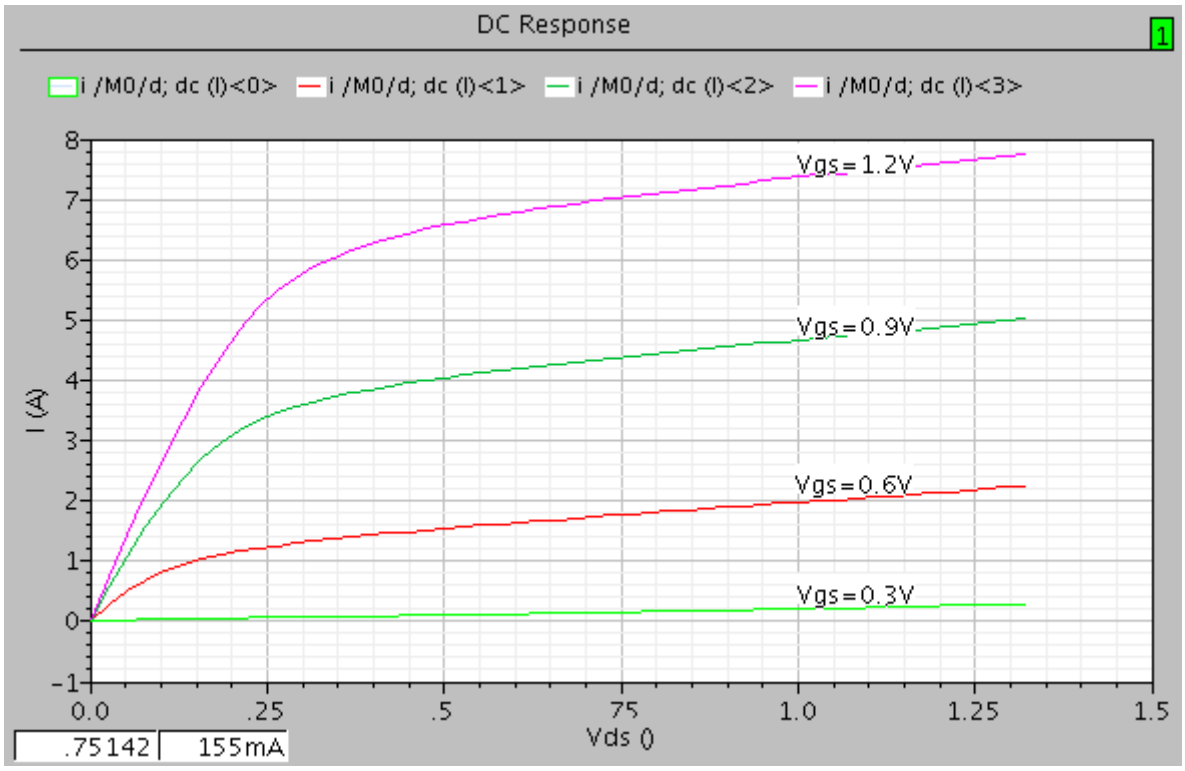


Figure 23: I_d versus V_{ds} for different values of V_{gs}, W=8000µm, L=0.1µm, number of fingers=2000.

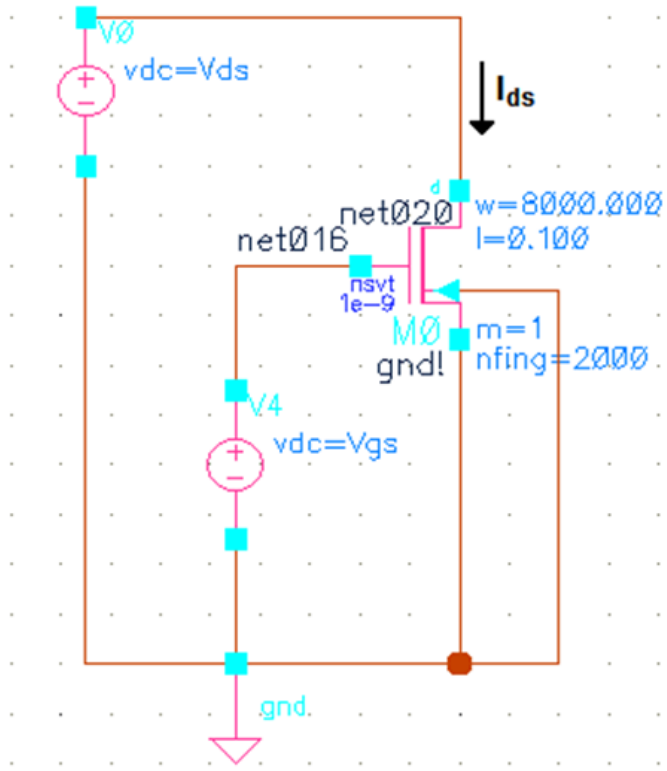


Figure 24: Circuit used for I_{ds} versus V_{gs} and V_{ds} analysis.

3.2.1 OUTPUT NETWORK

The load network was constructed such that the output is single-ended. This was done with the help of a first-order balun like the one described in 2.1.5. This balun was optimized in regard to highest possible efficiency, which did not equal the highest power (the waveform shaping this balun contributed to was utilized in the favor of efficiency). Because of this, and the fact that some inductor loss was included, the values in the finished design were not exactly as could be calculated by the formulas in section 2.1.5.

The output network with the balun and with the output bondwire inductances is shown in Figure 25. The output bondwire is needed to transfer the signal from on-chip to off-chip. To make this inductance as invisible as possible at the fundamental frequency, a capacitance (cc in Figure 25) was included in series to make a resonance at the fundamental frequency. However, because of the noninfinite Q-factor of this bondwire, this bondwire has an impact on both the optimal load resistance and of course on the efficiency. The resistances r (in Figure 25) is applied so that the Q-factor of the bondwire equals 150. The resistance r is calculated using equations 23 and 24:

$$R_s = \frac{2\pi f L}{Q} = \frac{2\pi \cdot 5.8GHz \cdot 0.2nH}{150} = 48.58m\Omega \quad (59)$$

$$R_{shunt} = r = (1 + Q^2) \cdot R_s = (1 - 150^2) \cdot 48.58m\Omega = 1.093K\Omega \quad (60)$$

The dc-resistance is included in the dc-feed inductance which is not shown in Figure 25.

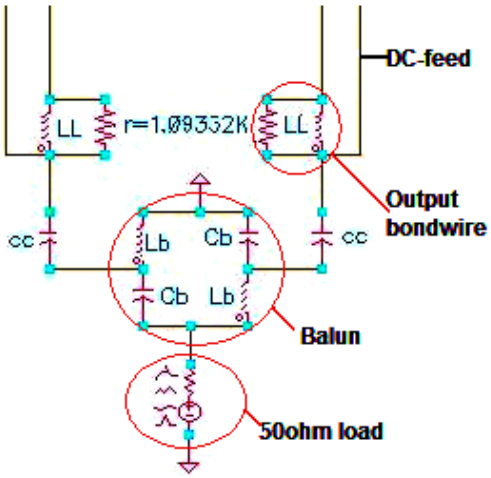
The balun inductance, L_b, is small (Lb=240pH) and can be made by a microstrip line. The Q-factor of such a line will depend on the PCB-technology/materials chosen. The exact Q-value is rather hard to foresee, so the loss resistance was chosen to be 50mΩ (which means a Q-factor of 175). This loss resistance is included internally in the inductance, and cannot be seen in Figure 25.

The component values of the output network are listed in Table 1.

As one can see, the dc-feed is applied through the load network which differs from the original inverse class-D design in Figure 10b. This will soon be explained.

It was desirable to reduce the number of required package pins. It was therefore interesting to see if it was possible to feed the required dc-current through the output network. This would save the two package pins which were needed to connect the two differential drains to the two dc-feed inductors off-chip (see Figure 10b). The dc-feed inductors could also been made entirely with bondwires, but it still needs some kind of connection from the outside.

It was found that it was possible to feed the dc-current trough the output network. This required two dc-feed inductors off-chip to prevent shortening of the output RF-power. It also required two dc-block capacitors to prevent dc-voltage at the load resistance. The capacitors used to resonate out the bondwires at the outputs were used for this (cc in Figure 25)



LL	200pH
r	1.09332KΩ
cc	3.76pF
Lb	240pH, 50mΩ
Cb	3.2pF
Load-resistance	50Ω

Figure 25: Output network.

Table 1: Output network component values.

3.2.2 THE RESONANCE LOAD FILTER

The resonance filter to short out all the harmonics was made out of the output capacitance of the cascode and a small on-chip inductance. This inductance can be seen as the component named L in the finished schematic shown in Figure 28. This internal inductance had to be very small because of the high output capacitance of the transistors. The optimal value of this inductance is as low as 80pH. A higher inductance totally destroys the class-D^{-1} waveforms and thereby the efficiency. Since the on-chip inductances have a very small Q-factor, it is on one side desired to have a small inductance. However, the problem is that one cannot make an arbitrarily small inductance within an integrated technology like this. However, to achieve the efficiency and power goals the inductance must be this small. In a layout this inductance probably must be made by several larger inductances in parallel. The loss resistance of this inductance was calculated to be 146mΩ. This is calculated from a Q-factor of 20 (this Q-factor was suggested by supervisor Oddgeir Fikstvedt and applies for all the on-chip inductors).

3.2.3 DRIVERS AND INPUT MATCHING

The drivers used to introduce the appropriate driving signal are made as inverters. Two inverters are needed, one for each input. The drivers can be seen in the finished schematic in Figure 28. A magnified section of this figure showing only one of the inverters is shown in Figure 26. The component values are listed in Table 2.

Ideally an inverter is capable of making a perfect square-shaped driving signal. The higher the inverter load is, the smaller the inverter transistors need to be. Because of the high frequency, and the large input capacitance of the transistors, it is impossible to make the input impedance of the main amplifier high for all odd-harmonics in the ideal square driving signal. This is why the driving signal becomes more of a sinus than a square-shaped waveform. The resulting driving signal can be seen as signal-net01332 (the orange graph) in Figure 30.

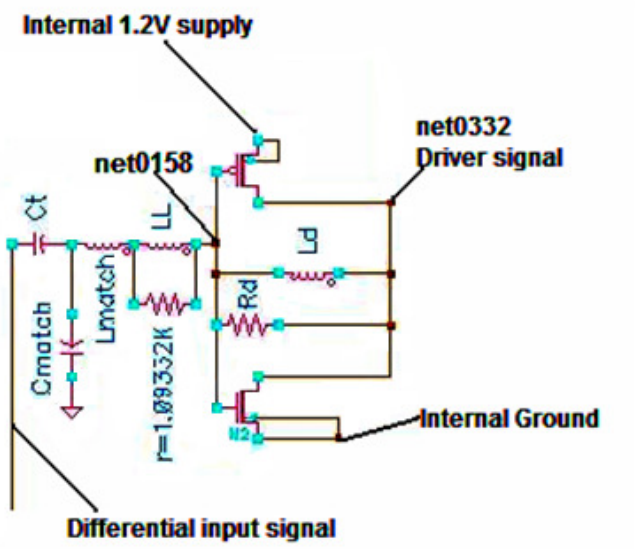
At first the inverters were designed by them self, but since they are completely dependent on the input impedance of the main amplifier, it was found that it was easier to design them directly connected to the inputs of the main amplifier. Because the pMOS transistor is weaker than the nMOS transistor, a rule of thumb is that the pMOS should be 3 times the size of the nMOS. In the finished design the size of the nMOS became 20µm, while the pMOS became 100µm. It was found that the size-difference between them had more influence on the stability than the actual shape of the driving signal. The sizes were thereby optimized for best possible stability. The resistance R_d and the inductance L_d of Figure 26 are used as part of the stabilization network of the total amplifier. Many different types of stabilization techniques were investigated, but this type of stabilization was the most efficient. The inductance L_d had also a great positive influence on the input impedance of the driver. This inductance partly resonates out the input capacitance of the driver so that the matching network was easier to make. Even though the on-chip inductances have a very low Q-factor (as previously described about 20) this coupling does not contribute to an excessive efficiency loss (of course it contributes to some loss, but that is also why it helps stabilizing). The Q-factor is implemented as a loss resistance of 911mΩ internally in the inductance (so it cannot be seen in Figure 26). This loss resistance is calculated with a Q-factor of 20.

The inverters were originally biased at 0.6V at the input gate node. This biasing is needed to give an appropriate driving signal at low input signals. Because of the inductor in the driver feedback and the inductor in the main amplifier feedback, this was no longer needed. The driver gate is biased through the dc-voltage level at the main amplifiers cascode midpoint; this can be seen by looking at the finished schematic of the total amplifier in Figure 28. This means that a voltage divider providing the 0.6V bias is no longer required.

The bondwire inductance LL in Figure 26 have a loss-resistance r=1.093KΩ. This is calculated with a Q-factor of 150 like the output bondwire described in 3.2.1. It is also included a loss-

resistance in the off-chip inductance Lmatch of 50mΩ. Lmatch is a small inductance and is part of the input matching network. This inductance is not critical for the performance of the amplifier, but it does improve the matching. The loss-resistance of 50mΩ is probably exaggerated (compared with the Q-factor used for the microstrip inductance in the balun, L_b), but it is better to be on the safe side. By simulations it was found that the value of this loss-resistance has almost no influence on the efficiency or stability anyhow.

Cmatch is a capacitor that provides the rest of the matching to 50Ω. Ct is a dc-block capacitor that separates the dc-voltage from the 50Ω input signal source.



Ld	500pH, 911mΩ
Rd	162Ω
LL	200pH
r	1.09332KΩ
Lmatch	45pH, 50mΩ
Cmatch	1.12pF
Ct	12pF
Width pMOS	100µm
Width nMOS	20µm

Figure 26: The input driver. Magnified lower-right part of the circuit in Figure 28.

Table 2: Driver network component values.

3.2.4 STABILITY

The toughest part of the design process was to make the amplifier stable. A lot of efficiency was lost in the process. The unstability was both at higher and lower frequencies than 5.8GHz.

One drawback with Cadence is that one can only do stability analyses on a single-ended topology and not on a differential. The design was made with differential inputs and a single-ended output, so the solution was to use an ideal balun at the inputs when doing the stability analysis. The original matching was however reduced (of unknown reasons) by this process, but it was decided that the matching was still acceptable enough to use the stability results, efficiency results, power results and so forth.

The stability analysis was done as a large signal analysis. A small signal analysis will for a switched amplifier give the wrong impression of the amplifier to be stable for all frequencies.

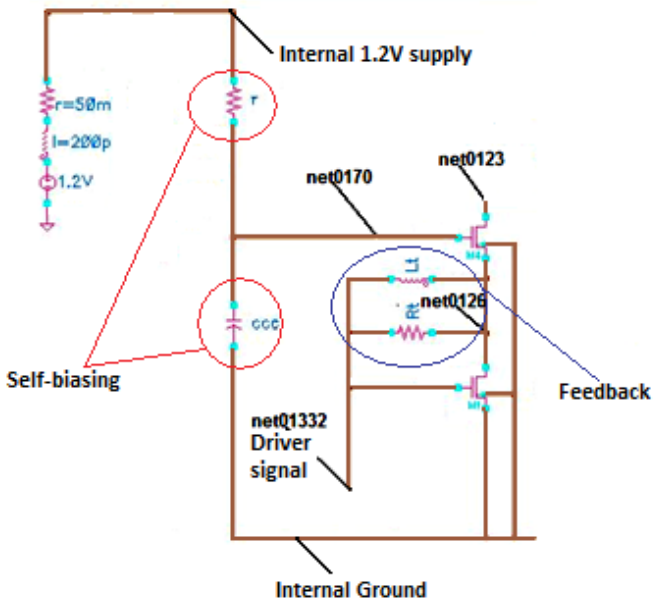
Many different types of feedback architectures were investigated. The method described in theory 2.2 was found to be the best in regard to efficiency. This method was used in the main amplifier, but also in the driving network as described previously. This method has the great advantage of both stabilizing and making the input matching easier. This feedback can be seen in Figure 27, and the corresponding component values are listed in Table 3.

In the main amplifier the feedback inductance Lt (Figure 27) resonates out the input capacitance of the cascode completely, which makes the drivers easier to design. A loss-resistance of 392mΩ is included in this inductance, which is calculated from a Q-factor of 20.

The self-biasing has also a great influence on the stability; this is described in the following chapter.

3.2.1 Self Biasing

The self-biasing network is included to distribute the voltage stress on the two transistors in the cascode equally as described in 2.7.1. The self-biasing network can also be seen in Figure 27. The self-biasing provides a voltage swing at the gate node of the common-gate transistor, allowing the drain-source voltage of the common-source transistor to reach the maximum allowable voltage. The self-biasing signal can be seen in Figure 30, net0170 (the yellow graph). This self-biasing network has a lot to say for the stability. It is thereby both optimized with regard to stability as well as the voltage waveforms (such that we stay within the design limits).



Lt	215pH, 392mΩ
Rt	170Ω
r	2Ω
ccc	7pF

Figure 27: One of the cascodes in the main amplifier, showing the feedback and the self-biasing.

Table 3: The component values of Figure 27.

3.2.2 The resulting Inverse class-D schematic

The finished class-D^{-1} amplifier schematic can be seen in Figure 28. This schematic fulfils the design goals of a PAE above 50% and an output power of 30dBm. It has a single-ended output where the optimal load resistance is matched to 50Ω. This schematic has an ideal balun at the input, which was needed for the stability and efficiency measurements. In these measurements the input signal source had an impedance of 100Ω so that the two differential input nodes should have an impedance of 50Ω. As already described, some of the input match was lost because of this balun, but the matching was considered good enough to use the stability and efficiency results.

The two differential inputs are matched to 50Ω.

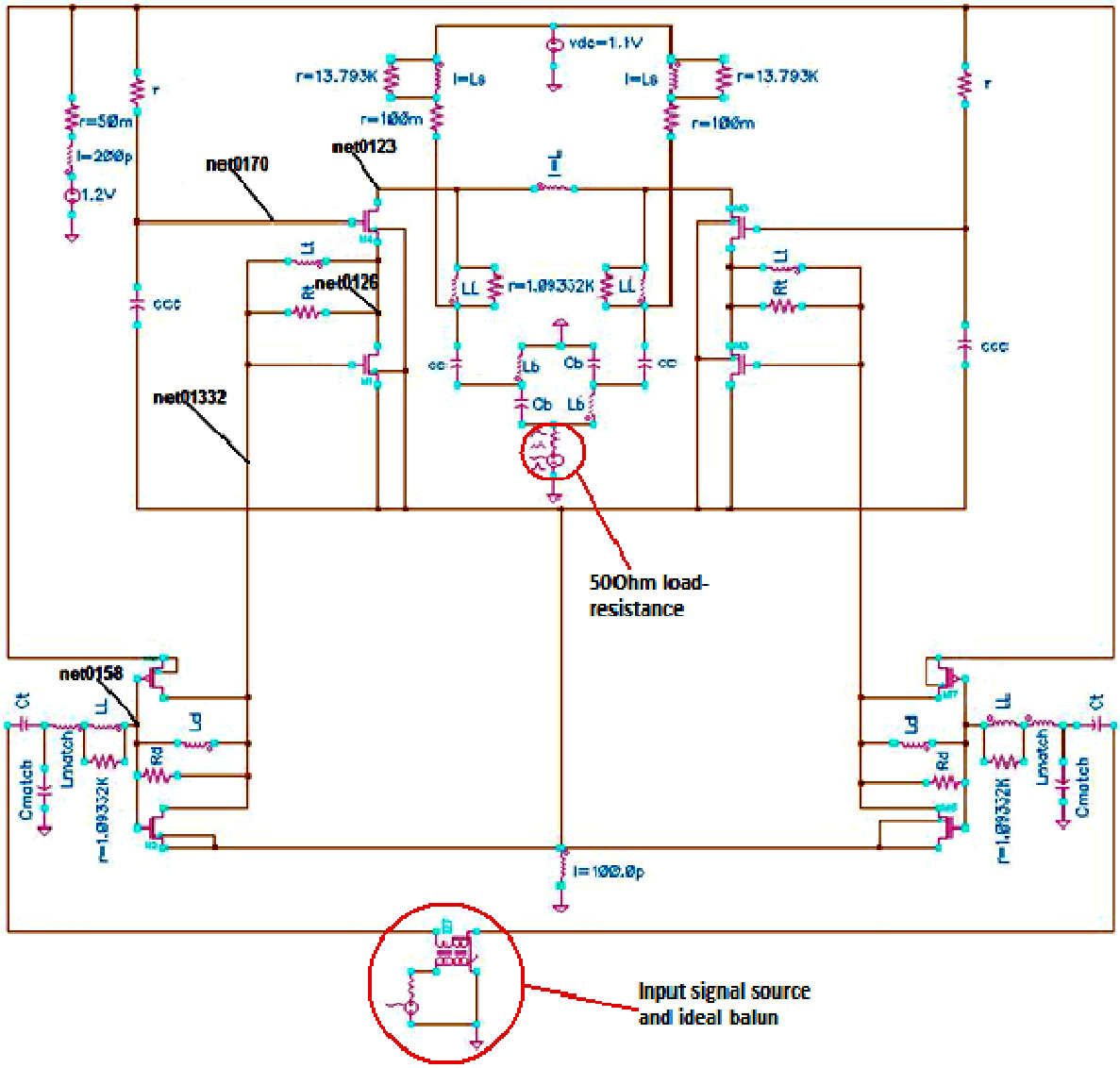


Figure 28: Resulting schematic of the inverse class-D amplifier.

The amplifier needs two voltage sources, one 1.2V source and one 1.1V source. When driven by one single-ended source the source voltage must be 1.6

4. SIMULATION RESULTS

4.1 RESULTS CLASS-E AMPLIFIER

The below presented results are simulated on the class-E schematic in Figure 22. They provide some information of the obtainable performance, but it is not the whole truth since they are simulated without the required driver network, the required matching and the

probably required stabilization. It is also not separated between the RF-loss and the dc-loss in the inductances.

Case	V_{dc}	L_1(RF-Choke)	C_1	C_2	R_L	L_2	Output Power	Power Gain	PAE
1:	1.1V	1.3nH	4.95pF	3.85pF	170mΩ	202pH	1.108W	19.52dB	51.42%
2:	1.4V	1.3nH	4.95pF	3.85pF	300mΩ	200pH	1.8W	19.73dB	47.18%
3:	1.0V	1.3nH	4.95pF	3.85pF	160mΩ	204pH	0.78W	16.88dB	54.5%

Table 4: Best results with RF-Choke loss resistance of 190mΩ, and R_L optimized for highest possible efficiency.

Case	V_{dc}	L_1(RF-Choke)	C_1	C_2	R_L	L_2	Output Power	Power Gain	PAE
1:	1.2V	1.3nH	4.95pF	3.85pF	120mΩ	202pH	0.785W	18dB	33.24%

Table 5: Results for case 1 in Table 4 but with 50mΩ loss included in RF-choke and in L2.

Case	V_{dc}	L_1(RF-Choke)	C_1	C_2	R_L	L_2	Output Power	Power Gain	PAE
1:	1.1V	0.5nH	4.95pF	3.85pF	170mΩ	202pH	1.109W	19.72dB	51.51%
2:	1.1V	0.2nH	4.95pF	3.85pF	180mΩ	202pH	1.11W	19.68dB	51.16%

Table 6: Results for decreased RF-choke inductance. All with loss resistance of 190mΩ in choke and no loss in wire-bonds. R_L optimized for highest possible efficiency.

Case	V_{dc}	L_1(RF-Choke)	C_1	C_2	R_L	L_2	Output Power	Power Gain	PAE
1:	1.1V	0.6nH	4.95pF	3.85pF	300mΩ	202pH	1.18W	17.55dB	48.57%
2:	1.2V	0.8nH	4.95pF	3.85pF	300mΩ	202pH	1.275W	17.92dB	46.65%
3:	1.1V	0.2nH	25pF	3.85pF	250mΩ	202pH	1.43W	18.55dB	48.85%

Table 7: Results for decreased RF-choke inductance. Case 1: Loss resistance of 110mΩ in choke, and loss resistance of 50mΩ in L2. Case 2: Loss resistance of 137.5mΩ in choke, and loss resistance of 50mΩ in L2. Case 3: Loss resistance of 50mΩ in RF-choke and in L2. R_L optimized for highest possible efficiency in all cases.

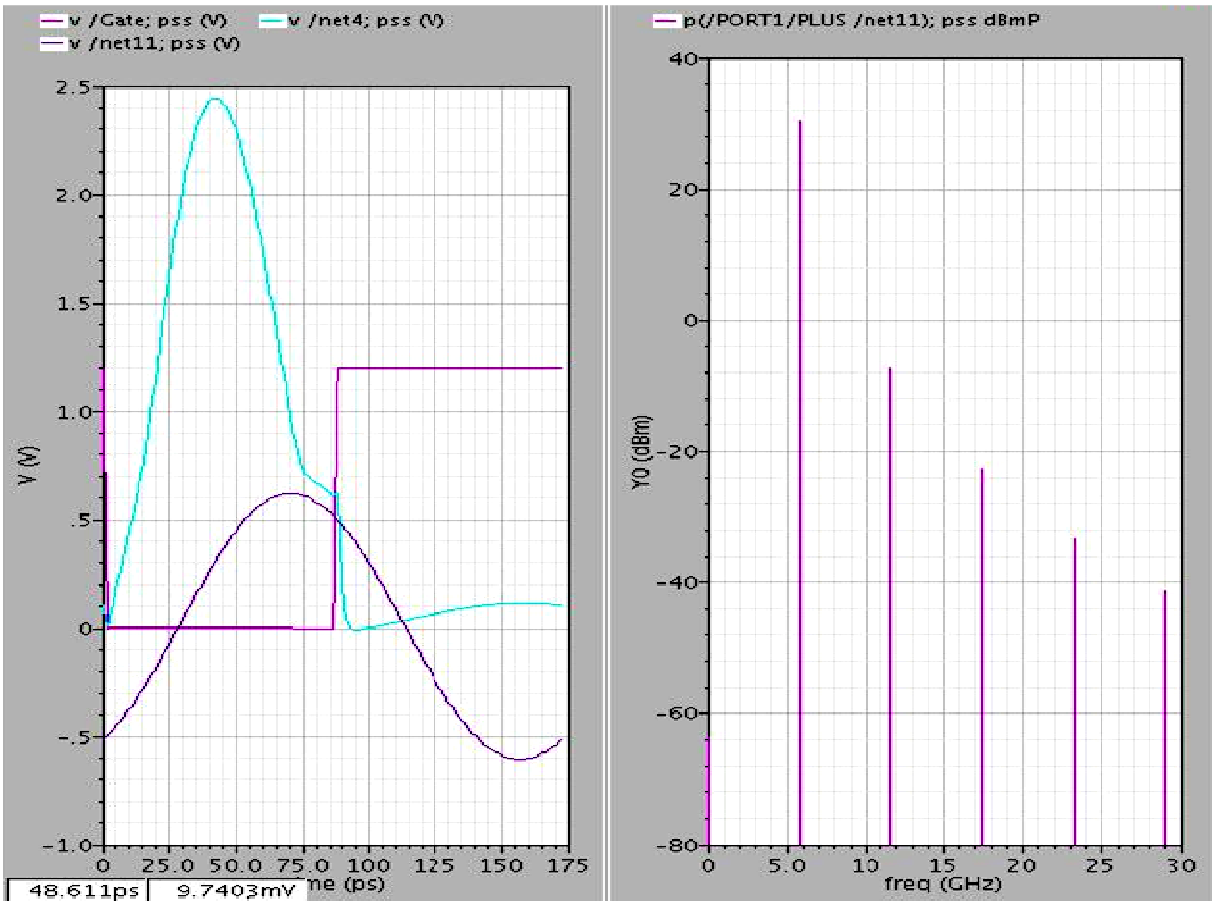


Figure 29: 1) Voltage waveforms at gate, net4 and net11 of Figure 22, Table 4 case 1. 2) Output power for the first five harmonics.

4.2 RESULTS INVERSE CLASS-D AMPLIFIER

The inverse class-D amplifier reaches the efficiency and the output power goals. Since the amplifier is designed to have a differential input, and not the single-ended input that was needed for the stability and efficiency analysis, the results are divided into two main categories; one with the ideal balun, and one without. This enables us to see the input match for each of the differential inputs, and also the required input voltage swing for each separate input.

The resulting component values of the amplifier schematic showed in Figure 28 are listed in Table 8. The loss resistances internally in the inductors are also listed.

Ls3	1.3nH
Ct	12pH
Lbalun	1.94nH
Wp	100µm
Cbalun	388fF

Wn	20µm
Ls2	1.3nH
Ls	2.2nH
LL	200pH
L	80pH, 146mΩ
Lb	240pH, 50mΩ
Lt	215pH, 391.7mΩ
Ld	500pH, 1Ω
cc	3.76pH
ccc	7p
Cb	3.2pF
Cmatch	1.12pF
R	2Ω
Rd	162Ω
Rt	170Ω
Lmatch	45pH, 50mΩ

Table 8: The component values used in the finished schematic (Figure 28), and the internal loss resistances that cannot be seen in the schematic.

4.2.1 SIMULATIONS WITH IDEAL BALUN

With the ideal balun we are able to simulate the stability K-factor. This K-factor is shown in Figure 30. The K-factor is above one for all frequencies. The K-factor is also shown in Figure 31, were all frequencies from 0-50GHz is simulated.

The voltage waveforms for different nodes of the schematic in Figure 28 are shown in Figure 30. The waveforms are simulated with an input voltage of 1.8V which is the maximum allowable voltage to stay within the voltage limits. A higher input voltage will lead to a too high voltage between net0158 and net0332. This can easily be seen in Appendix A, Figure 48 where the voltage waveforms are plotted for higher input voltages than 1.8V. The net0123 voltage does not increace above 2.5V for higher input voltages.

It is important that the difference between net0332 and ground, net0126 and ground, net0123 and net126, and net0158 and net0170 does not exceed the voltage limit of 1.32V. This applies if we use the same voltage limits between for gate-source, gate-drain, and drain-source. One can from Figure 30 see that the voltage retrictions are obtained.

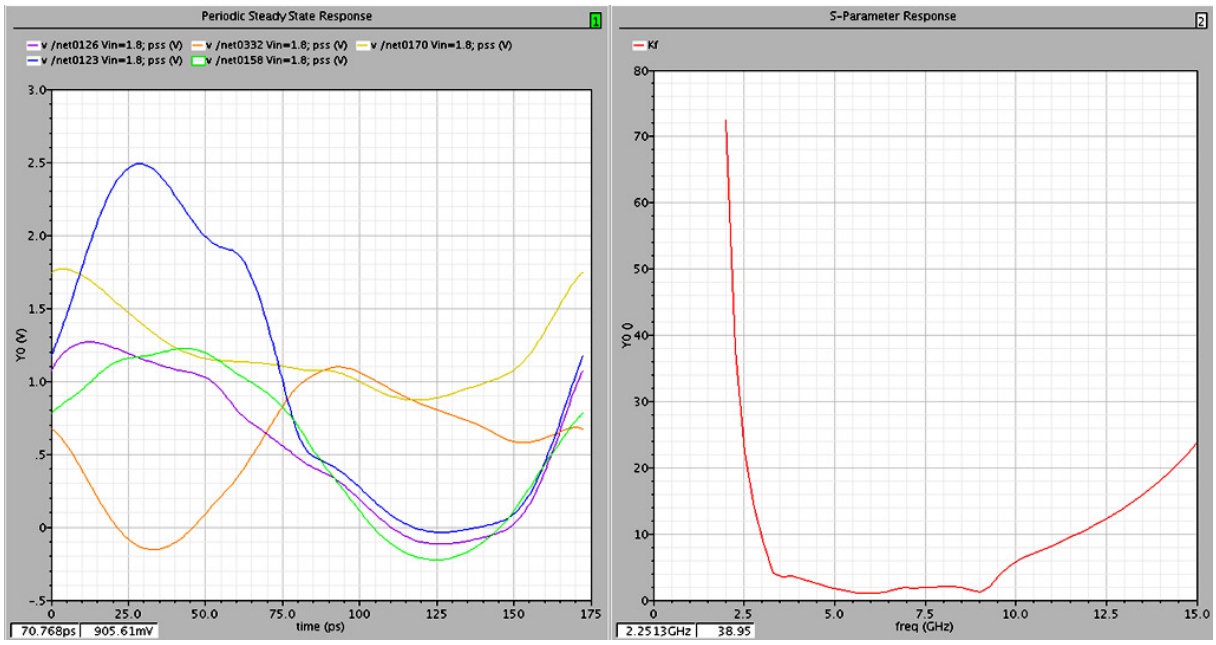


Figure 30: 1) Resulting voltage waveforms. 2) stability K-factor.

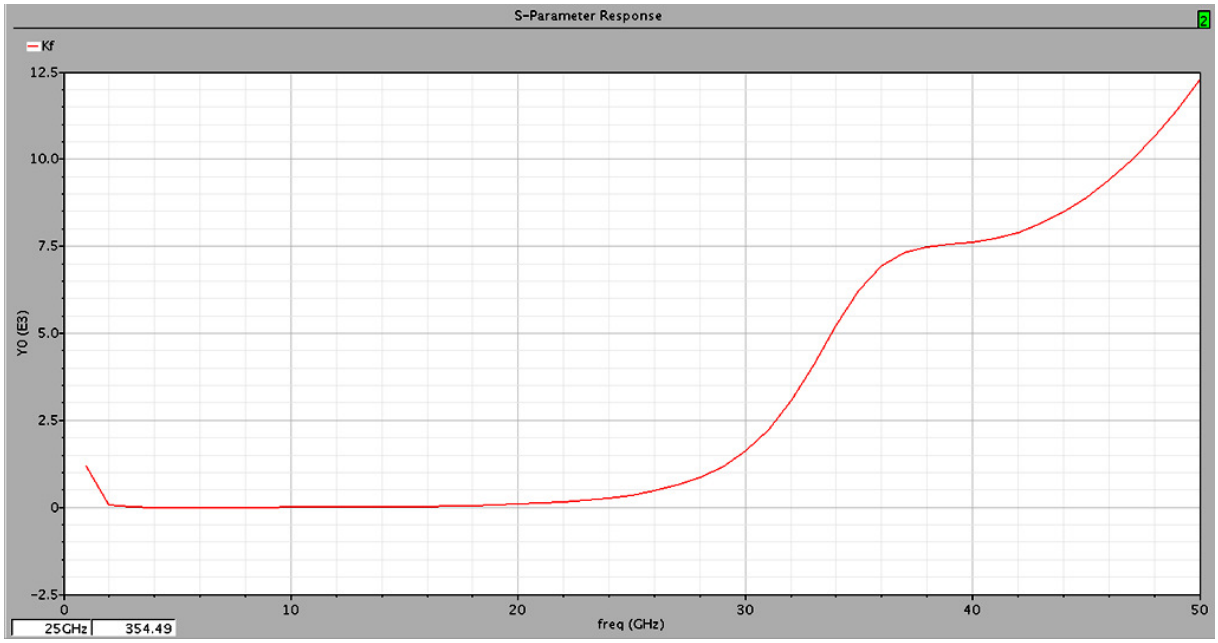


Figure 31: K-factor.

The output power and the efficiency are shown in Figure 32. The output power reaches 30dBm for a single-ended voltage of about 1.65V, and the PAE reaches 50% for the same input voltage. The PAE reaches a maximum of 51% for an input voltage of 1.8V, which is the maximum allowable input voltage.

The output Power and the PAE have an uneven response. The reason for this is unknown. Former simulations done in this thesis (that were less optimal in regard to efficiency), did not have this uneven response. This uneven response does not destroy the performance when the amplifier is used as intended; as a constant envelope amplifier.

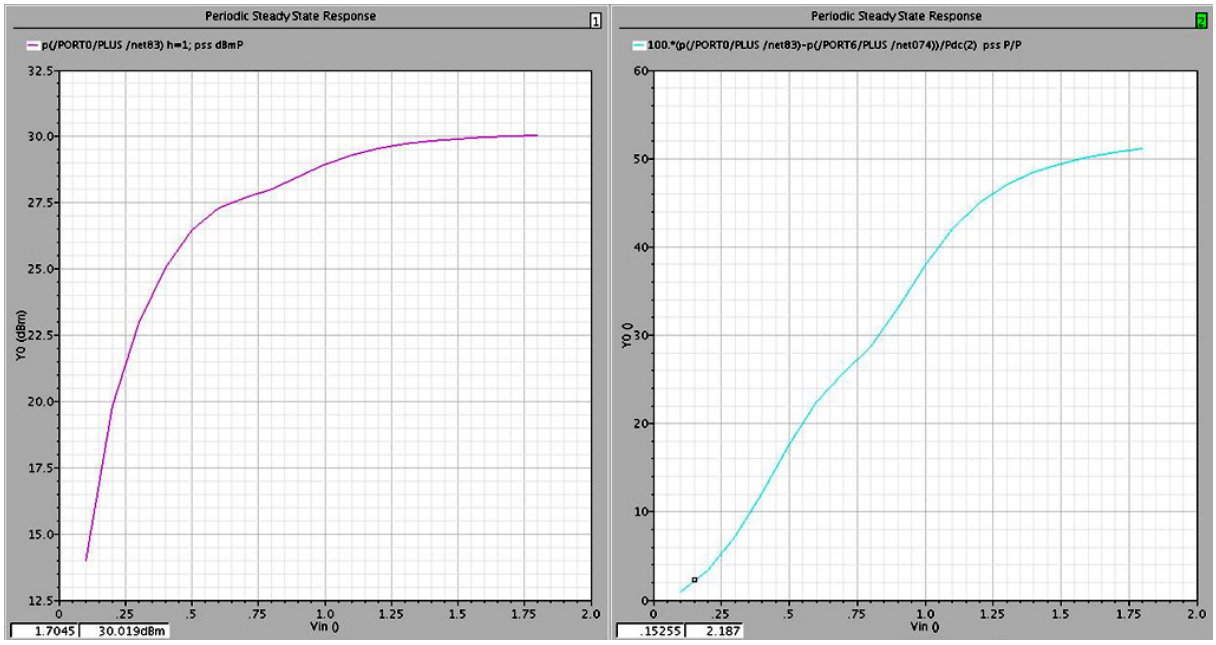


Figure 32: 1) Output power. 2) PAE.

The output power and the input power are shown to the left in Figure 33. The amplifiers gain is displayed to the right in the same figure. Cadence is unable to make a Pout versus Pin graph.

One can from this figure see that the gain goal of 25dB is not reached for the maximum output power. The gain becomes smaller than 25dB for output power levels larger than 28dBm.

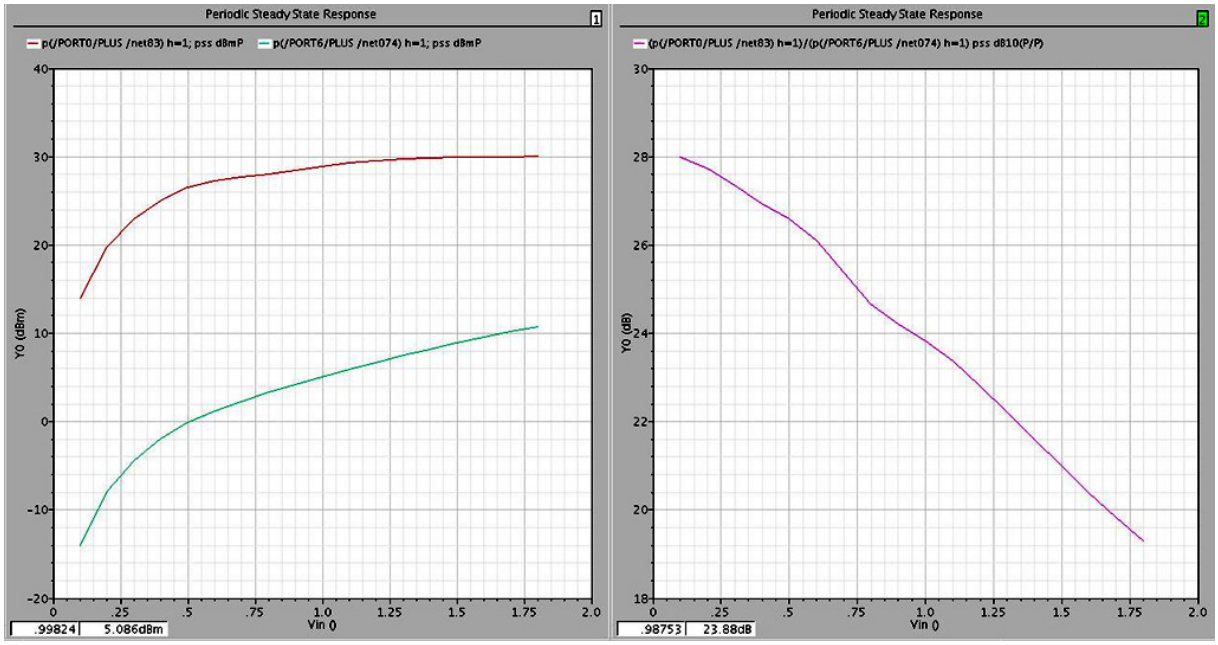


Figure 33: 1) P_{out} and P_{in}. 2) Power gain.

S_{11} is showed in Figure 34. If one compares S_{11} here with S_{11} for the differential inputs, one can see that the ideal balun decreases the matching. S_{11} equals -9.063dB at 5.8GHz, this is still a pretty good match, and not far from the often used requirement of -10dB.

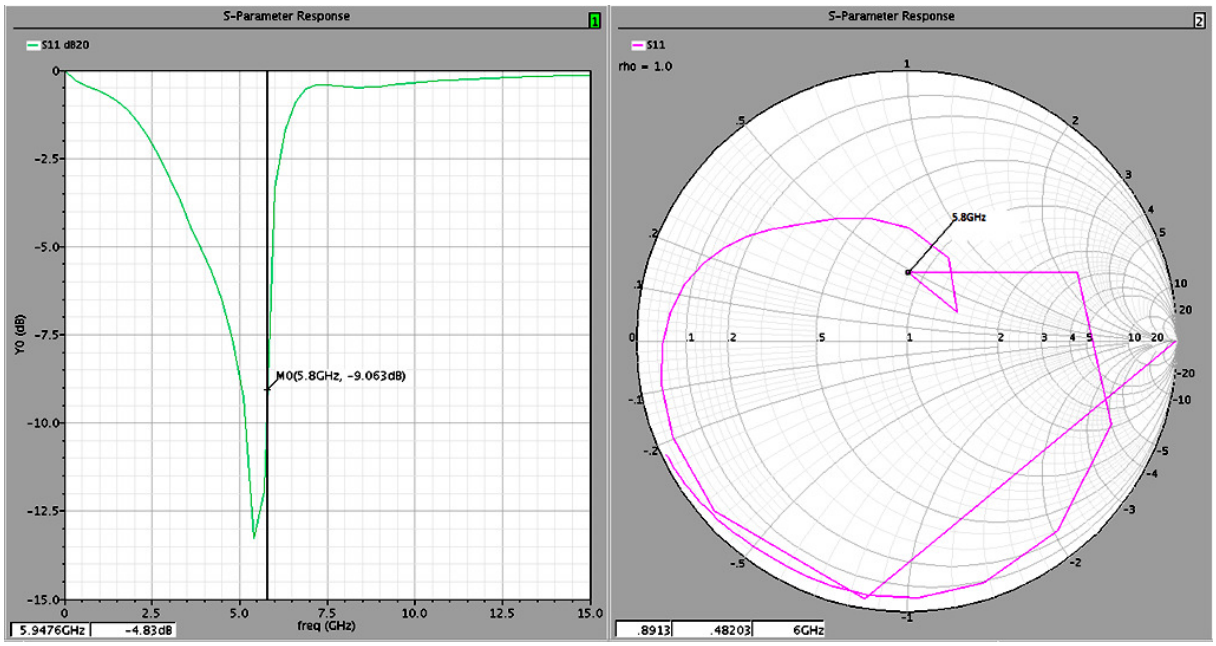


Figure 34: S_{11} for the resulting amplifier with input balun.

Figure 35 shows S_{12}, S_{22} and S_{21} for this amplifier, simulated with the input balun. S_{12} equals -34.17dB at 5.8GHz which is a very small reverse gain. S_{22} equals -6.087dB at 5.8GHz which means that the output match could be better. The output match can be hard to make for a power amplifier. It was decided (in consultation with supervisor Oddgeir Fikstvedt) that the focus should be on the input match. There was no time to take a closer look at the output match.

The forward gain S_{21} equals 26.18dB at 5.8GHz.

A magnified version of the S_{12}, S_{21} and S_{22} graphs with regard to frequency can be found in Appendix A, Figure 49.

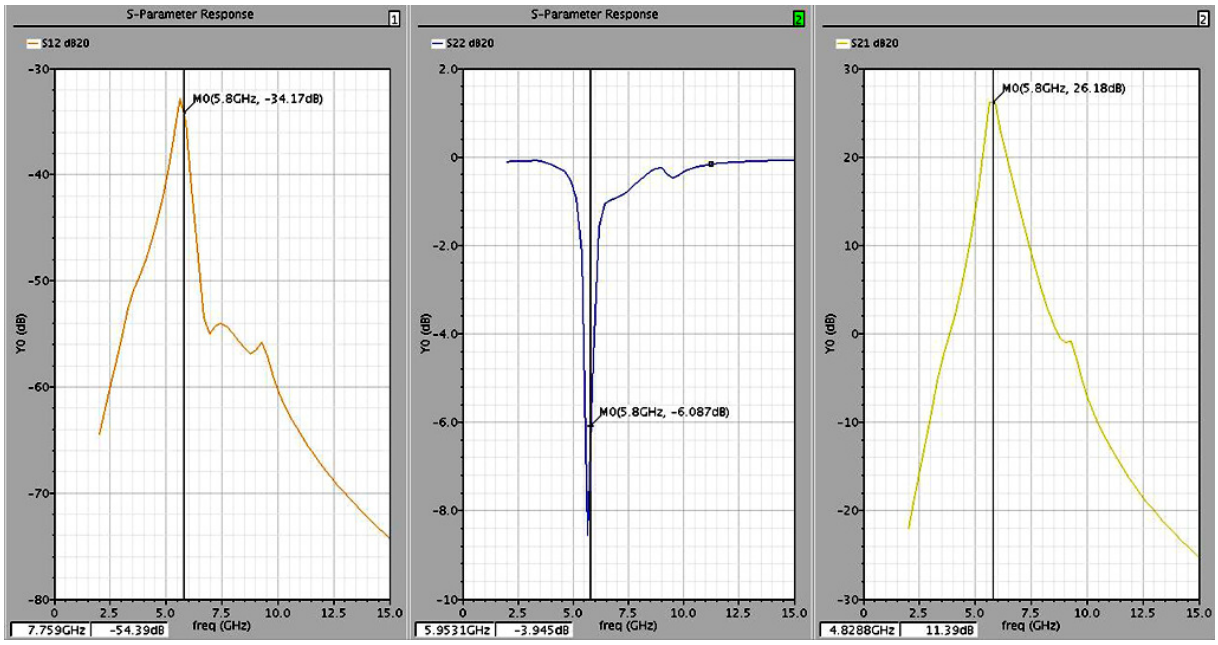


Figure 35: S_{12}, S_{22}, S_{21} for the resulting amplifier with the input balun.

Figure 36 shows the V_{ds}-voltage across the cascode and the current trough the cascode. One can see that the ideally square-shape of the current, and the ideally half-sinusoid shaped voltage is not obtained. The important part is that the overlap between the voltage and current is minimal.

To the right in the same figure, one can see the current drawn from the main voltage supply. The current drawn is about 1.8A. About 20mA is also drawn from the other voltage supply. This adds up pretty well with the previously calculated dc-current when the efficiency of about 50% in included in the calculations.

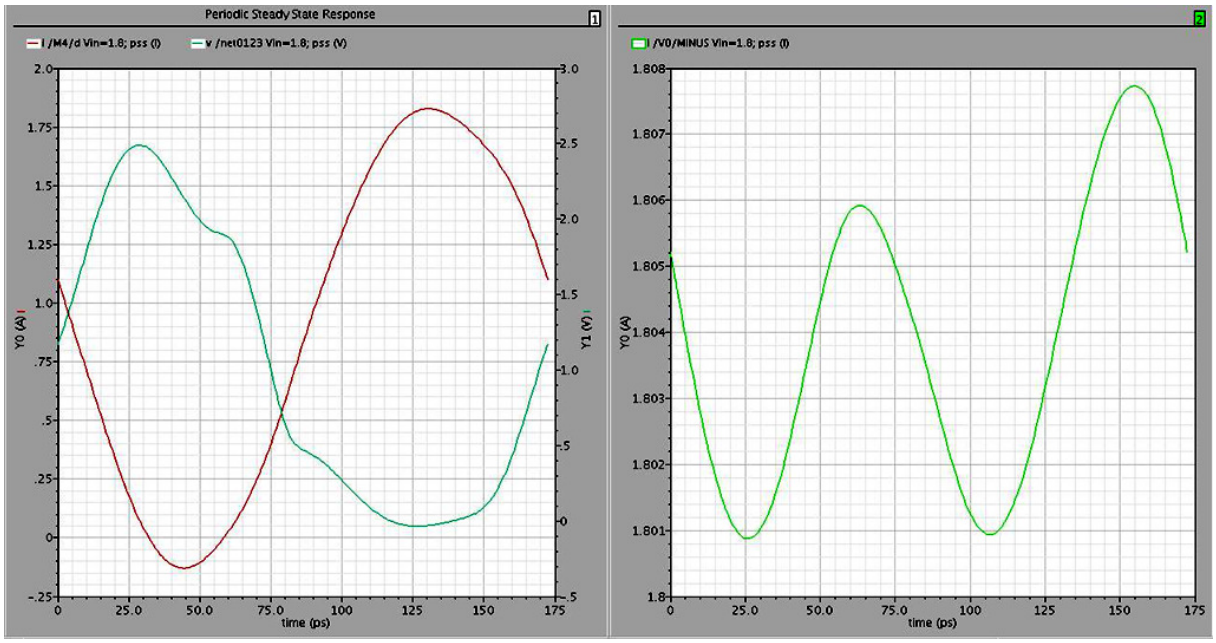


Figure 36: 1) The V_{ds}-voltage across the cascode and the current trough the cascode. 2) The total current from the main voltage source.

4.2.2 SIMULATIONS WITHOUT BALUN

Figure 37 shows the output power when the x-axis describes only one of the differential inputs. From this, one can see that the differential signals need to have an amplitude of 0.8V each to reach an output power of 30dBm.

PAE will not be presented for simulations without the input balun. Cadence is only capable of doing efficiency simulations with one input signal, and this will give a too high PAE.

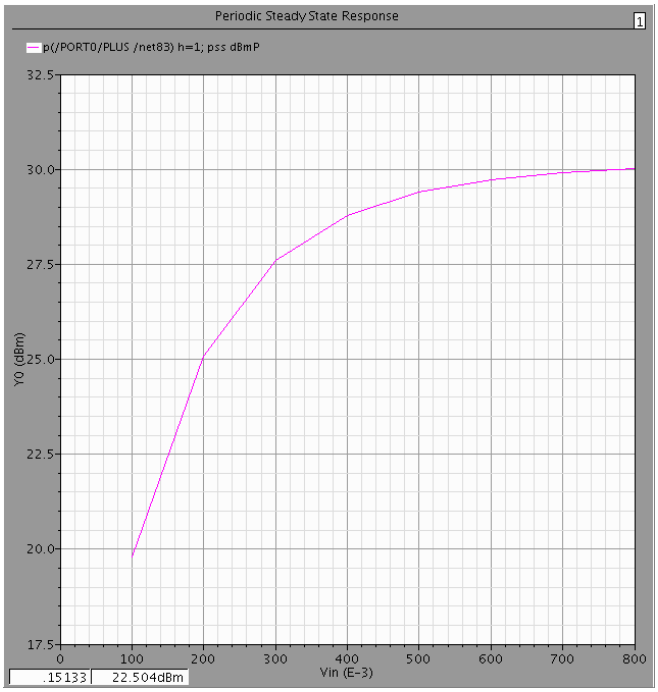


Figure 37: Output power. The voltage axis shows the voltage amplitude of one differential input.

Figure 38 shows S_{11} for one of the differential inputs. The input matching is very good with S_{11}=-36.5dB at 5.8GHz.

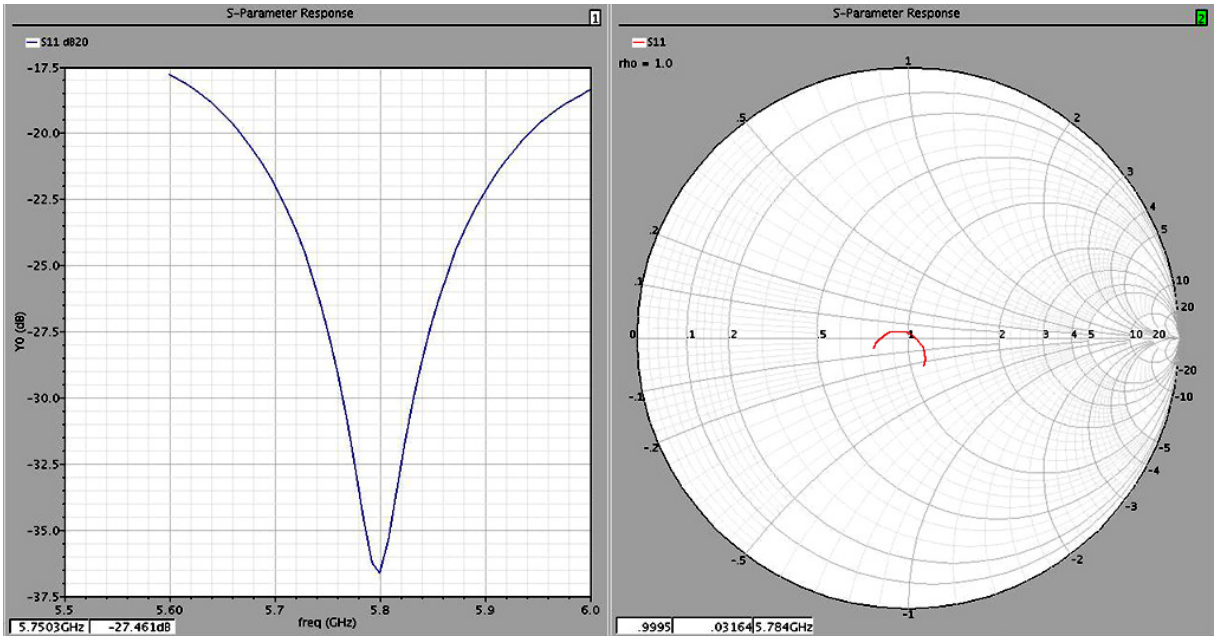


Figure 38: S_{11} for one of the differential inputs.

Figure 39 shows the rest of the S-parameters. S_{12} equals -36.5dB at 5.8GHz, S_{21} equals 24.1dB and S_{22} equals -8.5dB. The values of S_{12} and S_{21} do not say a lot about the performance when they only include one of the differential inputs.

A magnified version of this figure in regard to frequency can be found in Appendix A, Figure 50.

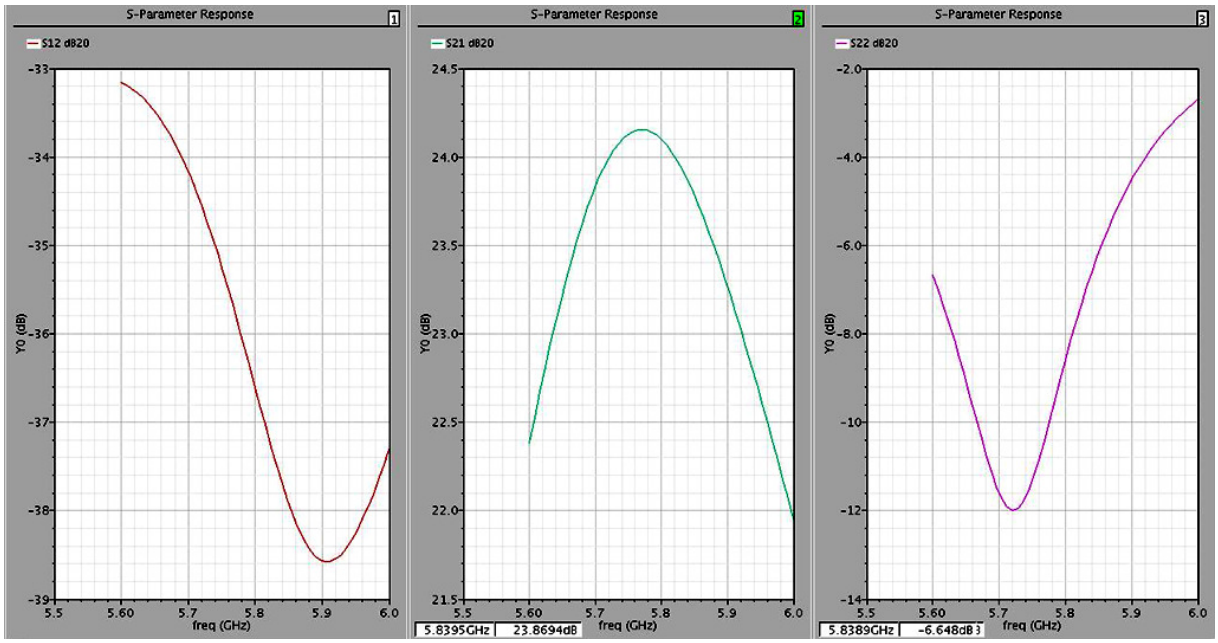


Figure 39: S_{12}, S_{21} and S_{22} for one of the differential inputs.

5. DISCUSSION OF RESULTS

The results from the class-E simulations are not to be taken as the whole truth since only a minimum of the realistic losses is included. The self-biasing technique was never implemented for this amplifier, which means that the voltage stress on the common-gate transistor was too high. If implemented, the self-biasing technique would steal some of the efficiency. This amplifier is also simulated with a completely ideal square-shaped input signal, and without the required input and output match. This will also lead to a higher efficiency than in a realistic amplifier design. Stability was not considered for this amplifier.

It is obvious that the right choice was made when it was decided to use the inverse class-D amplifier over the class-E amplifier. As one can see from the simulation results in chapter 4, the efficiency of the inverse class-D amplifier (where all the losses is included) is in the same order of magnitude as for the almost ideal class-E amplifier.

The class-D amplifier is made as realistic as possible (with all parasitic losses included), so the simulations results can be evaluated as realistically achievable.

One note should be made in regard to the stability analysis of the inverse class-D amplifier. This is the fact that parasitic oscillations can exist even though the K-factor analysis reports that the amplifier is unconditionally stable. This is because the stability analysis is done with only one input frequency. The switched amplifier operates in the transistors non-linear region. Because of this non-linearity, the risk is that a high powered input signal can transform the parasitic of the transistor so that the condition for oscillations can exist for a low powered source (noise) at another frequency.

It should also be noted that the quality of the transistor model as a switch is unknown. This quality has a big influence on the simulation results.

6. CONCLUSION

The simulations clearly show the benefit of the inverse class-D amplifier compared to the class-E amplifier for this specific application.

The output power and the efficiency goals were reached. Unfortunately the gain goal was not reached for the maximum output power and efficiency. The gain decreases below the goal of 25dB when the output power increases above 28dBm.

The power gain is 20.06dB in the point where the output power goal (30dBm) and the efficiency goal (50%) are reached.

The maximum output power is 30.04dBm with an efficiency of 51%. At this point the power gain is 19.2dB.

6.1 FURTHER WORK

To reach the designs gain goal, some further work needs to be done to decrease the needed input power.

A layout design and a prototype should be made to evaluate the accuracy of the simulations.

7. REFERENCES

1. Leenaerts, T.S.a.D.M.W., *A 2.4-GHz 0.18-um CMOS Self-Biased Cascode Power Amplifier.* IEEE jurnal of solide-state circuits, 2003. **38**(8).
2. Wikipedia, *Cascode.* 2009.
3. Huang, C.Y.a.Q., *A Common-Gate Switched 0.9-W Class-E Power Amplifier with 41% PAE in 0.25-um CMOS.* IEEE jurnal of solide-state circuits, 2001. **36**(5).
4. Brama, R., et al., *A 30.5 dBm 48% PAE CMOS class-E PA with integrated balun for RF applications.* Ieee Journal of Solid-State Circuits, 2008. **43**(8): p. 1755-1762.
5. Palaskas, Y., et al., *A 5-GHz 20-dBm power amplifier with digitally assisted AM-PM correction in a 90-nm CMOS process.* Ieee Journal of Solid-State Circuits, 2006. **41**(8): p. 1757-1763.
6. Jongchan Kang, J.Y., Kyoungjoon Min, Daekyu Yo, Joongjin Nam, Youngoo Yang, Member, IEEE, and Bumman Kim, Senior Member, IEEE, *A Highly Linear and Efficient Differential CMOS Power Amplifier With Harmonic Control.* IEEE Journal of Solid-State Circuits, 2006. **41**(6).
7. Wongkomet, N., L. Tee, and P.R. Gray, *A+31.5 dBm CMOS RF Doherty power amplifier for wireless communications.* Ieee Journal of Solid-State Circuits, 2006. **41**(12): p. 2852-2859.
8. *Microwave Encyclopedia, microwaves101.com.* 2006.
9. Gustavsson, U., *Design of an inverse class D amplifier using GaN-HEMT technology.* Ørebro University Department of Technology, Ørebro sweden, 2006.
10. Sokal, N.O. and A.D. Sokal, *Class-E - New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers.* Ieee Journal of Solid-State Circuits, 1975. **Sc10**(3): p. 168-176.
11. Nathan O. Sokal, W.H.o.D.A., Inc, ARRL Technical Advisor, *Class-E RF Power Amplifiers.* 2001.
12. Ulf Gustavsson, T.L., Christian Fager, Herbert Zirath, *Design of highly efficient, high output power, L-band vlass D^{-1} RF power amplifiers using GaN MESFET devices.* 10th European Conference on Wireless Technology, 2007.
13. Murata Manufacturing Co., L., *Murata inductor catalog.* 2008.

APPENDIX A

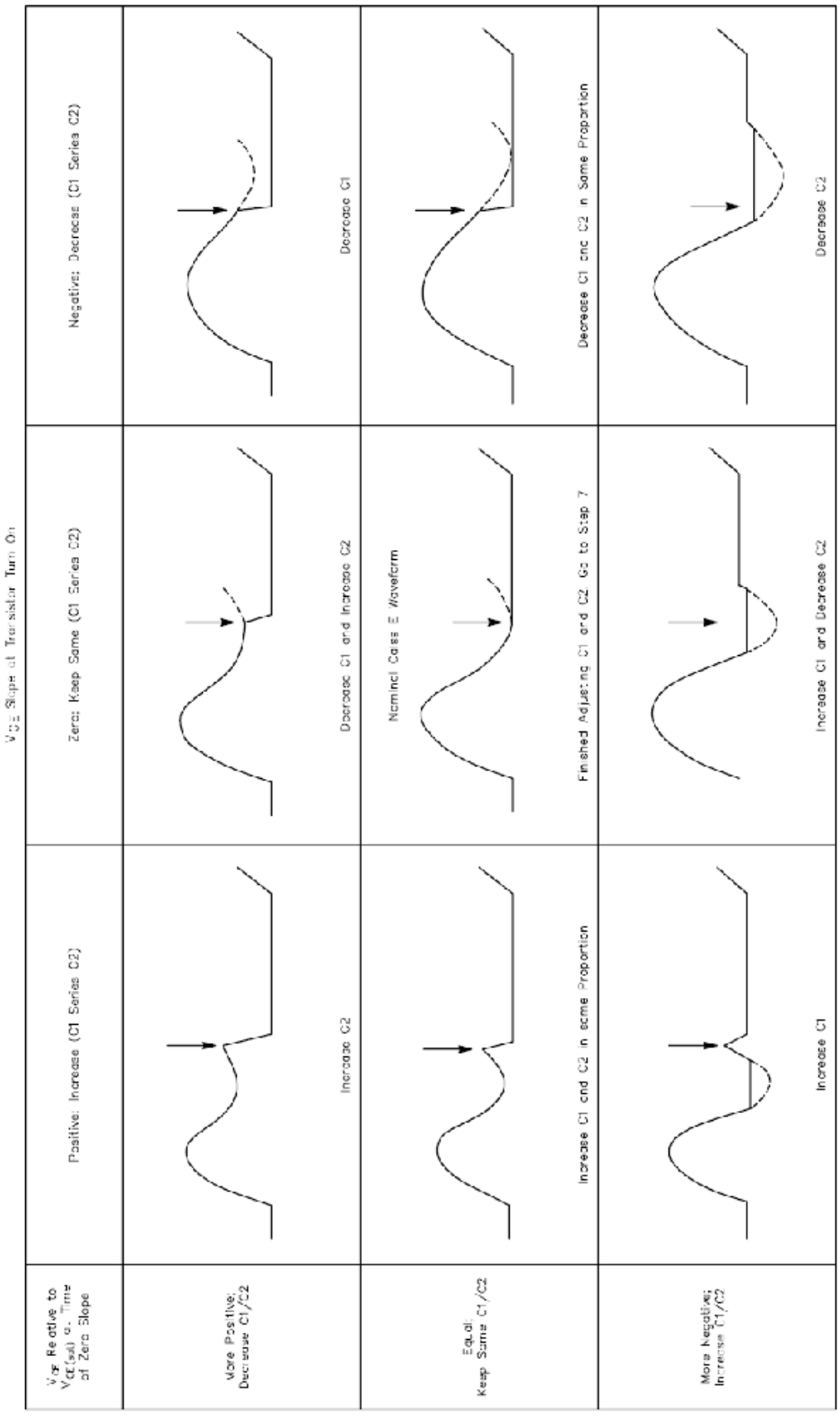


Figure 40: Class-E amplifier, design guidelines [11].

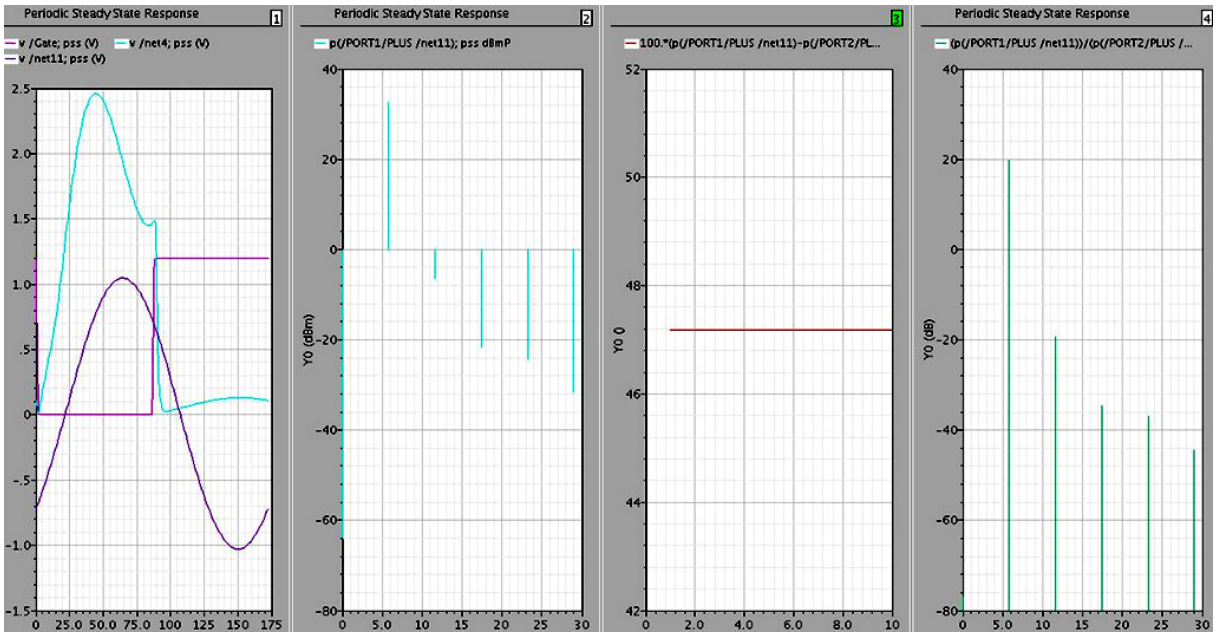


Figure 41: Simulation results case 2 of Table 4. 1) Waveforms on gate, net4 and net11 of Figure 22. 2) Output power. 3) Maximum efficiency. 4) Power Gain.

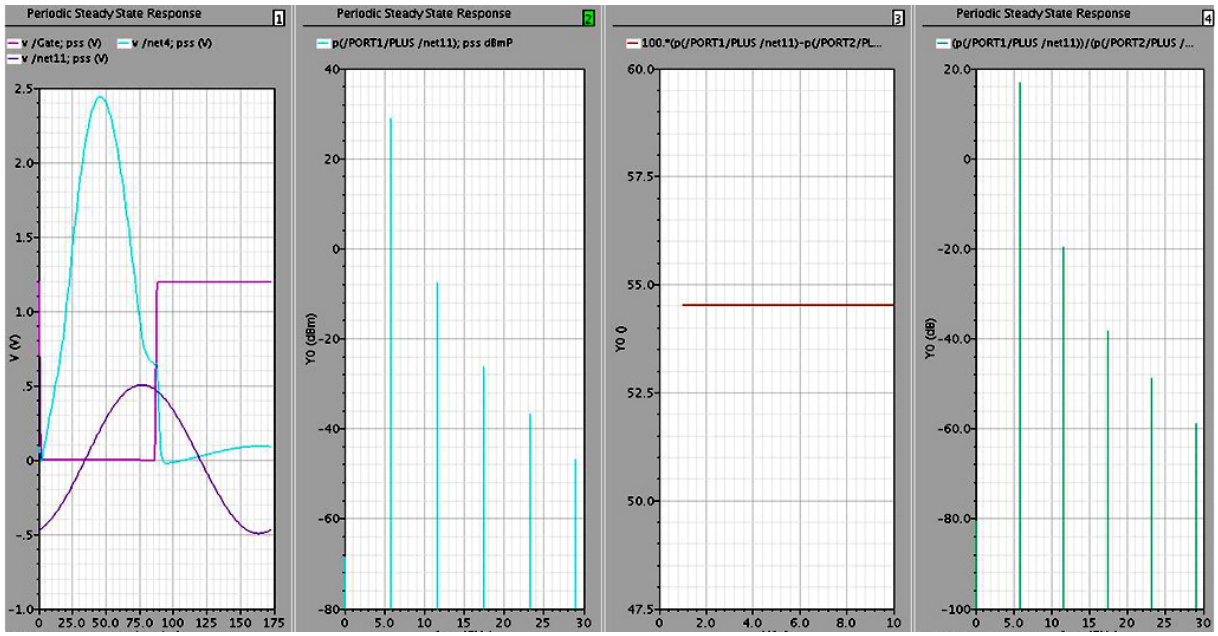


Figure 42: Simulation results case 3 of Table 4. 1) Waveforms on gate, net4 and net11 of Figure 22. 2) Output power. 3) Maximum efficiency. 4) Power Gain.

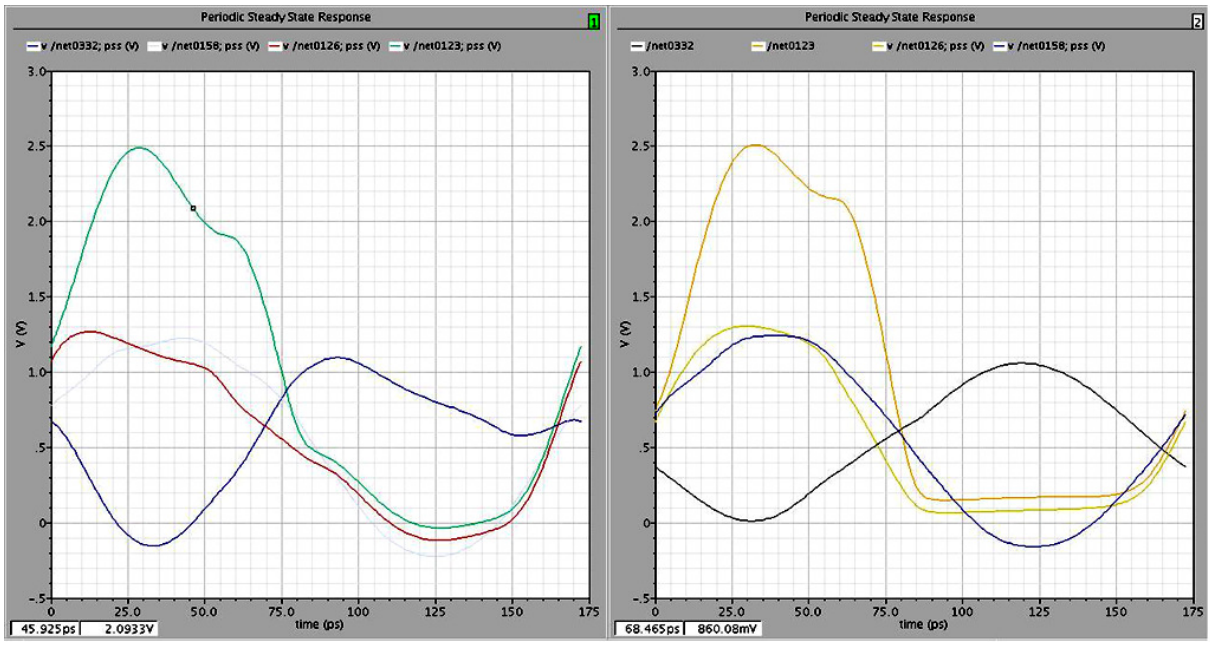


Figure 43: 1) Voltage waveforms with ground inductance. 2) Voltage waveforms without the ground inductance.

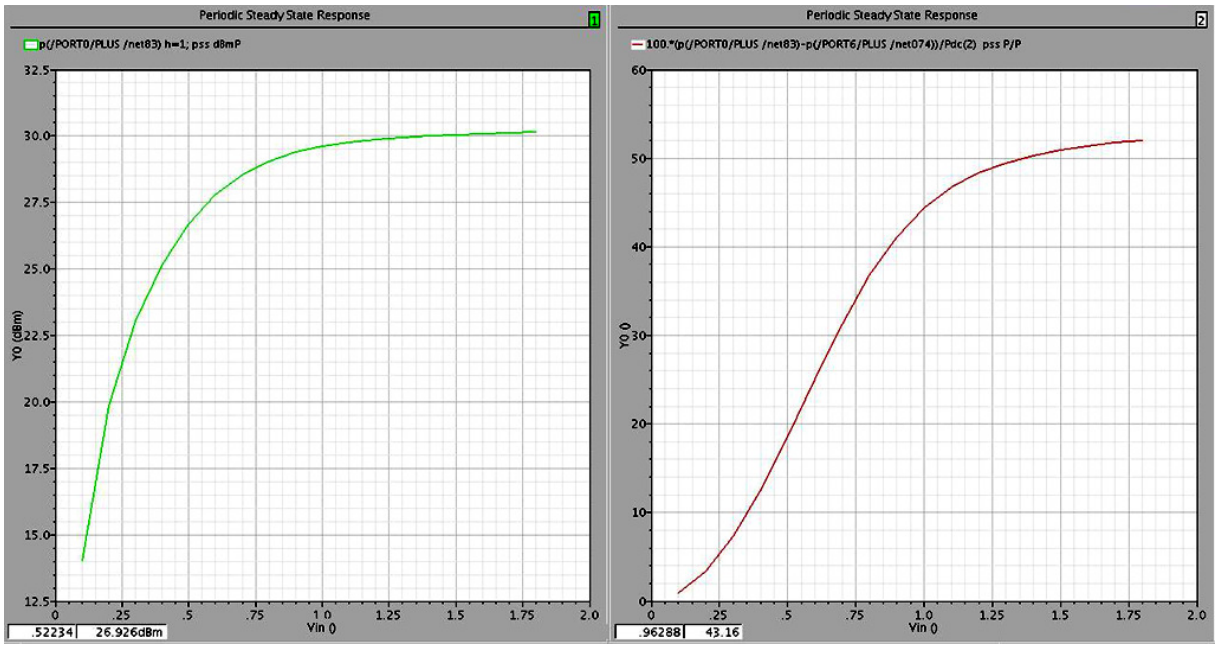


Figure 44: 1) Output power. 2) PAE. Both for the inverse class-D amplifier when the ground inductance is excluded.

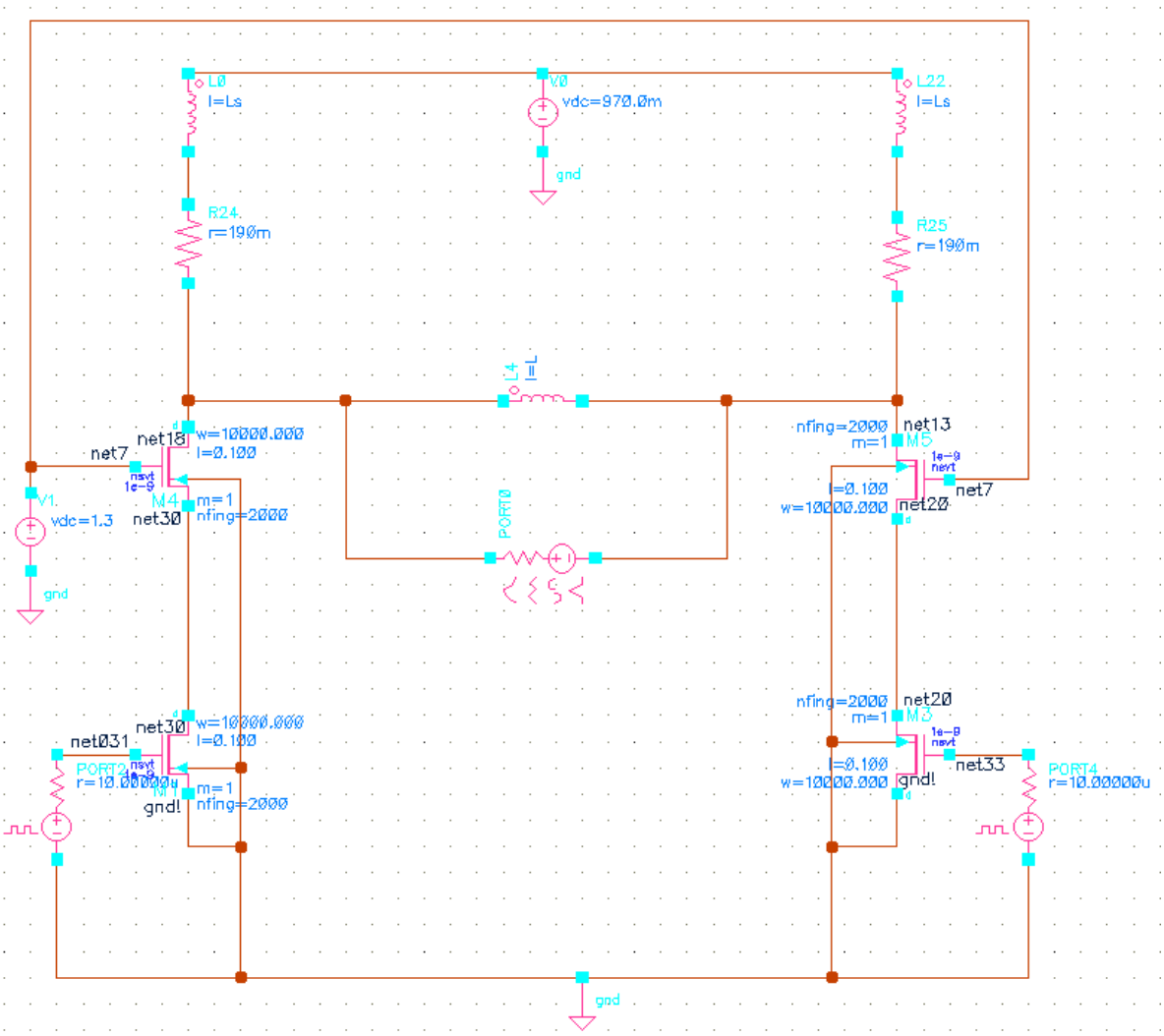


Figure 45: Almost ideal inverse class-D amplifier with a loss resistance of 190mΩ in the RF-choke inductances. L=80pH, Ls=2.2nH and the load resistance is 2.5Ω.

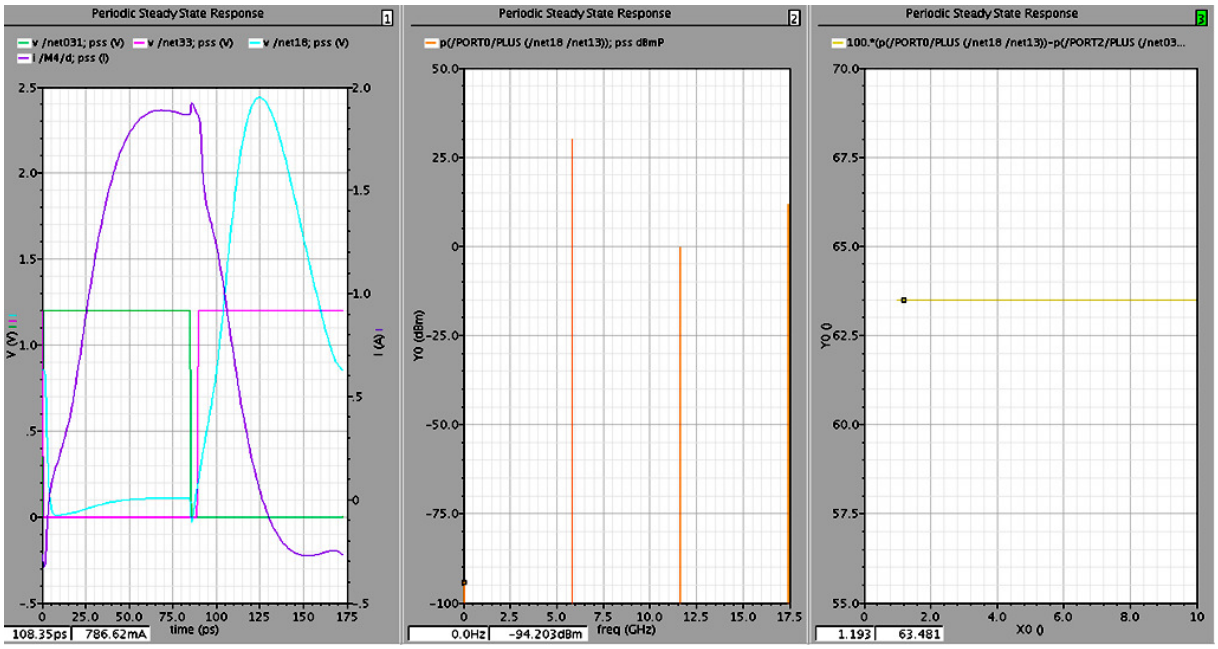


Figure 46: 1) The voltage and current waveforms. 2) Output power. 3) PAE. All for the circuit in Figure 45.

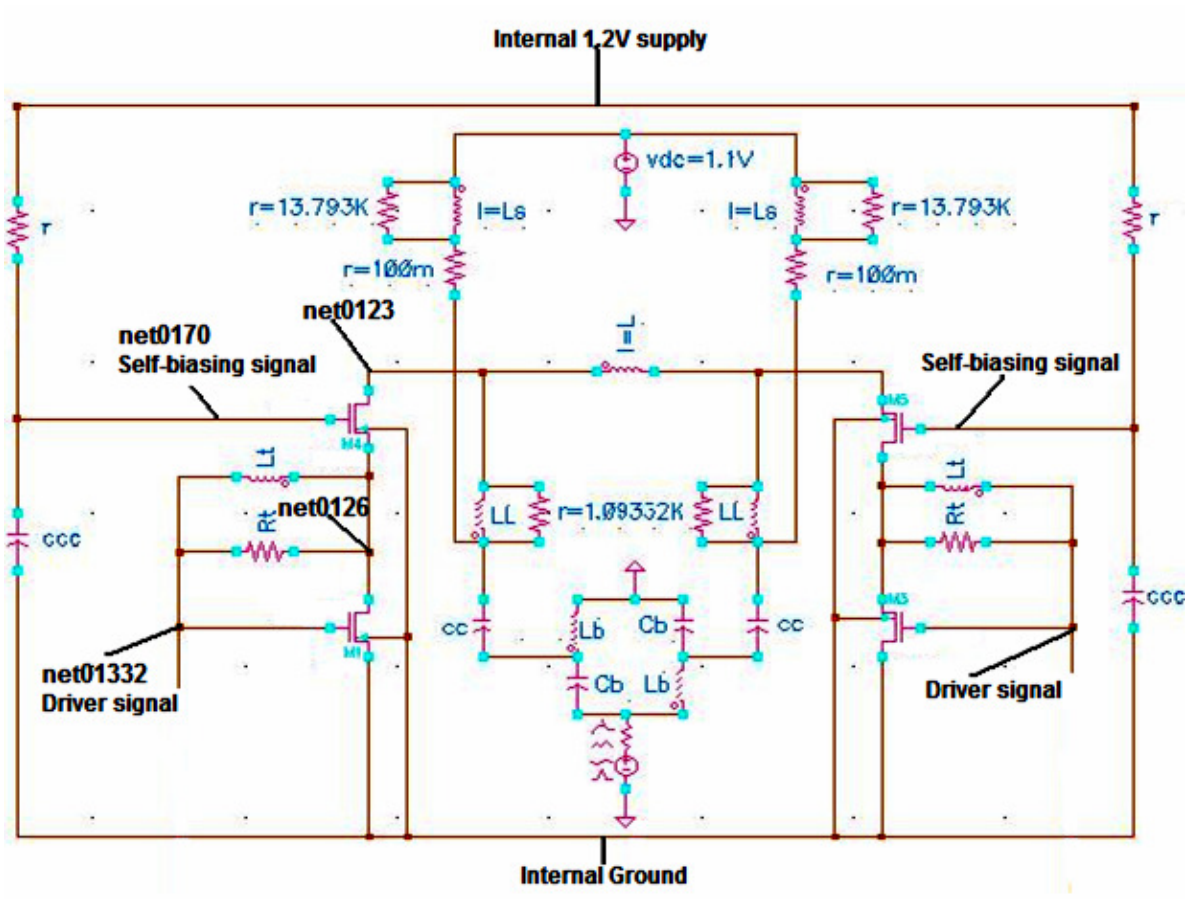


Figure 47: Magnified upper part of the circuit in Figure 28.

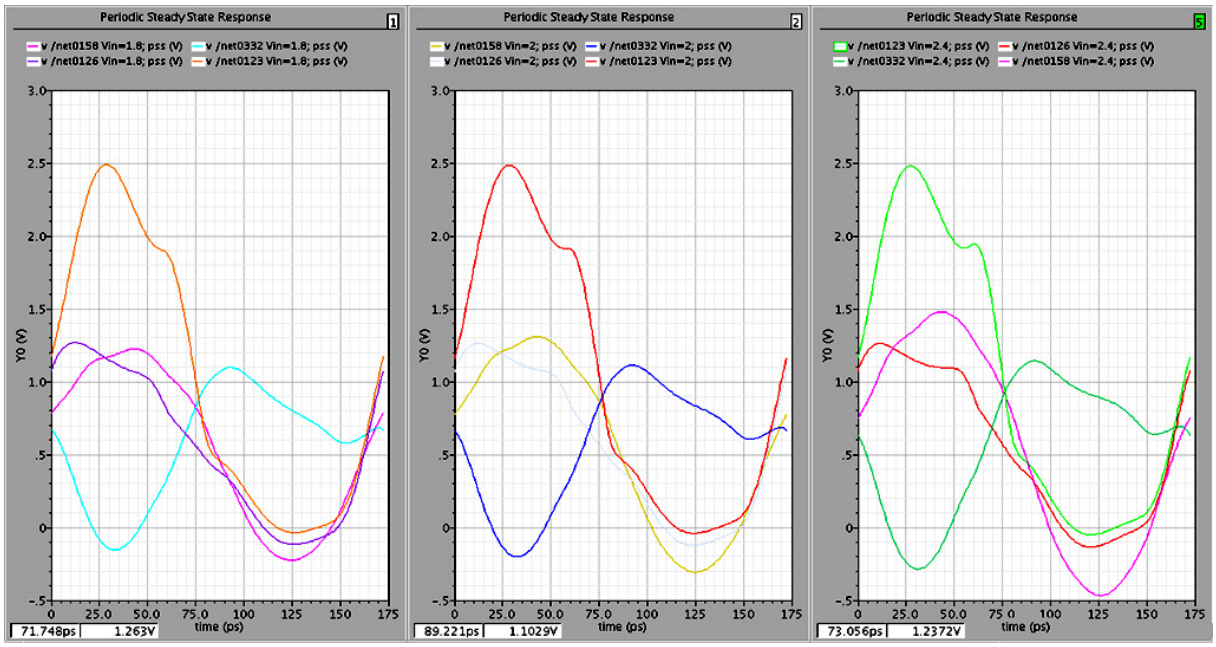


Figure 48: Voltage waveforms when increasing the input voltage above the limit of 1.8V.

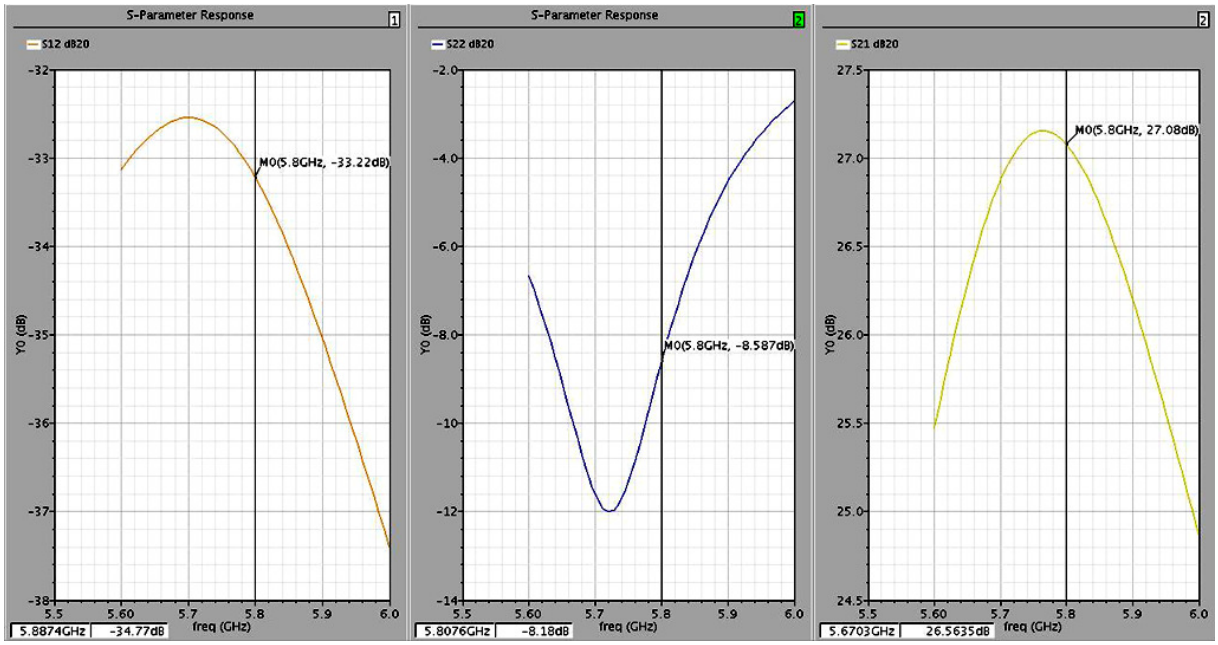


Figure 49: S_{12}, S_{22} and S_{21} for the resulting inverse class-D amplifier with the input balun.

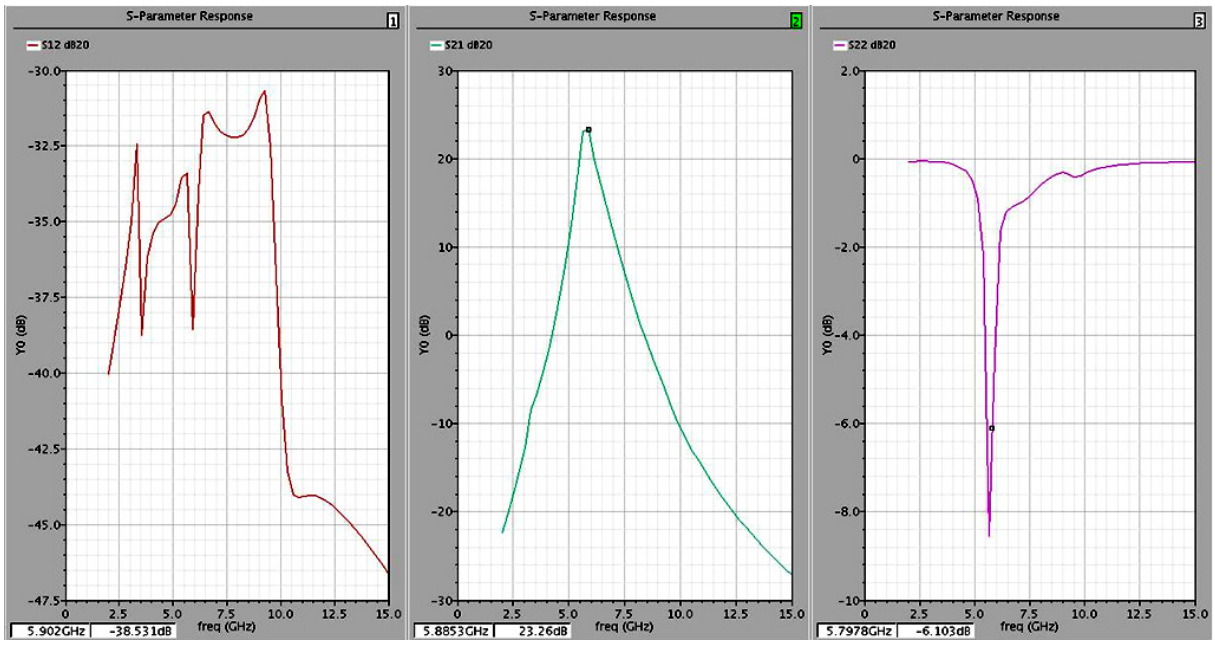


Figure 50: S_{12}, S_{22} and S_{21} for the resulting inverse class-D amplifier when only one of the differential inputs is included in the simulation.