NTNU

Norwegian University of
Science and Technology

Subthreshold Potential Modeling of FinFET and QuadFET

Dag-Martin Nilsen

Master of Science in Electronics
Submission date: June 2009
Supervisor: Tor A Fjeldly, IET

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Problem Description

Create a physical basis for precise potential modeling of nanoscale short-channel lightly doped FinFET and QuadFET operated in subthreshold regime, based on the work of Fjeldly et al.

Assignment given: 22. January 2009
Supervisor: Tor A Fjeldly, IET

Preface

This thesis will describe in detail my Master project, which is a part of the the "Master of Technology" education program at the Norwegian University of Technology and Science (NTNU) in Trondheim. The work was carried out at University Graduate Center at Kjeller (UNIK).

Special thanks to my supervisor Tor A. Fjeldly for all his guidance, encouragement and help. Also special thanks to Udit Monga for all the helpful guidance and advices, and to Åsmund Holen for many helpful discussions.

Summary

A precise subthreshold potential model for Quadruple FET (QuadFET) is presented in this thesis. The attempt of modeling FinFET ("Fin" FET) in the same way failed, but the procedure of the attempt will still be presented, and a conclusion of why this modeling did not work is given.

An analytical solution for the inter-electrode potential distribution of a double-gate MOSFET (DG MOSFET) is used for the QuadFET by performing a simple geometric scaling transformation. This is done with a high degree of precision due to structural similarities between the QuadFET and DG MOSFET, accounting for the difference in gate control of the two devices. A parabolic approximation is then used to model the cut-plane in the middle of the device, perpendicular to the electron flow from source to drain. The resulting analytical solution agrees very well with numerical simulations.

For the FinFET, the same analytical solution of the DG MOSFET is used directly in the ground plane of the device, assuming that the electric fields going through the ground plane, into the thick substrate, is negligible. Conformal mapping is then used in the same plane as modeled in the QuadFET, that is the plane in the middle of the device, perpendicular to the electron flow from source to drain, resulting in an analytical solution for the FinFET. Since the potential curvature in the source-drain direction was neglected when making the three dimensional problem of the FinFET to a two dimensional one, the modeling failed. However, an attempt of modeling the transistor has been tested, the electrostatics of the device is better known, and a new way of modeling the device is briefly discussed.

Contents

Notation and symbols

ε_{ox}	Relative dielectric permittivity of oxide
ε_{si}	Relative dielectric permittivity of silicon
t_{ox}	Oxide (insulator) thickness
t'_{ox}	Effective Oxide (insulator) thickness for silicon permittivity (t'_{ox}=$t_{ox}\varepsilon_{si}/\varepsilon_{ox}$)
λ_{Quad}	Characteristic length of QuadFET
λ_{DG}	Characteristic length of DG MOSFET
L	Gate length of FinFET and QuadFET
H	Height of FinFET
H_{eff}	Effective height of FinFET (H_{eff}=H+t'_{ox})
W	Width of FinFET
W_{eff}	Effective width of FinFET (W_{eff}=W+$2t'_{ox}$)
S	Length of sides in QuadFET
S'	Effective length of sides in QuadFET (S'=S+$2t'_{ox}$)
L'	Extended gate length of DG MOSFET (L'=$L\lambda_{DG}/\lambda_{Quad}$)
N_a	Acceptor doping
N_C	Effective density of states in conduction band
N_V	Effective density of states in valence band
n_i	Intrinsic electron density
m_n	Effective electron mass
m_p	Effective hole mass
h	Plancks constant
$\hbar$	Reduced Plancks constant
V_{bi}	Built in potential, band bending
V_{FB}	Flat band voltage
V_{th}	Thermal voltage
V_T	Threshold voltage
V_{gs}	Gate to source voltage
V_{ds}	Drain to source voltage
k_B	Boltzmann's constant
T	Temperature
q	Electron charge

χ	Electron affinity silicon
Φ_m	Gate metal work function
ϕ_b	Fermi-intrinsic band bending
φ_c	Potential difference between center in device and at gate-silicon interface
φ_m	Maximum potential in cut plane perpendicular to source-drain symmetry line in center of device
φ(x,y,z)	Potential distribution in body
φ(u,v)	2D Potential distribution in a device body in W-space
k	Modulus
K(k)	Complete elliptic integral of the first kind
F(k,w)	Legendre elliptic integral of the first kind

List of Figures

Chapter 1

Introduction

1.1 Background

MOSFETs (Metal Oxide Semiconductor Field-Effect Transistors) have existed since the beginning of the 1960's, and are still, by far, the most important type of transistor in the world. No other types of technology have yet been able to compete with the well known MOSFET technology. The worlds request for faster and smaller electronics has put an enormous pressure on the semiconductor industry to keep shrinking the transistor, especially since smaller also means faster and more logic on chip. However, the conventional single-gate MOSFETs is reaching its scaling limit due to problems such as leakage and loss of gate control. The search for alternative devices is for this reason extremely important in order to keep up the development in the semiconductor industry. Strong candidates to replace the conventional bulk MOSFET is the FinFET ("Fin" FET) and QuadFET (Quadruple FET). The replacement is needed in order to meet the ever growing demands for high-speed, low power CMOS (Complementary Metal Oxide Semiconductor) circuitry.

The scaling of the single-gate MOSFET into the sub-100nm range has been possible by for instance increasing the doping in the body and by using steep doping gradients. However, this will be detrimental for the charge carrier mobility, and thus lower the drain current and speed of the transistor. The FinFET and QuadFET have advantages compared to the bulk MOSFET in terms of short-channel effects and much improved gate control due to the use of volume inversion in the entire thin, lightly doped silicon body in all regimes of operation. The FinFET and QuadFET become for this reason superior to the ordinary MOSFET at short gate lengths.

The amount of current which is moving through the body of a transistor when operated in the subthreshold region is important to predict precisely, since it determines the off-state leakage current of the device, and therefore also the power dissipation in logic circuits. This is especially important in battery driven circuits with reduced power supplies.

1.1.1 Integrated circuits

An integrated circuit is a miniaturized electronic circuit that can consist of complete systems of both analog and digital functions (VLSI- very large scale integration) on a wafer. Integrated circuits are used in many battery driven circuits, such as cell phones, cameras, mp3-players, etc. CMOS technology has become the most used in these implementations because it provides density and power savings on the digital side, and a good mix of components for analog design[3].

1.1.2 Device simulation (TCAD)

A device simulator is a technology computer aided design (TCAD) tool, which apply numerical derivations based on complex equations, such as partial differential equations, to predict the behavior of a device.

Iterating Poisson's equation combined with a transport model for a given set of boundary conditions with a numerical device simulator, gives a prediction of the electrical characteristics of a device. The device is discretized in all three dimensions with a grid and then iterated with a PDE (Partial differential equation) solver, which means that the time of convergence and accuracy depends very much upon the grid distribution and size, solver type, models for carrier statistics and current continuity.

In this work the numerical device simulator Atlas from Silvaco is used to verify the models presented. Atlas has a range of models for different physical properties such as device electrostatics, charge carrier transport and noise.

1.1.3 Circuit simulation (SPICE)

Since the cost of manufacturing integrated circuits is high due to expensive photolithography and processing equipment, is it extremely important that the circuit is designed with high precision before produced. Simulating the circuit with a circuit simulator, such as SPICE (Simulation Program with Integrated Circuit Emphasis), is necessary in order to verify the circuit and make it ready for production.

A part of the development of FinFET and QuadFET is to create precise compact models for implementation in circuit simulators and circuit design tools, in order to use the transistors in an integrated circuit. Usually, a selection of models exists for a transistor, where an exact model has made the expense of being slow due to being more complex, and visa versa. Previous, less precise MOSFET models use many adjustable parameters which have to be extracted through analyzing measurement or a device simulator (TCAD). For the designer to choose an appropriate model for a specific circuit is often a difficult task.

1.1.4 Device modeling

In this thesis, a physically based device model is a description of the device behavior in terms of analytical, algebraic expressions. The model is further compact if it is described by analytical, explicit expressions. Compact models can also be based on preprocessing

routines, which imply iteration of models, resulting in parameter look-up tables for fast retrieval for use in simplified parameterized models. This is contrary to device simulations, which are numerical derivations of complex equations, such as partial differential equations.

1.2 Objectives of thesis

The objective of this thesis is to create a physical basis for precise potential modeling of nanoscale short-channel lightly doped FinFET and QuadFET in the subthreshold regime, based on the work of Fjeldly et al. The potential modeling can in future work be used to create a precise current and capacitance model in the subthreshold regime, and also be added to a threshold and strong-inversion model to give a compact model for the full regime of operation.

The modeling is based on a three-dimensional analysis for both the FinFET and the QuadFET, where the 2D analytical solution of the inter-electrode potential distribution of a DG MOSFET (Double-gate MOSFET)[2][1] is used in both analysis. Short-channel effects are intrinsic to this 2D and 3D analysis, and the DIBL-effect (Drain Induced Barrier Lowering) is added by the use of conformal mapping. The analytical solution from the DG MOSFET, can with the appropriate modifications be used as the inter-electrode potential distribution of the cut plane along the source-drain symmetry line in the middle of the QuadFET. In the case of the FinFET, the solution from the DG MOSFET is used as the potential distribution in the ground plane of the FinFET.

1.3 Important issues

In the attempt of modeling the subthreshold inter-electrode potential distribution of nanoscale short-channel FinFET and QuadFET, important terms are 3D electrostatics, DIBL, inversion charge, quantum mechanical effects, gate tunneling and noise. Below follows a summary of to what extent these topics are addressed in this thesis.

3D electrostatics. In this work, the two devices considered are of dimensions such that there is a significant coupling between all the contacts. For this reason, both devices must be modeled with a three dimensional analysis.

DIBL. Drain induced barrier lowering is the shift of both position and magnitude of the minimum potential along the source to drain symmetry line of a device, thus lowering the barrier for the charge carriers to reach drain. This happens especially for small devices at high source-drain voltages, and can in worst case lead to total lack of gate control. Due to the use of conformal mapping, this effect will be included in the modeling.

Inversion charge. In the near and above threshold regime, the electrostatic influence from the contacts starts to induce a significant amount of inversion charge in the silicon body which have to be taken into consideration. In this work however, only the subthreshold regime is considered and therefore the influence from the inversion charge on the body electrostatics is neglected.

Quantum mechanical effects. Classical theory is still applicable for device dimensions larger than 10nm[4]. All modeling in this work is because of this based on classical theory. Considering quantum mechanical effects are therefore outside the scope of this thesis.

Gate tunneling. In this work, a high-κ insulator material with relative permittivity of 7 and thickness of 1.6nm is considered. The gate tunneling is in this case quite small[5], and will not be considered.

Noise. Noise modeling is beyond the scope of this thesis.

1.4 Outline of thesis

In this thesis, the potential distribution in the cut planes perpendicular to the source-drain symmetry line in the middle of the FinFET and QuadFET, biased to operated in the subthreshold regime, are attempted to be modeled. These potential profiles are important for finding a subthreshold current and capacitance model in future work, and are for these reasons important to model. The devices considered have a low doped, fully depleted body, where the inter-electrode coupling between the contacts dominate the potential distribution. The inversion charge has of this reason been neglected. Conformal mapping is a central tool to solve the Laplace equation in this thesis.

Due to the structural similarities between the QuadFET and the DG MOSFET, the analytical 2D inter-electrode solution for the DG MOSFET has been used to map the cross-section along the source-drain symmetry line of the QuadFET by accounting for the difference in gate control between the two devices. From this, the potential distribution in the cut plane perpendicular to the source-drain axis, also called the vertical plane in the middle of the QuadFET, has been modeled.

For a relatively high FinFET (H=30nm) sitting on a thick substrate, the electrical fields going through the ground plane, into the substrate, is negligible. The analytical solution of the 2D potential distribution for the DG MOSFET has been used as the potential distribution in the ground plane of the FinFET. Further, conformal mapping has been applied to the vertical plane in the center of the device, resulting in a model for this cross-section.

Throughout this thesis, all models and results are compared with, and verified by the numerical device simulator Atlas from Silvaco. Atlas is a numerical solver, which has many different models for physical phenomena such as electrostatics, charge carrier transport, and classical and quantum mechanical carrier statistics. All constants used in the models are for this reason kept the same as in Atlas.

In chapter 2, modeling for different types of MOSFETs, since the late 1960s to present, are briefly reviewed.

In chapter 3, basic theory of conformal mapping is presented. The 2D Laplace equation of a rectangle, ie. (that is) a DG MOSFET, is solved with the conformal mapping technique.

In chapter 4, the conformal mapping technique and the solution to the 2D Laplace equation of the DG MOSFET is used to model the potential distribution in the cut planes

perpendicular to the source-drain direction in the middle of the FinFET and QuadFET. The layouts of the the two devices are presented, and at the end of the chapter, the results are discussed.

In chapter 5, a conclusion of the work in this thesis is given.

Finally, in chapter 6, possible future work is discussed.

Chapter 2

Review of MOSFET modeling

In this chapter, modeling for different types of MOSFETs, since the late 1960s to present, are briefly reviewed.

2.1 History of single gate MOSFET modeling

In the late 1960s and early 1970s, the development of simulation programs aimed to analyze nonlinear circuits started (SPICE released in 1972). Since the fundamental building blocks of integrated circuit simulation tools are the device models, the development of these building blocks started at the same time.

The first MOSFET model for the SPICE simulator, was the simple long-channel charge control model for small substrate doping, also known as the Shichman-Hodges model. It is based on the gradual channel approximation which states that under certain conditions, the electrostatic problem under the gate can be expressed in terms of two coupled one-dimensional equations[6]. The Shichman-Hodges model was modified and replaced by the Meyer I-V model, which included the effects of the depletion charge[7]. These models, called the Level 1 model, describes the current for gate voltages larger than threshold voltage, which means that the subthreshold current is assumed to be zero. Meyer also made a capacitance model based on the simple charge control model[8, pp.170-173], which, however, was not charge conserving.

The Level 2 model, unlike Level 1, does not model the subthreshold current as zero. It addresses second-order effects associated with small-geometry devices. The Ward-Dutton capacitance model was improved compared to the Meyer model in that it is charge conserving[9]. However, the capacitance model of Meyer is a subset of the Ward-Dutton model of Level 2. The problem with Level 2 is that convergence problems are often encountered due to that it is computationally very complex[10].

The Level 3 model is an improvement over Level 2 in that it is a semi-empirical short-channel model, developed to address the shortcomings of Level 2. For this reason, it seldom encounters convergence problems and it also runs faster. The DIBL-effect was included in this level in an empirical way. However, the failure of properly modeling the subthreshold current was a major drawback for Level 3. The capacitance model of level

3 was the Ward-Dutton model and a Meyer-type model[8, pp. 182-183].

Due to the rapid evolution of the MOS technology in the 1980s, the early models are clearly not appropriate to simulate circuits with large number of ever-smaller transistors. Another approach of modeling emerged with the BSIM (Berkeley Short-Channel IGFET Model) models (BSIM1, BSIM2 and HSPICE Level 28), where the creation of new physical models were dropped in favor of mathematical models characterized by a large number of SPICE parameters (more than a hundred in some cases).

In the 1990s, Philips began the third-generation modeling approach with BSIM3, its extension BSIM4 and MOS Model 9, where physically based models were reintroduced. The use of smoothing functions provided a smooth behavior of the device in all the regimes of operation[11].

The models mentioned in this section are the most used models for integrated circuit design from the 1970s to the start of the 21th century. More accurate models for the MOSFET have been created later on, but will not be discussed further in this review.

2.2 Modeling for DG MOSFET and GAA MOSFET (Gate-all-around)

With new devices, there must also be new models. A lot of work have already been done in modeling DG MOSFET and GAA MOSFET (gate-all-around)(see figure 2.1). Presenting all the different types of modeling are out of the scope of this thesis, so, in this section, the work of Fjeldly et al. on subthreshold potential modeling for nanoscale DG MOSFET and GAA MOSFET are shortly described[2][1].

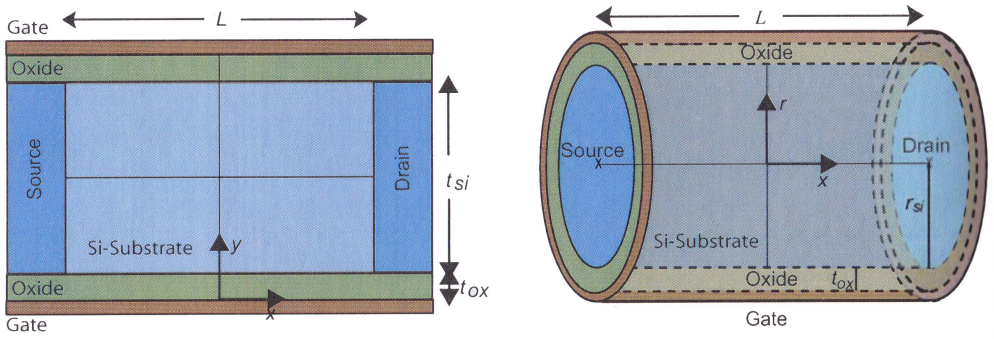

Figure 2.1: Device layout of DG MOSFET and GAA MOSFET in the doctoral thesis of Børli[1]. x and r are axial and radial coordinates, as indicated.

When a DG MOSFET and a GAA MOSFET is operated in the subthreshold regime, the applied voltage at the gates is too small to inflict significant inversion charges in the bodies of the transistors. The only contribution to the potential distribution left are then the inter-electrode potential, which means that the 2D and 3D Poisson's equation, which

have to be solved in order to get the potential distribution, reduces to the corresponding Laplace equation.

Conformal mapping is a mathematical tool used to solve the 2D Laplace equation in a simple way. The mapping was first demonstrated by Klös et al. to map the fields of a semi-infinite slab of silicon[12], where most of the short-channel effects became intrinsic to the model. Later on, the mapping technique was used on a sub-100nm bulk MOSFET by Østhaug et al. with good agreement compared to experimental results[13].

If conformal mapping is used on the DG MOSFET, it transforms (Schwarz-Christoffel) the DG MOSFETs body from the real $x, y \in$Z-plane to the semi-infinite $u, v \in$W-plane[2, ch. 3]. In this semi-infinite u, v-space, the Laplacian has a solution in form of an integral[14, pp. 365] which gives an analytical solution for the inter-electrode potential distribution[2, pp. 35] when integrated over the correct set of boundary conditions. Inverse transforming[2, pp. 30] the analytical solution, maps the inter-electrode potential back into the $x, y \in$Z-plane. The analytical solution agrees very well with numerical simulations. A more thorough explanation of what conformal mapping is and how it is used is given both the work of Kolberg[2] and Børli[1], as well as in chapter 3.1 in this thesis.

Conformal mapping is not directly applicable to the GAA MOSFET because of its 3D electrostatics. However, due to structural similarities between the DG MOSFET and the GAA MOSFET, the analytical solution for the DG MOSFET can be adapted to fit the 3D GAA MOSFET by using the characteristic lengths of the two devices[1, ch. 3.3.1]. A characteristic length is a measure of the penetration depth of the source and drain contacts into the silicon body of the device. By elongating the DG MOSFET, its analytical solution is adapted to give the inter-electrode potential distribution of the GAA MOSFET with great correspondence with numerical simulations[1]. This method is also used in this thesis, on the QuadFET.

Modeling in threshold and strong-inversion region, among other work, have also been performed with good results by Fjeldly et al.[2][1], however this will not be discussed in this review.

2.3 Potential modeling for FinFET

Some modeling have been performed for the FinFET (see figure 2.2), but relatively little compared to the DG- and the GAA MOSFET. Under follows some of the work most related to that of this thesis.

Potential modeling for nanoscale FinFET has been performed by obtaining an analytical solution of the 3D Laplace equation by using series expansion in sine/cosine and hyperbolic functions. By combining this subthreshold solution with a self-consistent solution of the Poisson's and Schrödinger equation for the strong-inversion region, a drain current model has been developed[15]. The results however, are not very impressive.

By considering 3D charge-sharing, top corner effect and surface potential lowering, a threshold voltage model has been made which shows good agreement with numerical simulations[16]

A compact drain current model for a long channel (500nm) GAA MOSFET has been proved to give a good current model for a FinFET with the same dimensions[17].

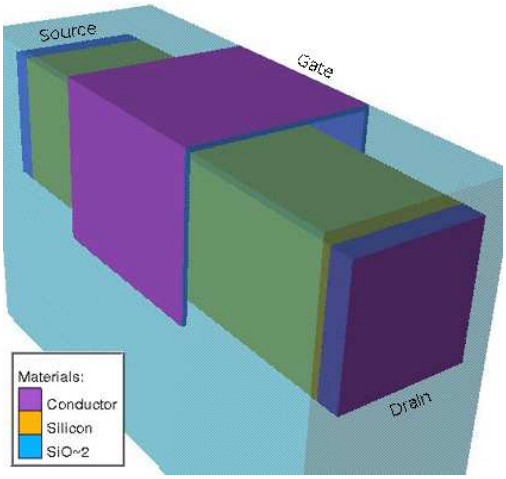

Figure 2.2: Basic layout of a FinFET

2.4 Potential modeling for QuadFET

Work regarding modeling the QuadFET, a transistor with rectangular cross-section and gate all around (see figure 2.3), very little has been done so far. However, the work of solving the 3D Laplace equation in an analytical way by using symmetry properties and parabolic approximations, giving the potential distribution of the device in subthreshold conditions, are under development by Fjeldly et al.

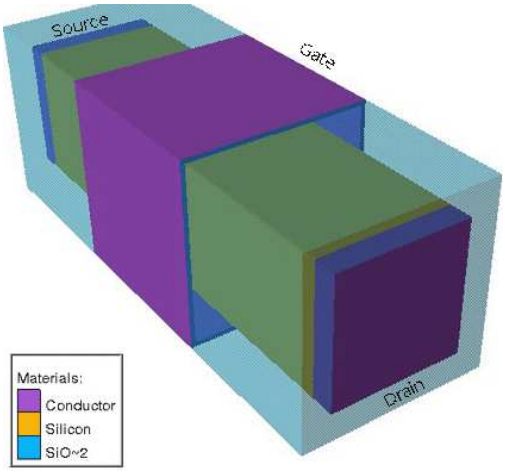

Figure 2.3: Basic layout of a QuadFET

Chapter 3

Basic theory

3.1 Conformal mapping

Conformal mapping is a function which preserves angles and directions of curves, and consists of multiple transformations $z = x + jy = f(w = u + jv)$. The angles and directions are preserved mathematically at any point z_0, except for points where $f'(z)$ is zero. That is, a map is conformal at a point if its derivative do not vanish. A transform of a multi angled polygon in the $x, y \in$Z-plane to the upper half of the $u, v \in$W-plane, is called the Schwarz-Christoffel transformation. This transformation maps the periphery of the polygon to the real axis of the W-plane, and the inner of the polygon to the upper half of the W-plane. A visualization of this transformation is given in fig 3.1.

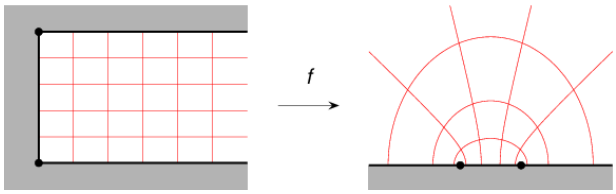

Figure 3.1: Visualization of Schwarz-Christoffel transformation

3.2 Conformal mapping for rectangles

When the transistors considered in this thesis is operated in the subthreshold regime, the electric fields from the inversion charge and the low density of doping charges in the silicon body, can be neglected. This is because the applied potential at the gates do not induce enough charge carriers to significantly affect the potential distribution in the body. Thus, the main contribution to the electrostatic potential comes from the contacts. Further, the main contribution to the subthreshold drain current will be along and near the source-drain symmetry axis in the double-gate, gate-all-around and QuadFET, and along the middle of the bottom plane in the FinFET. In order to find the distribution of

the potential in a cut plane of the FinFET and QuadFET, the 2D Laplace equation

$$\Delta\varphi(x,y) = \nabla^2\varphi(x,y) = -\frac{\rho}{\varepsilon} = 0 \tag{3.1}$$

must be solved. Here, φ(x,y) is the electrostatic potential, ε the permittivity and ρ the charge density in the body. Conformal mapping for a rectangle, ie. for instance the DG MOSFET or a cross section of the FinFET or QuadFET, can be used to solve this equation in the $u, v \in$W-plane, and the solution can then be mapped back into the $x, y \in$Z-plane.

The general Schwarz-Christoffel transformation for a rectangle is given by[14, pp. 354]

$$\frac{\partial z}{\partial w} = \frac{kC}{\sqrt{(1-w^2)(1-k^2w^2)}} \tag{3.2}$$

This transforms the rectangle or a cut from the real Z-plane to the complex W-plane. Here, k is the modulus which is given merely by the geometry of the cut, and $w = u + jv$. The rim of the rectangle now lies along the real u-axis with corners in $-1/k$, $-1/\sqrt{k}$, $1/k$ and $1/\sqrt{k}$, meanwhile the inner of the body is in the semi-infinite room of the complex W-plane. An illustration of the transformation is given in figure 3.2.

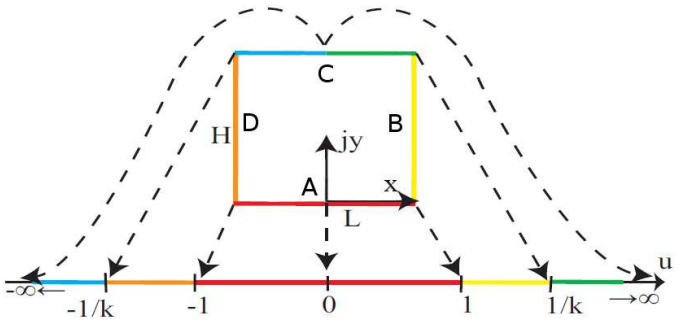

Figure 3.2: Mapping of a rectangle from the x,y∈Z-plane to the u,v∈W-plane[2, ch. 3]

The integral form of equation (3.2) becomes

$$z = kC\int_0^w \frac{\partial w'}{\sqrt{(1-w'^2)(1-k^2w'^2)}} + C_1 = kCF(k,w) + C_1 \tag{3.3}$$

Here C_1 is an integration constant, which is equal to zero if z is chosen to be zero at the center of the lower side L of the rectangle . The constant C is, like k, given by the geometry of the rectangle, and both will be determined in chapter 3.3. F is defined by the Legendre form of the elliptic integral of the first kind, given by[2, pp. 27]

$$F(k,w) = \int_0^w \frac{dw'}{\sqrt{(1-w'^2)(1-k^2w'^2)}}. \tag{3.4}$$

Calculation of equation (3.4) is well defined, so it can be determined by look-up tables, simple iteration algorithms or regular power expansions.

3.3 Geometric constants C and k

In order to complete the transformation from the Z- to the W-plane, the constants C and k must be determined. This is done by integrating (3.3) from $u = -1$ to $u = 1$ (along side A), giving the device length L

$$L = 2kC \int_0^1 \frac{du'}{\sqrt{(1-u'^2)(1-k^2u'^2)}} = 2kCK(k), \tag{3.5}$$

since $v = 0$ and $u = 1$ correspond to the lower right corner of the rectangle (see figure 3.2). Here, $K(k) = F(k, 1)$ is the complete elliptic integral of the first kind.

The height H of the rectangle is correspondingly given by integrating from $u = 1$ to $u = 1/k$ along the boundary, or equivalently from $u = 0$ to $u = 1/k$ subtracting the integral from $u = 0$ to $u = 1$, giving side B of the rectangle. Integrating in such a way results in

$$jH = kC(F(k, \frac{1}{k}) - F(k, 1)) \tag{3.6}$$

Using $F(k, 1) = K(k)$ and $F(k, 1/k) = K(k) - K(k')$, where k'=$\sqrt{1-k^2}$, equation (3.6) becomes

$$jH = jkCK(k') \tag{3.7}$$

Rearranging equation (3.5) gives

$$C = \frac{L}{2kK(k)}, \tag{3.8}$$

and combining this with equation (3.7) results in

$$\frac{L}{2H} = \frac{K(k)}{K(k')} = \frac{K(k)}{K(\sqrt{1-k^2})}, \tag{3.9}$$

which is used to find the modulus k.

Inserting equation (3.8) into the integral form of the Schwarz-Christoffel transformation for the rectangle (equation (3.3)), results in

$$z = x + iy = \frac{L}{2}\frac{F(k, w)}{K(k)} \tag{3.10}$$

3.4 Expressions along boundaries and symmetry lines

Expressions for the elliptic integral ($F(k, w)$) along the boundary and for symmetry lines inside of a device, are very useful when modeling the electrostatics of a transistor. In this section, expressions for mapping along the boundary and symmetry lines of the rectangle

are because of this presented. $F(k,w)$ can be expressed in terms of the standard elliptic integral of the first kind, $K(k)$, in the following way[18]:

From equation (3.4) the elliptic integral for $0 \leq u < 1$ becomes

$$F(k,u) = \int_0^u \frac{du'}{\sqrt{(1-u'^2)(1-k^2u'^2)}} \tag{3.11}$$

When starting to move along side B of the rectangle (see figure 3.2), ie. for $1 < u \leq 1/k$, the imaginary part starts to increase and the elliptic integral becomes

$$\begin{aligned} F(k,u) &= K(k) + j\int_1^u \frac{du'}{\sqrt{(1-u'^2)(1-k^2u'^2)}} \\ &= K(k) + j\left(K(\sqrt{1-k^2}) - F\left(\sqrt{1-k^2}, \sqrt{\frac{1-k^2u^2}{1-k^2}}\right)\right) \end{aligned} \tag{3.12}$$

The real part of the expression for the elliptic integral becomes smaller when moving along the top of the rectangle, ie. for $1/k < u < \infty$, and results in

$$\begin{aligned} F(k,u) &= K(k) + jK(\sqrt{1-k^2}) - \int_{1/k}^u \frac{du'}{\sqrt{(u'^2-1)(k^2u'^2-1)}} \\ &= F\left(\sqrt{1-k^2}, \sqrt{\frac{1-k^2u^2}{1-k^2}}\right) - jK(\sqrt{1-k^2}) \end{aligned} \tag{3.13}$$

For finding the elliptic integral for $-\infty < u < 0$, equation (3.11)-(3.13) are used together with the symmetry property

$$F(k,-u) = -F(k,u) \tag{3.14}$$

By using equation (3.10) together with (3.11)-(3.14), the transformation along the boundary of the rectangle becomes

$$x = \frac{L}{2}\begin{cases} F(k,u)/K(k), & \text{for } u \in \langle -1,1\rangle \quad \text{Side A} \\ 1, & \text{for } u \in \langle 1, \frac{1}{k}\rangle \quad \text{Side B} \\ F(k,\frac{1}{ku})/K(k), & \text{for } u \in \langle \frac{1}{k}, -\frac{1}{k}\rangle \quad \text{Side C} \\ -1, & \text{for } u \in \langle -\frac{1}{k}, -1\rangle \quad \text{Side D} \end{cases} \tag{3.15}$$

and

$$y = H\begin{cases} 0, & \text{for } u \in \langle -1,1\rangle \quad \text{Side A} \\ 1 - F(k', \sqrt{1-k^2u^2}/k')/K(k'), & \text{for } u \in \langle 1, \frac{1}{k}\rangle \quad \text{Side B} \\ 1, & \text{for } u \in \langle \frac{1}{k}, -\frac{1}{k}\rangle \quad \text{Side C} \\ 1 - F(k', \sqrt{1-k^2u^2}/k')/K(k'), & \text{for } u \in \langle -\frac{1}{k}, -1\rangle \quad \text{Side D} \end{cases} \tag{3.16}$$

This mapping is illustrated in the lower part of figure 3.3.

For the symmetry line along the middle, from side A to C of the rectangle, ie. for $u = 0$ and $v \in [0, \infty\rangle$, equation (3.17) is used [2, pp. 29].

$$y = H\frac{F\left(\sqrt{1-k^2}, \frac{v}{\sqrt{1+v^2}}\right)}{K\left(\sqrt{1-k^2}\right)} \tag{3.17}$$

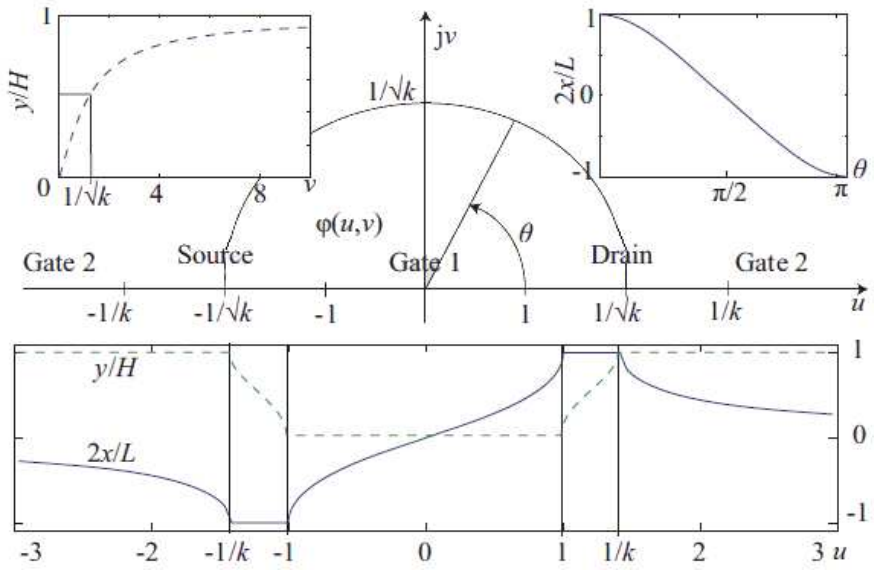

Figure 3.3: The body of a DG MOSFET or a rectangle mapped into the semi-infinite $u, v \in$W-plane. The mapping functions for the rim of the device are shown in the lower part, and the symmetry lines are shown in the upper left (gate-to-gate) and right (source-to-drain) corners. This is a plot produced by Kolberg[2, pp. 29], where k=0.4278.

This symmetry line (3.17) is plotted in the upper left corner of figure 3.3.

The other symmetry line from side B to D is located by keeping $y = H/2$, giving a constant imaginary part in equation (3.10). This requirement is only fulfilled when $v = \sqrt{1/k - u^2}$, giving the side B to D symmetry line a semicircle with radius $v = \sqrt{1/k}$ in the transformed u,v$\in$W-plane [2, pp. 29].

$$x = \frac{L}{2} \frac{F\left(\frac{2\sqrt{k}}{1+k}, \sqrt{k}u\right)}{K\left(\frac{2\sqrt{k}}{1+k}\right)} \tag{3.18}$$

This symmetry line (3.18) is plotted in the upper right corner of figure 3.3. Here, $\theta = cos^{-1}(\sqrt{k}u)$.

3.5 Inverse transformation

Equation (3.17) and (3.18) are used to find the potential along the symmetry lines. However, in order to find the potential in a plane, an inverse transformation of equation (3.10) must be obtained. By defining a regular grid in the $x, y \in$Z-plane and finding the corresponding points in the $u, v \in$W-plane, the following equation is obtained[1, pp. 35].

$$w = u + jv = \frac{sn(k,x)dn(k',y) + j \cdot cn(k,x)dn(k,x)sn(k',y)cn(k',y)}{cn^2(k',y) + k^2 sn^2(k,x)sn^2(k',y)} \tag{3.19}$$

Here, $sn(k,z)$, $cn(k,z)$ and $dn(k,z)$ are three basic Jacobi functions that arises when inverting the elliptic integral $F(k,w)$, which are given by

$$sn(k,z) = sin(am(k,z)) = w \tag{3.20}$$

$$cn(k,z) = cos(am(k,z)) \tag{3.21}$$

$$dn(k,z) = \sqrt{1-k^2 sin^2(am(k,z))} \tag{3.22}$$

Here $am(k,z)$ is the Jacobi amplitude and $k'=\sqrt{1-k^2}$.

Going deeper into the mathematics of conformal mapping is beyond the scope of this thesis. However, more information about conformal mapping can be located in the book by Weber[14].

3.6 Solution of the 2D Laplace equation (DG MOSFET)

A solution of the Laplacian in the $u,v \in$W-plane which describes the body potential, is given by the following integral along the u-axis[14, pp. 365]:

$$\varphi(u,v) = \frac{v}{\pi}\int_{-\infty}^{\infty} \frac{\varphi(u')}{(u-u')^2+v^2}du', \tag{3.23}$$

where φ(u) represents the boundary conditions of the rectangle, ie. for $u \in \langle -\infty, \infty \rangle$.

If the rectangle is applied a potential $V_{gs}-V_{FB}$, $V_{bi}+V_{ds}$, $V_{gs}-V_{FB}$ and V_{bi} along the boundary at side A, B, C and D respectively, the inter-electrode potential distribution throughout the rectangle has the solution (appendix A)

$$\begin{aligned}\varphi(u,v) =& \frac{1}{\pi}\Bigg\{\pi(V_{gs}-V_{FB}) + (V_{bi}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1-ku}{kv}\right) \\ &+ (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1+ku}{kv}\right) \\ &- (V_{bi}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1-u}{v}\right) \\ &- (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1+u}{v}\right)\Bigg\}\end{aligned} \tag{3.24}$$

This is the case for the DG MOSFET for constant boundary conditions, assuming that the influence on the potential in the body from the small oxide gaps, is negligible[19]. V_{gs}, V_{ds}, V_{FB} and V_{bi} are the gate to source potential (side A and C to D), drain to source potential (side B to D), flat-band voltage of the two gates, and the built-in potential which occurs due to the connection between the body and the source and drain contacts, respectively. Figure 3.4 shows the layout of the DG MOSFET used in the doctoral thesis of Sigbjørn Kolberg[2]. In this figure, t_{ox} is replaced by t'_{ox}, which is the oxide thickness using nitrided oxide and undoped silicon respectively, in order to apply

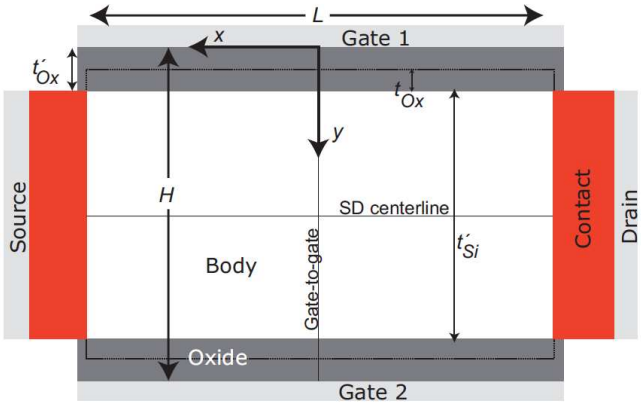

Figure 3.4: Layout of the DG MOSFET (double-gate MOSFET) used in the doctoral thesis of Sigbjørn Kolberg[2].

conformal mapping to the device. This is called extending the device body, and is also done with both the FinFET and the QuadFET later in this thesis.

The potential in the $u, v \in$W-plane along the symmetry lines of the DG MOSFET can be derived from equation (3.24). By keeping $u = 0$, the potential from side A to C (gate-to-gate) along the middle of the rectangle becomes

$$\begin{aligned}\varphi_{G-G}(v) =& \frac{1}{\pi}\Bigg\{2(V_{gs}-V_{FB})tan^{-1}\left(\frac{1}{v}\right) \\ &+ (V_{gs}-V_{FB})\left(\pi - 2tan^{-1}\left(\frac{1}{kv}\right)\right) \\ &+ (2V_{bi}+V_{ds})\left(tan^{-1}\left(\frac{1}{kv}\right) - tan^{-1}\left(\frac{1}{v}\right)\right)\Bigg\}\end{aligned} \tag{3.25}$$

Holding $v = \sqrt{1/k - u^2}$, which represents a semi-circle with radius $\sqrt{1/k}$ in the $u, v \in$W-plane, gives the potential along the other symmetry line of the rectangle, ie. from side B to D (source-to-drain), and equation (3.24) results in

$$\begin{aligned}\varphi_{S-D}(u) =& \frac{1}{\pi}\Bigg\{\pi(V_{gs}-V_{FB}) - (V_{gs}-V_{FB}-V_{bi})tan^{-1}\left(\frac{1-ku}{k\sqrt{1/k-u^2}}\right) \\ &- (V_{gs}-V_{FB}-V_{bi}-V_{ds})tan^{-1}\left(\frac{1+ku}{k\sqrt{1/k-u^2}}\right) \\ &+ (V_{gs}-V_{FB}-V_{bi})tan^{-1}\left(\frac{1-u}{\sqrt{1/k-u^2}}\right) \\ &+ (V_{gs}-V_{FB}-V_{bi}-V_{ds})tan^{-1}\left(\frac{1+u}{\sqrt{1/k-u^2}}\right)\Bigg\}\end{aligned} \tag{3.26}$$

Chapter 4

Potential modeling of FinFET and QuadFET

4.1 Device structures

The geometric layouts of the devices considered in this thesis are shown in figure 4.1 and 4.2. Both devices have gate length L=30nm and oxide thickness t_{ox}=1.6nm if not

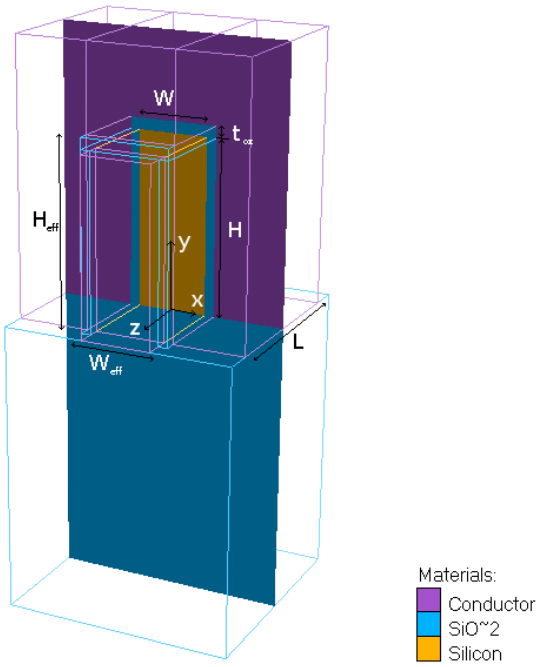

Figure 4.1: Geometric layout of the FinFET

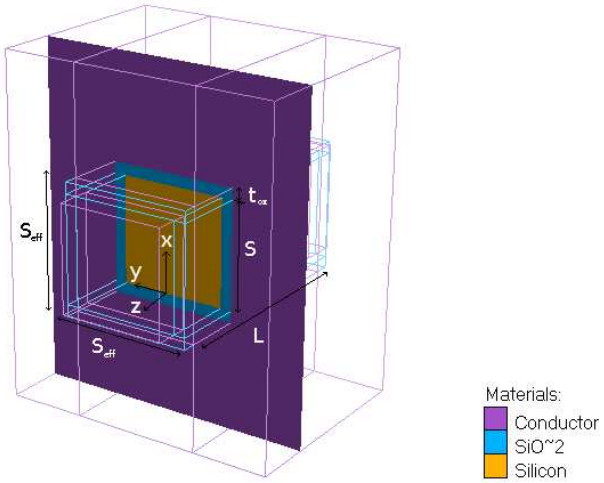

Figure 4.2: Geometric layout of the QuadFET with quadratic cross-section

specified otherwise.

In the FinFET, H_{eff}=H+t'_{ox} and W_{eff}=W+2t'_{ox} are the effective height and effective width of the device, respectively. Here, t'_{ox}=$t_{ox}\varepsilon_{Si}/\varepsilon_{ox}$ is the effective oxide thickness of the extended silicon body. ε_{ox} and ε_{Si} are the permittivity of nitrided oxide and undoped silicon, which are 7 and 11.9, respectively. If not specified otherwise, the height of the FinFET is H=30nm, and the width is W=12nm.

The QuadFET got a quadratic shape of the body with effective length of sides S_{eff}=S+2t'$_{ox}$. The sides are S=15nm if not specified otherwise.

The reason for extending the devices by using undoped silicon instead of nitrided oxide, is to apply conformal mapping to the transistors. This extension of a body can be performed if the assumption that the oxide thickness is relatively small compared to the thickness of the body, is made.

The bodies are doped with an acceptor concentration N_a of 10^{15}cm^{-3} in both devices, and they have both idealized Schottky contacts to the source and drain, which means negligible series resistance and no depletion regions. These contacts have a work function Φ_s=4.17eV, corresponding to that of n^+ silicon. The metal used at the gate contacts is a near mid-gap material with work function Φ_m=4.53eV, which corresponds to that of molybdenum. All the contacts in both devices are assumed to have equipotential surfaces.

In both devices, electrons will diffuse from the source and drain contacts, recombining with the holes in the acceptor doped body, thus making it fully depleted in all regimes of operation. This results in better gate control[20].

The built-in and flat-band voltages of both devices are given by

$$V_{bi} = \frac{E_g}{2q} + \phi_b + \frac{k_B T}{2q} ln\left(\frac{N_C}{N_V}\right), \tag{4.1}$$

and

$$V_{FB} = \frac{(\Phi_m - (\chi + \frac{E_g}{2} + q\phi_b))}{q} - \frac{k_B T}{2q} ln\left(\frac{N_C}{N_V}\right), \tag{4.2}$$

respectively. E_g is the silicon bandgap, χ is the electronic affinity for silicon, and ϕ_b=V_{th}ln(N_a/n_i) is the potential difference between Fermi levels of intrinsic and doped silicon. N_C and N_V are the effective density of states in the conduction and valence band. They are functions of the effective mass of electrons m_n and holes m_h as

$$N_C = 2\left(\frac{m_n k_B T}{2\pi\hbar}\right)^{3/2}, N_V = 2\left(\frac{m_p k_B T}{2\pi\hbar}\right)^{3/2}. \tag{4.3}$$

In this work however, they are assumed to be constants taken directly from Atlas, equal to N_C=2.84·10^{25}cm^{-3} and N_V=1.04·10^{25}cm^{-3}, since the purpose of this project is to test the models against numerical simulations.

4.2 Conformal mapping for QuadFET

Conformal mapping on a QuadFET requires to make the potential problem (Laplace equation 3.1) a two dimensional one. In the approach investigated, the potential profile in x- and y-direction of the QuadFET, ie. in the directions perpendicular to the source-drain direction, are assumed to be equal, which is a fair assumption. The analytical solution for the DG MOSFET is then adapted to the QuadFET by a technique proposed and used by Håkon Børli [19]. This adaption is illustrated in figure 4.3.

The major difference between a QuadFET and a DG device is the gate control. This difference can be expressed in terms of the characteristic lengths of the two devices, which is a measure of the electrostatic penetration depth of the source and drain contacts along the source-drain symmetry line. The characteristic lengths of the QuadFET and the DG MOSFET are given by[21, pp. 22]

$$\lambda_{Quad} = \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}} t_{ox} S} \tag{4.4}$$

$$\lambda_{DG} = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{ox} t_{si}}, \tag{4.5}$$

respectively. The characteristic length of the DG MOSFET used in this thesis is slightly different than the one used in the doctoral thesis of Børli[1].

By elongating the DG device to

$$L' = \frac{\lambda_{DG}}{\lambda_{Quad}} L, \tag{4.6}$$

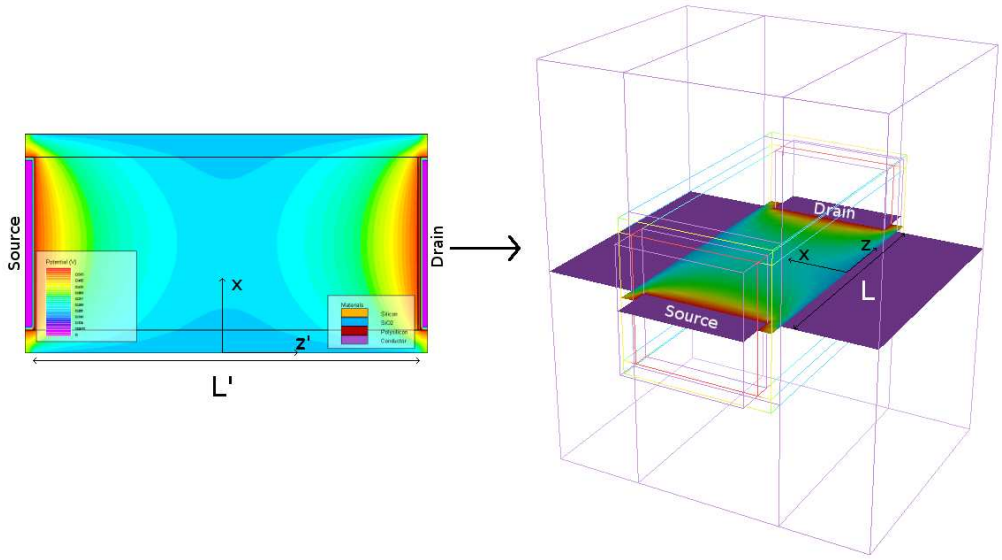

Figure 4.3: Illustration of adapting the potential profile from an elongated DG MOSFET with gate length $\lambda_{DG}/\lambda_{Quad}{\cdot}L$ (left), to the potential profile of a QuadFET with gate length L(right).

where L is the original gate length of the QuadFET, giving the device a modulus k′ given by

$$\frac{K(k')}{K(\sqrt{1-k'^2})} = \frac{L'}{2S_{eff}}, \tag{4.7}$$

and using equation (3.23), the inter-electrode potential distribution in the plane along the source-drain symmetry line of the QuadFET becomes

$$\begin{aligned}\varphi'(u,v) =& \frac{1}{\pi}\Bigg\{\pi(V_{gs}-V_{FB}) + (V_{bi}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1-k'u}{k'v}\right)\\ &+ (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1+k'u}{k'v}\right)\\ &- (V_{bi}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1-u}{v}\right)\\ &- (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\left(\frac{1+u}{v}\right)\Bigg\}\end{aligned} \tag{4.8}$$

The ratio $\lambda_{DG}/\lambda_{Quad}{=}\sqrt{2}$ is called the scaling factor, due to the fact that it is the length the DG MOSFET is scaled with.

By inverse transforming $\varphi'(u,v)$ with equation (3.19), the potential distribution is mapped back into the (x,z')-coordinates of the extended DG MOSFET. Compressing $\varphi(x,z')$ uniformly in the longitudinal direction, using the inverse scaling factor of

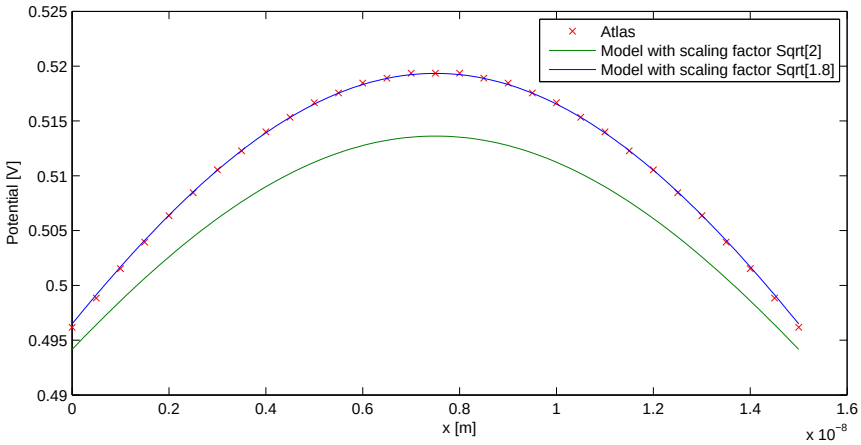

Figure 4.4: Comparison of the potential distribution in the middle of the device along the gate-to-gate symmetry line (ie. in the x-direction) with scaling factor $\lambda_{DG}/\lambda_{Quad} = \sqrt{2}$ (solid green) and $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$ (solid blue). Red crosses represents numerical simulations with Atlas. The plot is only through the body, without the oxides. V_{gs}=0V and V_{ds}=0V.

$\lambda_{Quad}/\lambda_{DG}$, results in a solution of the inter-electrode potential distribution of the Quad-FET. The only difference from the potential distribution of the QuadFET to that of the DG MOSFET, is the modulus k.

By holding u=0 in equation (4.8), the gate-to-gate symmetry line of the QuadFET is obtained in the same way as for equation (3.25). When this potential distribution is compared to numerical simulations, an error of approximately 5.7mV is obtained at the position v=$\sqrt{1/k'}$, ie. at the potential maximum in the vertical plane φ_m (see figure 4.4). The assumption made earlier in this chapter, that the potential profile in the x- and y-direction is equal, is the cause of the error. The assumption is only valid along the source-drain axis. When moving outside this axis, the assumption is broken, and an error is introduced. The total potential in the vertical plane is pulled down, resulting in a noticeable underestimation of φ_m.

Because of the underestimation, a new scaling factor is purposed. By extracting the maximum potential in the middle of the vertical cut for zero applied potential from numerical simulations, using equation (4.8), (4.7) and (4.6) to trace the scaling factor backwards, results in $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$. The inter-electrode potential distribution of the QuadFET is then obtained in the same way as for the scaling factor of $\lambda_{DG}/\lambda_{Quad} = \sqrt{2}$. The improved result is presented in figure 4.4.

The scalability of the purposed scaling factor $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$, ie. the capability of the scaling factor to produce good results with changing geometry, has been tested by comparing the maximum potential in the vertical plane φ_m for different geometry with Atlas. Figure 4.5 and 4.6 shows the great correspondence of φ_m to numerical simulations for gate lengths $L = \{15, 50\}$nm and thickness of sides $S = \{5, 25\}$nm, respectively. The model has of course a direct match with numerical simulations at gate

length L=30nm and sides S=15nm since the scaling factor has been extracted from Atlas for this geometry.

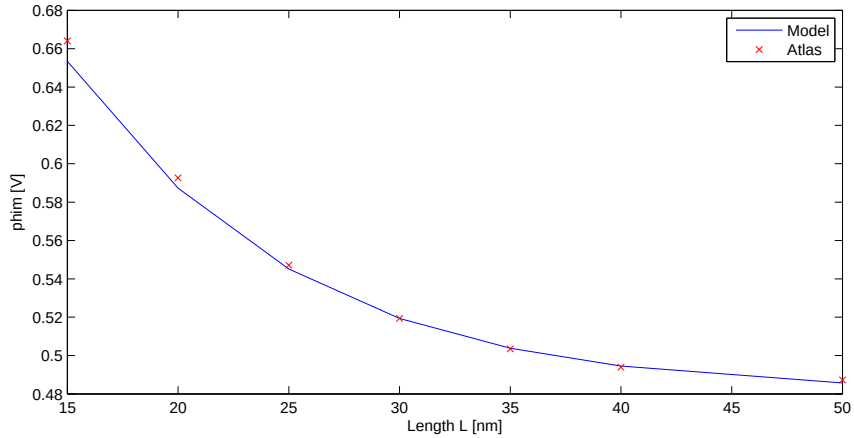

Figure 4.5: Gate length L testing of the scaling factor $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$ by comparing φ_m from model (solid blue line) with the one from Atlas (red crosses). V_{gs}=0V and V_{ds}=0V.

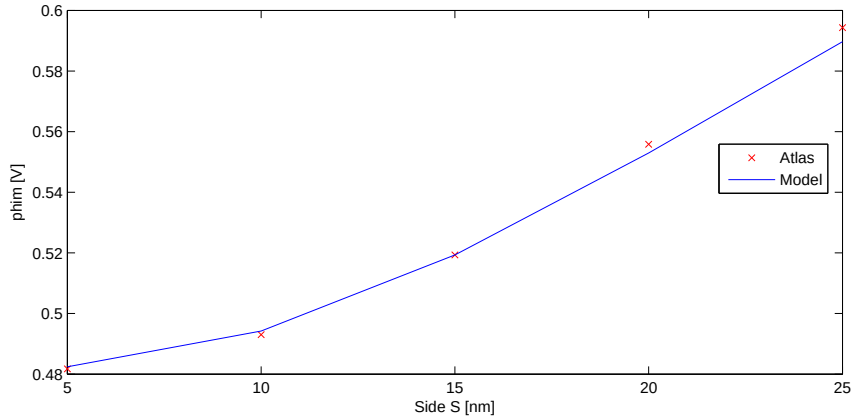

Figure 4.6: Side length S testing of scaling factor $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$ by comparing φ_m from model (solid blue line) with the one from Atlas (red crosses). V_{gs}=0V and V_{ds}=0V.

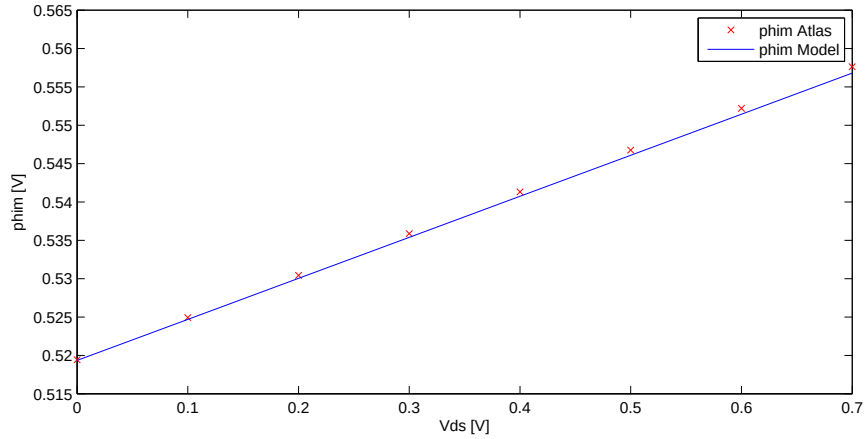

Figure 4.7: V_{ds} testing the scaling factor $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$ by changing the applied source-drain voltage and comparing φ_m from model (solid blue line) with the one from Atlas (red crosses). V_{gs}=0V

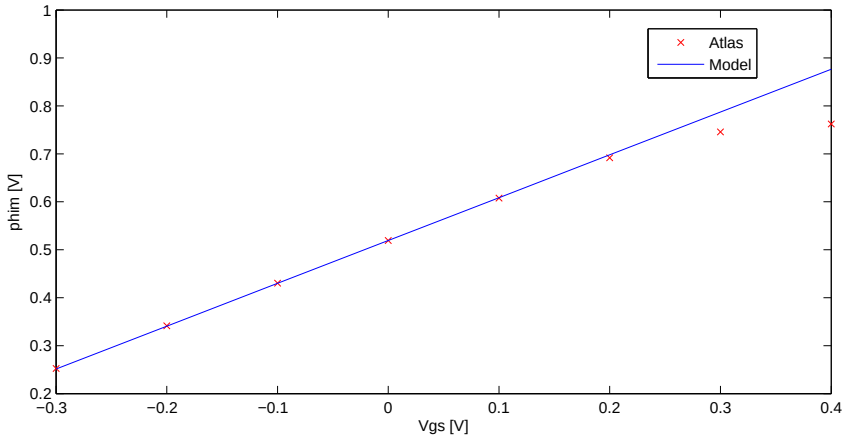

Figure 4.8: V_{gs} testing the scaling factor $\lambda_{DG}/\lambda_{Quad} \approx \sqrt{1.8}$ by changing the applied gate-source voltage and comparing φ_m from model (solid blue line) with the one from Atlas (red crosses). For gate-source voltages above 0.2V, the model breaks down since the transistor enters the near and above threshold regime. V_{ds}=0V.

The scaling factor has also been tested for different voltages. Figure 4.7 and 4.8 shows the great agreement of φ_m with numerical simulations for different contact voltages, $V_{ds} = \{0, 0.7\}$V and $V_{gs} = \{-0.3, 0.4\}$V respectively. At $V_{gs} \approx 0.3$V, the QuadFET enters the threshold regime, and the model based on conformal mapping breaks down due to the increasing amount of inversion charge in the body that have not been calculated for. However, in the subthreshold regime, the model agrees very well with numerical simulations. The good agreement with Atlas for high V_{ds}, shows how well the conformal mapping includes DIBL. For very high voltages (0.5-0.7V) however, the applied potential starts to induce a lot of carriers in the body near the source and drain, resulting in a higher φ_m than calculated for. The results however, are still very good, even though the device never will be operated with such high source-drain voltages.

4.3 Parabolic approximation for QuadFET

By using equation (4.8) together with (3.17), results in an expression for the gate-to-gate potential distribution in the middle of the device. However, in order to find the potential distribution in the whole vertical plane, not just along the symmetry lines, a parabolic approximation of the gate-to-gate potential distribution must be made in both x- and y-direction. A parabolic approximation with the form

$$\varphi(y) = \varphi_c\Big(1 - \Big(\frac{2y}{S_{eff}}\Big)^2\Big) + V_{gs} - V_{FB} \tag{4.9}$$

is used in the y-direction, and the corresponding approximation

$$\varphi(x) = \varphi_c\Big(1 - \Big(1 - \frac{2x}{S_{eff}}\Big)^2\Big) + V_{gs} - V_{FB} \tag{4.10}$$

in the x-direction. Here φ_c=φ_m−V$_{gs}$+V$_{FB}$. The total expression for the vertical plane, after inserting (4.9) into (4.10), becomes

$$\varphi(x,y) = \Big(\varphi_c\Big(1 - \Big(\frac{2y}{S_{eff}}\Big)^2\Big) + V_{gs} - V_{FB}\Big)\Big(1 - \Big(1 - \frac{2x}{S_{eff}}\Big)^2\Big) + V_{gs} - V_{FB} \tag{4.11}$$

Figure 4.9 shows a surface plot of the modeled potential profile in the vertical plane based on the parabolic approximation. In this figure, the potential in the oxide is included.

Figure 4.10 and 4.12 shows a contour and a surface plot of the model compared with numerical simulations with zero applied potential (V_{gs}=0V, V_{ds}=0V). These are in contrast to figure 4.9 in that they are plotted without the oxide. The model corresponds very well with Atlas in the middle of the device, which is the most important region when regarding the subthreshold current. However, when moving towards one of the four gates, the error becomes larger. The parabolic approximation is the reason for this increasing error since the distribution is not ideally parabolic, as figure 4.11 and 4.13 clearly shows.

Figure 4.14 shows another contour plot of the vertical plane, only biased differently (V_{ds}=0.3, V_{gs}=0), with the same good correspondence with numerical simulations as figure 4.10.

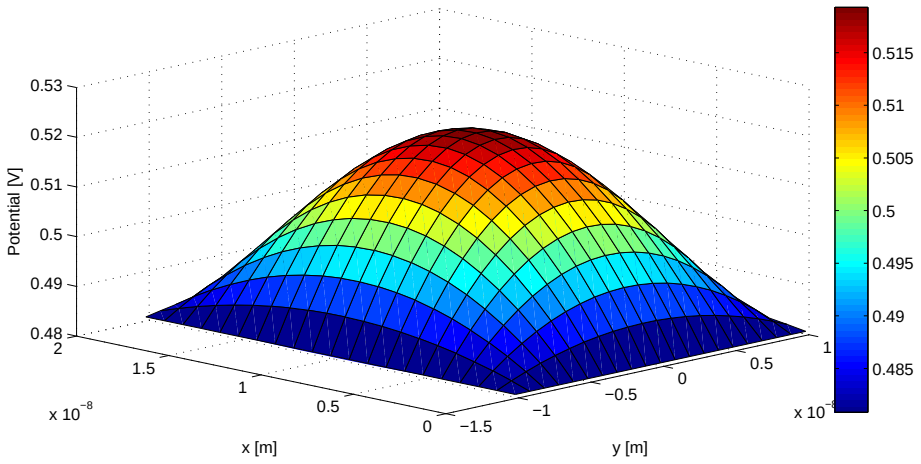

Figure 4.9: Modeled vertical plane potential profile in the middle of the QuadFET with parabolic approximation. The potential in the oxide is included in this plot, and V_{gs}=0 and V_{ds}=0.

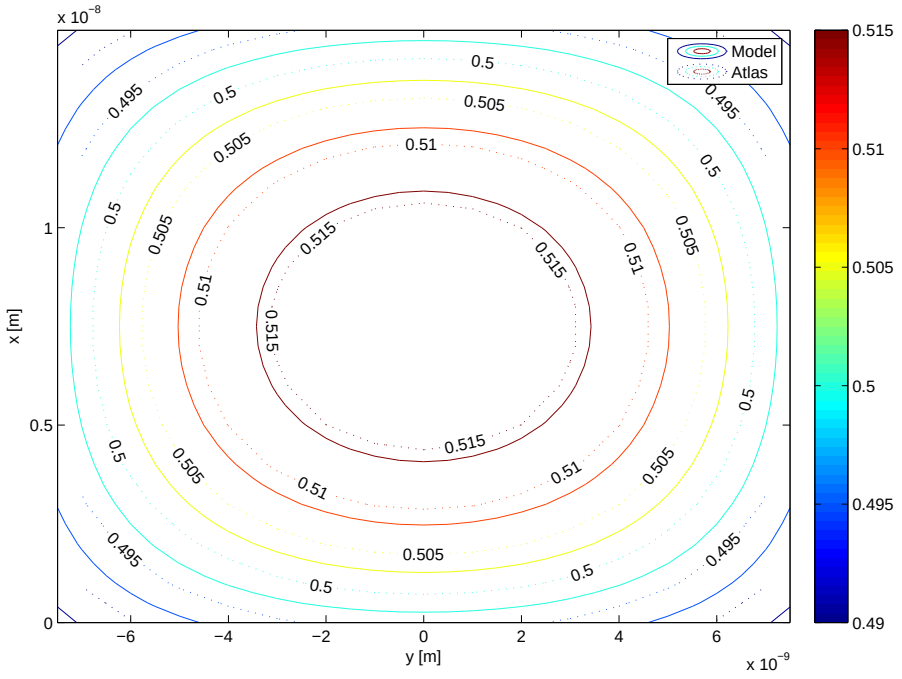

Figure 4.10: Contour plot of the potential distribution in the vertical plane in the middle (z=0) of the QuadFET, without the oxide. Solid lines represents the model, meanwhile dotted lines represents data from numerical simulations. V_{gs}=0V and V_{ds}=0V.

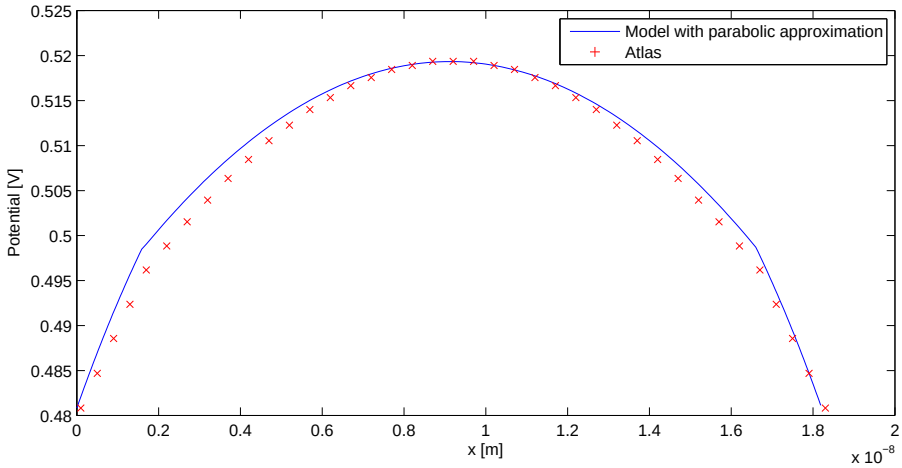

Figure 4.11: Gate-to-gate potential profile with oxides, where solid blue line represents the model with parabolic approximation, and red crosses represents numerical simulations. V_{gs}=0V and V_{ds}=0V.

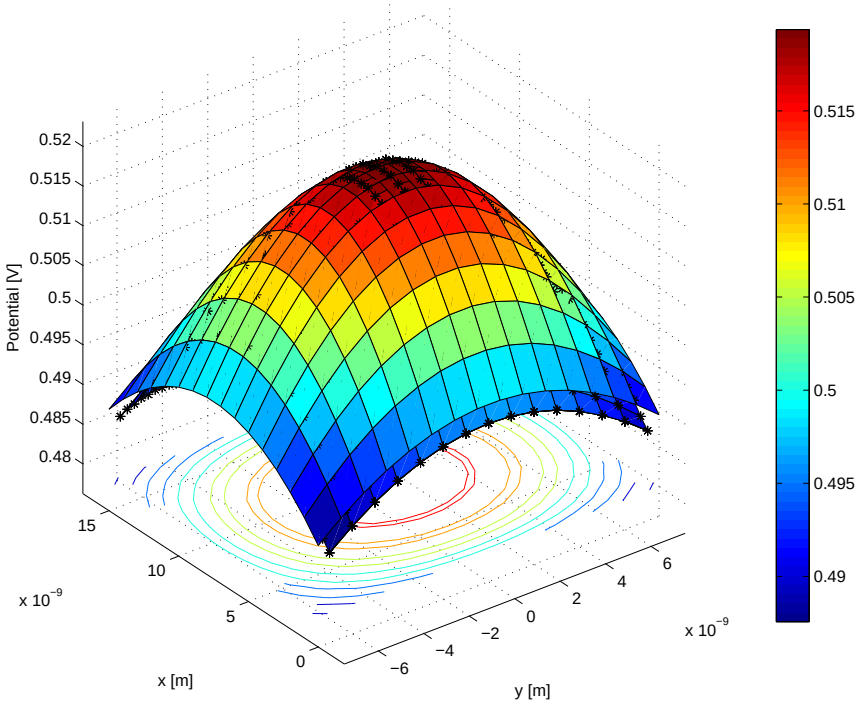

Figure 4.12: Surface plot of the potential distribution in the vertical plane in the middle (z=0) of the QuadFET, without oxides. Surface plot with crosses represents numerical simulations, and without crosses represents the model. V_{gs}=0 and V_{ds}=0.

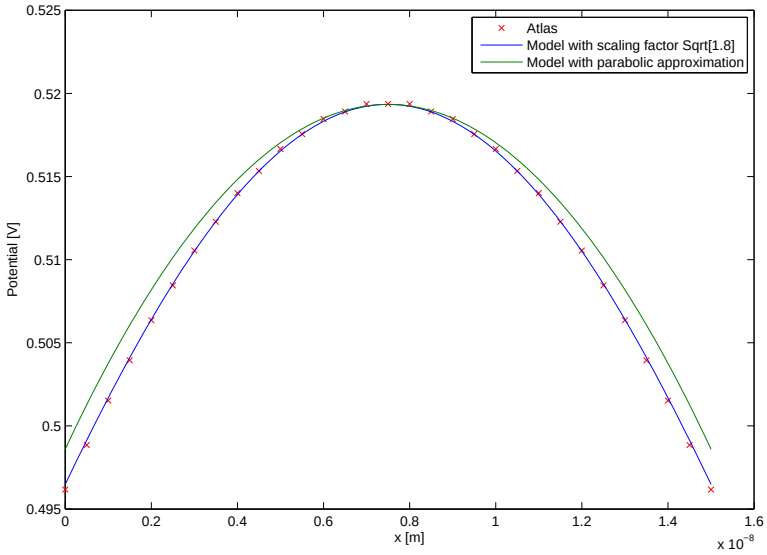

Figure 4.13: Gate-to-gate potential in the middle of the QuadFET (z=0) from numerical simulations (red crosses), model taken directly from conformal mapping (without parabolic approximation) (solid blue line), and model with parabolic approximation (solid green line). The plot is also here without the oxide. V_{gs}=0 and V_{ds}=0.

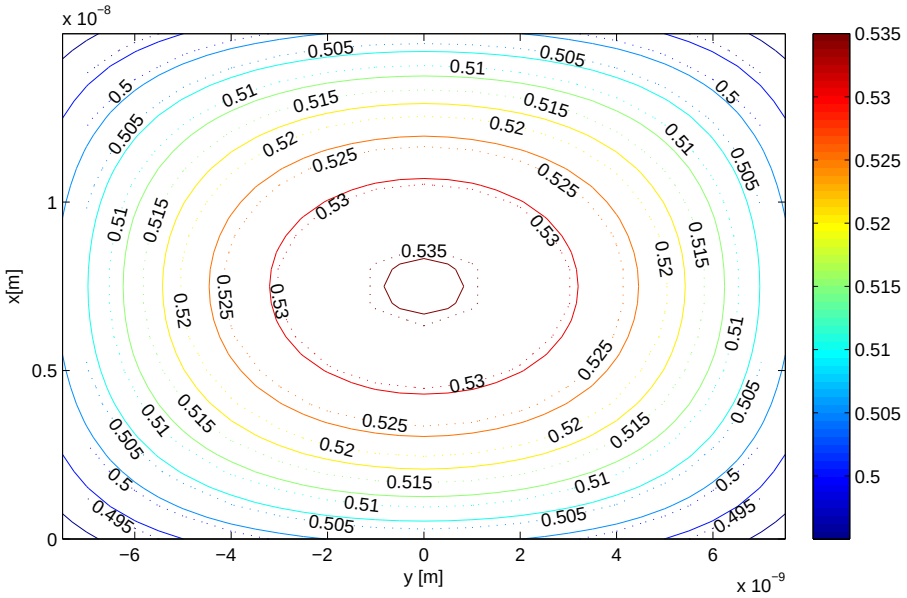

Figure 4.14: Contour plot of the potential distribution in the vertical plane in the middle (z=0) of the QuadFET, without the oxides. Solid lines represents the model, meanwhile dotted lines represents data from simulation with Atlas. V_{gs}=0 and V_{ds}=0.3

Figure 4.15 indicates again how well conformal mapping handles the DIBL-effect. However, when the minimum potential along the source-to-drain symmetry line moves towards source, the modeled vertical plane looses the appropriate potential to model the subthreshold current correctly. If a subthreshold current model is made from the vertical potential model presented in this thesis, the current would have been overestimated for large V_{ds}, because of the DIBL-effect. For this reason, it is important to also model the potential in other vertical planes in order to include the DIBL-effect in the current model.

The biggest error in the model for the vertical plane will be at the corners. The potential along the diagonal is plotted in figure 4.16 to show how big this error is.

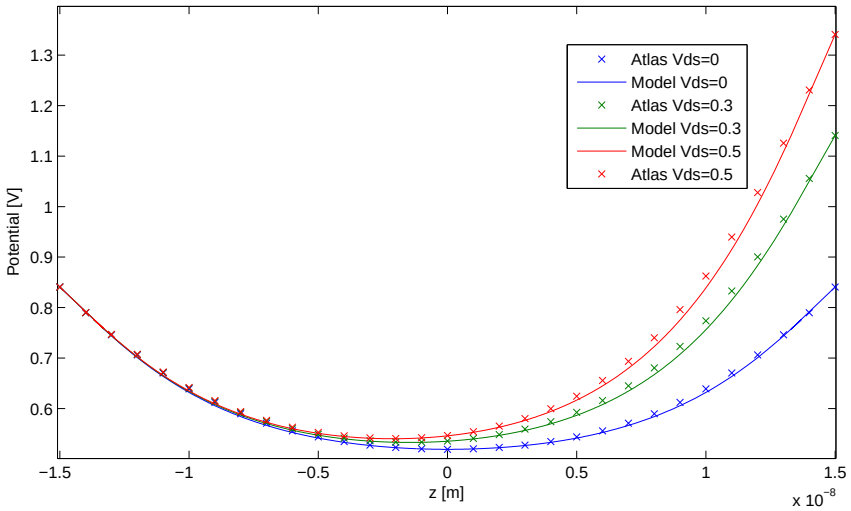

Figure 4.15: Potential distribution along the source-to-drain symmetry line in the QuadFET, where solid lines represents the model and crosses the numerical simulations. The DIBL-effect is shown, where the potential barrier decreases and shifts towards source. V_{gs}=0 and V_{ds}={0, 0.3, 0.5}.

4.4 Conformal mapping for FinFET

The FinFET is a more difficult device to model compared to the QuadFET, since it does not have the symmetry properties of the QuadFET. In order to use conformal mapping on the FinFET, also here the 3D Laplace equation must be made 2D. A method of doing it, is in this section tested.

When conformal mapping is applied on the vertical plane in the middle of the FinFET, the potential in the ground plane is the only potential at the boundary that is unknown and not constant. Since conformal mapping without constant boundary conditions is difficult to solve, an easy function for the potential in the ground plane must be obtained in order to solve equation (3.23).

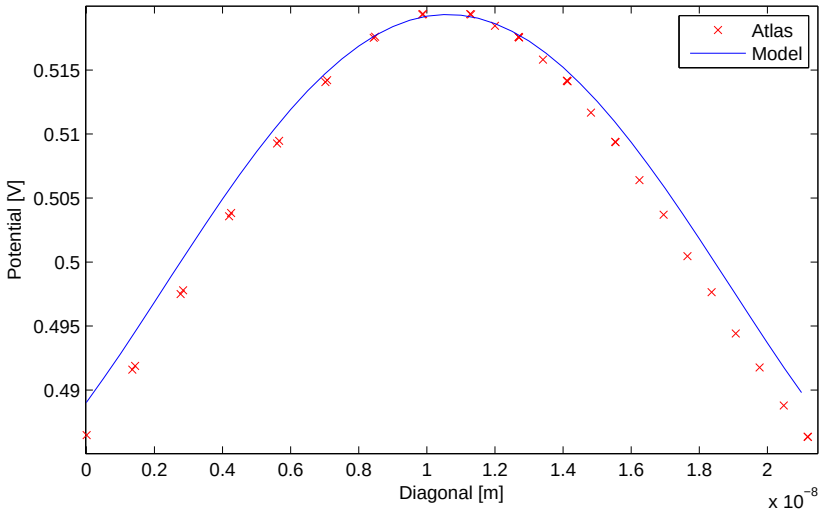

Figure 4.16: Potential along the diagonal of the vertical plane, where solid blue line represents the model and red crosses are numerical simulations. The plot is without the oxides, and V_{gs}=0 and V_{ds}=0.

If the height of the FinFET and the thickness of the substrate are relatively large, the vertical electric fields going into the substrate, through the ground plane, is negligible. The analytical solution of the inter-electrode potential distribution of a DG MOSFET [2] [1] is because of this used in the ground plane of the FinFET, giving the last boundary of the cut. The mapping of the FinFET is illustrated in figure 4.17.

However, the potential distribution along the gate-to-gate symmetry line in the DG device, given by equation (3.25), can not be used directly as the potential along the last boundary of the cut, ie. from u=-1 to u=1 (see dotted blue line in figure 4.17). A couple of approximations must first be introduced in order to obtain an analytical solution from equation (3.23).

By making a parabolic approximation of the gate-to-gate potential of the DG device with the form

$$\varphi(x, y = 0, z = 0) = \varphi_c(1 - \left(\frac{2x}{W}\right)^2) + V_{gs} - V_{FB}, \tag{4.12}$$

brings equation (3.23) one step closer to be solved. Here W is the width of the FinFET, φ_c=φ_m-V_{gs}+V_{FB} and φ_m is the maximum potential in the vertical plane. Transforming equation (4.12) to the $u, v \in$W-plane using equation (3.15) for $u \in \langle -1, 1\rangle$ results in

$$\varphi(u, v = 0) = \varphi_c\Big(1 - \Big(\frac{F(k, u)}{K(k)}\Big)^2\Big) + V_{gs} - V_{FB}, \tag{4.13}$$

Still, this potential distribution is too difficult to solve, so another approximation must be made for $F(k, u)$ (appendix B):

$$F^2(k, u) \approx 2(K^2(k) - 1) - 2(K^2(k) - 1)\sqrt{1 - u^2} + (2 - K^2(k))u^2 \tag{4.14}$$

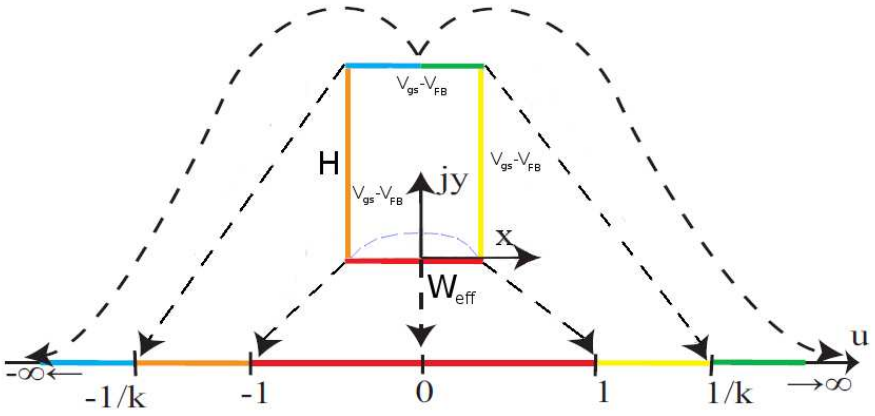

Figure 4.17: Mapping of the vertical plane of a FinFET from the x,y∈Z-plane to the u,v∈W-plane. The close to parabolic potential distribution in the ground plane is illustrated with dotted blue line.

Figure 4.18 shows how well the approximated $F^2(k,u)$ reproduce the exact one for low values of k ($k \approx 0.011$).

The resulting inter-electrode potential distribution of the FinFET, using the approximation for $F^2(k,u)$ in equation (4.14), together with equation (4.13) in equation (3.23), becomes (appendix C)

$$\varphi(u,v) = (V_{gs}-V_{FB}) + \frac{\varphi_c}{\pi}\left(tan^{-1}\left(\frac{1-u}{v}\right)+tan^{-1}\left(\frac{1+u}{v}\right)\right) - \frac{v\varphi_c}{\pi K^2(k)}\int_{-1}^{1}\frac{F^2(k,u')}{(u-u')^2+v^2}du', \tag{4.15}$$

where

$$\begin{aligned}
&\int_{-1}^{1}\frac{F^2(k,u)}{(u-u')^2+v^2} = \int_{-1}^{1}\frac{C+D\sqrt{1-u^2}+Eu^2}{(u-u')^2+v^2} \\
&= -\frac{2(1-K^2(k))}{v}\left(tan^{-1}\left(\frac{1-u}{v}\right)+tan^{-1}\left(\frac{1+u}{v}\right)\right) \\
&+ 2(1-K^2(k))\left(\pi + \frac{\pi}{v}\left[(1+v^2-u^2)+(2uv)^2\right]^{\frac{1}{4}}\sqrt{\frac{1}{2}\left(\sqrt{\frac{(1+v^2-u^2)^2}{(1+v^2-u^2)^2+(2uv)^2}}+1\right)}\right) \\
&+ (2-K^2(k))\left(2+\frac{u^2-v^2}{v}\left(tan^{-1}\left(\frac{1-u}{v}\right)+tan^{-1}\left(\frac{1+u}{v}\right)\right)+uln\left(\frac{1-2u+u^2+v^2}{1+2u+u^2+v^2}\right)\right)
\end{aligned} \tag{4.16}$$

A plot of the distribution from the ground plane to top-gate symmetry line (using equation (4.16) together with (3.17)), shown in figure 4.19, clearly indicates that the model fails miserably in reproducing the numerical simulation. The reason is that the curvature in the z-direction (source to drain) is neglected. In the ground plane (y=0),

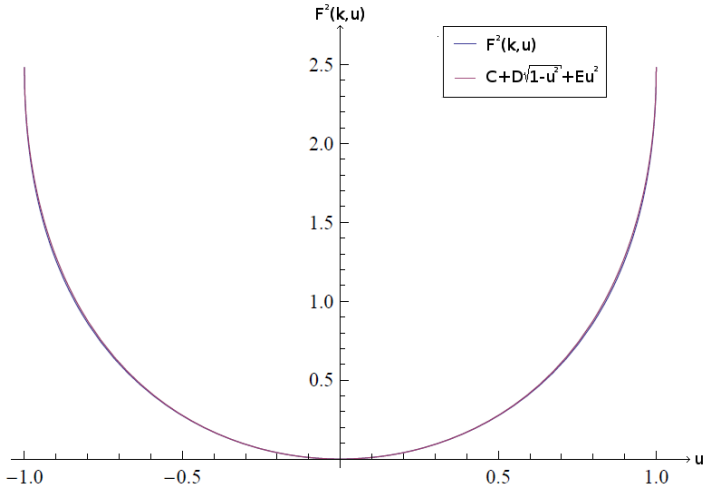

Figure 4.18: Approximated $F^2(k,u)$ (purple line) and the actual value of $F^2(k,u)$ (blue line). The modulus $k \approx 0.011$.

the curvature in the z-direction is calculated for due to the analytical solution from the DG device, which results in a perfect match with numerical simulations. However, when moving towards the top-gate ($y > 0$), $\partial^2\varphi/\partial z^2 = 0$, which results in a failed attempt to model the cut plane perpendicular to the source-drain symmetry line in the middle of the FinFET.

The reason of the small slope in the numerical simulation close to the ground plane (figure 4.19), is due to the fringe fields from the contacts going through the ground plane. However, this slope is so small that the fringe fields can be neglected.

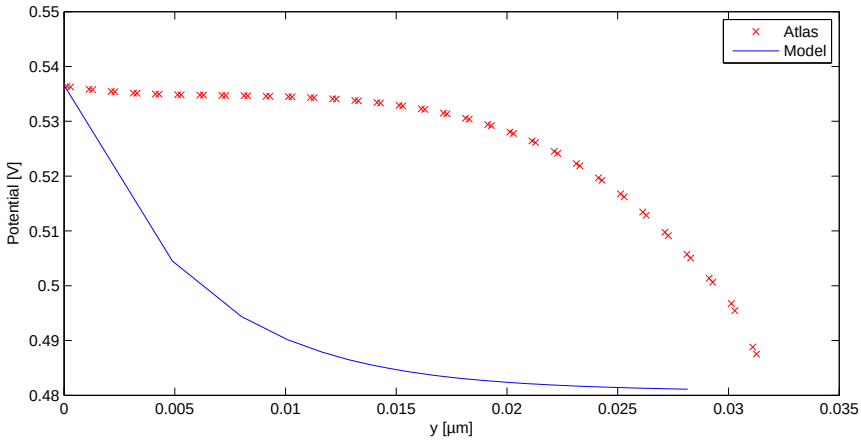

Figure 4.19: Ground plane (y=0) to top-gate (y=H_{eff}) symmetry line potential, where solid blue line represents the model and red crosses represents numerical simulations.

4.5 Oxide gap correction

Considering the extended bodies of the QuadFET and DG MOSFET closely, the boundaries are found to be piecewise equipotential except at the oxide gaps. In these small gaps, the potential distribution has been shown to be close to linear by numerical simulations [14]. In this thesis however, the gaps have been modeled as in the work of Sigbjørn Kolberg[2], by extending the source and drain $1/8t'_{ox}$ closer to the gates and extending the gates $7/8t'_{ox}$ closer to the source and drain, adjoining the contacts. This has proven to give an accuracy in the mV regime in the center of the body[2, pp. 34].

By applying this oxide correction, disregarding the different k's (k and k'), the expression for the potential in the QuadFET (4.8) and DG MOSFET (3.24) becomes (appendix D)

$$\begin{aligned}\varphi(u,v) =& \frac{1}{\pi}\Bigg\{ V_{bi}\left(tan^{-1}\left(\frac{1/k-\Delta u_2-u}{v}\right) - tan^{-1}\left(\frac{1+\Delta u_1-u}{v}\right)\right) \\ &+ (V_{gs}-V_{FB})\left(tan^{-1}\left(\frac{1+\Delta u_1-u}{v}\right) + tan^{-1}\left(\frac{1+\Delta u_1+u}{v}\right)\right) \\ &+ (V_{gs}-V_{FB})\left(\pi - tan^{-1}\left(\frac{1/k-\Delta u_2+u}{v}\right) - tan^{-1}\left(\frac{1/k-\Delta u_2-u}{v}\right)\right) \\ &+ (V_{bi}+V_{ds})\left(tan^{-1}\left(\frac{1/k-\Delta u_2+u}{v}\right) - tan^{-1}\left(\frac{1+\Delta u_1+u}{v}\right)\right) \end{aligned} \tag{4.17}$$

where Δu_1 and Δu_2 are the transformation of $7/8t'_{ox}$ at $u = 1$ or $u = -1$ and $u = 1/k$ or $u = -1/k$, respectively.

4.6 Discussion

In this chapter, the problem of modeling the potential distribution in the cut planes perpendicular to the source-drain symmetry lines in the middle of both nanoscale FinFET and QuadFET, have been confronted. When the two devices are operated in subthreshold, the main contribution to the device electrostatics is the inter-electrode capacitive coupling. In the process of modeling, the three dimensional Laplace equation has been attempted to be made two dimensional in order to use conformal mapping, by using the analogy of the devices to the DG MOSFET. Since there already exist good models based on conformal mapping for the DG MOSFET, this seems to be a good approach.

In the case of the FinFET, the three dimensional problem was not successfully converted to a two dimensional one, due to neglecting the curvature in the source-drain direction above the ground plane of the device. The modeling of the vertical plane of the FinFET failed miserably because of this. However, an attempt of modeling the transistor has been tested, and the electrostatics of the device is better known.

In the case of the QuadFET however, by the use of symmetry properties and clever adaption of the solution from the DG MOSFET, the potential distribution in the ver-

tical plane of the QuadFET has successfully been modeled. The incorporation of the DG MOSFETs solution was performed in a way that required an extraction from the numerical device simulator Atlas. However, the model with the extracted parameter, which leads to a scaling factor of $\lambda_{DG}/\lambda_{Quad}=\sqrt{1.8}$, shows great scalability for device thicknesses $S = \{20, 5\}$nm and gate lengths L=$\{50, 20\}$nm. Also with varying applied potential, $V_{ds} = \{0, 0.7\}$V and $V_{gs} = \{-0.3, 0.2\}$V, the model shows great correspondence with numerical simulations. Since the potential profile in the cut is not ideally parabolic, the biggest cause of error is the parabolic approximation. However, the results are acceptable even in the corners, and the potential in the center is generally very precise.

Chapter 5

Conclusion

In this thesis, the potential profiles in the cut planes perpendicular to the source-drain symmetry lines in the middle of nanoscale FinFET and QuadFET operated in subthreshold are endeavored to be modeled. These potential profiles are the most important ones for finding subthreshold current models for both devices in future work, and are one of the main reasons why they are modeled. All the results in this thesis are compared to the numerical device simulator Atlas from Silvaco.

Conformal mapping has been used to find an analytical solution with good scaling properties for the QuadFET, which agrees very well with numerical simulations. The incorporation of the DG MOSFETs solution was performed in a way that required an extraction from the numerical device simulator Atlas. However, the model with the extracted parameter, which leads to a scaling factor of $\lambda_{DG}/\lambda_{Quad}=\sqrt{1.8}$, shows great scalability.

The same has been attempted for the FinFET, only with a slightly different approach, without success. Due to neglecting the curvature in the source-drain direction above the ground plane of the device, the attempt of transforming the three dimensional problem to a two dimensional one, did not work. However, an attempt of modeling the transistor has been tested, and the electrostatics of the device is better known. A new approach of modeling the FinFET is already in progress by Fjeldly et al.

Chapter 6

Future work

A complete compact model must have procedures for calculating currents, capacitances and noise. In this thesis, the electrostatics in subthreshold region in the center vertical planes of FinFET and QuadFET have been considered. Only a small fraction related to compact modeling these nanoscale devices have been performed, and additional analysis are for this reason required including the ones discussed below.

6.1 Subthreshold potential model for FinFET

Since the modeling of the subthreshold potential in the cut plane perpendicular to the source-drain symmetry line in the middle of the FinFET failed in this thesis, it must be modeled in some other way. A method purposed by Fjeldly et al. is to solve the 3D Laplace equation

$$\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} + \frac{\partial^2 \varphi}{\partial z^2} = 0, \tag{6.1}$$

with the curvature in the z-direction modeled with an y-dependent quadratic function. The equation to solve thus becomes

$$\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} + f(y) = 0 \tag{6.2}$$

A difficult task however, is to find an analytical solution to this equation.

6.2 Modeling of other cut planes

Modeling of other vertical planes closer to source are important in order to get a good current model when a relatively large drain-source potential is applied. When V_{ds} increases, the DIBL-effect kicks in and makes the maximum potential in the vertical plane (or minimum potential along the source to drain symmetry line) move towards source and increase. The center vertical plane is then no longer the most favorable one to use for finding the subthreshold current.

6.3 Electrostatic modeling of threshold and strong-inversion

In order to get a complete compact model for all regimes of operation, the electrostatics of both the threshold and strong-inversion must be modeled. This is achieved using the length scaling transformation discussed in section 4.2

6.4 Drain current model

A current model is off course a very important part of compact modeling nanoscale devices. When establishing a compact model for the drain current, there are basically two main strategies. Firstly, the drift-diffusion model where the charge carriers experience a lot of collisions and scattering on its way through the body. Secondly, the ballistic transport model, where the gate length is so short that the carriers go through the body without significant scattering. Also an approach in between is possible with the quasi-ballistic transport model, which is a ballistic transport model with a statistical ballistic scattering constant which is included as a model parameter. The main advantages of using the drift-diffusion model are its simplicity and its easy recognition of processes.

6.5 Threshold voltage model

Creating a model for the threshold voltage is important, since it marks the onset of the transistor. Research groups have already performed threshold voltage modeling for the FinFET[16], but the QuadFET remains.

6.6 Capacitance modeling

In order to consider the speed of the FinFET and QuadFET, capacitance modeling are required. A capacitance model for the subthreshold regime of the QuadFET should not be to difficult to obtain. Electrostatics of the threshold and strong-inversion must be obtained before a capacitance model for these regimes of operation can be created.

6.7 Development of SPICE-type model

The analytical expressions for the subthreshold regime developed in this thesis can be used as a preprocessing routine where parameters are extracted from the analytical expressions, for instance the maximum potential in the center of the vertical plane, for use in parametrized compact models. These compact models are suitable for implementation in circuit simulators as SPICE. High computational speed and continuity in its derivatives with respect to applied biasing is necessary if the model is to be implemented in a SPICE simulator.

6.8 Noise

Noise modeling is also considered to be an important part of a compact model for nanoscale devices[3].

Bibliography

[1] H. Børli. *Modeling of drain current and intrinsic capacitances in nanoscale double-gate and gate-all-around MOSFETs.* PhD thesis, 2008.

[2] S. Kolberg. *Modeling of electrostatics and drain current in nanoscale double-gate MOSFETs.* PhD thesis, 2007.

[3] P. E. Allen and D. R. Holberg. *CMOS analog circuit design.* Oxford university press, 2002. 2. ed.

[4] A. Làzaro F. Danneville B. Iñiguez, T. A. Fjeldly and J. Deen. Compact modeling solutions for nanoscale double-gate and gate-all-around mosfets, 2006. Vol. 53, pp. 2128-2142.

[5] E. Nowak P. M. Solomon Y. Taur D. J. Frank, R. H. Dennard and P. W. Hon-Sum. *Device scaling limits of si mosfets and their application dependencies.* Proceedings of the IEEE, 2001. vol. 89, pp. 259-288.

[6] H. Shichman and D. A. Hodges. Modeling and simulation of insulated-gate field-effect transistor switching circuits, 1968. Vol. 3, no. 5, pp. 285-289.

[7] J. E. Meyer. Mos models and circuit simulation, 1971. Vol. 32, pp. 42-63.

[8] T. Ytterdal T. A. Fjeldly and M. Shur. *Introduction to device modeling and circuit simulation.* John Wiley and Sons, 1998.

[9] D. E. Ward and R. W. Dutton. A charge-oriented model for mos transistor capacitances, 1978. Vol. 13, no. 5, pp. 703-708.

[10] N. Aurora. *MOSFET modeling for VLSI circuit simulation: theory and practice.* Springer-Verlag, Wien, 1993.

[11] W. Liu. *MOSFET models for SPICE simulation, including BSIM3v3 and BSIM4.* John Wiley and Sons, 2001.

[12] A. Klös and A. Kostka. A new analytical method of solving 2d poisson's equation in mos devices applied to threshold voltage and subthreshold modeling, 1996. vol. 39, pp. 1761-1775.

[13] T. A. Fjeldly J. Østhaug and B. I niguez. Closed-form 2d modeling of sub-100nm mosfets in the subthreshold regime, 2004. vol. 1, pp. 70-79.

[14] E. Weber. *Mapping of fields.* New York: John Wiley and Sons, 1950. volume 1.

[15] Z. Yu D. Zhang and L. Tian. Compact modeling of 3d finfets.

[16] J.-H. Lee and B.-K. Choi. Threshold-voltage modeling of bulk finfets by considering charge-sharing and surface potenial, 2007. pp. 19-24.

[17] G. H. See S. Lin C. Wei G. Zhu, X. Zhou and J. Zhang. A unified compact model for finfet and silicon nanowire mosfets, 2009. Vol. 3, pp. 588-591.

[18] T. A. Fjeldly S. Kolberg and B. I niguez. Self-consistent 2d compact model for nanoscale double gate mosfets, 2006. vol. 3994, pp. 607-614.

[19] T. A. Fjeldly H. Børli, S. Kolberg. Precise modeling framework for short-channel double-gate and gate-all-around mosfets, 2008. vol. 55, pp. 2678-2686.

[20] M. Benachir J. Brini F. Balestra, S. Cristoloveanu and T. Elewa. Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance, 1987. vol. 8, no. 9, pp. 410-412.

[21] J-P. Colinge. *FinFETs and other multi-gate transistors.* Springer, 2008.

Appendix A

$\varphi(u, v)$ for DG MOSFET

The inter-electrode potential distribution of the DG MOSFET is derived by solving the Laplacian of the $u, v \in$W-plane (equation (3.23)).

By using

$$\int \frac{V}{(u-u')^2+v^2}du' = \frac{1}{v}\Big(tan^{-1}\Big(\frac{1-u}{v}\Big) + tan^{-1}\Big(\frac{1+u}{v}\Big)\Big), \tag{A.1}$$

where V is a constant potential, and applying the correct boundary conditions for the DG MOSFET as specified in chapter 3.6, the resulting solution of the Laplacian becomes

$$\begin{aligned}\varphi(u,v) =& \frac{1}{\pi}\Bigg\{\pi(V_{gs}-V_{FB}) + (V_{bi}+V_{FB}-V_{gs})tan^{-1}\Big(\frac{1-ku}{kv}\Big) \\ &+ (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\Big(\frac{1+ku}{kv}\Big) \\ &- (V_{bi}+V_{FB}-V_{gs})tan^{-1}\Big(\frac{1-u}{v}\Big) \\ &- (V_{bi}+V_{ds}+V_{FB}-V_{gs})tan^{-1}\Big(\frac{1+u}{v}\Big)\Bigg\}\end{aligned} \tag{A.2}$$

Appendix B

Approximation for $F^2(k,u)$

The purposed approximation of $F^2(k,u)$ has the form

$$F^2(k,u) \approx C + D\sqrt{1-u^2} + Eu^2 \tag{B.1}$$

Applying the boundaries for the region this approximation is used for, gives

$$\begin{aligned}
u \to \pm 1 \qquad & C + E = F^2(k, u = \pm 1) = K^2(k) \\
u \to 0 \qquad & C + D = 0 \\
u \to 0 \qquad & -\frac{D}{2} + E = 1 \\
u \to 0 \qquad & \frac{d^2}{du^2}(C + D\sqrt{1-u^2} + Eu^2) = -D + 2E = 2
\end{aligned} \tag{B.2}$$

Rearranging results in

$$D = 2(1 - K^2(k)) \tag{B.3}$$

$$E = D + K^2(k) = 2 - K^2(k) \tag{B.4}$$

$$C = -D = -2(1 - K^2(k)) \tag{B.5}$$

The approximtaion for $F^2(k,u)$ then becomes

$$F^2(k,u) \approx 2(K^2(k) - 1) - 2(K^2(k) - 1)\sqrt{1-u^2} + (2 - K^2(k))u^2 \tag{B.6}$$

Figure 4.18 shows the good agreement between the approximation and the exact function.

Appendix C

Deriving $\varphi(u,v)$ for the FinFET

The inter-electrode potential distribution of the FinFET in the $u,v \in$W-plane is derived by solving equation (3.23):

$$\begin{aligned}\varphi(u,v) =& \frac{v}{\pi}\int_{-\infty}^{\infty}\frac{\varphi(u')}{(u-u')^2+v^2}du' \\ &= \frac{v}{\pi}\Bigg[\int_{-\infty}^{-1}\frac{V_{gs}-V_{FB}}{(u-u')^2+v^2}du' \\ &+ \int_{-1}^{1}\frac{\varphi_c\big(1-(F(k,u)/K(k))^2\big)+V_{gs}-V_{FB}}{(u-u')^2+v^2}du' \\ &+ \int_{1}^{\infty}\frac{V_{gs}-V_{FB}}{(u-u')^2+v^2}du'\Bigg]\end{aligned} \tag{C.1}$$

Inserting the approximation in equation (4.14) for $F^2(k,u)$, the integral from u=-1 to u=1 of $D\sqrt{1-u^2}$ becomes the difficult part. It is solved in the following way:

$$\begin{aligned}&\int_{-1}^{1}\frac{\sqrt{1-u^2}}{((u-u')^2+v^2)}du' \\ &= \frac{-ju^2+2uv+j(1+v^2)}{2v\sqrt{1-u^2-2juv+v^2}}ln\bigg(\frac{2jv}{(1-u^2-2juv+v^2)^{3/2}}\bigg)-\frac{\pi}{2} \\ &- \frac{j}{2v}\sqrt{1-u^2+2juv+v^2}ln\bigg(-\frac{2jv}{(1-u^2+2juv+v^2)^{3/2}}\bigg) \\ &- \frac{-ju^2+2uv+j(1+v^2)}{2v\sqrt{1-u^2-2juv+v^2}}ln\bigg(-\frac{2jv}{(1-u^2-2juv+v^2)^{3/2}}\bigg)-\frac{\pi}{2} \\ &+ \frac{j}{2v}\sqrt{1-u^2+2juv+v^2}ln\bigg(\frac{2jv}{(1-u^2+2juv+v^2)^{3/2}}\bigg)\end{aligned} \tag{C.2}$$

$$= -\pi + \frac{-ju^2 + 2uv + j(1+v^2)}{2v\sqrt{1-u^2-2juv+v^2}}\left(ln\left(\frac{2jv}{(1-u^2-2juv+v^2)^{3/2}}\right) - ln\left(-\frac{2jv}{(1-u^2-2juv+v^2)^{3/2}}\right)\right)$$
$$+ \frac{j}{2v}\sqrt{1-u^2+2juv+v^2}\left(ln\left(\frac{2jv}{(1-u^2+2juv+v^2)^{3/2}}\right) - ln\left(-\frac{2jv}{(1-u^2+2juv+v^2)^{3/2}}\right)\right) \tag{C.3}$$

Since $ln(1) - ln(-1) = -j\pi$,

$$\int_{-1}^{1} \frac{\sqrt{1-u^2}}{((u-u')^2+v^2)}du' = -\pi + \frac{\pi}{2v}\left(\frac{-u^2-2juv+1+v^2}{\sqrt{1-u^2-2juv+v^2}} + \frac{\pi}{2v}\sqrt{1-u^2+2juv+v^2}\right) \tag{C.4}$$

and using $x + jy = |z|exp[j\phi]$, $x - jy = |z|exp[-j\phi]$, $z = \sqrt{x^2+y^2}$ and $tan(\phi) = |y/x|$,

$$\begin{aligned}\int_{-1}^{1} \frac{\sqrt{1-u^2}}{((u-u')^2+v^2)}du' =& -\pi + \frac{\pi}{2v}\left(\sqrt{\sqrt{(1+v^2-u^2)^2+(2uv)^2}exp[-j\phi]}\right.\\ &\left.+\sqrt{\sqrt{(1+v^2-u^2)^2+(2uv)^2}exp[j\phi]}\right)\\ =& -\pi + \frac{\pi}{2v}\left((1+v^2-u^2)^2+(2uv)^2\right)^{1/4}(exp[-\frac{j\phi}{2}]+exp[-\frac{j\phi}{2}])\\ =& -\pi + \frac{\pi}{v}\left((1+v^2-u^2)^2+(2uv)^2\right)^{1/4}cos\left(\frac{\phi}{2}\right)\end{aligned} \tag{C.5}$$

where

$$\phi = tan^{-1}(\left|\frac{2uv}{1+v^2-u2}\right|) \tag{C.6}$$

Using

$$cos(x) = \frac{1}{\pm\sqrt{1+tan^2(x)}} \tag{C.7}$$

result in

$$\int_{-1}^{1} \frac{\sqrt{1-u^2}}{((u-u')^2+v^2)}du' = \pi + \frac{\pi}{v}\left[(1+v^2-u^2)+(2uv)^2\right]^{\frac{1}{4}}\sqrt{\frac{1}{2}\left(\sqrt{\frac{(1+v^2-u^2)^2}{(1+v^2-u^2)^2+(2uv)^2}}+1\right)} \tag{C.8}$$

The complete expression for the inter-electrode potential distribution in the $u, v \in$W-plane then becomes

$$\varphi(u,v) = (V_{gs}-V_{FB}) + \frac{\varphi_c}{\pi}\left(tan^{-1}\left(\frac{1-u}{v}\right)+tan^{-1}\left(\frac{1+u}{v}\right)\right) - \frac{v\varphi_c}{\pi K^2(k)}\int_{-1}^{1}\frac{F^2(k,u')}{(u-u')^2+v^2}du', \tag{C.9}$$

where

$$\int_{-1}^{1}\frac{F^2(k,u)}{(u-u')^2+v^2}=\int_{-1}^{1}\frac{C+D\sqrt{1-u^2}+Eu^2}{(u-u')^2+v^2}$$
$$=-\frac{2(1-K^2(k))}{v}\Big(tan^{-1}\Big(\frac{1-u}{v}\Big)+tan^{-1}\Big(\frac{1+u}{v}\Big)\Big)$$
$$+2(1-K^2(k))\Bigg(\pi+\frac{\pi}{v}\Big[(1+v^2-u^2)+(2uv)^2\Big]^{\frac{1}{4}}\sqrt{\frac{1}{2}\Bigg(\sqrt{\frac{(1+v^2-u^2)^2}{(1+v^2-u^2)^2+(2uv)^2}}+1\Bigg)}\Bigg)$$
$$+(2-K^2(k))\Bigg(2+\frac{u^2-v^2}{v}\Big(tan^{-1}\Big(\frac{1-u}{v}\Big)+tan^{-1}\Big(\frac{1+u}{v}\Big)\Big)+uln\Big(\frac{1-2u+u^2+v^2}{1+2u+u^2+v^2}\Big)\Bigg) \tag{C.10}$$

Appendix D

Oxide correction

The body potential of both the DG MOSFET and the QuadFET (cut along source-drain symmetry line) in subthreshold is located by solving the solution to the laplacian in the $u, v \in$W-plane[2]

$$\varphi(u,v) = \frac{v}{\pi}\int_{-\infty}^{\infty} \frac{\varphi(u')}{(u-u')^2+v^2}du' \tag{D.1}$$

By using the boundary conditions of the bodies, disregarding the different values of k the two devices have,

$$\begin{aligned}
&\varphi_{-\infty\leq u\leq -1/k+\Delta u_2} = V_{gs} - V_{FB}\\
&\varphi_{-1/k+\Delta u_2\leq u\leq -1-\Delta u_1} = V_{bi}\\
&\varphi_{-1-\Delta u_1\leq u\leq 1+\Delta u_1} = V_{gs} - V_{FB}\\
&\varphi_{1+\Delta u_1\leq u\leq 1/k-\Delta u_2} = V_{bi} + V_{ds}\\
&\varphi_{1/k-\Delta u_2\leq u\leq \infty} = V_{gs} - V_{FB}
\end{aligned} \tag{D.2}$$

in the integral (D.1), gives

$$\begin{aligned}
\varphi(u,v) =& \frac{v}{\pi}\Bigg[\int_{-\infty}^{-1/k+\Delta u_2} \frac{V_{gs}-V_{FB}}{(u-u')^2+v^2}du'\\
&+\int_{-1/k+\Delta u_2}^{-1-\Delta u_1} \frac{V_{bi}}{(u-u')^2+v^2}du'\\
&+\int_{-1-\Delta u_1}^{1+\Delta u_1} \frac{V_{gs}-V_{FB}}{(u-u')^2+v^2}du'\\
&+\int_{1+\Delta u_1}^{1/k-\Delta u_2} \frac{V_{bi}+V_{ds}}{(u-u')^2+v^2}du'\\
&+\int_{1/k-\Delta u_2}^{\infty} \frac{V_{gs}-V_{FB}}{(u-u')^2+v^2}du'\Bigg]
\end{aligned} \tag{D.3}$$

Here u_{ox1} and u_{ox2} is the Schwarz-Christoffel transformation of the oxide gaps from the (x,y)-plane to the (u,iv)-plane. Solving the integrals and rearranging, results in

$$\begin{aligned}\varphi(u,v) =& \frac{1}{\pi}\Bigg\{ V_{bi}\left(tan^{-1}\left(\frac{1/k-\Delta u_2-u}{v}\right)-tan^{-1}\left(\frac{1+\Delta u_1-u}{v}\right)\right)\\ &+(V_{gs}-V_{FB})\left(tan^{-1}\left(\frac{1+\Delta u_1-u}{v}\right)+tan^{-1}\left(\frac{1+\Delta u_1+u}{v}\right)\right)\\ &+(V_{gs}-V_{FB})\left(\pi-tan^{-1}\left(\frac{1/k-\Delta u_2+u}{v}\right)-tan^{-1}\left(\frac{1/k-\Delta u_2-u}{v}\right)\right)\\ &+(V_{bi}+V_{ds})\left(tan^{-1}\left(\frac{1/k-\Delta u_2+u}{v}\right)-tan^{-1}\left(\frac{1+\Delta u_1+u}{v}\right)\right)\end{aligned} \tag{D.4}$$

When changing any geometric constants of the transistors, it is important to remember that not only the modulus k is changed, but also Δu_1 and Δu_2.