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Design of a high IIP2 2.4GHz RF Front-end

Thomas Eliassen

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Supervisor: Jukka Tapio Typpø, IET
Co-supervisor: Oddgeir Fikstvedt, Micrel Norway AS

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Problem Description

A receiver's linearity is an important parameter. IIP2 and IIP3 are parameters that describe a receiver's ability to suppress second- and third-order intermodulation products. In a heterodyne receiver usually only odd-order intermodulation will cause problems. In a homodyne or direct-conversion receiver also second-order intermodulation will cause problems.

In the project assignment second-order intermodulation and circuit architectures /topologies with high IIP2 suitable for use in a direct-conversion receiver were studied, as well as ways to cancel second-order intermodulation products.

Based on the project assignment, the student is to design a high IIP2 2.4GHz RF front-end (LNA and IQ mixers) in 0.18 micron CMOS technology suitable for use in a direct-conversion receiver. The front-end can be differential or single-ended. It is an advantage if the front-end has 50 ohm input impedance, but this is not an absolute requirement.

The specifications are as follows:

Frequency:	2.4GHz
IIP2:	30dBm
DSB NF @ 1MHz:	4dB
IIP3:	-20dBm
Current consumption:	3mA

The current consumption is the least important specification, and can be increased if necessary to reach the other specifications.

Assignment given: 16. January 2006
Supervisor: Jukka Tapio Typpø, IET

Abstract

This master thesis presents the design of a high IIP2 direct-conversion receiver front-end, consisting of a LNA and I- and Q-channel mixers. The front-end is implemented in a 0.18 μm technology with 1.8 V supply voltage. Problems that are especially severe for direct-conversion receivers are presented; 1/f-noise, DC offset, and second-order nonlinearity, with particular attention to the latter. Methods to improve the IIP2 are presented and explored in the design of the front-end. The complete front-end has -19.7 dBm IIP3, 4 dB noise figure, and consume 7.4 mA of current from a 1.8 V supply. Through mixer load tuning an IIP2 of more than +48 dBm is achieved for the front-end.

Acknowledgements

My thanks goes to my supervisor Oddgeir Fikstvedt, Jukka Typpö, and Trond Ytterdal for their help.

Thomas Eliassen
July 10, 2006

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Chapter 1

Introduction

The well established superheterodyne receiver has for a long time been the standard receiver architecture of choice due to high selectivity, sensitivity, and the many inherent problems with discrete implementations of direct-conversion receivers. As the demands for integration have increased the direct-conversion receiver has gotten new attention, as it allows for small, cheap, low power receivers. Many of the effects that makes discrete realizations of direct-conversion receivers difficult can be controlled or suppressed in integrated solutions [1, 15]. However, 1/f-noise, DC offset, and second-order intermodulation still require special attention when designing integrated direct-conversion receivers.

This paper presents a design of a front-end suitable for use in a direct-conversion receiver. The front-end consists of a low-noise amplifier and I- and Q-channel mixers. The specifications are given by table 1.1. The current consumption can be increased if necessary to reach the other requirements. It is an advantage if the front-end has $50\,\Omega$ input impedance, but this is not an absolute requirement.

A short introduction to the direct-conversion receiver will be given in this chapter, and the issues that are problematic for direct-conversion receivers in particular will be presented. For basic background theory on linearity, noise, LNA, and mixer the reader is referred to [11] and [16].

Parameter	Value	Unit
Frequency	2.4	GHz
IIP2	30	dBm
IIP3	-20	dBm
DSB NF @ 1MHz	4	dB
Current consumption	3	mA

Table 1.1: Front-end specifications

1.1 Direct-conversion receiver

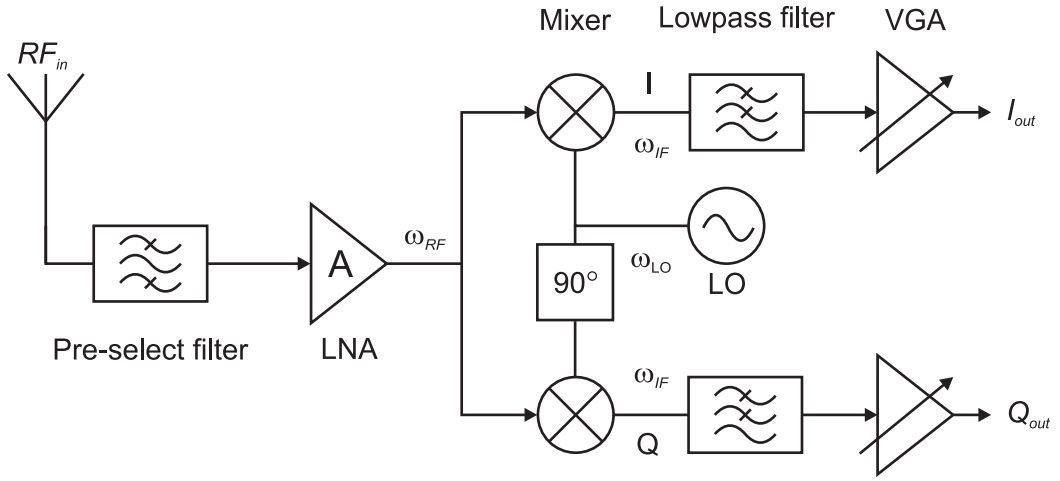


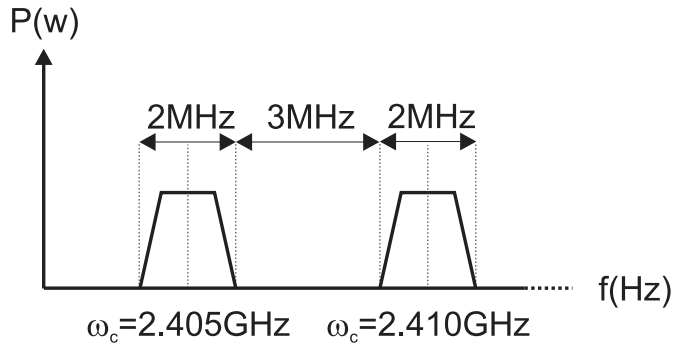
Figure 1.1: Direct-conversion receiver

A direct-conversion receiver is shown in figure 1.1. The antenna transforms a propagated electromagnetic wave to a RF-signal RF_{in}, and feeds it to a bandpass pre-select filter.

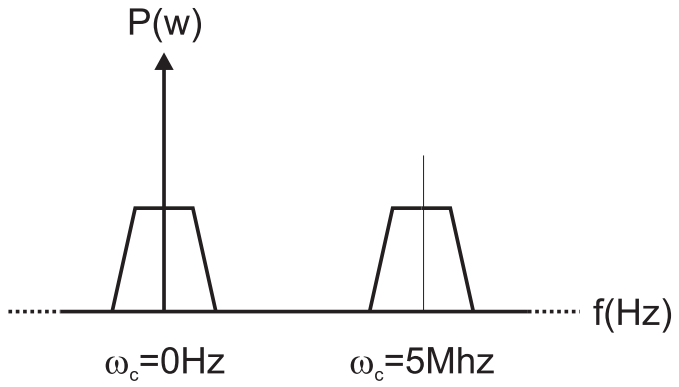
Strong out-of-band interferers could cause the receiver to saturate, and the purpose of the pre-select filter is to reject such interferers. The passband of the filter is set to the tuning range of the receiver. The pre-select filter needs to have a very low noise figure and insertion loss, as it is placed directly after the antenna and therefore will have great influence on the total noise figure of the receiver.

The signal is then amplified by the low-noise amplifier (LNA). The purpose of the LNA is to amplify the weak RF-signal while adding a minimum of noise. It is therefore designed with a minimum of passive components.

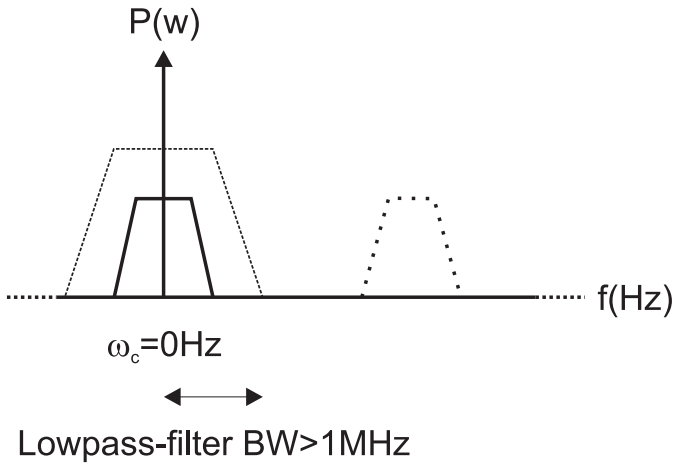
The output of the LNA is split to the I- and Q-channel mixers. The purpose of a mixer is to down-convert the signal from RF-frequency ω_{RF} to intermediate frequency ω_{IF}. The mixer functions as a multiplicator that multiplies ω_{RF} with the local-oscillator (LO) frequency ω_{LO}, generating products at sum and difference of the inputs. In a direct conversion receiver ω_{LO} is tuned to the desired channel, for instance the *Zigbee* channel with center frequency 2.405 GHz shown in 1.2a. In the 802.15.4/ZigBee standard, the 2.4 GHZ unlicensed band that spans from 2.4 GHz-2.483 GHz is split into 16 channels of 2 MHz bandwidth with 3 MHz spacing between each channel. The adjacent channel has center frequency 2.410 GHz. The multiplication in the mixer produces output frequencies at the sum and difference of the RF- and LO-frequencies. Thus, the desired channel is down-converted to 0 Hz center frequency (baseband), and the adjacent channel is down-converted to 5 MHz center frequency, as shown in figure 1.2b. The low-pass filter following the mixer performs the channel selection, and removes the adjacent channel and the sum components, see figure 1.2c. The separate I (In phase) and Q (Quadrature)



(a) Desired and adjacent channels after LNA



(b) Down-converted channels



(c) Low-pass filtering of down-converted spectrum

Figure 1.2: Direct conversion

paths are necessary in order to demodulate OFDM and O-QPSK signals. The LO signal fed to the Q-channel mixer is passed through a 90° frequency independent phase-shifter, generating quadrature between the upper path I and the lower path Q.

The variable gain amplifier (VGA) following the channel select filter is part of the automatic gain control (AGC) of the front-end. The purpose of the VGA and AGC is to fit the dynamic range of the signal coming from the previous stages to the dynamic range required by the baseband component following the VGA, typically an AD-converter. A front-end gain of 60 dB may be required for low power input signals to the antenna, while only 20-30 dB for high power input signals. The VGA gain may therefore be on the order of 20 dB to 60 dB, depending on the gain or loss of components preceding the VGA [14].

1.2 Problems with direct-conversion

The direct-conversion receiver is faced with several problems that can severely deteriorate its performance; 1/f-noise, DC offset, and second-order intermodulation.

1.2.1 1/f-noise

The spectral density of 1/f-noise (flicker noise) will, as suggested by its name, increase with decreasing frequency. Since the baseband consists of frequencies down toward DC, and the corner frequency can be as high as 1 MHz in a CMOS technology, low 1/f-noise is important for a direct-conversion receiver. The switches of the mixer will be the most important contributor, as 1/f-noise in the transconductor will get up-converted.

The origin of 1/f-noise is obscure, but it is most prevalent in components sensitive to surface phenomena; MOSFET technology is more affected than BJT technology [11].

Mean-square 1/f drain current for a MOSFET, is given by [11]

$$\overline{i_n^2} = \frac{K}{f}\frac{g_m^2}{WLC_{ox}^2}\Delta f \approx \frac{K}{f}\omega_T^2 A\Delta f, \tag{1.1}$$

where $A = WL$ is the area of the gate and K is an empirical constant for the component. It is seen that for a certain transconductance g_m, a large gate area and a thin dielectric layer t_{ox}, results in low 1/f-noise. K for a NMOS transistor is typically 50 times larger than for a PMOS [11].

1.2.2 DC offset

Large DC offsets can dominate over small input signals, cause overload of the baseband stages, and reduce the dynamic range of the receiver. It is caused by LO self-mixing and reradiation, device nonlinearities, and mismatch. DC offsets can be categorized as dynamic if it varies with time, or static if constant.

LO self-mixing occurs when the LO signal is mixed with itself due to leakage between the LO and RF port of the mixer, figure 1.3. This causes a static DC offset.

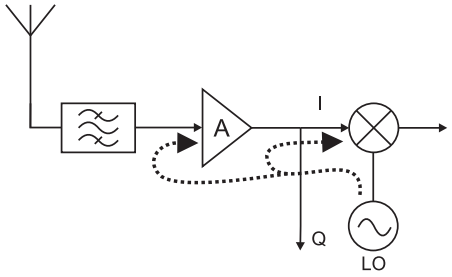


Figure 1.3: LO-RF leakage

Direct-conversion receivers are particularly prone to LO reradiation. The LO frequency is within the passband of the pre-select filter and LNA. When the receiver is active the finite reverse isolation of the receiver causes the LO energy to be radiated out through the antenna. The radiated LO can reflect off of objects in close proximity, and be reabsorbed by the receiver, see figure 1.4. This will cause a dynamic DC offset, as the magnitude depends on the placement and surroundings of the receiver. The radiated LO could also interfere with other receivers operating in the same band [1].

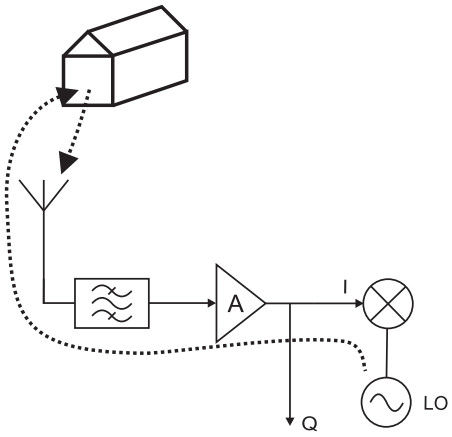


Figure 1.4: LO reradiation

DC offsets can be dealt with in a number of ways. AC coupling can be utilized if the wanted signal has little energy near DC. If the modulation uses Time Division Multiple Access (TDMA), the inactive time can be used to evaluate and remove the DC offset. LNA and mixer architectures with good port-to-port isolation and good layout of the circuit will help to reduce self-mixing and reradiation.

1.2.3 Second-order nonlinearity

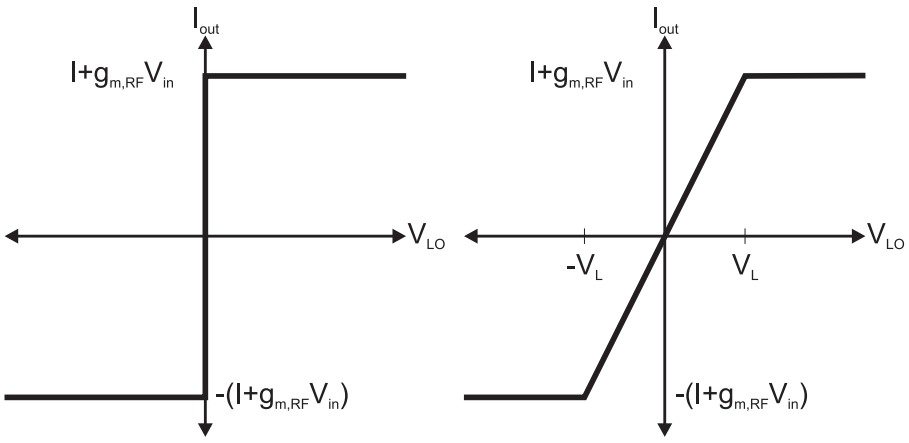
Second-order non-linearity in a receiver causes DC offset and frequency components at double the input frequencies. When the desired signal is accompanied by an interferer, intermodulation products at sum and difference of these two signals will be generated in addition to the DC offset. The difference component can be particularly damaging to a direct-conversion receiver, as it can interfere with the channel down-converted to baseband.

The main causes of second-order distortion are RF self-mixing, and device nonlinearity and mismatches [12]. These phenomena, and ways to improve second-order distortion performance, are discussed further in chapter 2.

Chapter 2

Second-order nonlinearity

2.1 RF self-mixing



(a) Hard switching (b) Soft switching

Figure 2.1: Hard and soft switching

RF self-mixing is similar to LO self-mixing, in that the respective signals are mixed with themselves. LO self-mixing causes a DC offset, while the RF self-mixing is experienced as a second-order nonlinearity.

Ideally the switches in a mixer should exhibit a hard-switching behavior, where only one switch is conducting at any given time. For a square-wave LO-signal this would be the case, as shown in figure 2.1a. In practice the LO-signal is a sine-wave, and both switches conduct when the LO has a value between $+V_L$ and $-V_L$, as shown in figure 2.1b [12].

It is shown in [12] that when the LO voltage is larger than $|V_L|$ the output current in the mixer

is given by the sum of the bias current and the RF signal current. However, when both switches conduct simultaneously, that is when the LO voltage is less than $|V_L|$, the output current from the switches is also dependent on the RF input voltage and the LO voltage. The output currents dependence on the LO voltage is linear, while the dependence on RF input voltage is square. Thus, second-order distortion occurs.

Results presented in [12] show that the IIP2 due to self-mixing is dependent on the RF-LO leakage and LO power, and to a first-order independent of any design-parameters. Thus, maximizing LO power and minimizing RF-LO leakage will maximize IIP2 when considering RF self-mixing.

2.2 Transconductor non-linearity and switch mismatch

The I-V relationship of the MOSFET transistor is inherently nonlinear, and the drain current will contain second-order components. The transconductor stage of the mixer will produce both a differential and a common-mode second-order intermodulation current [12]. The frequency conversion is performed by the switching stage. Considering a double-balanced mixer, ideally the low frequency differential intermodulation current from the transconductor reaching the switching stage will be upconverted to around the LO frequency and the common-mode current will get canceled due to the differential architecture. However, mismatches in the switching pairs will cause the dutycycle of the LO to deviate from 50%, and the intermodulation current from the transconductor will leak to the output of the mixer. The mismatch in a nominally identical transistor pair, i.e. the switches in the mixer, occur due to microscopic random variations in device dimensions, gate and channel doping levels, and oxide thickness. These effects cause variations in $\beta(\mu C_{ox}\frac{W}{L})$ and threshold voltage between the devices, leading to transconductance mismatch and DC offset.

2.3 Parasitic capacitance at common source node of mixer switches

The parasitic capacitance loading the common source node of the mixer switches has a deteriorating effect on the mixer IIP2, and will limit the maximum achievable mixer IIP2. A thorough and complex analysis of the mechanism is given in [12]. Basically, second-order intermodulation products are generated at the output due to mismatch and non-linearity in the switch pairs, which when subject to an interfering signal superimposed on the bias current generate second-order sidebands around the odd harmonics of the LO voltage spectrum at the common source node. The voltage spectrum at this node will generate an intermodulation current in the parasitic capacitance, which in turn is down-converted to baseband as second-order intermodulation products [3]. Minimizing the parasitic capacitance at the common source node will reduce this effect.

2.4 Techniques for IIP2 improvement

Multiple techniques for improvement of the second-order distortion performance have been published [2, 6, 4, 7, 20]. Although all of these have merit, the techniques presented in [7] and [20] are both easy to implement and offer good IIP2 performance. These are introduced here and further explored in the front-end design, chapter 3.

2.4.1 Load tuning

In [7] a technique is presented that uses load tuning to increase mixer IIP2. Through the use of this method the authors have achieved more than 20 dB increase in IIP2.

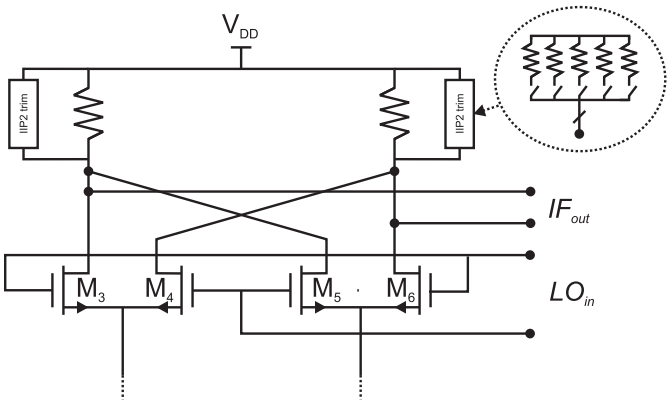


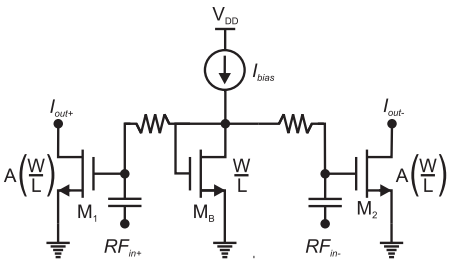
Figure 2.2: Mixer switches with IIP2 trim blocks

The idea is that a controlled imbalance in the load resistors of the mixer can compensate for imbalance due to mismatch between the transistors in the switch pairs, as well as mismatch in the load resistors themselves. Mismatch in the transconductor can not be corrected as it will affect both sides of the mixer equally due to the cross-coupling in the mixer. The tuning is implemented as illustrated in figure 2.2. The blocks “IIP2 Trim” are essentially controllable resistances in parallel with the regular mixer load. The blocks consist of a number of binary weighted resistors composed from unit-sized resistors with value equal to the regular mixer load. The resistance of the IIP2 trim blocks can be controlled by a digital signal. More resistors switched in will decrease the resistance of the total mixer load. The size of the resistors and resolution of the tuning is determined through simulations, taking process tolerances into consideration. The amount of controlled imbalance is so small that it does not affect the IIP3, noise, or gain.

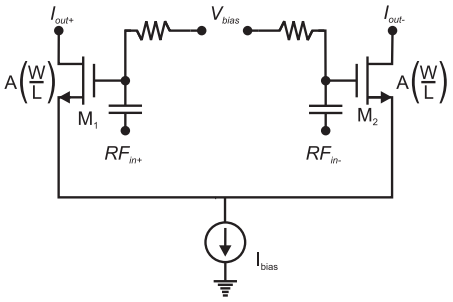
2.4.2 High IIP2 common-source transconductor

There are several transconductors to choose from for use as the input transconductor of the mixer. In [20] a comparison is conducted between the common-source, the differential, and a

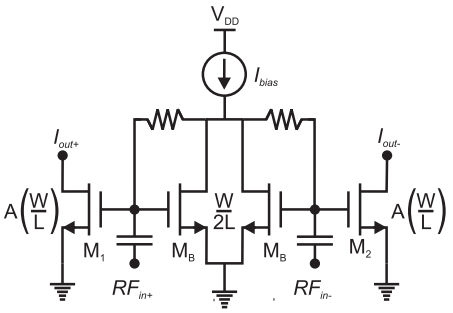
common-source transconductor with biasing proposed in that same article. The transconductors are shown in figure 2.3 .



(a) Common-source transconductor



(b) Differential pair transconductor



(c) Proposed common-source transconductor

Figure 2.3: Common-source, differential pair, and common-source with biasing scheme presented in [20]

The three transconductors have been compared with regards to single-ended IIP2 and IIP3 with varying drain-current. The results show that the common-source transconductor has the highest IIP3 for a given current-consumption, and that the proposed transconductor has slightly better IIP3 performance than the differential pair. Also, the two transistors stacked in the differential pair consume more voltage headroom compared to the common-source type transconductors where only one transistor consume headroom. When used in a mixer, all the transconductors will satisfy typical IIP3 requirements as they all have IIP3 between +5..+15 dBm. Linearization with regards to IIP3 can also always be performed by increasing the overdrive voltage or

increasing the drain current of the input device. When considering the IIP2 of the transconductors, both the proposed transconductor and the differential pair transconductor show much better performance than the regular common-source. It is also shown that the proposed transconductor provides a more stable current for large input signals, compared to the regular common-source transconductor.

Chapter 3

Front-end design

3.1 Choice of topologies

3.1.1 LNA

The LNA-topology must be highly linear, have high reverse isolation, contribute little noise, and have an input that can be matched to the 50 Ω antenna.

In [19] several LNA-topologies have been investigated; the resistively terminated, the $1/g_m$ terminated (common-gate), the shunt-series feedback, and the inductively degenerated. It is concluded that the inductively degenerated topology has the best noise figure of any of the architectures and is quite easily matched to 50 Ω. Matching through inductive degeneration will only create a narrow-band match, but it will be sufficient for the 2.4-2.483 GHz band.

The narrow bandwidth allows for the use of a tuned load; an inductor set to resonate with the total capacitance at the output node. This will increase the in-band gain and suppress out-of-band interferers.

A cascoded version of the inductively degenerated transistor will help to reduce the Miller-effect on the gate-drain capacitance and the interaction of the tuned output with the tuned input [11].

The linearity of the inductively source-degenerated cascode is typically greater than -5 dBm if noise and matching requirements are met. This makes the linearity of the subsequent stages the limiting factor for the front-end linearity [17].

A differential architecture will, as earlier stated, have good rejection of common-mode interferers. Also, second-order products generated by non-linearities will get canceled if the differential LNA is perfectly balanced.

From the reasons stated above, the differential inductively source-degenerated cascode LNA with tuned load is the architecture of choice in this paper, figure 3.1.

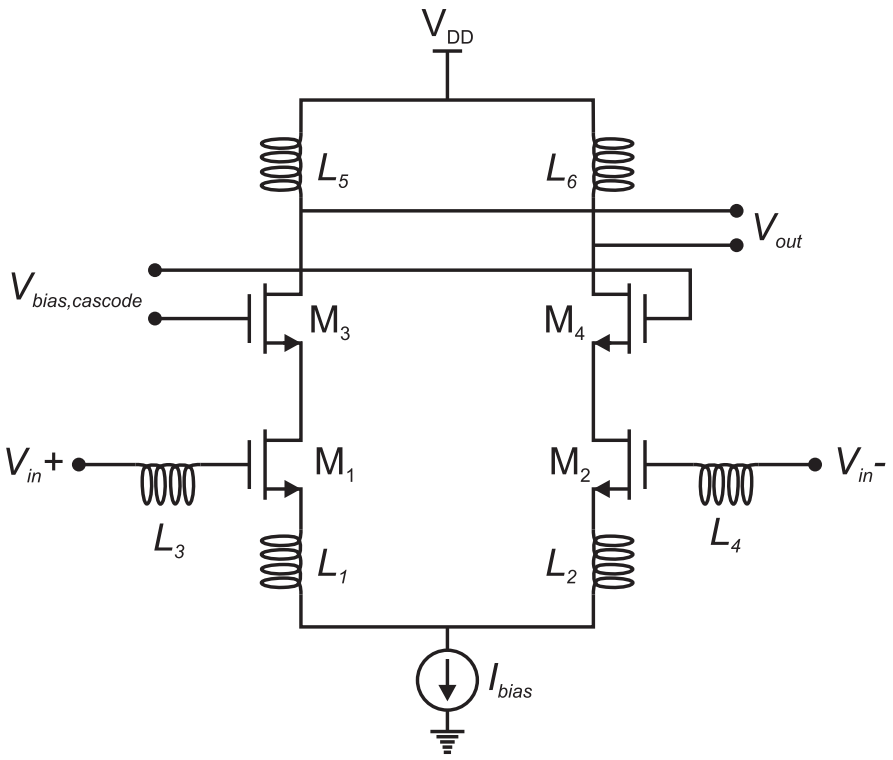


Figure 3.1: Proposed LNA architecture

3.1.2 Mixer

The active double-balanced Gilbert-cell mixer is the obvious architecture choice, not only because of the differential output from the LNA. The differential architecture is immune to second-order distortion when perfectly balanced. Also, the port-to-port isolation is excellent, thereby reducing the effect of self-mixing. The gain of the active mixer makes it favorable as it will reduce the effect of noise in the baseband stages following the mixer.

Considering the good second- and third-order distortion performance of the transconductor presented in [20], the double-balanced mixer with this transconductor is the mixer architecture of choice in this design. The architecture is shown in figure 3.2. Gate bias for the switches have been omitted in the figure.

3.2 The front-end

With the choice of topologies made in the previous section, the front-end designed here is illustrated in figure 3.3. The LNA receives a differential signal from the antenna, and drives the two mixers. The mixers receive a differential input from the LNA, and drive 3 pF loads which repre-

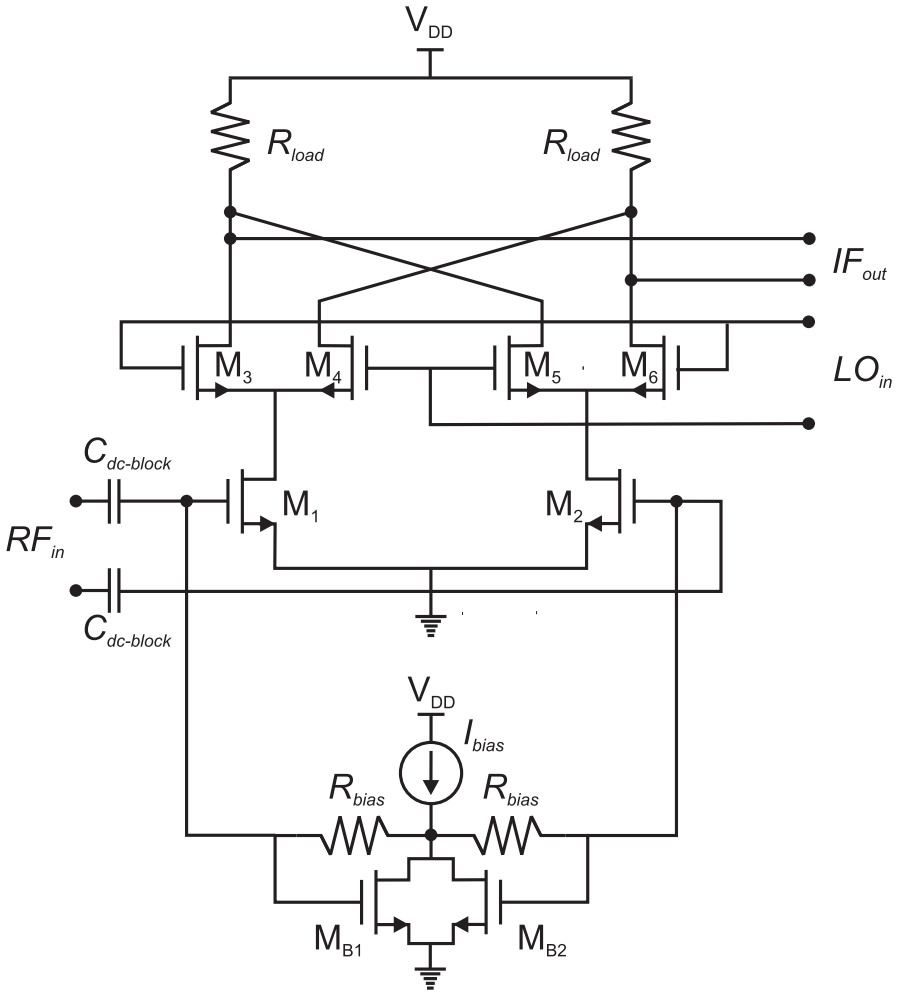


Figure 3.2: Proposed mixer architecture

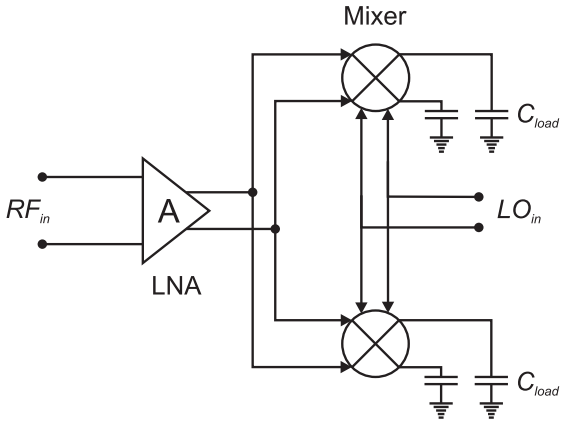


Figure 3.3: Front-end implemented

sent the capacitive inputs of the VGA. The 90° phase-shift of the LO-signal is not implemented, as the lower path mixer will only function as a dummy load to the LNA. All measurements and simulations made in this paper are performed on the upper path mixer.

3.2.1 System noise figure and linearity

For a system of cascaded components the well known Friis' equation gives the total noise factor of the system as [11]

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{\prod_{n=1}^{N-1} G_n}, \tag{3.1}$$

where F_n and G_n is the n-th components noise factor and gain, and N is the number of cascaded components.

The worst case, that is if all intermodulation products add in phase, input referred third-order intercept point for a cascaded system is given by [11]

$$\frac{1}{IIP3_{total}^2} = \frac{1}{IIP3_1^2} + \frac{G_1^2}{IIP3_2^2} + ... + \frac{\prod G_n^2}{IIP3_n^2}, \tag{3.2}$$

where $IIP3_n$ is in volts and G_n is the voltage gain.

From the above equations some useful insights can be made with regards to front-end noise and linearity. Equation (3.1) shows that for the cascaded system consisting of LNA and mixer, the total noise factor will be dominated by the noise contribution of the LNA and that the LNA gain will reduce the noise contribution of the mixer to the total noise factor. However, equation (3.2) shows that the mixer will need an increasingly higher third-order intercept point as the gain of the LNA is increased in order to keep the intercept point of the front-end constant, and that the LNA must have an IIP3 larger than the total front-end IIP3.

A too large mixer conversion gain can reduce the dynamic range and linearity of the mixer, and if the LNA gain is large as well, cause the stages following the mixer to overdrive. On the other hand, a too low conversion gain, or even conversion loss, will make the influence of noise from subsequent stages higher.

3.2.2 Package

A microchip fabricated on a silicon-wafer must have a *package*. The package has got several purposes. The pins on the package are connected to the pads on the chip through bondwire. Through the pins the chip can be supplied with ground and power, and external stimuli can be applied. The package also transports heat away from the chip and gives protection against environmental hazards like dust etc. When designing a chip the effects of the package must be taken into account as it can influence the LNA's input match and cause variations on the supply and ground nodes of the chip.

The package model used in this design is shown in figure 3.4.

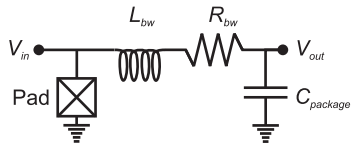


Figure 3.4: Package model

The pad is modeled in the process, and is capacitive. L_{bw} and R_{bw} models the inductance and loss of the bondwire. L_{bw} is an ideal 1 nH inductor and R_{bw} is a resistor of 2 Ω. The package capacitance $C_{package}$ has a value of 0.2 fF.

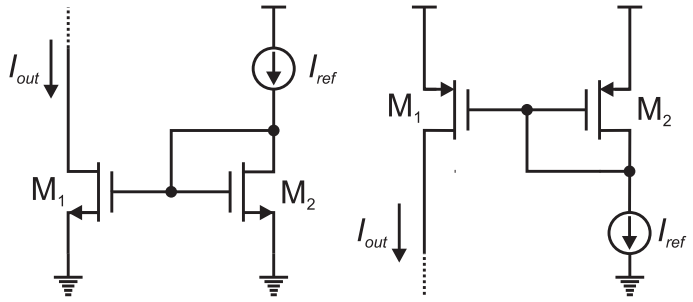
3.2.3 Bias

The master bias source used in the design is a 25 μA ideal current source, and all bias currents and voltages are derived from this single source.

Current sources and sinks

Current sources and sinks used in this design are simple current-mirrors. A NMOS mirror generates a current sink, figure 3.5a, while a PMOS mirror generates a current source, figure 3.5b.

The functionality of the mirrors is as follows, and is valid for both the current sink and source: The transistor M_2 is diode-connected; the gate and drain is the same node. M_2 has got a drain current I_{ref}, and the diode connection gives



(a) Current sink (b) Current source

Figure 3.5: Current-mirrors

$$V_{ds,M2} = V_{gs,M2} = V_{gs,M1}. \tag{3.3}$$

Assuming equal threshold voltage and lengths of both M_1 and M_2 and operation in the saturation region, since $V_{gs,M1} = V_{gs,M2}$ the relation between I_{ref} and I_{out} is given as

$$\frac{I_{ref}}{I_{out}} = \frac{W_{M2}}{W_{M1}} \tag{3.4}$$

or

$$I_{out} = I_{ref} \cdot \frac{W_{M1}}{W_{M2}}. \tag{3.5}$$

Thus, the width ratio can be chosen to get the wanted output current. Equal gate-length for both transistors makes the current-mirror less influenced by process variations. Any desired current can be generated from the master bias source by mirroring currents in this way, combining PMOS and NMOS mirrors and adjusting the ratios between the transistors in the mirrors.

A current source implemented using a current-mirror will have a finite output impedance, and the output current I_{out} will therefore change with varying $V_{ds,M1}$. The output impedance for a transistor operated in the saturation region is proportional to the gate-length, so minimum length for the current-mirror transistors is not advisable. In this design gate-length of 0.5μm is used in the current-mirrors.

Voltage sources

The voltage that appears at the drain of the diode-connected transistors in the mirrors can be used as bias voltage sources. If the source of a NMOS mirror is grounded, the voltage at the

drain is given by the drain current through the diode-connected transistor I_d and the width to length ratio as

$$V_D = \sqrt{\frac{I_D}{\frac{1}{2}k_n\frac{W}{L}}} + V_{th}, \tag{3.6}$$

where k_n is the gain-factor of the transistor and V_{th} is the threshold voltage.

3.3 LNA design

To have maximum power transfer from antenna to the LNA, the input of the LNA needs to be matched to the antenna. From the specification, the input impedance of the LNA should be 50 Ω. As the LNA used in this design is differential, this translates to 25 Ω input impedance per side of the LNA.

The input of a common-source stage is capacitive, and has got no real part. Through inductive degeneration a real part is created.

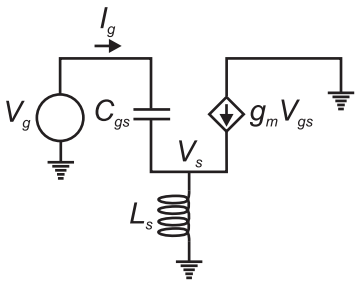


Figure 3.6: Small-signal model for common-source amplifier with inductive degeneration

The small-signal model of the input-circuit of one side of the differential inductively degenerated LNA is shown in figure 3.6. Considering only the gate-source capacitance C_{gs}, the transconductance g_m, and the degeneration inductor L_s, calculation of $Z_{in} = \frac{V_g}{I_g}$ gives

$$Z_{in} = \frac{g_m}{C_{gs}}L_s + sL_s + \frac{1}{sC_{gs}}. \tag{3.7}$$

The real part of the input impedance is proportional to the inductance of the degeneration inductor L_s. As the input impedance is purely real only at resonance, an extra degree of freedom is necessary. This is accomplished with an inductor L_g at the gate of the transistor, as illustrated in figure 3.7.

The input impedance is now

$$Z_{in} = \frac{g_m}{C_{gs}}L_s + s(L_s + L_g) + \frac{1}{sC_{gs}} = \omega_T L_s + s(L_s + L_g) + \frac{1}{sC_{gs}} \tag{3.8}$$

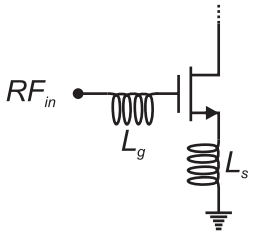


Figure 3.7: LNA input stage with inductive source-degeneration

or at resonance

$$Z_{in} = \frac{g_m}{C_{gs}} L_s = \omega_T L_s, \tag{3.9}$$

where ω_T is the unity gain frequency of the transistor. Due to the differential architecture, where the common source node of the degenerating inductors is a virtual ground, the input impedance will be largely unaffected by the non-zero impedance between the signal source ground and the ground of the current-source at the common source node [11].

As the current consumption for the whole front-end should be about 3 mA, the current for the LNA is set to 0.8 mA. To have sufficient overdrive voltage for good linearity, the width and length of input transistors M1 and M2 is set to 50 μm and 0.18 μm as a starting point for the design. For the given current consumption this transistor has $g_m = 5.6$ mS and $C_{gs} = 49$ fF, which corresponds to $\omega_T = 18$Grps, and an overdrive voltage of 34.4mV. From equation (3.7), the inductor L_s needed to create a real part is 0.21 nH, which is much less than the smallest inductor modeled in the process. Also, to create a purely real input impedance the total inductance in the input matching network $L = L_g + L_s$, has to resonate with the gate-source capacitance and is given by

$$L = \frac{1}{\omega_0^2 C_{gs}}, \tag{3.10}$$

which yields almost 87 nH for $C_{gs} = 49$ fF. Only 0.21 nH of this inductance is accounted for by L_s. Clearly this inductance can not be implemented on-chip.

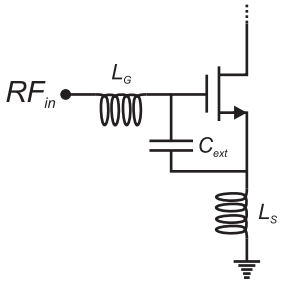


Figure 3.8: LNA input stage with additional capacitor C_{ext}

However, by adding an additional capacitor C_{ext} in parallel with the existing C_{gs}, figure 3.8, the inductance needed can be greatly reduced. With the added C_{ext} the expression for Z_{in} and inductance L needed must be rewritten:

$$Z_{in} = \frac{g_m}{C_{gs}+C_{ext}} L_s = \omega_T L_s, \tag{3.11}$$

$$L = \frac{1}{\omega_0^2 (C_{gs}+C_{ext})}. \tag{3.12}$$

Calculating C_{ext} from equation (3.12), assuming a total on-chip inductance of 14 nH, yields $C_{ext} = 255$ fF. From equation (3.11), $L_s = 1.36$ nH and $L_g = 12.64$ nH. However, in [11] it is shown that the minimum noise figure of the inductively degenerated LNA increases as the ratio $\frac{\omega_T}{\omega_0}$ decreases. Simulations with Eldo show that a C_{ext} of 255 fF will increase the noise figure to more than 4 dB for the LNA. Also, a 12.64 nH on-chip inductor has a Q-factor of only 6.6, which corresponds to a series resistance of 29 Ω; more than the wanted real part. The additional capacitance will also affect the gain of the LNA, which is given by

$$A_v = G_m Z_L. \tag{3.13}$$

Z_L is the load impedance, and G_m is the overall transconductance of the input transistor given by

$$G_m = g_m Q_{in}, \tag{3.14}$$

where Q_{in} is the quality factor of the series RLC input network. At resonance

$$Q_{in} = \frac{1}{\omega_0 C R} = \frac{1}{\omega_0 (C_{gs}+C_{ext})(R_s + \frac{g_m}{C_{gs}+C_{ext}} L_s)} \tag{3.15}$$

Inserting equation 3.15 into equation (3.14) gives

$$G_m = \frac{\frac{g_m}{C_{gs}+C_{ext}}}{2\omega_0 R_s}. \tag{3.16}$$

The series-resistances of L_s and L_g have been neglected in equation (3.15) as they are much smaller than the source resistance R_s. The nominal g_m of the input transistor is multiplied by Q_{in}. This is due to the voltage across C_{gs} and C_{ext}, and therefore V_{gs}, being Q_{in} times the voltage from the source, at resonance. From equations (3.16) and (3.13) it is seen that the addition of C_{ext} will decrease the available gain of the LNA.

A compromise has to be made between low noise, low current consumption, gain, and on-chip integration, and it was decided to reduce C_{ext} to 150 fF and instead use a high-Q off-chip inductor for L_g. The drawbacks of using an off-chip inductor are the additional cost for the customer

buying the off-chip inductors and the extra work necessary to mount them on PCB. An excerpt from the datasheet of the NIS0603 series of inductors is enclosed in appendix D. For instance, the 10 nH NIS06J10NTR has a Q-factor of 70 at 2.4GHz. The off-chip inductor can be modeled by an ideal inductor in series with a resistor R_s. R_s is calculated from the Q factor as

$$R_s = \frac{\omega_0 L}{Q}. \tag{3.17}$$

Through simulation with Eldo, taking the effect of package parasitics and bias circuitry into account, the final values for the input matching network was set to $L_s = 2.5$ nH and $L_g = 10$ nH.

The cascode transistors are chosen to be the same size as the input transistors. This choice is not necessarily ideal, but allows the drain of the input device and the source of the cascode transistor to be merged in the layout of the chip [11].

As mentioned earlier, the gain of the LNA depends on the overall transconductance G_m and the load impedance Z_L. The load impedance will dependend on the tuned load, the output impedance of the cascode transistor, and the input impedance of the I/Q-mixers following the LNA. The load inductor is tuned so that Z_L is resistive at the resonant frequency. Z_L is then

$$Z_L = R_p || R_{ds}, \tag{3.18}$$

where R_p is the parallel resistance of the tuned load due to the loss in the inductor, and R_{ds} is the output resistance of the cascode transistor, set by the cascode device current and length. The capacitive inputs of the mixers, as well as the drain capacitance of the cascode transistor and the inductors own parasitic capacitance to substrate, will affect the necessary inductor value. The process has a low-resistance thick top metal layer available that can be utilized for low-loss inductor design, reducing the series resistance R_s. R_p in equation (3.18) can be related to R_s by [11]

$$R_p = R_s(Q^2 + 1), \tag{3.19}$$

where Q is the quality factor of the load inductor. Thus, a high quality factor load inductor yields high gain for the LNA.

The value of the inductor was determined by adjusting the inductance to resonate at 2.44 GHz when the mixer was connected to the LNA output. Finally the inductor was set to 9.9 nH. The inductor utilizes the thick top metal layer of width 20 um, has a diameter of 418 μm, and has 5.5 turns.

The schematic of the complete LNA is shown in figure 3.9. The gate of the cascode transistors is connected to V_{dd} to ensure operation in saturation. The package and pad parasitics separating the on-chip and off-chip components are represented by the blocks *Package*, see chapter 3.2.2.

The bias circuit that generates the bias current I_{bias} and voltage $V_{bias,in}$ can be found in appendix E. Table 3.3 summarizes the component values of the LNA.

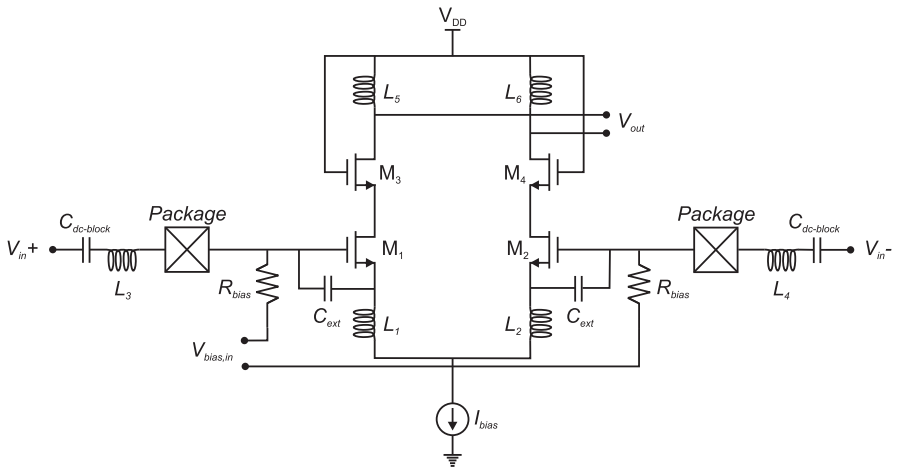


Figure 3.9: Complete LNA

Component	Value	Unit
M_1-M_4	W=50, L=0.18	μm
L_1-L_2	2.5	nH
L_3-L_4	10	nH
L_5-L_6	9.9	nH
R_{bias}	10	kΩ
$C_{dc-block}$	3	pF

Table 3.1: LNA components

3.4 Mixer design

3.4.1 Transconductor and switches

The input transconductor of the mixer consists of the input devices M_1 and M_2, and is biased as shown in figure 3.2. The transconductor bias current is set by the width to length ratio of the input devices and the bias devices M_{B1} and M_{B2}, and the bias current I_{bias}. To maximize the linearity of the transconductor, the smallest transistor in the process, width 25 μm and length 0.18 μm, is used for M_1 and M_2. The bias devices width are set to 35 μm and length 0.5 μm. Due to the two bias devices being in parallel, the current mirror ratio is approximately 1. This will not be ideal as far as current overhead is concerned, but the transconductor linearity is considered more important.

The overdrive voltage of the input devices in the transconductor must be larger than the maximum voltage swing to ensure that the devices do not enter the subthreshold region of operation. For a LNA gain of 27 dB, and assuming that the largest input signal is less than or equal to the 1 dB compression point (1 $\mathrm{dB_{CP}}$) of the front-end, the largest input signal to the mixer per side

is given by

$$1\,\mathrm{dB_{CP}} - 6\,\mathrm{dB} + G_{LNA} = (\mathrm{IIP3} - 9.64\,\mathrm{dB}) - 6\,\mathrm{dB} + 27\,\mathrm{dB} = -8.64\,\mathrm{dBm}, \tag{3.20}$$

where the -6 dB is due to only considering one phase of the differential signal, and the 1 $\mathrm{dB_{CP}}$ is related to the IIP3 specification of the front-end as [18]

$$1\,\mathrm{dB_{CP}} = \mathrm{IIP3} - 9.64\,\mathrm{dB}. \tag{3.21}$$

The following equation is then used to convert from power P in dBm to peak voltage:

$$V_{pk,out} = \sqrt{\frac{10^{\frac{P}{10}} \cdot 50 \cdot 1\,\mathrm{mW}}{0.5}}. \tag{3.22}$$

Solving for P=-8.64 dBm, the overdrive voltage of the input devices must be larger than 116.9 mV. This determines the minimum bias current in the transconductor, which for the device sizes given above is approximately 1.1 mA.

For the switch transistors, M_3 to M_6 in figure 3.2, a large transistor area is favorable for low 1/f-noise, as stated in chapter 1.2.1. However, large gate area will also increase the parasitic capacitance in the RF-path which degrades the IIP2, see chapter 2.3. Wide switches reduces the overdrive voltage for a given current. As the transconductor require a drain-source voltage of more than 500 mV for good linearity, a low overdrive voltage will reduce the necessary gate bias voltage of the switches, leaving more headroom for the mixer loads [8]. Considering the above, the width of the switches is chosen as twice the input device width. As the current through each switch is half the current through each input device in the transconductor the overdrive voltage of the switches will ideally be one fourth the overdrive voltage of the input devices. In practice it will be lower due to the body effect.

3.4.2 Load resistors and LO amplitude

Using the values found for transconductor and switch sizes, and the minimum current of 1.1 mA as a starting point, the LO amplitude and load resistor sizes is chosen as explained here. If the design does not satisfy the linearity and noise specification, the mixer bias current is increased and the process of determining LO voltage and load resistors repeated.

When choosing the load resistance, the largest signal swing at the output must be considered. To avoid clipping, and avoid that the switches enter the linear region of operation, the voltage drop across the load resistors and the difference between the drain-source voltage and $V_{ds,sat}$ of the switches, must be larger than the largest signal peak. Using a similar approach as that for finding the largest input signal to the mixer; for a LNA gain of 27 dB, and assuming a maximum mixer conversion gain of 9 dB, and that the largest input signal is less than or equal to the 1 dB compression point of the front-end, the largest output signal per side in dBm is

$$1\,\mathrm{dB_{CP}} - 6\,\mathrm{dB} + G_{LNA} + G_{mixer} = (\mathrm{IIP3} - 9.64\,\mathrm{dB}) - 6\,\mathrm{dB} + 27\,\mathrm{dB} + 9\,\mathrm{dB} = -0.64\,\mathrm{dBm}. \quad (3.23)$$

Converting to peak voltage using equation (3.22), and adding some margin, gives 0.36 V as the minimum voltage drop across the mixer load resistor and minimum difference between the drain-source voltage and $V_{ds,sat}$ of the switches.

The conversion gain of the mixer is proportional to the value of the load resistors [11]. There is no requirement on the conversion gain in the specification, but if subsequent stages were to be added a large conversion gain would be beneficial, see chapter 3.2.1. Thus, the load resistors are designed for maximum conversion gain. Assuming a minimum drain-source voltage of 0.5 V for the input devices and 0.6 V for the switches including the 0.36 V for signal swing, the bias voltage at the drain of the switches is minimum 1.1 V. The maximum load resistance for 1.1 mA current is then

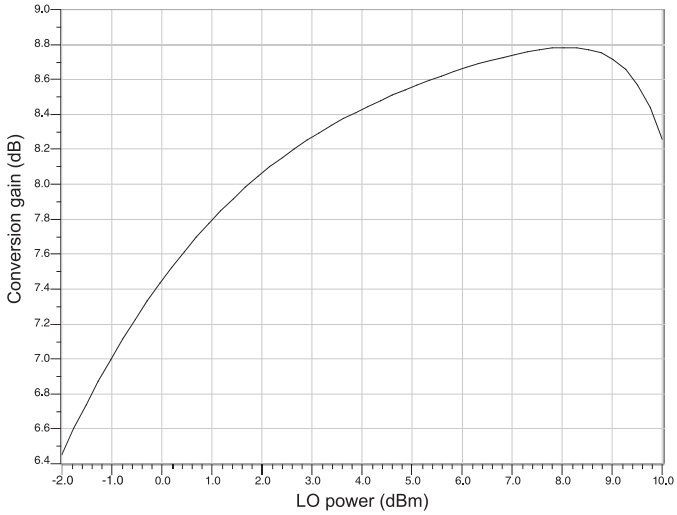
$$R_{load} = \frac{(1.8\,\mathrm{V} - 1.1\,\mathrm{V})}{0.55\,\mathrm{mA}} = 1270\,\Omega. \quad (3.24)$$

Now the LO amplitude can be determined. The LO amplitude should only be large enough for a good switching. A too small LO amplitude will increase the influence of self-mixing. A too large amplitude could cause spikes in the current and in the worst case cause transistors to leave the saturation region of operation. Even if this does not happen, the output spectrum can be dominated by the frequency components due to the spikes. This is caused by the parasitic capacitance on the common source node of the switches. By sweeping the LO voltage against IIP3, conversion gain, and noise the LO voltage can be determined. Such a plot for the resistor chosen above and 1.1 mA mixer current is shown in figure 3.10.

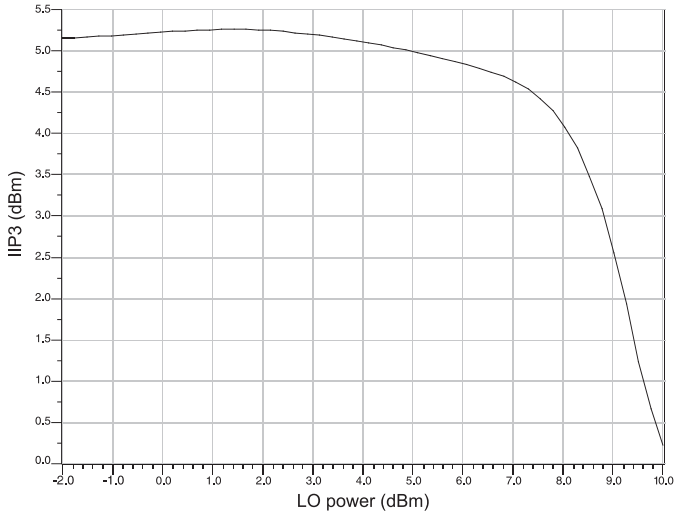
The mixer IIP3 required to reach the specified front-end IIP3 of -20 dBm for a LNA gain of 27 dB and IIP3 of -12.2 dBm is given by equation (3.2) to be 7.8 dBm for a worst case. The required mixer noise figure for a LNA noise figure of 2.5 dB and 27 dB gain is given by equation (3.1) to be maximum 25.7 dB. From figure 3.10 it is seen that the noise requirement is met for a LO power greater than 2 dBm. However, the IIP3 peaks at 5.25 dBm for a LO power of 1.5 dBm, hence the front-end will not meet the specification. The conversion gain does not exceed 9 dB, and the 0.36 V output headroom set earlier is therefore sufficient.

To meet the IIP3 specification, the mixer current can be increased. This increases the overdrive of the input devices and switches. However, the load resistors must be reduced to accommodate the increased voltage drop, which in turn will cause a decrease in conversion gain. Also, the LO power must be increased due to the increase in switch overdrive voltage. It is found that both the linearity and noise requirement can be met simultaneously by increasing the mixer current to 2.4 mA and using a LO power of 9.5 dBm. Then, the load resistors are 583 Ω, the mixer IIP3 is 8.4 dBm, and the noise figure is 24.1 dB.

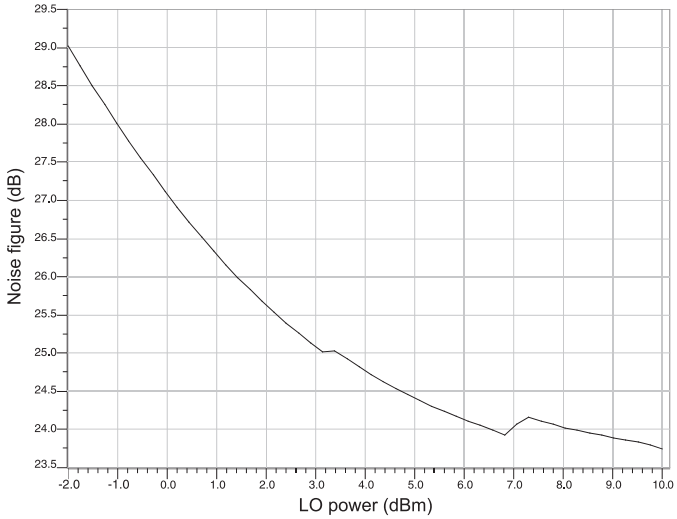
When the resistance value has been decided, the dimensions and resistor type must be considered. Three types of resistors are available in the process; non-salicided poly N+ and P+ type,



(a) Conversion gain



(b) IIP3



(c) Noise figure

Figure 3.10: Mixer conversion gain, IIP3, and noise figure versus LO power for 1.1 mA current

and non-salicided HR (High Resistance) type. From the process documents it is found that the P+ type has slightly better matching properties than the other types of resistors, and is therefore chosen for the mixer load. A wide resistor will have better matching properties compared to a narrow resistor, at the cost of area. In chapter 3.5 load tuning will be considered as a way of improving the IIP2, and if implemented the load mismatch will be compensated for. The load tuning utilizes many resistors of size equal to the regular mixer resistor, so big savings in area can be made if the mixer resistor area is minimized. Considering this, the 583 Ω resistor width is set to 2 μm and the length to 2.4 μm.

The bias circuit that generates the bias current I_{bias} and gate biasing for the switches can be found in appendix E. Table 3.4.2 summarizes the component values of the mixer.

Component	Value	Unit
M_1-M_2	W=25, L=0.18	μm
M_3-M_6	W=50, L=0.18	μm
R_{load}	583	Ω
M_{B1}-M_{B2}	W=35, L=0.5	μm
R_{bias}	10	kΩ
$C_{dc-block}$	1	pF

Table 3.2: Mixer components

3.5 Mixer load tuning

In chapter 2.4.1 load tuning was suggested as a way of improving IIP2 for the mixer. As stated, the size of the resistors in the IIP2 trim blocks and the resolution of the tuning must be determined through simulation. In this section is the resistor values in the IIP2 trim blocks, tuning range, area cost, and bit resolution in the IIP2 tuning explored.

3.5.1 Mismatch in nominally matched pairs

As stated in chapter 2.2, mismatch causes variations in β and threshold voltage between two nominally equal devices, and leakage of second-order intermodulation current to the mixer output.

Simulating mismatch

Usually Monte Carlo simulations are used to evaluate the effect of mismatch. In a Monte Carlo simulation multiple runs are performed with model parameters varying according to probability distributions for each run. However, the process used in this design is not set up for this. To be able to study mismatch without running Monte Carlo simulations, the mismatch has to be introduced by manipulating the transistor Spice model parameters manually. In order to keep the number of results and simulations manageable only threshold mismatch is considered here. To directly control the threshold of each transistor the model parameter $vth0$ is changed for their respective models. The actual threshold voltage will be very dependent on body effect, causing a change in $vth0$ to have less impact on the actual threshold voltage.

Standard deviation for device pair mismatch

From the process documents, the difference in threshold voltage between two transistors in a nominally identical transistor pair can be described by the standard deviation $\sigma(V_{th,diff})$. It is related to the dimensions of the transistors as

$$\sigma(V_{th,diff}) = \frac{A_{V_{th}}}{\sqrt{WL}} + C_0, \tag{3.25}$$

where $A_{V_{th}}$ and C_0 are technology constants. The width W and length L of the transistor is in micrometers. From the process documents the technology constants are given as $A_{V_{th}} = 4.787\,\text{mV}\cdot\mu\text{m}$ and $C_0 = 0.5328\,\text{mV}$.

Then, for the switches of the mixer

$$\sigma(V_{th,3} - V_{th,4}) = \sigma(V_{th,5} - V_{th,6}) = \frac{4.787}{\sqrt{75\,\mu\text{m} \times 0.18\,\mu\text{m}}} + 0.5328 = 1.84\,\text{mV}. \tag{3.26}$$

The standard deviation for the threshold voltage of a single transistor $\sigma(V_{th})$ in a nominally matched pair is $1/\sqrt{2}$ times smaller than the standard deviation for the difference between the transistors, see appendix A. Thus,

$$\sigma(V_{th}) = \frac{1}{\sqrt{2}} \cdot 1.84\,\text{mV} = 1.3\,\text{mV}. \tag{3.27}$$

Simulations show that a one standard deviation, or 1.3 mV, change in model parameter $vth0$ corresponds to a 1.1 mV change in actual threshold voltage. Increasing $\sigma(V_{th})$ by 0.25 mV compensates for this discrepancy, and $\sigma(V_{th}) = 1.55\,\text{mV}$ is used in the following sections.

3.5.2 IIP2 trim block

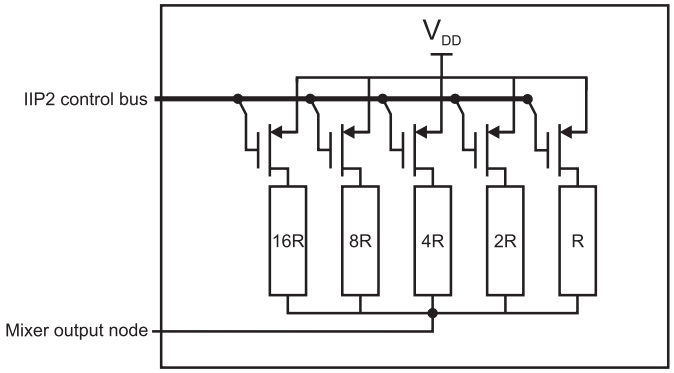


Figure 3.11: IIP2 trim block

Figure 3.11 shows how a single IIP2 trim block with 5 bit resolution is implemented. The smallest resistance value, that is when all resistors in the block are switched in, will determine the largest imbalance that can be canceled.

In order to decide on the tuning range necessary, a worst-case mismatch is determined by simulating the IIP2 of all combinations of $\pm 2\sigma(V_{th})$ mismatch for the transistors in the mixer. This assures that 95.4% of the possible combinations of threshold voltage mismatch in the pairs are covered.

Simulation shows a worst case IIP2 of +20.3 dBm, which occurs when M3 and M5 has two standard deviations increase, and M4 and M6 has two standard deviations decrease, in threshold voltage. Due to symmetry the IIP2 has the same value when M3 and M5 has two standard deviations decrease, and M4 and M6 has two standard deviations increase, in threshold voltage.

The IIP2 trim blocks can be represented by resistors $R_{trim,p}$ and $R_{trim,n}$ shunting the positive and negative outputs of the mixer. The smallest resistance R_{min} of the IIP2 trim block can now be determined by sweeping the value of one of the resistors for the worst-case mismatch. Which

resistor is dependent on how the mismatch has affected the balance of the mixer. From figure 3.12 it is seen that the IIP2 is at a maximum for a resistance of approximately 44 kΩ.

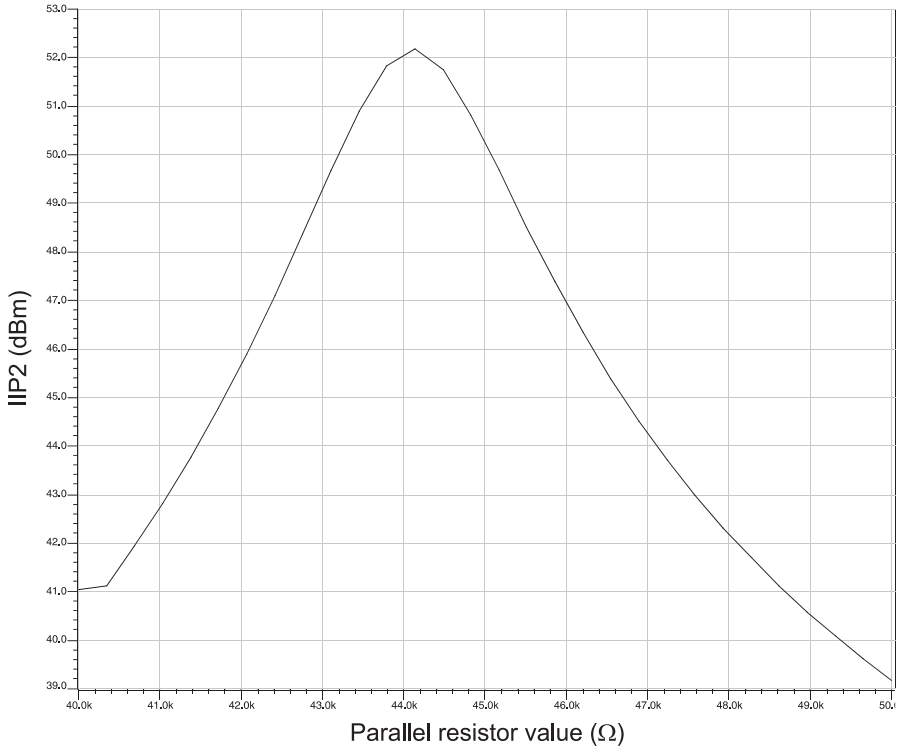


Figure 3.12: Resistance value for worst case offset

To account for other sources of imbalance R_{min} is chosen to be 20 kΩ. For the regular mixer load of 583 Ω this corresponds to a tuning range of approximately ±3%. Solving the following equation for R gives the smallest resistor in the IIP2 trim block for a resolution of N bits:

$$\frac{1}{R_{min}} = \sum_{i=0}^{N-1} \frac{1}{R2^i}, \tag{3.28}$$

Calculation of R for 5 and 7 bit resolution with $R_{min} = 20\,\text{k}\Omega$ gives $R = 38750\,\Omega$ and $R = 39688\,\Omega$ respectively. As the resistor chains should consist of unity resistors of value equal to the regular load, R is rounded to the closest multiple of the regular mixer resistance, which gives $R = 38478\,\Omega$ for 5 bit resolution and $R = 39644\,\Omega$ for 7 bit. Because of the parallel nature of the IIP2 trim block and the quantization to unity resistors, increasing the resolution changes R minimally. For simplicity R is set to 39644 Ω for both resolutions, or 68 unity resistors in series. The resistance of the switches have been ignored here. The tuning range and step size will be somewhat larger due to this resistance.

Table 3.3 shows the values for IIP2 trim blocks with 5 and 7 bit resolution. The area is calculated considering a 583 Ω mixer resistor laid out for minimum area with width 2 μm and length

Bit number	No. of unity resistors	Resistance	Area
5 bit			
1	68	39644 Ω	359 μm^2
2	136	79288 Ω	718 μm^2
3	272	158576 Ω	1436 μm^2
4	544	317152 Ω	2872 μm^2
5	1088	634304 Ω	5745 μm^2
Total	2108	-	11130 μm^2
7 bit			
1	68	39644 Ω	359 μm^2
2	136	79288 Ω	718 μm^2
3	272	158576 Ω	1436 μm^2
4	544	317152 Ω	2872 μm^2
5	1088	634304 Ω	5745 μm^2
6	2176	1268608 Ω	11489 μm^2
7	4352	2537216 Ω	22979 μm^2
Total	8636	-	45598 μm^2

Table 3.3: 5 and 7 bit IIP2 trim block values

2.64 μm.

Chapter 4

Simulation and results

The circuits were verified using the Mentor Graphics suite of IC design programs. Schematic drawing and netlisting was performed with Design Architect, and simulation of the circuits produced was performed using Eldo/Eldo RF. The graphs were plotted with EZWave.

The testbenches used in the simulations are shown in appendix E.

IIP2 and IIP3 simulations

To measure second- and third-order input referred intercept points IIP2 and IIP3 a two-tone test was performed. The two tones were spaced 5 MHz apart, and had equal power of -60 dBm.

Measuring the resulting spectrum, the IIP2 and IIP3 can be calculated as [21]

$$\text{IIPn} = \text{P}_{\text{in}} + \frac{\Delta}{n-1}, \tag{4.1}$$

where P_{in} is the input power in dBm and Δ is the difference between the fundamental signal component and nth order distortion component at the output, both in dB. Spice-code for the IIP2 and IIP3 measurements is found in appendix C.1.

Balun

To be able to study the non-linear behavior of the LNA and mixer it is necessary to use large signal sinusoidal steady state (SST) analysis. The Fourier-source that must be used when doing SST analysis is only available in a single-ended version. The input to the LNA and mixer is differential, hence the signal has to be converted from balanced to unbalanced by a *balun*. For simulation purposes, ideal voltage-controlled voltage-sources (VCVS) and current-controlled current-sources (CCCS) can be used to make a simple balun, as shown in figure 4.1a [9]. It consists of two VCVSs and two ideal current controlled current sources (CCCS), all of which have a gain of 0.5.

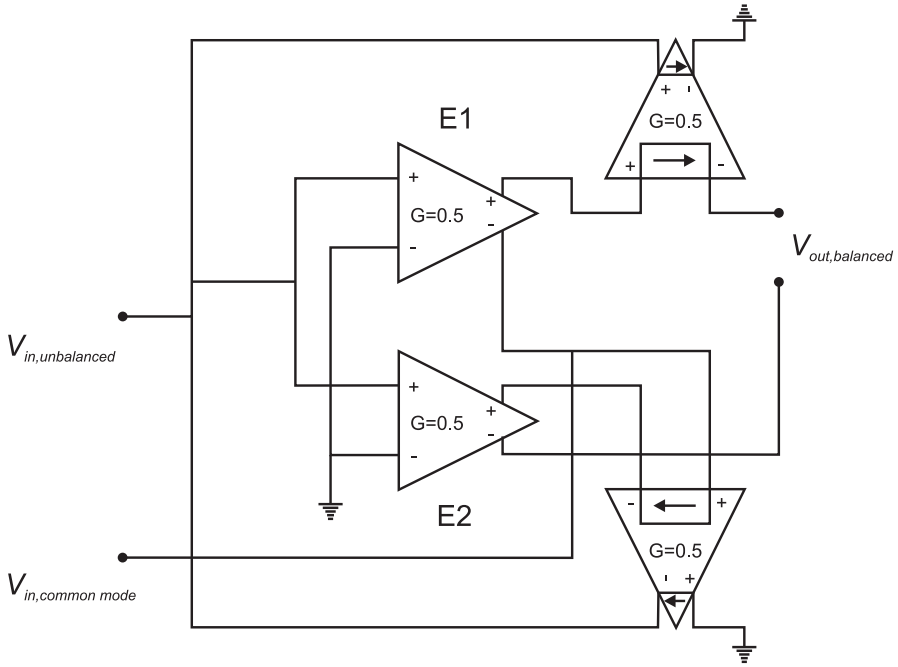


Figure 4.1: Balun

4.1 Results

Figure 4.2 shows the voltage gain of the LNA versus input frequency. The gain peaks at 27.16 dB, and varies less than 0.5 dB within the 2.4-2.483 GHz band. The bandpass nature of the LNA is evident, and out-of-band interferers will be attenuated.

Figure 4.3 shows the input reflection coefficient S_{11} versus input frequency. It varies between -18.2 dB and -31 dB in the band of interest, hence the LNA provides a good 50 Ω input match. The narrow band nature of the match is evident, as expected for the inductively degenerated LNA.

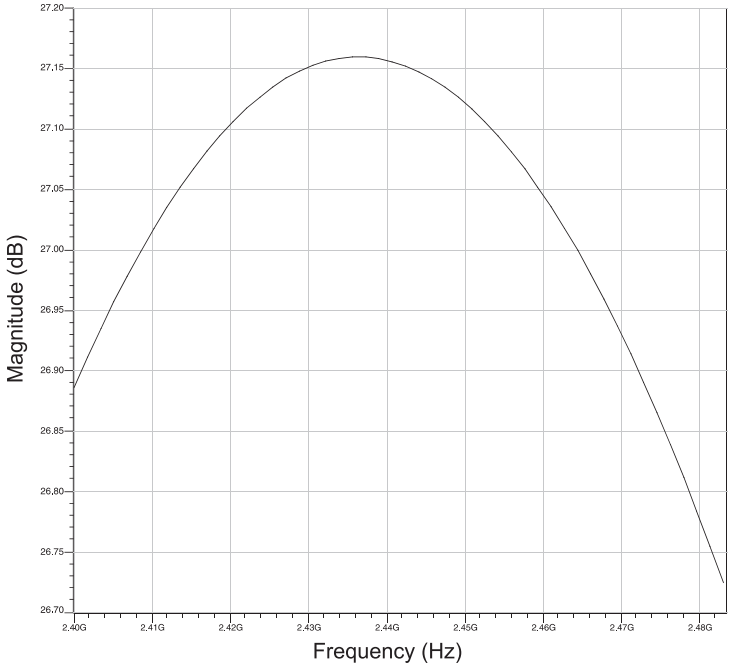


Figure 4.2: LNA voltage gain vs. input frequency

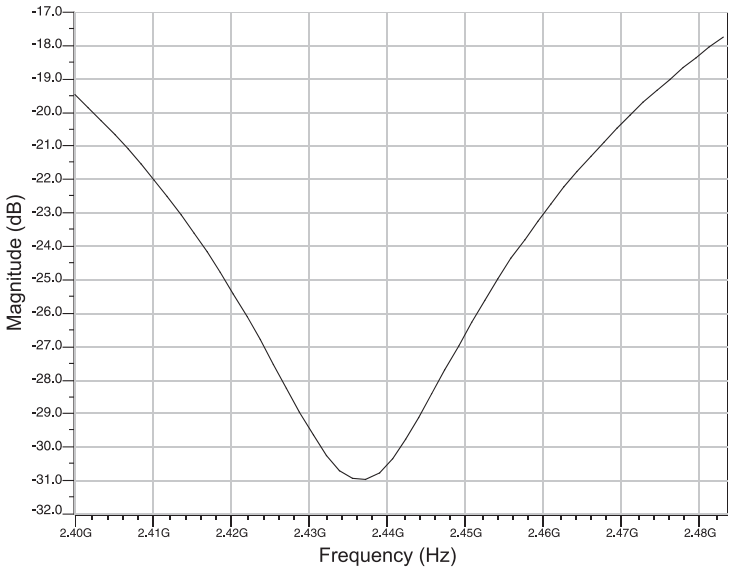


Figure 4.3: LNA S_{11} vs. input frequency

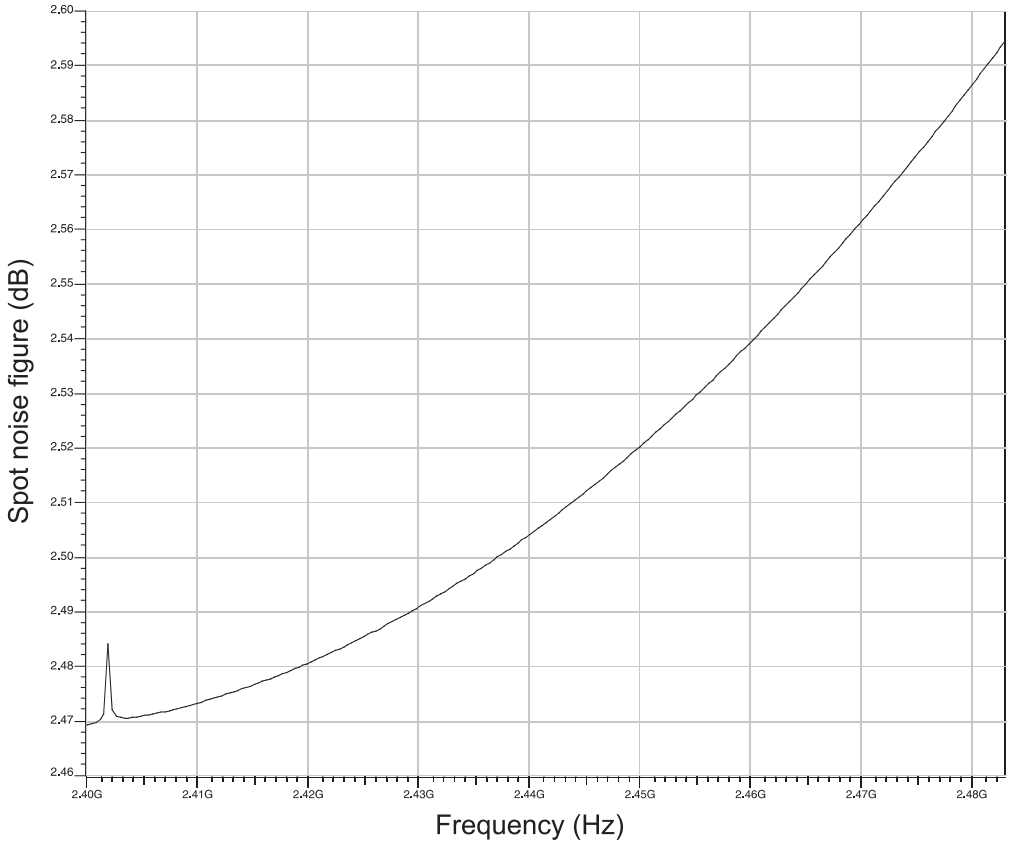


Figure 4.4: LNA spot noise figure vs. input frequency for 2.4-2.483 GHZ

Figure 4.4 shows how the LNA spot noise figure varies within the 2.4-2.483 GHz band. The spot noise figure is at a minimum of 2.47 dB at 2.4 GHz and increases to 2.6 dB at 2.483 GHz. Figure 4.5 shows the spot noise figure varying between 2.3 GHz and 2.483 GHz, and it is seen that the noise figure has a minimum of 2.47 dB at 2.39 GHz. The source impedance yielding a power match and the source impedance yielding a noise match normally do not coincide, and there is a trade-off between noise and input match [19]. Comparing figure 4.5 to figure 4.3 the spot noise figure minimum and the minimum S_{11} occur at relatively close frequencies. This might be due to the added C_{ext}, which has been used to create a simultaneous noise and power match in [13]. The purpose of adding C_{ext} was not to create such a match in the design presented here, but with increased effort this might be accomplished.

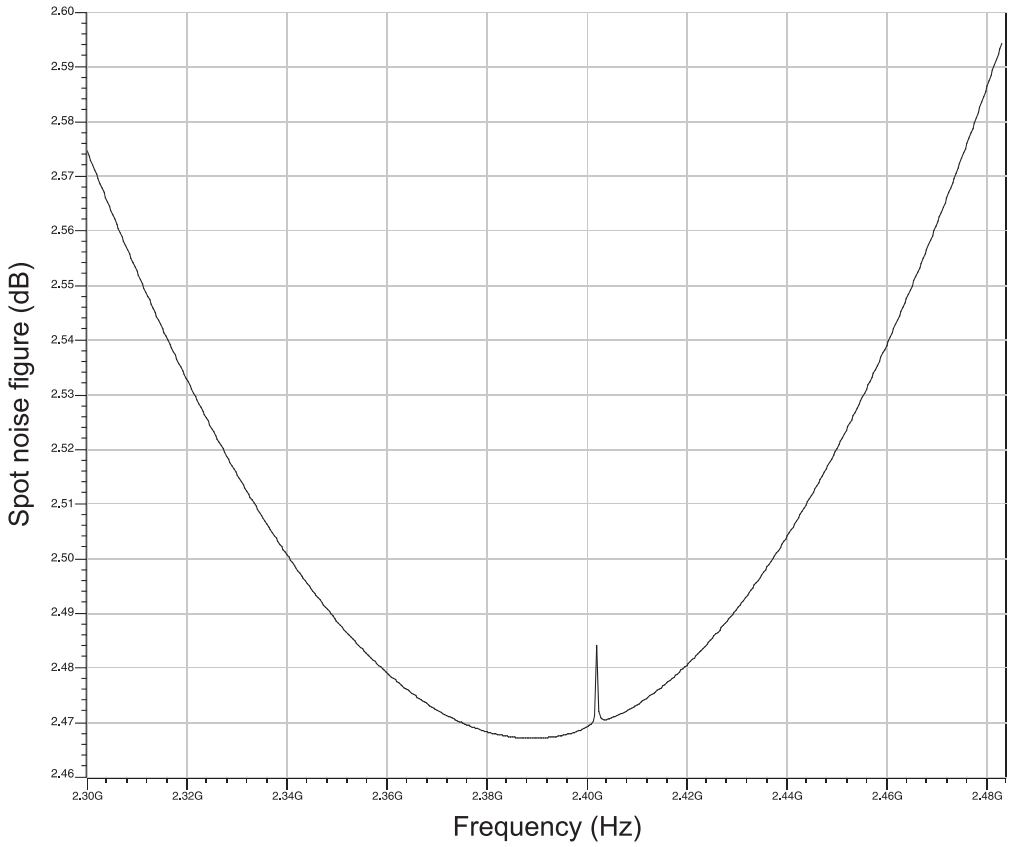


Figure 4.5: LNA spot noise figure vs. input frequency for 2.3-2.483 GHz

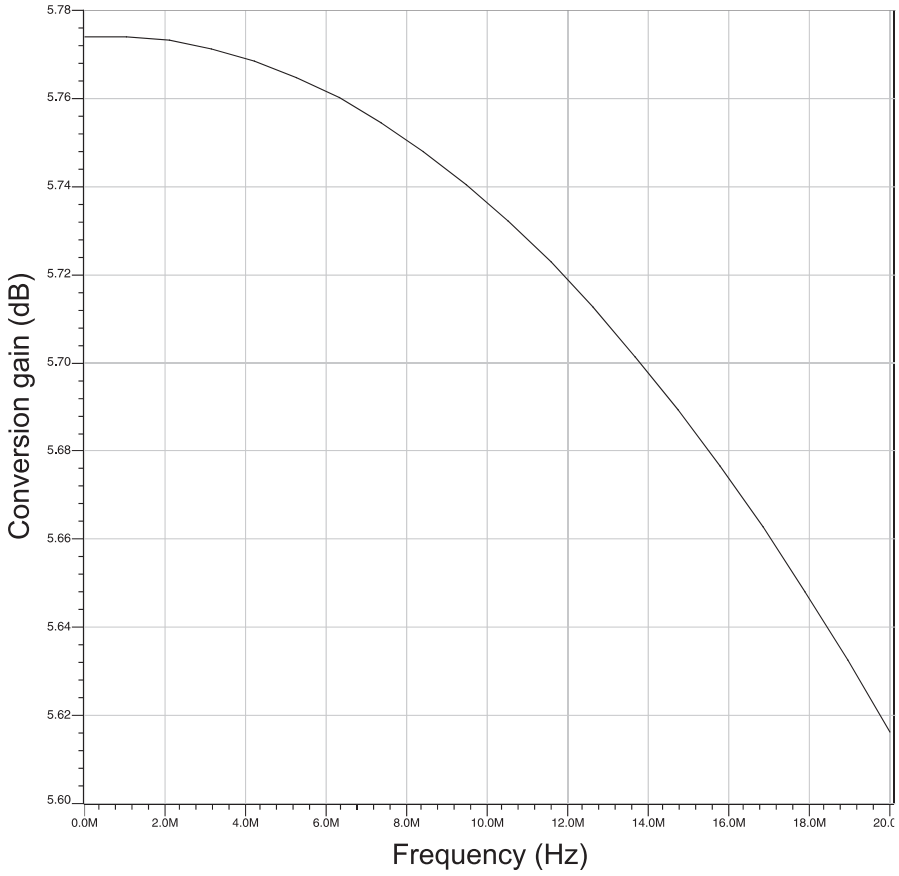


Figure 4.6: Mixer conversion gain vs. output frequency

Figure 4.6 shows the conversion gain of the mixer versus output frequency. Within a 20 MHz bandwidth the gain varies 0.15 dB, and has a peak of approximately 5.8 dB. Considering the well-known equation for mixer conversion gain [11]

$$A_{cg} = \frac{2}{\pi} g_m R_L, \tag{4.2}$$

where R_L is the mixer load resistance and g_m is the transconductance of the input device, and calculating for the 583 Ω R_L and the 8 mS simulated transconductance of the input devices yields a conversion gain of 9.5 dB. The reason for the discrepancy between theoretical conversion gain and simulated value is not clear.

Figure 4.7 shows the double sideband spot noise figure of the mixer versus output frequency. At 1 MHz the spot noise figure is 24.1 dB. The 1/f-noise is clearly dominant, and the 1/f-noise corner for the mixer is well above 1 MHz. Considering the 1/f-noise performance of the differential Gilbert-cell mixer presented in [5], where a 1/f-noise corner below 100 kHz is reported, the 1/f noise corner here must be considered as far from optimal.

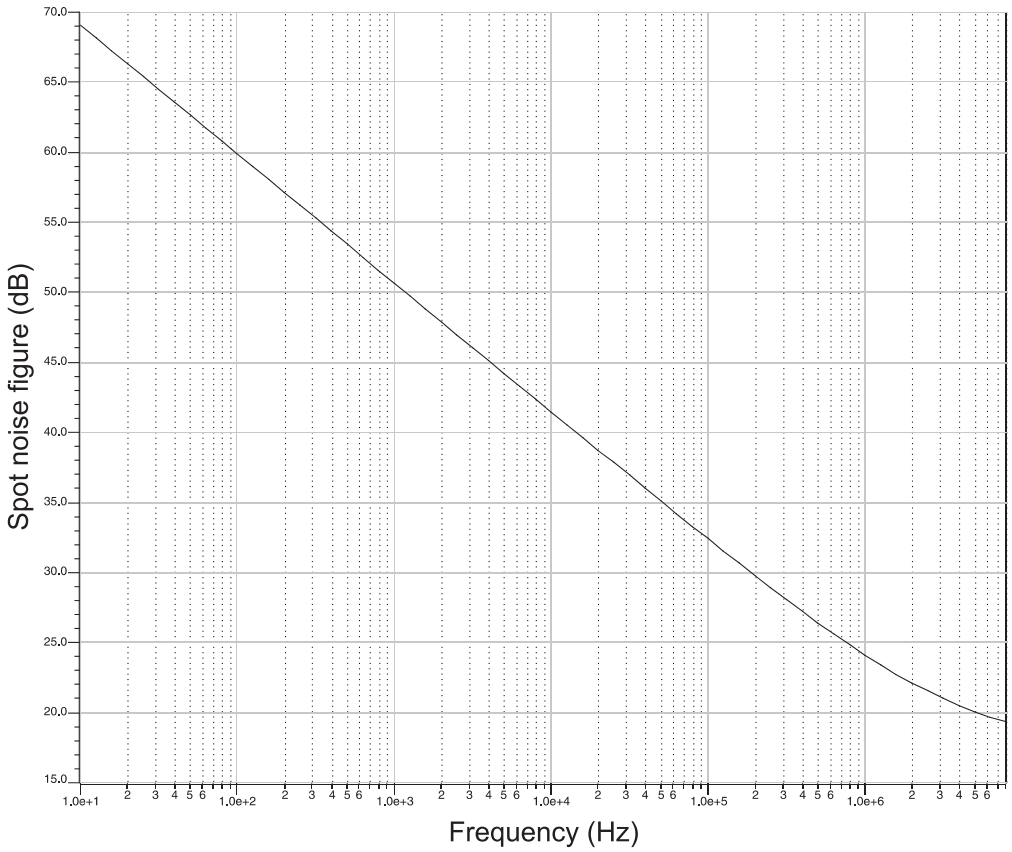


Figure 4.7: Mixer DSB spot noise figure vs. output frequency

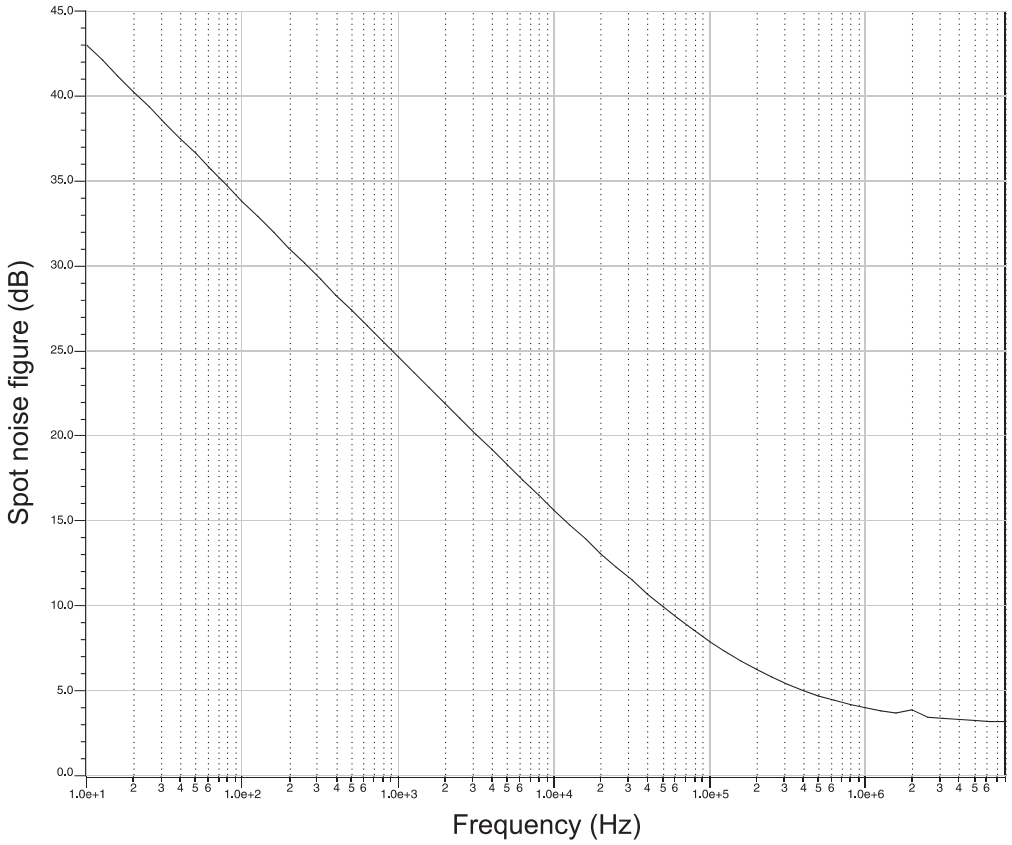


Figure 4.8: Front-end DSB spot noise figure vs. output frequency

Figure 4.8 shows the double sideband spot noise figure for the whole front-end. At 1 MHz the noise figure is 4 dB, as required by the specification. Compared to figure 4.7 the 1/f-noise corner is lower.

Table 4.1 shows the IIP3 and current consumption of the LNA, mixer and whole front-end. The IIP3 of the LNA is much lower than the -5 dBm expected from an inductively source-degenerated LNA architecture [17]. This is probably due to the low LNA current consumption. For the 8.4 dBm IIP3 of the mixer the total front-end IIP3 of -19.7 dBm is as expected from equation (3.2). The front-end IIP3 satisfies the specification.

The current consumption of the LNA, a single mixer, and total front-end with biasing is shown in table 4.1. The front-end consumes more than double the 3 mA current specified, but this was a flexible requirement and had to be exceeded to satisfy the linearity requirement. The difference between the total current consumption and that of the LNA and the two mixers together is 1.86 mA, which is due to the biasing circuitry. The biasing of the mixer transconductor, I_{bias} in figure 3.2, is responsible for 1.45 mA of this current.

Parameter	Value	Unit
LNA IIP3	-12.2	dBm
LNA current consumption	0.74	mA
Mixer IIP3	8.4	dB
Mixer current consumption	2.41	mA
Front-end IIP3	-19.7	dBm
Front-end total current consumption	7.42	mA

Table 4.1: LNA, mixer, and front-end linearity and current consumption

Case	IIP2 uncompensated	$R_{trim,x}$	IIP2 compensated	IIP2 improvement	$IIP2_{max}$
5 bit					
WCase	+20.3 dBm	42287 Ω	+48.3 dBm	+28 dB	+52.2 dBm
1	+35.2 dBm	211430 Ω	+57.4 dBm	+22.2 dB	+66.2 dBm
2	+44.7 dBm	634300 Ω	+65.3 dBm	+20.6 dB	+75.6 dBm
3	+35.6 dBm	211430 Ω	+54.1 dBm	+18.5 dB	+66.6 dBm
4	+47.9 dBm	634300 Ω	+51.7 dBm	+3.8 dB	+78.3 dBm
5	+27.2 dBm	90615 Ω	+52.1 dBm	+24.9 dB	+58.6 dBm
6	+79.0 dBm	-	-	-	+111.4 dBm
7 bit					
WCase	+20.3 dBm	43745 Ω	+51.8 dBm	+31.5 dB	+52.2 dBm
1	+35.2 dBm	230660 Ω	+62.5 dBm	+27.3 dB	+66.2 dBm
2	+44.7 dBm	634300 Ω	+65.3 dBm	+20.6 dB	+75.6 dBm
3	+35.6 dBm	253720 Ω	+64.3 dBm	+28.7 dB	+66.6 dBm
4	+47.9 dBm	845740 Ω	+62.9 dBm	+15.0 dB	+78.3 dBm
5	+27.2 dBm	97585 Ω	+58.5 dBm	+31.3 dB	+58.6 dBm
6	+79.0 dBm	-	-	-	+111.4 dBm

Table 4.2: IIP2 tuning results

IIP2 tuning results are shown in table 4.2. The IIP2 is measured for 5 and 7 bit tuning resolutions for the worst case and six cases of randomly generated switch mismatches. Either shunt resistor $R_{trim,p}$ or $R_{trim,n}$ were swept, with values corresponding to the resolution and calculations presented in chapter 3.5.2. The $vth0$ values used in each case and the values of the shunt resistor for 5 and 7 bit resolution are listed in appendix B. The maximum IIP2 achievable through tuning with an infinite resolution, $IIP2_{max}$, was found by fine-tuning the value of the shunt resistor.

The ideal case of no mismatch is not shown in the table, but yields an infinite IIP2. The front-end shows good IIP2 performance. The untuned IIP2 is above the +30 dBm required for all cases except the worst-case and case 5. The tuning of the mixer load yields good improvement in IIP2. The 5 and 7 bit resolution tuning offer an average increase in IIP2 of 19.7 dB and 25.7 dB, and average IIP2 after tuning of 54.8 dBm and +60.9 dBm, respectively. The maximum IIP2

Case	IIP3	Conversion gain	DC-offset
5 bit uncompensated			
WCase	-19.7 dB	5.23 dB	9.6 mV
1	-19.7 dB	5.23 dB	1.73 mV
2	-19.7 dB	5.23 dB	0.57 mV
3	-19.7 dB	5.23 dB	1.67 mV
4	-19.7 dB	5.23 dB	0.4 mV
5	-19.7 dB	5.23 dB	4.3 mV
6	-19.7 dB	5.23 dB	0.01 mV
5 bit compensated			
WCase	-19.7 dB	5.2 dB	1.06 mV
1	-19.7 dB	5.23 dB	0.01 mV
2	-19.7 dB	5.23 dB	0.01 mV
3	-19.7 dB	5.23 dB	0.05 mV
4	-19.7 dB	5.23 dB	0.18 mV
5	-19.7 dB	5.23 dB	0.27 mV
6	-	-	-

Table 4.3: IIP2 tuning influence on IIP3, conversion gain, and DC offset

achieved through tuning is +65.3 dBm. Case 6, with an uncompensated IIP2 of +79 dBm, can not be improved by neither resolutions. Case 4 with 5 bit resolution has little improvement in IIP2 compared to the other 5 bit cases, and 11.2 dB less improvement than that obtained with 7 bit resolution. This illustrates the drawback of using a small bit resolution; the larger stepsize could cause the tuning to miss the point where the IIP2 peaks.

As only threshold mismatch is taken into consideration here, the above results must be considered optimistic. Still, for all cases of randomly generated mismatches, both resolutions provide IIP2 more than 20 dB above the 30 dBm required. Considering this, and that the area of the 7 bit trim block is four times the area of the 5 bit trim block (table 3.3), it seems that higher resolution than 5 bit only is warranted if the margins are tighter and the higher average achievable IIP2 of the 7 bit resolution is indispensable.

Table 4.3 shows that the tuning has no influence on the IIP3 and conversion gain, but improves the DC-offset. The correlation seen between improved IIP2 and small DC-offset could be used to implement adaptive control of the tuning.

Table 4.4 shows the influence of self-mixing on IIP2. An attenuated duplicate of the two-tone RF input signal is applied to the LO-port. The IIP2 is measured for the ideal case and the six cases of threshold voltage mismatch, with RF-to-LO attenuation from -30 dB to -60 dB. Comparing the results to table 4.2, the ideal case and case 6 where the IIP2 initially is high suffers the most from the self-mixing. The ideal case has infinite IIP2 for no mismatch, which is reduced to 41 dBm for -30 dB attenuation. Case 6 has +79 dBm IIP2, which is reduced to 41.1 dBm for -30 dB attenuation; almost 30 dB reduction. Cases with initially low IIP2 experience little change in

Case	Attenuation from RF to LO port			
	-30 dB	-40 dB	-50 dB	-60 dB
Ideal	41 dBm	50.6 dBm	60.0 dBm	68.9 dBm
WCase	19.5 dBm	20.2 dBm	20.4 dBm	20.4 dBm
1	31.6 dBm	33.9 dBm	34.8 dBm	35.1 dBm
2	45.1 dBm	46.1 dBm	49.9 dBm	50.3 dBm
3	31.9 dBm	34.3 dBm	35.2 dBm	35.5 dBm
4	46.2 dBm	48.5 dBm	50.0 dBm	57.8 dBm
5	27.5 dBm	27.6 dBm	28.0 dBm	29.2 dBm
6	41.1 dBm	51.4 dBm	62.2 dBm	75.4 dBm

Table 4.4: IIP2 degradation due to self-mixing

IIP2 when experiencing self-mixing. The worst case IIP2 is reduced by less than 1 dB for -30 dB attenuation between the ports. It is interesting to notice that self-mixing actually increases the IIP2 for cases 5, 2 and 4. This is probably due to the phase relationship between second-order components of different origin canceling, hence increasing the IIP2. It is difficult to predict the actual attenuation and effect of self-mixing that can be expected without performing a layout and extracting parasitic capacitances. In any case, if load tuning is used and considering the more than 20 dB increase in IIP2 it yields, self-mixing will not cause the IIP2 to fall below the +30 dBm required.

Chapter 5

Conclusion

A front-end consisting of a LNA and two mixers suitable for use in a direct-conversion receiver have been designed. The specification is reached. The ground work for implementation of mixer load tuning is laid. The results show that the load tuning technique yields good improvement in IIP2, without causing degradation of conversion gain and IIP3. The final specification of the front-end is given in table 5.

Parameter	Value	Unit
LNA gain	> 26.7	dB
LNA IIP3	-12.2	dBm
LNA spot noise figure @ 2.44G	2.5	dB
LNA current consumption	0.74	mA
Mixer conversion gain	>5.6	dB
Mixer IIP3	8.4	dB
Mixer DSB spot noise figure @ 1 MHz	24.1	dB
Mixer current consumption	2.41	mA
Front-end S_{11}	< -18.1	dB
Front-end spot noise figure @ 1 MHz	4	dB
Front-end IIP3	-19.7	dBm
Front-end IIP2	>48.3	dBm
Front-end gain	>32.3	dB
Total current consumption	7.42	mA

Table 5.1: Front-end specification

5.1 Future work

As the front-end is not optimal, future work would include the following:

- Improvement of the LNA input matching network in order to have a simultaneous noise and power match.

- Substitute the simple off-chip inductor model used in the matching network of the LNA for a higher level model.

- Improve the mixers. In order to meet the noise and linearity specifications for the mixer the current was increased as explained in 3.4.2. The load resistors then had to be reduced, causing the conversion gain to drop. The 1/f-noise of the mixer is still high, and the current use in the mixer and biasing of the transconductor is inefficient. Using a charge-injection scheme as presented in [10] and [5] show promise of improving noise performance and linearity, without sacrificing conversion gain. It should also be considered if the use of the common-source transconductor can be justified, as a differential pair is more current efficient and might perform better than an inefficiently biased common-source stage.

- Implement the IIP2 trim blocks, and study the influence of switches and non-ideal resistors. Exploring adaptive control of the load tuning based on the correlation between high IIP2 and small DC-offset would also be an interesting task.

- Layout and parasitic extraction for the complete front-end to evaluate the port-to-port attenuation.

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Appendix A

Standard deviation for threshold voltage

The variance $\sigma^2(V_{th,1})$ and $\sigma^2(V_{th,2})$ of the threshold voltages for the transistors in a nominally matched pair are independent and equal. The variance of the difference in threshold can therefore be related to the variance of the threshold V_{th} of a single transistor in the pair as [22]

$$\sigma^2(V_{th,1} - V_{th,2}) = \sigma^2(V_{th,1} + V_{th,2}) = \sigma^2(V_{th,1}) + \sigma^2(V_{th,2}) = 2\sigma^2(V_{th}). \tag{A.1}$$

The standard deviation of V_{th} is then

$$\sigma(V_{th}) = \frac{1}{\sqrt{2}}\sigma(V_{th,1} - V_{th,2}). \tag{A.2}$$

Appendix B

IIP2 trim simulation values

B.1 Shunt resistor values

The shunt resistor values for 5 and 7 bit resolution were calculated using a small Matlab script:

```
R=39644; %Resistance value of smallest resistor in IIP2 trim block

for I=1:32 %5 bit IIP2 trim block control signal
A=bitget(double(I),5:-1:1); %Convert value of
                            %control signal from double to binary
B=[1/(16*R) 1/(8*R) 1/(4*R) 1/(2*R) 1/(R)]; %Set up vector for
                                            %admittance of
                                            %5 bit IIP2 trim block
F(I)=1/(sum(A.*B));  %Turn on or off resistor chains
                     %according to control signal
                     %and calculate resistance of IIP2 trim block
R_fivebit=sort(F,'descend'); %Sort values
end

%Same as above only for 7 bit
for J=1:128
C=bitget(double(J),7:-1:1);
D=[1/(64*R) 1/(32*R) 1/(16*R) 1/(8*R) 1/(4*R) 1/(2*R) 1/(R)];
G(J)=1/(sum(C.*D));
R_sevenbit=sort(G,'descend');
end
```

The resistance values in ohms generated by the program are as follows:

5 bit:
6,343e+005 3,1715e+005 2,1143e+005 1,5858e+005 1,2686e+005 1,0572e+005 90615 79288 70478 63430 57664 52859 48793 45307 42287 39644 37312 35239 33384 31715 30205 28832 27578 26429 25372 24396 23493 22654 21873 21143 20461

7 bit:
2,5372e+006 1,2686e+006 8,4574e+005 6,343e+005 5,0744e+005 4,2287e+005 3,6246e+005 3,1715e+005 2,8191e+005 2,5372e+005 2,3066e+005 2,1143e+005 1,9517e+005 1,8123e+005 1,6915e+005 1,5858e+005 1,4925e+005 1,4096e+005 1,3354e+005 1,2686e+005 1,2082e+005 1,1533e+005 1,1031e+005 1,0572e+005 1,0149e+005 97585 93971 90615 87490 84574 81846 79288 76885 74624 72492 70478 68573 66769 65057 63430 61883 60410 59005 57664 56383 55157 53983 52859 51780 50744 49749 48793 47872 46985 46131 45307 44513 43745 43004 42287 41594 40923 40273 39644 39034 38443 37869 37312 36771 36246 35735 35239 34756 34287 33830 33384 32951 32528 32117 31715 31324 30942 30569 30205 29850 29503 29163 28832 28508 28191 27881 27578 27282 26992 26708 26429 26157 25890 25628 25372 25121 24875 24633 24396 24164 23936 23712 23493 23277 23066 22858 22654 22453 22256 22063 21873 21686 21502 21321 21143 20969 20797 20628 20461 20298 20137 19978

B.2 Worst case and random values for $vth0$

The worst case and random values of $vth0$ used for mismatch simulation are shown in table B.1. The random values are normally distributed with $\mu = 307.5$ mV and $\sigma = 1.55$ mV, and were generated using Maple.

Case	M3	M4	M5	M6
WCase	0.3106	0.3044	0.3106	0.3044
1	0.3070403291	0.3063326940	0.3079884370	0.3064596922
2	0.3068865169	0.3080534431	0.3075070705	0.3070979292
3	0.3068865169	0.3080534431	0.3075070705	0.3070979292
4	0.3053830005	0.3067220789	0.3077021789	0.3068757870
5	0.3062998726	0.3077661748	0.3051197645	0.3091855622
6	0.3072640538	0.3074782083	0.3065455108	0.3063468386

Table B.1: Worst case and random values for $vth0$

Appendix C

Spice code

C.1 Intercept point measurements

Code for measurement of front-end IIP2:

```
*IIP2
.EXTRACT FSST LABEL=IM2_f2_f1 YVAL(PDBM(R_baseband),fund1-fund3)-
+ YVAL(PDBM(R_baseband),fund2-fund1)
.EXTRACT FSST LABEL=IIP2_f2_f1  MEAS(IM2_f2_f1) + YVAL(PDBM(V1), fund1)
```

Code for measurement of mixer and front-end IIP3:

```
*IIP3
.EXTRACT FSST LABEL=IM3_2f2_f1 YVAL(PDBM(R_baseband),fund1-fund3)-
+ YVAL(PDBM(R_baseband),2*fund2-fund1-fund3)
.EXTRACT FSST LABEL=IIP3_2f2_f1 MEAS(IM3_2f2_f1)/2 + YVAL(PDBM(V1), fund1)
```

Code for measurement of LNA IIP3:

```
.EXTRACT FSST LABEL=IM3 YVAL(PDBM(R_LNA),fund1)-
+ YVAL(PDBM(R_LNA),2*fund2-fund1)
.EXTRACT FSST LABEL=IIP3 MEAS(IM3)/2 + YVAL(PDBM(V1),fund1)
```

Appendix D

NIS0603 datasheet excerpt

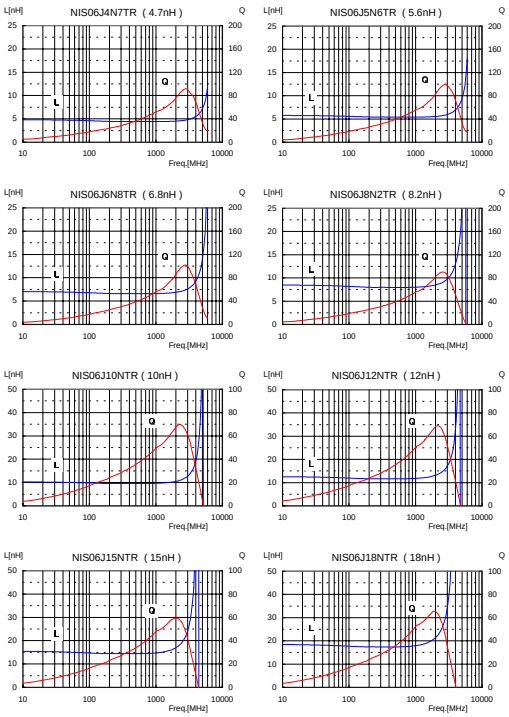

Figure D.1: NIS0603 Quality factor (Q) & inductance (L) over frequency comparison

Appendix E

Schematics

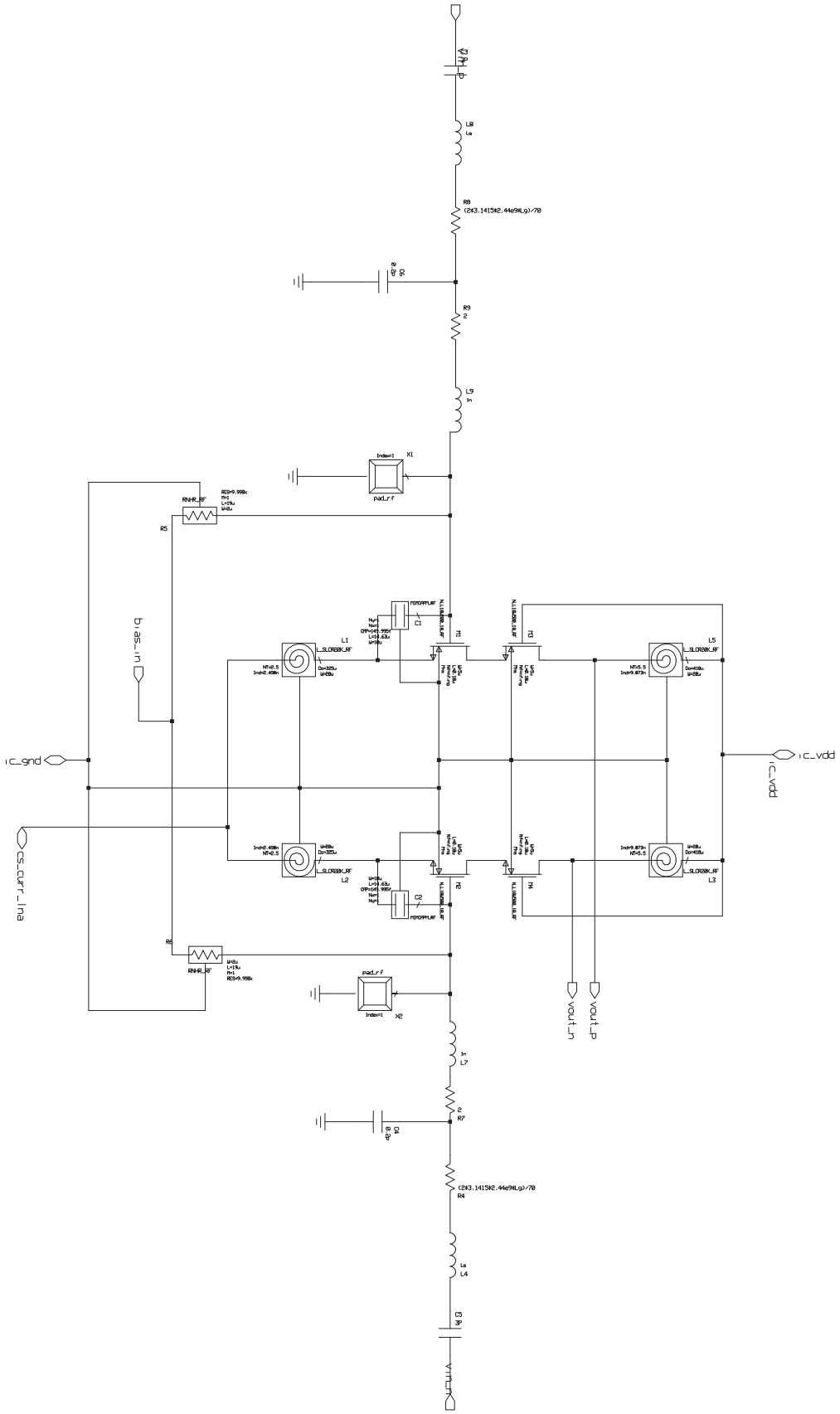

Figure E.1: LNA schematic

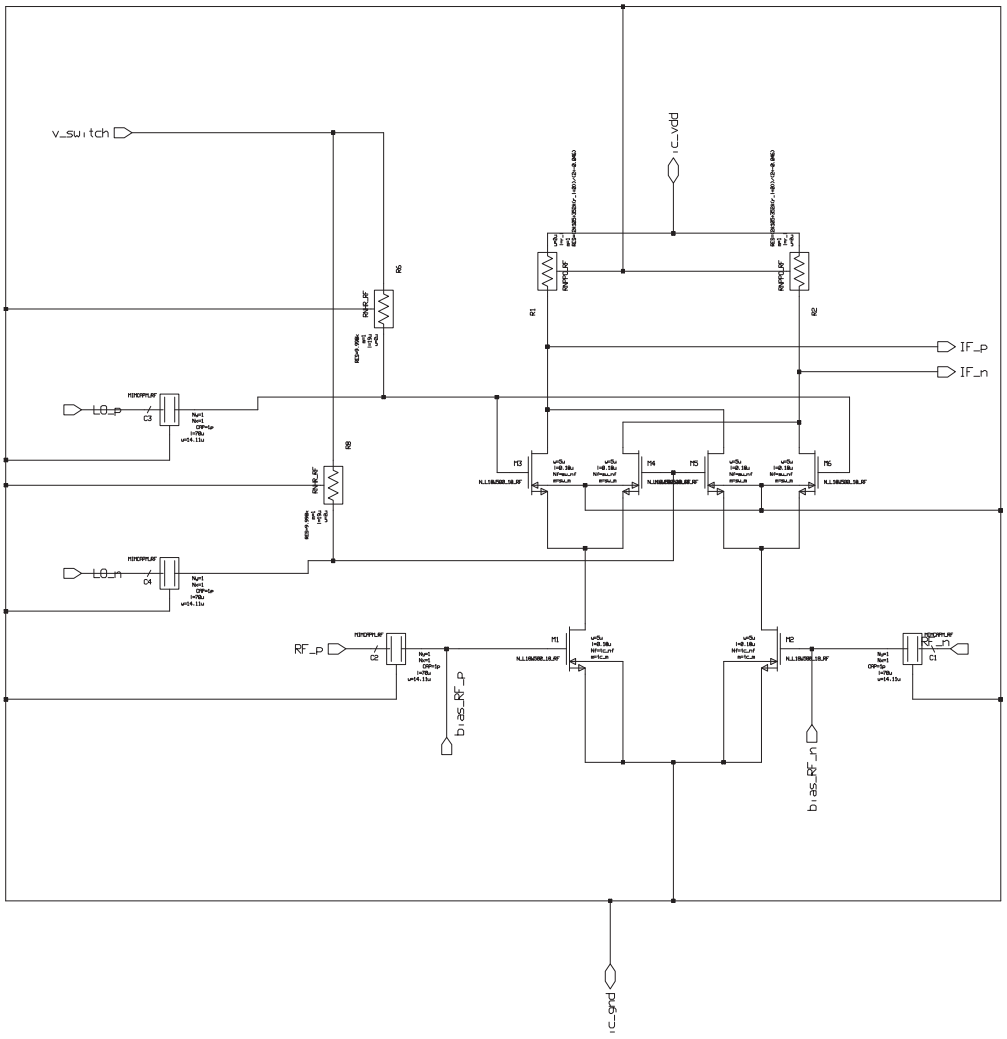

Figure E.2: Mixer schematic

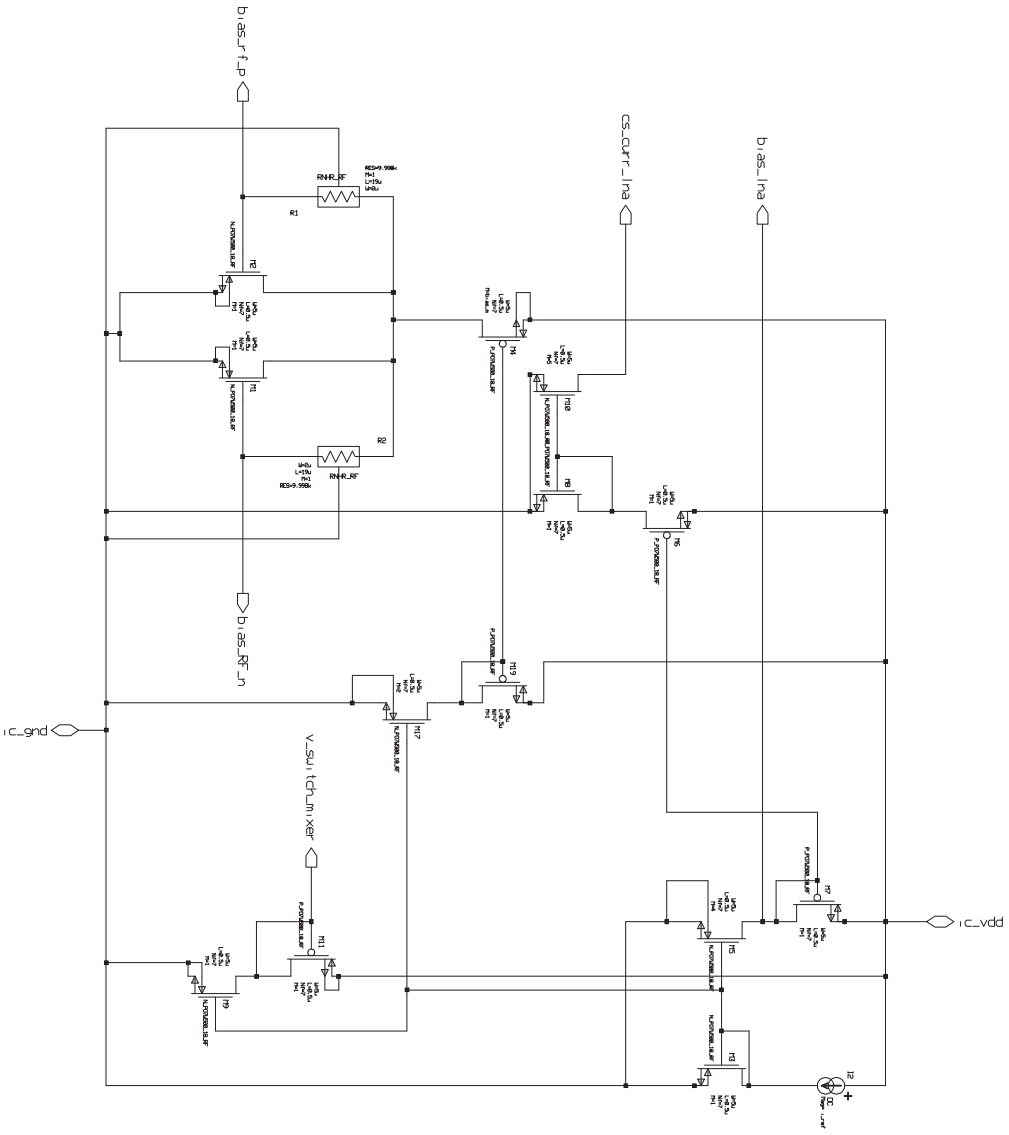

Figure E.3: Bias schematic

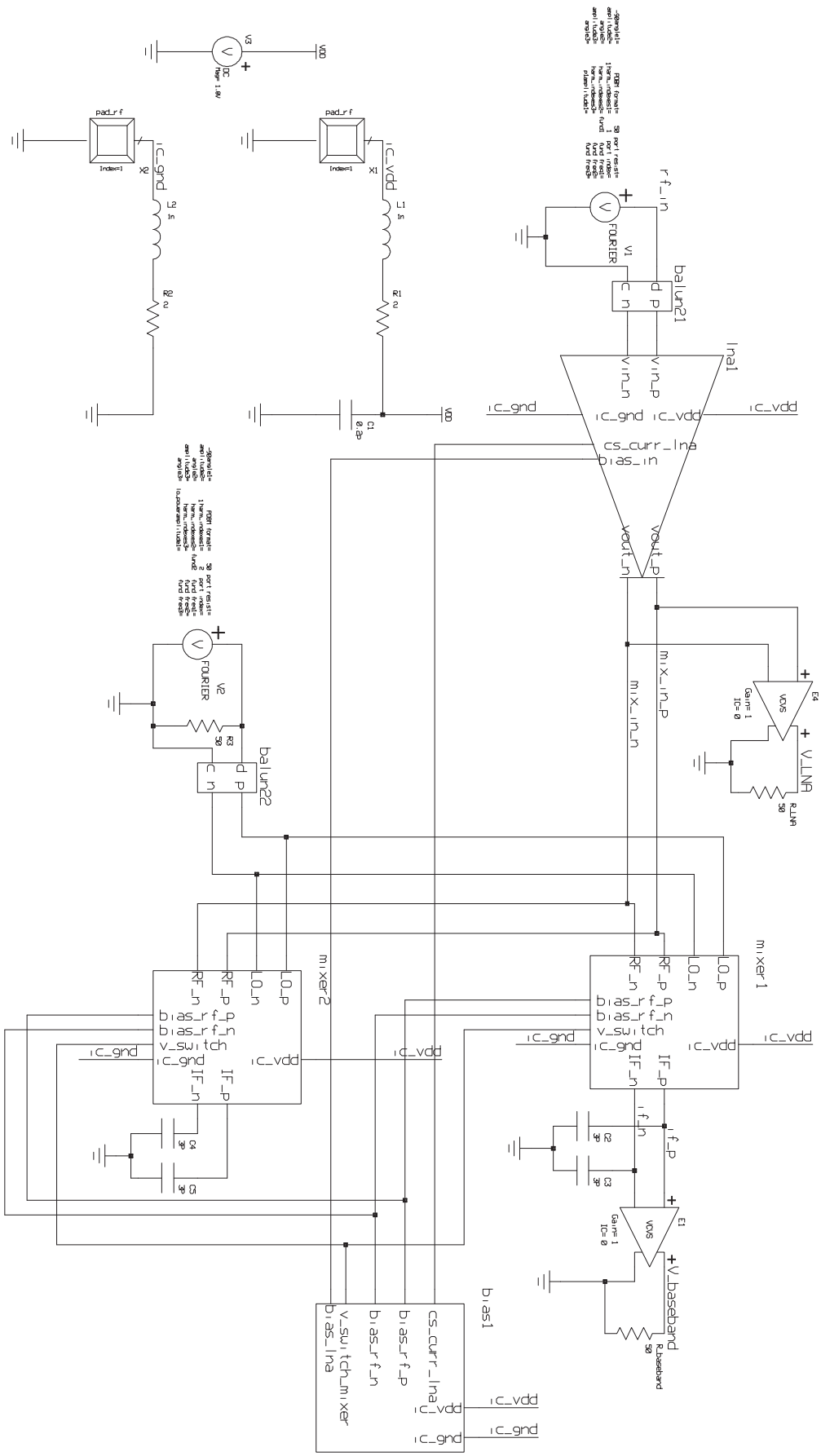

Figure E.4: Front-end testbench schematic

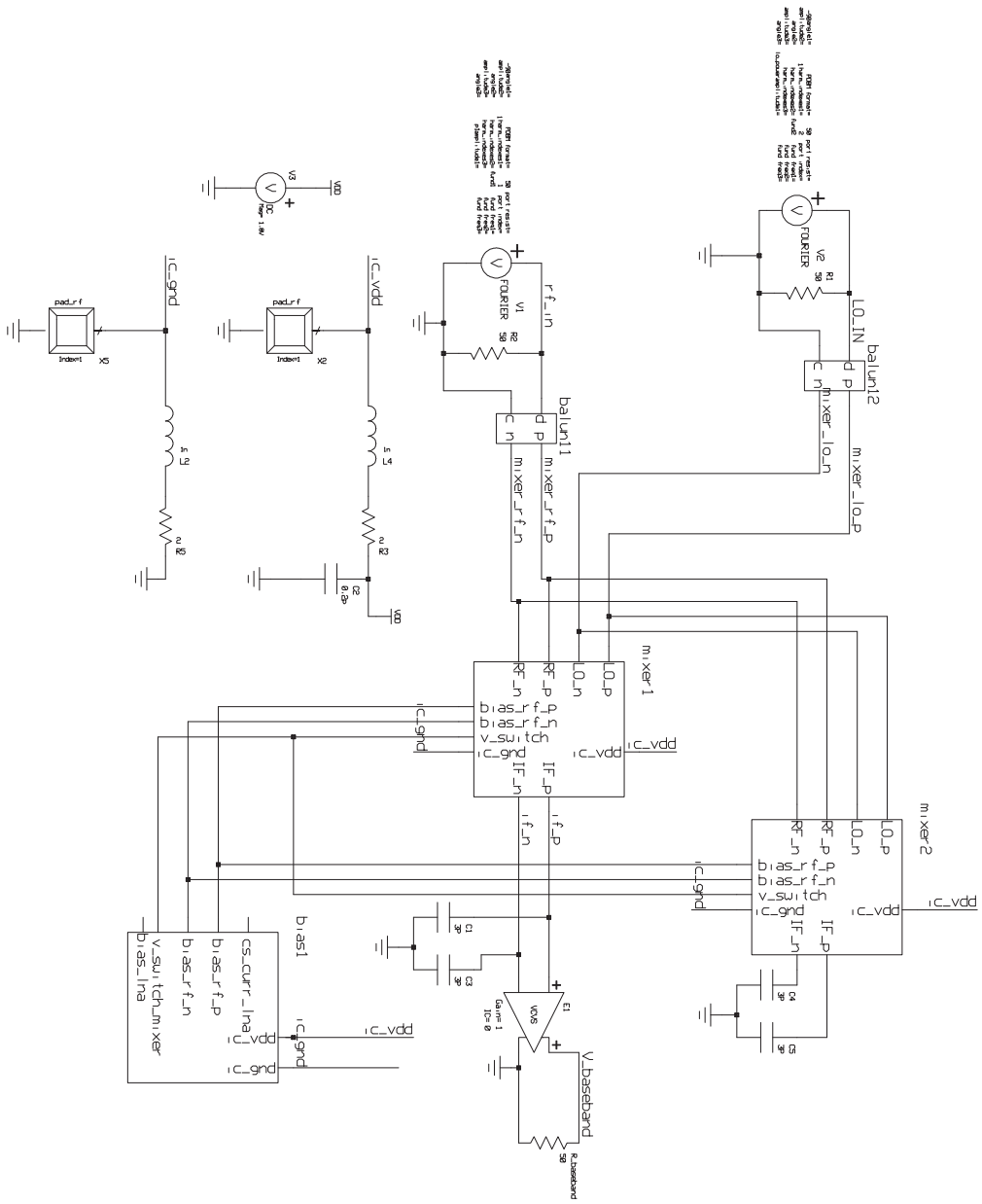

Figure E.5: Mixer testbench schematic

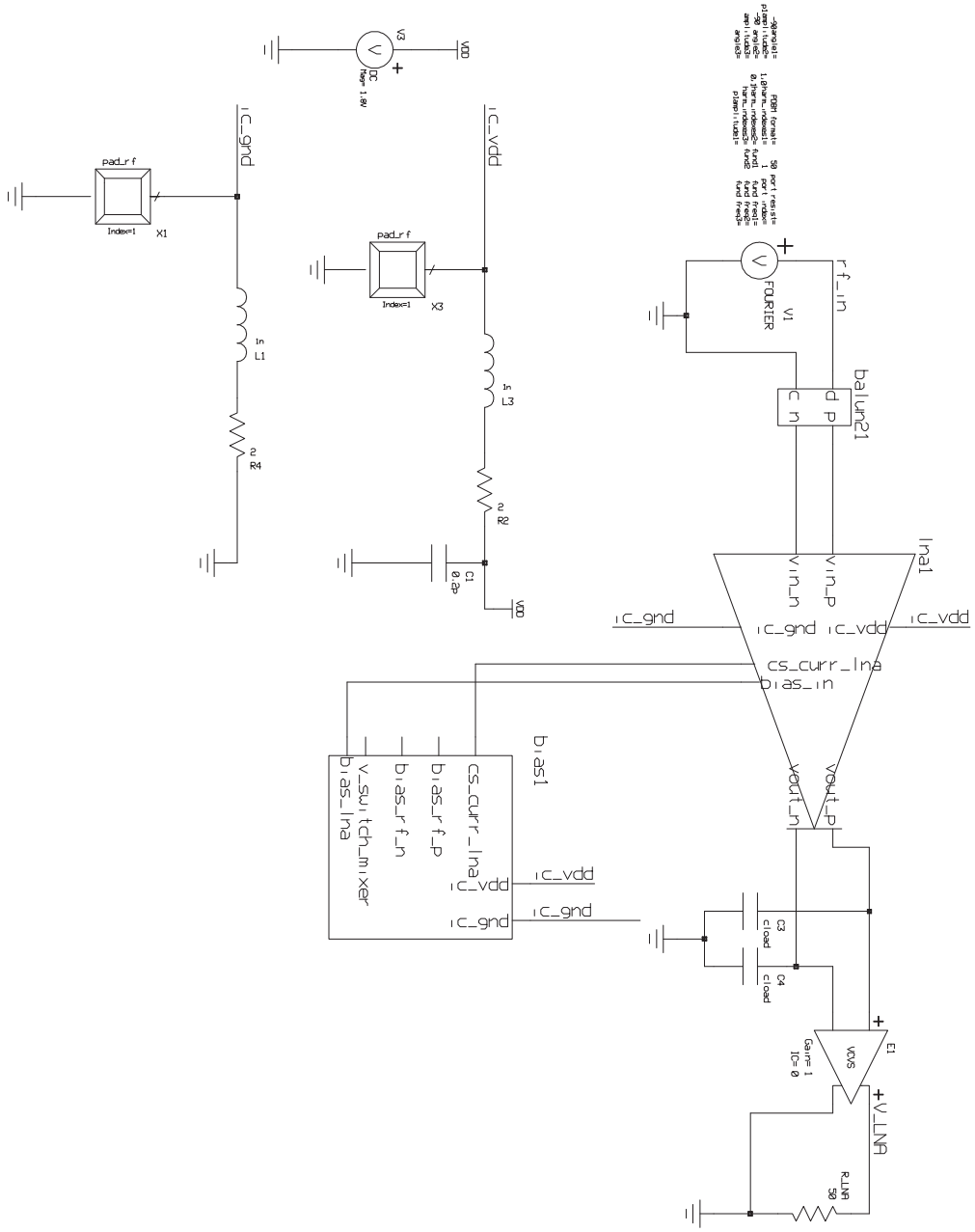

Figure E.6: LNA testbench schematic