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Comparator-Based Switched-Capacitor Integrator for use in Delta-Sigma Modulator

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Problem Description

New process technologies introduce challenges that must be overcome when re-using known design topologies.

One of the most important components in a switched-capacitor Delta Sigma ADC is the input integrator, where the accuracy of the traditional opamp-based integrators are dependent on high gain.

An integrator that tries to avoid or reduce the disadvantages that modern process technologies introduce for the input integrator should be designed in a 90nm process. Layout of the design is not essential, but can be done if there is time.

Assignment given: 27. January 2009
Supervisor: Trond Ytterdal, IET

Comparator-Based Switched-Capacitor Integrator for use in Delta-Sigma Modulator

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Abstract

A comparator-based switched capacitor integrator for use in a Delta Sigma ADC has been designed. Basic theory about comparator-based circuits has been presented and design equations have been developed.

The integrator had a targeted performance of a bandwidth of 1.5MHz with a SNR of 80dB. Due to the lack of a complete modulator feedback system, the integrator was simulated in open-loop. For the integrator not to saturate in open-loop, an overshoot calibration circuit was enabled during the simulation. This resulted in a severe deterioration of the integrated signal. The results are therefore significantly lower than expected, with a SNR of about 39dB but can be expected to be better in a closed-loop simulation. The power consumption of the implemented modules is 0.43mW. However, this is without several modules which were implemented as ideal.

Contents

Chapter 1

Introduction

As CMOS technology continue to scale down to smaller geometries, designing low power, high performance analog circuits are becoming more difficult due to reduced transistor output impedance, lowered supply voltage and increased leakage. This is a major drawback in designing operational amplifiers which is an important building block in many analog circuits. At the same time, technology scaling introduces higher unity gain frequency and lowered parasitic capacitances in transistors, opening up new possibilities for CMOS.

The objective of this work is to explore a new method called comparator-based switched-capacitor circuit (CBSC) for use in switched-capacitor Delta-Sigma Modulators ($\Delta\Sigma$) by designing an input integrator for the $\Delta\Sigma$.

1.1 Motivation

The introduction of CBSC [1] is a possible way to further allow technology scaling. With opamp based circuits, the accuracy of the circuit is very dependent of the open loop gain of the amplifier. It is possible to compensate for some of this by using cascoded devices, cascading several stages, multipath Miller compensation and so on. This again introduces new issues such as increased power consumption or stability problems.

CBSC has benefits which coincides well with technology scaling. Instead of forcing the input nodes to the same voltage, the charge transfer process is performed by current sources, while the virtual ground condition is detected by a comparator instead of being forced by opamps. This makes it possible to also take advantage of the increased speed in modern technologies to create high-speed comparators. Also, stability issues are eliminated with the removal of the opamp.

1.2 Prior work

After the publication of CBSC, several designs have been introduced. The first silicon-proven design is detailed in [2], with [3] shortly thereafter. Later, differential implementations was introduced [4][5][6]. The best ADC performance in time of writing was presented in [7].

The CBSC method is also applicable to other circuits. [8] presented a $\Delta\Sigma$ modulator using CBSC, while the technique is also explored in switched capacitor filters[9]. Recently, the first silicon-proven CBSC $\Delta\Sigma$ ADC was published [10].

Chapter 2

Delta-Sigma Modulation

This chapter will cover the basics of $\Delta\Sigma$ and examine the importance of the input integrator in the system in order to have a set of design equations before implementation. The focus will be on switched capacitor $\Delta\Sigma$, as the method of CBSC is not applicable for continuous-time modulators.

2.1 Principles of Delta-Sigma Modulators

The $\Delta\Sigma$ topology used in ADCs is a feedback system which, together with oversampling above the Nyquist frequency, is used to shape the quantization noise of the converter out of the signal band, making it possible to filter out digitally after quantization [11]. An antialiasing filter in front of the modulator and a digital decimator to reduce the sampling frequency after the noise filtering is also needed. Figure 2.1 shows a general block diagram of a $\Delta\Sigma$. The use of oversampling and noise shaping allows for a tradeoff between speed and accuracy, relaxing the requirements for analog circuitry.

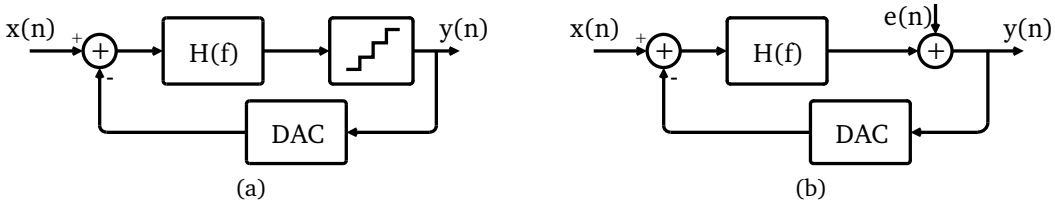


Figure 2.1: A general model of a $\Delta\Sigma$ modulator(a) and its linear model, showing added quantization noise(b)

The relationship in the z domain between the output Y(z), the input X(z) and the added quantization noise E(z) can be written as:

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \tag{2.1}$$

where the signal and noise transfer functions S_{TF} and N_{TF} can be found as[12]:

$$\begin{aligned} S_{TF} &= \frac{H(z)}{1+H(z)} \\ N_{TF} &= \frac{1}{1+H(z)} \end{aligned} \tag{2.2}$$

From these equations one can see that high gain is wanted from the loop filter H(z) inside the signal band, while low gain is necessary outside the band to shape the quantization noise.

2.1.1 Ideal $\Delta\Sigma$ Modulators

An ideal $\Delta\Sigma$ modulator, as shown in Figure 2.1, can be described in many different ways, depending on frequency band and topology. A general n-th order low pass modulator can be described with the following signal and noise transfer functions[12]:

$$\begin{aligned} STF(z) &= z^{-n} \\ NTF(z) &= (1-z^{-1})^n \end{aligned} \tag{2.3}$$

Transforming to the frequency plane with $z = e^{j\omega T} = e^{\frac{j2\pi f}{f_s}}$ and taking the absolute value of (2.3), the following transfer functions is found:

$$\begin{aligned} |STF(z)| &= 1 \\ |NTF(z)| &= \left(2sin(\frac{\pi f}{f_s})\right)^n \end{aligned} \tag{2.4}$$

Here, f is the signal frequency and f_s is the sampling frequency. A plot of $|NTF(z)|$ is shown in Figure 2.2.

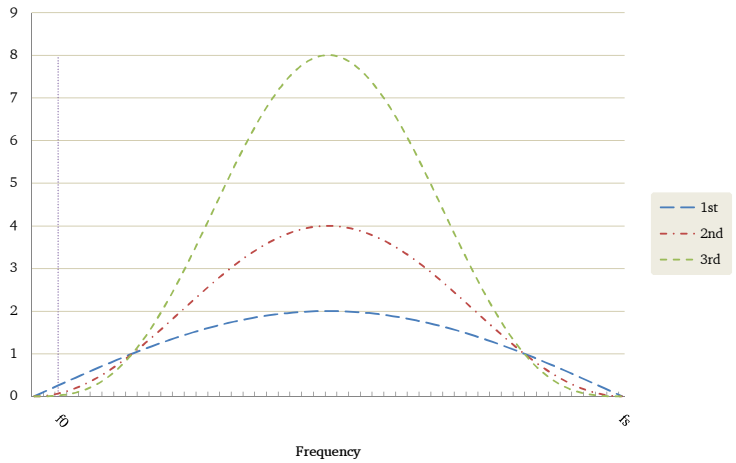


Figure 2.2: Noise transfer function for ideal $\Delta\Sigma$ modulator for n=1-3

2.1.2 Performance metrics

The most important performance parameters for accuracy are presented here to have a clear overview of their meaning when discussing them later on[12][13].

- **Signal to Noise Ratio:** The SNR of a $\Delta\Sigma$ is defined as the signal power divided by the noise power when measured at the output of the converter. The maximum achievable SNR of the converter is called the peak signal to noise ratio (SNR_p). An expression for the modulator SNR can be found as[13]:

$$SNR = \frac{3\pi}{2} \cdot (2^B - 1)^2 \cdot (2n+1) \cdot \left(\frac{OSR}{\pi}\right)^{2n+1} \tag{2.5}$$

  Here, B is the number of quantization bits of a n^{th} order modulator. However, this does not account for the coefficients in the modulator. Normally, the coefficients are lower than unity, leading to a SNR level lower than the ideal.

- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power and the power of both the distortion and the noise. This will always be a lower number then the SNR. Maximum SNDR is denoted as $SNDR_p$.

- **Effective Number of Bits:** ENOB is a metric of the accuracy of the converter and an ideal converter would have this number of bits to get the same performance. Assuming white quantization noise and a sinusoidal input signal, ENOB can be found as[11]:

$$ENOB = \frac{SNDR_{p,dB} - 1.76}{6.02} \tag{2.6}$$

- **Overload level:** The OL of a converter is the relative input amplitude where the SNR has decreased 3dB below SNR_p because the modulator somehow saturates and becomes unstable.

2.1.3 Critical building blocks

Input integrator

As the first component in the $\Delta\Sigma$ modulator, the input integrator should be discussed. As it operates directly on the input signal, this integrator dominates the total performance of the modulator. A simple schematic is shown for a SC opamp-based integrator in Figure 3.1.

What also is important to consider, is that the noise contribution of the integrators inside the feedback loop is also noise shaped. An approximation used for the total input referred integrator noise power $N_{in,tot}$ can be derived as[12, p.145]:

$$N_{in,tot} = \sum_{i=1}^{n} \frac{N_{in,i}}{\pi(2i-1)\prod_{j=1}^{i-1} a_j^2} \cdot \left(\frac{\pi}{OSR}\right)^{2i-1} \tag{2.7}$$

Here, i is the i^{th} integrator, $N_{in,i}$ is the noise power of each separate integrator, a_j are the coefficients before the i^{th} integrator and OSR is the oversampling ratio.

This reduces the input referred noise of the input integrator by $\frac{1}{OSR}$ compared to a standalone integrator, reducing the requirements for the analog circuitry significantly. For the 2nd integrator, the input referred noise is reduced by $\frac{\pi^2}{3a_1 OSR^3}$. This shows that the input integrator is highly important for oversampling $\Delta\Sigma$ modulators, while the requirements can be reduced for the following.

DAC

The digital to analog converter (DAC) in the feedback loop is also, together with the input integrator, a critical component in the modulator. This is because it feeds back a signal directly to the modulator input, and any noise or distortion from the DAC can not be distinguished from the signal.

Many modulators use a 1 bit DAC, as these are inherently linear since only one step exists. If a multibit DAC is used, the accuracy of this has to be as good as the total accuracy requirements in the modulator.

Also, nonlinearities such as capacitor mismatch, voltage reference nonidealites, charge injection and clock feedthrough contribute to accuracy degradation of the DAC. For high accuracy DACs, many Dynamic Element Matching techniques exist to reduce the matching requirements of the DAC[12].

Sampling switches

In modern process technologies, the supply voltage is reduced to as low as 1.0-1.3V. This leads to a very low gate overdrive voltage which makes the switch resistance high. Using transmission gates are also difficult, because the threshold voltages allow very little signal swing before one of them goes into subthreshold operation, giving a high resistance peak near $\frac{V_{DD}}{2}$, where the differential common mode voltage is often placed.

This makes the switch highly nonlinear, causing harmonic distortion. The two most common ways to overcome this problem is to either use clock boosting (boost clock voltage higher than V_{DD} by using a charge pump) or use a bootstrapping circuit as shown in Figure 2.3.

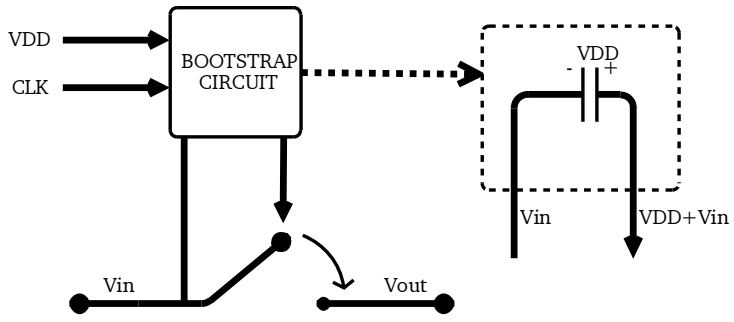


Figure 2.3: Bootstrapped switch

A bootstrapping circuit normally works by charging a capacitor to V_{DD} in the **off** period of a sample-and-hold operation so that when the sample phase begins, the capacitor is connected

between the input and the gate, keeping the gate-source voltage of the switch constant. However, to use techniques like this require a focus on reliability, as driving oxide voltages high above what the process allows can easily destroy the circuit.

2.2 Switched-Capacitor Requirements

2.2.1 Required Sampling Capacitance

Thermal noise can easily limit the performance of a SC circuit. The mean squared noise of a RC equivalent circuit can be found as $\overline{V_n^2} = \frac{k_B T}{C}$ [11]. For a differential SC integrator there is a sampling switch on each input which can be seen as a noisy resistor. As thermal noise is white and therefore uncorrelated, this will lead to a total thermal noise power of $\frac{2k_B T}{C}$. As shown in (2.7), noise from the first integrator is also suppressed by $\frac{1}{OSR}$. Thus, the total input referred thermal noise from the first integrator can be found as:

$$P_{no,diff} = \frac{2k_B T}{C \cdot OSR} \tag{2.8}$$

Assuming the input signal is sinusoidal and its differential amplitude limited to $V_{DD} \cdot OL$, where OL is a overloading factor to ensure modulator stability, the signal RMS power is found as:

$$\begin{aligned} P_{sig,diff} &= \left(\frac{1}{\sqrt{2}}\left(OL \cdot V_{DD}\right)\right)^2 \\ &= \frac{\left(V_{DD} \cdot OL\right)^2}{2} \end{aligned} \tag{2.9}$$

For a given SNR (in dB), the minimum sampling capacitor size can be found:

$$\begin{aligned} SNR &= 10log\left(\frac{\left(V_{DD} \cdot OL\right)^2 \cdot OSR \cdot C_S}{4k_B T}\right) \\ C_S &= \frac{4k_B T \cdot 10^{SNR_{dB}/10}}{OSR \cdot \left(V_{DD} \cdot OL\right)^2} \end{aligned} \tag{2.10}$$

2.2.2 Switch sizing

Switches are also an important source of nonidealities in SC circuits, especially in low-voltage circuits where the gate overdrive voltage is limited. The switch gate area should be small to minimize charge injection and clock feedtrough from the gate capacitor, but at the same time the on-resistance should be small enough to allow the capacitor voltages to settle within a certain error.

The output voltage across the sampling capacitors in Fig. 3.1 at the sampling time will settle exponentially dependent on the two time constants $\tau_1 = R_{S1}C1$ and $\tau_2 = R_{S3}C1$, with $\tau_{tot} = \tau_1 + \tau_2$ [14].

Assuming differential signals, the absolute voltage across the sampling capacitors at the end of phase $\Phi 1$ is $(V_{IN} - V_\epsilon) - (-V_{IN} + V_\epsilon) = 2V_{IN} - 2V_\epsilon$, which says that the absolute settling error for differential signals is twice the single ended. The relative settling error is the same though, as the signal amplitude is doubled.

As settling occurs quickly compared to the signal frequency due to oversampling, it is assumed that V_{IN} is a constant at the sampling time.

The worst case settling is found when the differential input signal has its maximum, which for a mid-rail common-mode voltage is at $V_{IN,diff} = OL \cdot V_{DD}$. For a given Signal-To-Distortion ratio, the allowed error can be found:

$$\begin{aligned} SDR &= 20log\left(\frac{OL \cdot V_{DD}}{2V_\epsilon}\right) \\ V_\epsilon &= \frac{OL \cdot V_{DD}}{2 \cdot 10^{SDR_{dB}/20}} \end{aligned} \tag{2.11}$$

Denoting the non-overlapping clocks duty cycle as α and f_s as the sampling frequency the total time allowed for settling is:

$$t_{sample} = \frac{\alpha}{f_s} \tag{2.12}$$

The allowed time constant τ_{tot} for the worst case $(OL \cdot V_{DD})$ can then be found as

$$\begin{aligned} 2V_\epsilon &= \frac{OL \cdot V_{DD}}{2} e^{\frac{-t_{sample}}{\tau_{tot}}} \\ \tau_{tot} &= \frac{t_{sample}}{ln\left(\frac{OL \cdot V_{DD}}{2V_\epsilon}\right)} \end{aligned} \tag{2.13}$$

which leads to an expression for the maximum allowed switch resistance for the two sampling switches:

$$R_{S1} + R_{S3} = \frac{1}{C1} \cdot \tau_{tot} \tag{2.14}$$

2.2.3 Jitter requirements

For high accuracy circuits at high frequencies, accurate switch on/off times are needed. An uncertainty in sampling time will cause a sampling error in the integrator. The SNR due to this jitter can be found as [12, ch3.2]:

$$\begin{aligned} SNR_{jitter} &= 10log\frac{OSR^3}{(\pi f_s \sigma_{\Delta T})^2} \\ &\Leftrightarrow \\ \sigma_{\Delta T} &= \sqrt{\frac{OSR^3}{(\pi f_s)^2 \cdot 10^{SNR_{jitter}/10}}} \end{aligned} \tag{2.15}$$

Here, OSR is the oversampling ratio, f_s is the sampling frequency and $\sigma_{\Delta T}$ is the standard deviation of the sampling uncertainty.

Chapter 3

Opamp based switched capacitor circuits

Opamp-based switched capacitor circuits are a fundamental building block of most discrete-time dataconverters. A basic opamp-based integrator is shown in Figure 3.1.

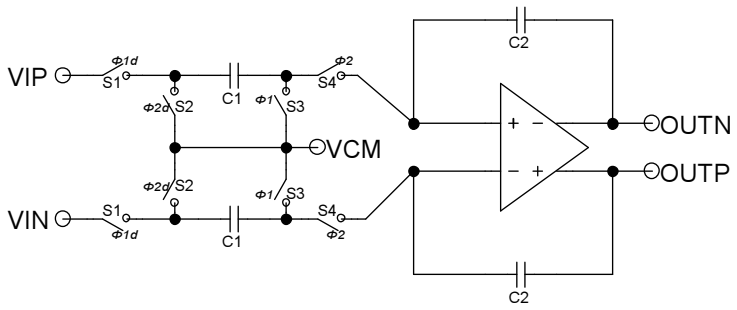


Figure 3.1: Opamp-based differential integrator

The sampling phase charges capacitors C1 to the input voltage, before the charge transfer phase where the opamp inputs are forced to virtual ground, resulting in a charge transfer on C_2 to discharge C_1. Its ideal transfer function when the feedback voltage $V_{ref} = V_{cm}$ is given as[15, p.337]:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C1}{C2}\frac{z^{-1/2}}{1 - z^{-1}} \tag{3.1}$$

Accuracy limitations specific to opamp based switched capacitor circuits are mainly due to finite opamp DC gain, bandwidth, noise and slew rate limitations. These effects cause both phase errors and gain errors in the transfer function.

A finite DC gain A will cause the inputs of the opamp to not be at virtual ground but instead at V_{out}/A. The effect of this leads to the transfer function[15, p.350]:

$$H(z) = \frac{C1 \cdot z^{-1/2}}{C2}\frac{1 - (1/A - C_1/(AC_2))}{1 - (1 - C_1/(AC_2))\, z^{-1}} \tag{3.2}$$

Finite opamp bandwidth B will also lead to changes in the transfer function:

$$H(z) = \frac{C1 \cdot z^{-1/2}}{C2} \frac{(1-\epsilon) + z^{-1}\epsilon C_2/(C_1+C_2)}{1-z^1} \tag{3.3}$$

where $\epsilon = e^{-\pi B/f_s}$.

Another effect that should be mentioned is incomplete settling of the outputs. The magnitude of the settling error will often vary with the previous output voltage and can generate harmonic distortion. The analysis of the total transfer function when including all non-ideal effects can be extremely complex and is not of much practical use.

Modern nano-scale technologies introduce several issues that can decrease accuracy of opamp-based circuits, among them reduced transistor intrinsic gain and reduced linearity due to a lower supply voltage [16]. There are several techniques to overcome many of these problems, but most proposed solutions impose some kind of tradeoff such as higher power consumption or reduced speed. Therefore, CBSC is introduced as a way to try to overcome some of these issues.

Chapter 4

Comparator-Based Switched Capacitor Circuits

This section will focus on theory needed to implement an integrator utilizing CBSC. Current sources are used to charge the capacitive network instead of the opamp outputs and a comparator is used to detect virtual ground at the inputs instead of forcing the inputs to virtual ground as opamps do.

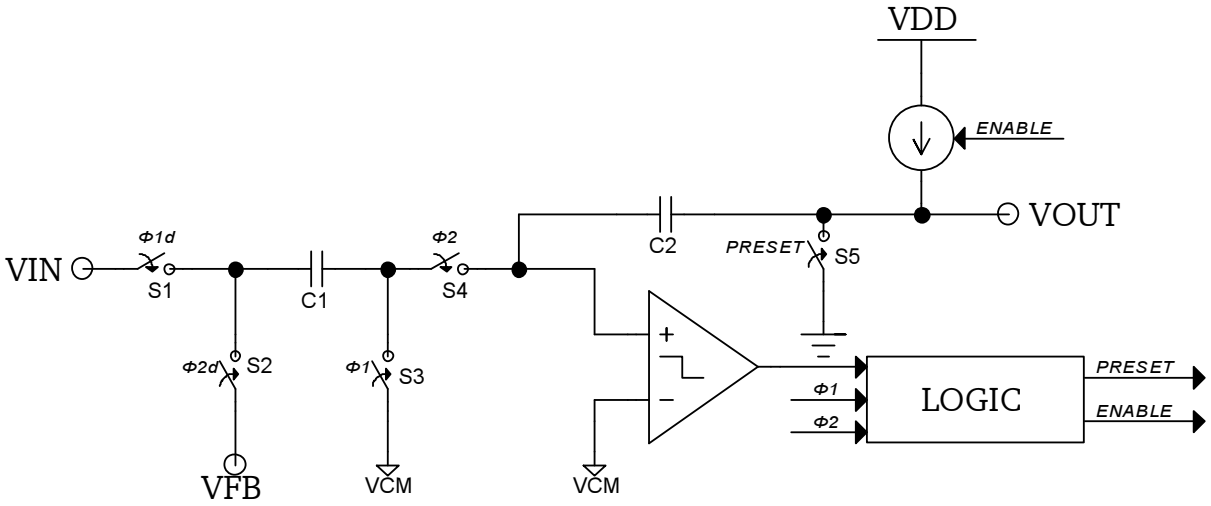


Figure 4.1: Schematic of CBSC integrator. Integrator is shown single-ended for simplicity.

A simplified schematic of a CBSC integrator is shown in Figure 4.1. The sampling phase ϕ_1 is equal as for opamp based circuits. In the charge transfer phase ϕ_2, the output is first preset to ground to ensure that the voltage on the comparator input is pushed below V_{CM} to ensure that it will toggle in the charge transfer phase(See Figure 4.2b for timing diagram). This also makes it possible to have asymmetrical gain in the comparator to make it toggle faster in one direction, as the direction of the toggling is already known.

The output voltage during the different phases are shown in Figure 4.2a. It is shown in Appendix A that a proper integration operation is performed, even though the output is preset to a fixed value.

For any SC circuit, it is not important how the correct output voltage is established at the output.

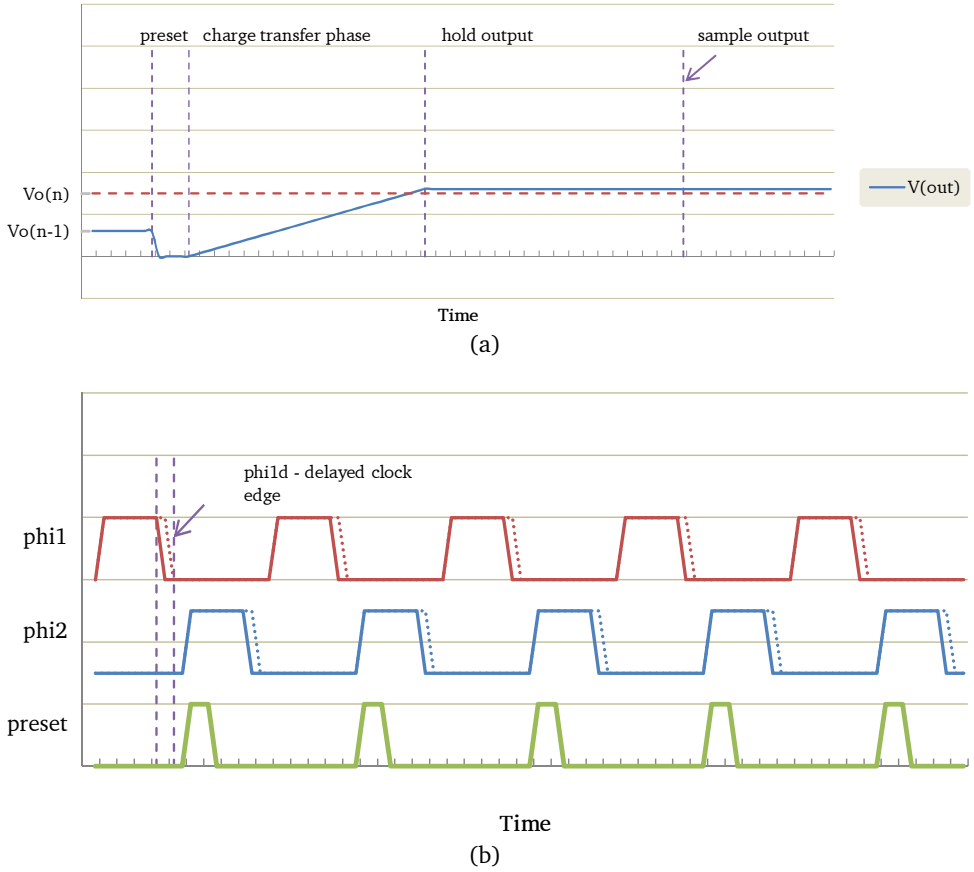


Figure 4.2: Output voltage settling of CBSC integrator (a) and CBSC clock phases (b). The phases are exaggerated compared to implementation.

In the CBSC case, the output voltage increases more or less linearly to the correct output voltage since a current source is charging a capacitor. However, as seen in Figure 4.2a, there will be a deviation on V(out) from the ideal Vo(n) due to a finite delay through the comparator and the logic generating control signals.

4.1 Noise in CBSC circuits

Noise in CMOS circuits are often analyzed by assuming that the circuits are in steady-state. Since CBSC circuits use a comparator, the circuits are not always in steady-state, and noise are also added during the transients [17]. Therefore, it is argued that a nonstationary noise analysis is necessary. An extensive analysis of the CBSC noise properties can be found in [17].

Due to the periodic sampling the noise is also filtered and aliased. A method for the periodic filtering of sampling circuits is also presented and applied to the CBSC pipeline ADC presented in [2]. The measurements of total input referred noise shows quite good correspondence with theoretical results, and the apparent dominating noise sources are estimated to be folded flicker noise from the preamplifier in the comparator at 42.8% of the total noise, preamp thermal noise at 28.6% and input sampling noise at 12.6%.

Therefore, controlling the noise in the comparator seems to be critical for high performance

CBSC circuits.

4.2 CBSC components and non-idealities

4.2.1 Switches

Switches in the sampling network of a CBSC sampling network have the same way of operating as for an opamp-based SC network. The largest problem for switches, specially for low-voltage circuits, is a signal dependent on-resistance. Switches operate in the linear region, giving a on-resistance of approximately:

$$\begin{aligned} i_D &= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn}) \cdot V_{DS} \\ r_{on} &= \frac{V_{DS}}{i_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})} \end{aligned} \tag{4.1}$$

With a signal applied to the MOSFET source, this gives rise to harmonic distortion of the input signal. Methods to reduce this are as mentioned using transmission ports, clock boosting or switch bootstrapping. Bootstrapping is the only way to completely avoid signal dependent on-resistance.

Other non-idealities are clock feedthrough and charge injection. Assuming a total switch gate capacitance C_G, the charge being fed through from the switch (distributed to source, drain and substrate) is given as the total gate capacitance times the voltage step on the gate, which is usually V_{DD}.

$$Q_{clkfeedthrough} = C_G \cdot V_{DD} \tag{4.2}$$

Here, V_{DD} is the gate clock voltage. The switch gate capacitance is proportional to oxide capacitance per area (C_{ox}) and the transistor gate area $W \cdot L$.

Charge injection is another problem that needs to be addressed for high-accuracy circuits. Before a switch is shut off, the total charge in the channel can be approximated as:

$$Q = C_{ox} W L \cdot (V_{GS} - V_T) = C_{ox} W L \cdot (V_{clk} - V_{in} - V_T) \tag{4.3}$$

A common approximation is that half of the charge is distributed to source and drain respecively [11]. However, as the impedance on each side of the switch is different and the clock fall time is finite, this is not entirely correct.

Both equations above show that the switch area must be minimized to reduce the non-idealities of switching. To also remove the signal dependent part of the charge injection, V_{GS} must not be dependent on the input signal, something which is also achieved by bootstrapping.

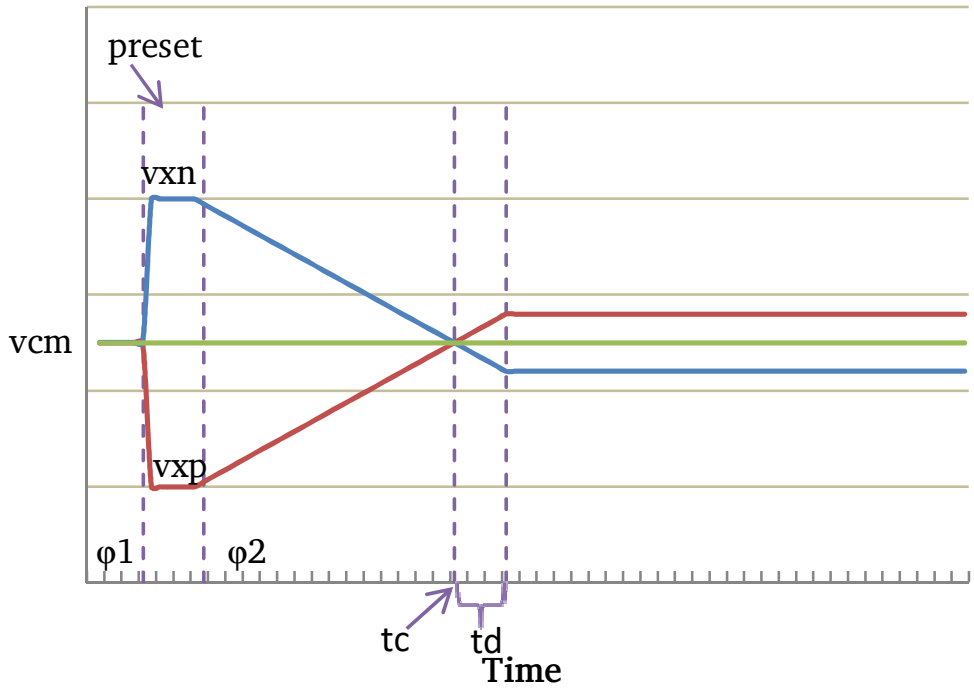


Figure 4.3: CBSC Comparator input voltages during charge transfer

4.2.2 Comparator

The comparator's task in a CBSC circuit is to detect the crossing time of the inputs to turn off the current sources in order to have a correct charge transfer. In Figure 4.3, the ideal comparator toggling time would be so that the current sources and sampling switches turned off at t_c. In reality, there is always a delay from when the inputs cross until the current sources turn off, denoted as t_d. This creates a overshoot that makes the output deviate from the ideal, as seen in Figure 4.2a.

For a pipelined ADC, where CBSC is most commonly used, this creates a DC offset which is propagated through the different stages. This reduces the possible dynamic range of the ADC, limiting performance.

For an integrator, the overshoot due to this delay results in a DC component being added to the output for every sample. As a standalone integrator, it will quickly go into saturation if this is not compensated for. When being used in a $\Delta\Sigma$ modulator, the feedback will compensate for this if it is not too large. DC offset on the input integrator is seen directly on the modulator output, thereby limiting the dynamic range of the modulator.

Therefore, the comparator should have an inherent offset to reduce overshoot or else techniques to remove or calibrate the overshoot are needed.

Several ways of detecting the crossing time have been suggested. Besides the most obvious by simply using a comparator, other topologies have also been designed. A dynamic zero-crossing detector was published[3] which consumes no static power, but the disadvantage of this is that it can not be extended to a fully differential implementation. Another silicon-proven zero-crossing detector is presented in [5], where a cascade of two preampliers connects to inverters to implement the zero-crossing operation.

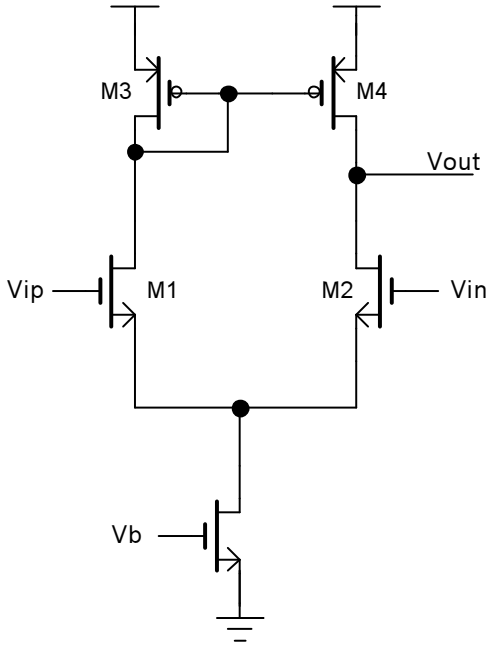


Figure 4.4: Example of preamplifier used in comparator

Preamplifier noise summary

For most threshold-detecting devices, a preamplifier is used to increase the sensitivity of the device and protect the inputs of the device from the noise occuring when a following positive feedback stage switches (kickback) [18].

The output noise from the preamplifier will cause jitter on the switching time of the following threshold detecting device [17]. Hysteresis can also be added to reject some of the input-referred noise [18]. This is achieved by using a positive feedback circuit, which also increases speed by increasing the effective gain.

The transconductance preamplifier, shown in Figure 4.4, is a common building block in differential CMOS circuits. Modeling the amplifier as a single-pole system with the output node as the dominant pole, the preamplifier's gain A_0 and time constant τ_o can be found as:

$$\begin{aligned} A_0 &= g_m \cdot r_{out} \\ \tau_o &= r_{out} \cdot C_L \end{aligned} \tag{4.4}$$

Noise from subsequent circuits in the comparator are reduced by the gain of the preamplifier and is therefore less important for the total noise contribution.

The input referred noise of the preamplifier when used in a CBSC system is derived as [17]:

$$\overline{v_n^2}(t_i) = 4k_B T R_n \frac{1}{4\tau_0} coth\left(\frac{t_i}{2\tau_0}\right) u(t_i) \tag{4.5}$$

The time t_i is the average time when the preamplifier crosses the following decision circuit threshold(See Figure 4.5) and adds timing jitter to the crossing. R_n is an equivalent noise

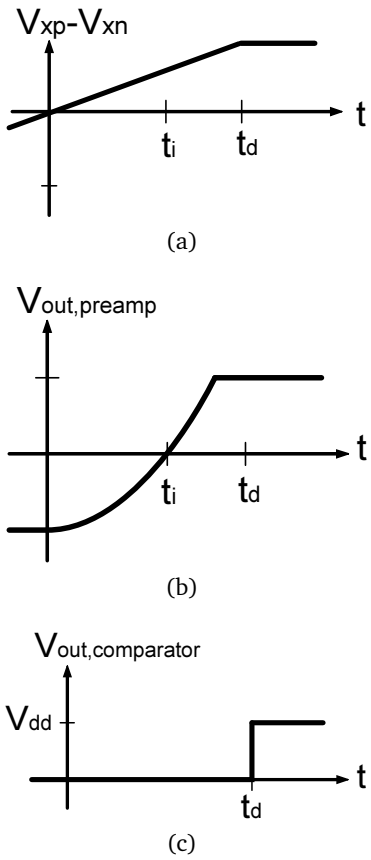


Figure 4.5: Comparator input voltage showing overshoot on input due to delay(a), preamplifier output showing the delay t_i to reach the comparator tripping point(b) and comparator output signal showing the total comparator delay t_d (c). Figure modified from [17].

resistance $Rn = \frac{G_n}{G_m^2}$, where G_m is the preamplifier transconductance and G_n is the modelled noise conductance of the noise source current PSD, $S_{xo} = 4kTG_n$ [17].

The two most interesting special cases of equation (4.5) can be found when $t_i \gg \frac{\tau_o}{2}$ and $t_i \ll \frac{\tau_o}{2}$. The input referred noise can then be found to be:

$$\overline{v_n^2}(t_i) = \begin{cases} 4k_BTR_n \cdot \frac{1}{4\tau_o} & \text{if } t_i \gg \frac{\tau_o}{2}, \\ 4k_BTR_n \cdot \frac{1}{2t_i} & \text{if } t_i \ll \frac{\tau_o}{2} \end{cases} \tag{4.6}$$

For a given preamplifier response time t_i and a given transconductance and load capacitance, it is shown theoretically in [17] that an infinite time constant τ_o gives the lowest effective noise bandwidth, meaning the preamplifier should have infinite output resistance. Then the input referred noise from (4.6) would be set from the response time and the equivalent noise conductance R_n.

Assuming all transistors are operating in active mode, the input referred noise voltage from a preamplifier is dominated by the input differential pair and can be found as [19, ch.7.5]:

$$\overline{v_{n,in}^2} = 8k_BT\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2}\right) + \frac{2K_N}{C_{ox}(WL)_1 f} + \frac{2K_P}{C_{ox}(WL)_3 f} \cdot \frac{g_{m3}^2}{g_{m1}^2} \tag{4.7}$$

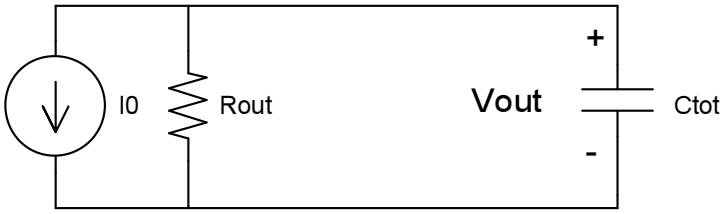


Figure 4.6: Equivalent circuit for current source charging a capacitive network

Here, g_{m1} and g_{m3} are the transconductance of the input transistor and load transistor from Figure 4.4, f is the frequency and $K_{N,P}$ is the flicker noise coefficients for N and P-type MOSFETS.

To lower flicker noise from the preamplifier, the gate area of the input differential pair should be maximized. At the same time, the gate capacitance should not be of the same magnitude as the sampling capacitors as it can affect the circuit operation.

Maximizing the transconductance of the input pair is important as this lowers both thermal noise from the input pair and increases the gain in the preamplifier. The transconductance of the active load should be minimized to make the input pair dominate the noise. At the same time, too large load transistors might introduce a dominant pole reducing the speed of the amplifier.

4.2.3 Current sources

For a fully differential implementation, p-type and n-type current sources are needed for each of the output nodes, as the charge transfer happens by charging one output and discharging the other. To have a correct charge transfer both current sources should be the same magnitude. If there is a mismatch, it will appear as if the common-mode voltage has changed. This can be visualized in Figure 4.3 if the ramp rate were higher on one signal than the other. The comparator will trigger when the inputs cross, resulting in a average voltage different from the common-mode voltage. Having an exact match between p-type and n-type current sources can be hard, therefore a common-mode feedback (CMFB) circuit is needed to stop the output common-mode from floating to one of the rails during the integration.

Current sources exhibit shot noise proportional to the output current which cannot be reduced. However, this noise is also seen at the input since the shot noise from the current source will cause a random charging of the capacitive network, again causing timing jitter on the comparator.

Output resistance and ramp rate

Using Kirchoff's current law, the differential equation for the equivalent circuit of a current source in Figure 4.6 can be set up as:

$$I_{out} = \frac{V_{out}}{R_{out}} + C \cdot \frac{dV_{out}}{dt} \tag{4.8}$$

This equation has many possible solutions, depending on how R_{out} varies with respect toV_{out}. Assuming that R_{out} is a constant, the solution is given as:

$$V_{out}(t) = I_0 R \cdot \left(1 - e^{-\frac{t}{R_{out}C}}\right) \tag{4.9}$$

CBSC is dependent on a linear voltage ramp rate to avoid signal dependent overshoot. Equation (4.9) can be approximated to if R_{out} is very large. The main problem is that r_{ds} of the current source transistors varies quite a lot with V_{out}(See for example [16]), which makes it hard to make an analytical expression for the output voltage.

The ideal case would be if R_{out} can be described as a linear function of V_{out}, $R_{out} = K \cdot V_{out}$. Then then the solution of (4.8) is given as:

$$V_{out}(t) = t \cdot \left(\frac{I_0}{C} - \frac{1}{KC}\right) \tag{4.10}$$

which would ensure a linear ramp rate across the entire voltage range. However, as the output resistance is highly nonlinear, it is not easy to make an analytical expression for this.

Current source sizing

The available time for charging the output node can be written as:

$$t_{charge} = \frac{\alpha}{f_s} - t_{preset} \tag{4.11}$$

where α is the clock duty cycle, f_s the clock frequency and t_{preset} is the part of the charge phase used to preset the outputs.

Assuming a constant current and allowing the output to reach all possible output voltages during this time, the necessary current is given by:

$$I_0 = \frac{C \cdot V_{DD}}{t_{charge}} \tag{4.12}$$

Linearization techniques

To make current source behave more ideal, several techniques to increase the output impedance can be used. The most obvious is to use cascoded current sources, as shown in Figure 4.7a. By doing this, the output impedance seen is increased from $r_{out} = r_{ds}$ to approximately $r_{out} = g_{m1} r_{rds1} r_{rds2}$ [11, p.137].

Using the square-law MOSFET approximations[11, p.59] for transistors operating in the active region, the output resistance can be found with these equations:

$$\begin{aligned} g_m &= \frac{2I_D}{V_{DS,sat}} \\ r_{ds} &= \frac{1}{\lambda I_D} \\ \lambda &= \frac{k}{2L\sqrt{V_{DS} - V_{DS,sat} + \Phi_0}} \end{aligned} \tag{4.13}$$

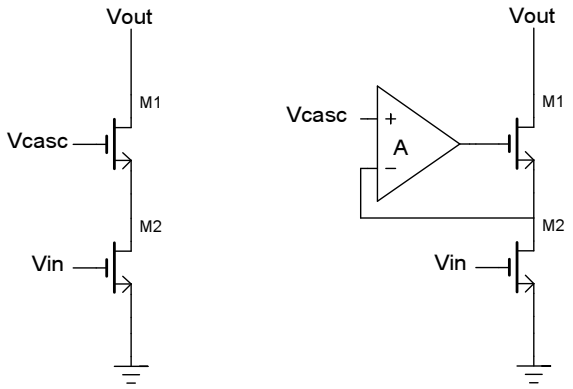


Figure 4.7: Cascoded current source (a) and enhanced output impedance current source(b)

Combining these gives an approximation for the output impedance for the current source in Figure 4.7a:

$$r_{out} = g_{m1} r_{rds1} r_{rds2} = \frac{8 L_1 L_2}{k_1 k_2 I_D V_{DS1,sat}} \sqrt{V_{DS1} - V_{DS1,sat} + \Phi_0} \sqrt{V_{DS2} - V_{DS2,sat} + \Phi_0} \quad (4.14)$$

Here, L is the transistor gate length, $V_{DS,sat}$ is the drain source saturation voltage and Φ_0 is the built-in voltage of a pn junction.

Increasing gate lengths is the most obvious way to increase the output resistance, but this can result in a large gate capacitance to have large enough charging currents. Since the current sources in CBSC should be able to turn on and off quickly, this is not ideal. An analytical expression for how the output resistance can be maximized can be hard to achieve due to the fact that the current sources should work across the entire output range, and it would be uncorrect because many of the parameters varies with the drain and gate voltages of the transistors. The transistors will also have to work in the linear region if the output voltage range is larger than $V_{DD} - 2V_{DS,sat}$.

The output impedance can also by enhanced by utilizing a feedback amplifier as shown in Figure 4.7b. The amplifier tries to keep the voltage at its negative input to V_{casc} by adjusting the gate voltage on M1, thereby increasing the cascode output impedance to $r_{out} = g_{m1} r_{rds1} r_{rds2} (1 + A)$, where A is the loop gain of the amplifier. For CBSC, this amplifier should have a slew rate that is higher than the output voltage ramp rate to be effective.

An example of a feedback amplifier implementation is shown in Figure 4.8 [4]. The first transistor M3 in the feedback path is acting as a level shifter, while the source follower M4 acts as an inverting amplifier, increasing the gate voltage on M1 to sink more current when the drain voltage on M2 decreases.

Another possible technique is to bias the current source transistor dynamically[6]. It can be achieved this by decreasing the voltage on the gate to compensate for the ramp rate reduction due to decreased output impedance, as shown in Figure 4.9. The disadvantage with this is a need for continouous calibration of the discharge current I_{small} with respect to process variations, temperature and voltage, where the calibration circuit has to be as accurate as the total system.

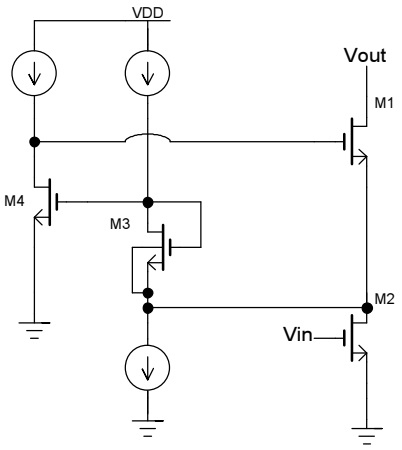


Figure 4.8: Current source with enhanced output impedance by using a feedback amplifier

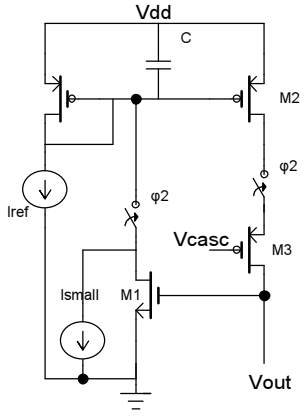


Figure 4.9: Dynamic biased current source

For high-speed CBSC current sources, a rapid increase of the output voltage occurs when charging, which creates a gate current across C_{gd} of the cascode device. This means that either large bypass capacitors are needed at the gate node to avoid a significant voltage change, or a unity gain buffer with high enough current sourcing/sinking capabilities could be used.

Also, to reduce power consumption due to this "gate leakage" and increase turn-on/off speed, the gate capacitance of the current source should be as low as possible.

4.2.4 Overshoot reduction techniques

Several non-idealities contributes to the DC offset seen from the input integrator. The most severe for high-speed CBSC circuits is the comparator delay because of the large current sources needed. Given a linear voltage ramp on the comparator inputs as shown in Figure 4.3, the total overshoot added to the output due to delays during one charge transfer phase is:

$$\begin{aligned} V_{offset} &= \frac{dV_{out}}{dt} \cdot (t_d + t_{cs} + t_l) \\ &= \frac{I_0}{C_{tot}} \cdot (t_d + t_{cs} + t_l) \end{aligned} \tag{4.15}$$

Here, t_d is the comparator delay, t_{cs} is the delay in turning off the current I_0 and C_{tot} is the total capacitance on the output node of the integrator.

Several approaches can be taken to minimize this overshoot. The most obvious is to minimize the turn-off time of the current sources, reducing propagation time through any sequential logic and increasing speed in the comparator. Increasing the speed in the comparator is costly in terms of power consumption, therefore other ways should be explored too.

In every sample, there is also charge added to the output by charge injection and clock feedthrough from the switches which will appear as a DC offset. This can be somewhat reduced by using dummy switches [19, ch.12.2], which will reduce some of the total charge injected. Except for this and minimizing the switch size not much can be done about to remove this offset.

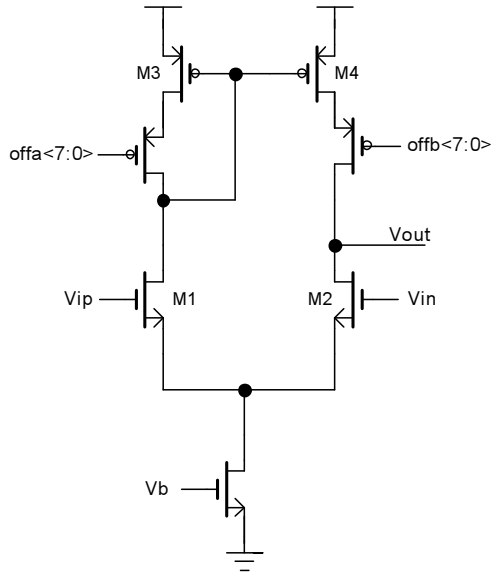


Figure 4.10: Preamplifier with offset adjustment [20]

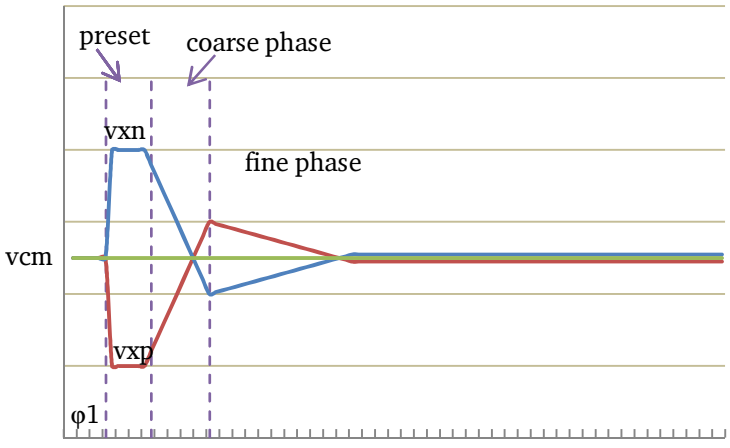


Figure 4.11: Output voltage with charge transfer phase split into coarse and fine parts

[20] includes two sets of binary sized transistors in the comparator preamplifier used to control the current in each of the differential branches as shown in Figure 4.10. By reducing or increas-

ing the current in each of the branches, a systematic, nonlinear offset will be introduced. The disadvantage is more capacitance on the output node of the preamplifier which reduces speed and higher noise.

Several publications(E.g. [2], [5], [10]) utilize a dual-phase charge transfer, where a coarse phase charges the outputs with a large current, while a small current discharges much of the overshoot thereafter as shown in Figure 4.11.

In addition, [5] reduces the overshoot in the coarse phase by subtracting a fixed amount of charge at the end of the coarse phase. This lowers the overshoot from the coarse phase, leaving more time for the fine (slow) part of the charge transfer phase.

Another option would be to sense the comparator inputs by using a slow, high-accuracy comparator in the next sampling phase to check if there still is overshoot on the comparator inputs. If so, a programmable amount of charge should be subtracted from the outputs every sample until the overshoot is calibrated away. The disadvantage is a higher complexity and the need for a low-power comparator with a better accuracy than the total system accuracy to completely remove the overshoot.

Chapter 5

Design of CBSC Integrator

5.1 Specifications

The requirements for the integrator design are quite loose, but there are a few design targets based on existing designs, as shown in Table 5.1. The design is based on a 90nm process, with a nominal supply voltage of 1.2V.

Name	Target	Value	Unit
Power consumption	<	0.9	mW
Dynamic range	>	70	dB
Signal bandwidth	>	1.5	MHz

Table 5.1: General specifications input integrator

$\Delta\Sigma$ topology

It is also of interest to try to design an integrator with the same or better accuracy as the currently best performing CBSC circuit [7]. With this as a background, a system ENOB of 13 has been chosen, which should be enough to cover the requirement for dynamic range from Table 5.1. Since all building blocks add noise and distortion, all calculations are based on a ENOB of 14 (86dB) to leave a design margin.

When deciding on a modulator topology, it is important to choose on the basis of the components that are to be designed. With the calculations for the sampling capacitance below, minimizing switch size to reduce charge injection,clock feedthrough and switch on/off time is desired. As seen in (2.10), a high overload factor OL is wanted to minimize C_S and thereby reduce area and power consumption.

In [13, ch.3], optimal coefficients can be found for different converter topologies. Multi-bit quantization puts strict accuracy requirements on the feedback DAC, and some kind of calibration technique is almost always necessary for high accuracy.

No high-accuracy design has so far been presented with a sampling speed higher than 200MS/s [6]. This is not yet presented as silicon-proven, therefore an OSR of 32 is chosen, yielding a

sampling frequency of f_s = 96MHz. It is further desirable to have a single-bit quantizer to simplify the DAC and quantizer design.

A possible topology would then be a 4^{th} order cascaded 2-2 modulator [13, ch.3.4.3] as shown in Figure 5.1.

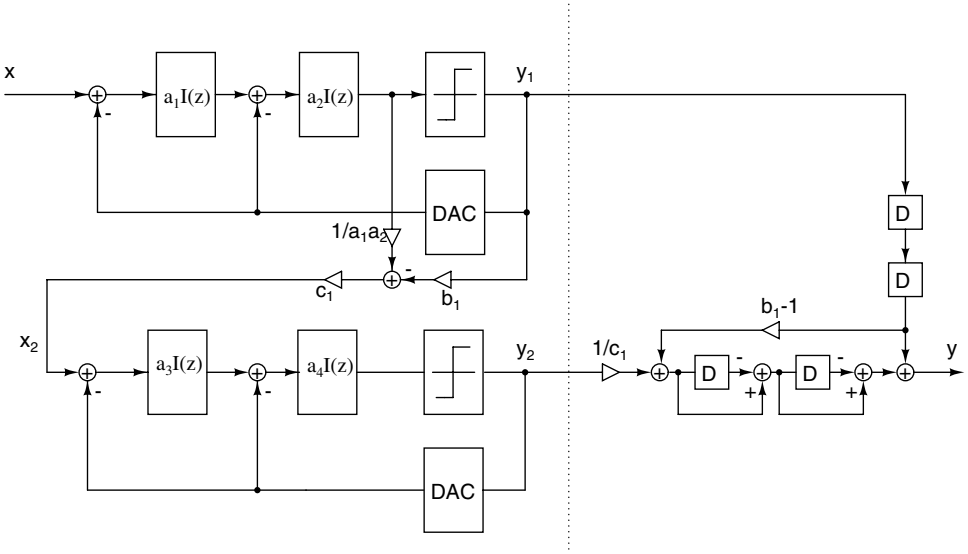


Figure 5.1: Fourth order cascaded 2-2 $\Delta\Sigma$ modulator

This single-bit modulator has a theoretical maximum SNR_p of 92dB, which ensures that the topology is not the performance limiting factor. This gives an overload level of 0.7.

The decided converter specifications are summarized in Table 5.2, and the integrator will be designed to fit into these specifications.

Symbol	Description	Value	Unit
f_s	Sampling frequency	96	MHz
α	Duty cycle non-overlapping clocks	0.45	
SNR_p	Theoretical peak converter SNR	92	dB
$(a_1, a_2, a_3, b_1, c_1)$	Loop coefficients	(0.5, 0.5, 0.5, 2, 0.5)	
OL	Overloading factor	0.7	
T	Design temperature	371	K

Table 5.2: General specifications $\Delta\Sigma$ converter

5.2 Supply voltage

The lowered supply voltage of nanoscale processes makes it difficult to maintain the same performance for a given power consumption [21]. Therefore, running the circuit on a higher supply voltage will give more headroom for the signal. In this design, a power supply of V_{DD}= 1.3V has been chosen instead of the nominal supply of 1.2V, which is an 8.3% increase.

A thorough summary of reliability issues and gate voltage can e.g. be found in [22]. Other effects such as Negative Bias Temperature Instability (NBTI) is experimentally tested for a 90nm

process in [23] without finding any issues for gate voltages as low as 1.3V. The process used in this implentation has a oxide thickness of 2.8nm, while other 90nm processes [24] support a 1.2V supply with oxide thickness as low as 1.8nm. This indicates that a minor increase in the maximum gate voltage can probably be tolerated. It is possible that this could lead to long-term reliability problems in production, but a detailed reliability analysis of the process is beyond the scope of this report.

5.3 Ideal model

When designing $\Delta\Sigma$ modulators, transistor simulations of the entire system to view the results will take very long time and is often only done as a final verification. To be able to do quick system simulations with one or more ideal components, an ideal CBSC integrator model written in Verilog-A has been designed. The model is able to simulate with for instance finite switch on/off resistance, delays in turning components on/off, comparator offset etc. This makes it easy to verify that the building blocks work as they are supposed to in the system and quickly find non-ideal effects that can affect the circuit performance.

A ideal Verilog-A model is also created to sample the output voltage at the end of each charge transfer period to extract FFTs of the output voltage.

5.4 Sampling network

Sampling capacitance and switch resistance

From equation (2.10) together with the data in Table 5.2 and a SNR of 86dB, a sampling capacitance of C_S**=307fF** is necessary.

Equations (2.11)-(2.14) are used to find the maximum sample switch resistance. With the same data as for the sampling capacitance, this is found to be **R=771**Ω.

5.4.1 Jitter

Using Equation (2.15) with a SNR due to jitter of 86dB, a 96MHz sampling frequency and an OSR level of 32, the standard deviation of sampling time uncertainty is found as:

$$\sigma_{\Delta T} = 30ps \tag{5.1}$$

To not have the performance limited by jitter, the switch should therefore be able to turn off faster than 30ps.

5.4.2 Switch design

To maximize differential signal swing, the common mode voltage should be placed around $V_{DD}/2$. As mentioned in Chapter 2, the low supply voltage forces the switches to be either

bootstrapped or clock boosted. Clock boosting is successfully used in the sampling network of the CBSC circuit of [20], while this design will use a bootstrapped design.

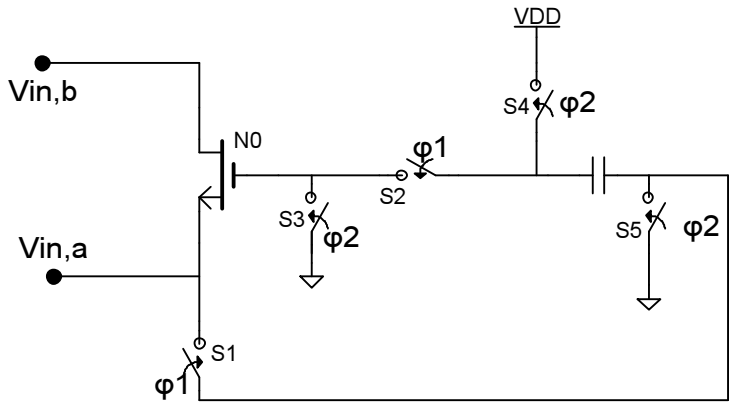


Figure 5.2: Fundamental operation of a bootstrapped switch, figure from [25].

Using two non-overlapping clocks ϕ_1 and ϕ_2, the capacitor in Figure 5.2 is first charged to V_{DD} in ϕ_2 while the switch is turned off. In ϕ_1, the input lifts the gate voltage to $V_{DD} + V_{in,a}$, turning the switch on and keeping the gate source voltage of the NMOS at $V_{GS} = V_{DD}$.

Several similar bootstrapped switch designs exist[26][25][27]. This implementation is based on [25], whose implementation is shown in 5.3.

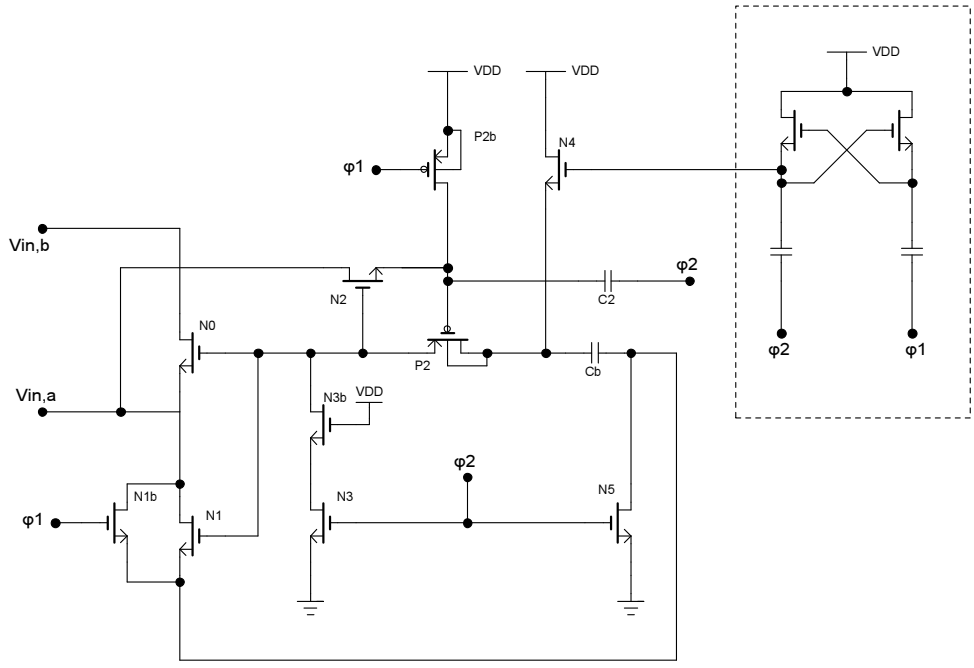


Figure 5.3: Bootstrapped switch implementation from [25]

The precharge phase occurs in ϕ_2, when the gate of N0 is pulled to ground and the capacitor Cb is charged to V_{DD}. The stapled rectangle in Figure 5.3 is a simple Nakagome charge pump [28]. This lifts the gate voltage of N4 to V_{DD} and $2V_{DD}$, ensuring that N4 is on when the source of N4 is at V_{DD}. At the same time, the voltage across C2 is 0V. The switch **on** state is initiated when ϕ_2 goes low. This charging of C2 causes a voltage drop on the gate of P2, which turns it slightly on. The positive feedback loop then starts turning on N2, causing P2 to turn more on.

This causes P2 itself to be bootstrapped to $V_{SG} \approx V_{DD}$, increasing linearity. Transistor N3b is included to protect the gate oxide of N3 of higher voltages than V_{DD}.

However, one issue remains unsolved with this implementation. The moment ϕ_2 goes low (before ϕ_1 goes high) and N2 is turned on, a low impedance path exists between V_{DD} and $V_{in,a}$ through P2b and N2. The implementation of this switch can therefore consume excessive current for low power applications and potentially harm signal integrity.

The workaround implemented in this project to avoid this is shown in Figure 5.4. Instead of connecting the switch to the input, it is connected to node A, which is 0V in ϕ_2 and approx. $V_{in,a}$ in ϕ_1. Complementing this switch with a PMOS switch to create a transmission gate ensures that P2 is still approximately bootstrapped with $V_{SG} \approx V_{DD}$, even if the linearity is not equally good. This ensures that P2 is turned on in a controlled way without creating any low impedance paths.

The switch itself can also be placed in a deep N-well to be able to bias the bulk for increased linearity, higher off-resistance and isolation from substrate noise. However, this is not done for this implementation as the well junction diode of the deep N-well is not modelled in the current model files made available for this implementaion.

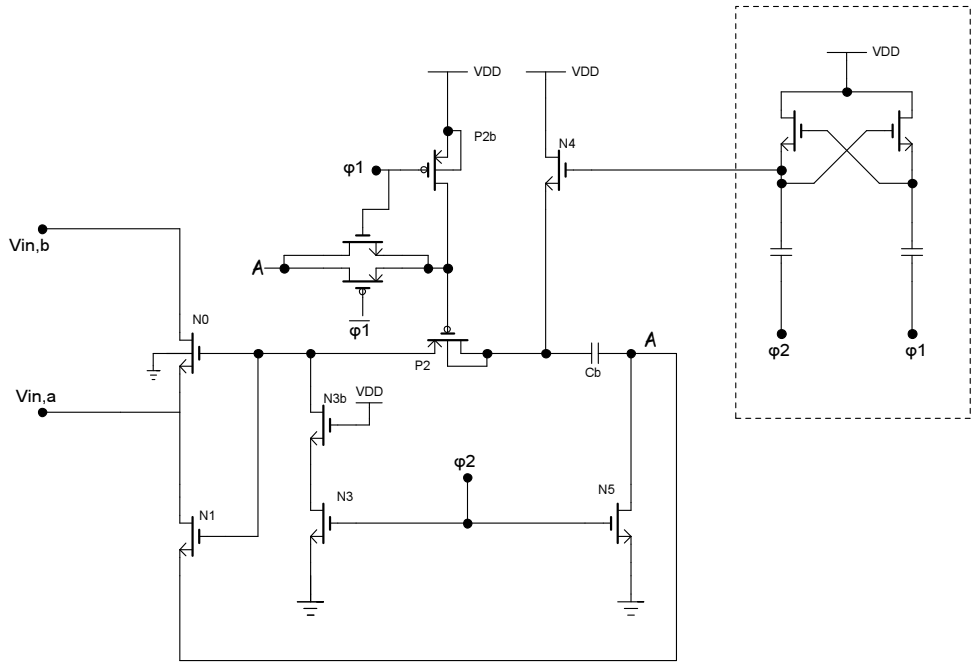


Figure 5.4: Bootstrapped switch implementation for sampling network

The main switch is designed with minimum length and width large enough to have a on-resistance of 500Ω to allow for some mismatch and still be within the needed maximum resistance. The bootstrapping capacitor, which charges the gate capacitance of N0, is sized so that V_{GS} of the switch N0 is above $90\% \cdot V_{DD}$ when on. The resistance through N1 and P2 are adjusted low enough so that the switch turn on and off at around 30ps. N3 and P2b are also sized to ensure fast turn on/off times while N4 and N5 are made just large enough to ensure that C_b are charged fully during the off phase.

5.5 Output preset circuit

In the preset phase both outputs will be pulled to the supply rails, yielding a need for large switches to quickly pull the outputs to their intended value. Since the current sources also starts up during this preset phase, the switches must be large enough to also source/sink this extra current.

To avoid charge injection, transmission gates are used as preset switches even though only one of the transistors are conducting. The transistors are equally sized, which to a first order cancels the charge injection. Simulations indicate that a preset phase of length $t_{preset} = 200$ps is needed to sufficiently pull the outputs towards the supply rails.

5.6 Comparator design

In designing a comparator, the focus was on keeping it as fast as possible within the power consumption limits and at the same time have low noise as discussed in 4.2.2. It should also be possible to preset the output nodes to ensure that the comparator is ready to toggle after the preset phase is done.

Two zero-crossing devices have been implemented at transistor level. The first one is based on the zero crossing detector of [20, ch.5], which consists of a differential to single-ended preamplifier followed by a positive-feedback threshold detection latch as shown in Figure 5.5. The output of the preamplifier must be near the positive rail in the preset phase to avoid too much leakage through M7. As the inputs of the preamplifier are ramped, the voltage on the latch input lowers and enough current leaks through M7 to cross the latch threshold, pulling the output low.

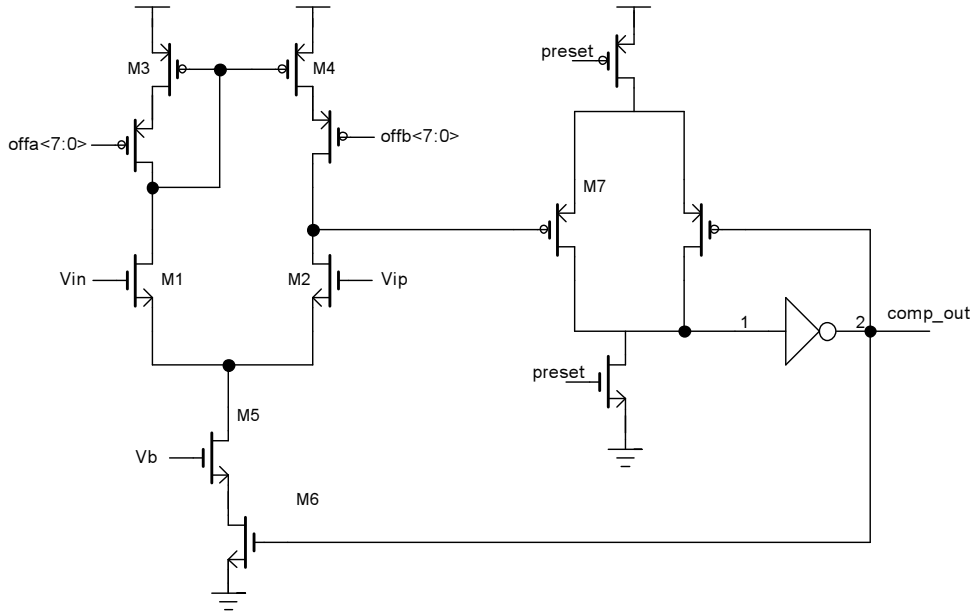


Figure 5.5: Comparator consisting of preamplifier and threshold detecting latch, from [20]

This zero-crossing device was discarded after system simulations due to the fact that the latch-side input was not isolated enough from kickback from the latch. For use in a pipelined ADC

this would be OK, as the sampling switch of the next stage closes instantly when the comparator toggles. However, for a integrator which should output a voltage dependent on the output from the previous phase, it would cause a signal error in the differential signal if charge is injected only into one of the differential nodes.

Therefore, a differential comparator was implemented instead.It is based on the self biased Bazes-amplifier [29] in Figure 5.6, which can be made differential by connecting the original output to the self biasing node and adding an extra set of input pairs [30]. This circuit has recently been used in a silicon-proven comparator-based $\Delta\Sigma$ ADC [10] and is shown in Figure 5.7.

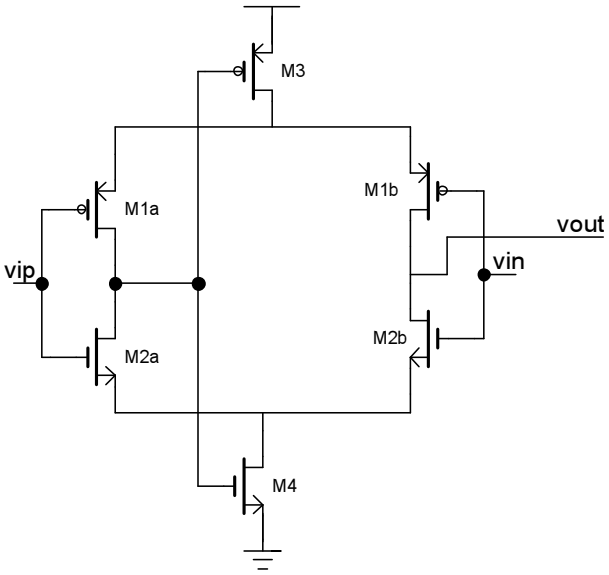


Figure 5.6: Self-biased complementary amplifier, from [29].

In Figure 5.7, the negative feedback that stabilize the common-mode consists of transistors M9 and M10, together with the replica input stage of transistors M1-M4. If the bias voltage on V_x for example starts floating upwards, the PMOS connected to the VDD supply sources less current while the NMOS connected to ground sinks more, causing the common-mode level to float back.

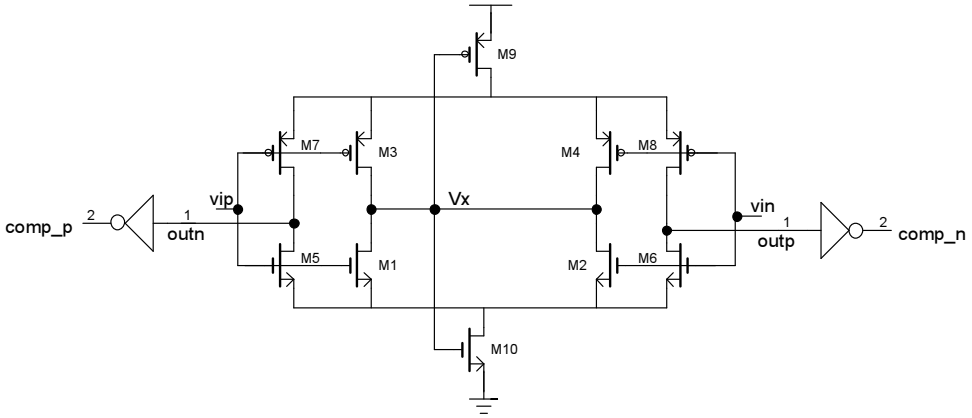


Figure 5.7: Comparator used for integrator consisting of a fully differential self-biased amplifier with skewed inverters as output buffers.

The differential-mode gain of the amplifier (without the buffers) is given as [29]:

$$A_0 = (g_{m,1} + g_{m,2}) \cdot (r_{ds,1} || r_{ds,2}) \tag{5.2}$$

Compared to a regular single-ended preamplifier, this circuit has an approximate doubling of small-signal gain due to the push-pull operation of the complimentary circuit [29].

The output time constant of the amplifier is the same as seen on a regular differential pair preamplifier [10]:

$$\tau_o = C_{out} \cdot r_{out} = (C_{DB,5} + C_{GD,5} + C_{DB,7} + C_{GD,7} + C_L) \cdot (r_{ds,5} || r_{ds,7}) \tag{5.3}$$

To lower noise in the circuit, g_m of the input pairs have been maximized by using a high $\frac{W}{L}$ ratio. The gate area of the input transistors is limited by the total gate capacitance, which has been set to 30fF, about 10% of the sampling capacitance.

The outputs of the amplifier have been connected to a pair of heavily skewed inverters. This is to increase the toggling speed of the comparator, and at the same time limit the current through the inverters outside the charge transfer phase when the inputs are at common-mode level. Pull-up/down of the output inverters for the preset phase is also included (not shown). This would potentially give a high leakage current through M5 and M8 in the preset phase, but as the inputs are pulled away from the common-mode level in the preset phase, only a few μA extra leaks through the pull-up/down transistors.

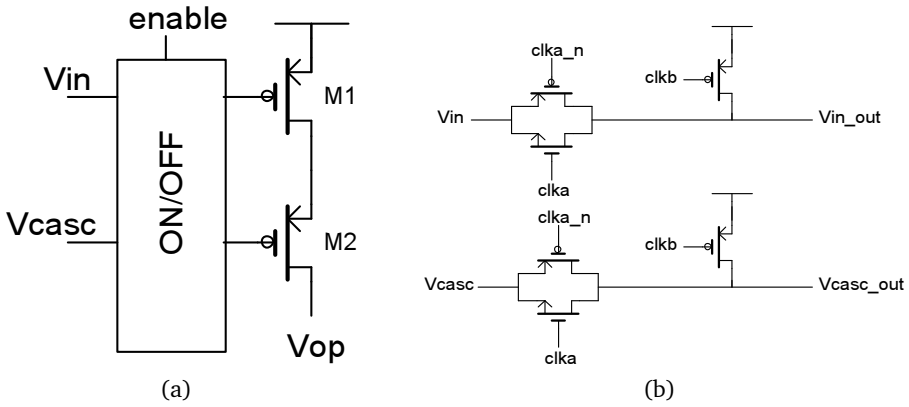
5.7 Current sources

The current sources consist of both a N-type and a P-type current source, which can be hard to match exactly. The approach taken is to have one large current source on each side together with several smaller sources. The large ones should be fairly good matched, while the small ones are controlled by the common-mode feedback system to match the sources even better. By using eight binary sized unit sources, a total of 128 different currents can be added or subtracted to the main current sources.

Current source sizing

Equation (4.11) gives an available charging time of $t_{charge} = \frac{0.45}{96MHz} - 200ps = 4.49ns$. The needed current for the outputs to reach the entire voltage range is found with Equation (4.12). Assuming a capacitance on the next stage of $C_{sample,2}$=100fF, then the total capacitance on the output node is found as $C_{tot} = C_{sample,2} + \frac{1}{\frac{1}{C_{sample}} + \frac{1}{C_{integration}}}$.

The integrator should have a gain of 0.5, which makes the integration capacitor two times as large as the samplingcapacitor. With a integration capacitor of 614fF, the total capacitance is then found to be $C_{tot} = 305fF$. The needed current is then $I_0 \approx 91\mu A$, but 150 μA is chosen to compensate for process variations, parasitic compensation and linearity falloff due to reduced current source output resistance near the rails.



(a) (b)

Figure 5.8: Cascoded current source implementation (a) and its enabling circuit (b)

Implementation

To ensure a high output impedance, the current sources are implemented as cascoded current sources as shown in Figure 5.8a. The transistors should ideally be biased so that they operate with a low $V_{DS,sat}$ to ensure active mode operation across most of the output voltage range.

The disadvantage with this is a need for very large current source transistors to give enough current, which will give a long switch on/off time. Therefore, the length is reduced so that the sources will turn off in less than 30ps after the pull-up/pull-down transistor turns on. The cascode bias voltages from Figure 5.8a were set to $V_{casc} \approx V_{cm}$. This makes it possible to reuse it for both the p-type and the n-type implementation, since V_{cm} is placed mid-rail.

Simulations showed that the main source of output ramp reduction was due to the charge injected from the output across the gate capacitance on the cascode transistor, changing the voltage of V_{casc}. Therefore, a lot of decoupling is needed on this node to avoid large changes in the bias voltage. An alternative would be to bias this node with an amplifier like in Figure 4.7b. This will require a amplifier that is stable for several different loads and also able to sink/source enough current to keep the cascode bias voltage stable.

The current sources were turned on and off with the enabling circuit shown in Figure 5.8b, which consists of simple transmission ports and pull-up/pull-down transistors. To avoid pulling the bias nodes up and down, the enabling clocks were designed using the logic circuit from Figure 5.9a. This ensures that the pull-up transistors is never on when the transmission gate is open, as can be seen in Figure 5.9b.

Instead of using a fast feedback amplifier, dynamic biasing of the input voltage were implemented [6]. This was done by feeding back the output voltage to a pull-down transistor as shown with transistor M4 in Figure 5.10. Transistor M5 is used as a resistance to limit current through the low impedance path that is created through M3-M4 when the output voltage ramps up. Transistors M4 and M5 were implemented as low-threshold voltage transistors so that M4 turns on for even a low V_{out}. Transient simulations showed that the current output varied with about 20μA while V_{out} were charged from 0-1V.

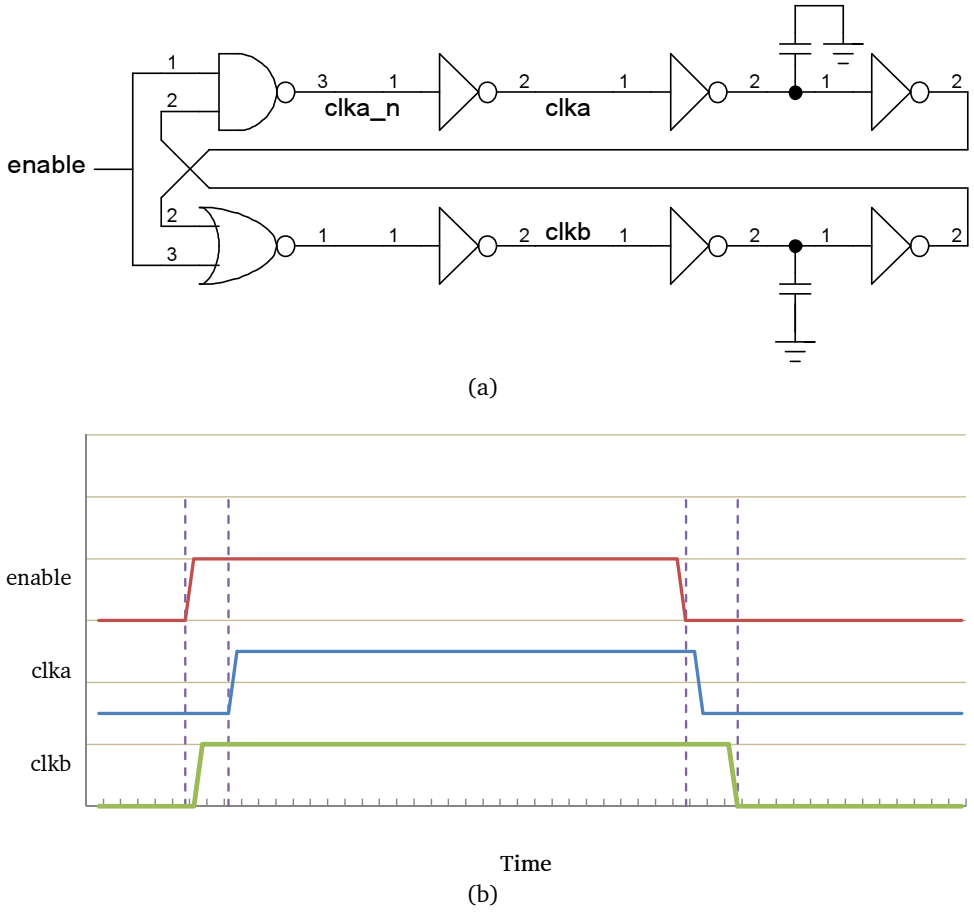


Figure 5.9: Sequential logic used to turn p-type current source on/off (a) and its waveform (b)

5.8 Overshoot correction

The overshoot creates a quite large DC component being added to the output signal, causing the integrator to saturate in a few clock cycles even with no input signal. This systematic overshoot can be reduced in several ways, a few are mentioned in Chapter 4.2.2.

For testing purposes, a overshoot correction circuit has been developed. This ensures that the integrator will not saturate while being simulated in open loop. The correction circuit works by connecting two "parasitic" capacitances to the two rails in the charge transfer period. When the current sources has turned off, the bottom side of the capacitors are shorted to subtract/add charge on the positive/negative output [5].

The size of the capacitor are set by using an ideal comparator which measures if overshoot happened in the previous charge transfer period. The result of this comparison makes an 8-bit binary up/down counter to increase or reduce the total capacitance depending on the comparison. A simplified schematic of the overshoot correction circuit is shown in Figure 5.11.

To have a perfect overshoot correction circuit, the overshoot compararator must have an accuracy better than the total system accuracy which demands a large area. However, if the amount of overshoot is not signal dependent, then a less accurate comparator can be used to reduce but not remove overshoot in order to better the modulator dynamic range by removing some DC.

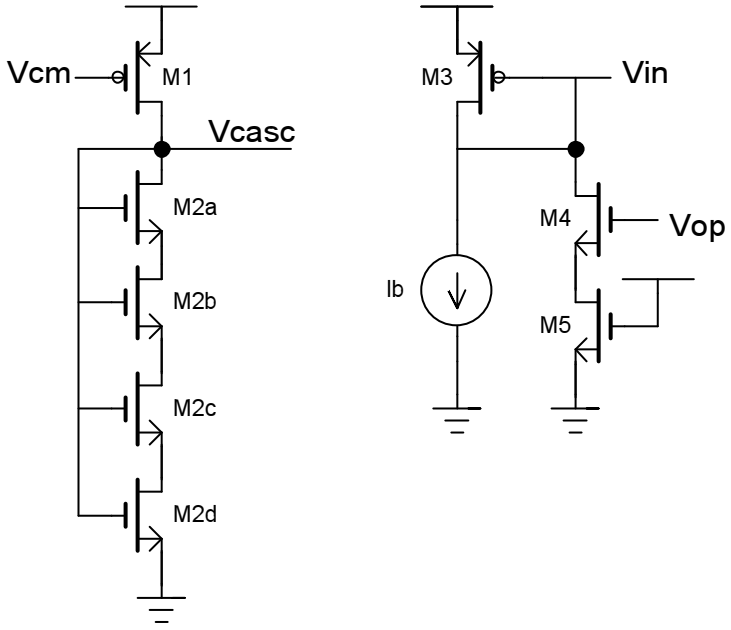


Figure 5.10: Bias network for p-type current source

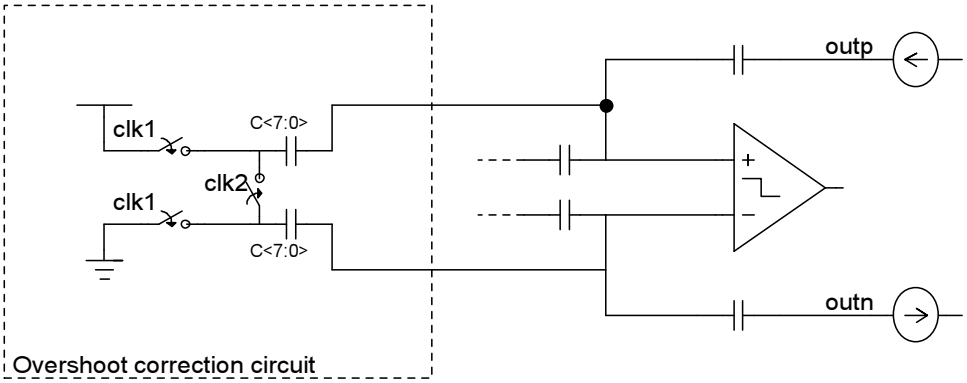


Figure 5.11: Overshoot correction circuit (stapled rectangle) to reduce the DC added to the output of the integrator.

5.9 Common-mode feedback

As discussed in section 4.2.3, there is a need for CMFB when using comparator-based circuits as an integrator. To find the average output voltage, two capacitors are connected back-to-back on the output nodes as shown in Figure 5.12 [10]. After the overshoot correction circuit has subtracted its charge, a comparator is used to compare V_{avg} to the common mode voltage.

Depending on the result, a 8-bit up/down binary counter together with AND gates are used to include more or less current in the p-type current source the next sample. The comparator is implemented as an ideal model, but can for example be implemented as a very low power cascoded inverter comparator [31] as shown in Figure 5.13.

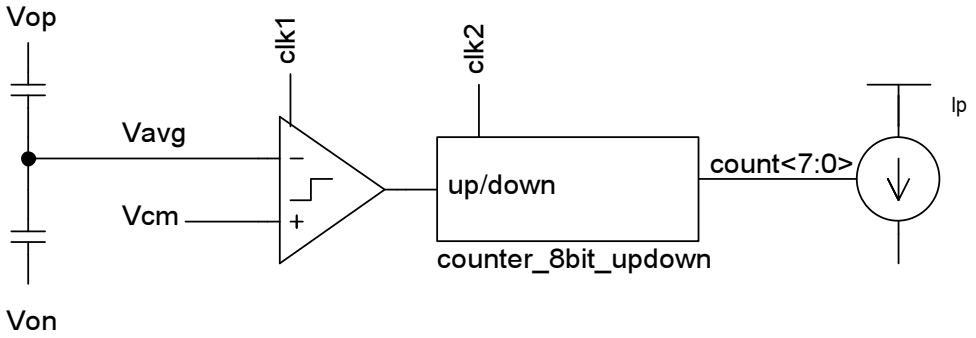


Figure 5.12: Common-mode feedback system

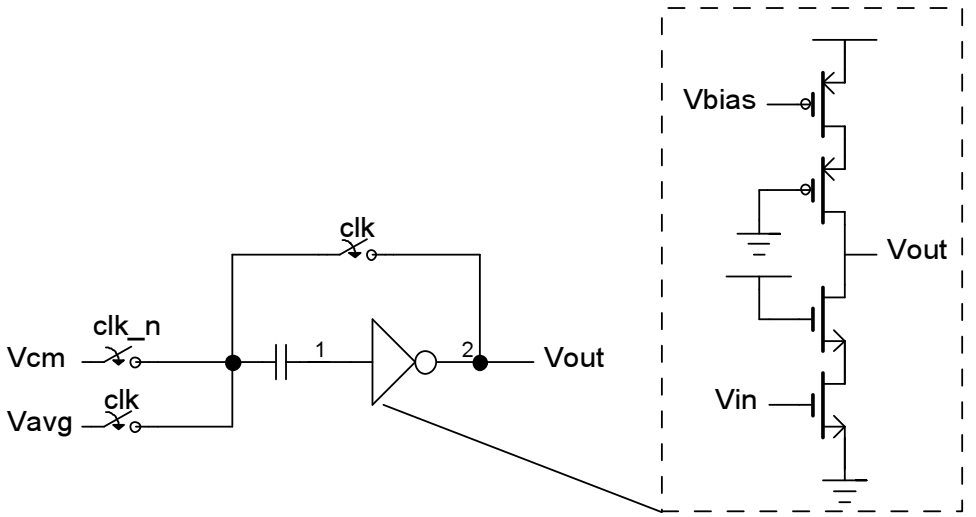


Figure 5.13: Low-power comparator, from [31]

5.10 Digital control logic

As digital design is not a significant part of the report, the control logic for the circuit is implemented as an ideal model written in Verilog-A. Creating the control logic is a trivial job and can be done by implementing a state machine and a few analog delay circuits. Since only an ideal model exists, no power consumption estimate has been done. However, compared to the analog circuitry it should use little power.

Chapter 6

Results and Discussion

To simulate the performance of the integrator, the ideal case would be to create an ideal modulator feedback system around the integrator to see how much the implemented integrator would limit total system performance compared to the ideal case.

Designing an entire modulator is not within the scope of this project, therefore the integrator has been simulated in open-loop to verify functionality. Since no feedback signal is applied, the input signal must be limited to not saturate the integrator. This means that the maximum SNR of the integrator cannot be found by this method. However, the simulation gives an insight in the relative signal distortion of the input integrator.

Also, the overshoot compensation module is constantly enabled (even after a startup phase) to ensure that DC is not added during the simulation. This might cause high-frequency noise to be added to the output as it changes the amount of charge to be subtracted each clock phase.

6.1 Input frequency and data sampling

The output voltages are sampled with a Verilog-A module that stores the outputs to a file at the end of each charge transfer phase. To ensure that the sampling will produce a correct spectrum, coherent sampling is used [32]. The equation to ensure coherent sampling is:

$$\frac{f_{in}}{f_s} = \frac{N_{cycles}}{N_{samples}} \tag{6.1}$$

By using a prime number as N_{cycles}, one is guaranteed that the same sampling pattern never occurs twice. For the integrator simulations, a input frequency of $f_{in} = 1.5MHz$ is used together with a 96MHz sampling frequency. Simulations on an ideal integrator showed that a combination of 257 cycles and 16448 samples yielded proper coherent sampling with no spectral leakage. The number of samples gives a SNR>100dB, which is more than enough for the real integrator.

6.2 Ideal components

Several components have not been implemented at transistor-level but are rather created as ideal Verilog-A modules. This include the clock generator, the logic signal generating module and the comparators used in the overshoot circuit and the common-mode feedback.

System simulations with the current sources show that there are problems in transient simulations with turning the current sources on and off multiple times. The bias network seems to not be good enough isolated from the pull-up/down transistors, causing the current sources to sometimes not turn properly on. Therefore, the transient simulations of the total integrator are made with ideal current sources created in Verilog-A. It is likely that real current sources will make the performance of the circuit worse due to reduced output resistance.

6.3 Simulation results

6.3.1 Power consumption

The power consumption is extracted by averaging the current over an entire signal period. The simulation was performed under the conditions shown in Table 6.1.

Name	Value	Unit
Input frequency	1.5	MHz
Input amplitude,differential	100	mV
Clock frequency	96	MHz
Temperature	27	$^{\circ}C$

Table 6.1: Simulation conditions for power consumption simulation

The following circuits are not included in the power consumption simulation, due to the fact that ideal models were used:

- Comparators in overshoot correction circuit and CMFB
- Up/down binary counters for overshoot correction circuit and CMFB
- Logic control signal generation module
- Current source biasing and feedback

Standalone simulations of the current source bias module shows that it draws about 20μA for each current source, while the feedback module draws an average of approximately 50μA for each current source.

The current drawn from the power supply by the other modules are shown in Table 6.2.

Without the current source bias and feedback, this gives a total current of 191μA (0.25mW). Adding the estimated current drawn by bias and feedback give a total of 331μA (0.43mW). The ideal modules will also have some impact on the total power consumption, but the result is still less than the requirements set in Table 5.1.

Module	Current	Comment
Bootstrapped switch	2μA	8 switches total in integrator
Comparator	128μA	
P-type current source	21μA	Will increase for larger amplitude input signal
N-type current source	0μA	Capacitor charging happens through preset circuit
Preset circuit	21μA	
Overshoot correction circuit	$2nA$	
Common-mode feedback	4.5μA	

Table 6.2: Supply current drawn by integrator modules

The power consumption in the current source feedback is fairly high due to the low impedance path created by the feedback loop and this current might have an even better effect on linearizing the current sources if it was used for a feedback amplifier instead.

Also, increasing the comparator speed can be done and still be within the power consumption requirements.

6.3.2 Open-loop integrator spectrum

The integrator is simulated in open-loop for 175 μs for different input amplitudes, and the last 16448 samples were extracted into Matlab. The plotting script uses Matlab's **fft** function, calculates a one-sided power spectral density (PSD) and estimates the SNR in a given frequency band. The PSD's from the simulations are shown in Figure 6.1.

As seen, there is severe distortion of the output signal. If the lowest frequencies up to 100kHz are excluded, the signal-to-distortion ratio is approximately 37dB for a 150mV input signal. Looking at the band from 1-2MHz where the signal component is located, the ratio is 49.1dB. This is not particularly good results compared to the design specifications given in section 5.1.

As seen in the PSD, one of the main reasons for this is an elevated noise floor which appears to be frequency-dependent. The reason for the high noise floor is found by simulating with no input signal, which showed a triangular output signal that has the same frequency-dependent PSD(shown in Figure 6.1a). The reason for this triangular wave is explained in section 6.4.1.

Several sources of harmonic distortion has also been identified that contributes to the low performance. As seen in Figure 6.1, every harmonic after the fundamental up to $f_s/2$ are quite strong. Since also even harmonics are present, this shows that the signals are not truly balanced. It is found that the bootstrapped switches and the preset circuit contribute to the even harmonics, as discussed later on, while all modules contribute to the odd harmonics.

6.4 Module performance and error sources

6.4.1 Overshoot correction circuit

As the circuit is simulated in open-loop, the overshoot correction circuit is continuously enabled, trying to avoid overshoot on the comparator inputs as this will be added as DC on the output.

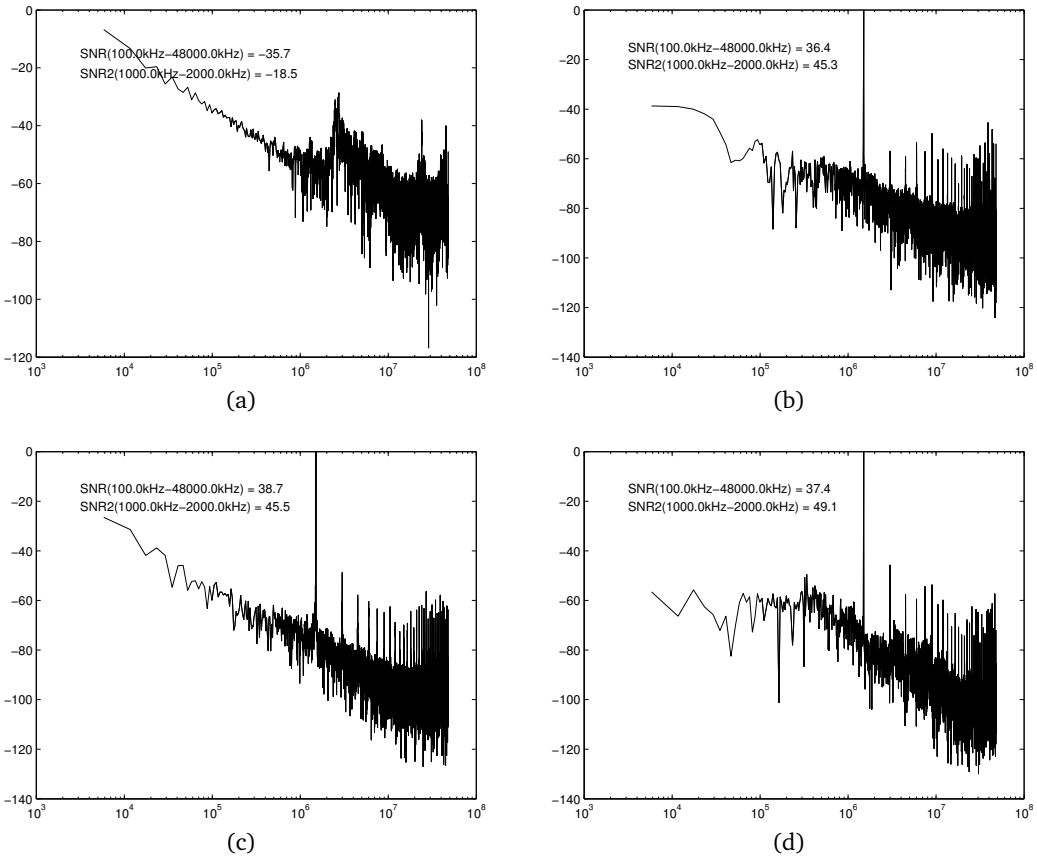


Figure 6.1: One-sided PSD of integrator outputs generated with 16448 samples, $f_{in} = 1.5MHz$, f_s=96MHz. No input signal(a), 50mV input(b), 100mV input(c) and 150mV input(d). All inputs are differential voltages. Y axis shows normalized power in dB, while the x axis is the frequencies from 1kHz to $f_s/2$.

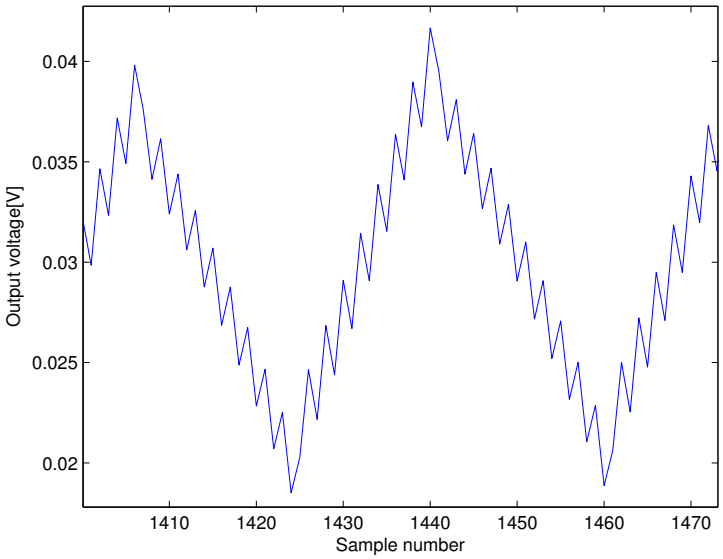


Figure 6.2: Sampled output voltage for zero input voltage showing the distortion from the overshoot correction circuit

The main problem found is the large-signal triangular wave shown in Figure 6.2, which is because of the way the overshoot correction circuit works.

As the circuit keeps switching between the two nearest capacitance values, the average charge removed does not completely cancel the overshoot, giving rise to a positive DC being integrated onto the output. When enough charge has been added, the correction circuit has to make an extra step in one direction to include more capacitance. Then the DC level being integrated turns negative, and the output seems to be integrating a negative DC value.

The final result of this is a 20mV peak-to-peak triangular waveform with a frequency peak around 2-3MHz for simulations at 27° C without mismatch. The frequency will change if the temperature is changed or if strong/weak transistor models are used.

The second problem with this circuit is when the smallest unit capacitor toggles in and out around an equilibrium. This causes an overshoot variation with an amplitude of about 2mV at the sampling frequency, which is added onto the low-frequency waveform as shown in Figure 6.2. When this high-frequency noise is folded back into the signal band, this might also be some of the reason for the elevated noise floor.

To find the real performance of the integrator it should therefore be simulated in an ideal closed-loop $\Delta\Sigma$ modulator. Then the correction circuit would subtract a constant charge for every sample except for a startup phase and eventually in some periodic calibration phases and will not deteriorate circuit performance like in the open-loop case. Unfortunately, the overshoot correction cannot be disabled when simulating in open-loop as the integrator will saturate during simulation.

6.4.2 Preset circuit

Due to final resistance in the transmission gates, the preset circuit fails to pull the differential outputs equally close to the supply rails. This causes the differential output to be wrong, as one of the differential outputs has a voltage that is lower/higher than ideal. This will appear as a

shift in the common-mode output if the preset circuit pulls the outputs to the same voltage each time.

However, since the preset circuit pulls the nodes from the previous output voltage and to the rails, there is a signal-dependent variation in how close to the supply rails the outputs is pulled. As it is hard to exactly match the resistance in p-type and n-type pull-up/pull-down transistors, the preset circuit will generate both even and odd harmonics on the differential output.

6.4.3 Comparator

In-system simulations of the comparator shows that the toggling delay after the input crossing is approximately 400 ps. This delay can easily be made shorter, but it is costly in terms of power consumption.

Sadly, the comparator delay seems to have some signal dependence, as the comparator delay varies from 360-440ps during a period of the input signal, which will result in a signal-dependent overshoot which creates harmonic distortion.

The varying delay might come from the the way CBSC operates, because the comparator inputs in the charging phase start on a voltage that is dependent on the previous output voltage as shown for $V_x[n-1/2]$ in Appendix A. This can cause some transistors to be in cutoff or in the linear region when the charging begins. The time to reach steady-state can then become dependent on the value of the previous sample.

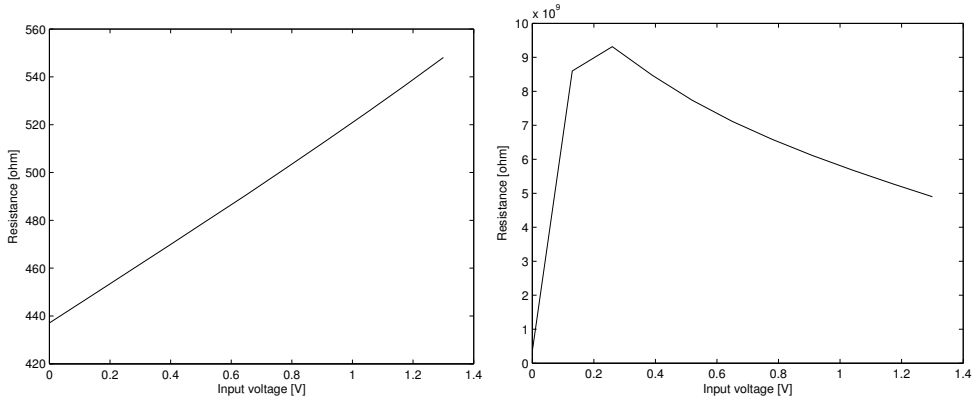
A way to reduce this effect is to increase the current in the input transistors so that steady-state operation is reached faster. This will reduce the signal dependence, but it will not remove it entirely. Another alternative might be to use a very high-speed preamplifier together with a positive feedback decision circuit [18] before the selfbiased amplifier. Signal dependence should not be an issue then, but it can increase the total comparator delay.

6.4.4 Switches

The switch on-resistance is simulated by running a transient simulation for 20 ns, turning the switch on and off with the clock generator to ensure all nodes are properly charged. Both inputs of the switch are the connected to a DC voltage and an AC analysis during the transient simulation is used to extract the resistance at 1Hz. Figure 6.3 shows a plot of the on/off resistances across the entire supply range. The on-resistance varies linearly with about 110Ω across the entire supply range, while the off resistance is several MΩ when the switch is turned off.

The switches is found to be contributing to the even-harmonic distortion in Figure 6.1. The main reason for this is that the gate voltage on the switch is $V_{gate,switch} \approx V_{in,absolute} + V_{DD}$. For a differential signal, the gate voltage on the two equivalent switches will be different. When the switch turns off, the gate voltage is pulled to absolute ground. The total charge injected across the gate capacitance is then $Q = C_{gate,switch} \cdot V_{gate,switch}$, which is not equal for the two differential paths.

Another reason for even harmonic distortion is because of the varying on-resistance. This causes the settling error in each of the differential paths to become different. However, as the resistance across the entire voltage range is less then the maximum resistance calculated in section 5.4, this should not affect performance to a large degree.



(a) (b)

Figure 6.3: AC resistance of bootstrapped switch across the supply voltage range when switch is turned on (a) and off (b).

Chapter 7

Conclusion and further work

For modern nano-scale process technologies, creating high-performance low power circuits is getting more difficult as the minimum geometries and the supply voltage decreases. One suggested way of overcoming this is to introduce new circuit topologies as in the case of comparator-based switched-capacitor circuits. This topology takes advantage of the increased speed in modern technologies and does not need high-gain amplifiers, something which makes it ideal for scaling. Issues such as linear current sources are introduced instead, but this is easier to achieve since there are fewer things constraining the design as the stability issue of amplifiers is removed.

The work of this thesis is to develop a set of basic design equations needed to implement a comparator-based integrator for use in $\Delta\Sigma$ ADCs. An input integrator for a high-performance modulator has been implemented at transistor level which targeted a SNR of 80dB and a 1.5MHz bandwidth with a power consumption of less than 0.9mW.

Each of the separate components works as intended with good performance but since a complete closed-loop modulator is not implemented, the simulation results are not accurate. Open-loop simulations need a calibration circuit running continuously to avoid saturating the integrator, which gives severe distortion of the output signal. Therefore, the maximum SNR found is as low as around 39dB.

The power consumption of the implemented modules gives a total power consumption of about 0.43mW, which is well within the requirements. However, this is not included several modules which are implemented as ideal modules.

The CBSC topology introduces many new challenges compared to the regular opamp-based circuits, mainly because of the large transients and the high speed needed by each of the components. This causes the analysis of comparator-based circuits to be much more complex than for opamp-based circuits, especially regarding noise where the analysis is dependent on the comparator topology.

Still, comparator-based circuits is a fairly new topology and the performance will probably become better in the years to come.

7.1 Further work

To have a measure of the performance the work of this thesis has in a $\Delta\Sigma$ modulator, an ideal model of a modulator should be created. This can easily be done with Verilog-A and can be used to give fast answers of how non-idealities of the CBSC integrator affect the total system performance.

One important issue still remaining on CBSC is a thorough analysis on variations in process, voltages and temperature. There are still no publications analyzing this and the effect it has on circuit performance, but these issues can be severe with regards to the yield of circuits using CBSC.

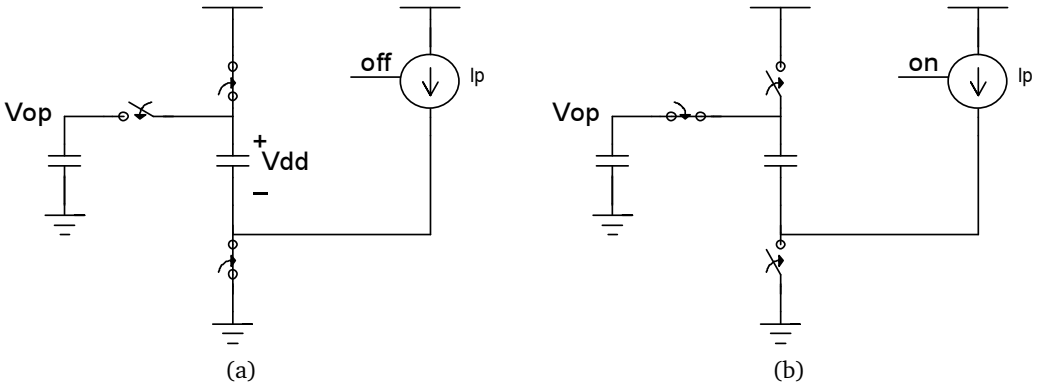


Figure 7.1: Current source off while charging the "bootstrapping" capacitor to V_{DD} (a) and current source enabled with capacitor connected between output and source (b)

What should also be considered are new topologies for creating current sources that are linear across a large output voltage range. One suggestion that should be analyzed is to increase the voltage across the current sources so that the output resistance would be large and almost constant over the entire output range. This could be done as depicted in Figure 7.1, by using a bootstrapping capacitor and charging the output node through this. Since the output voltage ramp starts at 0V, the voltage across the current source would start at $2V_{DD}$, giving a very linear output current for a larger output range than for a standalone current source.

The issue with this is that the voltage on top of the switch connected to ground will be negative. This prevents the use of a regular NMOS switch, as there will be a forward-biased pn-junction causing a severe current leakage into the substrate. Ways of implementing a switch like this could help on linearizing the current sources used in CBSC.

Appendix A

Proof - Principle of CBSC Integrator operation

The equations are set up denoting the signals as single-ended, as shown in Figure A.1.

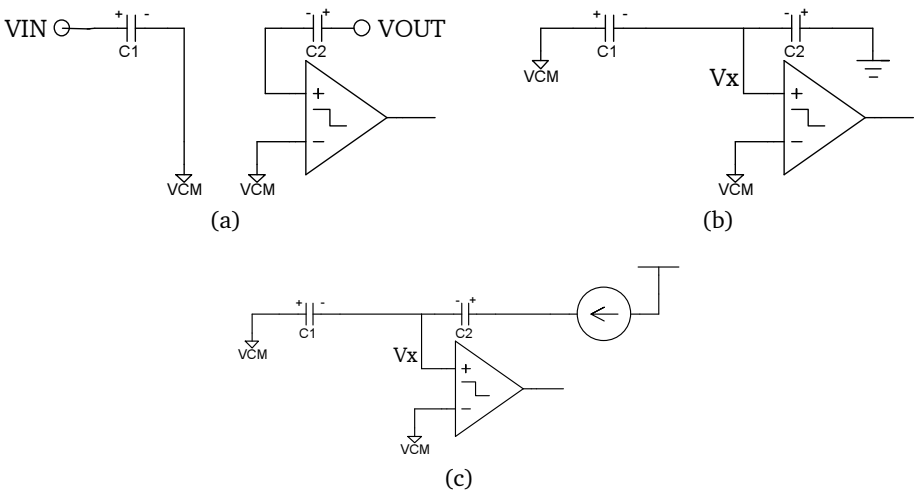


Figure A.1: Equivalent circuits for the CBSC operation. Sample phase(a), preset phase (b) and the charge transfer phase(c)

The end of the charge transfer phase are denoted as [n], while the sampling phase are denoted as [n-1]. The voltages right before the charging begin(preset phase) are denoted as phase [n-1/2].

Charge preservation from the sampling phase to the preset phase can be set up to find the voltage at node $V_x[n-\frac{1}{2}]$: The output node is pulled to absolute ground in the preset phase, which gives a output voltage of $-V_{cm}$, given a mid-rail common mode voltage.

$$C_1(V_{in}[n-1]-0)+C_2(V_o[n-1]-0)=C_1(0-V_x[n-\frac{1}{2}])+C_2(-V_{cm}-V_x[n-\frac{1}{2}]) \quad \text{(A.1)}$$

which yields

$$V_x[n-\frac{1}{2}] = -\frac{C_1 V_{in}[n-1] + C_2 V_o[n-1] + C_2 V_{cm}}{C_1 + C_2} \tag{A.2}$$

To discharge C_1, the total charge that is needed is $C_1 V_x$, and the same current goes through C_2 with opposite sign:

$$C_2 V_o[n] = Q_{C2[n-1]} - C_1 V_x[n-\frac{1}{2}] = C2(-V_{cm} - V_x[n-\frac{1}{2}]) - C_1 V_x[n-\frac{1}{2}] \tag{A.3}$$

Sorting this yields

$$C_2 V_o[n] = C_1 V_{in}[n-1] + C_2 V_o[n-1] \tag{A.4}$$

which, after taking the z-transform and sorting gives the well-known integrator transfer function:

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{A.5}$$

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Acronyms and Abbreviations

Transistor parameters and effects

Symbol	*Name*
C_{ox}	Oxide capacitance per area
NBTI	Negative Bias Temperature Instability

Performance measures

Symbol	*Name*
ENOB	Effective number of bits
PSD	Power spectral density
SNDR	Signal to noise and distortion ratio
SNR_p	Peak signal to noise ratio
SNR	Signal to noise ratio

Other

Symbol	*Name*
CBSC	Comparator-based switched-capacitor circuit
CMFB	Common-mode feedback
DAC	Digital to analog converter
$\Delta\Sigma$	Delta Sigma Modulator
f_s	Sampling frequency
OL	Overloading factor
RMS	Root Mean Square
SC	Switched capacitor