Modeling of Drain Current and Intrinsic Capacitances in Nanoscale Double-Gate and Gate-All-Around MOSFETs

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Preface

The thesis is submitted in fulfillment of the requirements for the degree Philosophiae Doctor at the Norwegian University of Science and Technology. The work has mainly been carried out at University Graduate Center, Kjeller and partly at Universitat Rovira i Virgili, Tarragona, Spain. I have been part of the project Smart Micro Systems for Diagnostic Imaging in Medicine (SMIDA), which is funded by the Norwegian Research Council.

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Completion of my Ph.D. program is certainly a joint accomplishment with my wife, Siw, since only her love, understanding and encouragement has made it possible.

Summary

A precise modeling framework for short-channel nanoscale double gate (DG) and gate-all-around (GAA) MOSFETs is presented covering all operating regimes from subthreshold to strong inversion.

In the subthreshold regime, the modeling of the electrostatics of the DG MOSFET is based on a conformal mapping analysis. This analytical 2D solution of Laplace's equation gives the inter-electrode capacitive coupling. The GAA MOSFET is a 3D structure to which the 2D conformal mapping technique is not directly applicable. However, due to the structural similarities, the DG calculations can also be applied with a high degree of precision to the cylindrical GAA MOSFET by performing a simple geometric scaling transformation to account for the difference in gate control in the two devices.

Near and above threshold, self-consistent procedures invoking the the 2D/3D Poisson's equation in combination with boundary conditions and suitable modeling expressions are used to model the electrostatics of the two devices.

The drain current is calculated as part of the self-consistent treatment, and based on the precise modeling of the 2D/3D electrostatics the intrinsic capacitances can also be extracted. The resulting electrostatics, drift diffusion current and intrinsic capacitances are in excellent agreement with numerical simulations.

A compact subthreshold drain current model for the GAA MOSFET is presented. Additionally, a parameterized model for drain current with all parameters extracted from the modeling framework is described. These are two examples of compact models suitable for inclusion in circuit simulators.

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Notation

ε_0	Permittivity of vacuum [$\mathrm{C^2N^{-1}m^{-2}}$]
ε_{ox}	Relative permittivity of gate-insulator
ε_{si}	Relative permittivity of silicon
λ_{DG}	Penetration depth of the electrostatic influence from source and drain of the double gate MOSFET [m]
λ_{GAA}	Penetration depth of the electrostatic influence from source and drain of the gate-all-around MOSFET [m]
μ_n	Electron mobility [$\mathrm{m^2V^{-1}s^{-1}}$]
τ_n	Momentum relaxation time of electrons [s]
ϕ_c	Center potential [V]
Φ_m	Metal work function [J]
φ	Total electrostatic potential, $\varphi = \varphi_1 + \varphi_2$ [V]
φ_1	Contribution from inversion charge to the electrostatic potential [V]
φ_2	Contribution from inter-electrode coupling to the electrostatic potential [V]
φ_{ox}	Potential-profile of oxide gap [V]
Ψ_s	Potential at silicon-insulator interface [V]
χ_s	Electron affinity of the semiconductor [J]
C_{ox}	Oxide capacitance $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ [$\mathrm{Fm^{-2}}$]
C_{si}	Silicon capacitance $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$ [$\mathrm{Fm^{-2}}$]
C_{XY}	Trans- $(X \neq Y)$ and self- $(X = Y)$ capacitances [F]
D_n	Electron diffusion coefficient [$\mathrm{m^2s^{-1}}$]
$\mathbf{E}$	Electric field [$\mathrm{N\ C^{-1}}$]
E_F	Fermi Energy level [J]
E_g	Band gap energy [J]
$\hbar$	Reduced Planck's Constant [Js]
I_{ds}	Drain current [A]
J_{ds}	Drain current density (per unit channel width) [$\mathrm{Am^{-1}}$]

k	Modulus of elliptic integral
$\hat{k}$	Complimentary modulus of elliptic integral, $\hat{k}^2 = 1 - k^2$
k_B	Boltzmann's constant [JK^{-1}]
L	Gate length [m]
m_n^*	Effective electron mass [kg]
n	Electron density [m^{-3}]
N_a	Acceptor doping density [m^{-3}]
N_{ceff}	Effective density of states for electrons [m^{-3}]
n_i	Intrinsic electron density [m^{-3}]
n_s	Sheet electron density [m^{-2}]
N_{veff}	Effective density of states for holes [m^{-3}]
q	Electron charge [C]
Q_X	Charge associated with electrode X [Cm^{-1}]
r_{ox}	Equivalent cylindrical oxide thickness of GAA [m]
r'_{ox}	Effective oxide thickness of GAA, $r'_{ox} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} r_{ox}$ [m]
r_{si}	Radius of GAA MOSFET silicon substrate [m]
T	Absolute temperature [K]
t_{ox}	Oxide thickness [m]
t'_{ox}	Effective oxide thickness, $t'_{ox} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}$ [m]
t_{si}	Silicon body thickness of DG MOSFET [m]
V_{bi}	Built in voltage [V]
V_D	Drain voltage, $V_D = V_{bi} + V_{ds}$, [V]
V_{ds}	Potential difference between drain and source [V]
V_F	Quasi Fermi potential [V]
V_{FB}	Flat band voltage for the gate [V]
V_G	Gate potential, $V_G = V_{gs} - V_{FB}$ [V]
V_{gs}	Gate potential referred to source potential [V]
v_s	Saturation velocity [ms^{-1}]
V_S	Source voltage, $V_S = V_{bi}$ [V]
V_{th}	Thermal voltage, $V_{th} = \frac{k_B T}{q}$ [V]
W	Channel width [m]

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Chapter 1

Introduction

1.1 Background

In December 1947 the first transistor was presented at the Bell laboratories by William Shockley, John Bardeen and Walter Battain. Since then, and in particular over the last 40 years, the semiconductor technology has developed with an amazing speed. The integrated circuit performance has grown exponentially with the scaling of the MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) dimensions as the primary driver. In high performance logic (i.e. processors) MOSFETs with 25nm physical gate lengths are now in production [1].

At this stage the long-lasting favorite of the industry, the single-gate MOSFET, is reaching its scaling limit, and the search for alternative devices intensifies. In addition to finding a device with superior scaling properties, the industry will look for candidates that can be fabricated with a cost and yield comparable to the present devices. The double-gate (DG) and cylindrical gate-all-around (GAA) MOSFETs are, indeed, two of the most interesting devices to meet these criteria.

The scaling of the single-gate MOSFET into the sub-100nm range has been possible by using for example high doping and steep doping gradients, which is detrimental for the charge carrier mobility. One of the operation merits of thin body and low-doped DG devices is volume inversion in the entire silicon body in all operation regimes. This volume inversion effect enhances charge carrier mobility particularly in the subthreshold regime, where the main channel of charge transport is along the source-to-drain symmetry line [2][3]. When increasing the gate biasing, moving from subthreshold into the

near and above threshold regimes, the current channel will shift from the center to the two silicon-insulator interfaces.

The GAA MOSFET can also, indeed, be designed to benefit from the volume inversion effect. Additionally, the GAA MOSFET obtains better scaling properties compared to the DG MOSFET as the cylindrical gate improves the gate control and suppresses short channel effects [3][4].

Many activities are going on in parallel for the semiconductor technology to continue its development to reach the future expectations of performance. One of these activities is device modeling, which gives a deeper understanding of the physical behavior of the devices. Compact models are also important tools in circuit design and simulation. These new devices pose a new challenge in device modeling as the field pattern is two and three dimensional. This is in contrast to many of the classical single gate 1D models which in their development are based on an increasing number of non-physical fitting parameters of obscure origin.

Another point is that the classical definition of the threshold voltage, which normally marks the onset of the device, loses much of its meaning in the undoped/lightly doped DG an GAA devices, as described in further detail in section 2.2.7.

A new model paradigm based on the specific central physical mechanisms in these kind of devices is therefore desirable and is the inducement to the work presented in this thesis.

1.1.1 Device Scaling - Moore's Law

Moore's Law describes an important trend in the history of computer hardware. It says that the number of transistors that can be inexpensively placed on an integrated circuit is increasing exponentially with time, doubling approximately every two years. The observation was first made by Intel co-founder Gordon E. Moore in 1965. The trend has continued up till today and is not expected to stop for another decade.

Almost every measure of the capabilities of digital electronic devices is linked to Moore's Law, for example processing speed and memory capacity. All of these are improving at roughly exponential rates as well. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy. Moore's Law describes this as a driving force of technological and social change in the late 20th and early 21st century.

1.1.2 Integrated Circuit Design

The evolution of very large scale integration (VLSI) technology has developed to the point where over two billion transistors can be integrated on a single chip[1]. Integrated circuits were normally subsystem components, partitioned by analog and digital boundaries. Now, however, complete systems are integrated on a chip combining both analog and digital functions. Complementary metal-oxide semiconductor (CMOS) technology has become the most widespread in these implementations because it provides density and power savings on the digital side, and a good mix of components for analog design [5].

1.1.3 Technical Computer Aided Design

Process and device simulators are technical computer aided design (TCAD) tools. The TCAD tools apply numerical derivations based on complex equations, such as partial differential equations, to predict the behavior of the device.

The process simulators can predict the structures that result from specified process sequences (such as diffusion and ion implantation), based on the physics and chemistry of the semiconductor processes. Athena from Silvaco is one example of a process simulator.

Numerical device simulators, on the other hand, predict the electrical characteristics that are associated with specified physical structures and bias conditions. This normally involves an iterative solution of Poisson's equation combined with a transport model for a given set of boundary conditions. A common way to accomplish this is by discretizing the 2D surface or 3D volume in a grid, and applying a partial differential equation solver to find solutions at the grid points in an iterative manner. The convergence and accuracy depend on the size an layout of the grid, and the complexity of the applied physical models.

In this work we have not considered the processing steps of the device. However, as experimental data is not readily available for the nanoscale devices considered, we use the Atlas device simulator from Silvaco to verify the accuracy of of our modeling framework. Atlas has a range of models for transport, carrier statistics, material properties, etc. These can be combined in the simulation of a wide range of customized 2D and 3D device geometries.

[1] Intel Itanium (code named Tukwila) was launched in February 2008 as the world's first microprocessor containing more than two billion transistors.

1.1.4 Circuit Simulation

Integrated circuits, unlike board-level designs composed of discrete parts, are impossible to breadboard before manufacture. In addition, the high costs of photolithographic masks and other manufacturing prerequisites make it essential that the circuit is as close to perfect as possible before the integrated circuit is built. Simulating the circuit with a circuit simulator is therefore required to verify circuit operation before manufacturing the integrated circuit.

Tools for simulating the behavior of simple circuits, electronic computer aided design tools (ECAD), began emerging in parallel with the development of integrated circuits. SPICE (Simulation Program with Integrated Circuit Emphasis) was first released in 1972 by Electronics Research Laboratory of the University of California, Berkeley, as a derivative of the CANCER program (Computer Analysis of Non-linear Circuits, Excluding Radiation) [6]. Since then SPICE has gone through several evolutions and is widely used by circuit designers.

One of the key building blocks in SPICE is the device models. Different research groups have steadily provided models and modeling approaches to SPICE, continuously improving the functionality of the simulator. The BSIM MOSFET model invented by the Berkeley group was the industry standard for many years. In 2005, however, the Compact Model Council, which works for standardization of compact models and model interfaces, decided to make the PSP model [7] developed by Phillips semiconductors and Pennsylvania State University, the industry standard.

SPICE simulators come with a selection of models for different semiconductors. The simplest models can be accessed quickly and may give adequate

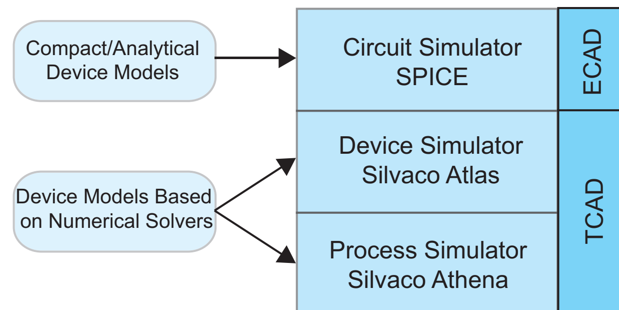

Figure 1.1: Hierarchy of the TCAD and ECAD tools.

results in many situations. For improved accuracy, the more complex models should be applied. These are often characterized by many parameters which must be identified empirically by analyzing measurements or by TCAD simulations. This is time-consuming and a difficult task considering that some models use hundreds of parameters, which cannot always be associated directly with physical mechanisms. Some manufacturers, however, provide ready to use SPICE parameters for their products, and some device simulators come with parameter extraction tools, which can be used directly as input to the SPICE models.

1.1.5 Device Modeling

Figure 1.1 illustrates the hierarchy of the TCAD and ECAD tools as described above. As indicated compact/analytical devices models are the fundamental building blocks of an efficient circuit simulator.

In this thesis, a compact physics based device model is a description of the device behavior in terms of analytical, mathematical expressions. The most efficient models are the ones which only involve explicit analytical expressions. Another approach is based on preprocessing routines which result in parameter look-up tables for fast retrieval and use in simplified parameterized models.

1.2 Objective

The objective of the thesis is to establish a detailed, physically based framework for precise modeling of short-channel DG and GAA MOSFETs. From this modeling scheme we may extract current-voltage and intrinsic capacitance characteristics of the devices. The framework may also serve as a starting point for the development of more compact modeling expressions suitable for use in circuit simulators.

The modeling framework is based on a two- and three-dimensional (2D and 3D) analysis for the DG and GAA MOSFETs, respectively. Short channel effects are intrinsic to this 2D and 3D analysis. The inter-electrode coupling of the DG device is solved analytically for the 2D device geometry, and with appropriate modifications it can also be applied to model the inter-electrode coupling of the 3D GAA device. The effect of the inversion charges are included self-consistently in an iterative procedure.

1.3 Scope

In the endeavor to model the behavior of nanoscale short-channel DG and GAA devices the main challenges are to determine the 2D/3D electrostatics, self-consistent modeling, charge transport, quantum-mechanical effects, gate tunneling and noise. Below follows a summary of to what extent these topics are addressed in this thesis.

2D and 3D electrostatics. In this work we are considering, as an example, a DG and GAA MOSFET with gate length of 25nm and a silicon body thickness/diameter of 12nm, ref. figure 2.1. This length/height ratio implies that there is a significant coupling, not only between the gate contacts but also between the source/drain contacts. Therefore a 2D solution is required to cover these mechanisms. Additionally, the cylindrical geometry of the GAA MOSFET must be properly accounted for with a 3D analysis.

Self-consistent modeling of inversion charge effects. Near and above threshold the electrostatic influence from the inversion charges becomes significant and has to be taken into consideration. We model the inversion charge contribution in a self-consistent manner in accordance with the 2D and 3D Poisson's equation for the DG and GAA MOSFET, respectively.

Charge transport. In nanoscale MOSFETs with channel lengths less than 100nm [8], the relaxation times of the carriers indicate that the drain current will have the character of both drift diffusion and ballistic transport. Numerical simulations, however, indicate that the use of the drift diffusion mechanism with constant mobility, reproduces quite well the current found from more advanced simulations. Hence, in all simulations used for comparison with the present model, we also use the drift diffusion mechanism with constant mobility. This serves the additional purpose of verifying the overall modeling procedures used. Ballistic and quasi-ballistic transport are briefly discussed in the review of models in section 2.2.4, and the drift-diffusion model is compared to the more sophisticated transport formalisms in chapter 5.

Quantum mechanical effects. When device dimensions are larger than 10nm, classical theory is still applicable [9], and the modeling framework presented in this thesis is based on classical theory. For smaller dimensions, quantum confinement has to be considered, and in section 2.2.3 a simplified quantum confinement model is briefly reviewed.

Gate tunneling. The modeling of gate tunneling is considered to be beyond the scope of this work. We have considered a high-κ dielectric with a relative permittivity of 7 and a thickness of 1.6nm, in which case the tunneling current

is quite small [10].

Noise. Noise modeling is beyond the scope of the present work.

1.4 List of Publications and Own Contributions

In my work I have contributed to the following international journal articles, conference proceedings and posters.

1.4.1 International Journal Articles

1. S. Kolberg, H. Børli and T. A. Fjeldly, "Modeling, Verification and Comparison of Short-Channel Double Gate and Gate-All-Around MOSFETs", *J. Math. and Comp. in Simulations*, doi:10.1016/j.matcom.2007.09.011, 2007.

2. H. Børli, S. Kolberg and T. A. Fjeldly, "Physics based Modeling of Short-Channel Nanowire MOSFET", *Journal of Physics: Conference Series*, vol. 100, no 52054, 2008. Available online: www.iop.org.

3. H. Børli, S. Kolberg, T.A. Fjeldly and B. Iñiguez, "Precise Modeling Framework for Short-Channel Double-Gate and Gate-All-Around MOSFETs", *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2678-2686, October 2008.

4. H. Børli, K. Vinkenes, T. A. Fjeldly, "Physics Based Capacitance Modeling of Short-Channel Double-Gate MOSFETs", *Physica Status Solidi*, pp. 1-4, 2008, doi:10.1002/pssc.200780124.

5. S. Kolberg, H. Børli, T. A. Fjeldly, "Compact Current Modeling of Short-Channel Multiple Gate MOSFETs", *Physica Status Solidi*, pp. 1-4, 2008, doi: 10.1002/pssc.200880125.

6. H. Børli, S. Kolberg and T. A. Fjeldly, "Capacitance Modeling of Short-Channel Double-Gate MOSFETs", *Solid State Electronics*, vol. 52, 2008, pp. 1486-1490, doi: 10.1016/j.sse.2008.06.022.

7. U. Monga, H. Børli and T. A. Fjeldly, "Compact Subthreshold Current and Capacitance Modeling of Short-Channel Double-Gate MOSFETs", *Mathematical and Computer Modelling*, submitted.

1.4.2 International Conference Proceedings

1. H. Børli, S. Kolberg, and T. A. Fjeldly, "Analytical Modeling Framework for Short-Channel DG and GAA MOSFETs," *Proc. NSTI-Nanotech 2007*, Santa Clara, CA, vol. 3, pp. 505-509, May 2007.
2. H. Børli, S. Kolberg and T. A. Fjeldly, "Physics Based Current and Capacitance Model of Short-Channel Double Gate and Gate-All-Around MOSFETs", *Proc. 2nd IEEE Int. Nanoelectronics Conf. (INEC 2008)*, pp. 844-849, Shanghai, China, March 2008. IEEE Ref. 978-1-4244-1573-1/08.
3. H. Børli, S. Kolberg, T. A. Fjeldly and B. Iñiguez, "Current and Capacitance Modeling of Short-Channel DG MOSFETs", *Proc. 7th IEEE Int. Caribbean Conf. on Devices, Circuits and Systems (ICCDCS 2008)*, no. 19, Cancún, Mexico, April, 2008. IEEE Ref. 978-1-4244-1957-9/08.
4. H. Børli, S. Kolberg and T.A. Fjeldly, "Capacitance Modeling of Short-Channel DG and GAA MOSFETs", *NSTI-Nanotech 2008*, vol. 3, pp. 745-749, June 2008.

1.4.3 Posters

1. H. Børli, S. Kolberg, and T. A. Fjeldly, "Development and Verification of a Precise Compact Model for Short-Channel Gate-All-Around MOSFETs," MOS-AK Workshop, Montreux, September 2006 [Poster].
2. S. Kolberg, H. Børli, and T. A. Fjeldly, "Verification of a Novel 2D Compact Model for Short-Channel Double Gate MOSFETs," MOS-AK Workshop, Montreux, September 2006 [Poster].
3. H. Børli, S. Kolberg and T. A. Fjeldly, "Analytical Modeling Framework for Short-Channel DG and GAA MOSFETs", DEEEA Workshop, Tarragona, July 2007 [Poster].
4. H. Børli and T. A. Fjeldly, "Self-Consistent 2D Modeling of Short-Channel Nanoscale DG and GAA MOSFETs", COMON Meeting, Eindhoven, April 2008 [Poster].

1.4.4 Own Contributions

In these publications my main contributions are summarized below.

- An analytical 2D solution of the Laplace equation for the DG MOSFET applying conformal mapping techniques, has previously been presented [11]. I have presented a new method of mapping the solution of the DG electrostatics into the longitudinal cross-section through the cylindrical axis of the GAA. This technique, which is based on the structural similarities between the two devices and their difference in gate control, does not give an exact solution of the 3D Laplace equation of the GAA MOSFET. However, it agrees very well with numerical simulations.

- The 2D solution of the Laplace equation of the DG MOSFET, presented by [11], has been improved to include a corner correction.The electrostatics close to the corner does not significantly influence the sub-threshold current calculations, but is more important for the intrinsic capacitance modeling.This corner correction also applies to the quasi-3D Laplace solution of the GAA MOSFET.

- The self-consistent calculation of the electrostatics of the DG MOSFET in the near threshold regime has been improved based on the work of [11]. This method has also been extended to model the near threshold electrostatics of the GAA MOSFET, properly accounting for the cylindrical geometry.

- A self-consistent method has also been developed to calculate the electrostatics in the above threshold regime.

- Based on this modeling framework with a two- and three-dimensional analysis of the electrostatics for the DG and GAA MOSFET respectively, the drift-diffusion current is modeled in all operation regimes.

- The framework model is also applied to model the intrinsic capacitances of the DG and GAA MOSFETs in all operation regimes.

Additionally, this thesis presents a new compact, analytical subthreshold current model for the GAA MOSFET in section 3.5 (not previously published).

1.5 Outline of Thesis

In this thesis we present a technique for 2D and 3D modeling of short-channel nanoscale DG and GAA MOSFETs. In low-doped devices working in the subthreshold regime, the potential distribution is dominated by the inter-electrode coupling between the body contacts. This body potential is determined by an analytical solution of the 2D Laplace equation using the technique of conformal mapping. Due to the structural similarities between the DG and GAA MOSFET this 2D solution of Laplace's equation can also be mapped into the longitudinal cross section of the GAA accounting for the difference in gate control between the two MOSFET geometries. Near and above threshold the influence of the inversion charge on the electrostatics is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson's equation. Based on the modeled electrostatics, we can calculate the drain current and the intrinsic capacitances of the device. Throughout the thesis, the modeling results are verified against the numerical simulator Atlas developed by Silvaco.

In chapter 2, the properties of the DG and GAA devices are defined. Moreover, essential physics and existing models related to these devices are reviewed. The models and theory introduced here represent much of the foundation for the modeling work in the subsequent chapters.

In chapter 3 the derivation of the inter-electrode electrostatics of the DG and GAA MOSFET is presented. The 2D Laplace equation of the DG device is solved analytically by using a conformal mapping technique. This technique is not directly applicable to the 3D structure of the GAA MOSFET, however, by accounting for the difference in gate control the 2D DG solution can also be applied for the GAA MOSFET. An extensive analysis of the error introduced by these simplifications is provided. The inter-electrode contribution is dominating in the sub-threshold regime, and the modeled sub-threshold drain current is derived and compared with numerical simulations. A compact, analytical subthreshold drain current model is presented at the end of the chapter.

In chapter 4 follows a description of the electrostatic modeling of the inversion charge of the DG and GAA devices. In accordance with the superposition principle the Laplace solution of the inter-electrode electrostatics can be separated from Poisson's equation. Near and above threshold the mobile charge carriers influence significantly the device electrostatics, and is modeled in a self-consistent manner in accordance with Poisson's equation. The quasi-Fermi potential and the drift diffusion current are included in this

self-consistent, iterative procedure.

In chapter 5 the drain current modeling in all operation regimes is summarized. Furthermore, an example of a parameterized, compact current-voltage model is presented where the parameters are extracted from the full modeling framework. At the end of the chapter the drift diffusion transport mechanism is compared to more sophisticated transport models.

In chapter 6 the modeling of the intrinsic capacitances of the DG and GAA MOSFETs is presented. If we can consider the DG and GAA as three terminal devices, they can be described with 9 self- and trans-capacitances. In the subthreshold regime the analytical solution of the Laplace equation gives a compact and analytical model of the capacitances of the DG device. Accounting for the improved gate control, the GAA subthreshold capacitances can be determined in a similar fashion. The effect of the inversion charge must be accounted for in the near and above threshold regimes, and the self-consistent analysis of the electrostatics in chapter 4 is applied to determine the capacitances in these regions of operation. We assume that the gate overlaps with source and drain, and at the end of the chapter a brief analysis of the extrinsic overlap capacitances is shown.

Finally chapter 7 contains the conclusion and chapter 8 discuss possible future work.

Chapter 2

Review of DG and GAA MOSFET Models

Double-gate (DG) and gate-all-around (GAA) transistors are considered to be very attractive options to improve the performance of CMOS devices and to overcome some of the difficulties encountered in further downscaling of MOSFETs into the sub-50-nm gate-length regime. Scaling of single-gate MOSFETs into the sub-100nm range, has been possible by for example using high doping and steep doping gradients. The DG and GAA MOSFETs can be designed with low body doping density, avoiding some of the detrimental effects to the charge carrier mobility caused by higher doping levels.

Therefore, considerable effort has been invested in the modeling of the DG and GAA devices recently, and this chapter gives a brief review of the main development in this area. In particular we focus on different approaches for modeling the current and capacitances of these devices [9][12]. First, however, the layout and properties of the DG and GAA devices are given, and then we review essential physics, which forms the basis of the modeling approaches.

2.1 Layout and Properties of DG and GAA MOSFETs

The schematic cross section of the DG MOSFET is illustrated to the left in figure 2.1. As indicated x is the direction from source to drain, parallel to the gate contact and y the direction perpendicular to the gate. The third dimension of the DG device, the width, W, is typically much larger than the

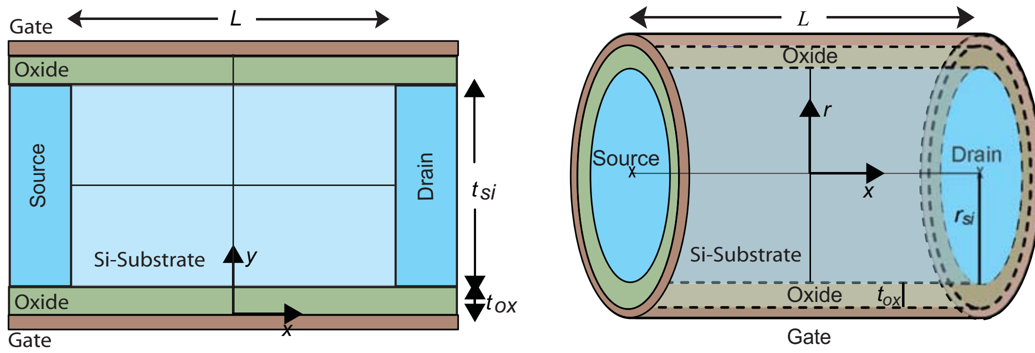

Figure 2.1: Schematic structure of the DG MOSFET (left) and GAA MOSFET (right).

other dimensions. The cylindrical GAA MOSFET is illustrated to the right in figure 2.1. Here x and r are the axial and radial coordinates, as indicated.

The properties of the DG and GAA devices considered are based on the template of the European Union research project, Silicon Nano-devices (SINANO) [11]. If not otherwise specified, the gate length is $L = 25$nm, the silicon thickness/diameter is $t_{si} = 2r_{si} = 12$nm, and the oxide thickness is $t_{ox} = 1.6$nm. We apply a p-type uniform silicon substrate doping $N_a = 1 \cdot 10^{15}\text{cm}^{-3}$, and a high-$\kappa$ gate insulator with a dielectric permittivity of $\varepsilon_{ox} = 7\varepsilon_0$, where ε_0 is the dielectric permittivity of vacuum. Idealized Schottky contacts with work function, $\Phi_m = 4.17$eV (corresponding to that of n+ silicon) are assumed for the source and drain, and a near mid-gap gate material with work function of 4.53eV at the gate contacts. This ensures equipotential surfaces on all the device contacts.

Effective oxide thickness

The calculations are simplified by using the well known technique of replacing the insulator layers of the DG device by electrostatically equivalent silicon layers with an effective thickness

$$t'_{ox} = t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}} \tag{2.1}$$

where $\varepsilon_{si} = 11.8\varepsilon_0$ is the dielectric permittivity of silicon. In this way we obtain a continuous electric field across the silicon-insulator interface. This scaling assumes that the electric field in the oxide is dominated by its y-

component, and that the lateral x-component can be ignored. In the central gate-region this is a very good assumption. In the corner regions of the device, however, the x-component of the electric field becomes more significant and results in a small error close to the corners.

A similar oxide scaling is applied in the GAA device. In cylindrical coordinates the oxide thickness is given by

$$r_{ox} = r_{si} \ln \left(1 + \frac{t_{ox}}{r_{si}}\right) \tag{2.2}$$

where r_{si} is the radius of the silicon substrate. Similarly to the DG device (2.1), r_{ox} is scaled so that the insulator material becomes electrostatically equivalent to the silicon substrate, i.e. $r'_{ox} = r_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}$. As for the DG this oxide scaling introduces a small error where the x-component of the electric field is significant.

2.2 Essential Physics

Some essential physics is here reviewed, in order to establish the foundation of the models that will be described in the subsequent sections and chapters.

2.2.1 Poisson's Equation

The electrostatic potential, $\varphi(x,y)$, in the semiconductor body of the DG MOSFET is given by the 2D Poisson's equation

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}}\left(N_a + n\right), \tag{2.3}$$

where $\varphi(x,y)$ is referred to the Fermi potential at the source contact, N_a is the acceptor doping density in the silicon body (n-channel device) and n is the mobile charge density.

The cylindrical GAA MOSFET is a 3D device, whose electrostatic potential, $\varphi(x,r)$, is given by Poisson's equation with cylindrical co-ordinates.

$$\frac{\partial^2\varphi(x,r)}{\partial x^2} + \frac{\partial^2\varphi(x,r)}{\partial r^2} + \frac{1}{r}\frac{\partial\varphi(x,r)}{\partial r} = \frac{q}{\varepsilon_{si}}\left(N_a + n\right) \tag{2.4}$$

For lightly doped devices, i.e. $N_a < 10^{16}\text{cm}^{-3}$ [13], the term N_a in equation (2.3) and (2.4) can often be ignored. In moderate to strong inversion the

inversion charge will normally be the dominant term, i.e. $n \gg N_a$. In the subthreshold regime, the depletion charge, N_a, will eventually become comparable to the inversion charge. However, under these bias conditions, the inter-electrode coupling will normally dominate the electrostatics. Therefore, a light doping represents relatively few carriers in the thin body of the DG and GAA devices, and the effect of the ionized impurities can be considered negligible in all normal operating regimes of the device.

The 2D Poisson's equation of equation (2.3) can be separated into a simplified Poisson equation and a Laplace equation for the mobile charge contribution and the inter-electrode coupling, respectively, in accordance with the superposition principle. I.e., for the DG device

$$\frac{\partial^2 \varphi_1}{\partial x^2} + \frac{\partial^2 \varphi_1}{\partial y^2} = \frac{qn}{\varepsilon_{si}} \tag{2.5}$$

$$\frac{\partial^2 \varphi_2}{\partial x^2} + \frac{\partial^2 \varphi_2}{\partial y^2} = 0 \tag{2.6}$$

where φ_1 can be related to the inversion charge, and φ_2 to the inter-electrode coupling. The electrostatic potentials of the source, drain and gate contacts are included in the boundary conditions of the Laplace equation (2.6). Therefore we obtain simplified boundary conditions of the Poisson's equation (2.5), where the boundary potentials can be set to zero. The total potential given as the sum of these two contributions $\varphi = \varphi_1 + \varphi_2$. The 3D Poisson's equation (2.4) can be separated in a similar manner.

The inter-electrode contribution, φ_2, can be found analytically as described in chapter 3. The inversion charge contribution, φ_1, is found in a self-consistent procedure as described in chapter 4.

2.2.2 Fermi-Dirac and Boltzmann Statistics

Electrons in solids obey the Fermi-Dirac distribution function, $f(E)$, where E is the energy of a given electron state. The Fermi-Dirac distribution simplifies to Boltzmann statistics when the Fermi energy level, E_F, lies several k_BT above the valence band (for acceptor type doping),

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_BT}\right)} \approx \exp\left(-\frac{E - E_F}{k_BT}\right) \tag{2.7}$$

where k_B is Boltzmann's constant and T is the absolute temperature. This is normally a good assumption for low to moderate doping concentrations.

Using classical Boltzmann statistics, the mobile charge density, n, in (2.3) and (2.4) is given by

$$n = \frac{n_i^2}{N_a} \exp\left(\frac{\varphi - V_F}{V_{th}}\right) \tag{2.8}$$

where n_i is the intrinsic carrier density for undoped silicon, φ is the total electrostatic potential, $V_{th} = \frac{k_B T}{q}$ is the thermal voltage and V_F is the quasi-Fermi potential referred to the applied source potential. We assume that V_F is constant over any given cross-section perpendicular to the x-axis.

2.2.3 Quantum Inversion Charge

With the incessant down-scaling of the MOSFET we eventually reach a limit where the quantum effect causes the energy bands in the channel to split. The quantum inversion charge is distributed in accordance with Fermi-Dirac statistics (ref. equation (2.7)) over a number of discrete energy levels, E_j.

As an illustration, a 1D quantum inversion carrier concentration assuming an idealized flat potential well with infinite walls is given by

$$n = \frac{m_n}{\pi\hbar^2} k_B T \sum_{j=1}^{l} \ln\left[1 + \exp\left(\frac{E_F - E_j}{k_B T}\right)\right] \tag{2.9}$$

Here $\hbar$ is the reduced Planck constant, E_j is the lowest energy of sub-band j measured relative to the conduction band and m_n is the density of states effective mass. This idealized model does not distinguish between differences in effective mass in the sub-bands. Additionally, accurate modeling of the electrostatic potential, particularly close to the barrier between source and drain, is crucial for obtaining a good estimate of the drain current. In this approach, however, the potential is assumed to be flat in the x-direction. This is therefore a very simplified model, which is presented here only as an illustration of some of the differences between a classical an a quantum-mechanical approach.

Assuming $t_{si} < L$ quantum effects will first be observed in the y-direction of the DG MOSFET (r-direction of the GAA MOSFET). Quantum effects become significant when the silicon substrate thickness becomes smaller than 10nm [14]. Here, however, the device dimensions considered are such that a classical treatment of the electron distribution is justified.

2.2.4 Transport Models

Drift Diffusion Model

One of the simplest models of charge transport is the drift-diffusion model with constant mobility. This model is based on the assumption that electron velocity in the semiconductor is proportional to the local, instantaneous electric field [15].

First we introduce the charge sheet density, $n_s(x)$, which is the charge density, $n(x, y)$, integrated with respect to y

$$n_s(x) = \int n(x, y)dy \tag{2.10}$$

The drift diffusion current density (current per unit channel width) can be expressed in terms of the quasi-Fermi potential, V_F, which is assumed to be constant over any given cross-section perpendicular to the x-axis.

$$J_{ds} = q\mu_n n_s(x)\frac{dV_F(x)}{dx} \tag{2.11}$$

Here q is the electron charge, $n_s(x)$ is the charge sheet density of equation (2.10), and μ_n is the constant electron mobility given by

$$\mu_n = \frac{q\tau_n}{m_n^*} \tag{2.12}$$

where m_n^* is the effective mass of electrons, and τ_n is the momentum relaxation time, which is an average measure of how fast the carrier momentum changes due to collisions. These collisions can be caused by lattice vibrations of the atoms (phonons), surface scattering, the presence of impurities and other crystal defects.

If equation (2.8) is solved with respect to V_F, we obtain, $V_F = \varphi - V_{th}\ln\left(\frac{nN_a}{n_i^2}\right)$. If this is inserted in (2.11) applying the charge sheet density of (2.10), we obtain the drift diffusion equation

$$J_{ds} = -qn_s\mu_n\mathbf{E}(x) - qD_n\frac{dn_s(x)}{dx} \tag{2.13}$$

where $\mathbf{E}(x) = -\frac{d\varphi}{dx}$ is the electric field and $D_n = \frac{\mu_n k_B T}{q}$ is the electron diffusion coefficient. In equation (2.13) the first term can be associated with the drift current and the second term with the diffusion current.

Velocity Saturation

The electron drift velocity is represented by $v(\mathbf{E}) = \mu_n \mathbf{E}$ in equation (2.13). This linear dependence gives a reasonable estimate for low field conditions, but is no longer valid at high fields.

In high fields the electrons gain considerable energy from the field. Similarly, the exchange of energy and momentum between the carriers and the crystal increases, and the net effect in most semiconductors is that the drift velocity saturates. A common model for the velocity saturation is given by [15]

$$v(\mathbf{E}) = \frac{\mu_n \mathbf{E}}{\left[1 + \left(\frac{\mu_n \mathbf{E}}{v_s}\right)^m\right]^{1/m}} \tag{2.14}$$

where m is a fitting parameter (i.e. $m \approx 2$ for electrons in silicon) and v_s is the saturation velocity, which is equal to approximately $1 \cdot 10^7$cm/s in silicon at room temperature.

Energy Transport and Hydrodynamic Models

The energy transport (ET) model follows the derivation by Stratton [16][17] which is obtained starting from the Boltzmann transport equation (BTE). The hydrodynamic (HD) model [8] is a higher order solution to the general BTE, compared to the drift-diffusion models described above. A set of simplified transport equations of carrier density, momentum and energy, are applied in order to find an approximate solution of the BTE.

Both the HD and ET models include non-stationary transport effects such as velocity overshoot, diffusion associated with carrier temperature and the dependence of impact ionization rates of carrier energy distributions. One of the key differences between the HD and ET models is that the former uses macroscopic relaxation times, which describe the ensemble of carriers, while the latter uses microscopic relaxation times, which describe how individual carriers scatter [8].

Ballistic Transport

As the channel lengths continue to shrink, they will eventually become so small that carriers may traverse from source to drain without scattering [18][19]. Effects of this so-called ballistic transport, occurs in devices with channel length shorter than the mean free path, which is about 100nm for

silicon at room temperature [8]. The drain current will therefore have the character of both 'collision-dominated' drift diffusion and 'collision-free' ballistic current, with an increasing shift towards the latter with decreasing gate lengths.

2.2.5 Capacitance Model

The four-terminal DG MOSFET can be described in terms of 16 trans- and self-capacitances, C_{XY}, of which 9 are independent owing to the principle of charge conservation [20][21]. Here, C_{XY} reflects the change of charge assigned to electrode X for a small variation in voltage applied to terminal Y according to the definition

$$C_{XY} = \pm \frac{\partial Q_X}{\partial V_Y} \tag{2.15}$$

where the plus sign is used for $X = Y$ (self-capacitances), and the minus sign is used for $X \neq Y$ (trans-capacitances). These signs are chosen to keep all of the capacitance terms positive [21].

The GAA MOSFET is a tree-terminal device and so is the DG when applying symmetric gate biasing. For this case, the number of capacitances reduces to 9 of which 4 are independent and can be represented by a 3×3 matrix

$$\mathbf{C} = \begin{bmatrix} C_{GG} & -C_{SG} & -C_{DG} \\ -C_{GS} & C_{SS} & -C_{DS} \\ -C_{GD} & -C_{SD} & C_{DD} \end{bmatrix} \tag{2.16}$$

where all the rows and columns should sum to zero for the device description to be charge conservative. The equivalent circuit of the three-terminal device is shown in figure 2.2 [15].

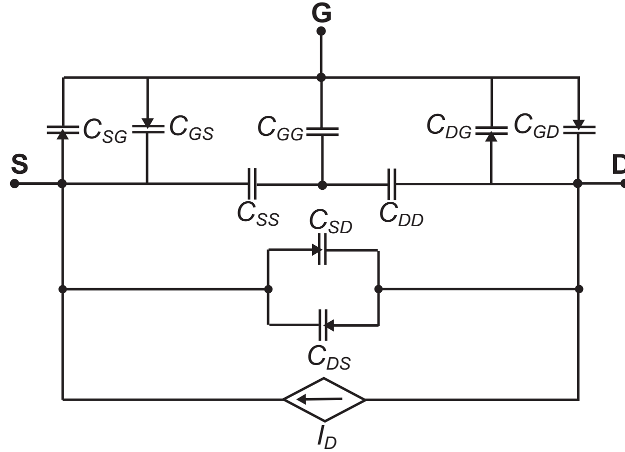

Figure 2.2: Equivalent circuit of charge conserving intrinsic capacitances for three-terminal MOSFETs [15].

2.2.6 Substrate Doping

In DG and GAA MOSFETs, the ultrathin silicon channel is often preferred to be undoped or lightly doped (for example with $N_a \leq 10^{16}\text{cm}^{-3}$ [13]) to avoid adverse effects associated with heavy doping, such as mobility degradation [22].

For n-channel devices, a light acceptor doping will shift the Fermi potential towards the valence band by $\phi_b = V_{th} \ln \left(\frac{N_a}{n_i}\right)$. This gives a larger potential difference between the source/drain contacts and the body, i.e. the built in voltage is increased

$$V_{bi} = \frac{E_g}{2} + \phi_b + \frac{V_{th}}{2} \ln \left(\frac{N_{ceff}}{N_{veff}}\right) \tag{2.17}$$

where E_g is the band-gap energy and N_{ceff} and N_{veff} are the effective density of states for electrons and holes, respectively. Similarly, the flat band voltage of the metal-insulator-semiconductor coupling at the gates becomes more negative with increasing n-type doping

$$V_{FB} = \frac{\Phi_m - \chi_s}{q} - \frac{E_g}{2} - \phi_b - \frac{V_{th}}{2} \ln \left(\frac{N_{ceff}}{N_{veff}}\right) \tag{2.18}$$

where Φ_m is the work function of the gate metal and χ_s is the electron affinity of the semiconductor.

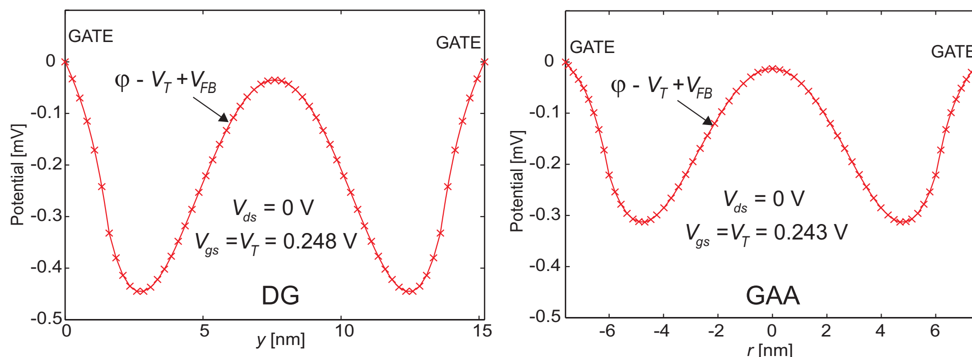

Figure 2.3: Numerically simulated (Silvaco Atlas) potential profiles along gate-to-gate symmetry line of the DG device (left) and GAA device (right) at the threshold voltage. To ease the comparison between the plots, the difference $V_T - V_{FB}$ is subtracted from the potential, φ.

2.2.7 Threshold Voltage

Historically, the most popular definition of the threshold voltage used in compact modeling is the gate voltage at which the band bending reaches $2q\phi_b$ at the silicon-insulator interface [23]. Under this condition, the inversion carrier density at the silicon-insulator interface equals the density of the dopant atoms in the silicon bulk, N_a. This definition has been physically reasonable and successful in identifying the turn-on condition for bulk devices, however, for undoped (or lightly doped) devices the inversion carrier density required for device turn-on exceeds N_a by a good margin. Therefore this definition becomes inadequate for the nanoscale devices considered here.

The threshold voltage is not applied directly as a parameter in any of the modeling schemes described in this report, and might even not really be of a high relevance when we discuss these modeling schemes. Anyway, with the legacy of the majority of MOSFET models in mind, we apply an alternative threshold voltage definition [3][11].

From the electrostatics we observe that in the subthreshold regime the majority of the carriers will move close to the S-D symmetry line, which is the path of minimum energy. With increasing gate biasing we reach a point where the contribution of the inversion charge is sufficiently high to cause the energy minimum and the current path to shift from the device center to the silicon-insulator interface.

The threshold voltage, V_T, can therefore be defined as the biasing point

($V_{gs} = V_T$, $V_{ds} = 0$V) where this shift takes place. This occurs when the two contributions to the potential (φ_1 and φ_2) add up to the 'constant' value $V_T - V_{FB}$ along the gate-to-gate (G-G) symmetry line. Numerical simulations carried out on the Atlas simulator from Silvaco, give threshold voltages of $V_T = 0.248$V and 0.243V for the present DG and GAA devices, respectively, ref. figure 2.3. (These threshold points can also be extracted from the self-consistent model as described in chapter 4. From figure 4.1 and 4.14 we observe that the modeled threshold points are $V_T \approx 0.25$ and ≈ 0.24 for the DG and GAA MOSFET, respectively).

Note that the potential along the G-G symmetry line at the threshold point is not perfectly flat, as φ_1 and φ_2 are differently distributed. Numerical simulations indicate minor fluctuations of less than 0.5mV, as illustrated in figure 2.3.

2.3 Long-Channel Modeling

In this section we review methods based on the solution of the 1D and 2D Poisson's equation for the DG and GAA MOSFETs, respectively. For long channel devices where short channel effects are negligible, these models are excellent tools for modeling current and capacitance.

2.3.1 Drain Current Model of Undoped DG

Long-channel drain current models have been developed for DG MOSFETs as presented by Taur et al. in [24] and [25] and by Ortiz-Conde et al. in [26]. The models are based on solving the 1D Poisson's equation in the transverse direction. Ortiz-Conde et al. solved Poisson's equation with respect to the surface and center of the silicon body potential, while Taur et al. introduced a new auxiliary variable β in their solution. In [12] it is proven that these two methods are equivalent, and in the following we have chosen to concentrate on the Taur method. The 1D Poisson's equation in the transversal direction is given by

$$\frac{\partial^2 \varphi(y)}{\partial y^2} = \frac{q n_i}{\varepsilon_{si}} \exp\left(\frac{\varphi(y) - V_F}{V_{th}}\right) \tag{2.19}$$

The quasi fermi potential V_F is assumed to be independent of y. Integrating (2.19) once, we obtain [24]

$$\frac{\partial \varphi}{\partial y} = \sqrt{\frac{2 q n_i V_{th}}{\varepsilon_{si}}} \sqrt{\exp\left(\frac{\varphi - V_F}{V_{th}}\right) + C_1} \tag{2.20}$$

where C_1 is the integration constant, which is determined by assuming symmetric gate properties, i.e. $\left.\frac{\partial\varphi}{\partial y}\right|_{y=t'_{ox}+t_{si}/2} = 0$. From this we obtain $C_1 = -\exp\left(\frac{\varphi(t'_{ox}+t_{si}/2)-V_F}{V_{th}}\right)$. Then by integrating (2.20) we get

$$\varphi(y) = V_F - 2V_{th}\ln\left[\frac{t_{si}}{2\beta}\sqrt{\frac{qn_i}{2\varepsilon_{si}V_{th}}}\cos\left(\frac{2\beta\left(t'_{ox}+t_{si}/2-y\right)}{t_{si}}\right)\right] \tag{2.21}$$

This is an implicit equation where β is determined by requiring continuity in the displacement field at the silicon-insulator interface

$$\varepsilon_{ox}\frac{V_{gs}-V_{FB}-\varphi(t'_{ox})}{t_{ox}} = Q = \varepsilon_{si}\left.\frac{\partial\varphi}{\partial y}\right|_{y=t'_{ox}} \tag{2.22}$$

where Q is the total mobile charge per unit gate area.

The parameter β can be solved explicitly by a very accurate procedure described by Yu et al. in [27].

The drain current can be calculated in accordance with Pao-Sah [28], who included both the drift and diffusion carrier transport components in the silicon body. Under the assumption of constant mobility and no velocity saturation in the channel the current can be expressed as

$$I_{ds} = \mu_n\frac{W}{L}\int_0^{V_{ds}} Q(V_F)dV_F \tag{2.23}$$

where $Q(V_F)$ is the total mobile charge per unit gate area. From equation (2.22) we can find Q expressed as a function of the auxiliary variable β [29]

$$Q = 2\varepsilon_{si}\left.\frac{\partial\varphi}{\partial y}\right|_{y=t'_{ox}} = \frac{8\varepsilon_{si}V_{th}}{t_{si}}\beta\tan\beta \tag{2.24}$$

If we substitute V_F by β as independent variable, equation (2.23) can be calculated analytically as

$$\begin{aligned} I_{ds} &= \mu_n\frac{W}{L}\int_{\beta_s}^{\beta_d} Q(\beta)\frac{dV_F}{d\beta}d\beta \\ &= \mu_n\frac{16W\varepsilon_{si}V_{th}^2}{Lt_{si}}\left.\left[\beta\tan\beta-\frac{\beta^2}{2}+\frac{t'_{ox}}{t_{si}}\beta^2\tan^2\beta\right]\right|_{\beta_d}^{\beta_s} \end{aligned} \tag{2.25}$$

The integration limits β_s and β_d are calculated for $V_F = 0$ and $V_F = V_{ds}$, respectively, using the explicit procedure in [27].

When short channel effects are not significant these models can continuously cover all operating regions without the need for nonphysical fitting parameters, as validated by numerical simulations in [25] and [26]. Even for short channel devices these models may yield satisfactory results in the strong inversion regime. However, in subthreshold and moderate inversion operating regimes, short channel effects become more important, and a 2D analysis is required for a physically based analysis without fitting parameters.

Charge Based Current Models

As an alternative to the long channel methods of Taur et al. [25] and Ortiz-Conde et al. [26] as discussed above, so-called charge-based methods have also been presented. In undoped DG nanoscale devices the depletion charge is normally negligible, and the inversion charge is equal to the total charge in the channel. The total inversion charge, Q, at a given x can then be written as

$$Q \equiv 2q\int_{t'_{ox}}^{t'_{ox}+t_{si}/2}(n-n_i)dy = -2C_{ox}(V_{GS}-V_{FB}-\Psi_s) \tag{2.26}$$

where Ψ_s is the potential of the silicon-insulator interface and $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$. This charge term is inserted in the Pao-Sah integral (2.23), and the following approximate expression for the drain current is obtained by [30]

$$I_{ds} = \frac{\mu_n W}{L}\left[2V_{th}(Q_d-Q_s)-\frac{Q_d^2-Q_s^2}{4C_{ox}}\right] \tag{2.27}$$

where Q_d and Q_s are the total inversion charge evaluated at the drain and source ends, respectively. The method is developed based on the approximation that $qt_{si}n_ie^{(\phi_c-V_F)} \ll V_{th}\varepsilon_{si}/t_{si}$, where ϕ_c is the center potential at $x=0$ and $y=t_{si}+t'_{ox}/2$. They also used an empirical smoothing function.

An improved charge model was developed by Sallese et al. [31], who presented the following expression for the drain-current

$$I_{ds} = \frac{\mu_n W}{L}\Bigg[2V_{th}\left(Q_d-Q_s\right)-\frac{Q_d^2-Q_s^2}{4C_{ox}}+ 8V_{th}^2\frac{\varepsilon_{si}}{t_{si}}\ln\left(1-\frac{t_{si}\left(Q_d-Q_s\right)}{8\varepsilon_{si}V_{th}}\right)\Bigg] \tag{2.28}$$

Sallese et al. observed that the integration constant, C_1, in equation (2.20), was most important in the subthreshold regime, and proposed to apply subthreshold asymptote to estimate C_1, which gave $C_1 \approx -\frac{2Q_G}{qn_it_{si}}$. The improvement of the Sallese method in equation (2.28) compared to equation (2.27) is

the logarithmic term, which depends on t_{si} and accounts for coupling between the two gates.

Both these charge-based methods introduce approximations to the exact 1D solution of Taur and Ortiz-Conde. In strong inversion the charge-based-methods give small deviations from the Taur and Ortiz-Conde methods. In subthreshold, however, the deviation is relatively large [12].

2.3.2 Capacitance Model DG

Moldovan et al. [32] have presented an explicit analytical charge and capacitance model for long channel, undoped DG MOSFETs. The total charge in the channel can be obtained by integrating the mobile charge sheet density over the channel length

$$Q_{Tot} = -W\int_{-L/2}^{L/2} Q dx = -\frac{W^2\mu_n}{I_{ds}}\int_0^{V_{ds}} Q^2 dV_F \qquad (2.29)$$

Using the charge-based model of Sallese et al. [31] the boundary condition of the 1D Poisson's equation (2.22) can be expressed in terms of the mobile charge sheet density per unit area, Q

$$\begin{aligned} V_{gs} - V_{FB} - V_F + V_{th}\ln\left(\frac{qn_i t_{si}}{8C_{ox}V_{th}}\right) - V_{th}\ln\left(\frac{C_{ox}}{C_{si}}\right) = \\ \frac{Q}{2C_{ox}} + V_{th}\left[\ln\left(\frac{Q}{8C_{ox}V_{th}}\right) + \ln\left(\frac{C_{si}}{C_{ox}} + \frac{Q}{8C_{ox}V_{th}}\right)\right] \end{aligned} \qquad (2.30)$$

where $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$ is the silicon capacitance per unit area. From (2.30) we can find the partial derivative

$$\frac{\partial V_F}{\partial Q} = -\frac{1}{2C_{ox}} - V_{th}\left(\frac{1}{Q} + \frac{1}{Q+2Q_0}\right) \qquad (2.31)$$

where $Q_0 = 4V_{th}C_{si}$. By inserting (2.31) in (2.29) and substitute V_F by Q, we obtain

$$Q_{Tot} = -\frac{W^2\mu_n}{I_{ds}}\int_{Q_s}^{Q_d}\left(\frac{Q^2}{2C_{ox}} + V_{th}Q + V_{th}\frac{Q^2}{Q+2Q_0}\right)dQ \qquad (2.32)$$

where Q_s and Q_d can be found implicitly from (2.30) for $V_F = 0$ and $V_F = V_{ds}$ respectively. The total charge in (2.32) is equal to the mobile charge associated with the gate contacts, Q_G.

The charges associated with the source and drain electrodes are determined by the Ward-Dutton linear charge partitioning scheme, which is widely accepted for bulk MOSFETs [20], and has also been proven reasonable for long

channel DG devices as verified by numerical simulations [32]. The charge associated with the drain and source contacts, Q_D and Q_S, respectively, can then be expressed as

$$Q_D = -W \int_{-L/2}^{L/2} \frac{x + L/2}{L} Q dx \tag{2.33}$$

$$Q_S = Q_{Tot} - Q_D \tag{2.34}$$

Equation (2.33) is solved analytically following the same steps as for Q_{Tot} in equation (2.29)-(2.32). The intrinsic capacitances are then found by equation (2.15). For the special case of zero drain bias C_{GG} is given by [32]

$$C_{GG} = -\frac{WL}{\frac{1}{2C_{ox}} + V_{th}\left(\frac{1}{Q_s} + \frac{1}{Q_s + 2Q_0}\right)} \tag{2.35}$$

When $V_{ds} = 0$, the remaining capacitances of the long-channel device can be found directly from C_{GG}, due to symmetry [33]

$$\begin{aligned} C_{GG} &= -2C_{GD} = -2C_{DG} = -2C_{GS} = -2C_{SG} \\ &= 6C_{SD} = 6C_{DS} = 3C_{DD} = 3C_{SS} \end{aligned} \tag{2.36}$$

2.3.3 Drain Current Model GAA

Long-channel drain current models are also available for GAA MOSFETs [34]. As for the DG models described in section 2.3.1, the GAA model is based on solving Poisson's equation in the radial direction accounting for the cylindrical symmetry. Poisson's equation is then given by

$$\frac{\partial^2 \varphi(r)}{\partial r^2} + \frac{1}{r}\frac{\partial \varphi(r)}{\partial r} = \frac{q n_i}{\varepsilon_{si}} \exp\left(\frac{\varphi(r) - V_F}{V_{th}}\right) \tag{2.37}$$

where it is assumed that V_F is constant in the radial direction. Equation (2.37) can be solved analytically giving

$$\varphi(r) = V_F + V_{th} \ln\left[\frac{-8\varepsilon_{si} V_{th} r_{si}^2 (\beta - 1)}{q n_i \left(r_{si}^2 + (\beta - 1) r^2\right)^2}\right] \tag{2.38}$$

The parameter, β, is found by invoking continuity in the displacement field at the silicon-insulator interface

$$\varepsilon_{ox} \frac{V_{gs} - V_{FB} - \varphi(r_{si})}{r_{si} \ln\left(1 + \frac{t_{ox}}{r_{si}}\right)} = Q = \varepsilon_{si} \left.\frac{\partial \varphi}{\partial r}\right|_{r = r_{si}} \tag{2.39}$$

where Q is the total mobile charge per unit gate area.

In [35] Iñiguez et al. presented an explicit continuous drain current model. This model uses a unifying expression which matches the asymptotic behavior of the device in strong inversion and subthreshold. Alternatively, Yu et al. [27] have presented a procedure for explicitly calculating β of the GAA device with high accuracy. This method uses the exact solution of Poisson's equation in all regions of operation and can therefore be considered more mathematically correct.

The drift diffusion current is found from the Pao-Sah integral which in the cylindrical case yields

$$I_{ds} = \mu_n \frac{2\pi r_{si}}{L} \int_0^{V_{ds}} Q(V_F) dV_F \tag{2.40}$$

From equation (2.39) we can find Q expressed as a function of β

$$Q = \varepsilon_{si} \left. \frac{\partial \varphi}{\partial r} \right|_{r=r_{si}} = Q_0 \left(\frac{1}{\beta} - 1 \right) \tag{2.41}$$

where $Q_0 = \frac{4\varepsilon_{si} V_{th}}{r_{si}}$. By substituting V_F by β in (2.40) we obtain

$$I_{ds} = \mu_n \frac{16\pi\varepsilon_{si} V_{th}^2}{L} \left[\frac{\eta}{4\beta^2} + \frac{1 - \frac{\eta}{2}}{\beta} + \frac{1}{2} \ln \beta \right] \Bigg|_{\beta_d}^{\beta_s} \tag{2.42}$$

where $\eta = \frac{4\varepsilon_{si} \ln\left(1 + \frac{t_{ox}}{r_{si}}\right)}{\varepsilon_{ox}}$, and β_s and β_d are calculated for $V_F = 0$ and $V_F = V_{ds}$, respectively, using the explicit procedure for the GAA in [27].

For long channel devices this model can continuously cover all operating regions without the need for nonphysical fitting parameters, as validated by numerical simulations in [34] and [35].

2.3.4 Capacitance Model GAA

Long channel capacitance models for the GAA have been presented by Moldovan et al. [36] and Yu et al. [33]. The total inversion charge is obtained by integrating the mobile charge sheet density over the channel length

$$Q_{Tot} = -2\pi r_{si} \int_0^L Q dx = -4\pi^2 r_{si}^2 \frac{\mu_n}{I_{ds}} \int_0^{V_{ds}} Q^2 dV_F \tag{2.43}$$

where I_{ds} is given in (2.42). From equation (2.41), β can be expressed in terms of the total mobile charge per unit gate area, i.e. $\beta = \frac{Q_0}{Q+Q_0}$.

From (2.39), we then find

$$\frac{\partial V_F}{\partial Q} = \frac{r_{si} \ln\left(1 + \frac{t_{ox}}{r_{si}}\right)}{\varepsilon_{ox}} + V_{th}\left(\frac{1}{Q} + \frac{1}{Q + Q_0}\right) \tag{2.44}$$

By inserting (2.44) in (2.43) and substitute V_F by Q we obtain an analytical solution for Q_{Tot}, which is equal to the absolute value of the mobile charge associated with the gate contact, $Q_G = -Q_{Tot}$. The charges associated with the source and drain electrodes are determined by a linear charge partitioning scheme, as described in section 2.3.2, giving analytical results for Q_S and Q_D. The intrinsic capacitances are then found by straight forward differentiations given by (2.15).

Note that in the case of the GAA we can express β as an explicit function of Q, as given in (2.41), while in the case of the DG, β cannot be explicitly expressed with Q, as seen from (2.24). Therefore the long channel capacitance model of the GAA can be based on the exact solution of Poisson's equation, (2.37), while the DG method is based on the approximated method of Sallese et al. [31], ref. equation (2.28).

2.4 Short-Channel 2D Modeling

In this section a threshold voltage model of the DG MOSFET based on the solution of the 2D Poisson's equation proposed by Chen et al. [37], will be reviewed. The length/height ratio of the MOSFET devices has steadily decreased in order to keep up with the down scaling rate of Moore's law. This results in an increased electrostatic coupling between the source and drain electrodes. This unwanted coupling give rise to so called short-channel-effects (SCEs), such as for example drain induced barrier lowering (DIBL) [15]. A 2D modeling approach is required to cover the SCEs.

When considering undoped and lightly doped devices only the mobile charge term is included on the right hand side of Poisson's equation, ref. section 2.2.1. The mobile charge in an undoped device is given by $n = n_i \exp\left(\frac{\varphi - V_F}{V_{th}}\right)$, ref. equation (2.8).

In this context the threshold voltage is defined as the gate voltage at which the minimum charge sheet density of inversion carriers, n_s, reaches a value adequate for identifying the turn-on condition, n_{sT}.

The quasi-Fermi potential, V_F, is approximated as a step function which is zero from source through the device, and makes a step equal to V_{ds} at the

drain-contact. This step-function approximation makes the model independent of V_{ds}, and the final result is incapable of directly model the DIBL. Based on the superposition principle the potential is split into a sum of two terms, $\varphi = \varphi_a + \varphi_b$. The first term, φ_a, is given by the 1D Poisson's equation in the x-direction

$$\frac{d^2\varphi_a}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \exp\left(\frac{\varphi_a}{V_{th}}\right) \tag{2.45}$$

where $\varphi_a\left(\pm\frac{L}{2}\right) = V_{bi}$. The second term, φ_b is given by the 2D equation

$$\frac{d^2\varphi_b}{dx^2} + \frac{d^2\varphi_b}{dy^2} = \frac{qn_i}{\varepsilon_{si}} \exp\left(\frac{\varphi_a}{V_{th}}\right) \left[\exp\left(\frac{\varphi_b}{V_{th}}\right) - 1\right] \tag{2.46}$$

where $\varphi_b\left(\pm\frac{L}{2}\right) = 0$, and the E-field is to be continuous when adjusted for the difference in permittivity across the silicon-insulator interface. The 2D equation is solved by a truncated Taylor expansion and with variable separation. The threshold voltage is then found to be

$$V_T = V_{FB} + \eta V_{th} \frac{\cosh(\theta)}{\cosh(\theta/2)} \ln\left(\frac{n_{sT}}{n_i t_{si}}\right) - \phi_{am}\left[\frac{\cosh(\theta)}{\cosh(\theta/2)}\eta - 1\right] \tag{2.47}$$

where ϕ_{am} is φ_a at the center, $x = 0$, θ and η are geometrical constants related to the 1D solution and the Debye length. The value of n_{sT} can be found from a long channel approximation, from numerical simulations or from measurements.

Based on this model one can analyze the sensitivity of the threshold voltage to the geometrical properties L, t_{si} and t_{ox}.

2.5 Conformal Mapping

Conformal mapping was introduced as a technique to calculate the two-dimensional effects of short-channel devices. The first example of the application of this technique was shown by Klös et al. in [38]. They used conformal mapping to map the fields of a semi-infinite slab of silicon into a complex plane with analytical solutions. The boundary conditions of this 2D solution included the field from the depletion charge and most short-channel effects became intrinsic to the model.

This bulk MOSFET model was later refined by Østhaug et al. [39], who simplified the integrals associated with the conformal mapping procedure. The model was also verified against experimental results from sub-100nm single gate devices with good agreement.

Based on the above work Kolberg et al. applied the conformal mapping procedure to the DG MOSFET [11][40][41][42][43], and found an analytical solution to the inter-electrode electrostatics of the device.

We have further improved the conformal mapping modeling of the DG MOSFET by including a corner correction to facilitate precise capacitance modeling. The conformal mapping technique has also been applied in a quasi-3D analysis of the GAA MOSFET [3][4][44][45][46][47][48][49][50][51][52][53][54].

Chapter 3

Inter-Electrode Electrostatics

3.1 Introduction

The inter-electrode electrostatics of the DG device can be described analytically based on the 2D Laplace equation. This solution, which is dominant in the subthreshold regime, is derived by performing a conformal mapping of the device cross-section from the normal (x, y)-plane to the upper half-plane of the complex (u, iv)-plane (section 3.2).

This technique is not directly applicable to the 3D structure of the GAA MOSFET. However, by performing a simple geometric scaling transformation, accounting for the difference in gate control in the two devices, the 2D DG solution can also be applied for the GAA MOSFET with a high degree of precision (section 3.3).

The inter-electrode contribution to the electrostatics is dominating in the subthreshold regime, and the modeled subthreshold drain current is derived and compared with numerical simulations in section 3.4. A compact, analytical subthreshold drain current model of the GAA MOSFET is presented in section 3.5.

3.2 Double-Gate MOSFET

3.2.1 Schwarz-Christoffel Transform

The conformal mapping between the rectangular DG device cross-section in the normal (x, y)-plane and the upper half-plane of the complex (u, iv)-plane,

is defined by the following Schwarz-Christoffel transform [41][42][55]

$$\frac{\partial z}{\partial w} = \frac{1}{\sqrt{1-w^2}\sqrt{1-k^2w^2}} \Rightarrow z = x + iy = \frac{L}{2}\frac{F(k,w)}{K(k)} \tag{3.1}$$

where $F(k, w)$ is the complex elliptic integral of the first kind, $K(k) = F(k, 1)$ is the corresponding complete elliptic integral, and $w = u + iv$. The modulus k is a constant between 0 and 1 determined implicitly by the geometric ratio

$$\frac{K(k)}{K\left(\sqrt{1-k^2}\right)} = \frac{L/2}{2t'_{ox} + t_{si}} \tag{3.2}$$

Figure 3.1 illustrates the mapping between the (x, y)-plane (left) and the (u, iv)-plane (right). The rectangular grid in the left plot maps into the curve shapes to the right. The angle-preserving characteristics of the conformal mapping is observed, as all the perpendicular crossings between the horizontal and vertical lines to the left are also perpendicular crossings to the right.

The boundary, i.e. the circumference of the rectangular DG body, maps onto the real u-axis, and the four corners map into the positions $u = \pm 1$ and $u = \pm\frac{1}{k}$. The boundary also includes the four insulator gaps which are drawn in green in the (x, y)-plane, and can also be discerned on the u-axis in the right figure. Moreover, the G1-G2 symmetry line and the S-D symmetry line map onto the imaginary iv-axis and the half-circle of radius $\frac{1}{\sqrt{k}}$ about the origin, respectively. The mapping of the silicon-insulator interfaces is also indicated [11][42].

3.2.2 Inverse Transform

It is often desirable to define a regular grid in the normal (x, y) plane, and then find the corresponding grid points in the transformed (u, iv)-plane. This is obtained by the inverse transform of (3.1). First we rewrite the complex elliptic integral

$$F(k,w) = F(k,\phi) = \int_0^{sin\phi} \frac{dt}{\sqrt{1-k^2\sin^2 t}} \tag{3.3}$$

where $\phi = \sin^{-1} w = \mathrm{am}(k, z)$ is the Jacobi amplitude [56], giving $\phi = F^{-1}(k, z) = \mathrm{am}(k, z)$. There are three basic Jacobi functions which arise from the inversion of the elliptic integral:

$$\mathrm{sn}(k,z) = \sin(\mathrm{am}(k,z)) = w \tag{3.4}$$

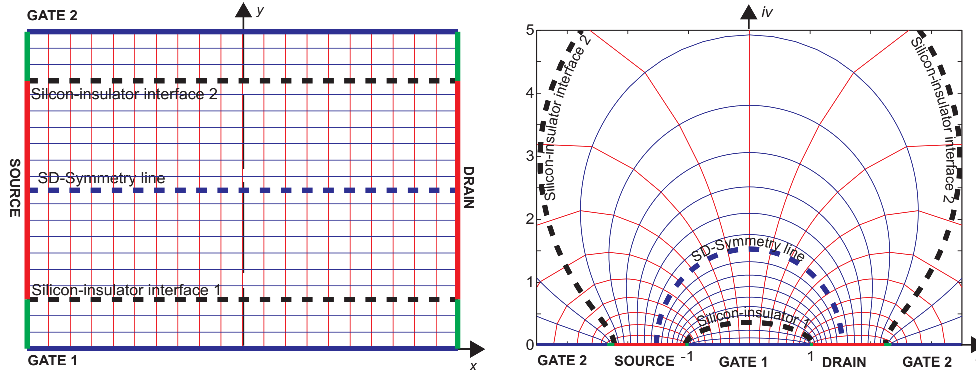

Figure 3.1: Mapping of DG-device between the (x, y)-plane (left) and the transformed (u, iv)-plane (right). The gate 1 and gate 2 electrodes are drawn with the bold blue lines, the source and drain in the bold red lines and the insulator gaps in the bold green lines. The SD-symmetry line is indicated with a bold blue dashed line and the silicon-insulator interfaces with bold black dashed lines.

$$\mathrm{cn}(k, z) = \cos(\mathrm{am}(k, z)) \tag{3.5}$$

$$\mathrm{dn}(k, z) = \sqrt{1 - k^2 \sin^2(\mathrm{am}(k, z))} \tag{3.6}$$

Routines exist for calculating the values of these Jacobi functions for real arguments ($z \in \Re$) and can be extended to also include complex arguments, $z = x + iy$, by the formula [56]

$$w = \frac{\mathrm{sn}(k, x)\mathrm{dn}(\hat{k}, y) + i \cdot \mathrm{cn}(k, x)\mathrm{dn}(k, x)\mathrm{sn}(\hat{k}, y)\mathrm{cn}(\hat{k}, y)}{\mathrm{cn}^2(\hat{k}, y) + k^2\mathrm{sn}^2(k, x)\mathrm{sn}^2(\hat{k}, y)} \tag{3.7}$$

where $\hat{k} = \sqrt{1 - k^2}$.

3.2.3 Solution of 2D Laplace Equation

The inter-electrode Laplace component of the potential distribution throughout the extended body can be expressed in the (u, iv)-plane as [55]

$$\varphi_2(u, v) = \frac{v}{\pi} \int_{-\infty}^{\infty} \frac{\varphi(u')du'}{(u - u')^2 + v^2} \tag{3.8}$$

where $\varphi(u')$ is the electrostatic potential along the entire boundary, i.e. along the real u-axis. The major contributions to this integral come from the four equipotential contacts and minor terms come from the insulator gaps at the

four corners. In the limit of zero insulator thickness, equation (3.8) results in the following analytical expression for the potential distribution [42]

$$\varphi_2(u,v) = \frac{1}{\pi}\begin{bmatrix} V_{G1}\left[\tan^{-1}\left(\frac{1-u}{v}\right) + \tan^{-1}\left(\frac{1+u}{v}\right)\right] + \\ V_{G2}\left[\pi - \tan^{-1}\left(\frac{1-ku}{kv}\right) - \tan^{-1}\left(\frac{1+ku}{kv}\right)\right] + \\ V_S\left[\tan^{-1}\left(\frac{1+ku}{kv}\right) - \tan^{-1}\left(\frac{1+u}{v}\right)\right] + \\ V_D\left[\tan^{-1}\left(\frac{1-ku}{kv}\right) - \tan^{-1}\left(\frac{1-u}{v}\right)\right] \end{bmatrix} \quad (3.9)$$

where V_{G1} and V_{G2} are the differences between the gate to source voltage, V_{gs1} and V_{gs2}, and the flat band voltage, V_{FB}, ref. equation (2.18), for gate 1 and 2, respectively, V_S is equal to the built in voltage, V_{bi}, ref. equation (2.17), and $V_D = V_{ds} + V_{bi}$, where V_{ds} is the drain-source voltage.

Figure 3.2 illustrates the inter-electrode potential distribution, which is calculated in the (u, iv)-plane by equation (3.9). This solution is then mapped back to the (x, y)-plane by the inverse transform as described in section 3.2.2. We observe that the source and drain electrodes are extended through the insulator gaps, which is in accordance with the assumption of zero insulator thickness. A more accurate treatment of the boundary through the insulator gaps will be described in section 3.2.4.

The potential, $\varphi_2(x, y)$, has a saddle point close to the center of the device. In the transversal y-direction this corresponds to the minimum energy, which will be located along the S-D symmetry line for symmetric gate biasing. This means that the major part of the electron conduction between source and drain will be along the S-D symmetry line in the subthreshold region [3].

In the lateral x-direction the saddle point corresponds to the maximum energy barrier between source and drain. Precise modeling of this barrier is crucial for accurate calculation of the current. For $V_{ds} = 0$V the saddle point will be situated at the device center, $x = 0$, $y = t_{ox} + t_{si}/2$. With increasing V_{ds}, the barrier potential is steadily raised (i.e. energy barrier lowered) and shifted towards the source side of the device, $x < 0$, as illustrated in figure 3.3. This drain induced barrier lowering (DIBL) is intrinsic to equation (3.9).

With increasing gate biasing, the gate-to-gate barrier profile flattens and the barrier eventually shifts to the silicon-insulator interfaces. At this stage the induced electron density will strongly influence the device electrostatics, requiring a self consistent analysis, described in chapter 4.

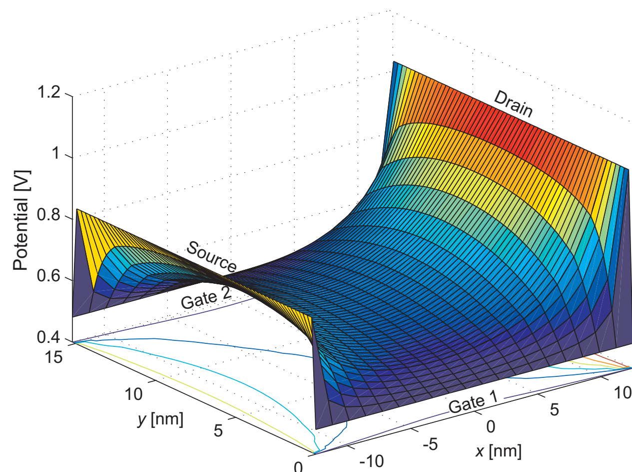

Figure 3.2: Inter-electrode potential distribution for the DG MOSFET for $V_{ds} = 0.2$V and $V_{gs} = 0$V. This corresponds to subthreshold conditions for the device considered.

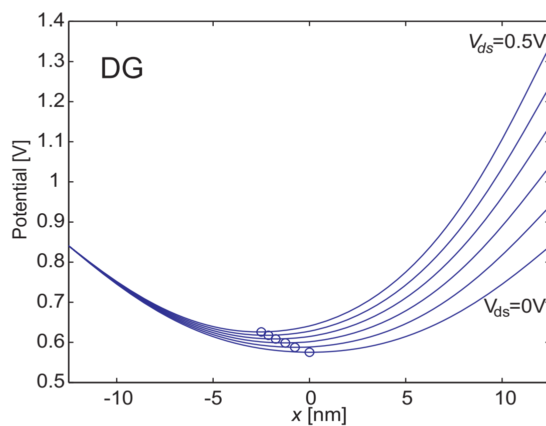

Figure 3.3: The Laplace potential of (3.9) along the S-D symmetry line for $V_{gs} = 0$V and $V_{ds} = 0, 0.1, 0.2, 0.3, 0.4, 0.5$V. The potential minima are indicated with symbols.

3.2.4 Corner Correction

The zero order corner approximation of equation (3.9) can be improved by including a more accurate treatment of the boundary potential across the four insulator gaps. Since the corners are located relatively far away from each other, we assume that the potential across the insulator gap can be modeled by using the conformal mapping technique for one separate corner with infinite gate length and drain/source heigth/depth defined by the following Schwarz-Christoffel transform [45][49][50][55]

$$\frac{\partial z_{1c}}{\partial w_{1c}} = \frac{\sqrt{w_{1c} - 1}}{w_{1c}} \tag{3.10}$$

where the subscript $1c$ indicates that this is a one-corner transform, $z_{1c} = ix_{1c} + y_{1c}$ and $w_{1c} = u_{1c} + iv_{1c}$. With the appropriate boundary conditions we obtain

$$z_{1c} = \frac{2t'_{ox}}{\pi}\left[\sqrt{w_{1c} - 1} - \tan^{-1}\left(\sqrt{w_{1c} - 1}\right)\right] + t'_{ox} \tag{3.11}$$

Figure 3.4 illustrates the (x_{1c}, y_{1c})-plane of the one-corner layout, with the infinite gate and source/drain boundary indicated with bold black lines. The denominator in (3.10) represent the 180° angle at $z_{1c} = -\infty$ while the square root term in the numerator corresponds to the 90° angle of the source/drain contact at $z_{1c} = t'_{ox}$. We assume an infinite overlap between the gate and the source/drain contact in this modeling scheme.

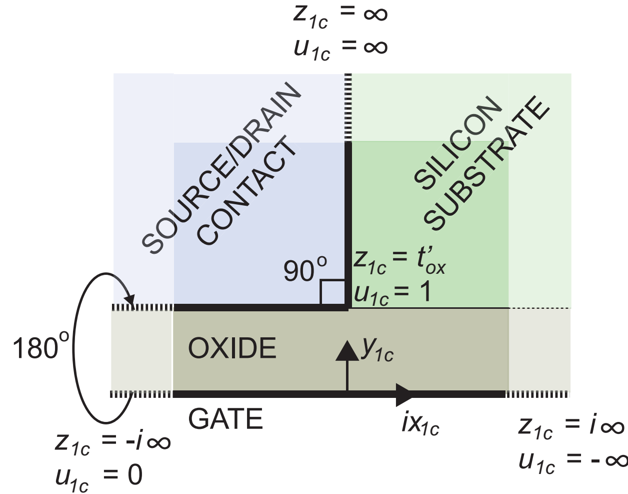

Figure 3.4: One corner analysis in the z_{1c}-plane with corresponding u_{1c}-values along the boundary.

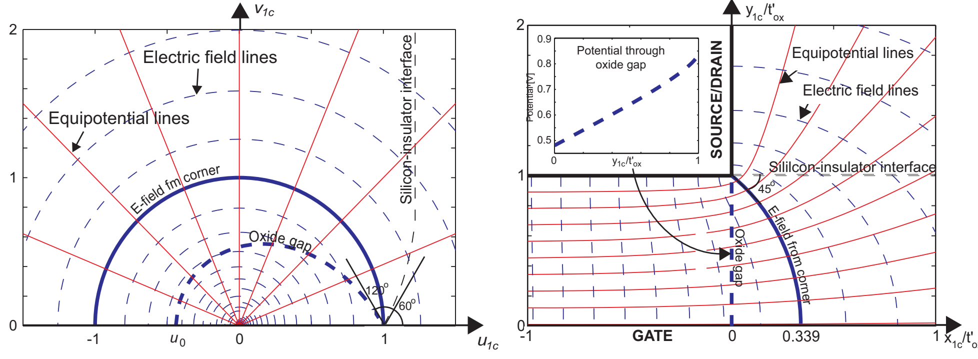

Figure 3.5: Equipotential lines and electric field lines in the transformed (u_{1c}, iv_{1c})-plane of one-corner analysis (left) and in the (x_{1c}, y_{1c})-plane (right). The inset (right) shows the potential profile through the oxide gap.

Applying the Laplace integral of equation (3.8), the potential distribution in the (u_{1c}, iv_{1c})-plane becomes

$$\varphi_{21_c}(u_{1c}, v_{1c}) = \frac{1}{2}\left(V_G + V_{S/D}\right) - \frac{1}{\pi}\left(V_G - V_{S/D}\right)\tan^{-1}\left(\frac{u_{1c}}{v_{1c}}\right) \tag{3.12}$$

This potential distribution is radially equipotential from the origin of the (u_{1c}, iv_{1c})-plane, as shown to the left in figure 3.5. The right plot shows the equipotential and electric field lines in the (x_{1c}, y_{1c})-plane.

Note that we also apply the effective insulator thickness, t'_{ox}, ref. section 2.1, in this analysis. As discussed, this will introduce an error if the x-component of the electric field in the insulator is significant. As can be observed in figure 3.5 the E-field emanating from the source/drain corner has an angle of 45° with the silicon-insulator interface, i.e. the x- and y-components of the E-field are equal at this point. Everywhere else inside the insulator the y-component is larger than the x-component. As this error only affects the correction of the boundary across the insulator gaps, we consider it a second order effect. In section 3.2.6 the error introduced by the insulator scaling is analyzed.

In annex A the insulator gap potential is investigated further by doing a series expansion about $z_{1c} = 0$ and $z_{1c} = t'_{ox}$. This gives further insight, and is also applied as boundary conditions for the insulator gap modeling function described next, and for the silicon-insulator potential profile in the above threshold regime, as described in chapter 4.

There is no explicit, analytical inverse transform of equation (3.11). There-

fore it is not possible to directly apply the exact one-corner potential profile of the insulator gap, as boundary condition in the four-corner DG MOSFET. In the following we will use a sixth order modeling function to model the insulator gap potential profile. This modeling function extracts its parameters from the one-corner analysis.

Modeling of Insulator Gap Potential

The sixth order function to model insulator-gap boundary for the four-corner DG MOSFET is given by

$$\varphi_{ox}(y) = Ay^6 + By + C \tag{3.13}$$

where the parameters A, B and C are determined from the gate potential, $\varphi_{ox}(0) = V_G$, the source/drain potential $\varphi_{ox}(t'_{ox}) = V_{S/D}$ and by the derivative at $y = 0$,

$$\left.\frac{\partial \varphi_{ox}}{\partial y_{1c}}\right|_{y_{1c}=0} = \frac{V_{S/D} - V_G}{t'_{ox}\sqrt{1+|u_0|}} \tag{3.14}$$

where u_0 is indicated in figure 3.5. This derivative is found from the series expansion about $z_{1c} = 0$ in annex A, ref. equation (A.5)

The 6th order approximation of (3.13) is compared to the potential profile obtained by the 'exact' one-corner analysis in figure 3.6. We observe a small deviation in the high curvature area close to the source/drain contact, but overall there is a very good agreement between the two curves.

The insulator gap potential, φ_{ox}, must then be transformed to the four-corner (u, iv)-plane so that it can be applied as the boundary potential, $\varphi(u)$, of the Laplace equation in (3.8).

This can be accomplished by performing a series expansion of the elliptic integral around $u = u_1$, where $u_1 = \left\{-\frac{1}{k}, -1, +1, \frac{1}{k}\right\}$ for the four corners, respectively. The transformed potential profile must be calculated separately for the different values of u_1. As the procedure is similar for all four corners, we have limited this text to only include the calculation of the gate 1 - drain (G1-D) insulator gap, $u_1 = 1$, as an example.

The approximate transform from the (x, y) to the (u, iv)-coordinates for the G1-D corner is given by

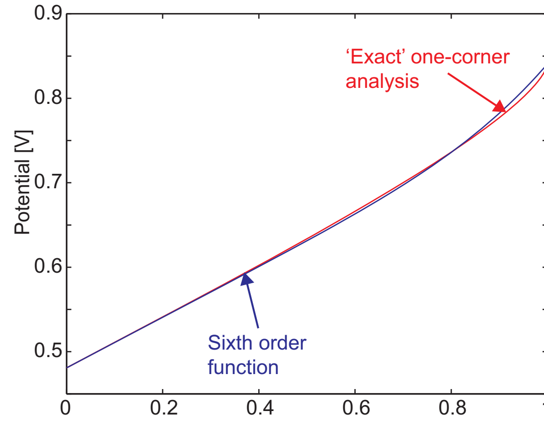

Figure 3.6: The potential profile across insulator-gap of one-corner analysis (red) compared with 6th order function.

$$y(u) = i\frac{L}{2}\left[\frac{F(k,u)}{K(k)} - 1\right] \approx \frac{L}{\sqrt{2(1-k^2)}K(k)} \times \left[(u-1)^{\frac{1}{2}} + \frac{(5k^2-1)(u-1)^{\frac{3}{2}}}{12(1-k^2)} + \Gamma \cdot (u-1)^{\frac{5}{2}}\right] \tag{3.15}$$

This corresponds to the two first terms of the series expansion of the elliptic integral around $u_1 = 1$. The third term, with the Γ-parameter, ensures that the transform has the correct value at the contact corner, $y(u) = t'_{ox}$. In this case Γ is given by

$$\Gamma = -\frac{1}{u_{ox1}^2} + \frac{1-5k^2}{12u_{ox1}(1-k^2)} + \frac{\sqrt{2-2k^2}t'_{ox}K(k)}{u_{ox1}^{\frac{5}{2}}L} \tag{3.16}$$

where u_{ox1} is the transformed value of t'_{ox}, associated with gate 1. The series expansion is compared to the exact elliptic integral across the G1-D gap in figure 3.7, and an excellent agreement is observed.

When $y(u)$ of equation (3.15), is inserted into (3.13), and we ignore all terms of $(u-1)^m$ with order greater than 3, we obtain

$$\varphi_{ox}(u) = A\frac{8(u-1)^3}{(K(k))^6(1-k^2)^3} + By(u) + C \tag{3.17}$$

The above is valid for the G1-D insulator gap, and similar procedures must be carried out for the three other insulator gaps. The calculation of the Laplace integral, with (3.17) as boundary potential, is outlined in annex B. Figure 3.8 shows a surface plot of the potential profile which includes this corner correction in all four corner regions. As compared to the simplified model of figure 3.2, we clearly observe the effect of the corner correction in figure 3.8.

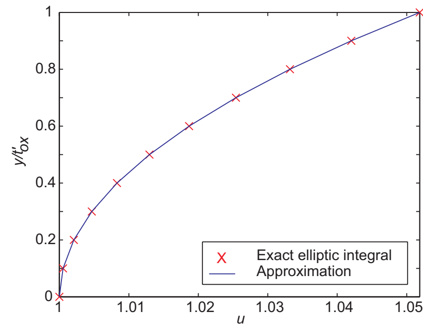

Figure 3.7: Comparison of exact (3.1) and approximate (3.15) 4-corner transform across the G1-D insulator gap.

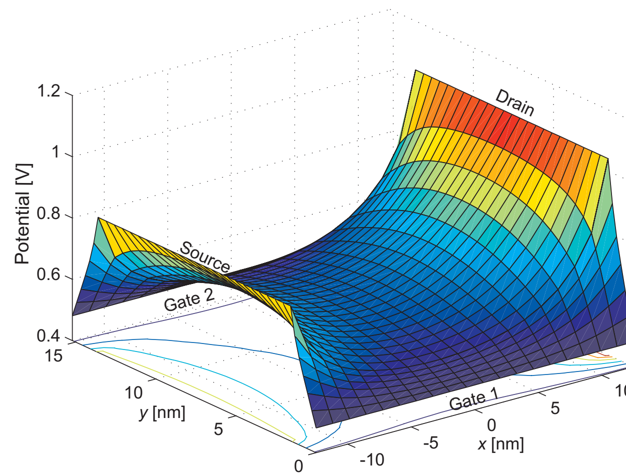

Figure 3.8: Inter-electrode potential distribution for the DG MOSFET including corner correction, $V_{ds} = 0.2$V and $V_{gs} = 0$V.

3.2.5 Asymmetric Gate

The main scope is to analyze the symmetrically biased DG and GAA devices. However, asymmetric gate biasing is intrinsic to the Laplace solution discussed above, and three examples are given in figures 3.9- 3.11 to illustrate the inter-electrode potential distribution for asymmetric gate biasing, asymmetric insulator thickness and asymmetric insulator material properties.

In all the examples we use a near mid-gap work function for gate 1 and 2, i.e. $\Phi_{mG1} = \Phi_{mG2} = 4.53$eV, and for simplicity zero drain bias is applied in these examples, i.e. $V_{ds} = 0$.

For asymmetric gate bias or gate structures the saddle point is shifted from the center of the device $y = t_{ox} + t_{si}/2$ towards one of the gates depending on the asymmetry. This means that the current path between S-D will also be shifted. In these three examples, figure 3.9- 3.11, we observe that the gate-to gate barrier is shifted towards the gate 1 contact.

3.2.6 DG Model Verification

The deviation between the DG model (figure 3.8) and numerical simulations (Silvaco Atlas) is plotted in figure 3.12 for different gate biasing. Here, the silicon substrate is replaced by an insulator with relative permittivity equal to that of silicon, ε_{si}, in the DG structure of the numerical simulator. Therefore no charges are included neither in the simulations nor in the model. In the left and right plot, for $V_{gs} = 0$V and 0.7V respectively, we observe error peaks of approximately 7-9mV close to the device corners. In the center plot of $V_{gs} = 0.35$V the error is practically zero throughout the device.

The inter-electrode potential distribution is depending on the potential difference between the gate, source and drain electrodes. At $V_{gsFlat} = V_{FB} + V_{bi}$($\approx$0.36V in this case) and $V_{ds} = 0$, there is no potential difference between the gate, source and drain contacts, and the potential distribution from the Laplace solution will be flat. Therefore, the error is very small in the middle plot of $V_{gs} = 0.35$V.

The error peaks observed in the left and right plot, for $V_{gs} = 0$V and 0.7V, respectively, can mainly be attributed to the equivalent insulator thickness scaling which assumes that there is no lateral electric field in the insulator, as described in section 2.1. Close to the corners of the device, however, the x-component of the E-field is significant. Additionally we could expect a small error caused by inaccuracies in the approximated boundary potential across the oxide gaps, as described in section 3.2.4.

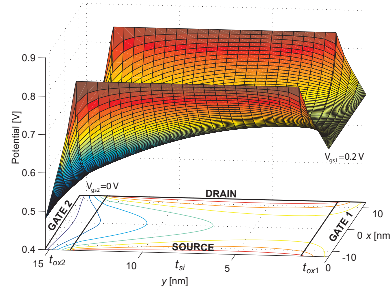

Figure 3.9: Asymmetrically biased DG device with $V_{gs1} = 0.2$V and $V_{gs2} = 0$V. $V_{ds} = 0$V, $t_{ox1} = t_{ox2} = 1.6nm$ and $\varepsilon_{ox1} = \varepsilon_{ox2} = 7$.

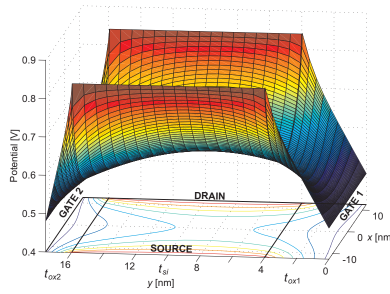

Figure 3.10: Asymmetric DG structure with $t_{ox1} = 4.0$nm and $t_{ox2} = 1.6$nm. $V_{gs1} = V_{gs2} = 0$V, $V_{ds} = 0$V and $\varepsilon_{ox1} = \varepsilon_{ox2} = 7$.

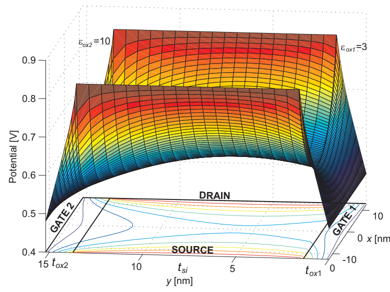

Figure 3.11: Asymmetric DG structure with $\varepsilon_{ox1} = 3$ and $\varepsilon_{ox2} = 10$. $V_{gs1} = V_{gs2} = 0$V, $V_{ds} = 0$V and $t_{ox1} = t_{ox2} = 1.6$nm

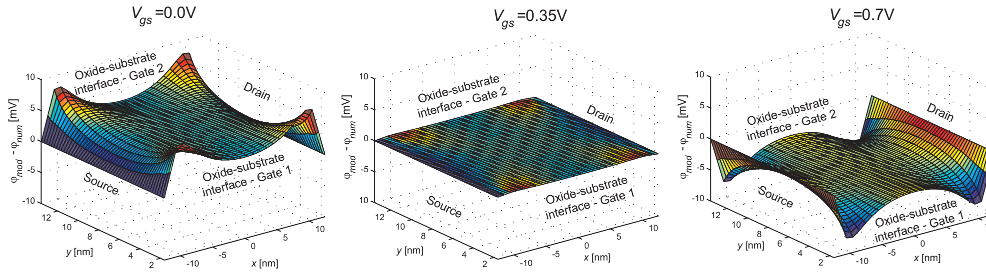

Figure 3.12: Deviation between modeled inter-electrode potential distribution and numerical simulations (Silvaco Atlas) of Laplace contribution at different gate biasing, $V_{ds} = 0$V in all plots.

At the device center there is an excellent correspondence between the simulations and the model with a maximum deviation of approximately 1-2mV. The potential close to the center is crucial for an accurate description of the S-D energy barrier, and the drift diffusion current in the subthreshold regime. Therefore, the error peaks in the corners of the device will not significantly influence the drain current modeling in subthreshold.

Close to threshold the error introduced by the inter-electrode potential distribution is very small, as observed in the center plot. With a further increase in the gate biasing the error peaks will return, however at this stage, the induced electron density will commence to dominate the device electrostatics, as described in chapter 4.

3.3 Gate-all-Around MOSFET

3.3.1 Adaptation of the Double-Gate Solution

Cylindrical GAA MOSFETs are 3D structures for which the conformal mapping method is not directly applicable. However, because of the cylindrical symmetry, we observe significant structural similarities between the 2D potential distribution obtained for the DG MOSFET and that of longitudinal cross sections through the cylinder axis of the GAA device. In fact, the major difference between the two is the gate control.

This difference can be expressed in terms of the characteristic lengths, which are a measure of the penetration depth of the electrostatic influence from the source and drain contacts along the S-D symmetry axis. The characteristic lengths for the DG and GAA MOSFETs are given by [57][58]

$$\lambda_{DG} = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right)t_{si}t_{ox}} \tag{3.18}$$

$$\lambda_{GAA} = r_{si}\sqrt{\frac{1}{4}+\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\ln\left(1+\frac{t_{ox}}{r_{si}}\right)} \tag{3.19}$$

respectively, where r_{si} is the radius of the GAA MOSFET silicon body.

We have proposed a technique for mapping the inter-electrode potential distribution for the DG MOSFET into that of the GAA MOSFET longitudinal cross-section [3][4][48][50]. First we calculate the potential distribution of a DG device with an extended gate length L' given by

$$L' = \frac{\lambda_{DG}}{\lambda_{GAA}}L \tag{3.20}$$

where L is the true length of the GAA MOSFET. The Schwarz-Christoffel transform of the extended device is determined from equation (3.1) by replacing the length, L, with the extended gate length L' and the modulus k by k' which is found from the geometric ratio, ref. equation (3.2).

$$\frac{K(k')}{K\left(\sqrt{1-k'^2}\right)} = \frac{L'/2}{2(r'_{ox}+r_{Si})} \tag{3.21}$$

The inter-electrode potential distribution can then be calculated by equation (3.8) to

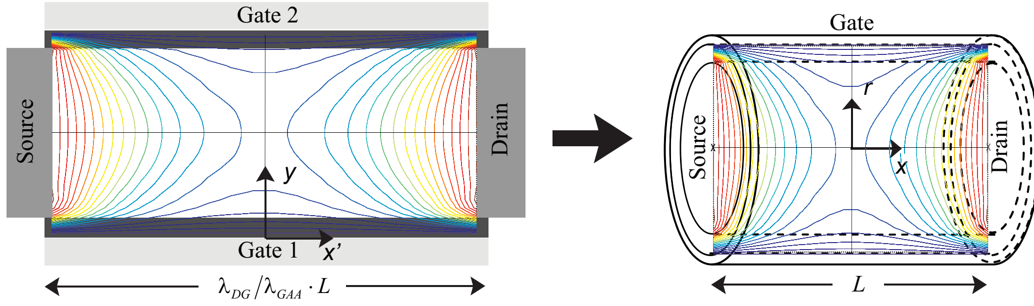

Figure 3.13: Schematic illustration of the mapping of a DG MOSFET inter-electrode potential distribution of an extended device of length $L' = \frac{\lambda_{DG}}{\lambda_{GAA}} L$ (left) into the longitudinal cross-section of a GAA device of length L (right).

$$\varphi_2'(u,v) = \frac{1}{\pi}\left[\begin{array}{l} V_G \Big[\tan^{-1}\left(\frac{1-u}{v}\right) + \tan^{-1}\left(\frac{1+u}{v}\right) + \\ \pi - \tan^{-1}\left(\frac{1-k'u}{k'v}\right) - \tan^{-1}\left(\frac{1+k'u}{k'v}\right) \Big] + \\ V_S \left[\tan^{-1}\left(\frac{1+k'u}{k'v}\right) - \tan^{-1}\left(\frac{1+u}{v}\right) \right] + \\ V_D \left[\tan^{-1}\left(\frac{1-k'u}{k'v}\right) - \tan^{-1}\left(\frac{1-u}{v}\right) \right] \end{array}\right] \quad (3.22)$$

The only difference between (3.22) and (3.9) is the value of k, and the fact that there is only one possible value of the gate potential for the GAA.

The potential distribution, $\varphi_2'(u, v)$, is then transformed to the (x', y)-coordinates of the the extended DG device. The transform is given by equation (3.1) applying the properties of the extended DG-device, i.e. L' and k'. Next, this potential distribution is mapped into the cross-section of the GAA by compressing it uniformly in the longitudinal direction using the scaling factor $\lambda_{GAA}/\lambda_{DG}$ ($= 0.69$ for the present device), as indicated in figure 3.13.

The corner correction, as described in section 3.2.4, is also applied for the GAA device. The circular shape of the source/drain and gate contact is not included in the 2D one-corner analysis. However, as the insulator thickness is relatively small compared to the silicon radius, we assume that this 3D effect does not significantly alter the insulator gap profile.

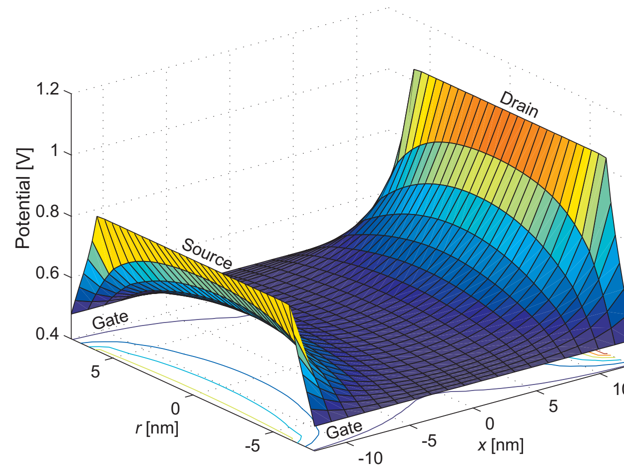

Figure 3.14: Inter-electrode potential distribution for the longitudinal cross-section through the cylinder axis of the GAA device including corner correction, $V_{ds} = 0.2$V and $V_{gs} = 0$V.

Figure 3.14 shows a surface plot of the potential profile of the GAA device which includes the corner correction. Compared to the potential profile of the DG device in figure 3.8, we observe the improved gate control of the GAA structure as the potential distribution is flatter in the central region of the device.

3.3.2 Verification of GAA-Mapping Model

Here the modeled inter-electrode electrostatics of the GAA MOSFET is compared with numerical simulations (Silvaco Atlas) in order to verify the accuracy of the mapping procedure outlined above.

Scaling properties

To check the scaling properties of the GAA MOSFET model, the potential at the device center was calculated for a range of gate lengths, keeping all other dimensions fixed. The device center is not arbitrarily chosen to evaluate the scaling properties. For $V_{ds} = 0$V the center point represents the energy barrier between the source and drain contacts in the subthreshold regime. Even when a nonzero drain-bias is applied, the barrier stays close to the

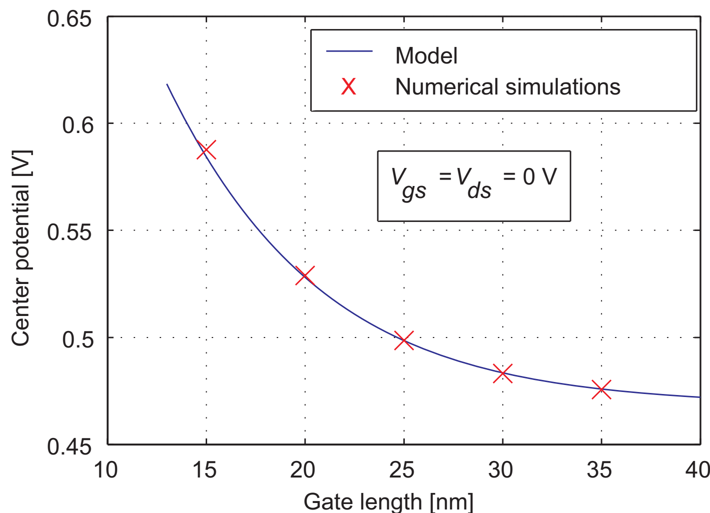

Figure 3.15: Modeled and simulated scaling of the subthreshold center potential with gate length for GAA MOSFETs, $r_{si} = 6$nm and $t_{ox} = 1.6$nm.

device center. Therefore, the device center is a crucial point in determining the drain current in subthreshold.

As shown in figure 3.15, the modeled center point potential agrees very well with numerical simulations down to a gate length of at least 15 nm, demonstrating the good scaling properties of this modeling technique.

Error along S-D symmetry line

In the following analysis the insulator thickness is set to 0.1 nm, practically zero, to avoid corner effects obscuring the analysis, ref. discussion on errors introduced by the effective oxide thickness scaling in section 2.1. Additionally, we replace the silicon substrate with an insulator in the numerical simulator. The insulator is assigned the electrostatic properties of silicon, i.e. a relative permittivity of $\varepsilon_{si} = 11.8$. Therefore, no charges are involved neither in the model nor in the simulator in this analysis.

The modeled versus the simulated GAA potential along the S-D symmetry line is plotted in figure 3.16. We observe a maximum deviation of 7mV, a distance 2.4nm from the source and drain contacts. At the center the deviation is less than 1.5mV. The DG to GAA mapping technique does not directly account for the cylindrical geometry of the source and drain contacts. This might explain why the largest deviation in the GAA electrostatics is

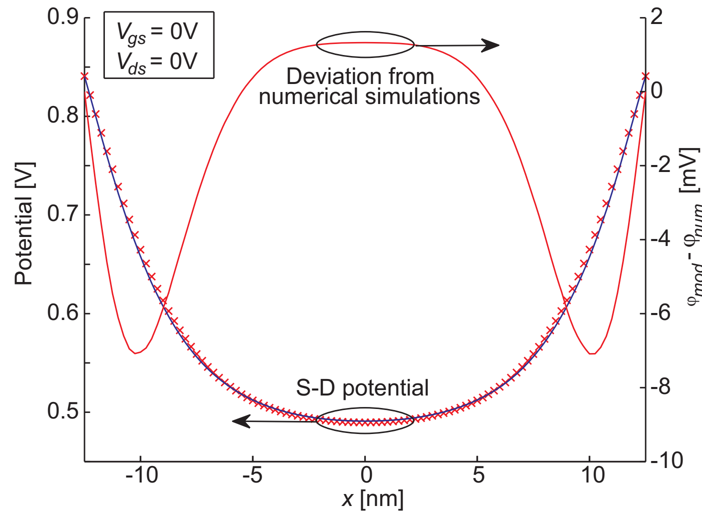

Figure 3.16: Potential profile along the S-D symmetry line of the GAA device. Blue line is modeled potential, red x's are numerical simulated results. The red line indicates the deviation between model and simulations. $V_{GS} = V_{ds} = 0$V, $t_{ox} = 0.1$nm.

located close to source and drain.

Error at different biasing levels

As discussed in subsection 3.2.6, the inter-electrode contribution depends on the potential differences between the electrodes. There is a biasing point, $V_{ds} = 0$V and $V_{gsFlat} \approx 0.36$V, where the Laplace-potential is flat throughout the device. In the left plot of figure 3.17 we see that the error is very small for $V_{gs} = 0.4$V, which is close to V_{gsFlat}.

When the difference in electrode potential increases, either down into sub-threshold, $V_{gs} < V_{gsFlat}$ or up into the strong inversion regime, $V_{gs} > V_{gsFlat}$, we observe a corresponding increase in the error. Similarly, in the right plot of figure 3.17 we observe that the error on the drain side tends to increase when the difference in potential between the drain and gate electrode increases.

Position of error peak

As observed from plot 3.16 and 3.17, the position of the peak error seems to be relatively independent of biasing level and the extremum is situated

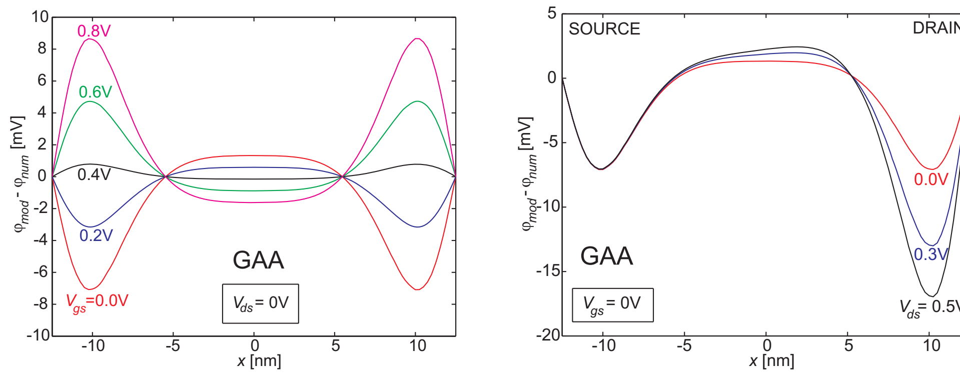

Figure 3.17: Difference between model and numerical simulations of GAA device for $V_{ds} = 0$V and different V_{gs} (left), and for $V_{gs} = 0$V and different V_{ds} (right), $t_{ox} = 0.1$nm.

approximately 2.4nm from the source and drain electrode in all cases.

The left plot of figure 3.18 shows the model error of three GAA-devices of different length with constant r_{si} and t_{ox}. The results show that the distance between the error peak and the source contact seems to be independent of the lateral dimensions as well.

In the right plot of figure 3.18 the model errors of three GAA-devices of different substrate radius are compared. We observe that the peak error

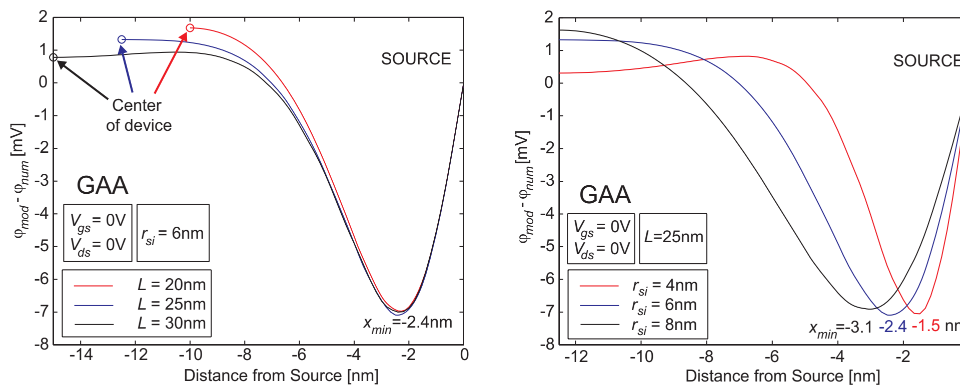

Figure 3.18: Difference between model and numerical simulations of GAA device for different device lengths, L (left) and different silicon radius, r_{si} (right), $V_{gs} = 0$V, $V_{ds} = 0$V $t_{ox} = 0.1$nm.

position is depending on the transversal dimensions, and moves closer to the source/drain contact for thinner devices. As λ_{DG} in (3.18) and λ_{GAA} in (3.19), which are the basis of the DG to GAA mapping technique, are given in terms of the silicon body radius/thickness and oxide thickness, and are independent of the gate length, these results are not unexpected.

Conclusion

In the above analysis we observed that the mapping of a DG solution into the GAA device resulted in two error peaks along the S-D symmetry line. Due to the peaks' proximity to the source and drain contacts, for all realistic length/height ratios, these errors do not significantly influence the modeling of the S-D energy barrier, which is situated close to the device center in the subthreshold regime. Therefore this approach should give adequate accuracy for the subthreshold drain current modeling.

3.4 Subthreshold Drift-Diffusion Current

As discussed above the main current path between source and drain in the subthreshold regime, will be along the S-D symmetry line. In deep subthreshold the density of mobile charge is so small that it does not significantly influence the electrostatics of the channel. The subthreshold drain current model is therefore based on the solution of Laplace's equation.

3.4.1 Double Gate Device

The drift diffusion current expressed as a function of quasi Fermi potential was introduced in equation (2.11). If we assume that V_F is constant over any given cross-section perpendicular to the x-axis, and assume that the mobile charges are distributed in accordance with classical Boltzmann statistics, ref. equation (2.8), the charge sheet density of equation (2.10) is given by

$$n_s(x) = \frac{2Wn_i^2}{N_a} \exp\left(\frac{-V_F}{V_{th}}\right) \int_{t'_{ox}}^{t_{si}} \exp\left(\frac{\varphi(x,y')}{V_{th}}\right) dy' = n_{s0}(x) \exp\left(\frac{-V_F}{V_{th}}\right) \tag{3.23}$$

where W is the device width. Here we introduce $n_{s0}(x)$, which multiplied by $e^{-V_F/V_{th}}$ equals the charge sheet density. Moving the factor $\exp\left(-\frac{V_F}{V_{th}}\right)$ outside the integral of equation (3.23), gives an analytical solution to the integral with V_F as the integration variable in equation (2.11) [59], i.e.

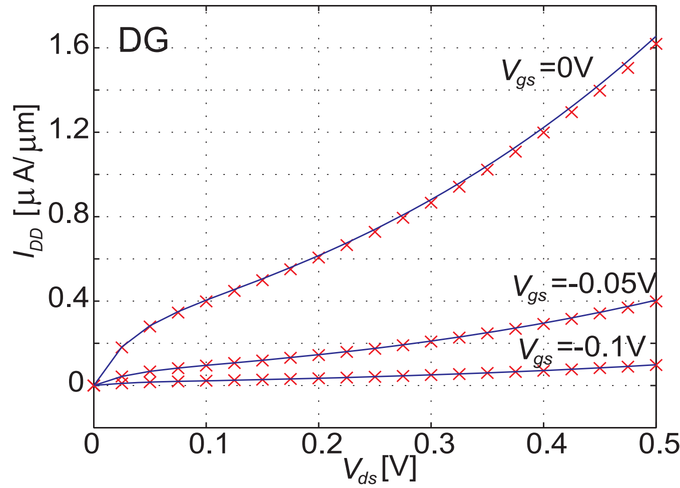

Figure 3.19: Modeled subthreshold drift diffusion current for DG (blue lines) compared with numerical simulations (red symbols).

$$I_{DD} = q\mu_n \frac{\int_0^{V_{ds}} \exp\left(\frac{-V_F}{V_{th}}\right) dV_F}{\int_{-L/2}^{L/2} \frac{dx'}{n_{s0}(x)}} = \frac{q\mu_n V_{th}\left(1 - \mathrm{e}^{-V_{ds}/V_{th}}\right)}{\int_{-L/2}^{L/2} \frac{dx'}{n_{s0}(x')}} \tag{3.24}$$

In the subthreshold regime, we consider the charge contribution to the potential negligible. Therefore, the total potential in equation (3.23) is approximated by the inter-electrode potential contribution, i.e. $\varphi(x,y) \approx \varphi_2(x,y)$.

The charge sheet density can be obtained by solving the integral of equation (3.23) numerically with Simpson's formula. Here, we have based the drift-diffusion current calculations on 101 equally spaced G-G cut-lines from source to drain, where $n_{s0}(x)$ is calculated for each of these cuts. This is inserted in the integral of equation (3.24), which again is solved numerically. We observe an excellent agreement between the model and the simulations in figure 3.19.

3.4.2 Cylindrical Gate-All-Around Device

The expression of drift diffusion current in equation (3.24) is still valid for the GAA device, however, when calculating the charge sheet density, n_{s0}, we must include the cylindrical geometry.

$$n_{s0}(x) = \frac{n_i^2}{N_a} 2\pi \int_0^{r_{si}} r' \exp\left(\frac{\varphi(x,r')}{V_{th}}\right) dr' \tag{3.25}$$

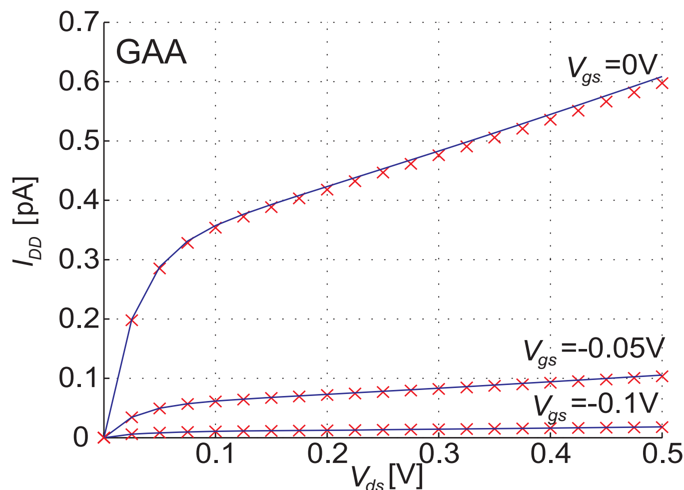

Figure 3.20: Modeled subthreshold drift diffusion current for GAA (blue lines) compared with numerical simulations (red symbols).

The charge sheet density can be obtained by solving the integral of equation (3.25) numerically with Simpson's formula. Here, the calculations are based on 101 equally spaced G-G cut-lines from source to drain to estimate $n_{s0}(x)$. This is inserted in the integral of equation (3.24), which also has to be solved numerically. We observe an excellent agreement between the modeled and the simulated current in figure 3.20.

3.5 Compact Subthreshold Current Model

The current calculations in section 3.4 applied numerical integration routines (Simpson's formula) in order to determine the charge sheet density, n_{s0}, for a number of equally spaced G-G cutlines. Additionally, the integral in the denominator of equation (3.24) was solved numerically. By making some simplifications a more compact, analytical solution to the drift diffusion current is possible.

Considering the GAA MOSFET, we know that the main current path between source and drain is along the S-D symmetry line in the subthreshold regime. The minimum potential along this path is the location of the energy barrier, whose height and shape are very important for determining the current. Differentiating equation (3.22) with respect to u along the S-D symmetry line, we obtain the following expression for u_{min} as derived for the

DG MOSFET in annex D (ref. equation (D.4) which must be mapped from the extended DG solution into the cross section of the GAA as described in section 3.3)

$$u_{min} = \frac{-(1+k')(V_D - V_S)}{2k'(V_D - 2V_G + V_S)}, \quad v_{min} = \sqrt{\frac{1}{k'} - u_{min}^2} \tag{3.26}$$

Using the conformal mapping function of (3.1) (replacing L by L' and k by k'), we obtain the corresponding x'_{min}, of the extended DG device. The position of the barrier minimum of the GAA MOSFET is then $x_{min} = x'_{min}\frac{\lambda_{GAA}}{\lambda_{DG}}$ and the barrier potential is given by $\phi_{min} = \varphi_2(u_{min}, v_{min})$.

We then assume that the gate-to-gate potential profile at the barrier can be approximated by a parabola

$$\varphi_{min}(x_{min}, r) = V_G + (\phi_{min} - V_G)\left[1 - \left(\frac{r}{r'_{ox} + r_{si}}\right)^2\right] \tag{3.27}$$

Using this parabolic approximation of the gate-to-gate potential profile at the barrier we obtain an analytical solution of the charge sheet density of equation (3.25)

$$\begin{aligned} n_{s0min} &= \frac{n_i^2}{N_a} 2\pi \int_0^{r_{si}} r' \exp\left(\frac{\varphi(x, r')}{V_{th}}\right) dr' \qquad (3.28) \\ &= \frac{n_i^2 \pi (r'_{ox} + r_{si})^2 V_{th}}{N_a(\phi_{min-V_G})} \cdot e^{\frac{\phi_{min} r'_{ox}(r'_{ox}+2r_{si}) + V_G r_{si}^2}{V_{th}(r'_{ox}+r_{si})^2}} \left[e^{\frac{r_{si}^2(\phi_{min}-V_G)}{(r'_{ox}+r_{si})^2 V_{th}}} - 1\right] \end{aligned}$$

We also apply a parabolic approximation of the potential profile along the S-D symmetry line.

$$\varphi(x) = \phi_{min} + (x - x_{min})^2 \varphi''_{2min} \tag{3.29}$$

Here ϕ_{min} is the barrier potential and $\varphi''_{2min} = \left.\frac{d^2\varphi_2}{dx^2}\right|_{x=x_{min}}$ is the curvature of the inter-electrode potential at the barrier point ($u = u_{min}$) as derived for the DG MOSFET in annex D (ref. equation (D.8), which must be mapped from the extended DG solution into the cross section of the GAA as described in section 3.3). This parabola will not terminate in the correct boundary potentials at the source and drain contacts. However, as the parabola has the correct curvature at the barrier point, the potential profile in the vicinity of the barrier becomes quite accurate. In fact, as long as we model the potential profile correctly before it increases 2-3 thermal voltages from the barrier

voltage the most significant contribution to the integral in the denominator of equation (3.24) is modeled correctly.

The integral in the denominator of equation (3.24) can then be approximated to:

$$\int_{-L/2}^{L/2} \frac{dx'}{n_{s0}(x')} \approx \frac{e^{\frac{\phi_{min}}{V_{th}}}}{n_{s0min}} \int_{-L/2}^{L/2} \frac{dx'}{\exp\left(\frac{\varphi(x')}{V_{th}}\right)}$$
$$= \frac{\sqrt{\pi V_{th}}\left[\text{erf}\left(\frac{\sqrt{\varphi''_{2min}}(L-2x_{min})}{2\sqrt{2}\sqrt{V_{th}}}\right) + \text{erf}\left(\frac{\sqrt{\varphi''_{2min}}(L+2x_{min})}{2\sqrt{2}\sqrt{V_{th}}}\right)\right]}{n_{s0min}\sqrt{2\varphi''_{2min}}} \tag{3.30}$$

where the error function is defined as $\text{erf}(z) = \frac{2}{\sqrt{\pi}} \int_0^z e^{-t^2} dt$.

Figure 3.21 illustrates the modeled subthreshold current obtained by this simplified method. Both in figure 3.20 and 3.21 the maximum relative deviation between the model and the numerical simulations occurs at $V_{gs} = 0\text{V}$ and $V_{ds} = 0.5\text{V}$ and is 1.8% and 1.2%, respectively. The increasing error for increasing V_{gs} can be explained by the increasing density of mobile charges, which are ignored in these subthreshold models. Anyway, a max deviation below 2% is indeed acceptable. A marginally better result in the compact model compared to the more exact modeling scheme, could reflect effects introduced by the parabolic trial functions which fortuitously turn out more accurate in this case.

A similar comparison at $V_{gs} = -0.1\text{V}$ and $V_{ds} = 0.5\text{V}$ gives 0.5% and 0.8% relative deviation between the models and simulations in figure 3.20 and 3.21, respectively. As should be expected, the exact modeling scheme gives better results than the compact model in this case.

A similar compact current model is possible for the DG MOSFET, as will be reported in [60]. However, in the expression of the charge sheet density, n_{s0min}, ref. equation (3.28), error functions will replace some of the exponential functions. Consequently, the 3D cylindrical geometry leads to a simplified expression of the charge sheet density of parabolic potential profiles as compared to the DG MOSFET.

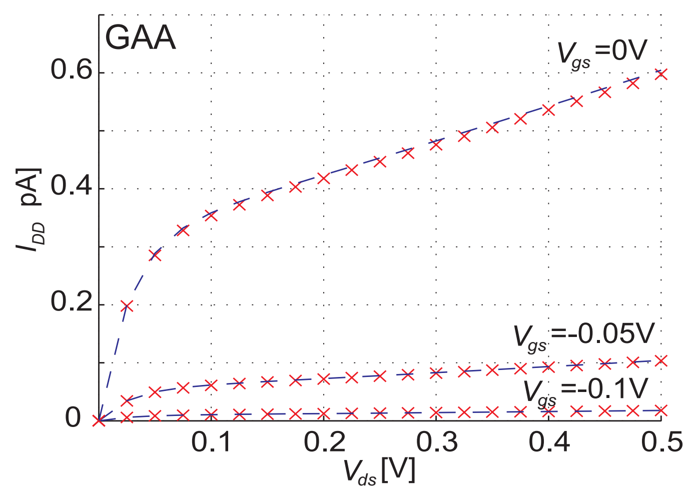

Figure 3.21: Compact model of subthreshold drift diffusion current for GAA (blue dashed lines) compared with numerical simulations (red symbols).

Chapter 4

Near and Above Threshold

4.1 Introduction

Poisson's equation can be divided in two superimposed parts, as described in section 2.2.1. The Laplace equation describes the inter-electrode capacitive coupling, ref. chapter 3. This is the dominating contribution to the device electrostatics in the subthreshold regime. When the gate bias is increased, however, we reach a point where the electrostatic effect of the inversion charge can no longer be neglected. Poisson's equation is solved self-consistently in 2 and 3 dimensions for the DG and GAA MOSFET, respectively, to determine this inversion charge contribution. At finite drain bias, the self-consistency also encompasses the quasi-Fermi potential distribution and the drain current.

In section 4.2 and 4.3 these procedures are described for the DG and GAA MOSFET, respectively. There is a separate procedure for the near threshold and the above threshold operation regimes for both devices.

4.2 Double-Gate MOSFET

4.2.1 DG Near Threshold

The charge contribution to the DG electrostatics, φ_1, is given by the 2D Poisson's equation, ref. equation (2.5). Our approach involves determining the parameters of a set of modeling functions self-consistently in accordance with the 2D Poisson's equation and the boundary conditions. The modeling

functions approximate the potential profiles along the S-D symmetry line and along a number of equally spaced G-G cutlines.

The procedure is initialized by the 1D Poisson's equation in the y-direction and an estimate of the quasi-Fermi potential at the center point. The modeling functions are then updated self-consistently in accordance with 2D Poisson's equation. This procedure is described in detail in the following.

Initialization - Quasi-Fermi Potential

The quasi-Fermi potential as a function of x is derived from equation (3.24)

$$V_F(x) = -V_{th} \ln \left(1 - \frac{I_{DD}}{q\mu_n V_{th} W} \int_{-L/2}^{x} n_{s0}(x')dx' \right) \tag{4.1}$$

where $n_{s0}(x)$ is given in equation (3.23). Initially the charge sheet density is calculated assuming $\varphi(x, y) = \varphi_2(x, y)$, i.e. we ignore the charge term. When increasing the gate biasing from subthreshold conditions up to the threshold voltage, the charge contribution increases and becomes quite significant. This leads to an increasing error in the initial estimate of V_F. However, the quasi-Fermi potential rapidly converges in the subsequent iterations when the charge contribution is included in the self-consistent procedure as described below.

Center Potential and Gate-to-Gate Symmetry Line

Based on the initial value of $V_F(0)$, we can estimate the center potential, $\varphi_1 \left(0, t'_{ox} + \frac{t_{si}}{2}\right) = \phi_{1c}$. We assume that the charge contribution to the gate-to-gate (G-G) potential has a parabolic shape given by

$$\varphi_1(0, y) = \phi_{1c} \left[1 - \left(1 - \frac{y}{t'_{ox} + \frac{t_{si}}{2}} \right)^2 \right] \tag{4.2}$$

which satisfies the boundary conditions at the gate contacts, i.e. $\varphi_1(0, 0) = \varphi_1 (0, 2t'_{ox} + t_{si}) = 0$, and at the device center, i.e. $\varphi_1 \left(0, t'_{ox} + \frac{t_{si}}{2}\right) = \phi_{1c}$. From equation (4.2) we find

$$\frac{d^2\varphi_1}{dy^2} = -\frac{2\phi_{1c}}{\left(t'_{ox} + \frac{t_{si}}{2}\right)^2} \tag{4.3}$$

Hence for the device center, the 2D Poisson's equation can be written as

$$-\frac{2\phi_{1c}}{\left(t'_{ox}+\frac{t_{si}}{2}\right)^2}=\frac{qn_i^2}{\varepsilon_{si}N_a}\exp\left(\frac{\phi_{1c}+\varphi_2\left(0,t'_{ox}+\frac{t_{si}}{2}\right)-V_F(0)}{V_{th}}\right)-\frac{d^2\varphi_1}{dx^2} \quad (4.4)$$

The x-curvature, $\frac{d^2\varphi_1}{dx^2}$, is set equal to zero in the initial solution. In subsequent iterations, however, the x-curvature at the center point is estimated from the modeling expression of the S-D symmetry line.

Figure 4.1 compares the modeled center potential (final value after iterative procedure has converged), $\phi_c - V_{gs} + V_{FB}$, with numerical simulations (where $\phi_c = \phi_{1c} + \phi_{2c}$ is the sum of the charge and inter-electrode contributions to the potential at the center point). For $V_{gs} > 0.3$V, the assumption of a parabolic G-G potential profile tends to break down. At this biasing level mobile charges commence to accumulate at the silicon-insulator interfaces and give a significant contribution to φ_1. The G-G potential profile in these regions will have high curvature which can not be represented accurately by a parabolic curve shape.

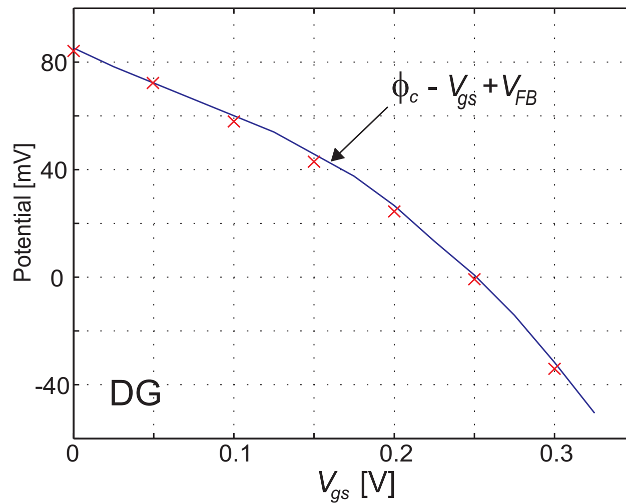

Figure 4.1: The amplitude of the center potential, $\phi_c - V_{gs} + V_{FB}$, plotted as a function of gate bias. The self-consistent solution is plotted with the blue line and the numerical simulations are marked with red symbols. ($V_{ds} = 0$V)

Source-to-Drain Symmetry Line

Next, we consider the potential distribution along the S-D symmetry line. Below threshold the total potential is relatively large close to the source and drain contacts, allowing a significant amount of charges to accumulate in these regions [11][37]. These accumulated charges give a rapid change of the potential and a high x-curvature in these regions. As we approach the central region of the device, however, the the gate contacts and the curvature in the y-direction start to dominate the electrostatics. In the transition between the source/drain influenced regions, and the central gate influenced region, two characteristic potential minima are formed along the S-D symmetry line of the charge potential. These minima tend to melt together when the gate voltage is increased above 0.3V, for the device considered, as the charge accumulation effect in the source/drain regions becomes less pronounced, and similarly the charge density in the central region increases.

This tendency can be observed in figure 4.2 where the charge potential, φ_1, along the S-D symmetry line is plotted for different gate biasing conditions ($V_{ds} = 0$V). At $V_{gs} = 0.3$V, we observe that the potential minima have moved further away from the source/drain contacts and are less distinct, as compared to the plots of $V_{gs} = 0.1$ and 0.2V.

The charge contribution to the potential profile, φ_1, along the S-D symmetry

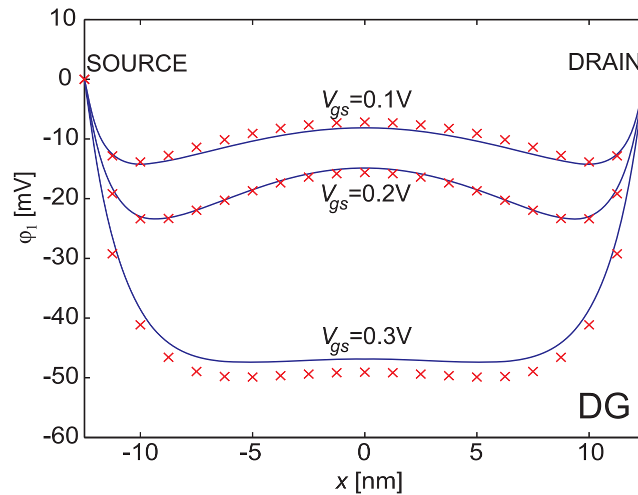

Figure 4.2: The charge potential, φ_1, along the S-D symmetry line for different gate biasing ($V_{ds} = 0$V). Model is plotted with blue lines and numerical simulations indicated with red symbols.

line is modeled by considering the charge accumulation close to the source and drain contacts and combine these with a forth order modeling expression to model the potential profile in the central region. The potential is calculated self-consistently in accordance with the 2D Poisson's equation at the center point and at the minima. Additionally we estimate the electric field at the source and drain contact and apply the given boundary conditions.

The perpendicular electric field at the source and drain contacts can be approximated by applying a 1D Poisson's equation and assuming a linear approximation for the potentials, as reported in [3][11]. The electric field of the inversion charge near source, $\mathbf{E}_{S1} = -\frac{d\varphi_1}{dx}\Big|_{x=-L/2}$, can be written as

$$\mathbf{E}_{S1} \approx \frac{qn}{\varepsilon_{si}} \int_{-\frac{L}{2}}^{\infty} \exp\left(-\frac{(\mathbf{E}_{S1}+\mathbf{E}_{S2})\left(x+\frac{L}{2}\right)}{V_{th}}\right) dx = \frac{qnV_{th}}{\varepsilon_{si}(\mathbf{E}_{S1}+\mathbf{E}_{S2})} \tag{4.5}$$

where $\mathbf{E}_{S2} = -\frac{d\varphi_2}{dx}\Big|_{x=-L/2}$, which will be described in more detail below. The electron concentration at the boundary between the body and the source contact is given by $n = \frac{n_i^2}{N_a}\exp\left(\frac{V_{bi}}{V_{th}}\right)$, ref. equation (2.8). If equation (4.5) is solved for $\mathbf{E}_{S1}$, we obtain

$$\mathbf{E}_{S1} = -\frac{\mathbf{E}_{S2}}{2}\left[1 \pm \sqrt{1 + 2\left(\frac{\mathbf{E}_0}{\mathbf{E}_{S2}}\right)^2}\right] \tag{4.6}$$

where $\mathbf{E}_0 = \sqrt{\frac{2qnV_{th}}{\varepsilon_{si}}}$, the plus sign is applied for $V_{GS} - V_{FB} \leq V_S$ and the minus sign for $V_{GS} - V_{FB} > V_S$. Note that (4.6) can also be used to determine $\mathbf{E}_{D1}$ by replacing $\mathbf{E}_{S2}$ by $\mathbf{E}_{D2}$.

The E-field of equation (4.6) is based on two assumptions. First, the potential is assumed to be linear along the S-D symmetry line close to the source and drain contact. Second, the infinite upper limit of the integral demands that the significance of the exponent inside the integral of equation (4.5) vanishes within the limits of where the linear approximation is reasonable. The potential must fall off by 2-3 thermal voltages in the linear region for this to be true. This is normally a good assumption below and near threshold.

The electric field from the inter-electrode coupling, $\mathbf{E}_{S2}$, can be found by differentiating the potential distribution in equation (3.9), $\frac{d\varphi_2}{du}$, and the conformal mapping transform in (3.1), $\frac{dx}{du}$, along the S-D symmetry line. Details of this calculation are given in annex D. At the center of the source contact the following analytical expression is obtained

$$\mathbf{E}_{S2} = \frac{-2}{L\pi}\left(\frac{1-k}{1+k}\right)\left[V_G\frac{4\sqrt{k}}{1-k} + V_D\frac{1-\sqrt{k}}{1+\sqrt{k}} - V_S\frac{1+\sqrt{k}}{1-\sqrt{k}}\right]\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right) \tag{4.7}$$

Similarly on the drain side, $\mathbf{E}_{D2} = -\frac{d\varphi_2}{dx}\Big|_{x=L/2}$ one obtains

$$\mathbf{E}_{D2} = \frac{2}{L\pi}\left(\frac{1-k}{1+k}\right)\left[V_G\frac{4\sqrt{k}}{1-k} - V_D\frac{1+\sqrt{k}}{1-\sqrt{k}} + V_S\frac{1-\sqrt{k}}{1+\sqrt{k}}\right]\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right) \tag{4.8}$$

Under these assumptions the contribution to the potential from the charge accumulation can be calculated to

$$\phi_{SA} \approx \mathbf{E}_{S1}\int_{-\frac{L}{2}}^{\infty}\exp\left(-\frac{(\mathbf{E}_{S1}+\mathbf{E}_{S2})\left(x+\frac{L}{2}\right)}{V_{th}}\right)dx = -\frac{1}{2}\left(\frac{\mathbf{E}_0}{\mathbf{E}_{S1}+\mathbf{E}_{S2}}\right)^2 V_{th} \tag{4.9}$$

At the drain side $\mathbf{E}_{S1}$ and $\mathbf{E}_{S2}$ are replaced by $\mathbf{E}_{D1}$ and $\mathbf{E}_{D2}$, respectively. We note from equation (4.6) that in the limiting case of $\mathbf{E}_{S2} = 0$, $\mathbf{E}_{S1} = \frac{\mathbf{E}_0}{\sqrt{2}}$. Therefore, the charge accumulation potential has a maximum value of $|\phi_{SA}|_{max} = |\phi_{DA}|_{max} = V_{th}$.

The electronic contribution to the potential will vanish exponentially when moving away from the source and drain contacts. This is modeled with the following function

$$\varphi_{SA}(x) = \phi_{SA}\exp\left(-\frac{(\mathbf{E}_{S1}+\mathbf{E}_{S2})\left(x+\frac{L}{2}\right)}{V_{th}}\right) \tag{4.10}$$

However, due to the linear approximation of equation (4.5), the magnitude of ϕ_{SA} of equation (4.9) will always be smaller than the potential drop from the source/drain contact to the corresponding minimum. Therefore, in our modeling scheme, we scale the exponential expression of equation (4.10) by a factor, α_S and correspondingly α_D on the drain side. Initially $\alpha_S = \alpha_D = 2$.

We then combine these exponential functions with a forth order function

$$\begin{aligned}\varphi_1\left(x, t'_{ox}+\frac{t_{si}}{2}\right) = {} & ax^4+bx^3+cx^2+dx+e+ \\ & \alpha_S\phi_{SA}\exp\left(-\frac{(\mathbf{E}_{S1}+\mathbf{E}_{S2})\left(x+\frac{L}{2}\right)}{\alpha_S V_{th}}\right)+ \\ & \alpha_D\phi_{DA}\exp\left(-\frac{(\mathbf{E}_{D1}+\mathbf{E}_{D2})\left(x-\frac{L}{2}\right)}{\alpha_D V_{th}}\right)\end{aligned} \tag{4.11}$$

Note that α_S and α_D are also included in the denominator of the exponential functions so that the derivative of these terms are independent of the scaling factors at the source and drain contacts. The parameters a, b, c, d and e of (4.11) are found from the following boundary conditions.

- Center potential from equation (4.4), $\varphi_1\left(0, t'_{ox} + \frac{t_{si}}{2}\right) = \phi_{1c}$.
- The potential at the source and drain contact, $\varphi_1\left(\mp\frac{L}{2}, t'_{ox} + \frac{t_{si}}{2}\right) = 0$.
- Estimated E-field at source and drain contact $\left.\frac{d\varphi_1}{dx}\right|_{x=\mp\frac{L}{2}} = -\mathbf{E}_{S1/D1}$.

The scaling factors, α_S and α_D, are optimized so that the 2D Poisson's equation is satisfied in the two minima. The positions of these minima are given by the modeling expression (4.11), and the x-curvature can be found directly from the second derivative of (4.11). The y-curvature is determined by drawing a parabola between the gate-boundaries an the potential minima (ref. equation (4.2) and (4.3)). We then apply a binary search pattern to determine the scaling factors, $\alpha_{S/D}$, which give the minimum deviation between the left and right hand side of the 2D Poisson's equation in these points.

Figure 4.3 illustrates an example of the different contributions in equation (4.11), and figure 4.4 compares the modeled potential contribution from the charge, φ_1, the inter-electrode coupling, φ_2, and the total potential, φ, with numerical simulations.

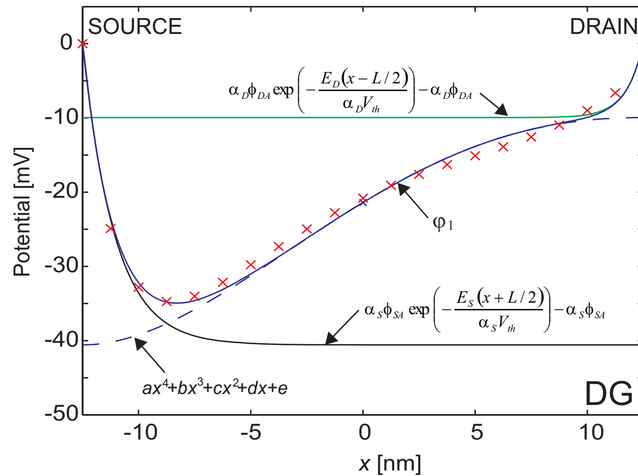

Figure 4.3: The charge potential, φ_1, along the S-D symmetry line for $V_{gs} = 0.25$V and $V_{ds} = 0.5$V. Different contributions to modeled charge potential are indicated. Numerical simulations are plotted with red symbols. Note that $\alpha_S\phi_{SA}$ and $\alpha_D\phi_{DA}$ have been subtracted from the exponential terms to ease the comparison of the different contributions.

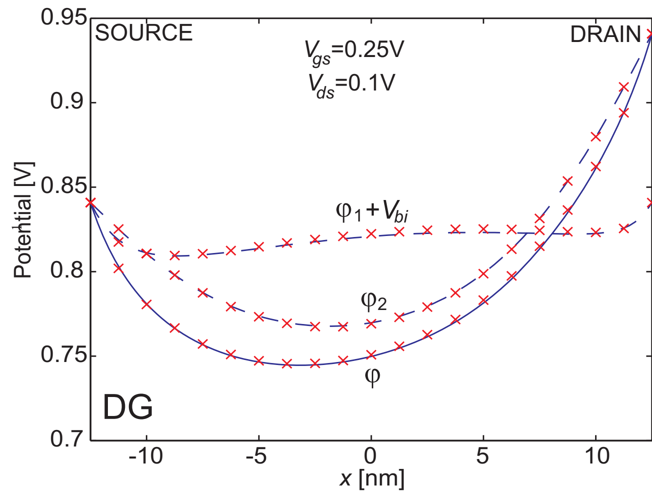

Figure 4.4: Modeled and numerically simulated total potential, φ, and the contributions, φ_1 and φ_2 along the S-D symmetry line for $V_{gs} = 0.25$V and $V_{ds} = 0.1$V. The constant voltage V_{bi} has been added to φ_1 to ease the comparison of the different terms.

Gate-to-Gate Cutlines

Based on the results for φ_1 along the S-D symmetry line, we can calculate φ_1 of a number of equally spaced G-G cutlines from source to drain. The G-G cuts, which represent the charge contribution to the potential, $\varphi_1(x, y)$, are modeled by parabolas as given in equation (4.2), where ϕ_{1c} is replaced by the corresponding value of the modeled S-D potential profile $\varphi_1\left(x, t'_{ox} + \frac{t_{si}}{2}\right)$.

Drain Current and Quasi-Fermi Potential

The drift-diffusion current was introduced in equations (2.11) and (3.24). In the drift-diffusion current expression we have to determine the charge sheet density, $n_{s0}(x)$, as given in equation (3.23).

The integral of (3.23) is calculated numerically, using Simpson's formula, for a number of equally spaced G-G cuts from source to drain, ref. discussion above and figure 4.5. Note that it is the total potential $\varphi = \varphi_1 + \varphi_2$ that enters into the exponential of equation (3.23). Simpson's formula is also applied when solving the integral in the denominator of the current expression in equation (3.24).

A new estimate of the quasi-Fermi potential, $V_F(x)$, can then be obtained by equation (4.1). Based on this new estimate of $V_F(x)$, we can return to find a better estimate of the center potential. Then the parameters of the S-D symmetry line are updated, which in turn gives new boundary conditions of the G-G cut lines. This updated potential distribution leads to a new estimate of the current and V_F, and the procedure can be repeated. The procedure typically converges after 2-3 iterations.

Figure 4.5 compares the modeled charge potential grid and numerical simulations for $V_{gs} = 0.25\text{V}$ and $V_{ds} = 0.1\text{V}$, and the inset shows the quasi-Fermi potential. Note that we do not explicitly model the silicon-insulator potential profiles, even though they are plotted with bold lines and compared to numerical simulations in the figure. These are based on the value of the equally spaced parabolic G-G cuts at the silicon-insulator interface. An excellent agreement between the model and the numerical simulations is observed.

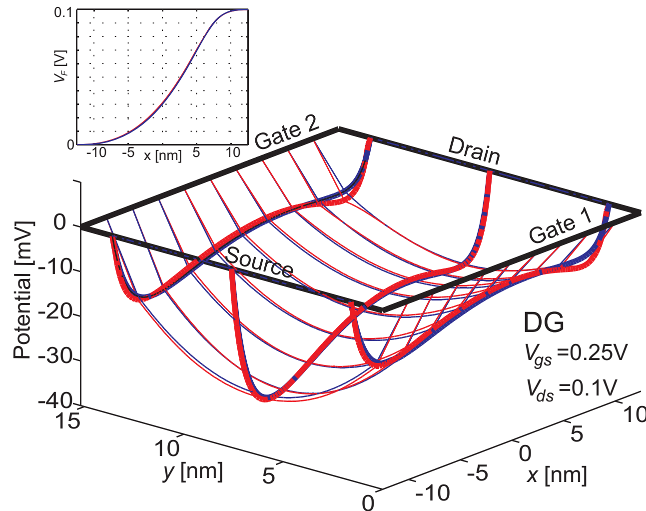

Figure 4.5: Modeled charge potential, φ_1, of the DG device (blue lines) compared to numerical simulations (Silvaco Atlas) (red lines). The plot includes 9 G-G cutlines, the S-D symmetry line (bold) and the silicon-insulator potential profiles (bold). Inset shows modeled quasi-Fermi potential ($V_F(x)$) (blue line) from source to drain compared to numerical simulations (red line).

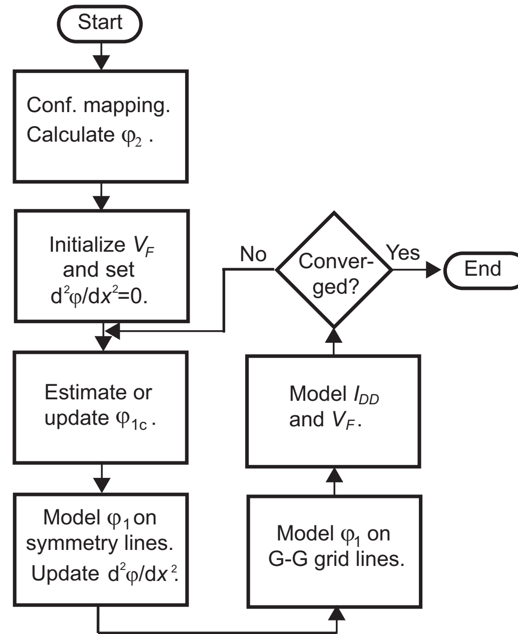

Figure 4.6: Flow diagram of self-consistent procedure of calculating electrostatics and current in the near threshold regime.

The self-consistent procedure for the near threshold regime, is summarized in the flow diagram of figure 4.6 [3]. The drift-diffusion current as a function of V_{ds} is plotted in figure 4.7 for V_{gs} from 0V to 0.3V. We observe an excellent agreement between the model and the numerical simulations.

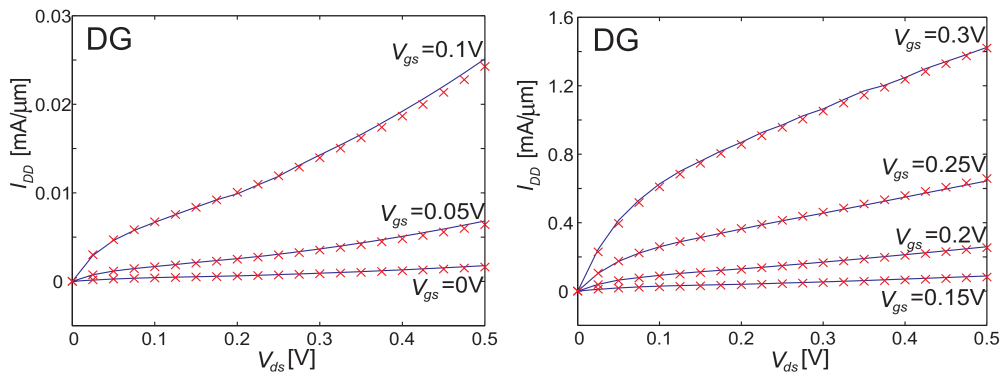

Figure 4.7: Modeled drift-diffusion current in the near threshold regime for DG (blue lines) compared to numerical simulations (red symbols).

4.2.2 DG Above Threshold

Similarly to the near-threshold modeling we apply a number of modeling functions whose parameters are optimized self-consistently in accordance with the 2D Poisson's equation, to model the electrostatics in the above threshold regime.

Initialization - Quasi-Fermi Potential

The quasi-Fermi potential is initialized by using a piecewise linear function with value of $V_F(0) = (1 - 0.8V_{ds})\frac{V_{ds}}{2}$ at the center, $x = 0$. This is found empirically as a good estimate for the device considered. A simple linear function, i.e. $V_F(x) = V_{ds}\frac{x}{L} + \frac{V_{ds}}{2}$, would also work, but the procedure would normally need an extra iteration to converge.

This serves as a starting point, and we will return to the self-consistent calculation of the quasi-Fermi potential at the end of this section.

Initialization of Center Potential and Gate-to-Gate Symmetry Line

Based on the initial value of $V_F(0)$, a first estimate of the potential profile along the G-G symmetry line is made by the 1D long channel solution of Taur et al. [25], ref. equation (2.21). As this is a solution of the 1D Poisson's equation, it is assumed that the x-curvature is zero, initially, i.e. $\left.\frac{d^2\varphi}{dx^2}\right|_{x=0} = 0$. Note this 1D solution gives the total potential, and the charge contribution is found by $\varphi_1(y) = \varphi(y) - \varphi_2(y)$.

Source-to-Drain Symmetry Line

Next, we establish the potential profile along the S-D symmetry line, which is modeled by a forth order polynomial in combination with exponential functions which model the charge accumulation close to the source/drain contacts, ref. (4.10)

$$\varphi_1 = ax^4 + bx^3 + cx^2 + dx + e + \phi_{SA}\mathrm{e}^{-\frac{S\left(x+\frac{L}{2}\right)}{V_{th}}} + \phi_{DA}\mathrm{e}^{-\frac{D\left(x-\frac{L}{2}\right)}{V_{th}}} \quad (4.12)$$

The parameters of the polynomial are found from the center potential (estimated by G-G symmetry line) and the potential and electric field at the source and drain contacts. These boundary conditions must be adjusted to account for the value and derivative of the two exponential terms.

The charge accumulation close to the source/drain contacts, which was discussed in section 4.2.1, is not as pronounced above threshold. Therefore the assumptions of equation (4.6) are no longer as accurate as in the near threshold regime. However, as the gate voltage is increased, the accuracy of the electrostatics along the S-D symmetry line becomes less important, since the channel has moved from the center of the device to the silicon-insulator interfaces. Therefore the charge accumulation terms in (4.12) do have adequate accuracy for this region as well. On the other hand, a more accurate modeling of the potential profile along the silicon-insulator interfaces is required, and we will return to this in a separate subsection below.

Figure 4.8 plots the S-D potential profile, φ_1, based on equation (4.12), where the center potential has been optimized self-consistently as described below. The inter electrode contribution, φ_2, and the total potential, φ, are also shown. The modeled potential profiles agree very well with the numerical simulations, and the maximum deviation is less than 5 mV.

Self-Consistent Adjustment of Center Potential

When the S-D and G-G symmetry lines have been established, the center potential is adjusted self-consistently in accordance with the 2D Poisson's

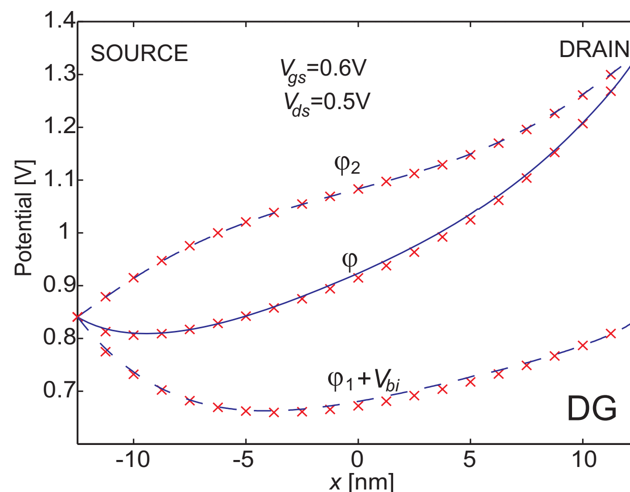

Figure 4.8: Modeled and numerically simulated total potential and the contributions, φ_1 and φ_2 along the S-D symmetry line for $V_{gs} = 0.6$V and $V_{ds} = 0.5$V. The constant voltage V_{bi} has been added to φ_1 to ease the comparison of the different terms.

equation (2.3), which is solved with respect to $\varphi = \phi_c$, i.e.

$$\phi_c = \varphi\left(0, t'_{ox} + \frac{t_{si}}{2}\right) = V_F(0) + V_{th}\ln\left(\frac{\frac{d^2\varphi}{dx^2} + \frac{d^2\varphi}{dy^2}}{\frac{qn_i^2}{\varepsilon_{si}N_a}}\right) \tag{4.13}$$

where the x-curvature is estimated from the second derivative of the modeling function of equation (4.12), i.e. $\frac{d^2\varphi_1}{dx^2} = 2c$, and the curvature of the inter-electrode potential, $\frac{d^2\varphi_2}{dx^2}$, which is derived in annex D. The y-curvature is estimated by the second derivative of the long channel solution in (2.21),

$$\frac{d^2\varphi}{dy^2} = \frac{8\beta^2 V_{th}}{\cos^2\left(\frac{\beta(t'_{ox}+t_{si}/2-y)}{t_{si}/2}\right)t_{si}^2} \tag{4.14}$$

which must be evaluated for $y = t'_{ox} + t_{si}/2$ (i.e. cos-function in denominator equals 1).

Based on the adjustment of the center potential, the potential profiles of the S-D and G-G symmetry lines can be updated accordingly.

Potential Profile along Silicon-Insulator Interface

The potential along the silicon-insulator interface is modeled by a set of modeling functions as indicated by the different colors in figure 4.9 and 4.10.

Source side (black curve): The black part of the curve in figure 4.10 extends from the center of the device to a distance t'_{ox} from the source contact and is modeled by a parabola.

The parameters of the parabola are determined from three points; at the center, $x = 0$, one effective insulator thickness from the source contact, $x = -L/2 + t'_{ox}$ and halfway between these points, $x = \frac{-L/2+t'_{ox}}{2}$. Initially we use Taur's long channel approximation [25]. Separate values of the auxiliary variable β must be calculated for each of these points based on the estimated quasi-Fermi voltage, $V_F(x)$, ref. equation (2.21).

In the following iterations the potential at these three points are adjusted self-consistently in accordance with the 2D Poisson's equation, ref. equation (4.13). The x-curvature is estimated from the second derivative of the parabola (black curve) which was calculated in the previous iteration. The y-curvature is approximated by the second derivative of the long channel approximation of equation (4.14), which must be evaluated for $y = t'_{ox}$.

Drain side: On the drain side we have two cases that must be treated differently depending on V_{ds}. To distinguish between them we use the following

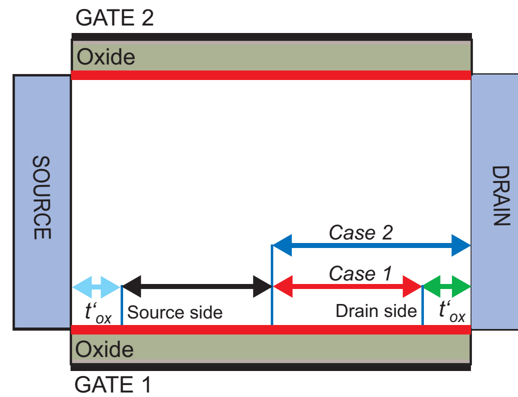

Figure 4.9: Cross section of DG device with different modeling regions indicated.

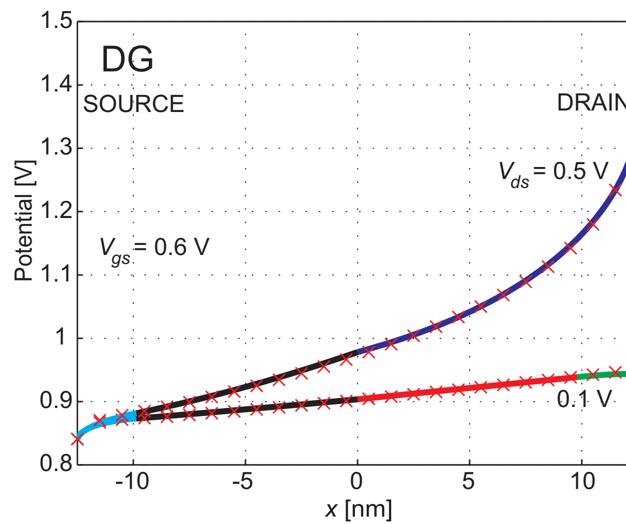

Figure 4.10: Silicon-interface surface potential of DG device for V_{gs} =0.6V and V_{ds} =0.1V and 0.5V. Red symbols are numerical simulations (Silvaco Atlas).

condition. When $V_{gs}-V_{FB} > V_{ds}+V_{bi}$, case 1 is applied, else case 2 is applied (ref. figure 4.9).

Case 1: For low drain biasing the surface potential is approximately linear up to a distance t'_{ox} from the drain contact as can be observed for $V_{ds} = 0.1$V in figure 4.10. We use Taur's long channel solution [25] to estimate the potential at $x = L/2 - t'_{si}$, and model the potential linearly between this point and the center point. This is indicated with the red line in figure 4.10.

As the x-curvature of the linear line is zero, self-consistency is fulfilled by the long channel solution at $x = L/2 - t'_{si}$ in this case.

Case 2: For higher drain biasing we use the following function to model the potential profile, which extends from the drain contact to the center

$$\varphi(x, t'_{si}) = A\left(x - \frac{L}{2}\right) + B\left(x - \frac{L}{2}\right)^{\frac{2}{3}} + V_D \qquad (4.15)$$

In annex A, we found that by carrying out a serial expansion about the drain contact corner the inter-electrode potential was described by a $\frac{2}{3}$-root term, ref. equation (A.10). The exponent of the B term in (4.15) is therefore based on this one-corner analysis. The silicon-insulator potential terminates at the sharp corner of the ideal drain contact, which is a weak singularity for the electric field. This means that the derivative of the potential, i.e. the electric field, approaches infinity at this point. A and B are determined by the potential at the center ($x = 0$) and at a point in between ($x = \frac{L}{4}$). The latter is initiated by Taur's long channel solution and adjusted self-consistently in accordance with equation (4.13), where the x-curvature is derived from (4.15), $\frac{d^2\varphi}{dx^2} = -\frac{2B}{9(x-L/2)^{\frac{4}{3}}}$, and the y-curvature is given by equation (4.14). The resulting potential profile is plotted with the blue line in figure 4.10.

Potential close to source and drain contacts: Close to the source contact (cyan curves) and close to the drain contact in case 1 (green curve), the surface potential is modeled by a combination of a term with exponent $\frac{2}{3}$ and linear term as in case 2 of the drain surface potential.

At the drain side we use equation (4.15), where A and B are decided from the value and derivative of the red line at $x = L/2 - t'_{ox}$. This is shown as the green line in figure 4.10.

At the source side appropriate sign changes must be applied to (4.15), and V_D must be replaced by V_S, i.e.

$$\varphi(x, t'_{ox}) = A\left(x + \frac{L}{2}\right) + B\left(x + \frac{L}{2}\right)^{\frac{2}{3}} + V_S \qquad (4.16)$$

The derivative of this function is infinity at the source contact corner, $x = L/2$, as desired. A and B are decided by the potential and derivative of the parabola at $x = -L/2 + t'_{ox}$ (black curve).

Gate-to-Gate Cutlines

Based on the S-D symmetry line and the silicon-insulator potential profile, we can calculate a number of equally spaced G-G cutlines from source to drain. The G-G cuts, which represent the total potential, $\varphi_1 + \varphi_2$, are modeled by a sixth order function

$$\varphi(y) = \hat{a}\left(y - \frac{t_{si}}{2} - t'_{ox}\right)^6 + \hat{b}\left(y - \frac{t_{si}}{2} - t'_{ox}\right)^4 + \hat{c}\left(y - \frac{t_{si}}{2} - t'_{ox}\right)^2 + \hat{d} \quad (4.17)$$

The parameters $\hat{a}$, $\hat{b}$, $\hat{c}$ and $\hat{d}$ are determined from the following boundary conditions

- The potential along the S-D symmetry line.
- The potential along the silicon-insulator interface.
- The derivative at the silicon-insulator interface, given by $\left.\frac{d\varphi}{dy}\right|_{y=t'_{ox}} = \frac{\varphi(x,t'_{ox})-V_G}{t'_{ox}}$, where we have assumed that the potential is linear through the insulator.
- The y-curvature along the S-D symmetry line of the device, which is determined self-consistently in accordance with the 2D Poisson's equation, i.e.

$$\frac{d^2\varphi}{dy^2} = \frac{qn_i^2}{\varepsilon_{si}N_a}\exp\left(\frac{\varphi(x, t'_{ox} + \frac{t_{si}}{2}) - V_F(x)}{V_{th}}\right) - \frac{d^2\varphi}{dx^2} = 2\hat{c} \quad (4.18)$$

  Here the x-curvature, $\frac{d^2\varphi}{dx^2} = \frac{d^2\varphi_1}{dx^2} + \frac{d^2\varphi_2}{dx^2}$, is estimated from the second derivative of the modeling function of (4.12), $\frac{d^2\varphi_1}{dx^2} = 12ax^2 + 6bx + 2c$ [1], and the curvature of the inter electrode potential, $\frac{d^2\varphi_2}{dx^2}$, which is derived in annex D.

Close to the source and drain contacts the G-G potential cuts become very flat in the central part and have high curvature close to the silicon-insulator

[1] The exponential terms of (4.12) can be ignored since they are only significant close to the source and drain electrodes, where we assume flat G-G profiles as described next.

interface. These boundary conditions can give unwanted oscillations in the modeling function of (4.17). To avoid this, we insert two triangles with one side along the source and drain contact and the triangle top at the S-D symmetry line, as indicated in figure 4.11. On the drain side the triangle top is assumed to be one characteristic length, λ_{DG}, ref. equation (3.18), from the contact. On the source side the triangle top is assumed to be at the minimum of the total potential along the S-D symmetry line, but not further than λ_{DG} from the source contact.

Inside the triangle the potential is modeled as constant in the y-direction and equal to the potential along the S-D symmetry line in the x-direction. Outside the triangle, a modified version of equation (4.17) is applied, where the $(y - \frac{t_{si}}{2} - t'_{ox})^n$ factors are replaced by $(y - y_\triangle(x))^n$, where $y_\triangle(x)$ is the y-value of the triangle edge, i.e.

$$\varphi(y) = \check{a}(y - y_\triangle(x))^6 + \check{b}(y - y_\triangle(x))^4 + \check{d} \tag{4.19}$$

We use the same set of boundary conditions as for equation (4.17), but the parabolic term, $\check{c}$, vanishes, as the curvature at the edge of the triangle is assumed to be zero.

Drain Current and Quasi-Fermi Potential

We follow the same procedure as in section 4.2.1 to determine the drift-diffusion drain current and quasi-Fermi potential. The charge sheet density, $n_{s0}(x)$, ref. equation (3.23), is obtained from the electrostatics which has been calculated above. The integral of (3.23) is calculated numerically, using Simpson's formula, for a number of equally spaced G-G cuts from source to drain. Simpson's formula is also applied when solving the integral in the numerator of the current expression in equation (3.24).

A new estimate of the drift-diffusion current and quasi-Fermi potential, $V_F(x)$, can be obtained by equation (3.24) and (4.1), respectively. Based on the new estimate of $V_F(x)$, we can return to find a better estimate of the center potential. Then the parameters of the S-D symmetry line and silicon-insulator potential profiles are updated, which in turn gives new boundary conditions of the G-G cut lines. This updated potential distribution leads to a new estimate of the drift diffusion current and $V_F(x)$, and the procedure can be repeated. The procedure typically converges after 2-3 iterations.

Figure 4.11 compares the modeled potential grid and numerical simulations for $V_{gs} = 0.6$V and $V_{ds} = 0.5$V, and the inset shows the quasi-Fermi potential. An excellent agreement between the model and the simulator is observed.

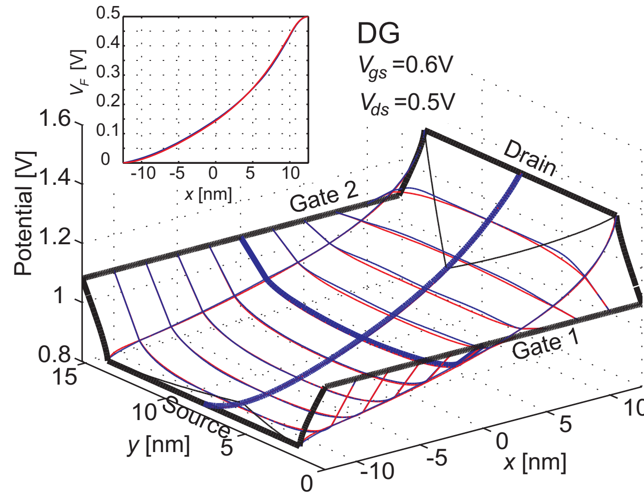

Figure 4.11: Modeled electrostatics of DG device (blue lines) compared to numerical simulations (Silvaco Atlas) (red lines). Includes 9 G-G cutlines (G-G symmetry line in bold), the S-D symmetry line (bold) and the silicon-insulator potential profiles. Inset shows modeled quasi-Fermi potential (blue) from source to drain compared to numerical simulations (red).

The self-consistent procedure for the above-threshold regime, is summarized in the flow diagram of figure 4.12 [3]. The drift-diffusion current as a function of V_{ds} is plotted in figure 4.13 for V_{gs} from 0.4V to 0.8V. An excellent agreement between the modeled drain current and the numerical simulations is observed.

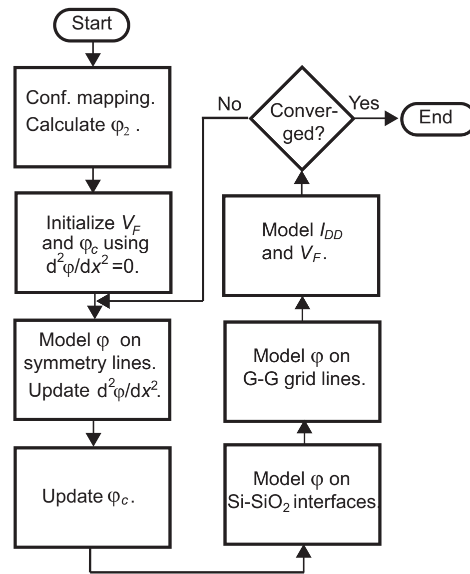

Figure 4.12: Flow diagram of self-consistent procedure of calculating electrostatics and current in the above threshold regime.

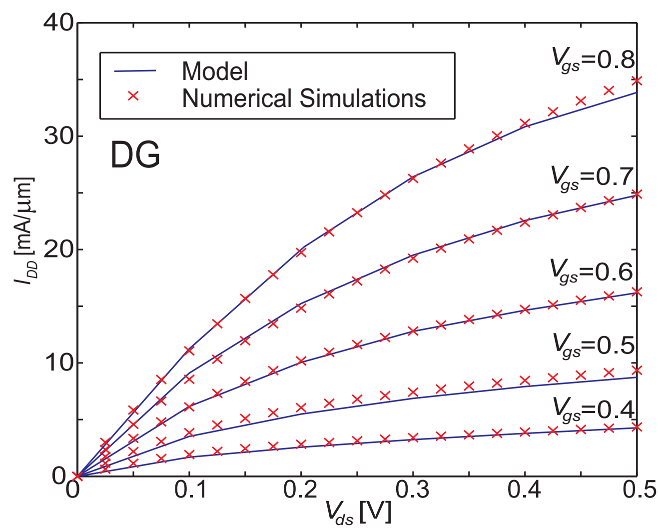

Figure 4.13: Modeled drift-diffusion current in the above threshold regime for DG (blue lines) compared to numerical simulations (red symbols).

4.3 Gate-all-Around MOSFET

The modeling of the cylindrical GAA device follows the same procedure and uses the same modeling functions as the DG MOSFET both in the near and above threshold regimes. The major difference is that the cylindrical geometry must be properly accounted for, and the self-consistency must be linked to the 3D Poisson's equation with cylindrical co-ordinates, ref. equation (2.4).

Section 4.3.1 outlines the modeling procedure in the near threshold regime and section 4.3.2 the procedure above threshold.

4.3.1 GAA Near Threshold

Initialization - Quasi-Fermi Potential

The charge sheet density, $n_{s0}(x)$, for the GAA device is given by equation (3.25). Initially, we assume that the inter-electrode contribution dominates the electrostatics, and set $\varphi(x, r') \approx \varphi_2(x, r')$ in the exponent inside the integral of $n_{s0}(x)$. Based on this estimate, the quasi-Fermi potential is initiated by equation (4.1).

Center Potential and Gate-to-Gate Symmetry Line

Very similar to what we did in the case of the DG device, we estimate the center potential $\varphi_1(0,0) = \phi_{1c}$ assuming that the charge contribution to the G-G potential has a parabolic shape given by

$$\varphi_1(0, r) = \phi_{1c}\left[1 - \left(\frac{r}{r'_{ox} + r_{si}}\right)^2\right] \tag{4.20}$$

which satisfies the boundary conditions at the gate contact, i.e. $\varphi_1(0, r'_{ox} + r_{si}) = 0$, and at the device center $\varphi_1(0,0) = \phi_{1c}$. From the cylindrical co-ordinates of Poisson's equation, we then find

$$\lim_{r\to 0}\left(\frac{1}{r}\frac{d\varphi_1}{dr} + \frac{d^2\varphi_1}{dr^2}\right) = -\frac{4\phi_{1c}}{(r'_{ox} + r_{si})^2} \tag{4.21}$$

Hence for the device center, Poisson's equation with cylindrical co-ordinates can be written as

$$-\frac{4\phi_{1c}}{(r'_{ox} + r_{si})^2} = \frac{qn_i^2}{\varepsilon_{si}N_a}\exp\left(\frac{\phi_{1c} + \varphi_2(0,0) - V_F(0)}{V_{th}}\right) + \frac{d^2\varphi_1}{dx^2} \tag{4.22}$$

The x-curvature, $\frac{d^2\varphi}{dx^2}$, is set equal to zero initially, and is estimated from the modeling function of the S-D symmetry line in subsequent iterations.

Figure 4.14 compares the modeled center potential (final value after iterative procedure has converged), $\phi_c - V_{gs} + V_{FB}$, with numerical simulations (where $\phi_c = \phi_{1c} + \phi_{2c}$). We observe a somewhat larger deviation between the model and the numerical simulations, compared to the DG device (ref. figure 4.1). The parabolic function might no longer be as accurate as the potential profile along the G-G symmetry line seems to be flatter close to the center of the cylinder. Additionally due to the cylindrical geometry the curvature of the parabola is multiplied by two in the center, ref. equation (4.21). Therefore the error in the curvature of the parabolic modeling function will be amplified. However, we observe that the maximum deviation in the center potential is in the order of 2-3 mV, and this is more than adequate.

Source-to-Drain Symmetry Line

The modeling of the charge potential along the S-D symmetry line is done in exactly the same manner as for the DG-device as described in section 4.2.1, applying the same modeling functions and boundary conditions. The assumptions made for calculating $\mathbf{E}_{S1}$ and $\mathbf{E}_{D1}$ are still valid. The electric

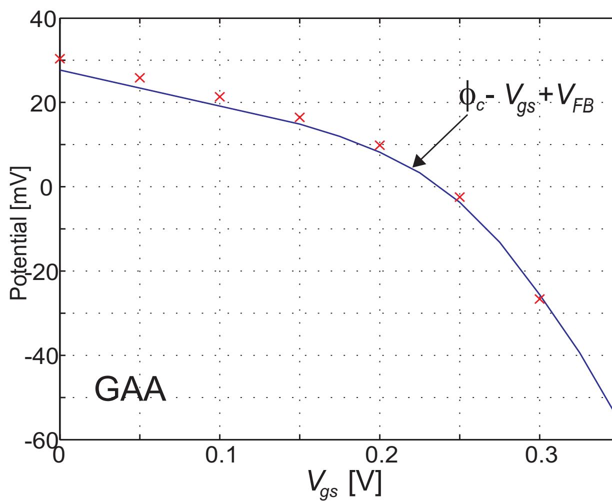

Figure 4.14: The amplitude of the center potential, $\phi_c - V_{gs} + V_{FB}$, plotted as a function of gate bias. The self-consistent solution is plotted with the blue line and the numerical simulations are marked with red symbols. ($V_{ds} = 0$V)

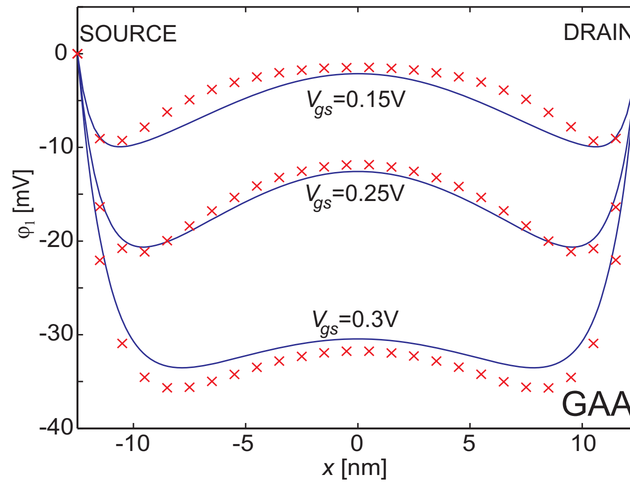

Figure 4.15: The charge potential plotted along the S-D symmetry line for different gate biasing, $V_{ds} = 0$V. Model is plotted with blue lines and numerical simulations indicated with red symbols.

fields from the inter-electrode contributions, $\mathbf{E}_{S2}$ and $\mathbf{E}_{D2}$, are given by the expressions in (4.7) and (4.8), respectively, replacing k by k', ref. equation (3.21).

Figure 4.15 shows the charge contribution to the potential, φ_1, along the S-D symmetry line plotted for three different gate biasing levels. We recognize the two potential minima close to the source and drain contacts, ref. discussion in section 4.2.1.

Figure 4.16 illustrates an example of the different contributions of the modeling function in equation (4.11) for the GAA device, and figure 4.17 compares the modeled potential contribution from the charge, φ_1, the inter-electrode coupling, φ_2, and the total potential, φ, with numerical simulations.

Gate-to-Gate Cutlines

Exactly as we did in the case of the DG device, we calculate a number of equally spaced G-G cutlines from source to drain. The G-G cuts, which represent the charge contribution to the potential, $\varphi_1(x, y)$, are modeled by parabolas as given in equation (4.20), where ϕ_{1c} is replaced by the corresponding value of the modeled S-D potential profile $\varphi_1(x, 0)$.

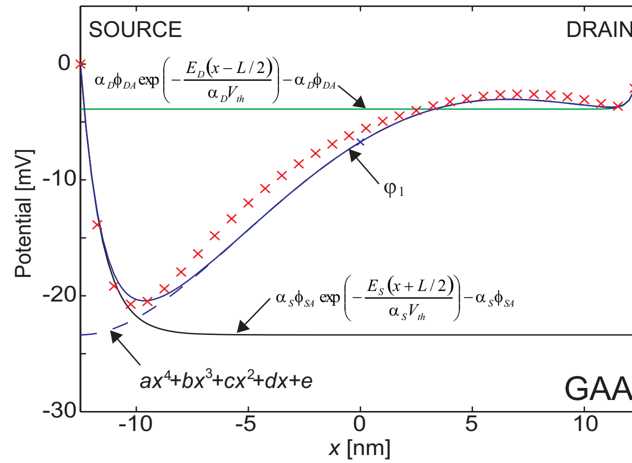

Figure 4.16: The charge potential, φ_1, along the S-D symmetry line for $V_{gs} = 0.25$V and $V_{ds} = 0.3$V. Different contributions to the modeled charge potential are indicated, ref. equation (4.11). Numerical simulations are plotted with red symbols. Note that $\alpha_S \phi_{SA}$ and $\alpha_D \phi_{DA}$ have been subtracted from the exponential terms associated with the source and drain sides, respectively, to ease the comparison of the different contributions.

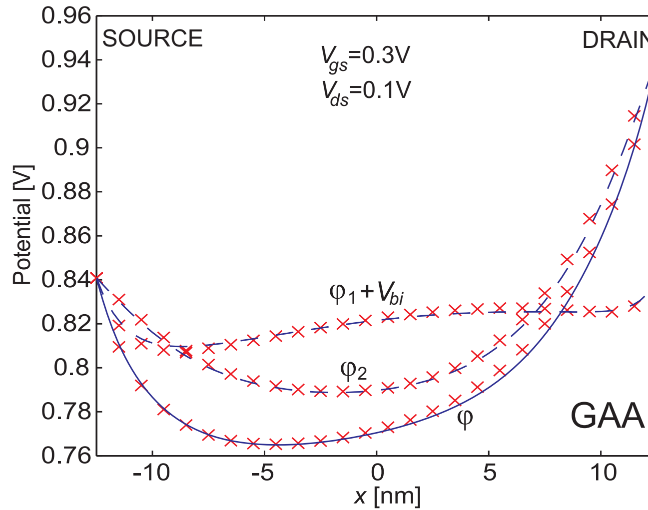

Figure 4.17: Modeled and numerically simulated total potential, φ, and the contributions, φ_1 and φ_2 along the S-D symmetry line for $V_{gs} = 0.3$V and $V_{ds} = 0.1$V. The constant voltage V_{bi} has been added to φ_1 to ease the comparison of the different terms.

Drain Current and Quasi-Fermi Potential

The drift-diffusion current, I_{DD}, and the quasi-Fermi potential are calculated in the same manner as for the DG device. However, we must account for the cylindrical geometry when calculating the charge sheet density, ref equation (3.25).

Based on this new estimate of $V_F(x)$, we can return to find a better estimate of the center potential. Then the parameters of the S-D symmetry line are updated, which in turn gives new boundary conditions of the G-G cut lines. This updated potential distribution leads to a new estimate of the current and $V_F(x)$, and the procedure can be repeated. The procedure typically converges after 2-3 iterations and is summarized in the flow diagram of figure 4.6.

Figure 4.18 compares the modeled charge potential grid with numerical simulations for $V_{gs} = 0.25$V and $V_{ds} = 0.1$V, and the inset shows the quasi-Fermi potential. An excellent agreement between the model and numerical simulations is observed.

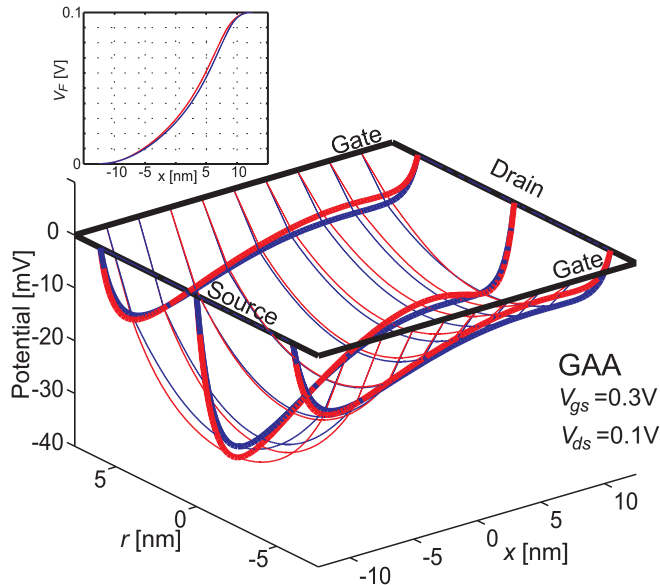

Figure 4.18: Modeled charge contribution to the electrostatics of GAA device (blue lines) compared to numerical simulations (Silvaco Atlas) (red lines). Includes 9 G-G cutlines, the S-D symmetry line (bold) and the silicon-insulator potential profiles (bold). Inset shows modeled quasi-Fermi potential (blue line) from source to drain compared to numerical simulations (red line).

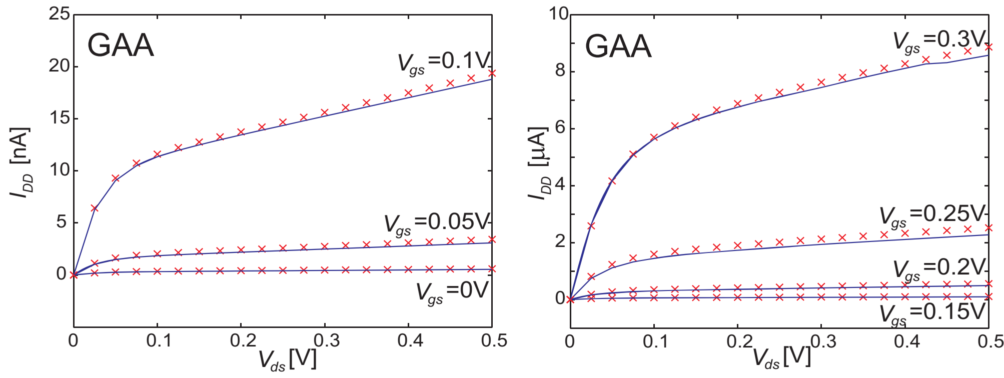

Figure 4.19: Modeled drift-diffusion current in the near threshold regime for GAA (blue lines) compared to numerical simulations (red symbols).

The modeled drift-diffusion current as a function of V_{ds} is plotted in figure 4.19 for V_{gs} from 0V to 0.3V. These results also agree very favorably with the numerical simulations.

4.3.2 GAA Above Threshold

Initialization

The quasi-Fermi potential is initialized by the same piecewise linear function as used for the DG device, ref. section 4.2.2. The initial value of $V_F(0)$ is then applied in the long channel solution of Iñiguez et al. [35], ref. equation (2.38), to initialize the potential profile along the G-G symmetry line. Initially the x-curvature is assumed to be zero, i.e. $\left.\frac{d^2\varphi}{dx^2}\right|_{x=0} = 0$.

Source-to-Drain Symmetry Line

The modeling of the charge potential, φ_1, along the S-D symmetry line is performed in the exactly same manner as for the DG-device as described in section 4.2.2, applying the same modeling functions and boundary conditions.

Figure 4.20 plots the S-D potential profile, φ, and the contribution from the inversion charge, φ_1 and inter-electrode, φ_2. The potential profiles agree very well with the numerical simulations.

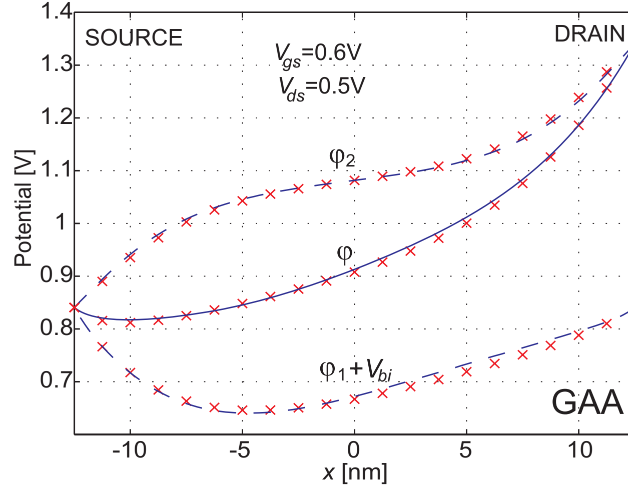

Figure 4.20: Modeled and numerically simulated total potential, φ, and the contributions, φ_1 and φ_2 plotted along the S-D symmetry line for $V_{gs} = 0.6$V and $V_{ds} = 0.5$V. The constant voltage V_{bi} has been added to φ_1 to ease the comparison of the different terms.

Self-Consistent Adjustment of Center Potential

When we have found estimates of the potential profiles along the S-D and G-G symmetry lines, the center potential is adjusted self-consistently in accordance with the 3D Poisson's equation, i.e.

$$\phi_c = \varphi(0,0) = V_F(0) + V_{th} \ln \left(\frac{\frac{d^2\varphi}{dx^2} + \frac{1}{r}\frac{d\varphi}{dr} + \frac{d^2\varphi}{dr^2}}{\frac{qn_i^2}{\varepsilon_{si} N_a}} \right) \tag{4.23}$$

where the x-curvature along the S-D symmetry line is estimated from the second derivative of the modeling function, φ_1, and the second derivative of the inter-electrode potential, $\frac{d^2\varphi_2}{dx^2}$. The latter is derived in annex D. The two terms of Poisson's equation involving variable r, are estimated by the long channel solution of equation (2.38)

$$\frac{1}{r}\frac{d\varphi}{dr} + \frac{d^2\varphi}{dr^2} = -\frac{8r_{si}^2 V_{th}(\beta - 1)}{\left[r_{si}^2 + r^2(\beta - 1)\right]^2} \tag{4.24}$$

which is evaluated for $r = 0$. This adjustment of the center potential updates the boundary conditions of the S-D and G-G cut lines.

Silicon-Insulator Potential Profiles

The potential along the silicon-insulator interface is modeled by the same set of modeling functions as for the DG device. The modeling functions are determined from a number of points along the interface, which are updated self-consistently. The x-curvature in these points are estimated from the modeling functions, and the two terms of Poisson's equation involving the variable r are estimated from the long channel solution of equation (4.24), evaluated at $r = r_{si}$.

Gate-to-Gate Cutlines

Based on the potential profile along the S-D symmetry line and the silicon-insulator interfaces, a number of equally spaced cutlines are calculated applying the modeling function of equation (4.17). The three first boundary conditions of the cutlines are equal to the boundary conditions for the DG model. However, the final boundary condition as given in equation (4.18), must be modified to account for the cylindrical geometry. Along the S-D symmetry line ($r = 0$), the two r-terms of Poisson's equation add up to $\lim_{r\to 0}\left(\frac{d^2\varphi}{dr^2} + \frac{1}{r}\frac{d\varphi}{dr}\right) = 2\frac{d^2\varphi}{dr^2}$. Therefore along the S-D symmetry line the r-curvature is given by

$$\left.\frac{d^2\varphi}{dr^2}\right|_{r=0} = \frac{1}{2}\left[\frac{qn_i^2}{\varepsilon_{si}N_a}\exp\left(\frac{\varphi(x, t'_{ox} + \frac{t_{si}}{2}) - V_F(x)}{V_{th}}\right) - \frac{d^2\varphi}{dx^2}\right] \tag{4.25}$$

Similar to the DG model, we introduce two triangles with one side along the source and drain electrodes, and the triangle top at the S-D symmetry line. Inside the triangle the potential is modeled as constant in the y-direction and equal to the potential along the S-D symmetry line in the x-direction. Outside the triangle equation (4.19) is applied (replacing y by the r-coordinate). On the drain side the triangle top is set to be one characteristic length, λ_{GAA}, from the drain contact, ref. equation (3.19). On the source side the triangle top is set to the minimum of the total potential along the S-D symmetry line, but not further than λ_{GAA} away from the source contact. These triangles are indicated in figure 4.21.

Drain Current and Quasi-Fermi Potential

The drain current and quasi-Fermi potential are calculated in the same manner as for the near-threshold regime of the GAA, ref. section 4.3.1. The

modeled quasi-Fermi potential is shown in the inset of figure 4.21 and the modeled drift-diffusion current as a function of V_{ds} is plotted in figure 4.22.

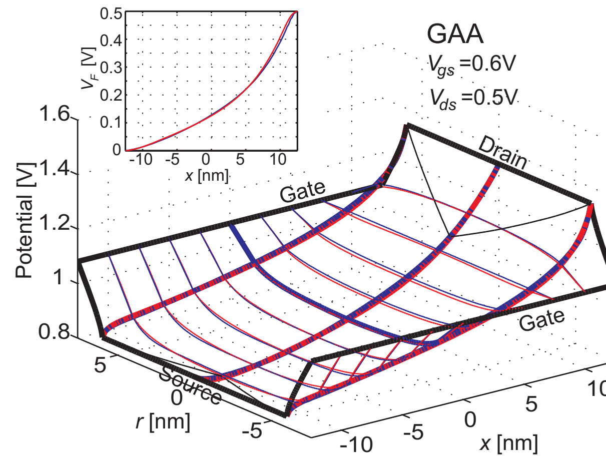

Figure 4.21: Modeled electrostatics of GAA device (blue lines) compared to numerical simulations (Silvaco Atlas) (red lines). Includes 9 G-G cutlines (G-G symmetry line in bold), the S-D symmetry line (bold) and the silicon-insulator potential profiles. Inset shows modeled quasi-Fermi potential ($V_F(x)$) (blue) from source to drain compared to numerical simulations (red).

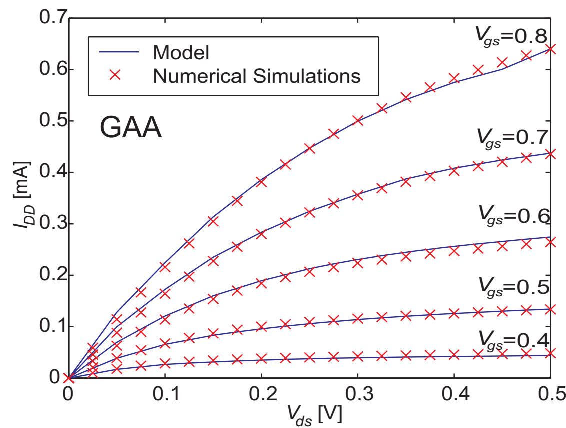

Figure 4.22: Modeled drift-diffusion current in the near threshold regime for GAA (blue lines) compared to numerical simulations (red symbols).

Chapter 5

Drain Current Modeling

5.1 Modeled Drift Diffusion Current

The drift diffusion current plotted as a function of V_{ds} in the subthreshold regime was presented in figure 3.19 and 3.20 for the DG and GAA devices, respectively. Similarly the drift-diffusion current of the DG device in near and above threshold regimes was presented in figure 4.7 and 4.13, and for the GAA device in figure 4.19 and 4.22.

In figure 5.1 the same results are presented in semi-logarithmic plots as a function of V_{gs}. Here, the subthreshold model is applied for $V_{gs} \leq 0$V, the near threshold model for 0V$< V_{gs} \leq 0.35$V and the above threshold model for $V_{gs} > 0.35$V for both the DG and the GAA MOSFET.

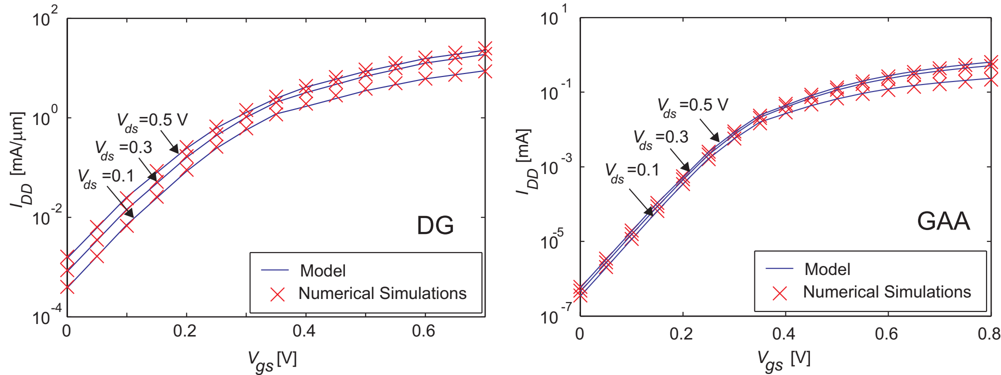

Figure 5.1: Modeled and simulated transfer characteristics of DG (left) and GAA MOSFET (right) for V_{ds} =0.1, 0.3 and 0.5V.

5.2 Compact Current Modeling

The main concern in compact modeling is to find analytical expressions for the current-voltage characteristics which are compatible with the efficiency requirements of circuit simulators. In section 3.4 an analytical model of the drift diffusion current in the subthreshold regime for the GAA MOSFET was presented.

A compact drain current model which covers all operating regimes from subthreshold to strong inversion, was presented in [11][61]. This model is based on an interpolation function which matches the limiting behavior in subthreshold and strong inversion, and at a point close to threshold.

$$I_{DD} = 10^{\wedge}\left[\log_{10}\frac{I_{sub}}{\left[1+\left(\frac{\log_{10}(I_{sub})}{\log_{10}(I_{inv})}\right)^{m}\right]^{\frac{1}{m}}}\right] \tag{5.1}$$

Here I_{sub} and I_{inv} are the asymptotes of the current in subthreshold and strong inversion regimes. These asymptotes are linear functions in the semilogarithmic plot and are determined by two points in subthreshold and two points in strong inversion, as indicated in the left plot of figure 5.2. The parameter m is found by matching the interpolated curve to the near threshold calculation as indicated by the asterisk in the left plot.

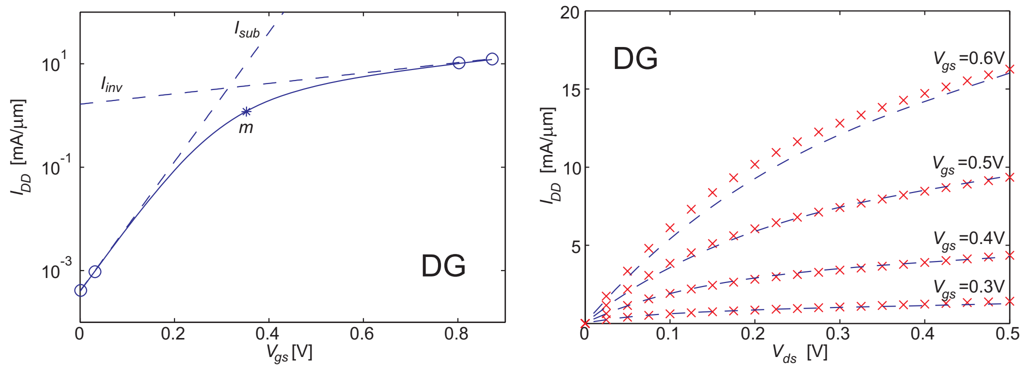

Figure 5.2: To the left the subthreshold and strong inversion asymptotes (dashed lines) and the near threshold current calculation (asterisk) are illustrated. The solid lines are the resulting interpolating function. To the right, the modeled DG compact current (dashed lines) is compared to numerical simulations (symbols).

The resulting drain current of the DG MOSFET is compared with numerical simulations in the right plot of figure 5.2. This compact modeling scheme can also be applied for the GAA MOSFET, and we obtain similar accuracy in the drift diffusion current as shown in [61].

5.3 Transport formalisms

In section 2.2.4 a brief introduction to some transport models was given. The modeled current in figure 5.1 is based on the drift diffusion model with constant mobility (DD). However, in nanoscale MOSFETs, with channel lengths less than about 100 nm [8], the scattering rates of the carriers indicate that the drain current will have the character of both drift-diffusion and ballistic/quasi-ballistic transport, with an increasing shift towards the latter with decreasing gate length. In the following we will carry out a comparison between the simple DD model and more sophisticated transport mechanisms [3].

Figure 5.3 compares numerically simulated DG and GAA MOSFET drain current I_d versus V_{gs} using different transport formalisms (energy transport, hydrodynamic, drift diffusion with velocity saturation (DDvs), and drift diffusion with constant mobility (DD)) at the gate lengths 12.5 nm, 25 nm, and 50 nm.

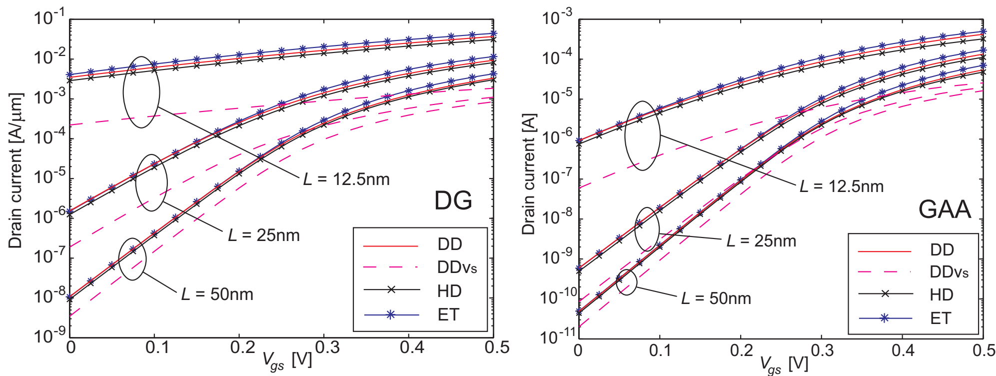

Figure 5.3: Simulated DG (left) and GAA (right) drain current versus gate bias for different transport formalisms and gate lengths, L =12.5, 25 and 50nm. $V_{ds} = 0.5$V. (DD=drift diffusion with constant mobility, DDvs=drift diffusion with velocity saturation, HD=hydrodynamic, ET=energy transport)

We notice that the energy transport (ET) formalism, which presumably is the most precise [16], consistently gives the highest I_d. The hydrodynamic model (HD), which is somewhat less precise, predicts a $20-30\%$ lower I_d for the 25 nm device in moderate to strong inversion. It is interesting to note that DD with constant mobility, using the default value from Atlas ($\mu_n = 1000\text{cm}^2/\text{Vs}$), gives results in between those of the ET and HD formalisms, tracking quite well their dependence on V_{gs}. As expected, DD with a typical saturation velocity (DDvs) gives I_d-values almost a decade lower than the other models for the 25 nm device, (using the Atlas default values of $v_s = 1.03 \cdot 10^7\text{cm/s}$ and $m = 2$, ref. equation (2.14)).

From this, we may conclude that, in the near-ballistic regime, the DDvs formalism fails to predict the magnitude of the drain current, primarily because of the limit imposed on the carrier velocity. However, using the DD formalism, which has no upper bound on the velocity, seems to compensate quite well for this deficiency to give estimates of I_d that are well within the range of values predicted by the physically better justified ET and HD formalisms. Moreover, a still better overall agreement with either ET or HD can be obtained simply by suitably adjusting the DD mobility parameter. Similar observations have also been made by comparison between DD transport and Monte Carlo simulations [62]. In terms of our modeling, the application of the DD represents a great simplification over the use of any of the other formalisms.

Chapter 6

Capacitance Modeling

In section 2.2.5, we introduced a capacitance model which is based on the charge conservation principle. We saw that a three terminal device can be described by 9 trans- and self-capacitances C_{XY}, of which 4 are independent. For symmetric gate biasing the DG MOSFET can be considered a three-terminal device, and the GAA device is also, indeed, a three terminal device.

The equivalent circuit of this capacitance model, which was presented in figure 2.2, is reprinted inside the DG/GAA-cross section in figure 6.1. Note that we assume that the gate contacts overlap the source and drain contacts, and

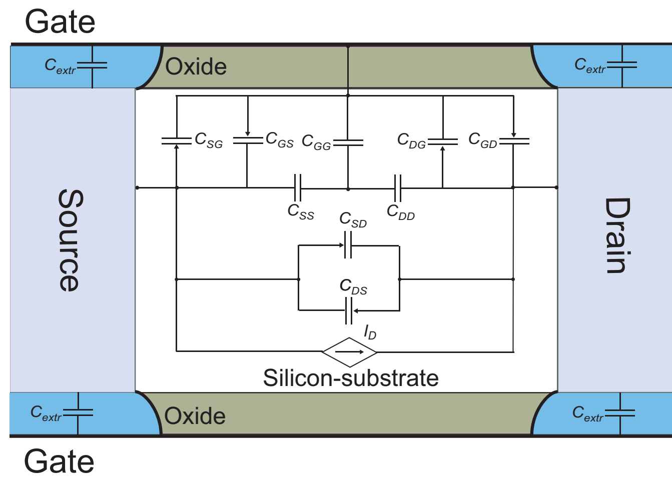

Figure 6.1: Cross section of DG and GAA device with equivalent circuit of charge conserving intrinsic capacitances, C_{XY}. Extrinsic overlap capacitances, C_{extr}, and boundaries between the intrinsic and extrinsic capacitances are indicated.

this results in extrinsic capacitances, C_{extr}, associated with the overlapping regions. The boundaries between the intrinsic and extrinsic capacitances are also indicated and will be explained in detail below.

Section 6.1 and 6.2 describe the DG and GAA models of the intrinsic trans- and self-capacitances in subthreshold and in the near/above threshold regions, respectively. The extrinsic overlap capacitances are analyzed in section 6.3.

6.1 Subthreshold - Intrinsic Capacitances

6.1.1 Double Gate

In the subthreshold regime the inter-electrode coupling dominates the behavior of the device. The intrinsic subthreshold capacitance model is therefore based on the solution of Laplace's equation, φ_2, as described in chapter 3.

If we can assume zero body charge, we know that the electric field emanating from a charge on electrode X must terminate on a charge of opposite sign on electrode Y. Therefore, the electrode charges associated with the inter-electrode coupling add up to zero charge when summed over all electrodes, due to the charge conservation principle [20].

According to Gauss' law, the total charge assigned to an electrode, is proportional to the integrated perpendicular electric field, $\mathbf{E}_\perp$, terminating on that electrode. In accordance with the thin oxide approximation, we extend the source and drain contacts through the oxide gap at the corners of the device. Applying the inter-electrode potential distribution of equation (3.9) we can then determine the charge associated with electrode X to

$$\begin{aligned} Q_X &= \varepsilon_{si} W \int_{z_{min}}^{z_{max}} \mathbf{E}_\perp dz = i\varepsilon_{si} W \int_{u_{min}}^{u_{max}} \left.\frac{d\varphi_2}{dv}\right|_{v\to 0} du \\ &= \frac{i\varepsilon_{si}W}{\pi} \left[\begin{array}{l} V_G \ln\left(\frac{(u-1)(ku+1)}{(u+1)(ku-1)}\right) + \\ V_S \ln\left(\frac{u+1}{ku+1}\right) + V_D \ln\left(\frac{ku-1}{u-1}\right) \end{array} \right] \Bigg|_{u_{min}}^{u_{max}} \end{aligned} \tag{6.1}$$

where $V_G = V_{gs} - V_{FB}$ is the difference between the gate-source voltage and the flat band voltage, $V_S = V_{bi}$ is the built in voltage of the source electrode and $V_D = V_{bi} + V_{ds}$ is the sum of the built in voltage and the drain-source voltage. In equation (6.1) we made the following substitution of variables to

perform the integral over $\mathbf{E}_\perp$

$$\mathbf{E}_\perp dz = -\frac{d\varphi_{2\perp}}{dz}dz = -\lim_{v\to 0}\frac{d\varphi_2/dv}{dz/dv}\frac{dz}{du}du = i\left.\frac{d\varphi_2}{dv}\right|_{v\to 0} du \tag{6.2}$$

where we used the relationship $\left.\frac{dz/du}{dz/dv}\right|_{v\to 0} = -i$. The limits of integration, (z_{min}, z_{max}) or (u_{min}, u_{max}), in (6.1) are the lower and upper extremities of the electrode, X, to which the charge is to be assigned. As we consider symmetrical gate-biasing, the calculation of the charge associated with the gate, Q_G, must include both gate contacts. Due to symmetry this is solved by applying (u_{min}, u_{max}) corresponding to the gate 1 contact in equation (6.1), and multiply the result by 2.

The thin oxide approximation of equation (6.1), deviates significantly from numerical simulations. Therefore, a more accurate treatment of the boundary potentials across the four oxide gaps is required, and we apply the corner correction, based on the one-corner conformal mapping, as described in section 3.2.4.

The major contribution to the intrinsic capacitances will still be given by expression (6.1), using the appropriate integration limits as discussed below. In addition the minor, but still significant contribution from the four oxide gaps must be included, and a detailed description of the calculation of these contributions to Q_X and C_{XY} is given in annex C.

For determining the charge associated with the drain (Q_D) and source (Q_S) electrodes, the integration runs from $y = t'_{ox}$ to $t_{si} + t'_{ox}$ for $x = \pm\frac{L}{2}$, respectively, or between the corresponding coordinates on the u-axis of the four-corner (u, iv)-plane (see figure 3.1). The latter are obtained from the Schwarz-Christoffel transform in equation (3.1).

For the gate electrodes (Q_G), we notice from the right plot of figure 3.5 that the charges close to the corners, between the bold solid and dashed lines, correspond to field lines that terminate on the sides of the source/drain electrodes. Therefore, in order to preserve intrinsic total charge neutrality, these charges should be excluded and assigned to the extrinsic capacitances. From the one-corner analysis in section 3.2.4, we find that the integration of the intrinsic gate charge should run between $x = -\frac{L}{2} + x_0$ and $\frac{L}{2} - x_0$ for the two gates, where $x_0 = 0.339t'_{ox}$, or between the corresponding coordinates along the u-axis.

The capacitances are calculated by differentiating the electrode charges with respect to the various electrode potentials in accordance with equation (2.15). We note that Q_X is a linear function in V_Y, which means that these capacitances are bias independent. Due to symmetry and charge conservation, we

find that $C_{GS} = C_{GD} = C_{SG} = C_{DG} = \frac{C_{GG}}{2}$, $C_{DS} = C_{SD}$, and $C_{SS} = C_{DD}$, in the subthreshold regime where the inter-electrode contribution is dominant. For zero drain biasing, $V_{ds} = 0$V, these relationships are valid in all regions of operation [49][50].

The modeled inter-electrode capacitances at different device lengths are compared to numerical simulations in figure 6.2. The length of the source and drain electrodes and the oxide thickness are held constant, i.e. $t_{si} = 12$nm and $t_{ox} = 1.6$nm, and we observe that the source and drain self-capacitances, C_{SS} and C_{DD} are not noticeably affected by the change in gate length. As expected we also observe that the capacitances associated with the gate, the red and blue curves, increases for increasing gate lengths until they flatten out at $L \approx 30-35$nm. This concurs with, C_{DS} and C_{SD}, approaching zero, and can be considered the long channel limit above which short channel effects are no longer significant. Note that the capacitances are given in femto-farad/μm.

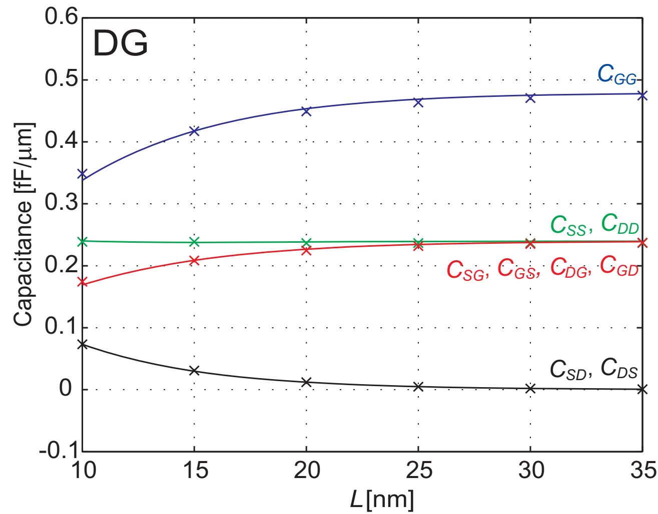

Figure 6.2: Modeled intrinsic subthreshold capacitances (lines) plotted as a function of DG device length. Oxide and substrate thicknesses are held constant, $t_{si} = 12$nm and $t_{ox} = 1.6$nm. Model is bias independent. Numerical simulations (symbols) were carried out at $V_{ds} = 0$V and $V_{gs} = -0.2$V.

6.1.2 Gate-All-Around MOSFET

In section 3.3 we introduced a technique for mapping the 2D Laplace solution, φ_2', of the DG device into the longitudinal cross-section through the central axis of the GAA MOSFET. The central axis divides the longitudinal cross-section in two parts of symmetrical electrostatics. Considering one of these radial surfaces, it must be rotated 360° about the central axis to cover the cylindrical volume, as illustrated in figure 6.3.

The approximate charge associated with the cylindrical gate contact is then given by

$$Q_G = i\varepsilon_{si} 2\pi \left(r_{si} + \frac{r'_{ox}}{2} \right) \int_{u_{min}}^{u_{max}} \left. \frac{d\varphi_2'}{dv} \right|_{v \to 0} du \tag{6.3}$$

where φ_2' is the GAA inter-electrode potential of the cross-section given in equation (3.22). The factor $2\pi\left(r_{si} + \frac{r'_{ox}}{2}\right)$ corresponds to the 360° rotation of the radial surface about the central axis. Due to the cylindrical geometry, the density of the electric field lines through the insulator will decrease, moving from the silicon-insulator interface to the gate contact. This effect is not correctly accounted for in the quasi-3D solution applied, and to compensate for this deficiency we use the electric field at the center of the insulator, $\frac{r'_{ox}}{2}$, to estimate the gate charge, Q_G.

The charge associated with the circular source and drain contacts is given by

$$Q_{S/D} = 2\pi i \varepsilon_{si} \int_0^{r_{si}} r \mathbf{E}_{\perp GAA} dr \tag{6.4}$$

The perpendicular electric field terminating at the source and drain contacts

Figure 6.3: Radial cross-section of the GAA MOSFET. This surface must be rotated 360° about the central axis to cover the cylindrical volume.

is calculated analytically in accordance with

$$\mathbf{E}_{\perp GAA} = -\lim_{v \to 0} \left(\frac{d\varphi_2'}{dv} \right) / \left(\frac{dz}{dv} \right) \tag{6.5}$$

where the numerator is given by

$$\lim_{v \to 0} \frac{d\varphi_2'}{dv} = \frac{1-k'}{\pi} \left[\frac{V_D}{(u-1)(k'u-1)} + \frac{V_S}{(u+1)(k'u+1)} - \frac{2V_G(k'u^2+1)}{(u^2-1)(k'^2u^2-1)} \right] \tag{6.6}$$

and the derivative of the transform of the extended DG device along the boundary, $v = 0$, is given by

$$\lim_{v \to 0} \frac{dz'}{dv} = \frac{iL'}{2\sqrt{1-u^2}\sqrt{1-k'^2u^2}\mathrm{K}(k')} \tag{6.7}$$

In accordance with the procedure described in section 3.3, this calculation of the extended DG device can be mapped into the GAA MOSFET by compressing it uniformly in the longitudinal direction using the scaling factor $\lambda_{GAA}/\lambda_{DG}$, i.e. $\frac{dz}{dv} = \frac{\lambda_{GAA}}{\lambda_{DG}} \frac{dz'}{dv}$. The perpendicular electric field along the source and drain contact can then be found by inserting equation (6.6) and the downscaled (6.7) into (6.5).

The integral of equation (6.4) is then calculated numerically to estimate Q_S and Q_D. The capacitances C_{SY} and C_{DY}, where $Y = S, D, G$, are then found by carrying out a numerical differentiation of Q_S and Q_D with respect to the source, drain and gate voltages.

The modeled subthreshold GAA capacitances at different device lengths are compared to numerical simulations in figure 6.4. All radial dimensions are held constant, and we observe that the source and drain self-capacitances, C_{SS} and C_{DD} are not noticeably affected by the change in gate length. The capacitances associated with the gate, the red and blue curves, increases for small gate lengths, however the change is not as pronounced as for the DG in figure 6.2. We also observe a small rise in, C_{DS} and C_{SD}, for small gate lengths. Relatively, the coupling between the source and drain electrode, which give rise to short channel effects, is significantly smaller for the GAA compared to the DG MOSFET. Note that the capacitances are given in atto-farad.

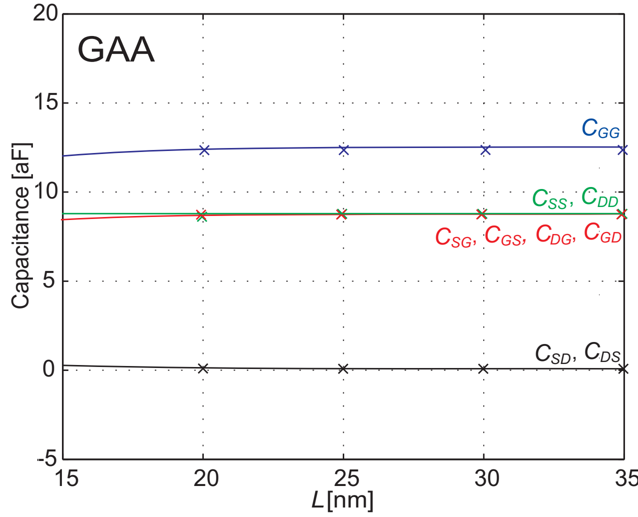

Figure 6.4: Modeled intrinsic subthreshold capacitances (lines) plotted as a function of GAA device length. Radial dimensions are held constant, r_{si} = 6nm and t_{ox} = 1.6nm. Model is bias independent. Numerical simulations (symbols) were carried out at V_{ds} = 0V and V_{gs} = −0.2V.

6.2 Near and Above Threshold - Intrinsic Capacitances

In the near and above threshold regimes, both the inter-electrode coupling and the inversion charge will contribute to the capacitance. The former is bias independent, as pointed out in the previous section, and will pay its constant contribution to the capacitances in all operating regimes. The contribution of the inversion charges, on the other hand, will steadily become more significant to the intrinsic capacitances as the gate biasing increases.

6.2.1 Double Gate MOSFET

We use the self-consistent device electrostatics, from chapter 4, to determine the inversion charge distribution associated with the electrodes. From the modeled silicon-insulator interface potential, $\varphi_1(x, t'_{ox})$, we can estimate the perpendicular electric field at the gate contacts, $\mathbf{E}_{1\perp}(x) = -\frac{\varphi_1(x,t'_{ox})}{t'_{ox}}$. The electrode charge, Q_{G1}, associated with the body charge can then be determined as

$$Q_{G1} = 2W\varepsilon_{si}\int_{-L/2}^{L/2}\mathbf{E}_{1\perp}(x')dx' \tag{6.8}$$

The charges on the gate contact associated with the body charge is not limited to the gate length as assumed by the integration limits of equation (6.8). Some field lines emanating from the body charge will terminate on the gate contacts at $|x| > \frac{L}{2}$. The integral should, therefore, ideally run over $\mp\infty$. However, we assume that the error made by this assumption is negligible.

At source and drain, the charges may be difficult to determine precisely from the perpendicular electric field because of strong corner effects. Instead, we calculate the total body charge, $Q_B = q\int_{-L/2}^{L/2} n_s(x)dx$, where n_s is the charge sheet density, ref. equation (2.10). We then divide the device in two equal parts separated by the G-G symmetry line, where Q_{BS} is the body charge in the half closest to source and Q_{BD} the body charge closest to drain.

We then split the gate charge into two terms, $Q_{G1} = Q_{G1S} + Q_{G1D}$. The first term, Q_{G1S}, is associated with source, i.e. integral runs from $-\frac{L}{2}$ to 0 in equation (6.8), and the second term, Q_{G1D}, is associated with drain, i.e. integral runs from 0 to $\frac{L}{2}$.

The charge associated with source and drain can then be approximated to $Q_{S1} = Q_{BS} - Q_{G1S}$ and $Q_{D1} = Q_{BD} - Q_{G1D}$. These charges are finally differentiated numerically with respect to the terminal voltages in order to determine the contribution from the body charges to the capacitances.

Figure 6.5 shows two examples of the modeled capacitances of the DG device versus V_{gs} for $V_{ds} = 0.1$V and 0.5V, covering operating conditions from deep subthreshold to strong inversion. Figure 6.6 shows the modeled capacitances as a function of V_{ds} for $V_{gs} = 0.25$V and 0.6V. The model compares quite well with the numerical simulations.

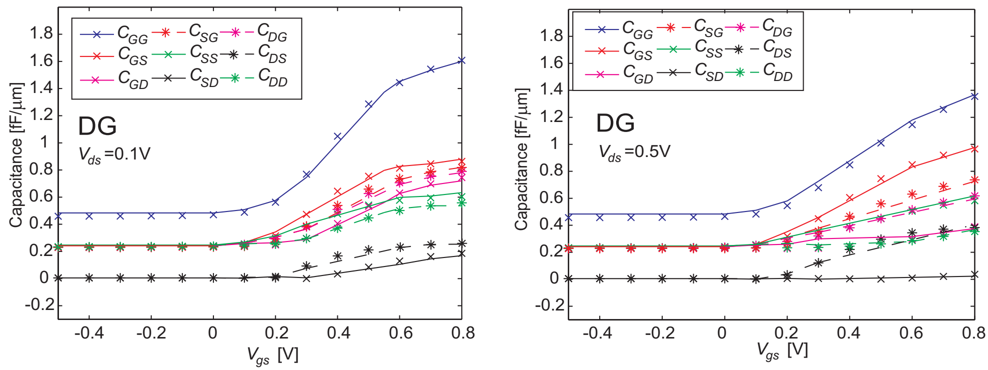

Figure 6.5: Intrinsic capacitances of DG device as a function of V_{gs}, for $V_{ds} = 0.1$V (left) and $V_{ds} = 0.5$V (right). Model is plotted with lines and numerical simulations with symbols.

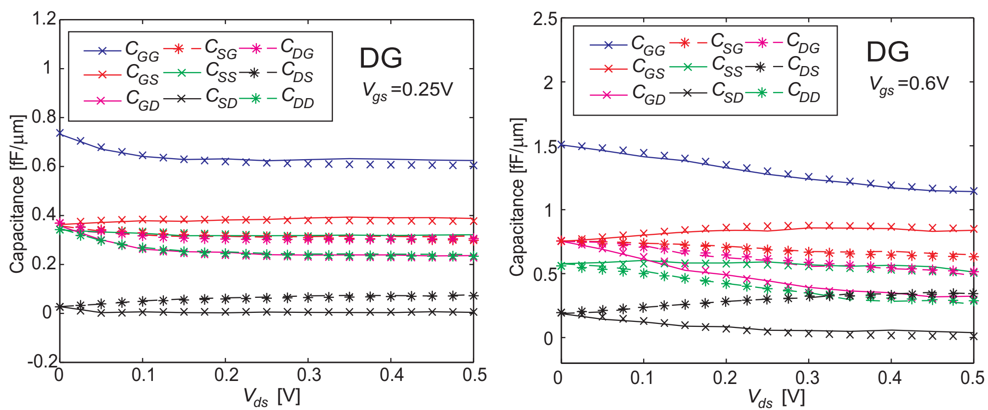

Figure 6.6: Intrinsic capacitances of DG device as a function of V_{ds}, for $V_{gs} = 0.25$V (left) and $V_{gs} = 0.6$V (right). Model is plotted with lines and numerical simulations with symbols.

6.2.2 Gate-All-Around MOSFET

The electrostatics of the GAA device, as derived in chapter 4, is the basis of the charge contribution to the intrinsic capacitances in the near and above threshold regimes. We follow a similar procedure as for the DG device, but due to the cylindrical geometry there are a few differences which are pointed out below.

The perpendicular electric field at the silicon-insulator interface can be estimated by

$$\mathbf{E}_{1\perp} = -\frac{\varphi_1(x, r_{si})}{r'_{ox}} \tag{6.9}$$

Note that the cylindrical geometry has been accounted for in the oxide thickness of r'_{ox}, ref. equation (2.2). However, due to decreasing density of field lines moving from the silicon-insulator interface to the gate contact the magnitude of $\mathbf{E}_{1\perp}$ is also decreasing. Imposing continuity of the electric field across the silicon-insulator interface, equation (6.9) represents the magnitude of the electric field at $r = r_{si}$. The gate charge, Q_{G1}, associated with the body charge is then given by

$$Q_{G1} = 2\pi r_{si}\varepsilon_{si}\int_{-L/2}^{L/2} \mathbf{E}_{1\perp}(x')dx' \tag{6.10}$$

Note that in this case, in contrast to the quasi-3D analysis based gate charge calculation in section 6.1.2, we have a proper 3D self-consistent analysis of the potential, $\varphi_1(x, r_{si})$, along the silicon-insulator interface, and the approximations of equation (6.3) are no longer necessary.

The charges associated with source and drain, Q_{S1} and Q_{D1}, respectively, are determined from the difference between the total body charge and the charges associated with gate in a similar manner as for the DG. The body charge can be determined from the integral, $Q_B = q\int n_s(x)dx$, where the charge sheet density, n_s, for cylindrical geometry is given by

$$n_s(x) = \frac{n_i^2}{N_a}2\pi\int_0^{r_{si}} r' \exp\left(\frac{\varphi(x, r') - V_F(x)}{V_{th}}\right) dr' \tag{6.11}$$

Finally, the self- and trans-capacitances are found by numerical differentiation with respect to the electrode voltages.

Figure 6.7 shows two examples of the modeled capacitances of the GAA device versus V_{gs} for V_{ds} = 0.1V and 0.5V, covering operating conditions from deep subthreshold to strong inversion. Figure 6.8 shows the modeled capacitances as a function of V_{ds} for V_{gs} = 0.25V and 0.6V. The model

compares quite well with the numerical simulations performed by the Silvaco Atlas device simulator.

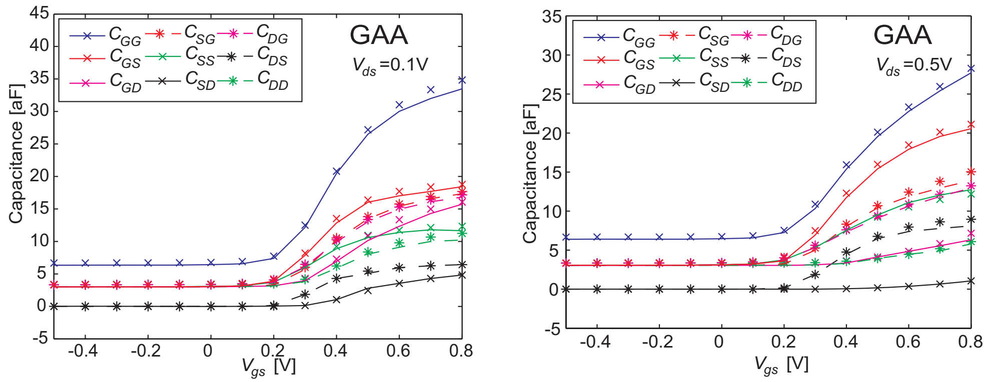

Figure 6.7: Intrinsic capacitances of GAA device as a function of V_{gs}, for V_{ds} = 0.1V (left) and V_{ds} = 0.5V (right). Model is plotted with lines and numerical simulations with symbols.

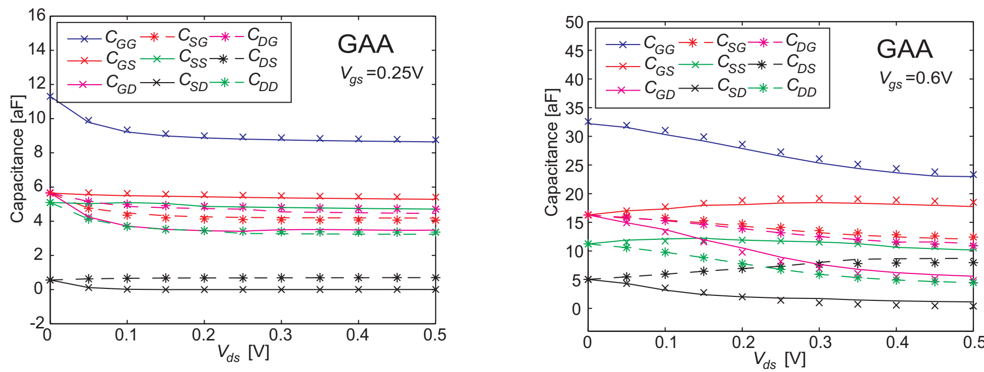

Figure 6.8: Intrinsic capacitances of GAA device as a function of V_{ds}, for V_{gs} = 0.25V (left) and V_{gs} = 0.6V (right). Model is plotted with lines and numerical simulations with symbols.

6.3 Extrinsic Overlap Capacitance

The extrinsic overlap capacitances, C_{extr}, which are indicated in figure 6.1, can be approximated as parallel plate capacitors. For the DG device the parallel plate capacitance is given by $C_{extr_{DG}} \approx \frac{\varepsilon_{ox} W d_{S/D}}{t_{ox}}$, where $d_{S/D}$ is the overlap length between the gate and the source/drain electrodes (neglecting external fringing capacitances). For the cylindrical GAA device the parallel plate approximation becomes $C_{extr_{GAA}} \approx \frac{2\pi\varepsilon_{ox} d_{S/D}}{\ln\left(1+\frac{t_{ox}}{r_{si}}\right)}$.

A more accurate analysis, however, is given by the one-corner conformal mapping procedure as described in section 3.2.4. Using $\varphi_{2_{1c}}$ of equation (3.12), Q_X per unit gate width in equation (6.1), can be calculated to

$$Q_{X_{1c}} = i\varepsilon_{si} \int_{u_{min}}^{u_{max}} \left. \frac{d\varphi_{2_{1c}}}{dv} \right|_{v\to 0} = i\frac{\varepsilon_{si}(V_G - V_{S/D})}{\pi} \ln\left(\frac{u_{max}}{u_{min}}\right) \tag{6.12}$$

Analog to the capacitance model introduced in section 2.2.5, the one-corner analysis represents a two-terminal device, with four self- and trans-capacitances of which one is independent, i.e. in the resulting 2×2 capacitance matrix all entries have equal magnitude, but cancel each other by pairwise opposite signs.

The integral of equation (6.12) can either be solved along the S/D contact or along the gate contact. As long as the contact is deep enough so that the E-field can be considered perpendicular through the oxide at the contact depth, ref. right plot of figure 3.5, these solutions will give equal results. Along the gate contact $u_{min} = -1$ (ref. figure 3.5) and u_{max} is found implicitly from the conformal mapping of the one-corner transform (ref. (3.11))

$$d_{S/D} + \frac{2t'_{ox}}{\pi}\left[\sqrt{1-u_{max}} - \frac{1}{2}\ln\left(\frac{\sqrt{1-u_{max}}+1}{\sqrt{1-u_{max}}-1}\right)\right] = 0 \tag{6.13}$$

The total extrinsic overlap capacitance contribution from the four corners of the DG device is then given by

$$C_{extr_{DG}} = 4W\frac{dQ_{X_{1c}}}{dV_{S/D}} = \frac{4W\varepsilon_{si}}{\pi}\ln\left(\frac{u_{min}}{u_{max}}\right) \tag{6.14}$$

In the case of the cylindrical GAA the total extrinsic overlap capacitance can be approximated to (ref. discussion of equation (6.3))

$$C_{extr_{GAA}} \approx 4\varepsilon_{si}\left(r_{si} + \frac{r'_{ox}}{2}\right)\ln\left(\frac{u_{min}}{u_{max}}\right) \tag{6.15}$$

Chapter 7

Conclusion

A precise modeling framework for short-channel nanoscale double-gate (DG) and cylindrical gate-all-around (GAA) MOSFETs has been presented. In the subthreshold regime the DG modeling is based on a conformal mapping analysis of the potential distribution in the device body arising from the inter-electrode capacitive coupling. The DG inter-electrode coupling can also be applied with a high degree of precision to the GAA MOSFET by performing a simple geometric scaling transformation to account for the difference in gate control in the two devices. The modeling of the drain current and the intrinsic capacitances in subthreshold are based on this inter-electrode coupling. For accurate capacitance modeling a special treatment of the insulator-gap boundary has been implemented.

Near and above threshold, where the effect of the inversion charge can no longer be neglected, self-consistent procedures invoking Poisson's equation in combination with boundary conditions and suitable modeling expressions for the potential are applied. The DG modeling is based on the 2D Poisson's equation, while the GAA is based on the 3D Poisson's equation with cylindrical symmetry. The drain current is calculated as part of the self-consistent treatment, and the intrinsic capacitances can also be extracted.

The modeled DG and GAA electrostatics, drain current and intrinsic capacitances have been compared with the Atlas device simulator from Silvaco. They all show excellent agreement with the numerical simulations in all operation regimes. A compact subthreshold GAA drift diffusion current model and a parameterized compact current model covering the full range of bias conditions are also presented. These compact models would be suitable for implementation in circuit simulators such as SPICE.

Chapter 8

Future Work

A complete compact model must have procedures for calculating currents, capacitances and noise. Here we have considered the electrostatics, drain current and intrinsic capacitances of the DG and GAA MOSFETs. There are many issues related to the compact modeling of these nanoscale devices which require additional analysis, including the ones discussed below.

8.1 Development of SPICE-Type Model

Due to the complexity of the analysis and the strict requirement of not introducing any fitting parameters, our models apply iterative procedures in order to establish the electrostatics in the near and above threshold regimes. The framework model must therefore be implemented as a preprocessing routine, from which parameters can be extracted and used in compact circuit simulation tools. This way we can meet the requirement of high computational speed of the SPICE simulator.

8.2 Noise

Noise modeling is also an important part of a compact model for nanoscale devices. Several research groups are working with this subject [63].

8.3 FinFET

Candidates for next generation device technology also include the FinFET. The framework model of the DG and GAA MOSFET may serve as a good foundation on which modeling procedures for the FinFET can be developed. The FinFET is a 3D device, for which the 2D conformal mapping cannot be directly applied. However, bearing in mind the solution for GAA in subthreshold, it is worth investigating if this 2D Laplace solution can be fitted into the FinFET as well.

8.4 Transport Mechanisms

Our modeling scheme applies the drift diffusion transport formalism with constant mobility, ignoring velocity saturation and ballistic transport mechanisms. Especially in the subthreshold regime where the inter-electrode coupling dominates the electrostatics, it may be possible to achieve compact models with more sophisticated transport formalisms.

8.5 Quantum Inversion Charge

In our modeling scheme we apply the classical Boltzmann distribution for calculating the inversion charge. With a body thickness of 12nm, we are approaching the limit where quantum effects commences to become significant. Therefore a quantized charge distribution should be analyzed.

Appendix A

Series Expansion of One-Corner Potential

A.1 Introduction

The one-corner analysis in chapter 3 applied the Schwarz-Christoffel transform (ref. equation (3.11))

$$z_{1c} = \frac{2t'_{ox}}{\pi}\left[\sqrt{w_{1c}-1} - \tan^{-1}\left(\sqrt{w_{1c}-1}\right)\right] + t'_{ox} \tag{A.1}$$

We obtained the following solution to the Laplace equation (ref. equation (3.12))

$$\varphi_{2_{1c}}\left(u_{1c}, v_{1c}\right) = \frac{1}{2}\left(V_G + V_{S/D}\right) - \frac{1}{\pi}\left(V_G - V_{S/D}\right)\tan^{-1}\left(\frac{u_{1c}}{v_{1c}}\right) \tag{A.2}$$

The potential distribution of the (u_{1c}, iv_{1c}) and (x_{1c}, y_{1c})-plane are indicated in figure 3.5. Here, we will further analyze the one-corner potential profile by carrying out a series expansion about $z_{1c} = 0$ and $z_{1c} = t'_{ox}$

A.2 Series Expansion About $z_{1c} = 0$

In this section we will analyze the potential profile about $z_{1c} = 0$ moving along the real y_{1c} axis in the z_{1c}-plane of figure 3.5. The insulator gap is therefore perpendicular to the ix_{1c}-axis at $z_{1c} = 0$, and the angle preserving property of conformal mapping requires that the same is true with respect to the u_{1c}-axis in the w_{1c}-plane at $u_{1c} = u_0 = -0.439$.

To simplify the mapping function we carry out a series expansion of the square root and the inverse tangent terms of equation (A.1) about $v_{1c} = 0$ to the first order

$$\sqrt{u_0 - 1 + iv_{1c}} \approx \sqrt{u_0 - 1} + \frac{v_{1c}}{2\sqrt{1 + |u_0|}}$$
$$\tan^{-1}\left(\sqrt{u_0 - 1 + iv_{1c}}\right) \approx \tan^{-1}\left(\sqrt{u_0 - 1}\right) - \frac{v_{1c}}{2|u_0|\sqrt{1 + |u_0|}}$$

When these series expansions are inserted in equation (A.1), we obtain the following simplified mapping, which is valid about $z_{1c} = 0$ along the real y_{1c} axis.

$$z_{1c} = y_{1c} \approx \frac{t'_{ox}}{\pi}\frac{v_{1c}}{|u_0|}\sqrt{1 + |u_0|} \tag{A.3}$$

The potential variation for small v_{1c} at $u_{1c} = u_0$ has the form

$$\begin{aligned}\varphi_{1c}(u_0, v_{1c}) &= \frac{1}{2}\left(V_G + V_{S/D}\right) - \frac{1}{\pi}\left(V_G - V_{S/D}\right)\tan^{-1}\left(\frac{-|u_0|}{v_{1c}}\right) \\ &\approx V_G - \frac{1}{\pi}\left(V_G - V_{S/D}\right)\frac{v_{1c}}{|u_0|} \end{aligned} \tag{A.4}$$

where we have used the expansion $\tan^{-1}(t) \approx \frac{\pi}{2} - \frac{1}{t}$ valid for $t \to \infty$.

Solving equation (A.3) with respect to v_{1c} and inserting this into (A.4) we obtain the following linear function of y_{1c}

$$\varphi(0, y_{1c}) \approx V_G - \left(V_G - V_{S/D}\right)\frac{y_{1c}}{t'_{ox}\sqrt{1 + |u_0|}} \tag{A.5}$$

The slope of the curve for small $\frac{y_{1c}}{t'_{ox}}$ is therefore $(1 + |u_0|)^{-1/2} \approx 0.834$. Figure A.1 shows that this first order series expansion about $z_{1c} = 0$ is quite acceptable for $\frac{y_{1c}}{t'_{ox}}$ up to 0.6 and has a maximum error of about 17% at $\frac{y_{1c}}{t'_{ox}} = 1$. The derivative of equation (A.5) is applied as boundary condition for the modeling function of the insulator gap potential of equation (3.13).

A.3 Series Expansion About $z_{1c} = t'_{ox}$

Next we carry out the series expansion about $z_{1c} = t'_{ox}$ ($w_{1c} = 1$), and due to the presence of the corner, we have to expand (A.1) with respect to

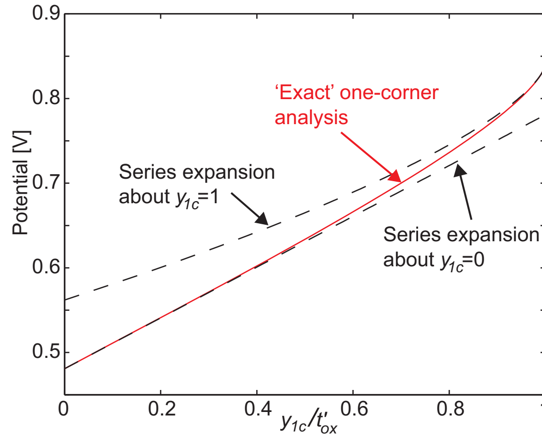

Figure A.1: The potential profile across insulator-gap of one-corner analysis compared to series expansions about $y_{1c} = 0$ and $y_{1c} = t'_{ox}$.

$\hat{w_{1c}} = u_{1c} + iv_{1c} - 1$. It turns out that this expansion has to be carried out to third order in $\sqrt{\hat{w_{1c}}}$ in order to find a non-zero result, i.e.

$$ix_{1c} + y_{1c} \approx t'_{ox} \left[1 + \frac{2}{3\pi} \left((u_{1c} - 1)^2 + v_{1c}^2\right)^{\frac{3}{4}} \exp\left(i\frac{3}{2} \tan^{-1}\left(\frac{v_{1c}}{u_{1c} - 1}\right)\right)\right] \tag{A.6}$$

Since we are moving along the real y_{1c}-axis ($ix_{1c} = 0$) in the negative direction the phase angle inside the exponent of (A.6) equals π (180°). This means that $\tan^{-1}\left(\frac{v_{1c}}{u_{1c}-1}\right) = \frac{2}{3}\pi = 120°$, and in the left plot of figure 3.5 we observe this angle of 120° between the bold dashed line and the u_{1c}-axis at $u_{1c} = 1$. The relation between u_{1c} and v_{1c} then becomes $u_{1c} - 1 = -\frac{v_{1c}}{\sqrt{3}}$, and equation (A.6) can then be rewritten

$$\left(1 - \frac{y_{1c}}{t'_{ox}}\right) = \frac{4\sqrt{2}}{3 \cdot 3^{\frac{3}{4}}\pi} v_{1c}^{\frac{3}{2}} \tag{A.7}$$

Using similar approximations as in (A.4), we find

$$\varphi_{1c}(1, v_{1c}) \approx V_{S/D} + \frac{1}{\pi}\left(V_G - V_{S/D}\right) v_{1c} \tag{A.8}$$

Inserting v_{1c} from (A.7) we get

$$\varphi_{1c}(1, v_{1c}) \approx V_{S/D} + \left(V_G - V_{S/D}\right) \left(\frac{2187}{1024 \cdot \pi^2}\right)^{\frac{1}{6}} \left(1 - \frac{y}{t'_{ox}}\right)^{\frac{2}{3}} \tag{A.9}$$

Figure A.1 shows that this series expansion about $z_{1c} = t'_{ox}$ is acceptable for $\frac{y_{1c}}{t'_{ox}}$ down to 0.9. Note also that the derivative of (A.9) at $y_{1c} = t'_{ox}$ is infinite. For completeness we also carry out a series expansion of the potential profile abount $y = t'_{ox}$ into the contact corner along the silicon insulator interface. This can be estimated by using a similar expansion of the transform about $y = t'_{ox}$. We are now moving in the negative imaginary direction in the z_{1c}-plane, and the phase angle inside the exponent of (A.6) equals $-\pi/2$. This means that $\tan^{-1}\left(\frac{v_{1c}}{u_{1c}-1}\right) = \frac{\pi}{3} = 60^\circ$, and in the left plot of figure 3.5 we observe this angle of 60° between the silicon-insulator line and the u_{1c}-axis at $u_{1c} = 1$.

Following the above procedure, we obtain $\frac{x_{1c}}{t'_{ox}} = \frac{4\sqrt{2}}{3 \cdot 3^{\frac{3}{4}}\pi} v_{1c}^{\frac{3}{2}}$. This is then inserted in the general expression of the potential in (A.2). Assuming $v_{1c} \ll 1$, we obtain

$$\varphi_{1c}\left(1, v_{1c}\right) \approx V_{S/D} + \left(V_G - V_{S/D}\right)\left(\frac{2187}{1024 \cdot \pi^2}\right)^{\frac{1}{6}}\left(\frac{x_{1c}}{t'_{ox}}\right)^{\frac{2}{3}} \qquad \text{(A.10)}$$

Note that the potential is a function of $x_{1c}^{\frac{2}{3}}$. This $\frac{2}{3}$-root relation is applied as boundary condition in the modeling expression of the silicon-insulator interface potential in the self-consistent procedure as described in section 4.2.2.

Appendix B

Corner Correction - Integrals

The modeled oxide gap potential is part of the boundary condition of the Laplace equation as given in (3.8). In this annex we will outline the procedure for calculating the contribution from these oxide gaps to 2D potential profile. For simplicity the calculation of the G1-D oxide gap contribution is shown, with the serial expansion of the elliptic integral around $u_1 = 1$. The contribution of the three other oxide gaps are calculated in a similar manner.

As seen in polynomial approximation of the oxide gap potential of equation (3.17), $\varphi_{ox}(u)$ contains one constant term C and four terms which include the integration variable on the form $(u'-1)^m$. These terms give the following integrals, denoted $\mathbf{I}_0$ for the constant term and $\mathbf{I}_m$ for the $(u'-1)^m$ terms:

$$\begin{aligned} \mathbf{I}_0 &= \frac{v}{\pi}\int_1^{1+u_{ox1}} \frac{du'}{(u-u')^2+v^2} \\ &= \frac{1}{\pi}\left[\tan^{-1}\left(\frac{u-1}{v}\right) - \tan^{-1}\left(\frac{u-u_{ox1}-1}{v}\right)\right] \end{aligned} \tag{B.1}$$

$$\begin{aligned} \mathbf{I}_{\frac{1}{2}} &= \frac{v}{\pi}\int_1^{1+u_{ox1}} \frac{(u'-1)^{\frac{1}{2}}du'}{(u-u')^2+v^2} \\ &= \frac{i}{\pi}\left[\sqrt{1-u-iv}\tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u-iv}}\right) - \right. \\ &\quad \left. \sqrt{1-u+iv}\tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u+iv}}\right)\right] \end{aligned} \tag{B.2}$$

$$
\begin{aligned}
\mathbf{I}_{\frac{3}{2}} &= \frac{v}{\pi}\int_{1}^{1+u_{ox1}} \frac{(u'-1)^{\frac{3}{2}}du'}{(u-u')^2+v^2} \\
&= \frac{1}{\pi}\Bigg[2\sqrt{u_{ox1}}v + \\
&\quad i(1-u+iv)^{3/2}\tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u+iv}}\right) \\
&\quad -i(1-u-iv)^{3/2}\tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u-iv}}\right)\Bigg]
\end{aligned} \tag{B.3}
$$

$$
\begin{aligned}
\mathbf{I}_{\frac{5}{2}} &= \frac{v}{\pi}\int_{1}^{1+u_{ox1}} \frac{(u'-1)^{\frac{5}{2}}du'}{(u-u')^2+v^2} \\
&= \frac{1}{3\pi}\Bigg[2\sqrt{u_{ox1}}(u_{ox1}+6u-6)v + \\
&\quad 3i(1-u-iv)^{5/2}\tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u-iv}}\right) - \\
&\quad 3i(1-u+iv)^{5/2}\tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u+iv}}\right)\Bigg]
\end{aligned} \tag{B.4}
$$

$$
\begin{aligned}
\mathbf{I}_{3} &= \frac{v}{\pi}\int_{1}^{1+u_{ox1}} \frac{(u'-1)^{3}du'}{(u-u')^2+v^2} \\
&= \frac{1}{2\pi}\Bigg[u_{ox1}(u_{ox1}+4u-4)v - \\
&\quad v\left(v^2-3(u-1)^2\right)\ln\left(\frac{(u_{ox1}-u+1)^2+v^2}{(u-1)^2+v^2}\right) - \\
&\quad 2(u-1)\left((u-1)^2-3v^2\right)\times \\
&\quad \left(\tan^{-1}\left(\frac{u-u_{ox1}-1}{v}\right)-\tan^{-1}\left(\frac{u-1}{v}\right)\right)\Bigg]
\end{aligned} \tag{B.5}
$$

Here u_{ox1} is the oxide thickness of the G1-D gap transformed to the (u, iv)-plane. In accordance with (3.15), (3.17) and (B.1)-(B.5) the G1-D-gap's contribution to the Laplace inter-electrode potential can be written as

$$\varphi_{LG1-D}(u,v) = \frac{8A\mathbf{I}_3}{(K(k))^6(1-k^2)^3} + \frac{BL}{\sqrt{2(1-k^2)}K(k)} \times \left[\mathbf{I}_{\frac{1}{2}} + \frac{(5k^2-1)\mathbf{I}_{\frac{3}{2}}}{12(1-k^2)} + \Gamma\mathbf{I}_{\frac{5}{2}}\right] + C\mathbf{I}_0 \tag{B.6}$$

Similarly the contribution from the three other corners, i.e. G1-S, G2-D and G2-S, must be calculated.

Appendix C

Corner Correction - Capacitance

The modeled oxide gap potential is part of the boundary condition of the Laplace equation as given in (3.8). In this annex we will outline the procedure for calculating the contribution from these oxide gaps to the trans- and self-capacitances, C_{XY}.

As previously defined, Q_X is the charge which can be associated with electrode X, which is given by

$$Q_X = \varepsilon_{Si} \int_{u_{min}}^{u_{max}} \left. \frac{\partial \varphi_2(u,v)}{\partial v} \right|_{v \to 0} du \tag{C.1}$$

where u_{min} and u_{max} are the lower and upper limits of the X-contact to which the charge should be associated.

For simplicity we calculate the contribution of the G1-D oxide gap as an example, with the serial expansion of the elliptic integral around $u_1 = 1$. Based on the integrals, $\mathbf{I}_m$, found in the previous annex, ref. equations (B.1)-(B.5), we can calculate the charge contributions to Q_X in accordance with equation (C.1).

$$Q_{X0} = \varepsilon_{Si} \int_{u_{min}}^{u_{max}} \left. \frac{\partial \mathbf{I}_0}{\partial v} \right|_{v \to 0} du = \frac{\varepsilon_{Si}}{\pi} \ln \left(\frac{u - 1 - u_{ox1}}{u - 1} \right) \Bigg|_{u=u_{min}}^{u=u_{max}} \tag{C.2}$$

$$\begin{aligned} Q_{X\frac{1}{2}} &= \varepsilon_{Si} \int_{u_{min}}^{u_{max}} \left. \frac{\partial \mathbf{I}_{\frac{1}{2}}}{\partial v} \right|_{v \to 0} du \\ &= -\frac{2\varepsilon_{Si}}{\pi} \sqrt{1-u} \tan^{-1} \left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u}} \right) \Bigg|_{u=u_{min}}^{u=u_{max}} \end{aligned} \tag{C.3}$$

$$\begin{aligned} Q_{X\frac{3}{2}} &= \varepsilon_{Si} \int_{u_{min}}^{u_{max}} \left.\frac{\partial \mathbf{I}_{\frac{3}{2}}}{\partial v}\right|_{v\to 0} du \\ &= \frac{2\varepsilon_{Si}}{\pi} \left(\sqrt{u_{ox1}} u + (1-u)^{3/2} \tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u}} \right) \right) \Bigg|_{u=u_{min}}^{u=u_{max}} \end{aligned} \tag{C.4}$$

$$\begin{aligned} Q_{X\frac{5}{2}} &= \varepsilon_{Si} \int_{u_{min}}^{u_{max}} \left.\frac{\partial \mathbf{I}_{\frac{5}{2}}}{\partial v}\right|_{v\to 0} du \\ &= \frac{\varepsilon_{Si}}{3\pi} \Bigg[\sqrt{u_{ox1}} \left(6u^2 + 2u(u_{ox1} - 6) \right) - \\ &\qquad 6(1-u)^{5/2} \tan^{-1}\left(\frac{\sqrt{u_{ox1}}}{\sqrt{1-u}} \right) \Bigg] \Bigg|_{u=u_{min}}^{u=u_{max}} \end{aligned} \tag{C.5}$$

$$\begin{aligned} Q_{X3} &= \varepsilon_{Si} \int_{u_{min}}^{u_{max}} \left.\frac{\partial \mathbf{I}_{\frac{5}{2}}}{\partial v}\right|_{v\to 0} du \\ &= \frac{\varepsilon_{Si}}{2\pi} \Bigg[u_{ox1} u \left(2u + u_{ox1} - 4 \right) + \\ &\qquad +2(u-1)^3 \ln\left(\frac{u - u_{ox1} - 1}{u - 1} \right) \Bigg] \Bigg|_{u=u_{min}}^{u=u_{max}} \end{aligned} \tag{C.6}$$

Here the integration limits, $u = u_{min}$ and $u = u_{max}$, correspond to the lower and upper limits of the X-electrode to which the charge should be associated, ref. (C.1). The constant terms, which vanish when inserting the upper and lower integration limits, have been omitted to simplify the above results.

Finally we can write the G1-D-gap contribution to the charge associated with the X-electrode as

$$\begin{aligned} Q_{XG1-D} &= A \frac{8 Q_{X3}}{(K(k))^6 (1-k^2)^3} + C Q_{X0} + \\ &\quad B \frac{L}{\sqrt{2(1-k^2)} K(k)} \left[Q_{X\frac{1}{2}} + \frac{(5k^2 - 1) Q_{X\frac{3}{2}}}{12(1-k^2)} + \Gamma Q_{X\frac{5}{2}} \right] \end{aligned} \tag{C.7}$$

Where A, B and C are given in equation (3.13) and Γ in (3.16). The capacitance C_{XY} is then given by the differentiation in equation (2.15). As the parameters A, B and C of equation (C.7) depend linearly on the terminal voltages, this capacitance contribution is bias independent. Similarly the capacitance contribution from the three other corners must be calculated.

Appendix D

Differentiation of Inter-Electrode Potential

The S-D symmetry line of the DG device maps into a semi-circle with radius $\frac{1}{\sqrt{k}}$ about the origin of the (u, iv) plane as shown in figure 3.1. The Schwarz-Christoffel transform of equation (3.1) and the inter-electrode potential distribution of equation (3.9) are here combined to find the first and second derivative of the Laplace potential along this symmetry line. At the end the second derivative along the gate-to-gate symmetry line is also derived.

D.1 First Derivative

Along the S-D symmetry line, v can be expressed in terms of u, i.e. $v = \sqrt{\frac{1}{k} - u^2}$, and the mapping function of equation (3.1) can be rewritten to [42]

$$x = \frac{L}{2}\frac{\mathrm{F}\left(\frac{2\sqrt{k}}{1+k}, \sqrt{k}u\right)}{\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right)}, \quad y = t'_{ox} + \frac{t_{si}}{2} \tag{D.1}$$

The derivative of the transform with respect to u along the S-D symmetry line can then be calculated to

$$\left.\frac{dx}{du}\right|_{v=\sqrt{\frac{1}{k}-u^2}} = \frac{\sqrt{k}L}{2\sqrt{1-ku^2}\sqrt{1-\left(\frac{2ku}{1+k}\right)^2}\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right)} \tag{D.2}$$

Similarly the inter-electrode potential of equation (3.9) can be evaluated along the S-D symmetry line by replacing v with $v = \sqrt{\frac{1}{k} - u^2}$. This potential

differentiated with respect to u is given by

$$\left.\frac{d\varphi_2}{du}\right|_{v=\sqrt{\frac{1}{k}-u^2}} = \frac{(1-k)\left[(1+k+2ku)V_D - 4kuV_G - (1+k-2ku)V_S\right]}{\pi\sqrt{\frac{1}{k}-u^2}\left((1+k)^2-4k^2u^2\right)} \tag{D.3}$$

The inter-electrode contribution to the electric field along the S-D symmetry line, $\mathbf{E}_2 = -\frac{d\varphi_2}{dx}$, is found by dividing (D.3) with (D.2). The perpendicular E-field at center of the source and drain contacts, ref. equation (4.7) and (4.8), are found by evaluating $\mathbf{E}_2$ at $u = \mp\frac{1}{\sqrt{k}}$, respectively.

The position of the inter-electrode potential extremum along the S-D symmetry line can be found by solving equation $\frac{d\varphi_2}{du} = 0$, which has a simple analytical solution

$$u_{ext} = \frac{-(1+k)(V_D - V_S)}{2k(V_D - 2V_G + V_S)} \tag{D.4}$$

In the subthreshold regime where the effect of the charge contribution to the electrostatics can be neglected, this gives a good estimate of the position of the energy barrier between source and drain.

D.2 Second Derivative

The second derivative of the inter-electrode potential is given by

$$\frac{d^2\varphi_2}{dx^2} = \frac{d}{dx}\left(\frac{\frac{d\varphi_2}{du}}{\frac{dx}{du}}\right) = \frac{du}{dx}\frac{d}{du}\left(\frac{\frac{d\varphi_2}{du}}{\frac{dx}{du}}\right) = \frac{\frac{d^2\varphi_2}{du^2}}{\left(\frac{dx}{du}\right)^2} - \frac{d\varphi_2}{du}\frac{\frac{d^2x}{du^2}}{\left(\frac{dx}{du}\right)^3} \tag{D.5}$$

The second derivative of the transform along the S-D symmetry line is calculated to

$$\left.\frac{d^2x}{du^2}\right|_{v=\sqrt{\frac{1}{k}-u^2}} = \frac{Lk^{\frac{3}{2}}u\left(1+k(6+k-8ku^2)\right)}{2(1-ku^2)^{\frac{3}{2}}\left((1+k)^2-4k^2u^2\right)\sqrt{1-\left(\frac{2ku}{1+k}\right)^2}\,\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right)} \tag{D.6}$$

and the second derivative of the potential with respect to u is given by

$$\begin{aligned}\left.\frac{d^2\varphi_2}{du^2}\right|_{v=\sqrt{\frac{1}{k}-u^2}} = -&\frac{k(1-k)}{\pi\sqrt{\frac{1}{k}-u^2}(1-ku^2)\left(1+k(2+k-4ku^2)\right)^2}\times\\ &\Big[(1+k+2ku)^2(-2-(1+k)u+4ku^2)V_D+\\ &(1+k-2ku)^2(-2+(1+k)u+4ku^2)V_S+\\ &4(1+k(2+k+4ku^2-8k^2u^4))V_G\Big]\end{aligned} \tag{D.7}$$

When equation (D.2), (D.3), (D.6) and (D.7) are inserted in (D.5), the final expression of the curvature along the S-D symmetry line simplifies to

$$\left.\frac{d^2\varphi_2}{dx^2}\right|_{y=t'_{ox}+\frac{t_{si}}{2}} = \frac{8(1-k)k\sqrt{\frac{1}{k}-u^2}\left(\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right)\right)^2}{L^2\pi(1+k)\left((1+k)^2-4k^2u^2\right)} \times \left[(1+k+2ku)V_D+(1+k-2ku)V_S-2(1+k)V_G\right] \tag{D.8}$$

In accordance with Laplace equation the curvature in the y-direction equals the negative of the curvature in the x-direction. Therefore, we can also find $\frac{d^2\varphi_2}{dy^2} = -\frac{d^2\varphi_2}{dx^2}$ along the S-D symmetry line from equation (D.8).

The curvature along the G-G symmetry line ($u = 0$), can be derived in a similar manner rewriting the mapping function to [42]

$$x = 0, \quad y = (t_{si}+2t'_{ox})\,\frac{\mathrm{F}\left(\sqrt{1-k^2}, \frac{v}{\sqrt{1+v^2}}\right)}{\mathrm{K}\left(\sqrt{1-k^2}\right)} \tag{D.9}$$

Following the same steps as above we obtain

$$\left.\frac{d^2\varphi_2}{dy^2}\right|_{x=0} = -\frac{v(1-k)(1+k)^2(1+kv^2)\left(V_D-2V_G+V_S\right)\left(\mathrm{K}\left(\sqrt{1-k^2}\right)\right)^2}{\pi\left(2t'_{ox}+t_{si}\right)^2(1+v^2)(1+k^2v^2)} \tag{D.10}$$

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